

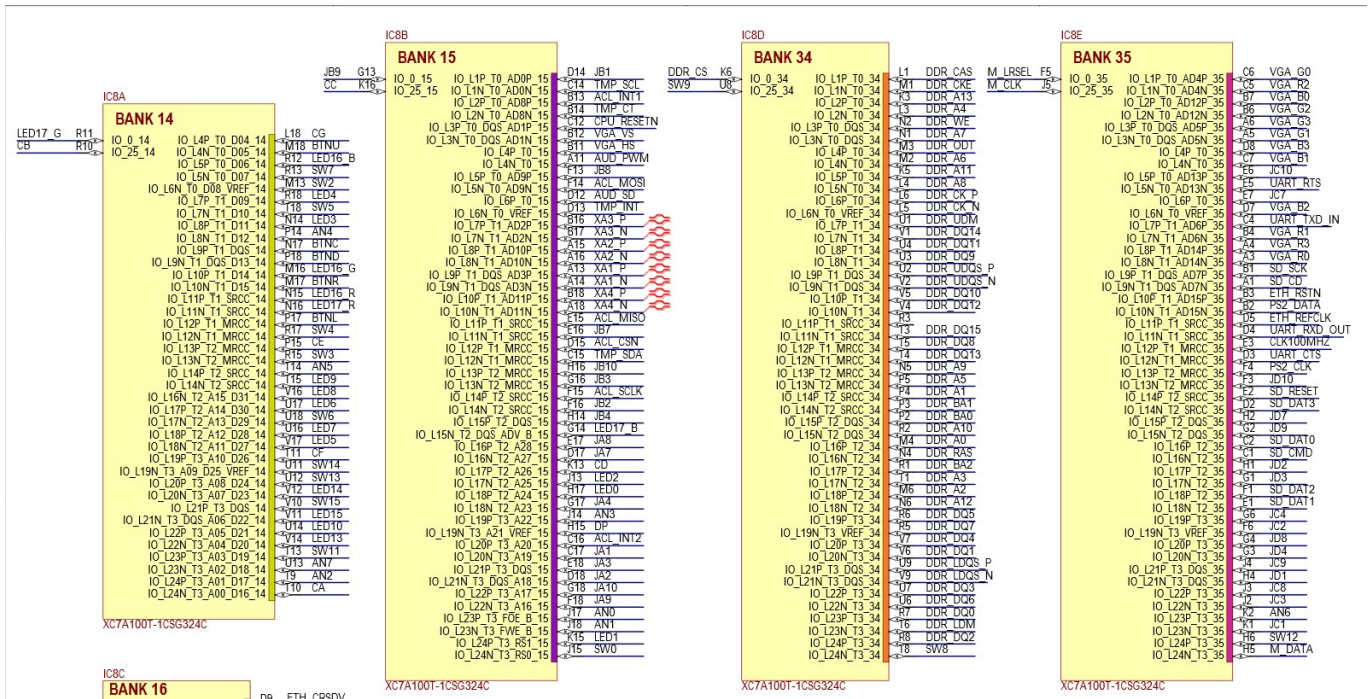
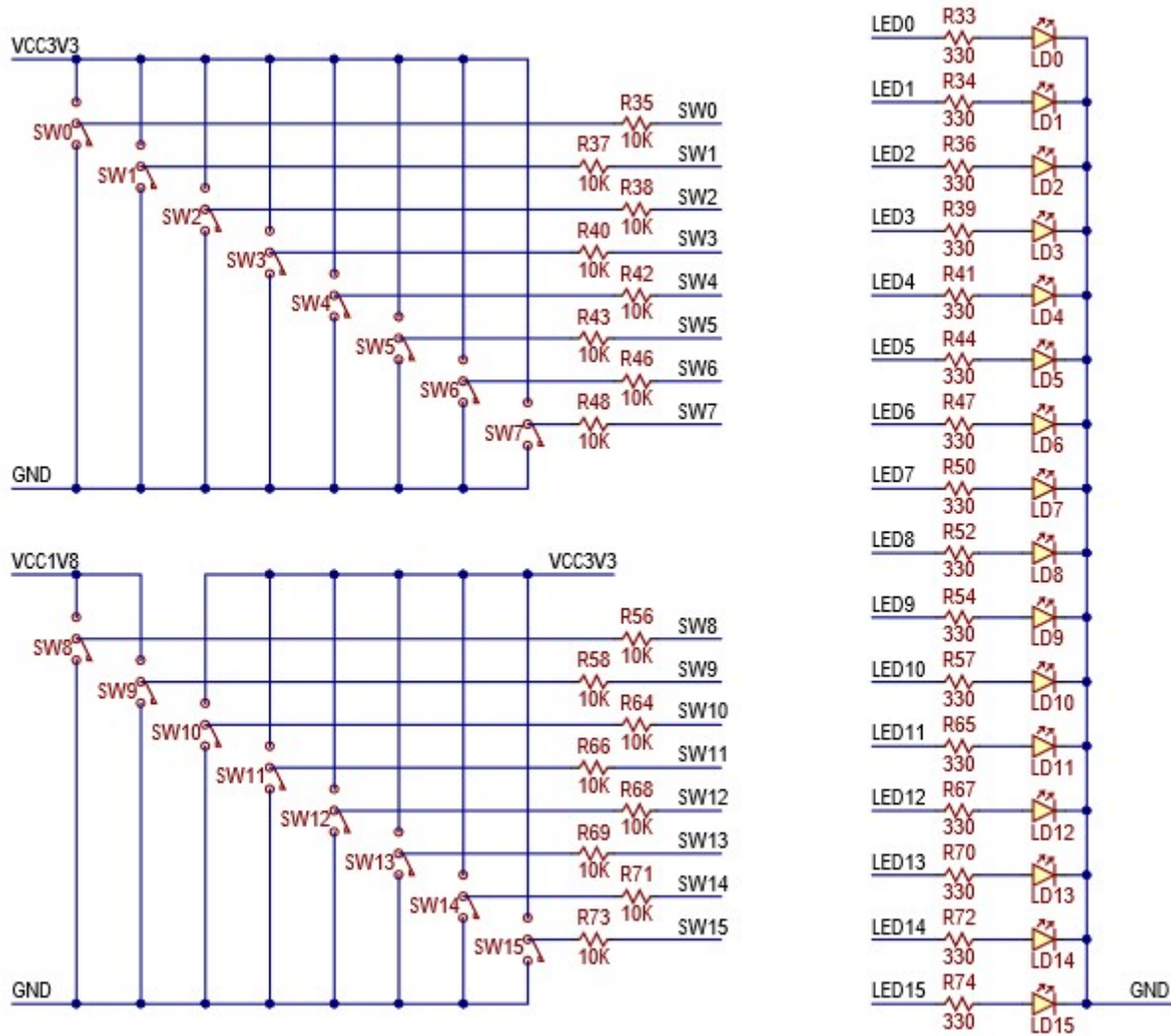
# Digital electronics 1 - 03 vivado

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## Multiplexer 4-to-1

### Table with connections

Connector	Pin	Program
SW0	J15	a_i
SW1	L16	a_i
SW2	M13	b_i
SW3	R15	b_i
SW4	R17	c_i
SW5	T18	c_i
SW6	U18	d_i
SW7	R13	d_i
SW14	U11	sel_i
SW15	V10	sel_i
LED0	H17	f_o
LED1	K15	f_o



```

architecture Behavioral of mux_2bit_4to1 is
begin

    f_o <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;

end architecture Behavioral;

```

### Source code of testbench file

```

p_stimulus : process
begin
    -- Report a note at the beginning of stimulus process
    report "Stimulus process started" severity note;

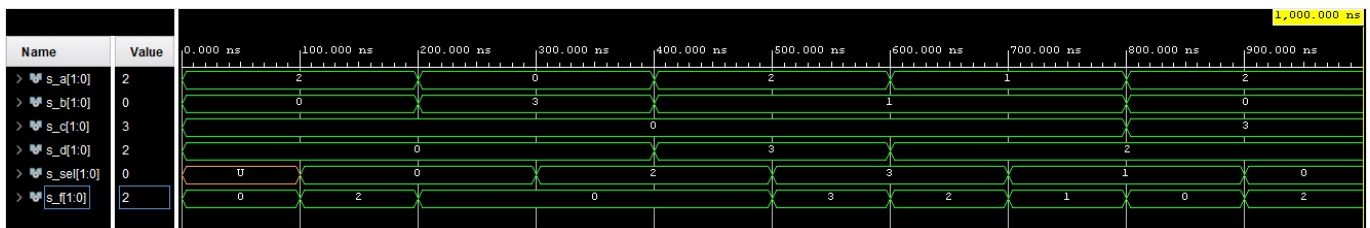
    s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "10"; wait for 100 ns;
    s_sel <= "00"; wait for 100 ns;

    s_d <= "00"; s_c <= "00"; s_b <= "11"; s_a <= "00"; wait for 100 ns;
    s_sel <= "10"; wait for 100 ns;
    s_d <= "11"; s_c <= "00"; s_b <= "01"; s_a <= "10"; wait for 100 ns;
    s_sel <= "11"; wait for 100 ns;
    s_d <= "10"; s_c <= "00"; s_b <= "01"; s_a <= "01"; wait for 100 ns;
    s_sel <= "01"; wait for 100 ns;
    s_d <= "10"; s_c <= "11"; s_b <= "00"; s_a <= "10"; wait for 100 ns;
    s_sel <= "00"; wait for 100 ns;

    -- Report a note at the end of stimulus process
    report "Stimulus process finished" severity note;
    wait;
end process p_stimulus;

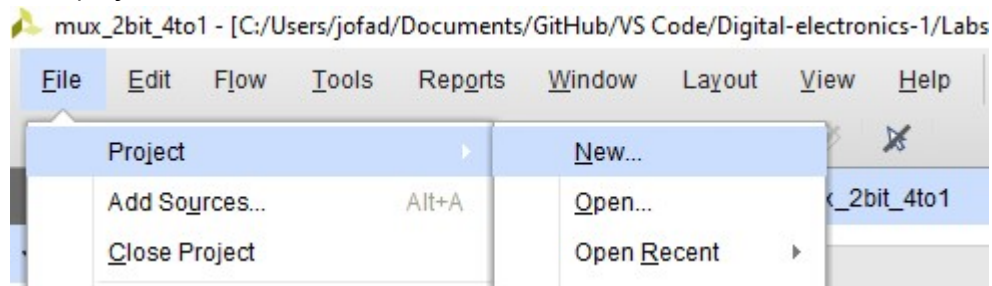
```

### Screenshot with simulated time waveforms

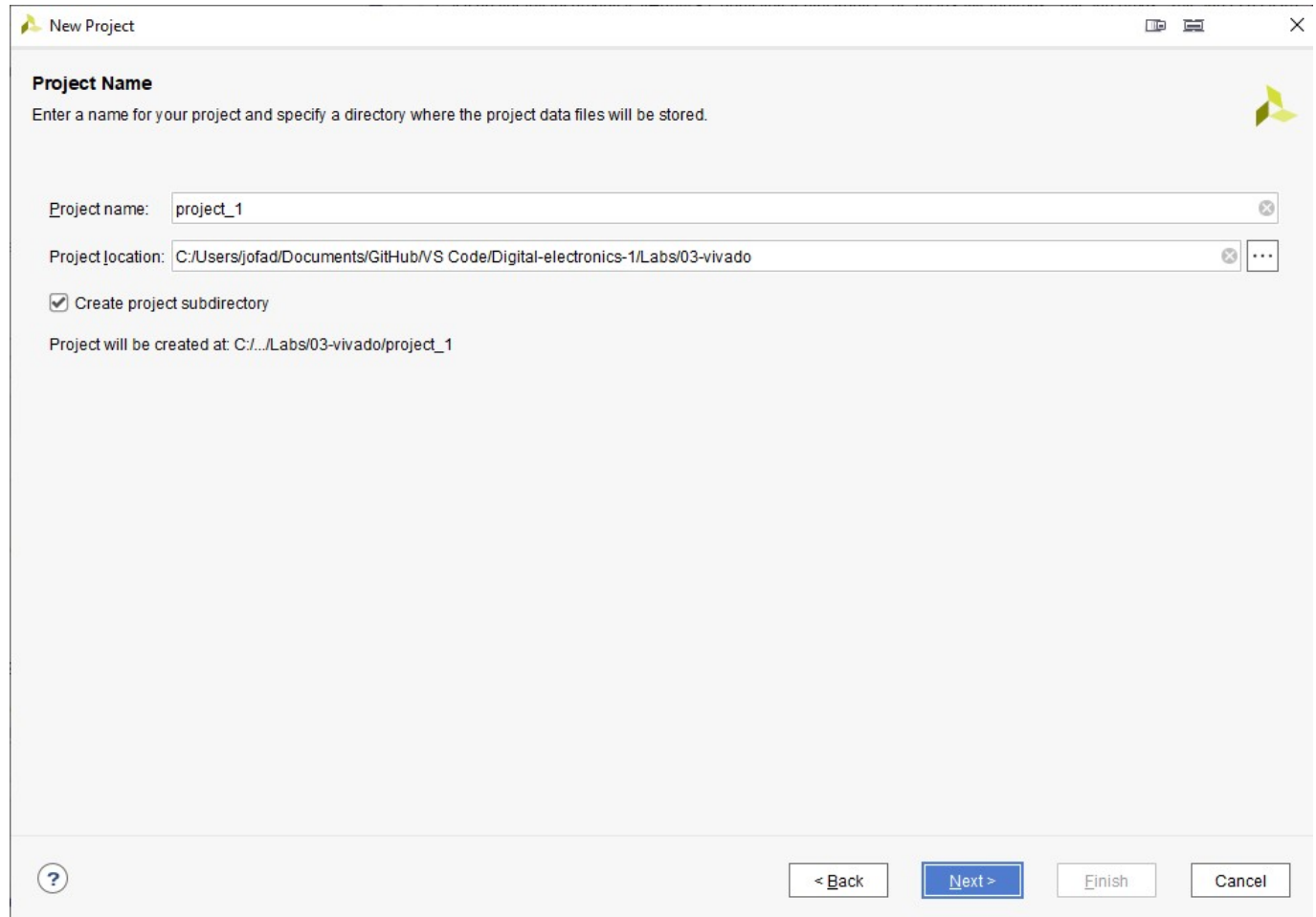


## Vivado tutorial

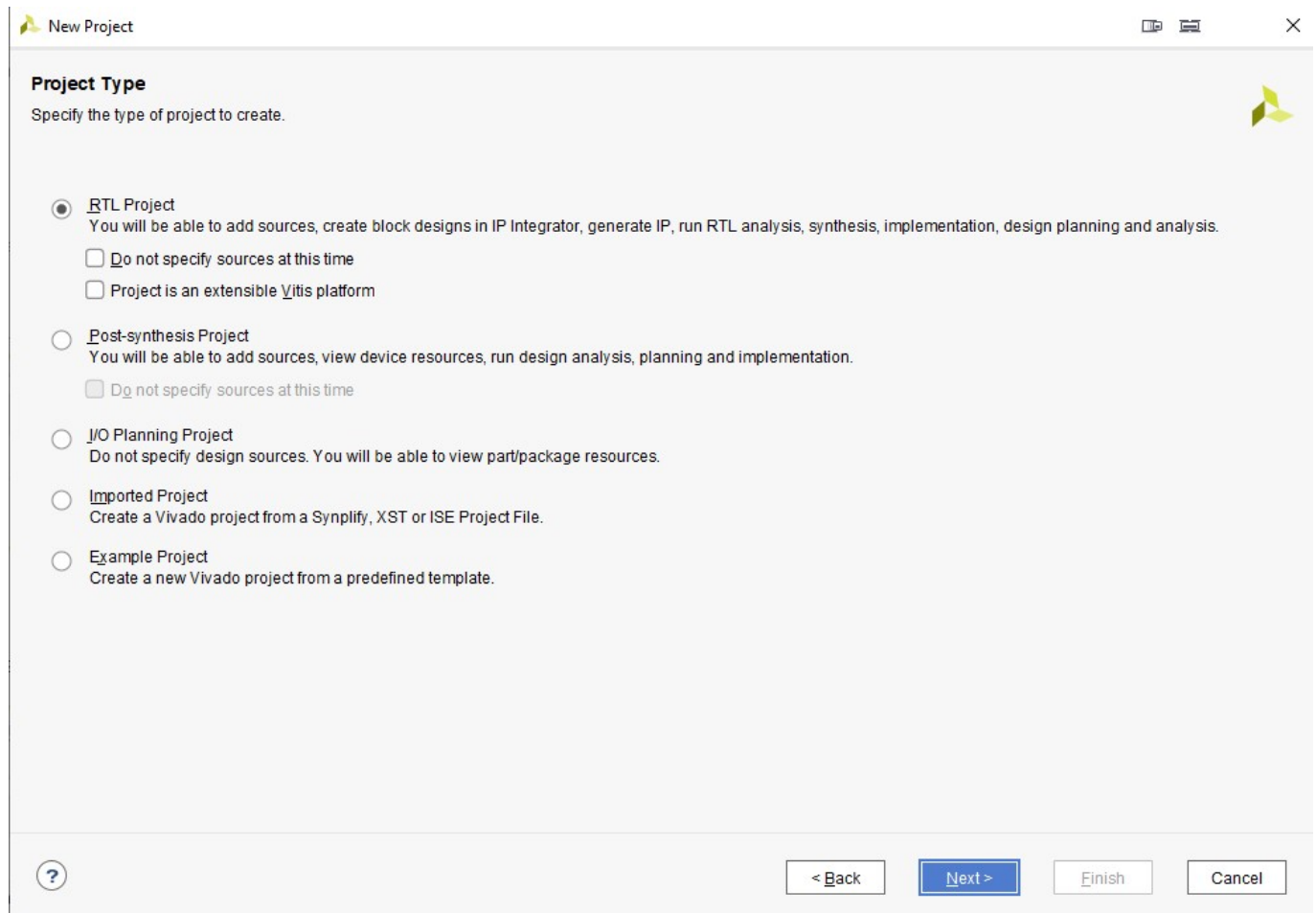
Click project and new, next window click next



Type your project name and choose directory to save it



Choose RTL Project



**New Project**

**Project Type**  
Specify the type of project to create.

☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ Project is an extensible Vitis platform



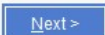


☐ **Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

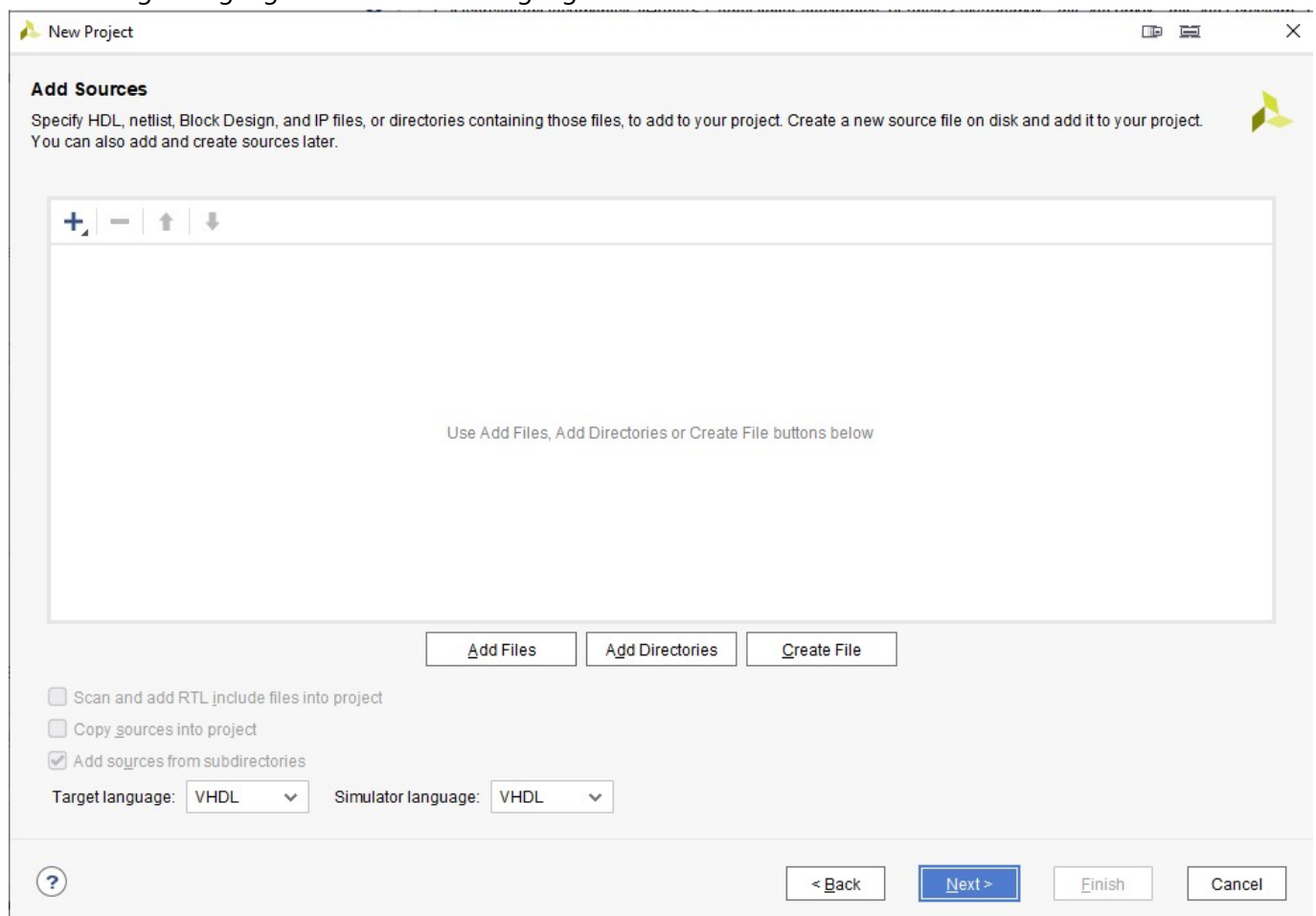
☐ **I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**  
Create a new Vivado project from a predefined template.


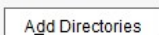
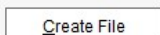
Choose target language and simulation language VHDL and create file



**New Project**

**Add Sources**  
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below



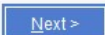


  

☐ Scan and add RTL include files into project

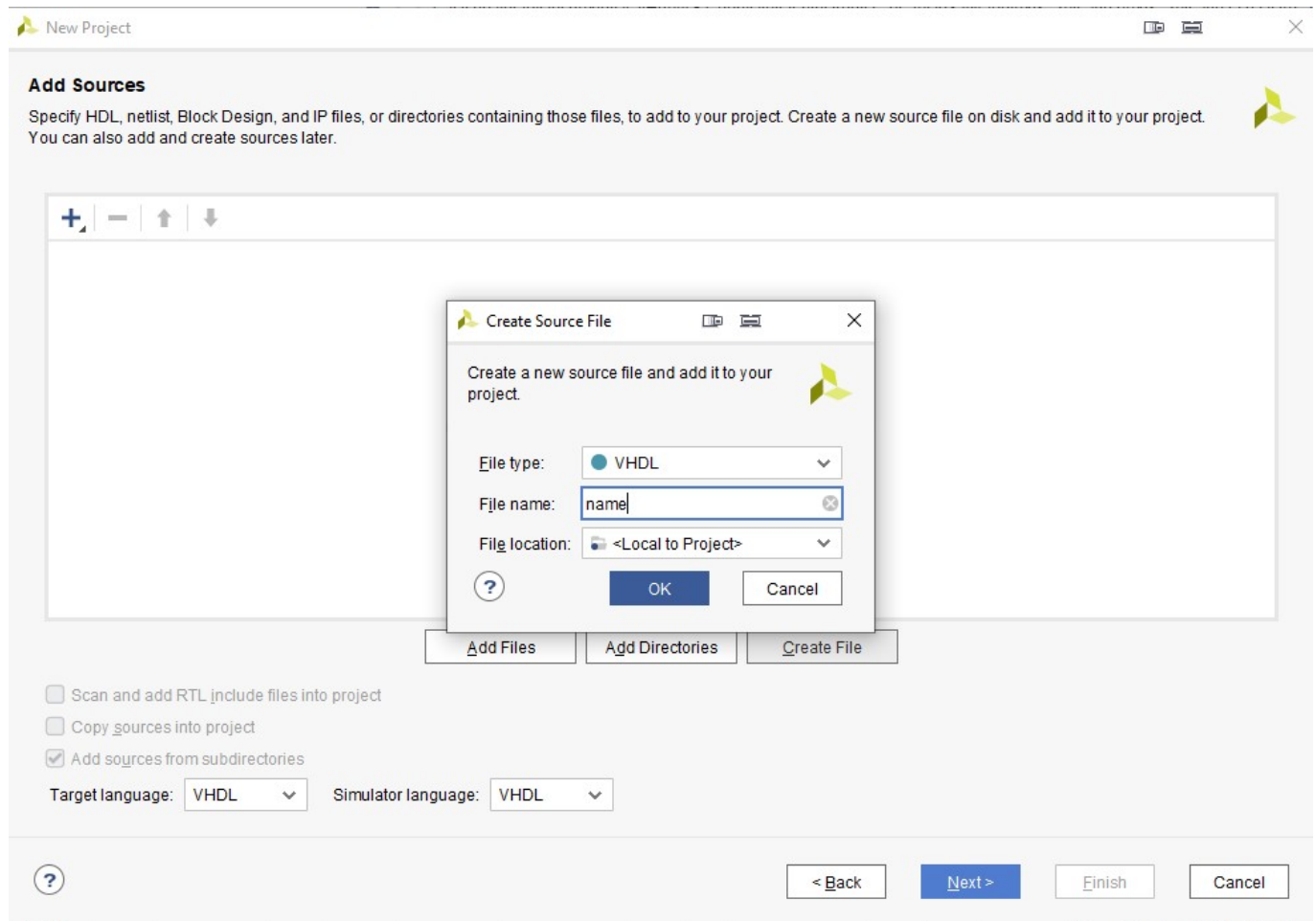
☐ Copy sources into project

☒ Add sources from subdirectories

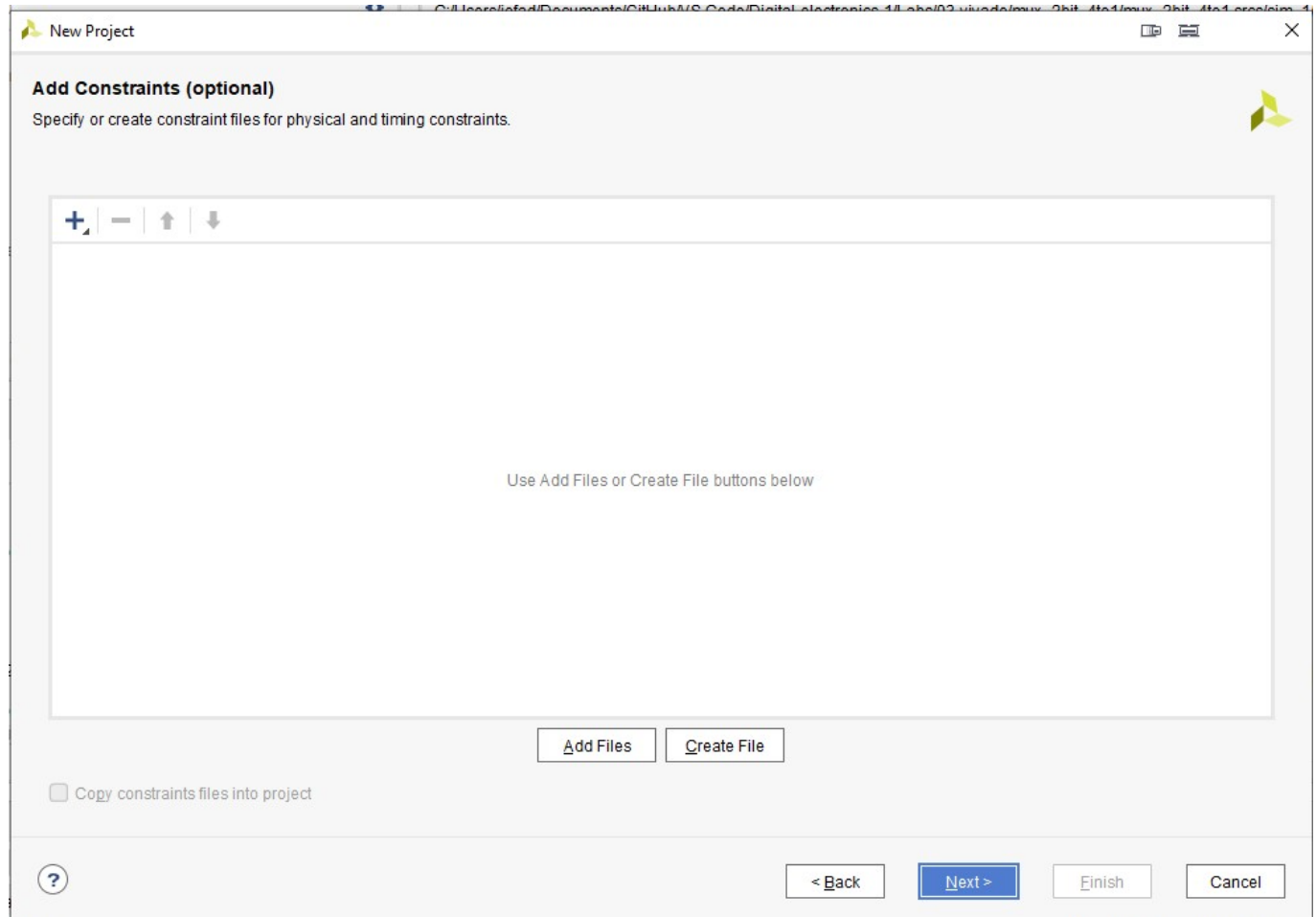
Target language: VHDL Simulator language: VHDL

Type name of design file and choose file type VHDL and click OK



In constraints click next



Click on boards in top panel and find Nexys A7-50T, choose it and click next



**New Project**

**Default Part**  
Choose a default Xilinx part or board for your project.

Parts | **Boards**

[Reset All Filters](#) [Install/Update Boards](#)

Vendor:  Name:  Board Rev:

Search:  (5 matches)

Display Name	Preview	Vendor	File Version	Part	I/O Pin Cou
<a href="#">Nexys A7-100T</a>		digilentinc.com	1.0	xc7a100tcsg324-1	324
<a href="#">Nexys A7-50T</a>		digilentinc.com	1.0	xc7a50tcsg324-1L	324
<a href="#">Nexys4</a>		digilentinc.com	1.1	xc7a100tcsg324-1	324
<a href="#">Nexys4 DDR</a>		digilentinc.com	1.1	xc7a100tcsg324-1	324
<a href="#">Nexys Video</a>					

[? < Back](#) [Next >](#) [Finish](#) [Cancel](#)

Finally check project summary and click on finish

**New Project**

**VIVADO**  
HLx Editions

**New Project Summary**

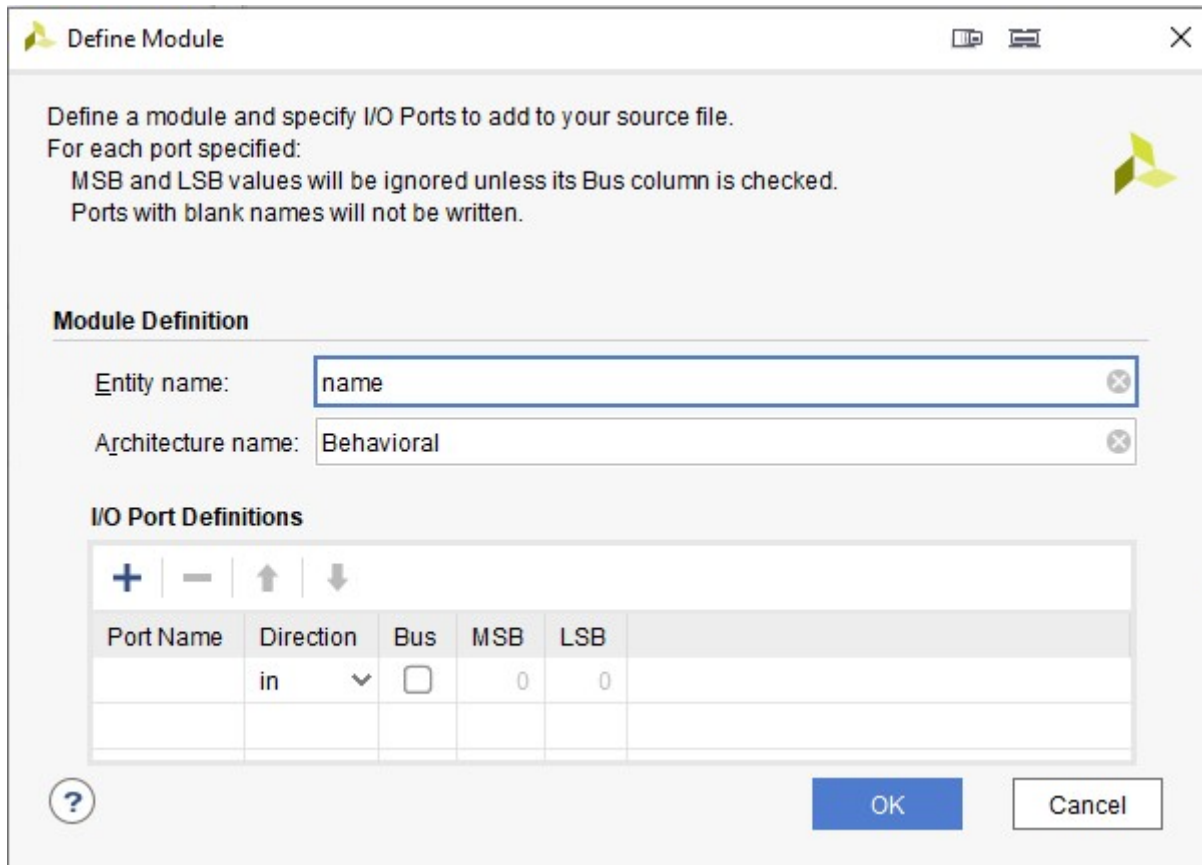
- A new RTL project named 'project\_1' will be created.
- 1 source file will be added.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:  
 Default Board: Nexys A7-50T  
 Default Part: xc7a50tcsg324-1L  
 Product: Artix-7  
 Family: Artix-7  
 Package: csg324  
 Speed Grade: -1L

**XILINX**

To create the project, click Finish

[? < Back](#) [Next >](#) [Finish](#) [Cancel](#)

If you want, add some I/O ports definition



Define a module and specify I/O Ports to add to your source file.  
For each port specified:  
MSB and LSB values will be ignored unless its Bus column is checked.  
Ports with blank names will not be written.

**Module Definition**

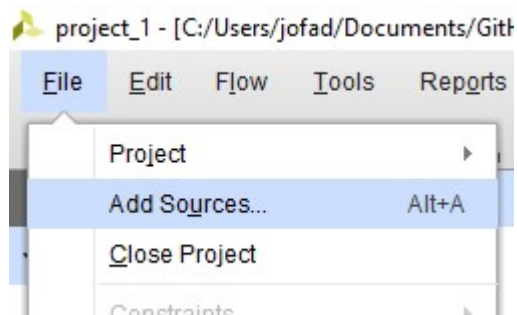
Entity name:

Architecture name:

**I/O Port Definitions**

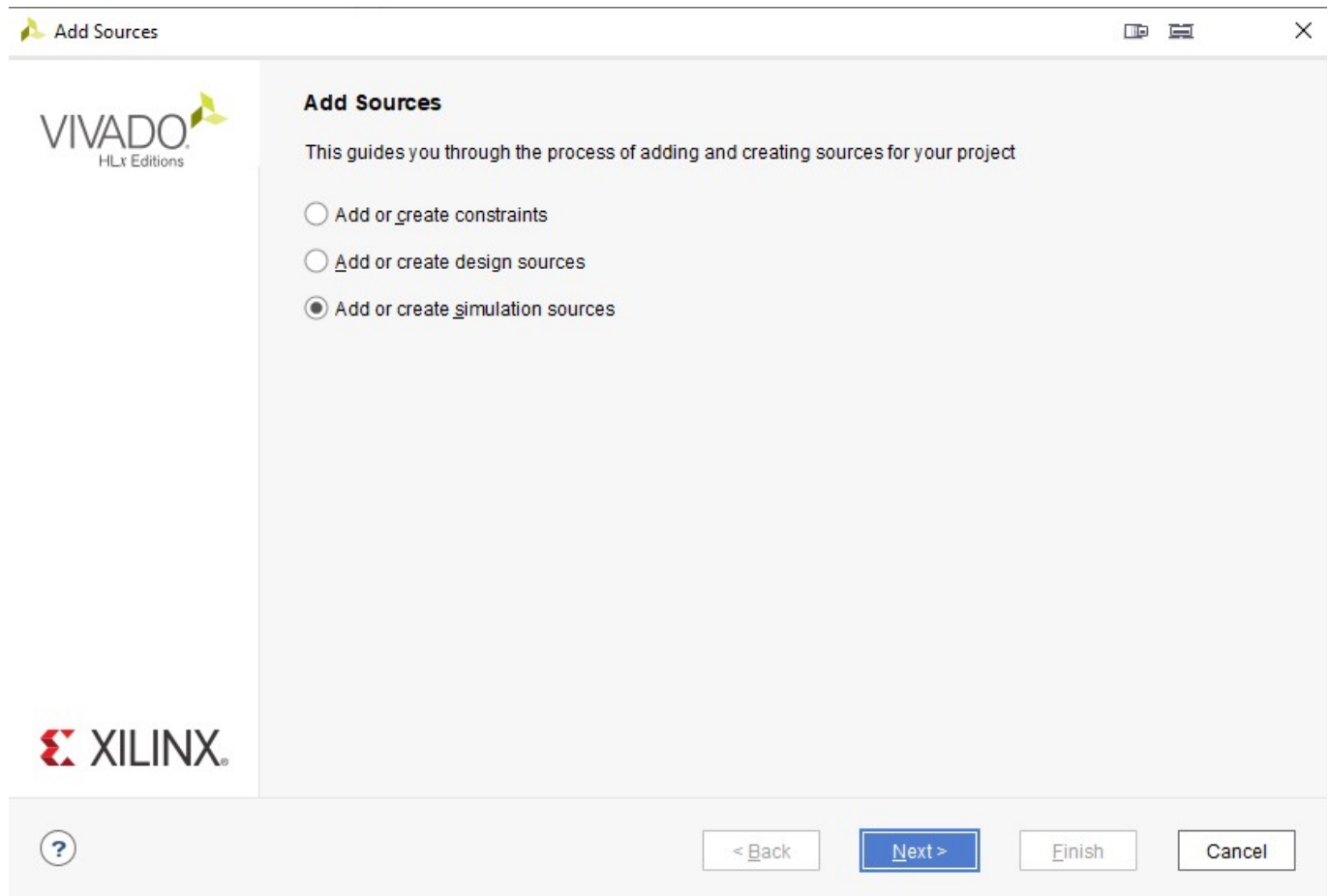
Port Name	Direction	Bus	MSB	LSB	
	in	<input type="checkbox"/>	0	0	

Click file and add sources

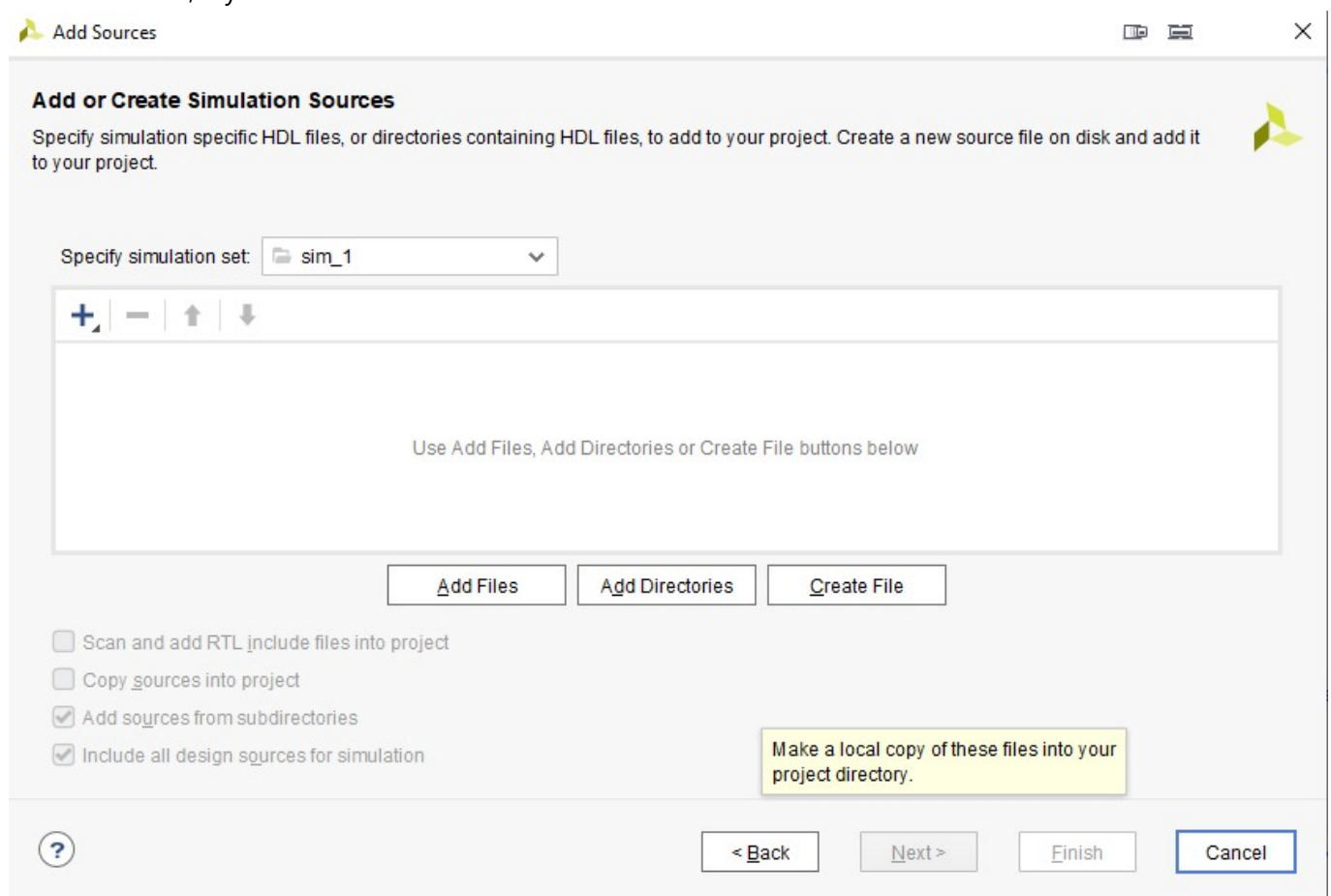


Check add or create simulation sources and click next

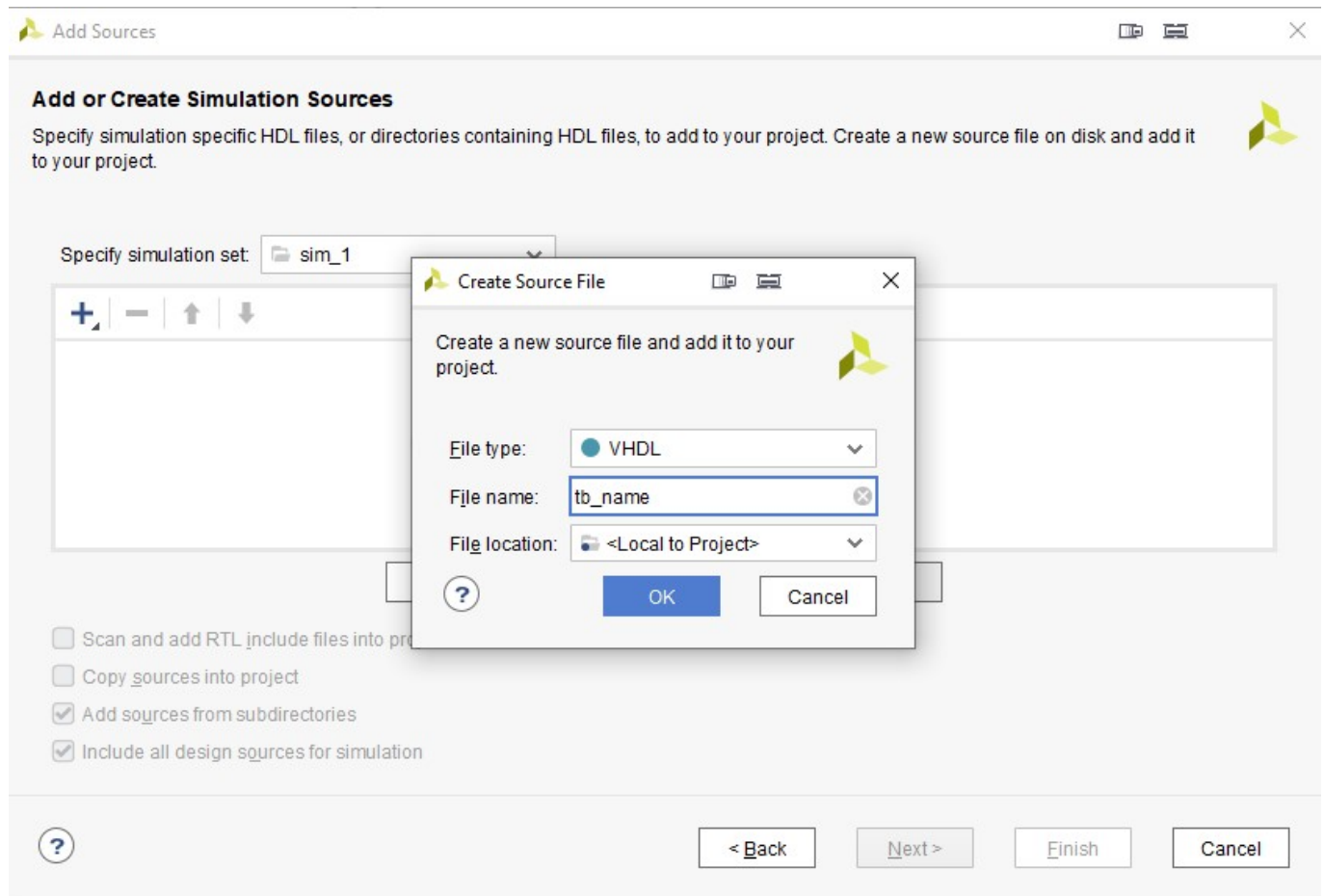




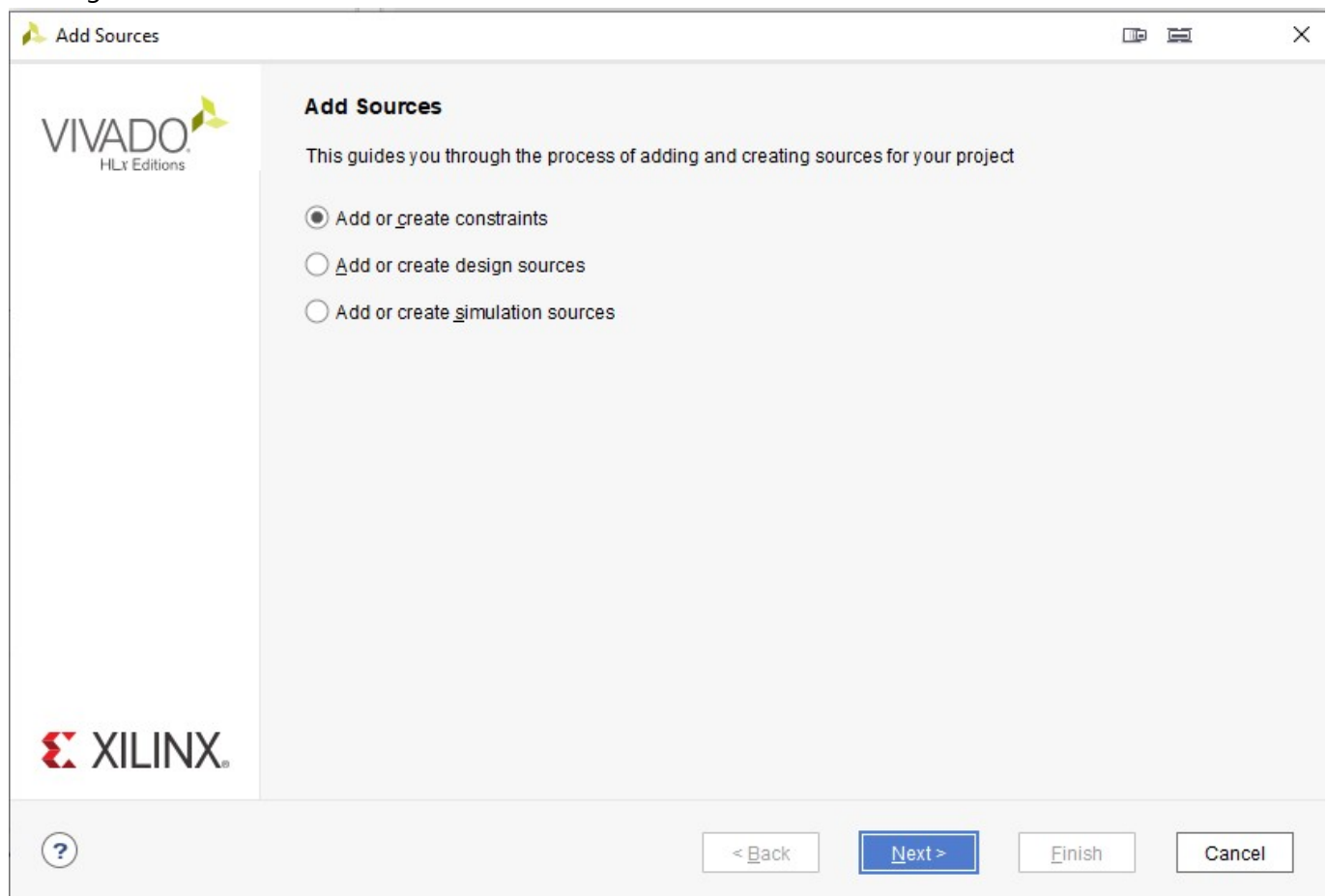
Click create file, if you do it click finish



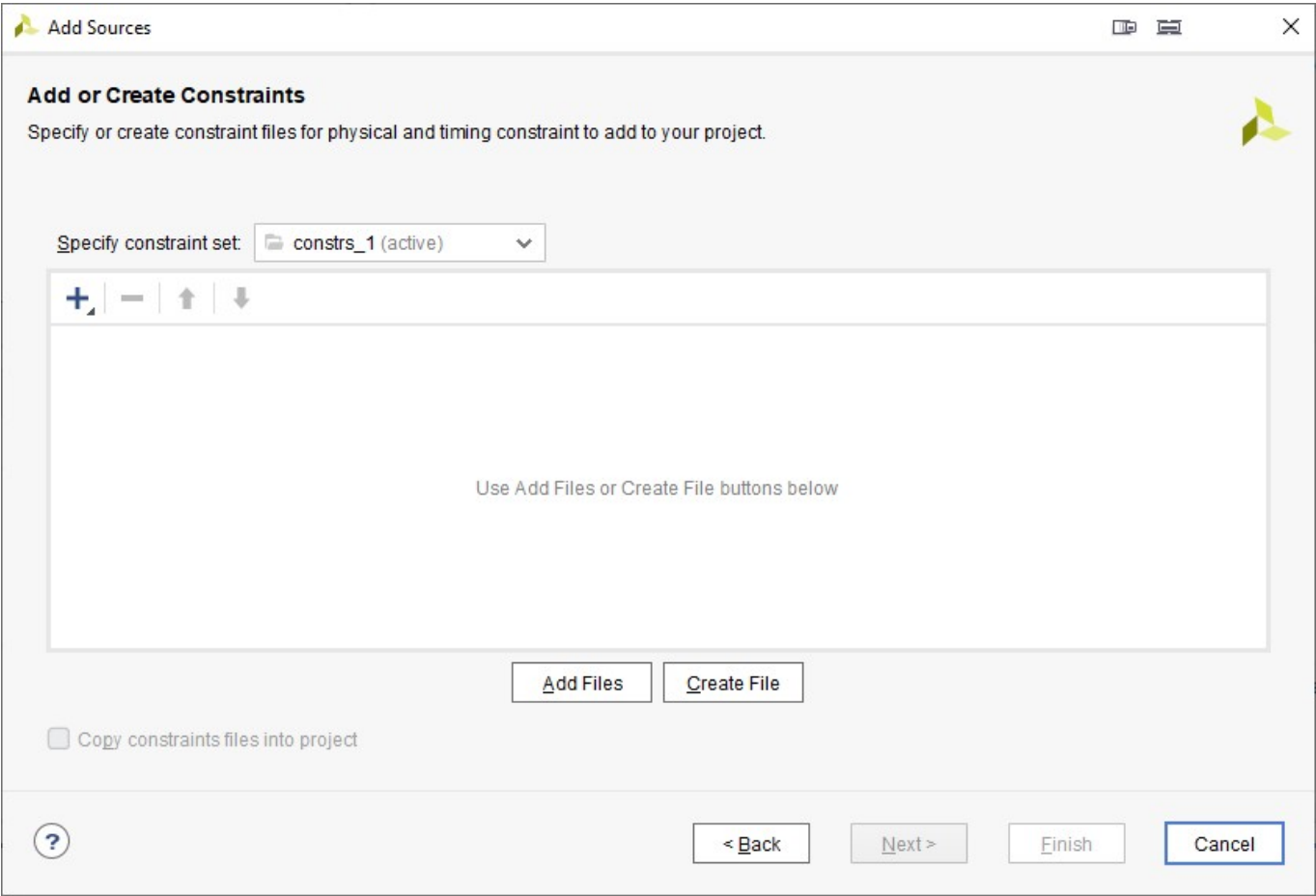
Type *tb\_* as testbench and *file name* *tb\_name*, click OK



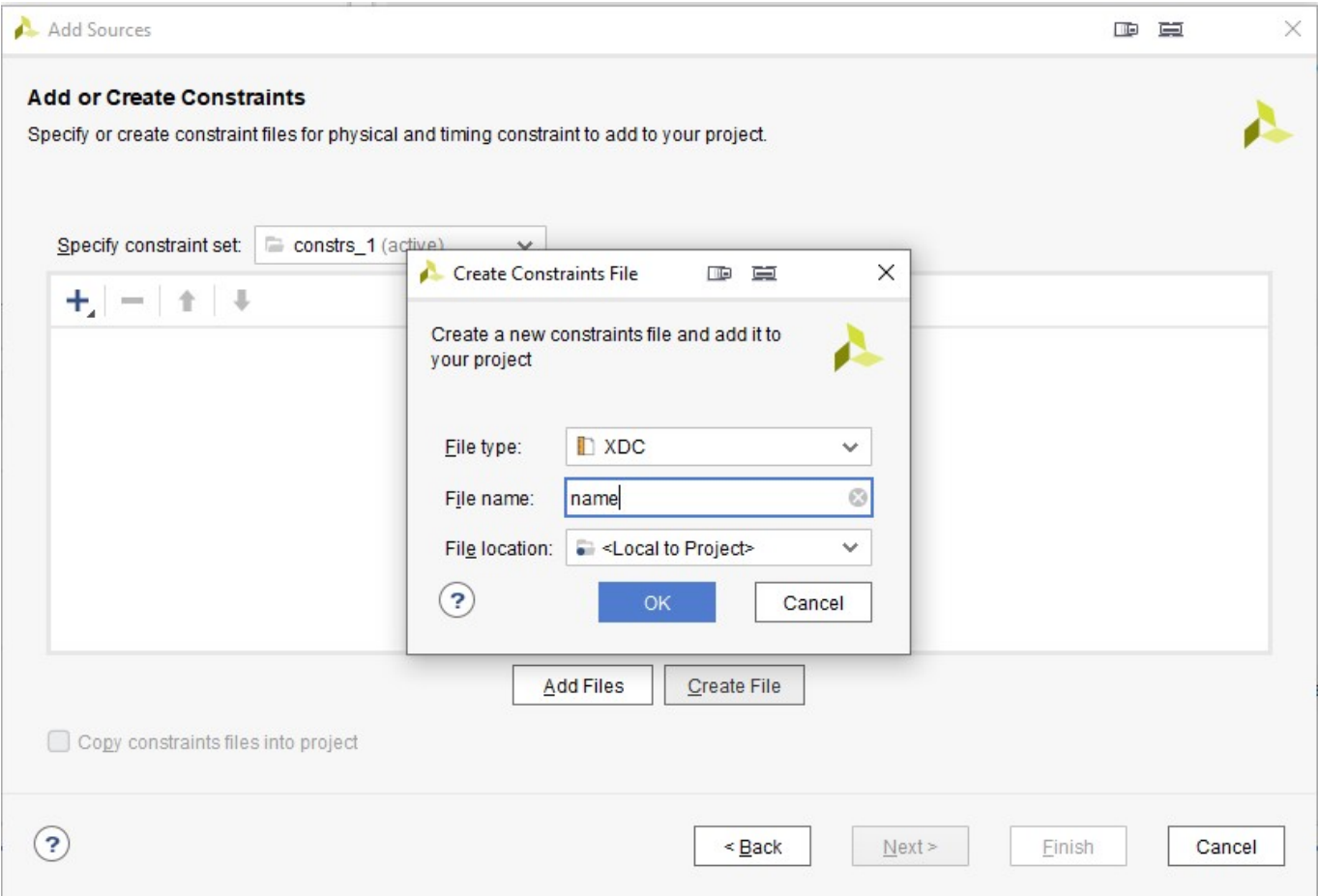
Click again file, add sources and choose add or create constraints, click next



Click create file, when created click finish

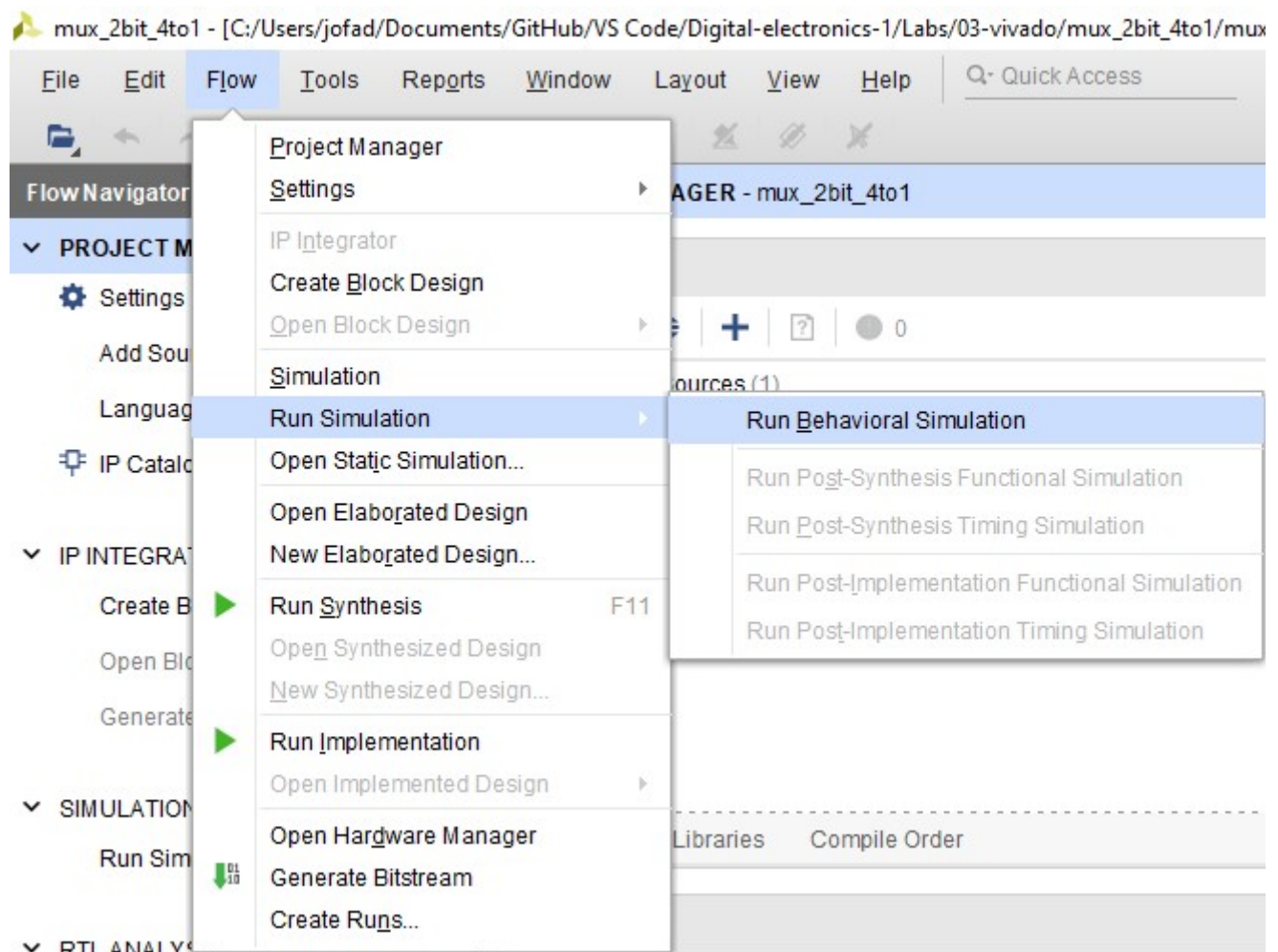


Type name of file and click OK



Your project was created

For run simulation click flow -> run simulation -> run behavioral simulation



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[GitHub repository](#)