

INFORME TRABAJO FINAL



Universidad del Cauca

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Presentado a:

Ing. Fulvio Yesid Vivas

Circuitos digitales

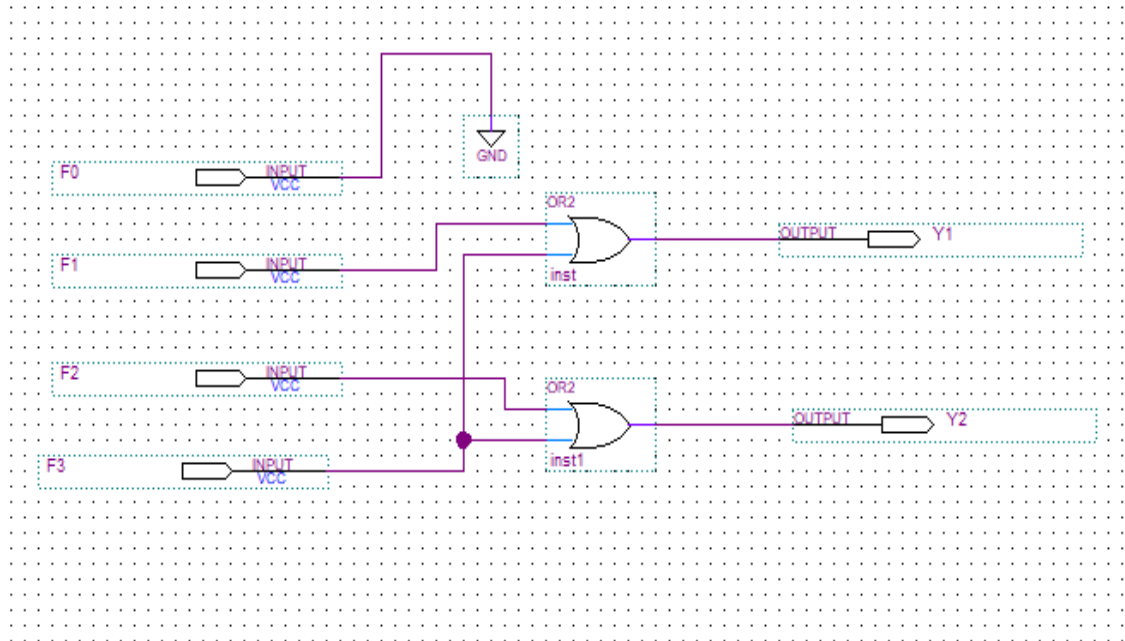
Universidad del Cauca

Facultad de Ingeniería Electrónica y Telecomunicaciones

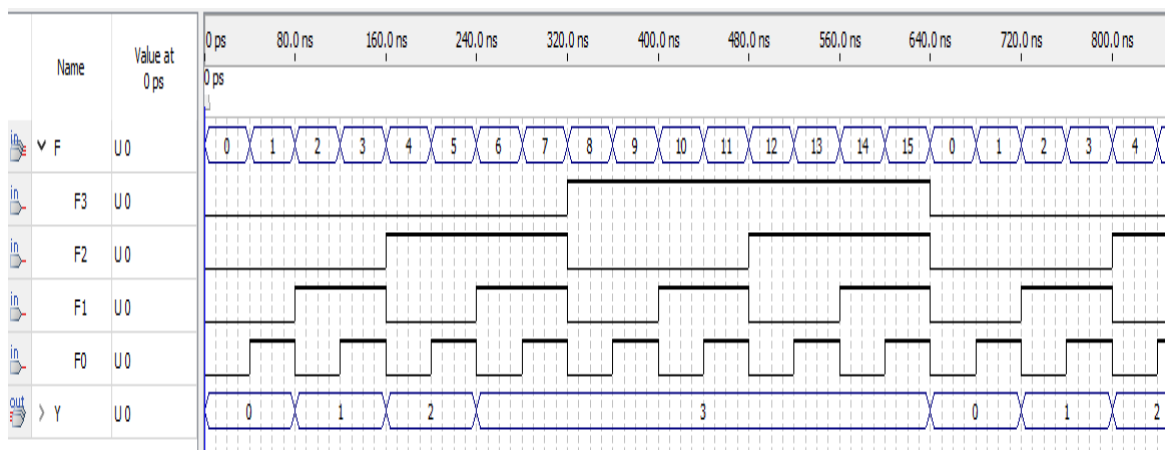
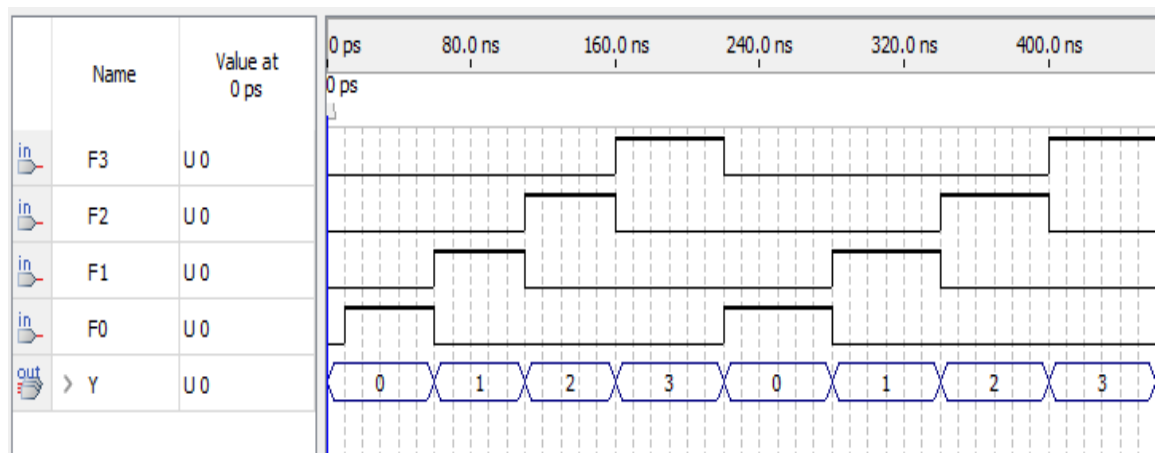
Popayán

2023

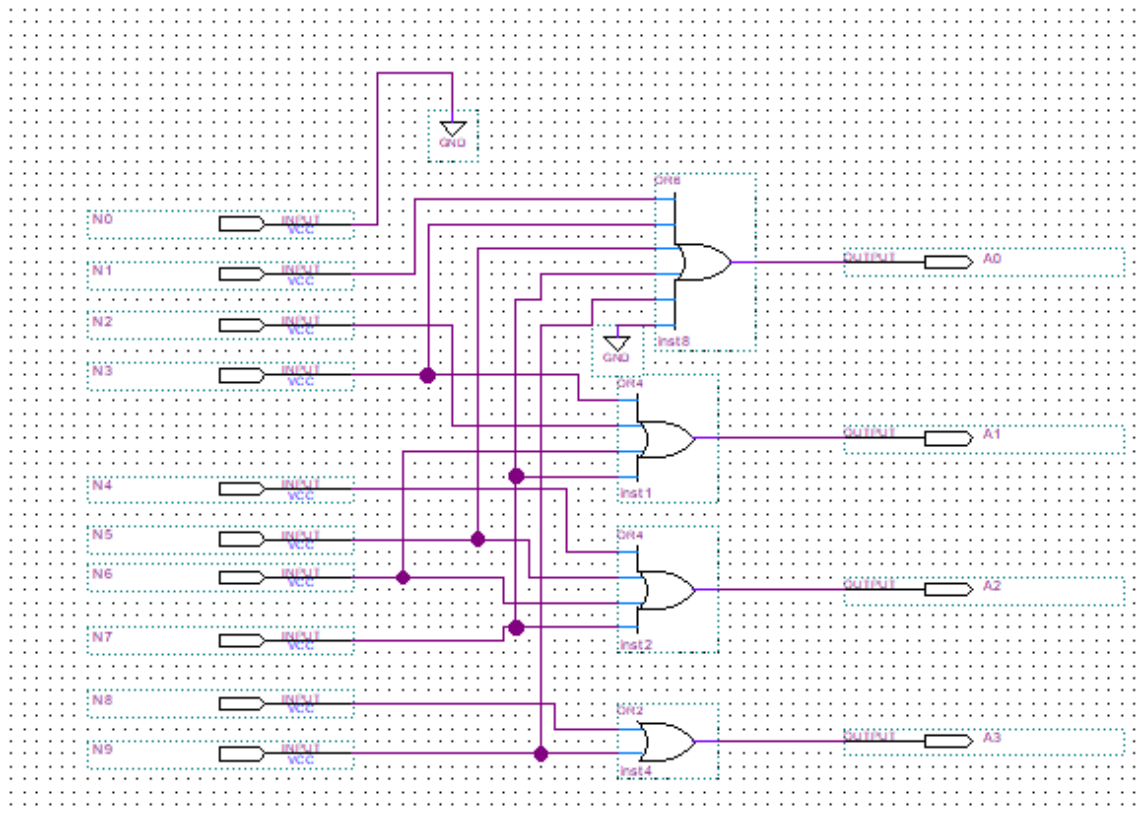
Componente codificador de 4 a 2:



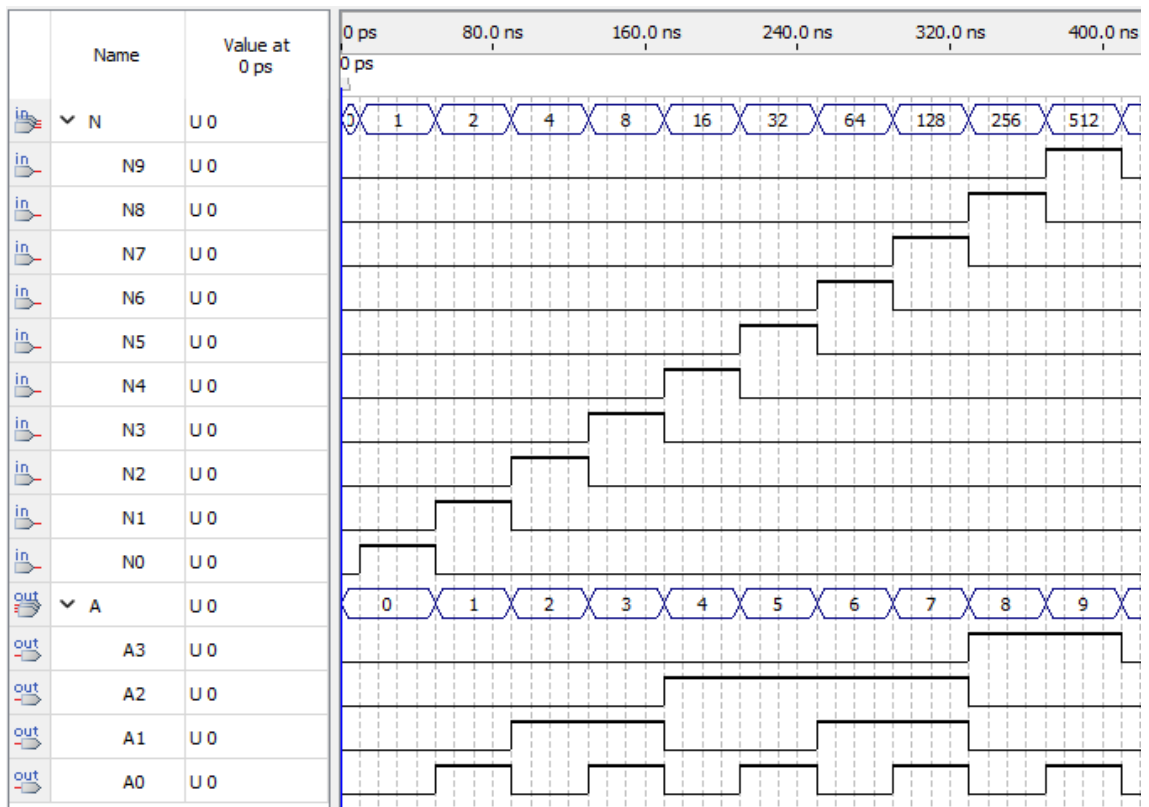
Simulación:



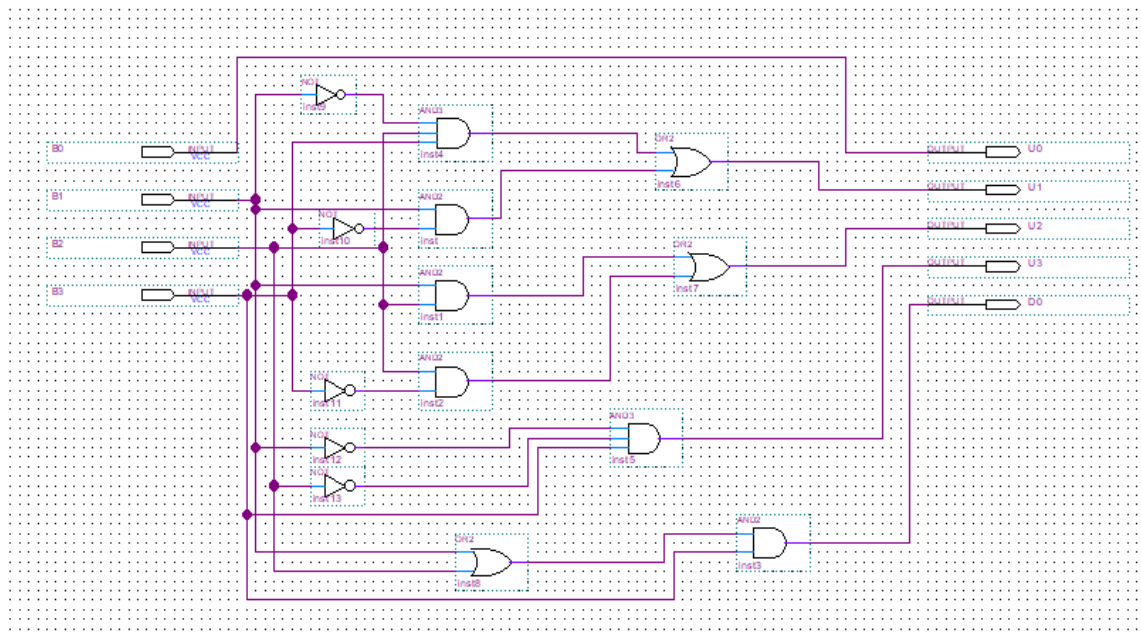
Componente codificador a BCD propuesto por el profesor en clase de 9 a 4:



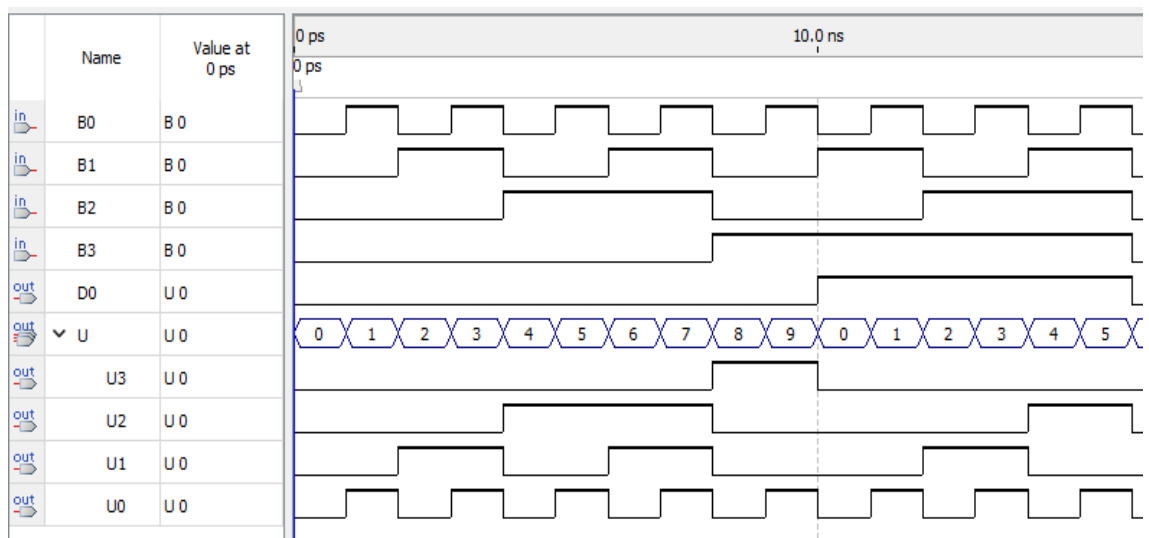
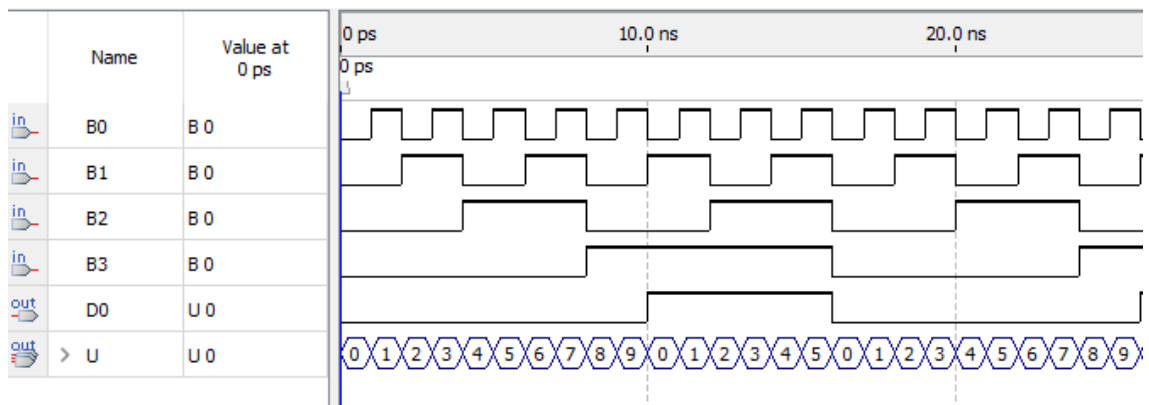
Simulación:



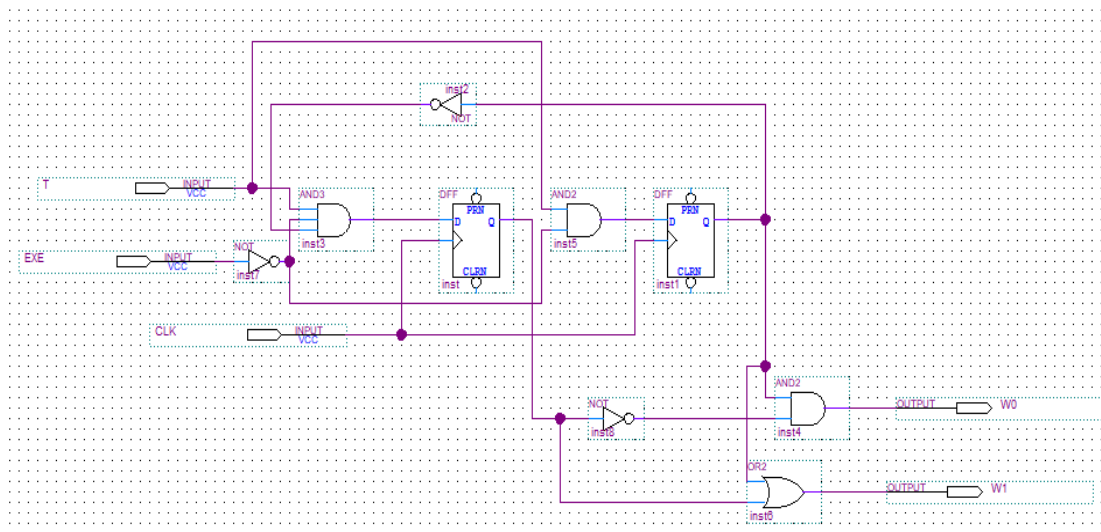
Comparador de bits a BCD:



Simulación:



MAQUINA DE CONTROL



Simulación:

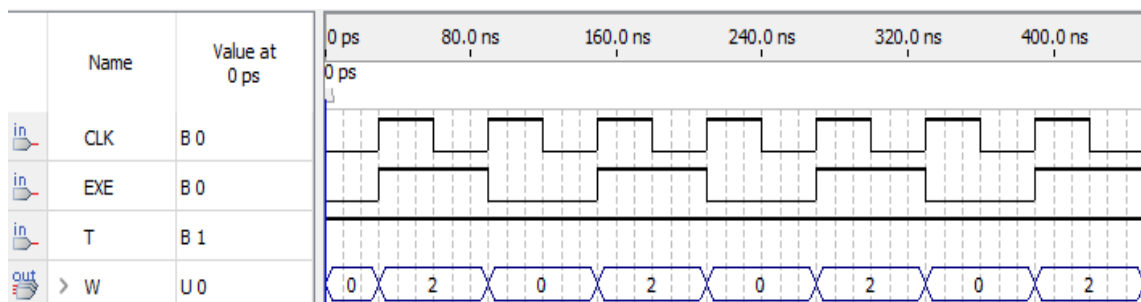
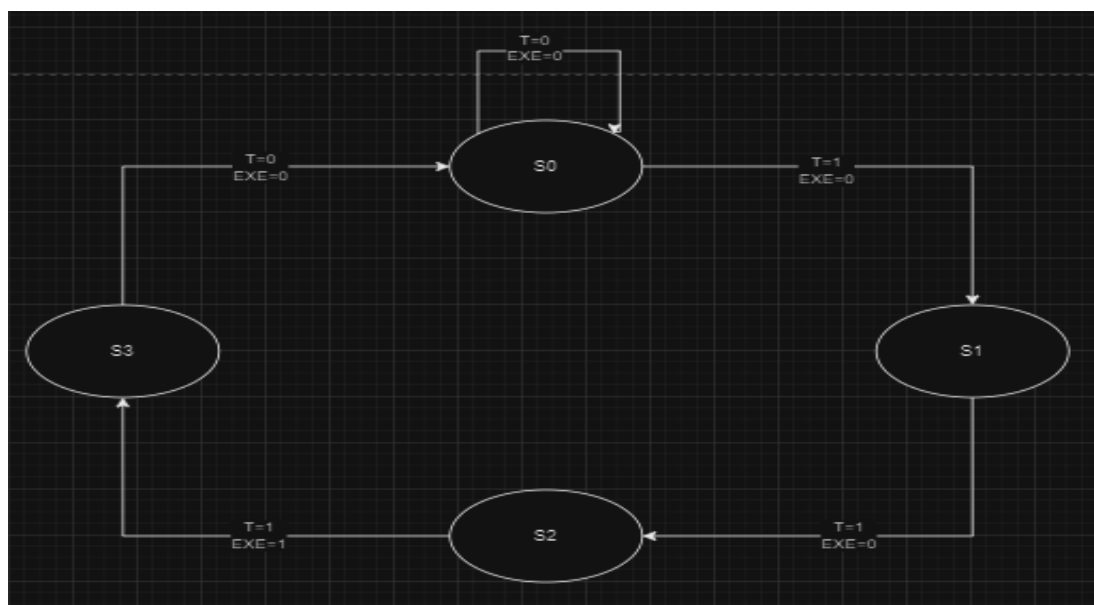


Diagrama de estados:

(4 estados)



Nombre:

Materia:

UD MM AA

EA	T_e	$E F$	Y	S_0	S_1	S_2	S_3
S_0	1 0	S_1	0	0 0			
S_1	1 0	S_2	0	0 1			
S_2	1 1	S_3	0	1 1			
S_3	0 0	S_0	1	1 0			
$Q_1 Q_0$	$T E$	$Q_1^+ Q_0^+$	Y	D_0	D_1		
0 0	0 0	0 0		0	0		
0 0	0 1	x x	0 0	x	x		
0 0	1 1	x x		x	x		
0 0	1 0	0 1		0	1		
0 1	0 0	x x		x	x		
0 1	0 1	x x	0 1	x	x		
0 1	1 1	x x		x	x		
0 1	1 0	1 1		1	1		
1 1	0 0	x x		x	x		
1 1	0 1	x x	0 1	x	x		
1 1	1 1	x x		x	x		
1 1	1 0	1 0		1	0		
1 0	0 0	0 0		0	0		
1 0	0 1	x x	1 1	x	x		
1 0	1 1	x x		x	x		
1 0	1 0	x x		1	0		

$$Y = Q_1 + Q_0$$

$$Y = Q_1 + Q_0$$

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D_1	T_e	$Q_1 Q_0$	0 0	0 1	1 1	1 0
0 0	0	x	x	1		
0 1	x	x	x	1		
1 1	x	x	x	1		
1 0	0	x	x	1		

$$D_1 = T \bar{E}$$

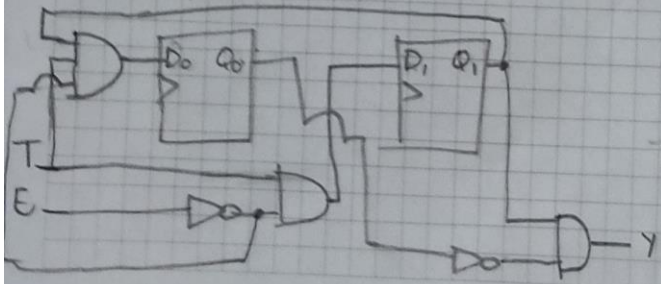
D_2	T_e	$Q_1 Q_0$	0 0	0 1	1 0	1 1
0 0	0	x	x	1		
0 1	x	x	x	1		
1 1	x	x	x	0		
1 0	0	x	x	x		

$$D_0 = \bar{Q}_1 T \bar{E}$$

Salida

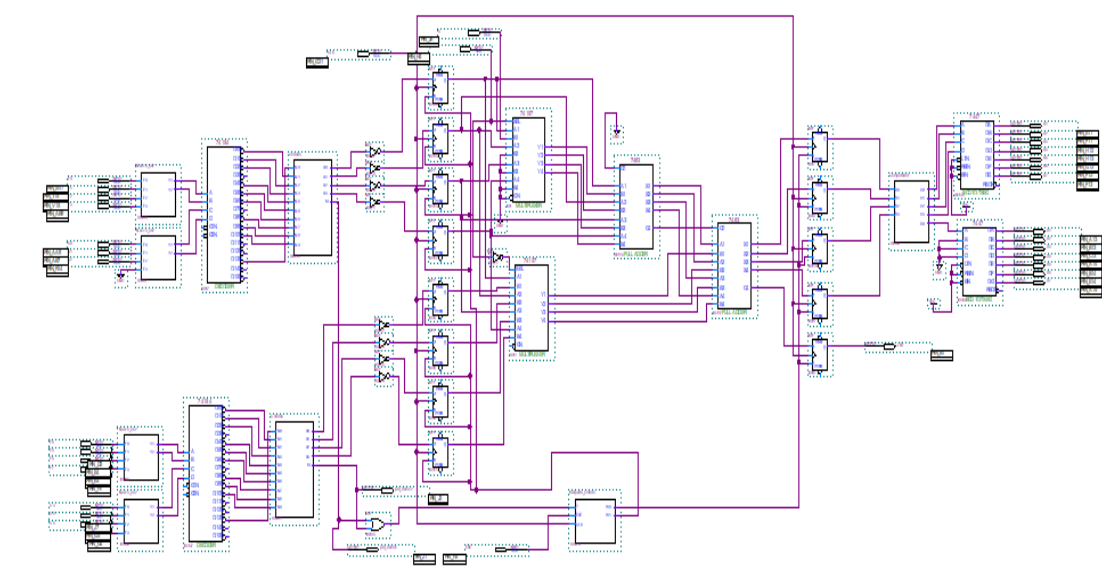
$Q_1 Q_0$	0 1	0 0
0 0	0	0
1 1	1	0

$$Y = Q_1 \bar{Q}_0$$



Estado actual		Entrada		Estado futuro		salidas		D1	D0
Q1	Q0	T	E	Q1+	Q0+	W0	W1	D1	D0
00		0	0	0	0	00		0	0
		0	1	X	X			X	X
		1	1	X	X			X	X
		1	0	0	1			0	1
01		0	0	X	X	01		X	X
		0	1	X	X			X	X
		1	1	X	X			X	X
		1	0	1	1			1	1
11		0	0	X	X	01		X	X
		0	1	X	X			X	X
		1	1	X	X			X	X
		1	0	1	0			1	0
10		0	0	0	0	11		0	0
		0	1	X	X			X	X
		1	1	X	X			X	X
		1	0	X	X			X	X

CIRCUITO FINAL



Simulacion:

