

```
graph TD; subgraph System [ ]; subgraph CPU [Central Processing Unit (CPU)]; CU[Control Unit (CU)]; ALU[Arithmetic/Logic Unit (ALU)]; end; MU[Memory Unit (MU)]; end; CPU <--> MU; System <--> IO[Input/Output Devices (I/O)];
```

Central Processing Unit (CPU)

Control Unit (CU)

Arithmetic/Logic Unit (ALU)



Memory Unit (MU)



Input/Output Devices (I/O)