False Sharing

RAM

→ Cache Line

update Cache

Cache 1

CPU 1

| 3 | 8 | 7 | 4 | 3 | 1 | 0 | 6 |

update Cache

| 3 | 8 | 7 | 4 | 3 | 1 | 1 | 6 |

Cache 2

CPU 2

| 3 | 8 | 7 | 4 | 3 | 1 | 0 | 6 |

update Cache   ②   inc. ①

| 3 | 8 | 7 | 4 | 3 | 1 | 1 | 6 |