



# PSE - Introduction – Neural Network based Image Classification on Heterogeneous Platforms

Dennis Weller & Sarath Mohanachandran Nair

INSTITUTE OF COMPUTER ENGINEERING (ITEC) - CHAIR FOR DEPENDABLE NANO COMPUTING (CDNC)



### **Organisational Matters**



Enrollment:

**QISPOS:** (SPO 2008)

- zu TSE (Nr. 455) anmelden
- zu PSE (Nr. 529) anmelden

**Campus:** (SPO 2015)

- 1. TSE (Nr. 7500075) zu überfachlichen Qualifikationen hinzufügen
- 2. zu TSE (Nr. 7500075) anmelden
- 3. zu PSE (Nr. 7500076) anmelden

### **Organisational Matters**



Not all mandatory grades?

#### fehlende Noten?



Falls Noten noch nicht eingetragen sind oder Nachprüfungen anstehen:

- Auf jeden Fall in Odyssee anmelden
- Beim ersten Treffen Notenauszug mitbringen
- QISPOS/Campus-Anmeldung schnellstmöglich nachholen

#### **Motivation**



- Neural Networks (NN) are deployed for
  - Classification
  - Prediction
  - Function Approximation
  - Recognizing Patterns e.g. objects in real scenes
- Neural Networks Applications
  - Autonomous Driving
  - Face Recognition
  - Natural Language Processing
  - Gesture Recognition





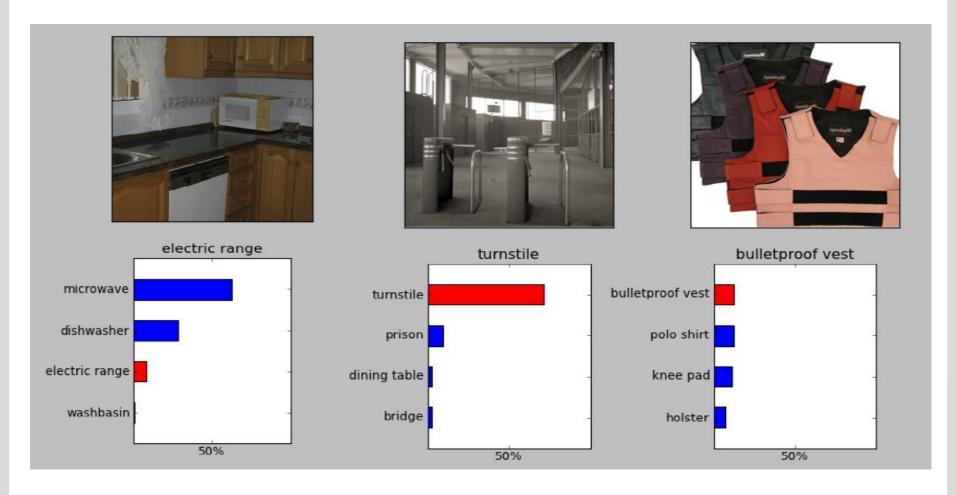
- 1. Human Face
- 2. Ball
- 3. Glass

. . .

# **Image Classification**



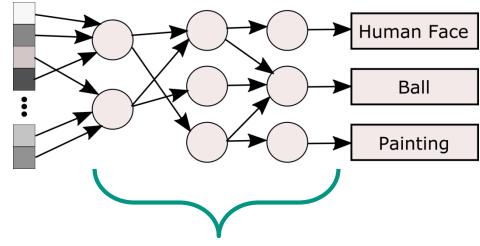
Classification results: Probabilistic



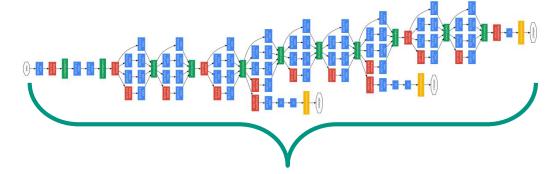
#### **Neural Network Models**



- Back-Propagation
- Boltzman Machines
- Deep Neural Networks
- **.** . . .



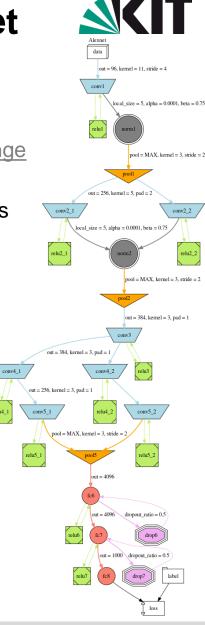
3-layer Neural Network



Googlenet: 50-layer Deep Neural Network (with Inception layers)

# Deep Neural Network Example: AlexNet

- AlexNet
  - Convolutional Neural Network
  - Winner of the <u>ImageNet Large Scale Visual Recognition Challenge</u> 2012
  - Consists of 8 layers: 5 convolutional and 3 fully-connected layers
- NN properties:
  - Topology of the Net (Number of Layers, Activation Functions)
  - Learning Rule
  - Objective Function
  - Learning Parameters



#### **Deep Neural Network – Pros and Cons**



- Advantages
  - Massive Parallelism
  - Unsupervised Learning Possible
- Disadvantages
  - Huge Data Set needed for Training (Unsupervised Learning)
  - Very Compute Intensive
  - High Computationally Costs: learning/classification time, power consumption
- Problem solution
  - Heterogeneous Platforms: CPUs, GPUs, FPGAs, ASICs

## **Heterogeneous Platforms**







# ■ CPU:

- Good performance for a wide range of computations: integer operations, floating point operations
- Instructions run sequential thus bad performance for complex neural network computations

#### GPU

- Single Instruction Multiple Data Units (SIMD), parallel computing of geometric problems as vector operations, convolutions etc.
- + High Performance
- High Energy Consumption
- Good performance only for specific kind of calculations (vector operations)

#### FPGA

- Semi-customized architecture thus tailor made designs
- Parallelism, Pipelining, Multiple Instructions Multiple Data (MIMD)
- Low Power Consumption
- High Design Cycles using conventional programming schemes like VHDL (several month)

#### ASICs

- Very high performance, very low power consumption
- Must be manufactured







# Roadmap



Phase	von – bis	Dauer
Auftaktveranstaltung	18.10.	
Anmeldung/Einteilung	18.10. – 25.10.	
Erstes Gruppentreffen	28.10. – 31.10.	
Pflichtenheft	04.11. – 22.11.	3 Wochen
Entwurf	25.11. – 20.12.	4 Wochen
Weihnachtspause	23.12. – 06.01.	
Implementierung	07.01. – 31.01.	4 Wochen
z.B. Klausurpause	03.02. – 14.02.	
Qualitätssicherung	17.02. – 06.03.	3 Wochen
interne Abnahme	09.03. – 13.03.	
Abschlusspräsentation	16.03. – 20.03.	

### Responsible persons



1 responsible persons for each phase

Phase	Anteil
Pflichtenheft	10%
Entwurf	30%
Implementierung	30%
Qualitätssicherung	20%
Abschlusspräsentation	10%

## **Weekly Meetings**



- Project duration: October 2019 March 2020
- Working Effort: 2 days/week
- Weekly Group Meetings with Advisors
  - Proposal: Friday morning

#### **Recommended Materials**



- Book: "Neural Networks for Pattern Recognition" Christopher M. Bishop
- Neural Network Online Courses
  - https://www.coursera.org/learn/neural-networks
- OpenCL
  - https://www.khronos.org/opencl/
- Intel (Altera) OpenCL SDK
  - https://software.intel.com/en-us/intel-opencl
- FPGA SoC (OpenCL compatible) DE1SoC (F-type)
  - http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=205&No=836&PartNo=4
- Intel Movidius Neural Compute Stick
  - http://developer.movidius.com