KOD: S61

BLAD NR: 01

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1)

HEX	BIN
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

$DB3_{16} = \underline{\underline{1101\ 1011\ 0011_2}}$

to convert from binary to octal a easy way its to group the binary number into 3 bits group.

$110\ 110\ 110\ 011_2 = \underline{\underline{6663}}_8$

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2) 35_{10} in binary is:

	quotient	remainder	
35/2	17	1	Least significant bit
17/2	8	1	
8/2	4	0	
4/2	2	0	
2/2	1	0	
1/2	0	1	Most significant bit

10 0011

In 8-bit binary: $0010\ 0011_2$

-35_{10} : Invert: $0010\ 0011_2$

$1101\ 1100_2$

add +1 to the inverted binary number

$$\begin{array}{r} 1101\ 1100 \\ +1 \\ \hline \end{array}$$

Answer: $1101\ 1101_2 \Rightarrow -35_{10}$

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3) $(x+y+z)(x+y+\bar{z})$

$= \underbrace{xx}_{=x} + xy + x\bar{z} + yx + \underbrace{yy}_{=y} + y\bar{z} + zx + zy + \underbrace{z\bar{z}}_{=0}$

$= x + xy + x\bar{z} + yx + y + y\bar{z} + zx + zy =$

$= x(1 + y + \bar{z} + y + z) + y(1 + \underbrace{\bar{z} + z}_{=1})$

$=y$ $=1$

$= x(\underbrace{1 + y + 1}_{=1}) + y(\underbrace{1+1}_{=1})$

$= \underline{\underline{x + y}}$

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4) $\overline{a+\overline{bc}}\cdot\overline{\overline{a}(b+c)}=0$

Left Hand side (LHS) = $\overline{a+\underbrace{\overline{bc}}_{\text{by De Morgan's law (1)}}}\ \overline{\overline{a}(b+c)}$

$$=\underbrace{\overline{(a+\overline{b}+\overline{c})}\,\overline{(\overline{a}b+\overline{a}c)}}_{\text{by De Morgan's law (2)}}$$

$$=(\overline{a}\cdot\overline{\overline{b}}\cdot\overline{\overline{c}})(\underbrace{\overline{\overline{a}b}}\cdot\underbrace{\overline{\overline{a}c}})\quad\text{by De Morgan's law (1)}$$

$$=(\overline{a}bc)(\overline{\overline{a}}+\overline{b})(\overline{\overline{a}}+\overline{c})$$

$$=\overline{a}bc\,(a+\overline{b})(a+\overline{c})$$

$$=\overline{a}bc(\underbrace{aa}_{=a}+a\overline{c}+\overline{b}a+\overline{b}\overline{c})$$

$$=\underbrace{a\overline{a}}_{=0}bc+\underbrace{a\overline{a}}_{=0}b\underbrace{\overline{c}c}_{=0}+\underbrace{\overline{a}a}_{=0}\underbrace{b\overline{b}}_{=0}c+\overline{a}\underbrace{b\overline{b}}_{=0}\underbrace{c\overline{c}}_{=0}$$

$$=0\quad=\text{Right Hand Side (RHS)}$$

QED

De Morgan's law:

- $\overline{x}+\overline{y}=\overline{xy}$ (1)
- $\overline{x}\cdot\overline{y}=\overline{x+y}$ (2)

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5)

Row	X_3	X_2	X_1	X_0	output
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	–
5	0	1	0	1	–
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	–
10	1	0	1	0	–
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	–

Karnaugh - map

X_3X_2 \ X_1X_0	00	01	11	10
00	0 (0)	1 (1)	0 (3)	0 (2)
01	– (4)	– (5)	1 (7)	1 (6)
11	0 (12)	1 (13)	– (15)	0 (14)
10	0 (8)	– (9)	0 (11)	– (10)

$\bar{X}_3 X_2$

$\bar{X}_1 X_0$

Answer : $f(x_3, x_2, x_1, x_0) = \bar{X}_3 X_2 + \bar{X}_1 X_0$

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6) table:

INPUT			OUTPUT	
X_2	X_1	X_0	Z_1	Z_0
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

for Z_1:

$X_2 \backslash X_1X_0$	00	01	11	10
0	1	1	0	1
1	1	0	0	0

$$Z_1 = \overline{X_1}\,\overline{X_0} + \overline{X_2}\,\overline{X_1} + \overline{X_2}\,\overline{X_0}$$

for Z_0:

$X_2 \backslash X_1X_0$	00	01	11	10
0	1	0	1	0
1	0	1	0	1

$$Z_0 = \overline{X_2}\,\overline{X_1}\,\overline{X_0} + X_2\overline{X_1}X_0 + \overline{X_2}X_1X_0 + X_2X_1\overline{X_0}$$

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7)
```
entity oddparity is
   Port ( in1 : in std_logic_vector (3 downto 0);
          parity : in std_logic;
          out1 : out std_logic_vector (4 downto 0));
end oddparity;

architecture rlt of oddparity is
begin
   Process ( in1 , parity)
      Variable op : std_logic_vector (3 downto 0);
   begin
      op := in1;
      Case op is
         when "0000" => parity <= '1'; out1 <= "10000";
         when "0001" => parity <= '0'; out1 <= "00001";
         when "0010" => parity <= '0'; out1 <= "00010";
         when "0011" => parity <= '1'; out1 <= "10011";
         when "0100" => parity <= '0'; out1 <= "00100";
         when "0101" => parity <= '1'; out1 <= "10101";
         when "0110" => parity <= '1'; out1 <= "10110";
         when "0111" => parity <= '0'; out1 <= "00111";
         when "1000" => parity <= '0'; out1 <= "01000";
         when "1001" => parity <= '1'; out1 <= "11001";
         when "1010" => parity <= '1'; out1 <= "11010";
         when "1011" => parity <= '0'; out1 <= "01011";
         when "1100" => parity <= '1'; out1 <= "11100";
         when "1101" => parity <= '0'; out1 <= "01101";
         when "1110" => parity <= '0'; out1 <= "01110";
         when "1111" => parity <= '1'; out1 <= "11111";
         when others => parity <= '0'; out1 <= "00000";

      end ceese;
      en process;
end rlt;
```

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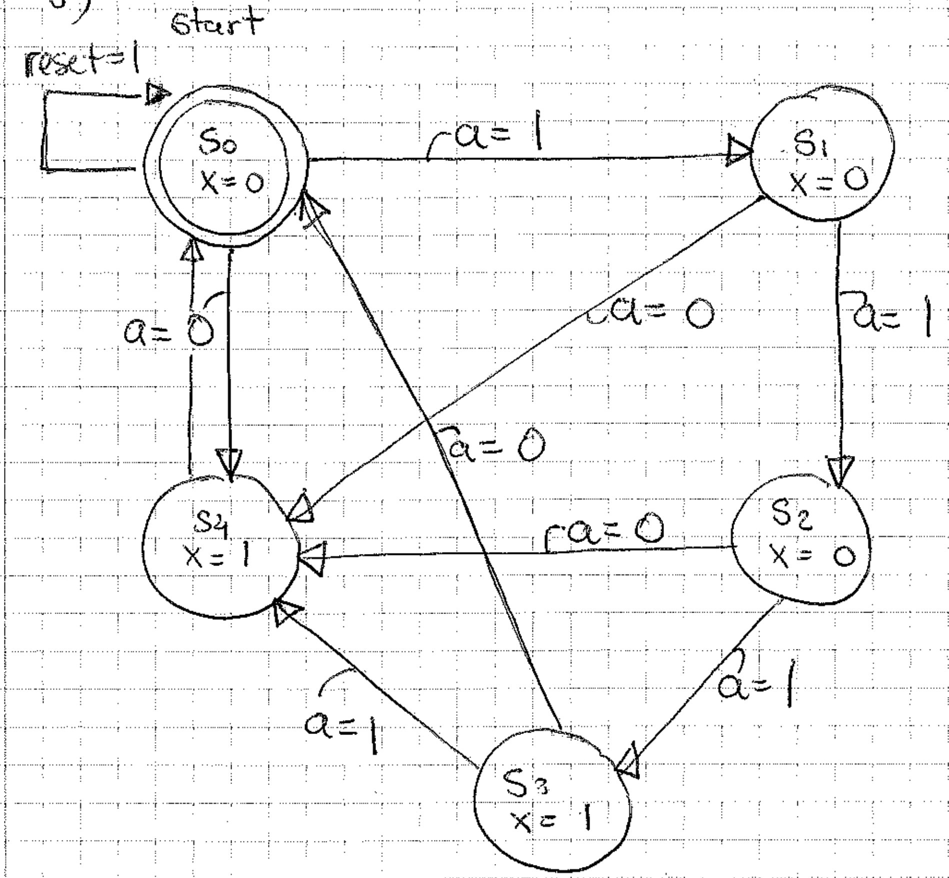
8)



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9)

State table:

S	X = 0	X = 1	Z
A	B	C	0
B	C	D	0
C	B	D	1
D	C	A	0

$\Rightarrow$ binary coding:

State(S)	Binary(Q)
A	00
B	01
C	10
D	11

$\Rightarrow$ transition table:

Q ($q_1 q_0$)	X = 0 (Q^+)	X = 1 (Q^+)	Z
00	01	10	0
01	10	11	0
10	01	11	1
11	10	00	0

D flip-flop: $q^+ = D$

q	q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

$\Rightarrow$ Exitation table:

Q	X = 0	X = 1	Z
00	01	10	0
01	10	11	0
10	01	11	1
11	10	00	0

$Q = \{q_1, q_0\}$ $D = \{d_1, d_0\}$

• δ function:

X \ $q_1 q_0$	00	01	11	10
0	0 (0)	1 (1)	1 (3)	0 (2)
1	1 (4)	1 (5)	0 (7)	1 (6)

X \ $q_1 q_0$	00	01	11	10
0	1 (0)	0 (1)	0 (3)	1 (2)
1	0 (4)	1 (5)	0 (7)	1 (6)

$$d_1 = \overline{q_1} q_0 + \overline{X} q_0 + X \overline{q_0}$$

$$d_0 = \overline{X}\,\overline{q_0} + q_1 \overline{q_0} + X \overline{q_1} q_0$$

• λ function:

$q_1 q_0$	00	01	11	10
	0	0	0	1

$$Z = q_1 \overline{q_0}$$

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9) Circuit Diagram :