Mittuniversitetet
MID SWEDEN UNIVERSITY

Exam – ET061G – 22 Augusti 2019

Digitalteknik med VHDL

Time	5 hours
Support material	none
No. of questions	6
No. of pages	7
No. of points	50 (25 for passed)

- Please hand in one task per page.
- Rationale may not be so scarce that they become difficult to follow.
- Reasoning behind equations should be explained.
- Calculations shall be sufficiently complete to show how the result was obtained.
- Each task must be concluded with a clearly written answer.

David Krapohl, tel: 010-142 8755, e-post: david.krapohl@miun.se

Tasks

Exercise 1.

a) Convert the following decimal number to hexadecimal, octal and binary notation: 3 P.

$$15.25_{10}$$

b) Use the left-shift operation to calculate the binary result using 8-bit registers: 2 P.

$$111011_2 \times 8_{10}$$

c) Calculate two's complement of -39 using 8 bit registers. 2 P.

Solution 1.

a)

$$\begin{aligned} \text{binary: } & 001111.01_2 \\ & \underbrace{001}_{1}\underbrace{111}_{7}.\underbrace{010}_{2} \\ & \underbrace{1111}_{F}.\underbrace{0100}_{4} \\ \text{octal: } & 17.2_8 \\ \text{hex: } & F.4_{16} \end{aligned}$$

b) vänsterskift 3x

$$\begin{aligned} & 111011 << 3 \\ \Rightarrow & [1]11011000_2 \end{aligned}$$

c) -39 in two's complement with 8 bit registers.

$$\begin{array}{rl} & 0010\,0111 \\ \Rightarrow & 1101\,1000 \\ + & 0000\,0001 \\ = & 1101\,1001 \end{array}$$

Exercise 2.

a) Determine if the following equality is true: 4 P.

$$(a + \bar{b})c = (a\bar{b}c) + \overline{(\bar{a}b)}c$$

b) Minimise the following Boolean equation: 4 P.

$$\bar{a} \cdot \bar{c} \cdot \bar{d} + \overline{(a \cdot d)}$$

c) Minimise the function $f(abcd) = \sum(0, 5, 6, 7, 8, 9, 13, 14, 15) + d(2, 4, 10, 12)$ with the help of a Karnaugh-map. Draw a gate level diagram for the minimised expression. 5 P.

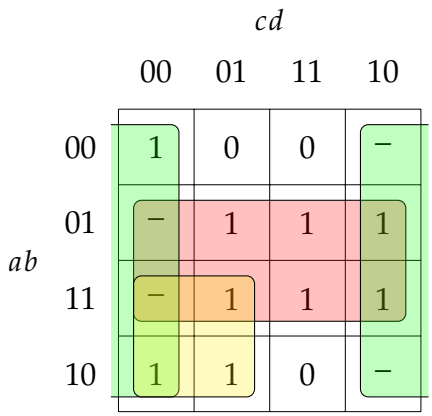
Solution 2.

a) yes, they are the same.

$$\begin{aligned}
&= a\bar{b}c + (\bar{\bar{a}} + \bar{b})c \\
&= a\bar{b}c + ac + \bar{b}c \\
&= (a\bar{b} + a + \bar{b})c \\
&= (a(\bar{b} + 1) + b)c \\
&= (a + \bar{b})c
\end{aligned}$$

b) Fastest solution:

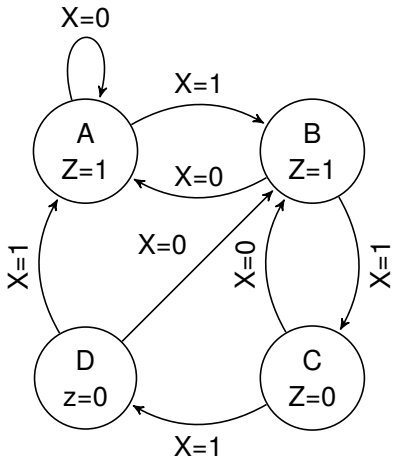
$$\begin{aligned}
&= \bar{a} \cdot \bar{c} \cdot \bar{d} + \overline{a \cdot d} \\
&= \bar{a} \cdot \bar{c} \cdot \bar{d} + \bar{a} + \bar{d} \\
&= \bar{a}(\bar{c} \cdot \bar{d} + 1) + \bar{d} \\
&= \bar{a} + \bar{d}
\end{aligned}$$



c) $f = \bar{d} + b + a\bar{c}$

Exercise 3.

Develop Boolean expressions that model the behaviour of the state machine below. 6 P.
Use binary coding and D-flipflops.



Solution 3.

State table

	0	1	
A	A	B	1
B	A	C	1
C	B	D	0
D	B	A	0

Transition table

	0	1	
00	00	01	1
01	00	10	1
10	01	11	0
11	01	00	0

Exitation table

	0	1	
00	00	01	1
01	00	10	1
10	01	11	0
11	01	00	0

E \ q_1q_0	00	01	11	10
0	0	0	0	0
1	0	1	0	1

$$d_0 = E\overline{q_1}q_0 + Eq_1\overline{q_0}$$

E \ q_1q_0	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$d_1 = \overline{E}q_1 + q_1\overline{q_0} + E\overline{q_0}$$

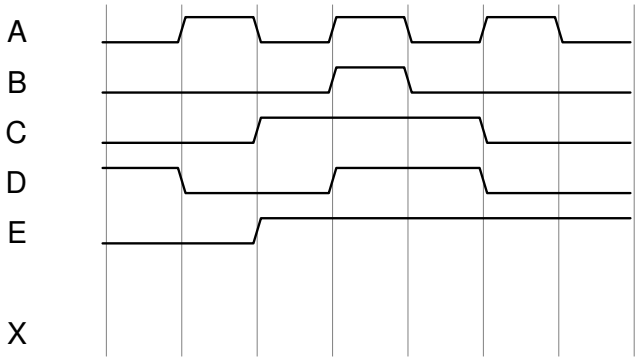
$$z = \overline{q_1}$$

Exercise 4.

Draw a gate level diagram for the equation below and complete the waveform output for X.

$$X = AB + \overline{A}B + C\overline{D} + D\overline{E} + \overline{B}C \quad (1)$$

4 P.



4 P.

Solution 4.

Exercise 5.

Write the truth table and draw the gate level diagram for a full adder. Complete the VHDL code below to achieve the same functionality. XOR can be used. 9 P.

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3
4  entity full_adder is
5      Port ( a : in STD_LOGIC;
6      b : in STD_LOGIC;
7      Cin : in STD_LOGIC;
8      sum : out STD_LOGIC;
9      Cout : out STD_LOGIC);
10 end full_adder;
11
12 architecture behaviour of full_adder is
13 begin
14     -------------------------------
15     -- <<<write your code here>>>
16     -------------------------------
17 end behaviour;
```

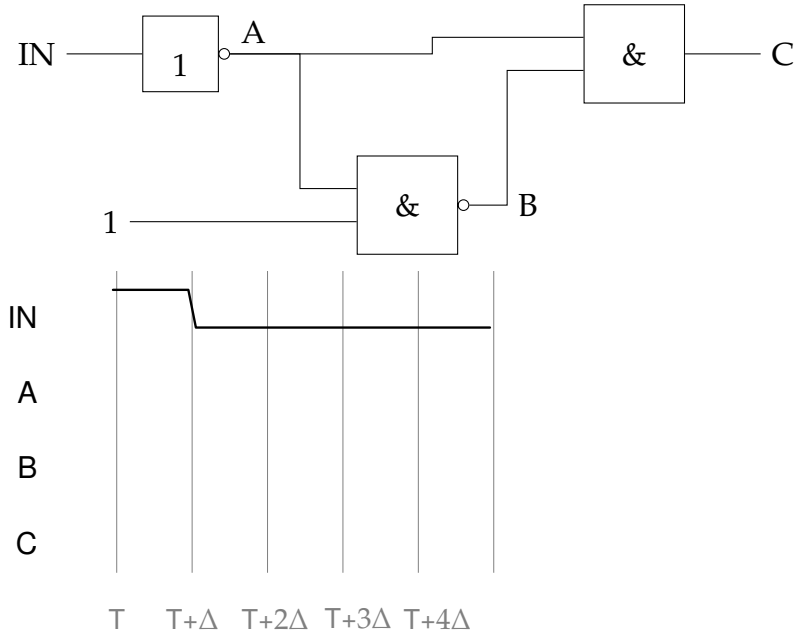
Solution 5.

Different solutions possible

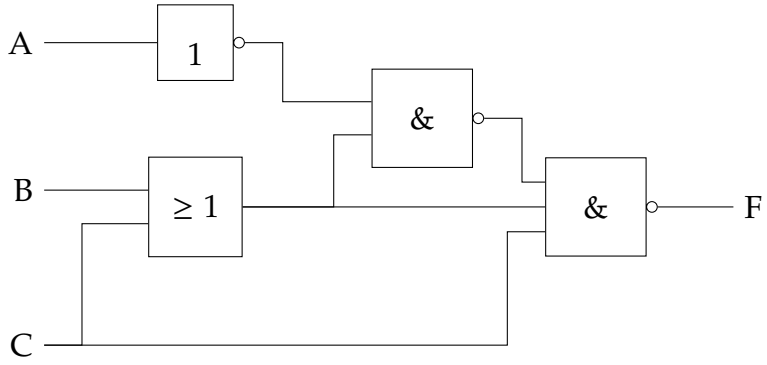
```
1
2
3  -- ----------------------
4      sum <= a xor b xor Cin;
5      Cout <= ((a xor b) and Cin)  or (a and b);
```

Exercise 6.

a) Draw or describe the signal behaviour for A, B and C with respect to delta delay when the input signal switches from 1 to 0. 4 P.



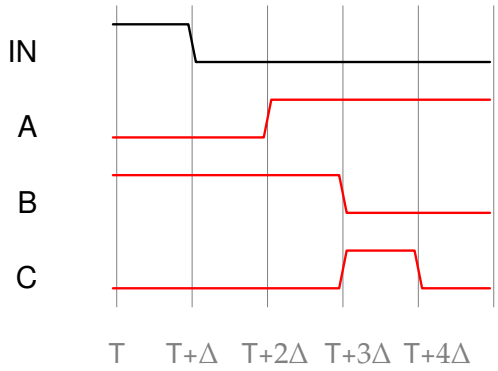
b) Calculate the maximum gate delay path for the following gate level circuit with the given delays. 3 P.



Gates	Delay
inverter	0.1ns
nand	0.4ns
and	0.9ns
or	0.3ns

Solution 6.

a)



b) Gate delays:

$$0.3ns + 0.4ns + 0.4ns = \underline{1.1ns}$$