Laboration 3

# Digitalteknik med VHDL
# Adder

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## 1 4-Bit components

In this lab we will be creating different components that can be re-used in the future lab. Emphasis now is on designing, simulating and verifying that the components are implemented according to specifications. We will focus more on SIMULATION. Addition and Multiplication has been attempted in Lab 2. The other components can be achieved based on a hints.

## 2 Design the components

Create the following 4-bit arithmetic operator modules:

- adder (**add4**)
  Hint: ('0' & in_1) + ('0' & in_2)
- multiplicator (**mul4**)
  Hint: in_1 * in_2
- inverter (**invrt4**)
  Hint: NOT(in_1)
- bitwise and (**bit_and4**)
  Hint: (in_1 AND in_2)
- bitwise or (**bit_or4**)
  Hint: (in_1 OR in_2)

```
entity add4 is -- s_out <= ( '0' & in_1 ) + ( '0' & in_2 )
Port ( in_1 : in STD_LOGIC_VECTOR (3 downto 0);
in_2 : in STD_LOGIC_VECTOR (3 downto 0);
s_out : out STD_LOGIC_VECTOR (4 downto 0));
end add4;

entity mul4 is -- m_out <= in_1 * in_2
Port ( in_1 : in STD_LOGIC_VECTOR (3 downto 0);
```

```
in_2 : in STD_LOGIC_VECTOR (3 downto 0);
m_out : out STD_LOGIC_VECTOR (7 downto 0));
end mul4;

entity invrt4 is -- i_out <= NOT ( in_1 )
Port ( in_1 : in STD_LOGIC_VECTOR (3 downto 0);
i_out : out STD_LOGIC_VECTOR (3 downto 0));
end invrt;

entity bit_and4 is -- a_out <= ( in_1 AND in_2 )
Port ( in_1 : in STD_LOGIC_VECTOR (3 downto 0);
in_2 : in STD_LOGIC_VECTOR (3 downto 0);
a_out : out STD_LOGIC_VECTOR (3 downto 0));
end bit_and4;

entity bit_or4 is -- o_out <= ( in_1 OR in in_2 )
Port ( in_1 : in STD_LOGIC_VECTOR (3 downto 0);
in_2 : in STD_LOGIC_VECTOR (3 downto 0);
o_out : out STD_LOGIC_VECTOR (3 downto 0));
end bit_or4;
```

## 3 Simulation

Simulate the components and confirm their correct behaviour. To do this create a simulation test-bench that generates two 4-bit counters in two for-loops such that one for-loop is embedded inside the other. Use the simulation test-bench `add8_tb.vhd` in lab 2, section 2.2 as hint. It is recommended to simulate all the components together so that the results can be seen and reported easily using only one waveform.

## 4 Report

Write a report with six sections, one for each of the arithmetic operators and the testbench. In each section of the first 5 sections of the report include VHDL-code as text (not as images) and understandable results from simulations (as screenshot not as phone snapshot). In section six of the report, explain how your test bench works. Submit your report via the Moodle page according to the deadline specified.