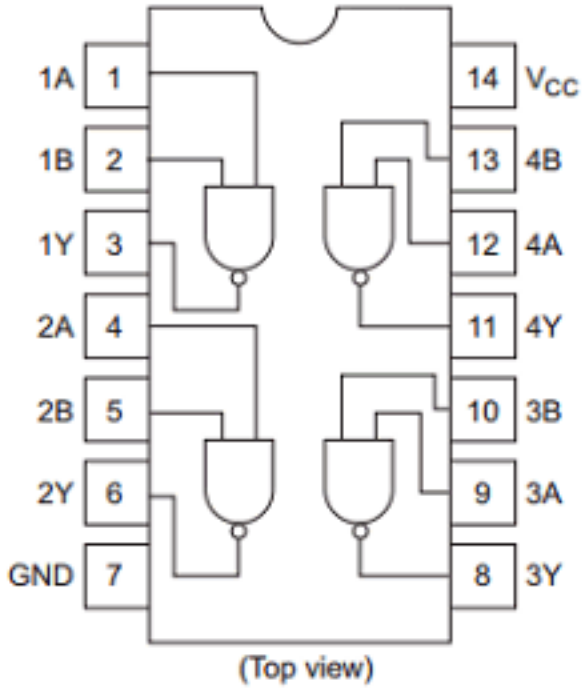
Johannes Joujo

Task 1



Länk

Port 1 and 2 are 1A and 1B into a nand gate that gives the result to the 1Y.

Port 4 and 5 are 2A and 2B into a nand gate that gives the result to 2Y.

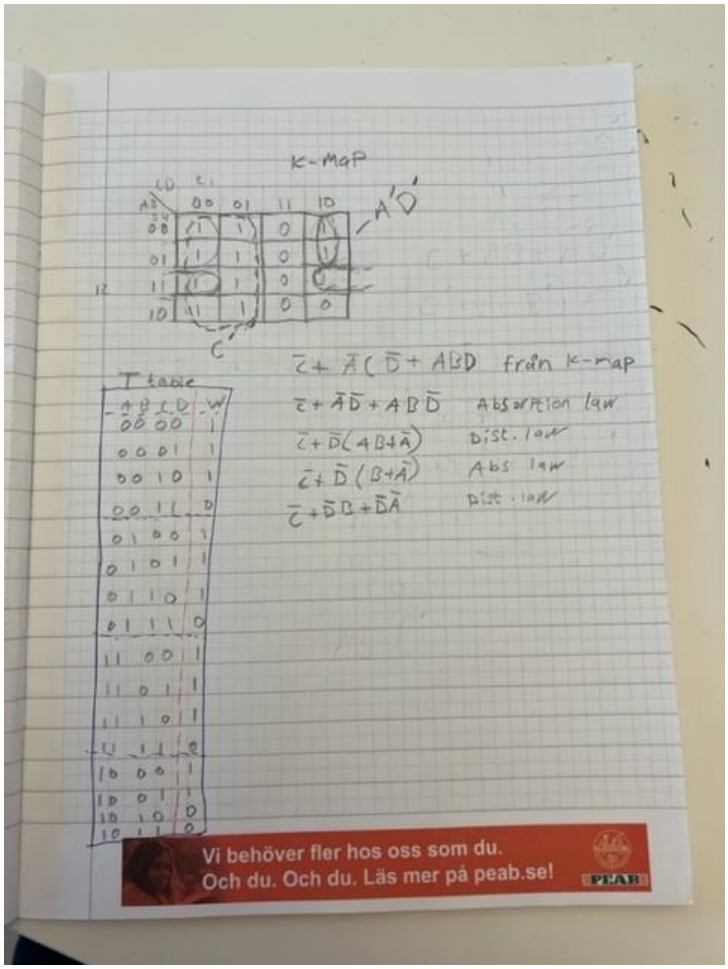
Number 7 is ground.

Number 14 is the common collector voltage.

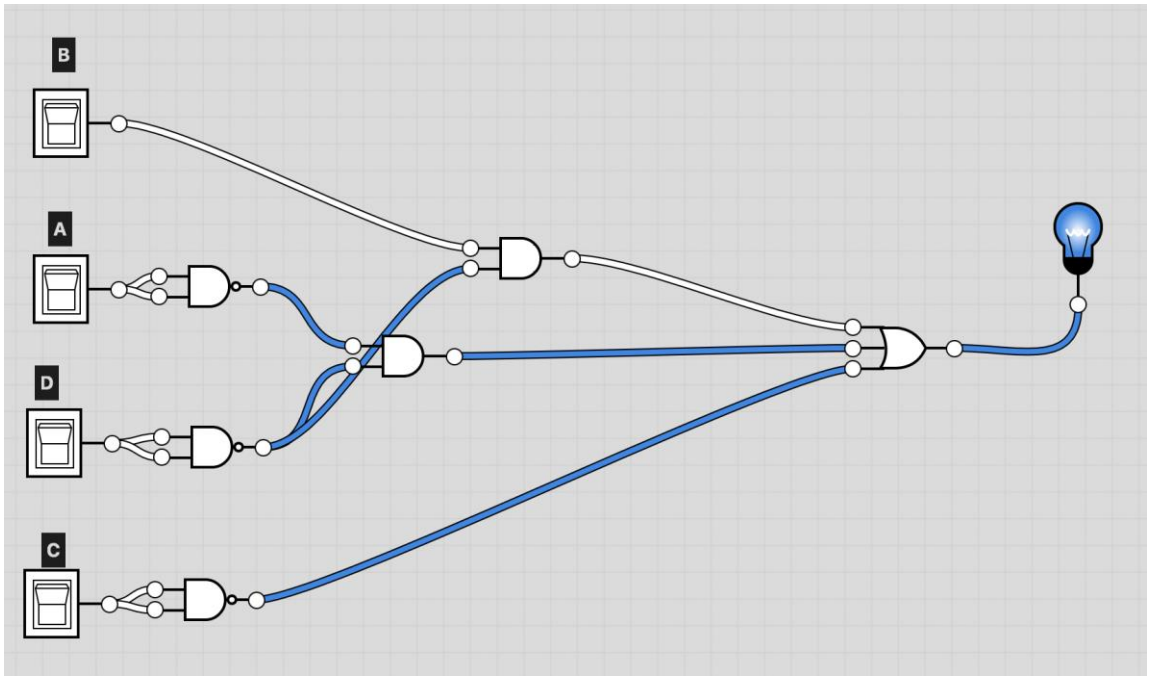
In the same was as above 4B and 4A goes into a nand gate and give the result through port 11 which is 4Y.

Port 10 and 9 goes into a nand gate that gives the result to port 8.

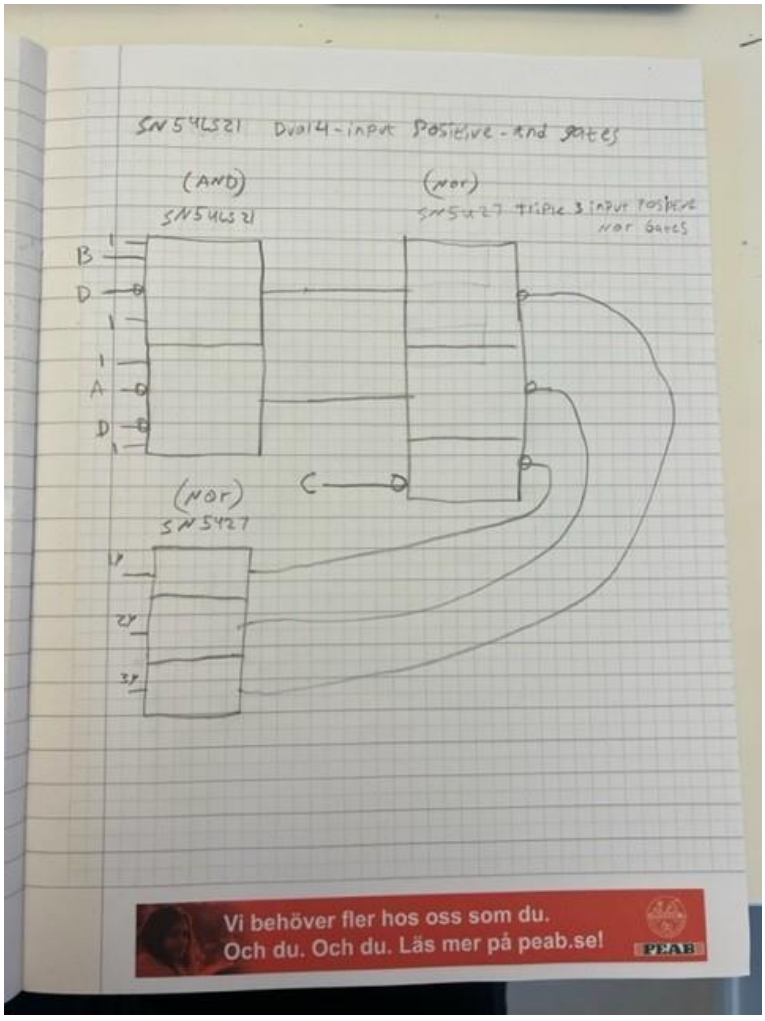
Task 2


K-MaP
T table
$\bar{C} + \bar{A}C\bar{D} + A\bar{B}D$ från K-map
$\bar{C} + \bar{A}\bar{D} + AB\bar{D}$ Absorption law
$\bar{C} + \bar{D}(AB + \bar{A})$ Dist. law
$\bar{C} + \bar{D}(B + \bar{A})$ Abs law
$\bar{C} + \bar{D}B + \bar{D}\bar{A}$ Dist. law
Vi behöver fler hos oss som du.
Och du. Och du. Läs mer på peab.se!
PEAB

Task 3


B
A
D
C

Task 4


SN54LS21 Dual 4-input Positive-and gates
(AND)
SN54LS21
(NOR)
B
D
A
D
C
(NOR)
SN5427
Vi behöver fler hos oss som du.
Och du. Och du. Läs mer på peab.se!
PEAB

I was thinking that B and D’ would go in to the first and gate with two 1 because the result will still be dependent on the value of B and D’. Same with A’ and D’. The outputs go into an nor gate with C’, because it's a nor gate I use it again to switch the values back to what they are supposed to be.

3 report

I searched 74HC00 and copied a picture of the circuit, I also searched what each port does.

In task 2 I used my knowledge and drew a k-map with a truth table. I paired the ones and got a expression from the k-map I later simplified it with the laws.

In task 3 I followed the simplified version of that expression and used gates to visualize it, I used the truth table to control if it was correct and it gave the same answers on the output.

In task 4 I found an AND and an XOR 74HC00 series that I could use.