Mittuniversitetet
MID SWEDEN UNIVERSITY

Exam – ET061G – 9 Juni 2021

Digitalteknik med VHDL

Time	4 hours
Support material	none
No. of questions	6
No. of pages	6
No. of points	50 (25 for passed)

- Please hand in one task per page.
- Rationale may not be so scarce that they become difficult to follow.
- Reasoning behind equations should be explained.
- Calculations shall be sufficiently complete to show how the result was obtained.
- Each task must be concluded with a clearly written answer.
- The exam must be solved individually.

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Tasks

Exercise 1.

a) Convert the following octal number to hexadecimal, decimal using binary numbers notation: 3 P.

$$\mathbf{71.72_8}$$

b) Use the shift operation to calculate the binary result using 8-bit registers: 2 P.

$$\mathbf{01101010_2 \div 16_{10}}$$

c) Calculate $\mathbf{33 - 37}$ using 8 bit registers. 2 P.

Exercise 2.

a) Determine if the following equality is true: 4 P.

$$\overline{\mathbf{xy} + \mathbf{xy} \cdot \overline{\mathbf{x} \cdot \mathbf{y}}} = (\overline{\mathbf{xy} + \mathbf{xy}}) \cdot \mathbf{1}$$

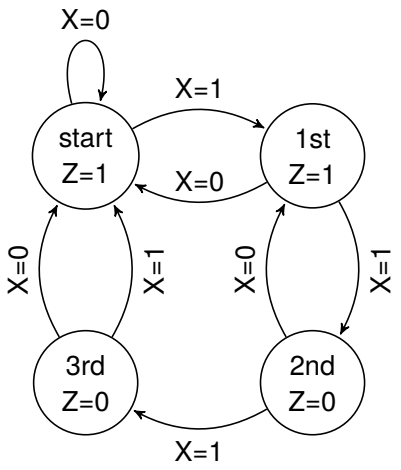
b) Minimise the following Boolean equation: 4 P.

$$\mathbf{abc} + \mathbf{ab} + (\overline{\mathbf{ac}} \cdot \mathbf{a} + \overline{\overline{\mathbf{ac}}} \cdot \mathbf{a})$$

c) Minimise the function $\mathbf{f(abcd)} = \sum(\mathbf{2, 5, 10, 13}) + \mathbf{d}(\mathbf{7, 13})$ to product of sums-form with the help of a Karnaugh-map. Draw a gate level diagram for the minimised expression. 5 P.

Exercise 3.

Create the Boolean expressions that describe the behaviour of the state graph below. 6 P.
Use binary code and T-flipflops. The characteristic equation is $Q^+ = \bar{T}Q + T\bar{Q}$ (hint: rewrite to table).

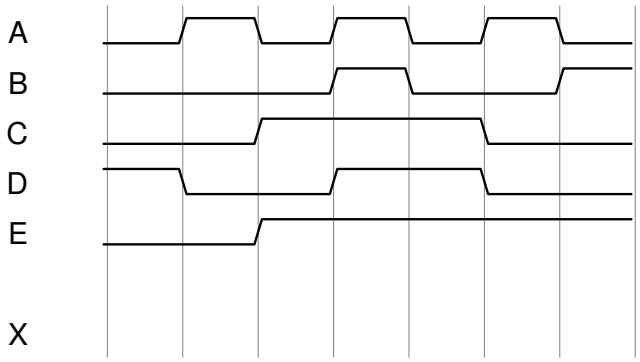


Exercise 4.

a) Draw a gate level diagram for the equation below and complete the waveform output for X.

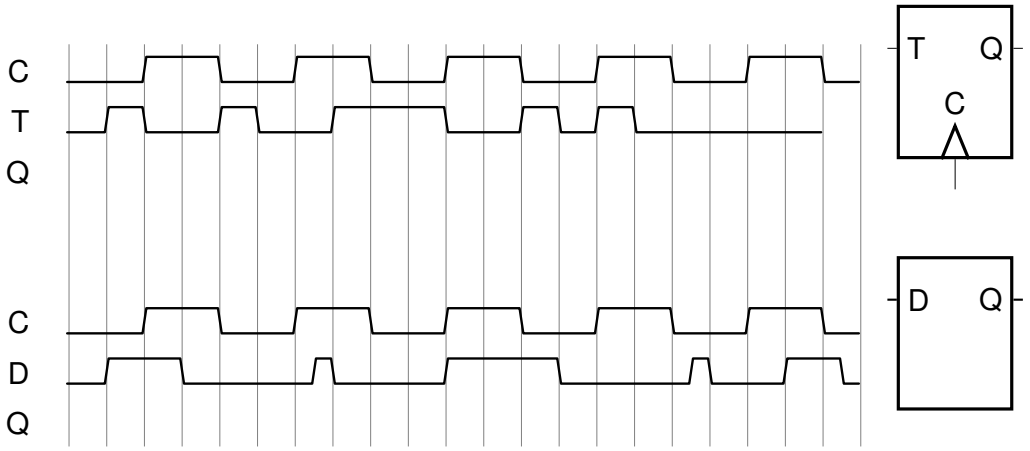
$$X = \overline{AB} + A\overline{B} + C\overline{D} + DE + \overline{B}C \quad (1)$$

2 P.



2 P.

b) Decide on the type of device and complate the timeing diagram for Q. You can draw in the image and include it into your submission. 4 P.



Exercise 5.

Below is a state machine in VHDL code. What kind of state machine is it? What does it do? Draw the state diagram with all inputs and states! 9 P.

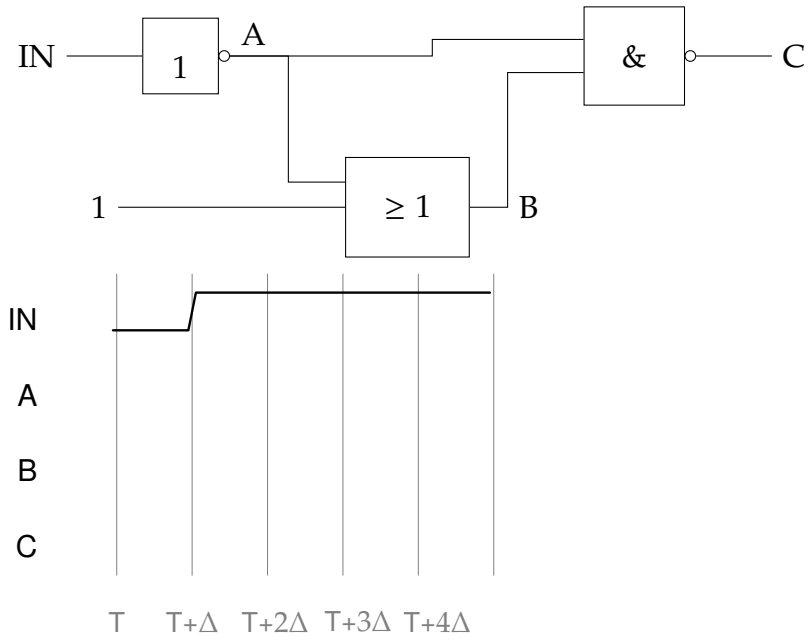
```
1 library ieee;
2 use ieee. std_logic_1164.all;
3
4 entity seqdata is
5   port (clk: in std_logic; -- klocka
6         clr: in std_logic; -- starta om
7         din: std_logic;    -- sekvens input
```

```
8         z: out std_logic); -- output
9  end seqdata;
10
11 architecture seqdata of seqdata is
12 type state_type is (s0, s1, s2, s3, s4);
13 signal present_state, next_state: state_type;
14
15 begin
16
17 sres: process(clk, clr) -- reset och forandring av tillstand
18     begin
19         if clr = '1' then
20             present_state <= s0;
21         elsif clk'event and clk = '1' then
22             present_state <= next_state;
23         end if;
24     end process;
25
26 state: process (present_state, din) -- logik for tillstand
27     begin
28   case present_state is
29     when s0 =>
30       if din = '0' then
31         next_state <= s1;
32       else
33         next_state <= s0;
34     when s1 =>
35       if din = '1' then
36         next_state <= s2;
37       else
38         next_state <= s1;
39     when s2 =>
40       if din = '1' then
41         next_state <= s3;
42       else
43         next_state <= s1;
44     when s3 =>
45       if din = '0' then
46         next_state <= s4;
47       else
48         next_state <= s2;
49     when s4 =>
50       if din = '1' then
51         next_state <= s2;
52       else
53         next_state <= s1;
```

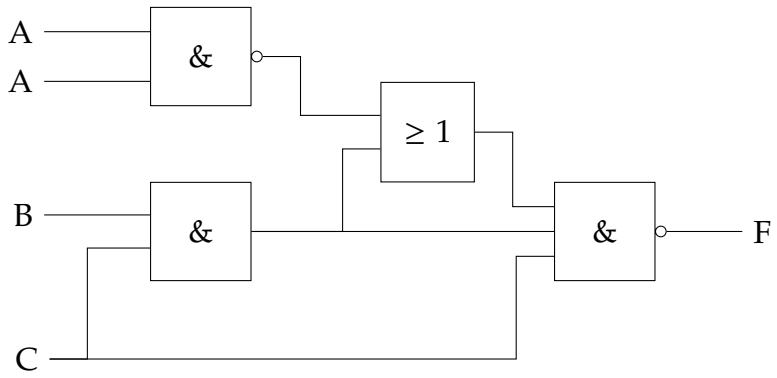
```
54      when others =>
55        null;
56    end case;
57    end process;
58
59  outp: process (present_state) -- output
60      z <= '1';
61      if present_state = 's4' then
62          z <= '0';
63    end process;
64
65  end seqdata;
```

Exercise 6.

a) Draw or describe the signal behaviour for A, B and C with respect to delta delay when the input signal switches from 0 to 1. 4 P.



b) Calculate the maximum gate delay path for the following gate level circuit with the given delays. 3 P.



Gates	Delay
inverter	0.1ns
nand	0.4ns
and	0.9ns
or	0.3ns