

#### **LEGAL NOTICE:**

© Copyright 2008 to 2022 NVM Express, Inc. ALL RIGHTS RESERVED.

This erratum is proprietary to the NVM Express, Inc. (also referred to as "Company") and/or its successors and assigns.

NOTICE TO USERS WHO ARE NVM EXPRESS, INC. MEMBERS: Members of NVM Express, Inc. have the right to use and implement this erratum subject, however, to the Member's continued compliance with the Company's Intellectual Property Policy and Bylaws and the Member's Participation Agreement.

NOTICE TO NON-MEMBERS OF NVM EXPRESS, INC.: If you are not a Member of NVM Express, Inc. and you have obtained a copy of this document, you only have a right to review this document or make reference to or cite this document. Any such references or citations to this document must acknowledge NVM Express, Inc. copyright ownership of this document. The proper copyright citation or reference is as follows: "© 2008 to 2022 NVM Express, Inc. ALL RIGHTS RESERVED." When making any such citations or references to this document you are not permitted to revise, alter, modify, make any derivatives of, or otherwise amend the referenced portion of this document in any way without the prior express written permission of NVM Express, Inc. Nothing contained in this document shall be deemed as granting you any kind of license to implement or use this document or the specification described therein, or any of its contents, either expressly or impliedly, or to any intellectual property owned or controlled by NVM Express, Inc., including, without limitation, any trademarks of NVM Express, Inc.

#### **LEGAL DISCLAIMER:**

THIS DOCUMENT AND THE INFORMATION CONTAINED HEREIN IS PROVIDED ON AN "AS IS" BASIS. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, NVM EXPRESS, INC. (ALONG WITH THE CONTRIBUTORS TO THIS DOCUMENT) HEREBY DISCLAIM ALL REPRESENTATIONS, WARRANTIES AND/OR COVENANTS, EITHER EXPRESS OR IMPLIED, STATUTORY OR AT COMMON LAW, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, VALIDITY, AND/OR NONINFRINGEMENT.

All product names, trademarks, registered trademarks, and/or servicemarks may be claimed as the property of their respective owners.

The NVM Express® design mark is a registered trademark of NVM Express, Inc. PCI-SIG®, PCI Express®, and PCIe® are registered trademarks of PCI-SIG. InfiniBand™ is a trademark and servicemark of the InfiniBand Trade Association.

NVM Express Workgroup c/o VTM Group 3855 SW 153<sup>rd</sup> Drive Beaverton, OR 97003 USA info@nvmexpress.org

# **NVM Express® Technical Errata**

Errata ID	107
Revision Date	07/10/2022
Affected Spec Ver.	NVM Express® Base Specification Revision 2.0a
Corrected Spec Ver.	

#### Errata Author(s)

Name	Company
Mike Allison, Judy Brock, Bill Martin	Samsung

#### **Errata Overview**

This ECN is an effort to get consistency on formatting within the NVMe 2.0 family of specifications.

**Revision History** 

ite vision i nstory	
Revision Date	Change Description
1/4/2022	Initial creation
1/6/2022	Added the changes for NOTES and KEYS.
1/10/2022	Changed Namespace commands to Namespace Management commands in section 3.1.2.2. Added a note to a change in punctuation that was hard to see.
2/11/2022	Corrected trademarks and copyright dates.
3/3/2022	Fixed trademark.
7/6/2022	Integrated
7/10/2022	Editorial changes per Mike Allison

# **Description of Changes**

#### **NVM Express Base Specification 2.0a**:

- Updated lists to include and/or designations
- Removed optional support designations as the support is already defined in another section of the specification.
- Moved optional designations to be done by controller type.
- Properly states the optional support for the Vendor Specific properties.
- Reduce the definition of the Power State descriptions by utilizing ... to show the sequence of entries.
- Editorial fixes on punctuation.

#### Editor's Note:

**BLACK** text indicates unchanged text; **BLUE** text indicates newly inserted text, **RED** text indicates deleted text; **GREEN** text indicates editor notes.



## **Description of NVM Express Base Specification 1.0a changes:**

<The specification is inconsistent on capitalization of the words "Notes" and "Keys" in figures. The decision is to use capitalized words instead of all caps. Therefore the following changes need to occur:</p>

Change "KEY" to "Key" globally in figure notes, Change "NOTES" to "Notes" globally in figure notes.>

# 3 **NVM Express Architecture**

•••

3.1 NVM Controller Architecture

...

3.1.2 Controller Types

...

#### 3.1.2.2 Administrative Controller

An Administrative controller is a controller whose intended purpose is to provide NVM subsystem management capabilities. While an I/O controller may support these same management capabilities, an Administrative controller has fewer mandatory capabilities. Unlike an I/O controller, an Administrative controller does not support I/O commands that access to user data stored on an NVM subsystem's non-volatile storage medium. NVMe Transports may support a transport specific mechanism to allow an Administrative controller to load a dedicated NVMe management driver instead of a generic NVMe driver (refer to the applicable NVMe Transport binding specification for details).

Examples of management capabilities that may be supported by an Administrative controller include the following.

- Ability to efficiently poll NVM subsystem health status via NVMe-MI using the NVMe-MI Send and NVMe-MI Receive commands (refer to the NVM Subsystem Health Status Poll section in the NVMe Management Interface specification);
- Ability to manage an NVMe enclosure via NVMe-MI using the NVMe-MI Send and NVMe-MI Receive commands;
- Ability to manage NVM subsystem namespaces using the Namespace Attachment and Namespace Management commands;
- Ability to perform virtualization management using the Virtualization Management command; and
- Ability to reset an entire NVM subsystem using the NVM Subsystem Reset (NSSR) register if supported-; and
- Ability to shutdown an entire NVM subsystem using the NVM Subsystem Shutdown (NSSD) property.

..

#### 3.1.2.3 Discovery Controller

...

#### 3.1.2.3.4 Features Support

•••

#### 3.1.2.3.4.1 Asynchronous Event Configuration (Feature Identifier 0Bh), (Optional)

•••

### 3.1.3 Controller Properties

...

**Figure 35: Property Definition** 

Offset (OFST)	Size (in bytes)	I/O Controller <sup>1</sup>	Admin. Controller <sup>1</sup>	Discovery Controller <sup>1</sup>	Name
1000h		T	Т	T	Transport Specific
1300h		0	0	0	Vendor Specific (Optional)

#### Notes:

- 1. O/M/P definition: O = Optional, M = Mandatory, R = Reserved, T = Transport Specific
- 2. Mandatory for memory-based transport implementations. Reserved for message-based transport implementations.
- 3. Optional for memory-based transport implementations. Reserved for message-based transport implementations.

...

#### 3.1.3.6 Offset 1Ch: CSTS - Controller Status

Figure 47: Offset 1Ch: CSTS - Controller Status

Bits	Type	Reset <sup>1</sup>	Description
31:07	RO	0h	Reserved
06	RO	Impl Spec	Shutdown Type (ST): When CSTS.SHST is set to a non-zero value, then this bit indicates the type of shutdown reported by CSTS.SHST. If this bit is set to '1', then CSTS.SHST is reporting the state of an NVM Subsystem Shutdown. If this bit is cleared to '0', then CSTS.SHST is reporting the state of a controller shutdown.  If CSTS.SHST is cleared to 00b, then this bit is ignored.
05	RO	0b	<b>Processing Paused (PP):</b> This bit indicates whether the controller is processing commands. If this bit is cleared to '0', then the controller is processing commands normally. If this bit is set to '1', then the controller has temporarily stopped processing commands in order to handle an event (e.g., firmware activation). This bit is only valid when CC.EN is set to —'1'.
l			

...

#### 3.1.3.15 Offset 48h: BPMBL – Boot Partition Memory Buffer Location (Optional)

This optional property specifies the memory buffer that is used as the destination for data when a Boot Partition is read (refer to section 8.2). If the controller does not support the Boot Partitions feature, then this property shall be cleared to 0h.

Figure 56: Offset 48h: BPMBL - Boot Partition Memory Buffer Location (Optional)

Bits	Type	Reset	Description
63:12	RW	0h	<b>Boot Partition Memory Buffer Base Address (BMBBA):</b> This field specifies the 52 most significant bits of the 64-bit physical address for the Boot Partition Memory Buffer.
11:00	RO	0h	Reserved

•••

#### 3.5 Controller Initialization

#### 3.5.1 Memory-based Transport Controller Initialization

Upon completion of the transport-specific controller initialization steps defined within the relevant NVMe Transport binding specification, the host should perform the following sequence of actions to initialize the controller to begin executing commands:

- The host waits for the controller to indicate that any previous reset is complete by waiting for CSTS.RDY to become '0':
- The host configures the Admin Queue by setting the Admin Queue Attributes (AQA), Admin Submission Queue Base Address (ASQ), and Admin Completion Queue Base Address (ACQ) to appropriate values;
- The host determines the supported I/O Command Sets by checking the state of CAP.CSS and appropriately initializing CC.CSS as follows:
  - a. If the CAP.CSS bit 7 is set to '1', then the CC.CSS field should be set to 111b;
  - b. If the CAP.CSS bit 6 is set to '1', then the CC.CSS field should be set to 110b; and
  - c. If the CAP.CSS bit 6 is cleared to '0' and bit 0 is set to '1', then the CC.CSS field should be set to 000b:
- 4. The controller settings should be configured. Specifically:
  - a. The arbitration mechanism should be selected in CC.AMS; and
  - b. The memory page size should be initialized in CC.MPS;
- 5. The host enables the controller by setting CC.EN to '1';
- 6. The host waits for the controller to indicate that the controller is ready to process commands. The controller is ready to process commands when CSTS.RDY is set to '1';
- 7. The host determines the configuration of the controller by issuing the Identify command specifying the Identify Controller data structure (i.e., CNS 01h);
- 8. The host determines any I/O Command Set specific configuration information as follows:
  - a. If the CC.CSS field is set to 000b, then the host should determine the configuration of each namespace by issuing the Identify command for each namespace, specifying the Identify Namespace data structure (CNS 00h);
  - b. If the CAP.CSS bit 6 is set to '1', then the host does the following:
    - Issue the Identify command specifying the Identify I/O Command Set data structure (CNS 1Ch):
    - ii. Issue the Set Features command with the I/O Command Set Profile Feature Identifier (FID 19h) specifying the index of the I/O Command Set Combination (refer to Figure 289) to be enabled;
    - iii. For each I/O Command Set that is enabled:
      - 1. Issue the Identify command specifying the I/O Command Set specific Active Namespace ID list (CNS 07h) with the appropriate Command Set Identifier (CSI) value of that I/O Command Set; and
      - 2. For each NSID that is returned:
        - a. If the enabled I/O Command Set is the NVM Command Set or an I/O Command Set based on the NVM Command Set (e.g., the Zoned Namespace Command Set) issue the Identify command specifying the Identify Namespace data structure (CNS 00h); and
        - Issue the Identify command specifying each of the following data structures (refer
          to Figure 274): the I/O Command Set specific Identify Namespace data structure,
          the I/O Command Set specific Identify Controller data structure, and the I/O
          Command Set independent Identify Namespace data structure;
- 9. If the controller implements I/O queues, then the host should determine the number of I/O Submission Queues and I/O Completion Queues supported using the Set Features command with the Number of Queues feature identifier. After determining the number of I/O Queues, the

- NVMe Transport specific interrupt registers (e.g. MSI and/or MSI-X registers) should be configured:
- 10. If the controller implements I/O queues, then the host should allocate the appropriate number of I/O Completion Queues based on the number required for the system configuration and the number supported by the controller. The I/O Completion Queues are allocated using the Create I/O Completion Queue command;
- 11. If the controller implements I/O queues, then the host should allocate the appropriate number of I/O Submission Queues based on the number required for the system configuration and the number supported by the controller. The I/O Submission Queues are allocated using the Create I/O Submission Queue command; and
- 12. To enable asynchronous notification of optional events, the host should issue a Set Features command specifying the events to enable. To enable asynchronous notification of events, the host should submit an appropriate number of Asynchronous Event Request commands. This step may be done at any point after the controller signals that the controller is ready (i.e., CSTS.RDY is set to '1').

•••

#### 3.5.2 Message-based Transport Controller Initialization

...

The controller initialization steps after an association is established are described below. For determining capabilities or configuring properties, the host uses the Property Get and Property Set commands, respectively.

- 1. NVMe in-band authentication is performed if required (refer to section 8.13.2);
- 2. The host determines the controller capabilities;
- 3. The host determines the supported I/O Command Sets by checking the state of CAP.CSS and appropriately initializing CC.CSS as follows:
  - a. If the CAP.CSS bit 7 is set to '1', then the CC.CSS field should be set to 111b;
  - b. If the CAP.CSS bit 6 is set to '1', then the CC.CSS field should be set to 110b; and
  - c. If the CAP.CSS bit 6 is cleared to '0' and bit 0 is set to '1', then the CC.CSS field should be set to 000b;
- 4. The host configures controller settings. Specific settings include:
  - a. The arbitration mechanism should be selected in CC.AMS: and
  - b. The memory page size should be initialized in CC.MPS:
- 5. The controller should be enabled by setting CC.EN to '1';
- 6. The host should wait for the controller to indicate the controller is ready to process commands. The controller is ready to process commands when CSTS.RDY is set to '1';
- 7. The host determines the configuration of the controller by issuing the Identify command specifying the Identify Controller data structure (i.e., CNS 01h);
- 8. The host determines any I/O Command Set specific configuration information as follows:
  - a. If the CC.CSS field is set to 000b, then the host should determine the configuration of each namespace by issuing the Identify command for each namespace, specifying the Identify Namespace data structure (CNS 00h); and
  - b. If the CAP.CSS bit 6 is set to '1', then the host does the following:
    - Issue the Identify command specifying the Identify I/O Command Set data structure (CNS 1Ch);
    - ii. Issue the Set Features command with the I/O Command Set Profile Feature Identifier (FID 19h) specifying the index of the I/O Command Set Combination (refer to Figure 289) to be enabled; and
    - iii. For each I/O Command Set that is enabled:
      - 1. Issue the Identify command specifying the I/O Command Set specific Active Namespace ID list (CNS 07h) with the appropriate Command Set Identifier (CSI) value of that I/O Command Set; and

#### 2. For each NSID that is returned:

- a. If the enabled I/O Command Set is the NVM Command Set or an I/O Command Set based on the NVM Command Set (e.g., the Zoned Namespace Command Set) issue the Identify command specifying the Identify Namespace data structure (CNS 00h); and
- b. Issue the Identify command specifying each of the following data structures (refer to Figure 274): the I/O Command Set specific Identify Namespace data structure, the I/O Command Set specific Identify Controller data structure, and the I/O Command Set independent Identify Namespace data structure;

#### 9. The host should determine:

- a. the maximum I/O Queue size using CAP.MQES; and
- b. the number of I/O Submission Queues and I/O Completion Queues supported using the response from the Set Features command with the Number of Queues feature identifier;
- 10. The host should use the Connect command (refer to section 6.3) to create I/O Submission and Completion Queue pairs; and
- 11. To enable asynchronous notification of optional events, the host should issue a Set Features command specifying the events to enable. The host may submit one or more Asynchronous Event Request commands to be notified of asynchronous events as described by section 5.2. This step may be done at any point after the controller signals that the controller is ready (i.e., CSTS.RDY is set to '1').

...

#### 3.5.3 Controller Ready Modes During Initialization

...

The controller shall be able to process without error as described in section 3.5.4.1.:<change period to colon>

- a) all Admin commands not listed in Figure 103 by the time the controller is ready;
- b) all Admin commands listed in Figure 103 within, up to, and including CRTO.CRWMT amount of time after the controller is enabled; and
- all NVM commands within, up to, and including CRTO.CRWMT amount of time after the controller is enabled.

...

#### 3.5.4 Controller Ready Timeouts During Initialization

. . .

The details regarding these timeouts during controller initialization are as follows:

- a) The CAP.TO field shall be set as described in Figure 36-; < Note: changing a period to semicolon>
- b) If the CAP.CRMS field is cleared to 00b', then:
  - i. the Controller Ready Independent of Media Timeout (CRTO.CRIMT) field is reserved;
  - ii. the Controller Ready With Media Timeout (CRTO.CRWMT) field is reserved; and
  - iii. the worst-case time the host should wait after the controller is enabled (i.e., CC.EN transitions from '0' to '1') for the controller to become ready (CSTS.RDY transitions from '0' to '1') is indicated by CAP.TO-; <Note: changing a period to semicolon>
- c) If the controller is in Controller Ready With Media mode (i.e., the CC.CRIME bit is cleared to '0'), then:
  - the Controller Ready Independent of Media Timeout (CRTO.CRIMT) field is not applicable;
     and

- ii. the Controller Ready With Media Timeout (CRTO.CRWMT) indicates the worst-case time the host should wait after the controller is enabled for:
  - the controller to become ready and be able to process all commands without error as described in section 3.5.4.1; and
  - 2. all attached namespaces and media required to process Admin commands to become ready-; <Note: changing a period to semicolon>

and

- d) If the controller is in Controller Ready Independent of Media mode (i.e., the CC.CRIME bit is set to '1'), then
  - the Controller Ready With Media Timeout (CRTO.CRWMT) field indicates the worst-case time that host software should wait for all attached namespaces and media required to process Admin commands to become ready after the controller is enabled; and
  - ii. the Controller Ready Independent of Media Timeout (CRTO.CRIMT) field indicates the worst-case time the host should wait after the controller is enabled for the controller to become ready and be able to process:
    - 1. all commands that do not access attached namespaces; and
    - 2. Admin commands that do not require access to media

without error as described in section 3.5.4.1.

•••

#### 3.7 Resets

...

#### 3.7.2 Controller Level Reset

...

A Controller Level Reset consists of the following actions:

- The controller stops processing any outstanding Admin or I/O commands;
- All I/O Submission Queues are deleted;
- All I/O Completion Queues are deleted;
- The controller is brought to an Idle state. When this is complete, CSTS.RDY is cleared to '0'; and
- All controller properties defined in section 3.1.3 and internal controller state are reset, with the following exceptions:
  - o for controllers using a memory-based transport:
    - the Admin Queue properties (AQA, ASQ, or ACQ) are not reset as part of a Controller Reset;
    - the Controller Memory Buffer Memory Space Control property (CMBMSC) is reset as part of neither a Controller Reset nor a Function Level Reset; and
    - the Persistent Memory Region Memory Space Control Upper property (PMRMSCU) and the Persistent Memory Region Memory Space Control Lower property (PMRMSCL) are not reset as part of a Controller Reset::<change period to semicolon>

and

- for controllers using a message-based transport:
  - there are no exceptions

...

## 5 Admin Command Set

•••

#### 5.2 Asynchronous Event Request command

. .

The following event types are defined:

- a) Error event: Indicates a general error that is not associated with a specific command (refer to Figure 144). To clear this event, host software reads the Error Information log (refer to section 5.16.1.2) using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0':
- b) SMART / Health Status event: Indicates a SMART or health status event (refer to Figure 145). To clear this event, host software reads the SMART / Health Information log (refer to section 5.16.1.3) using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0'. The SMART / Health conditions that trigger asynchronous events may be configured in the Asynchronous Event Configuration feature using the Set Features command (refer to section 5.27.1.8);
- c) **Notice event:** Indicates a general event (refer to Figure 146). To clear this event, host software reads the appropriate log page as described in Figure 146. The conditions that trigger asynchronous events may be configured in the Asynchronous Event Configuration feature using the Set Features command (refer to section 5.27.1.8)—;<change period to semicolon>
- d) **I/O Command Specific Status events:** Events that are specific to an I/O command (refer to Figure 147).; <change period to semicolon>
- e) **Immediate events:** Events that are only reported when an outstanding Asynchronous Event Request command exists at the time the event occurs. If the event occurs and there is no outstanding Asynchronous Event Request command, then the event shall not be reported. No log page is associated with these events. These events include:
  - A. Normal NVM Subsystem Shutdown event;

and

f) **Vendor Specific event:** Indicates a vendor specific event. To clear this event, host software reads the indicated vendor specific log page using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0'.

..

#### 5.17 Identify command

•••

#### 5.17.2 Identify Data Structures

#### 5.17.2.1 Identify Controller data structure (CNS 01h)

. . .

Figure 275: Identify - Identify Controller Data Structure, I/O Command Set Independent

Bytes	I/O <sup>1</sup>	Admin <sup>1</sup>	Disc <sup>1</sup>	Description		
	Controller Capabilities and Features					
				Power State Descriptors		
2079:2048	М	М	R	<b>Power State 0 Descriptor (PSD0):</b> This field indicates the characteristics of power state 0. The format of this field is defined in Figure 276.		
2111:2080	0	0	R	<b>Power State 1 Descriptor (PSD1):</b> This field indicates the characteristics of power state 1. The format of this field is defined in Figure 276.		

Figure 275: Identify – Identify Controller Data Structure, I/O Command Set Independent

Bytes	1/0 <sup>1</sup>	Admin <sup>1</sup>	Disc <sup>1</sup>	Description
2143:2112	0	0	R	<b>Power State 2 Descriptor (PSD2):</b> This field indicates the characteristics of power state 2. The format of this field is defined in Figure 276.
		T	1	
2175:2144	0	0	R	Power State 3 Descriptor (PSD3): This field indicates the characteristics of power state 3. The format of this field is defined in Figure 276.
2207:2176	0	0	R	Power State 4 Descriptor (PSD4): This field indicates the characteristics of power state 4. The format of this field is defined in Figure 276.
2239:2208	θ	θ	R	Power State 5 Descriptor (PSD5): This field indicates the characteristics of power state 5. The format of this field is defined in Figure 276.
2271:2240	Ð	0	R	Power State 6 Descriptor (PSD6): This field indicates the characteristics of power state 6. The format of this field is defined in Figure 276.
2303:2272	Ð	0	R	Power State 7 Descriptor (PSD7): This field indicates the characteristics of power state 7. The format of this field is defined in Figure 276.
2335:2304	Đ	0	R	Power State 8 Descriptor (PSD8): This field indicates the characteristics of power state 8. The format of this field is defined in Figure 276.
2367:2336	Ð	θ	R	Power State 9 Descriptor (PSD9): This field indicates the characteristics of power state 9. The format of this field is defined in Figure 276.
2399:2368	Đ	θ	R	Power State 10 Descriptor (PSD10): This field indicates the characteristics of power state 10. The format of this field is defined in Figure 276.
2431:2400	Đ	0	R	Power State 11 Descriptor (PSD11): This field indicates the characteristics of power state 11. The format of this field is defined in Figure 276.
2463:2432	Q	0	R	Power State 12 Descriptor (PSD12): This field indicates the characteristics of power state 12. The format of this field is defined in Figure 276.
2495:2464	0	0	R	Power State 13 Descriptor (PSD13): This field indicates the characteristics of power state 13. The format of this field is defined in Figure 276.
<del>2527:2496</del>	0	0	R	Power State 14 Descriptor (PSD14): This field indicates the characteristics of power state 14. The format of this field is defined in Figure 276.
2559:2528	Ð	0	R	Power State 15 Descriptor (PSD15): This field indicates the characteristics of power state 15. The format of this field is defined in Figure 276.
<del>2591:2560</del>	0	0	R	Power State 16 Descriptor (PSD16): This field indicates the characteristics of power state 16. The format of this field is defined in Figure 276.
<del>2623:2592</del>	Đ	Ð	R	Power State 17 Descriptor (PSD17): This field indicates the characteristics of power state 17. The format of this field is defined in Figure 276.
2655:2624	0	0	R	Power State 18 Descriptor (PSD18): This field indicates the characteristics of power state 18. The format of this field is defined in Figure 276.
2687:2656	0	0	R	Power State 19 Descriptor (PSD19): This field indicates the characteristics of power state 19. The format of this field is defined in Figure 276.
<del>2719:2688</del>	0	0	R	Power State 20 Descriptor (PSD20): This field indicates the characteristics of power state 20. The format of this field is defined in Figure 276.
<del>2751:2720</del>	Ð	0	R	Power State 21 Descriptor (PSD21): This field indicates the characteristics of power state 21. The format of this field is defined in Figure 276.
2783:2752	Đ	0	R	Power State 22 Descriptor (PSD22): This field indicates the characteristics of power state 22. The format of this field is defined in Figure 276.
2815:2784	0	0	R	Power State 23 Descriptor (PSD23): This field indicates the characteristics of power state 23. The format of this field is defined in Figure 276.
2847:2816	Ð	0	R	Power State 24 Descriptor (PSD24): This field indicates the characteristics of power state 24. The format of this field is defined in Figure 276.
2879:2848	θ	Ð	R	Power State 25 Descriptor (PSD25): This field indicates the characteristics of power state 25. The format of this field is defined in Figure 276.
2911:2880	Đ	θ	R	Power State 26 Descriptor (PSD26): This field indicates the characteristics of power state 26. The format of this field is defined in Figure 276.
2943:2912	Đ	0	R	Power State 27 Descriptor (PSD27): This field indicates the characteristics of power state 27. The format of this field is defined in Figure 276.
2975:2944	0	0	R	Power State 28 Descriptor (PSD28): This field indicates the characteristics of power state 28. The format of this field is defined in Figure 276.

Figure 275: Identify - Identify Controller Data Structure, I/O Command Set Independent

Bytes	I/O <sup>1</sup>	Admin <sup>1</sup>	Disc <sup>1</sup>	Description
3007:2976	0	Ф	R	Power State 29 Descriptor (PSD29): This field indicates the characteristics of power state 29. The format of this field is defined in Figure 276.
3039:3008	0	Ф	R	Power State 30 Descriptor (PSD30): This field indicates the characteristics of power state 30. The format of this field is defined in Figure 276.
3071:3040	0	0	R	<b>Power State 31 Descriptor (PSD31):</b> This field indicates the characteristics of power state 31. The format of this field is defined in Figure 276.
Vendor Specific				
4095:3072	0	0	0	Vendor Specific.
NOTES:				

- 1. O/M/R definition: O = Optional, M = Mandatory, R = Reserved.
- 2. Mandatory for I/O controllers using a message-based transport. Reserved for I/O controllers using a memory-based transport.

#### 5.24 Sanitize command

#### 5.24.1 Command Completion

Sanitize command specific status values are defined in Figure 305.

Figure 305: Sanitize – Command Specific Status Values

Value	Description
20h	Namespace is Write Protected: The command is prohibited while the namespace is write protected (refer to section 8.12). <adding a="" period=""></adding>

#### 5.27 Set Features command

#### 5.27.1 Feature Specific Information

#### 5.27.1.4 Volatile Write Cache (Feature Identifier 06h), (Optional)

#### 5.27.1.9 Autonomous Power State Transition (Feature Identifier 0Ch), (Optional)

### 5.27.1.10 Host Memory Buffer (Feature Identifier 0Dh), (Optional)

# 5.27.1.11 Timestamp (Feature Identifier 0Eh), (Optional) 5.27.1.13 Host Controlled Thermal Management (Feature Identifier 10h), (Optional) 5.27.1.14 Non-Operational Power State Config (Feature Identifier 11h), (Optional) 5.17.1.19 Sanitize Config (Feature Identifier 17h), (Optional) 5.17.1.20 Endurance Group Event Configuration (Feature Identifier 18h), (Optional) 5.17.1.24 Software Progress Marker (Feature Identifier 80h), (Optional) 5.27.1.25Host Identifier (Feature Identifier 81h), (Optional<sup>1</sup>) <editor - delete footnote as well.> 5.27.1.26 Reservation Notification Mask (Feature Identifier 82h), (Optional<sup>2</sup>) <editor – delete footnote as well.> 5.27.1.27 Reservation Persistence (Feature Identifier 83h), (Optional3) <editor – delete footnote 7 I/O Commands ... **Reservation Report command** 7.5 Figure 406: Registered Controller Data Structure Description Bytes

Mandatory if reservations are supported by the controller as indicated in the ONCS field in the Identify

Controller data structure.

<sup>&</sup>lt;sup>2</sup> Mandatory if reservations are supported by the namespace as indicated by a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure.

<sup>&</sup>lt;sup>3</sup> Mandatory if reservations are supported by the namespace as indicated by a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure.

Figure 406: Registered Controller Data Structure

Bytes	Description
	<b>Reservation Status (RCSTS):</b> This field indicates the reservation status of the controller described by this data structure.
02	Bits 7:1 are reserved. <editor: a="" adding="" period=""></editor:>
	Bit 0 is set to '1' if the controller is associated with a host that holds a reservation on the namespace.
	•

#### ...

# 8 Extended Capabilities

•••

#### 8.13 NVMe over Fabrics In-band Authentication

...

## 8.13.4 Common Authentication Messages

...

### 8.13.4.2 **AUTH\_Failure Messages**

...

<Editor: Each row added a period at the end>

Figure 442: AUTH\_Failure reason code explanations

Value	Description
01h	Authentication failed: Authentication of the involved host or NVM subsystem failed.
02h	<b>Authentication protocol not usable:</b> The protocol descriptors proposed by the host do not satisfy the security requirements of the controller (refer to section 8.13.4.1).
03h	<b>Secure channel concatenation mismatch:</b> The SC_C value indicated by the host does not satisfy the security requirements of the controller (refer to section 8.13.4.1).
04h	<b>Hash function not usable:</b> The HashIDList proposed by the host does not satisfy the security requirements of the controller (refer to section 8.13.5.2).
05h	<b>DH group not usable:</b> The DHgIDList proposed by the host does not satisfy the security requirements of the controller (refer to section 8.13.5.2).
06h	Incorrect payload: The payload of the received message is not correct.
07h	<b>Incorrect protocol message:</b> The received message is not the expected next message in the authentication protocol sequence.
All other values	Reserved