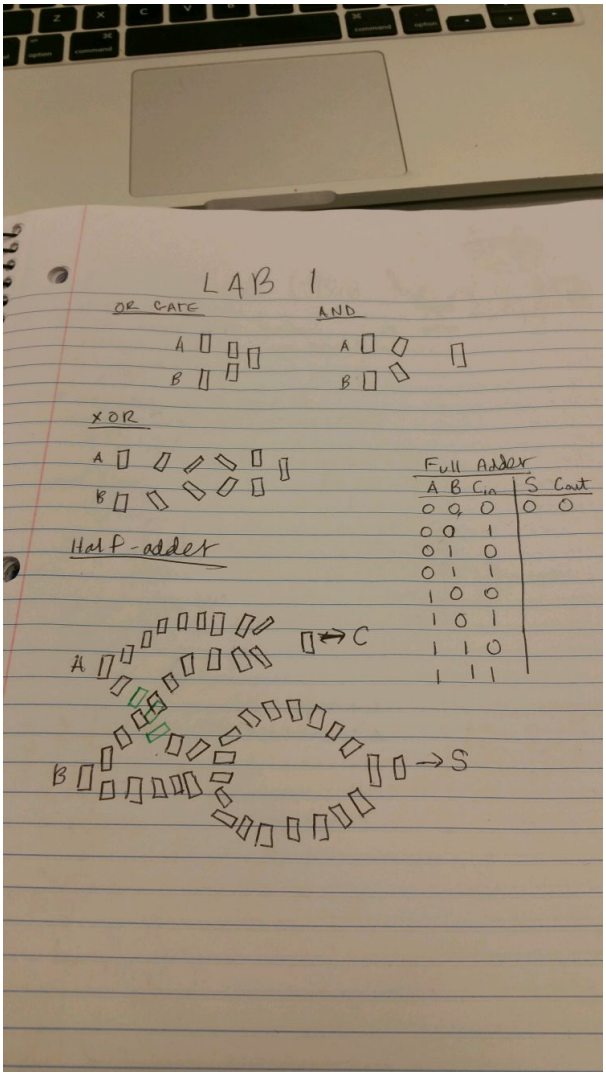
Lab 1: Super Secret Lab John Enquist



In terms of propagation delays, there was no issue with the AND, OR, and XOR gates, as the time it took for dominoes to fall had no effect on the output of the gate. On the half and full adders however, we had to build our gate with respect to propagation delays in order to have the domino sequences fall at the correct time. For example, if the path of A for the half adder fell too quickly, it would reach the XOR gate before B, resulting in a potentially incorrect output for S and C.

For a 4-bit ripple carry adder, one has to factor in a different propagation delay for each adder in order to account for the carry-in input. If it takes 2 seconds for the first adder's carry-out to work, then the next adder cannot start until 2 seconds later than the first. This process extends to the next two adders, adding 2 extra seconds for each adder after the first. The same process applies to a 16 bit adder, making the last adder have a propagation delay of 30 seconds after the first to account for the time it takes for the last carry to reach the final adder.