OPEN Alliance RGMII EPL

EPL Recommendation for Automotive Application

Author & Company	OPEN Alliance TC6 Members
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The document provides EPL parameters for a Gigabit MII interface. The parameters are based on the RGMII Gigabit MII interface and adapted to Automotive requirements.

Version Control of Document

Version	Author	Description	Date
1.0	Harald Zweck	Initial document, draft	2014-08-14
1.1	Harald Zweck		2014-08-19
2.0	Harald Zweck	Replaces all versions before V2.0	2016-04-25
2.1	Harald Zweck	Update of V2.0 based on feedback from OPEN Alliance TC6 members*	2016-06-20
2.2	Harald Zweck	Update of V2.1 based on feedback from OPEN Alliance TC6 members*	2016-07-04
2.2 RC01	Harald Zweck	Release candidate of draft V2.2	2016-07-04
2.2 RC02	Harald Zweck	Release candidate of draft V2.2	2016-10-24
2.2 public	Harald Zweck	Public document	2016-10-25

*details provided in appendix

Restriction level history of Document

Version	Restriction Level	Description	Date
1.0	OPEN Technical Member internal only	draft	2014-08-14
1.1	OPEN Technical Member internal only	draft	2014-08-19
2.0	OPEN Technical Member internal only	draft	2016-04-25
2.1	OPEN Technical Member internal only	draft	2016-06-20
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Contents

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2 Acknowledgements

TC6 would like to thank the following members:

Heiko Ehrich, TÜV Nord
Wes Mir, Delphi
David Ortiz, KDPOF
Pablo Tapia, KDPOF

3 Glossary

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4 Purpose of this document

The RGMII interface is commonly used for connecting two Ethernet enabled devices to each other, especially in consumer oriented applications.

Products used in the Automotive industry typically must be designed according to more challenging parameter values, like wider temperature ranges, deeper voltage drops, harsher parasitic effects, etc.

The intention of this document is to add to the existing RGMII parameters, defined in the documents “RGMII V1.3” and “RGMII V2.0” a set of definitions which makes the electrical-physical layer more robust and moves it closer to Automotive requirements.
This specification does not provide compatibility to other RGMII specifications.

This document does not cover the management interface.

5 Pinout of the OPEN RGMII interface

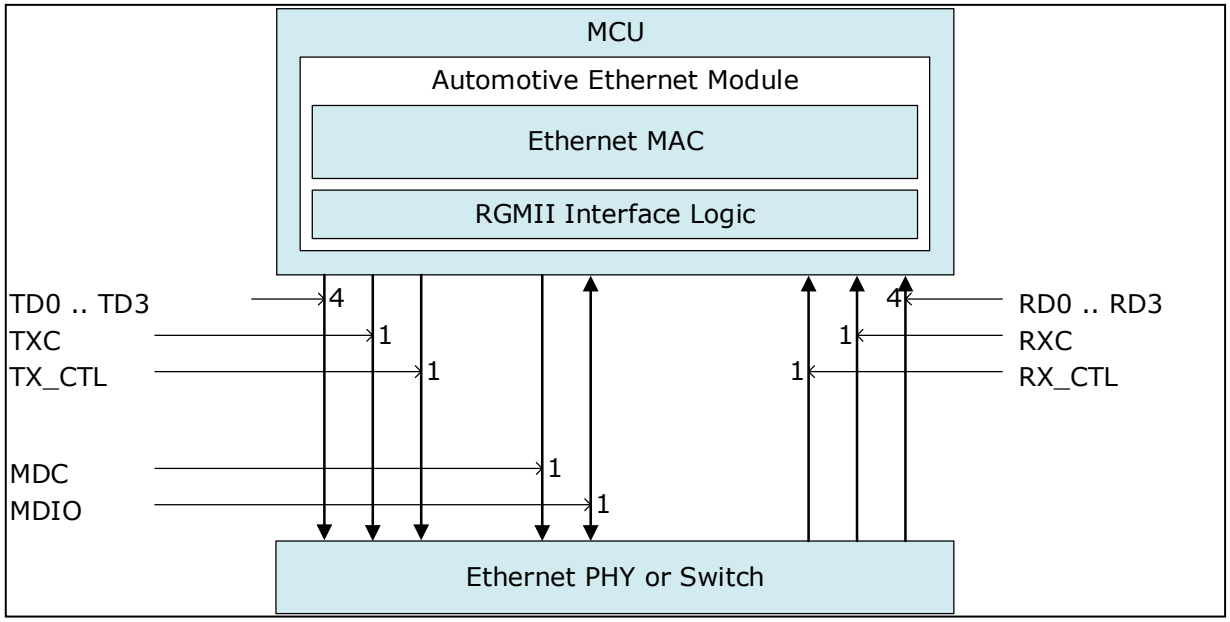

Figure 1: Pinout of the OPEN RGMII interface

Symbol	Signal Description	Signal Source	Comment
TXC	Transmit reference clock	MAC	
TD0 .. TD3	Data bits [3..0] during the rising edge of TXC, data bits [7..4] during the falling edge of TXC	MAC	
TX_CTL	TXEN during rising edge of TXC, a logical derivative of TXEN and TXERR during falling edge of TXEN.	MAC	
RXC	Receive reference clock	PHY / Switch	
RD0 .. RD3	Data bits [3..0] during the rising edge of RXC, data bits [7..4] during the falling edge of RXC.	PHY / Switch	
RX_CTL	RXDV during the rising edge of RXD, a logical derivative of RXDV and RXERR during the falling edge of RXC.	PHY / Switch	
MDC	Timing reference for the MDIO signal	MAC	For technical details see management interface
MDIO	Transfer of data and status between MAC and PHY	MAC / PHY (bi-directional)	

Table 1: OPEN RGMII Pin Definition

6 Definition of signal levels

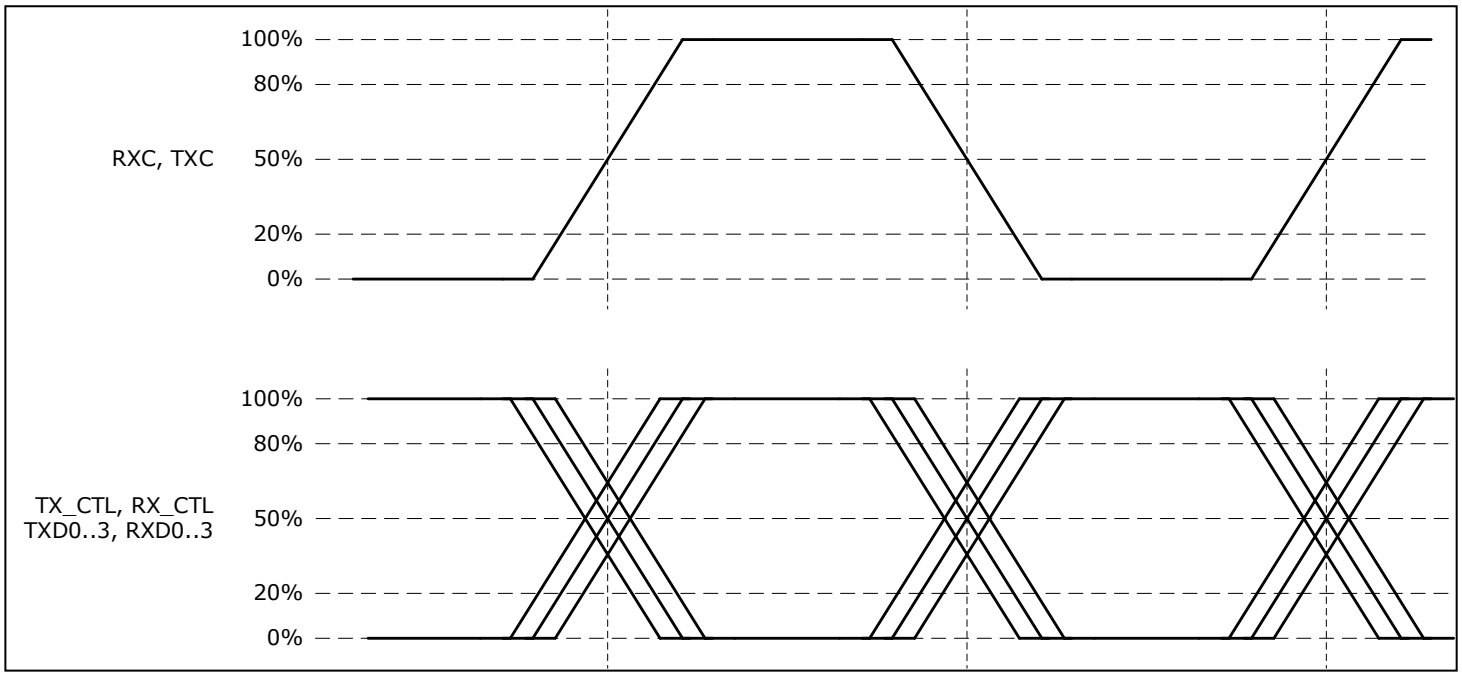

Figure 2: Signal levels of the OPEN RGMII interface

The operating voltage of the electrical interface can be chosen independent of this document by the implementer. Its parameters shall be specified in the device datasheet.

The 100% value shown in Fig. 2 is equivalent to the nominal operation voltage level used for the electrical interface (e.g. for a 3.3V nominal voltage electrical interface 100% corresponds to 3.3V).

As a consequence all signal levels defined in this specification are fixed voltages. Variations of the interface voltage do not modify them. All timing parameters are fixed and independent of the interface voltage (e.g. slopes).

7 Signal Timing

7.1 Signal Delay modes

The OPEN RGMII interface uses Double Data Rate (DDR) data transfer scheme. It requires that the clock signal is delayed against the data and control signals.

Note: The parameters in this document assume a delay mismatch between clock and data of 150psec.

The OPEN RGMII interface definition supports two delay modes.

Delay on Destination (DoD):
Clock, data and control signals are transferred edge aligned. The delay of the clock signal has to be accomplished by the receiver device.

Delay on Source (DoS):
The transmitter device already provides a delayed clock signal.

7.2 Signal timing parameters in DoD mode

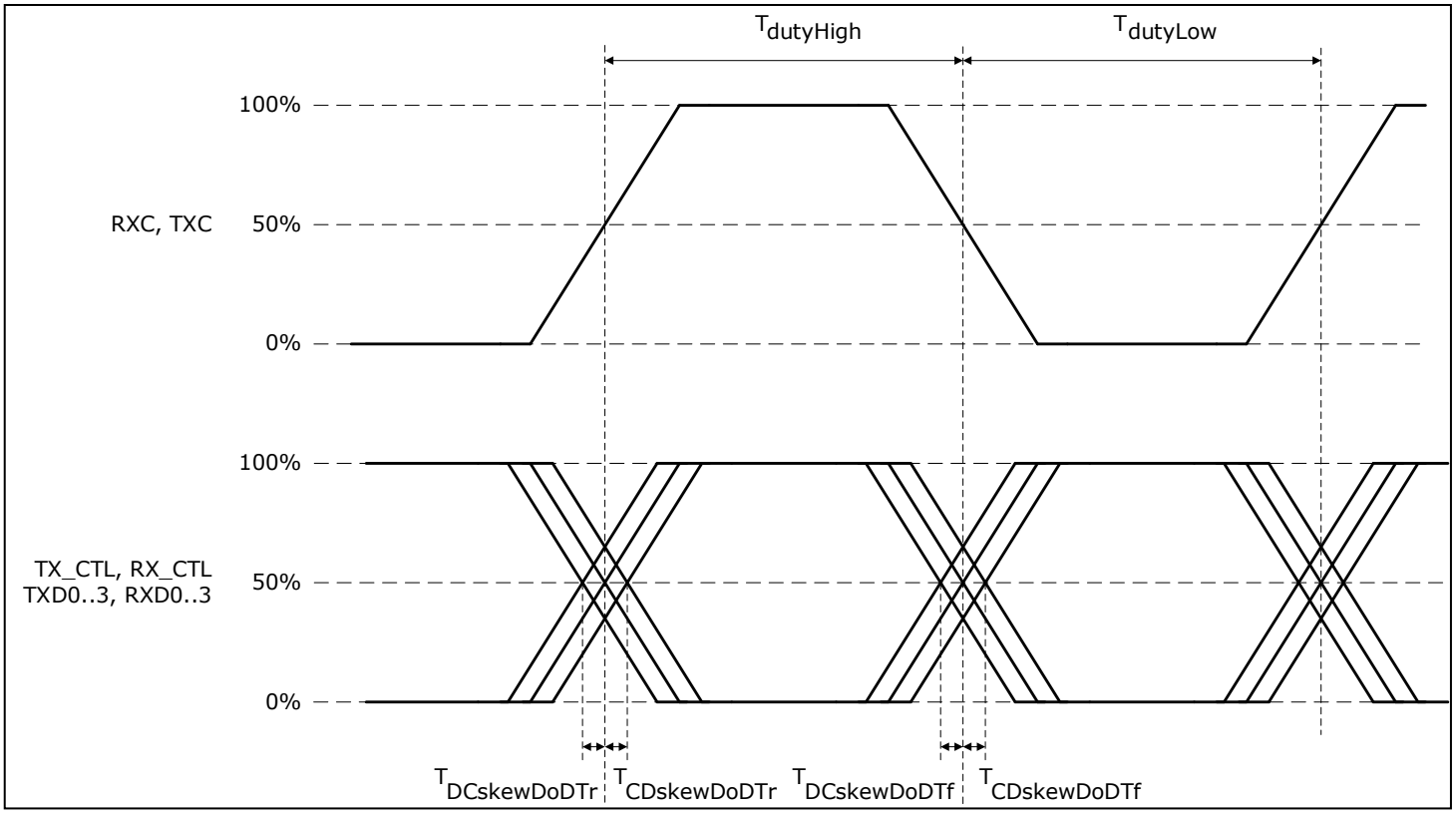

Figure 3: Signal timing parameters at signal source in DoD mode

Symbol	Parameter	Min Value	Max Value	Units	Comment
$T_{dutyHigh}$	Clock duty cycle high min time	3.6		ns	
$T_{dutyLow}$	Clock duty cycle low min time	3.6		ns	
$T_{DCskewDoDTr}$	Data to Clock skew in Delay on Destination mode at signal source rising edge		0.5	ns	
$T_{CDskewDoDTr}$	Clock to Data skew in Delay on Destination mode at signal source rising edge		0.5	ns	
$T_{DCskewDoDTf}$	Data to Clock skew in Delay on Destination mode at signal source falling edge		0.5	ns	
$T_{CDskewDoDTf}$	Clock to Data skew in Delay on Destination mode at signal source falling edge		0.5	ns	

Table 2: Duty cycle and skews at signal source in DoD mode

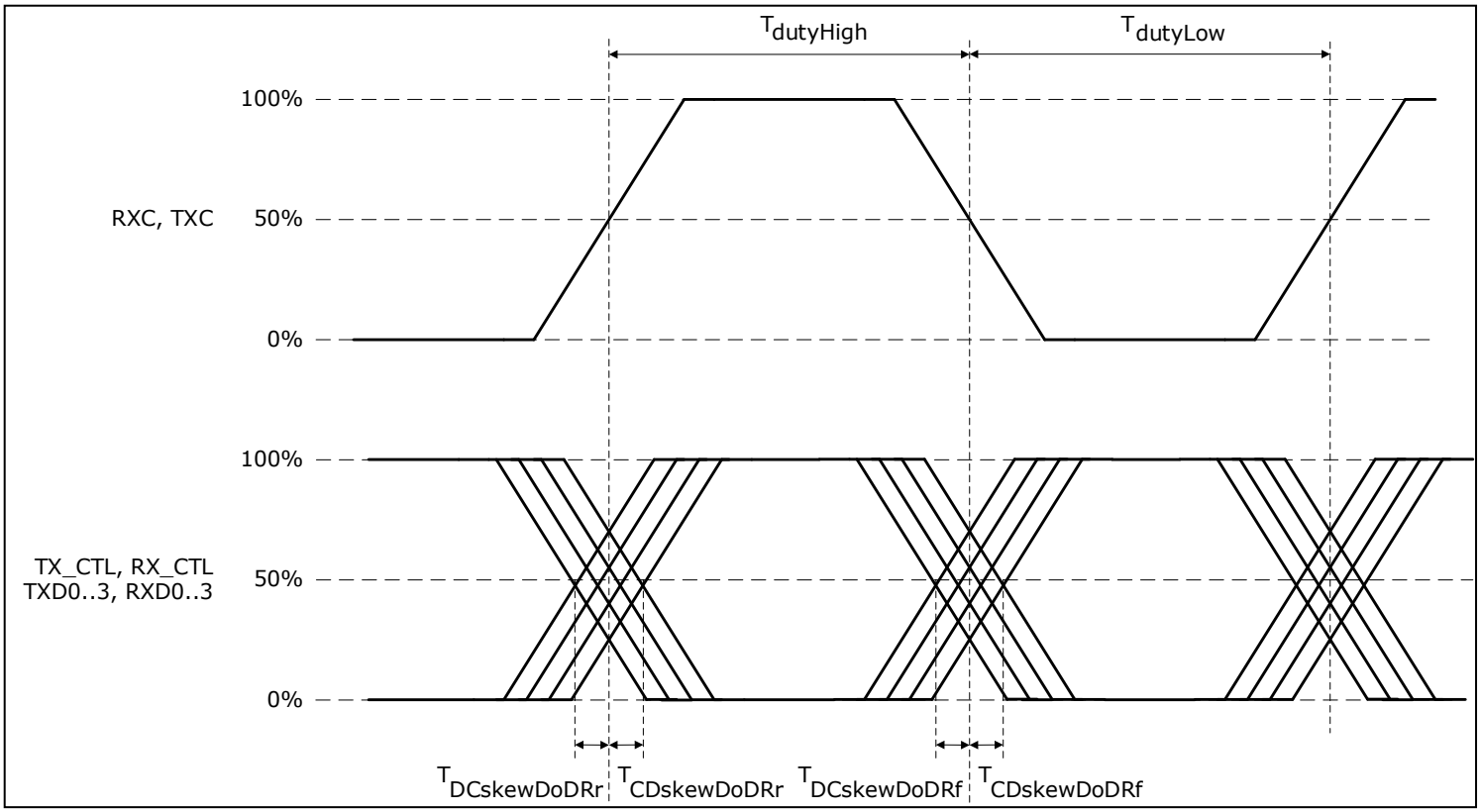

Figure 4: Signal timing parameters at signal destination in DoD mode

Symbol	Parameter	Min Value	Max Value	Units	Comment
$T_{dutyHigh}$	Clock duty cycle high min time	3.6		ns	
$T_{dutyLow}$	Clock duty cycle low min time	3.6		ns	
$T_{DCskewDoDRr}$	Data to Clock skew in Delay on Destination mode at signal destination rising edge		0.65	ns	
$T_{CDskewDoDRr}$	Clock to Data skew in Delay on Destination mode at signal destination rising edge		0.65	ns	
$T_{DCskewDoDRf}$	Data to Clock skew in Delay on Destination mode at signal destination falling edge		0.65	ns	
$T_{CDskewDoDRf}$	Clock to Data skew in Delay on Destination mode at signal destination falling edge		0.65	ns	

Table 3: Duty cycle and skews at signal destination in DoD mode

7.3 Signal timing parameters in DoS mode

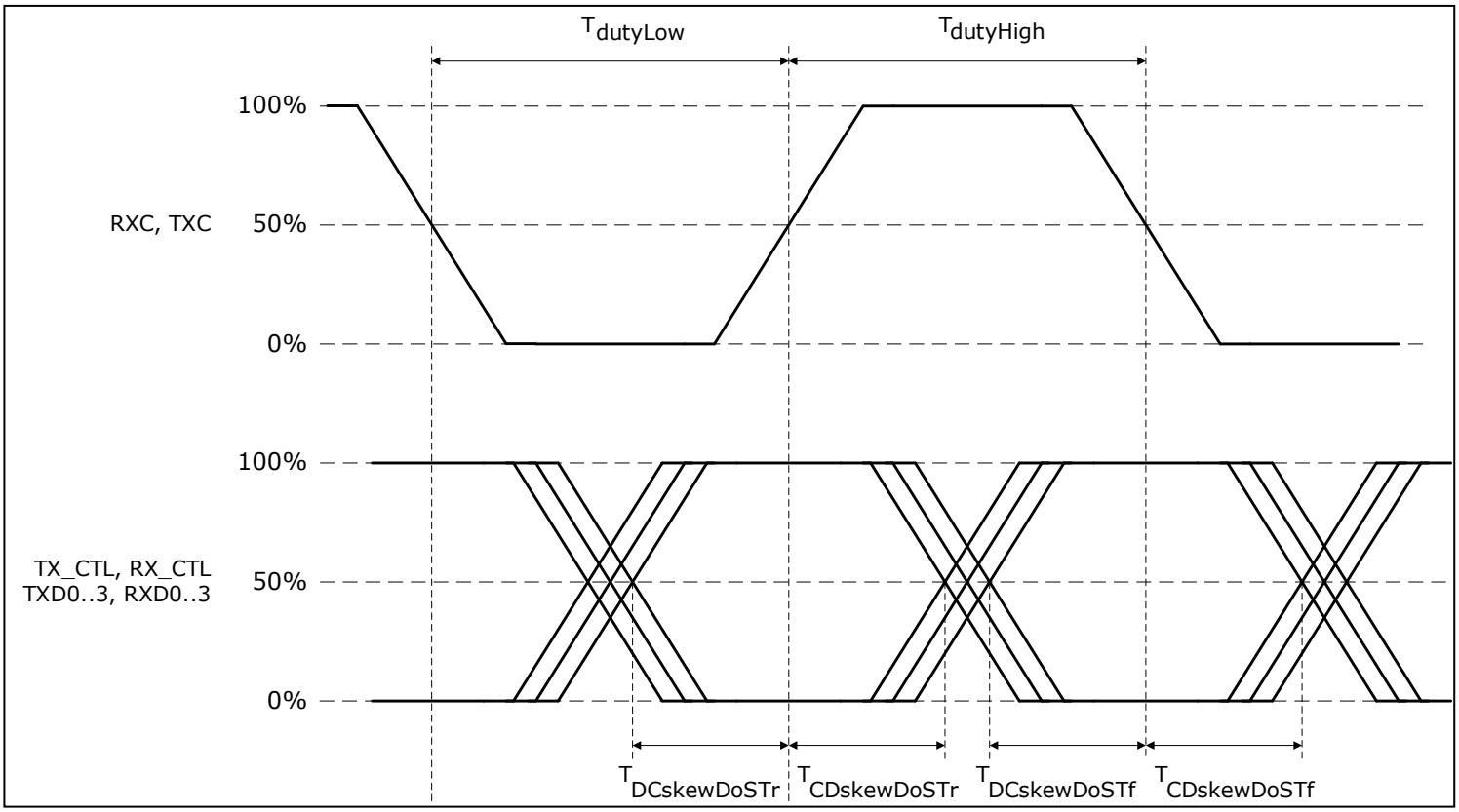

Figure 5: Signal timing parameters at signal source in DoS mode

Symbol	Parameter	Min Value	Max Value	Units	Comment
$T_{dutyHigh}$	Clock duty cycle high min time	3.6		ns	
$T_{dutyLow}$	Clock duty cycle low min time	3.6		ns	
$T_{DCskewDoSTr}$	Data to Clock skew in Delay on Source mode at signal source rising edge	1.2		ns	
$T_{CDskewDoSTr}$	Clock to Data skew in Delay on Source mode at signal source rising edge	1.2		ns	
$T_{DCskewDoSTf}$	Data to Clock skew in Delay on Source mode at signal source falling edge	1.2		ns	
$T_{CDskewDoSTf}$	Clock to Data skew in Delay on Source mode at signal source falling edge	1.2		ns	

Table 4: Duty cycle and skews at signal source in DoS mode

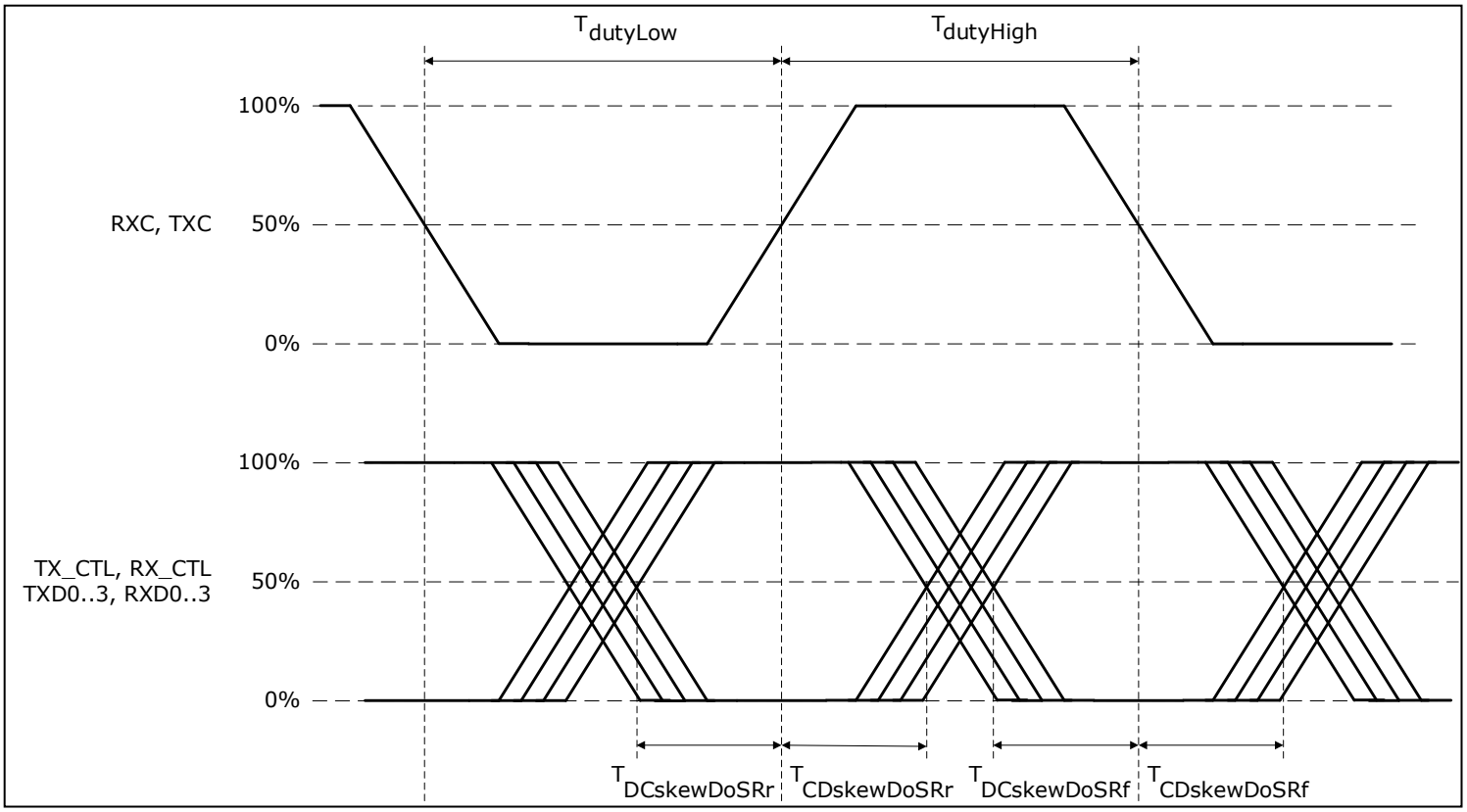

Figure 6: Signal timing parameters at signal destination in DoS mode

Symbol	Parameter	Value		Units	Comment
$T_{dutyHigh}$	Clock duty cycle high min time	3.6		ns	
$T_{dutyLow}$	Clock duty cycle low min time	3.6		ns	
$T_{DCskewDoSRr}$	Data to Clock skew in Delay on Source mode at signal destination rising edge	1.05		ns	
$T_{CDskewDoSRr}$	Clock to Data skew in Delay on Source mode at signal destination rising edge	1.05		ns	
$T_{DCskewDoSRf}$	Data to Clock skew in Delay on Source mode at signal destination falling edge	1.05		ns	
$T_{CDskewDoSRf}$	Clock to Data skew in Delay on Source mode at signal destination falling edge	1.05		ns	

Table 5: Duty cycle and skews at signal destination in DoS mode

8 General Parameters

Symbol	Parameter	Min Value	Max Value	Units	Comments
CloadR_max	Max capacitive load of signal at receiver		5	pF	
tR_max	Max signal rise time		1	ns	From 20% to 80%*
tF_max	Max signal fall time		1	ns	From 80% to 20%*

Table 6: General Parameters

Note *: Rise / fall time condition is valid for test purposes for a load of 5pF at the signal source.

Note: The distributed output load of the transmitter has to be considered by PCB design.

9 References

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10 Appendix A

Version control details

Changes for update V2.0 to V2.1

Page old	Page new	change
1	1	Changed document title from “OPEN RGMII EPL” to “OPEN Alliance RGMII EPL”
1	1	Added abstract to cover page
4	4	Removed disclaimer table at the top of the page
7	6	Table with reference to glossary removed
8	7	Removed reference to Gigabit in the first sentence
8	7	Inserted information about compatibility to other RGMII specifications
8	7	Inserted reference to other RGMII documents
8	7	Removed reference to IEEE MDC/ MDIO interface
9	8	Updated names of data signals
9	8	Removed reference to IEEE MDC/ MDIO interface
10	9	Updated the note below the figure
11	10	Inserted reference to delay mismatch
12	11	Replaced in all locations “transmitter” with “signal source”
13	12	Replaced in all locations “receiver” with “signal destination”
14	13	Replaced in all locations “transmitter” with “signal source”
15	14	Replaced in all locations “receiver” with “signal destination”
16	15	Table 6: Removed line with symbol Cl_max and inserted line with symbol CloadR_max
16	15	Inserted note below table 6

Changes for update V2.1 to V2.2

Page old	Page new	change
9	9	updated text below figure 2
16	16	Removed unnecessary remarks

Changes for update V2.2 to V2.2 RC01

Page old	Page new	change
9	9	Updated text in second paragraph below figure 2

Changes for update V2.2 RC01 to V2.2 RC02

Page old	Page new	change
15	15	Added note 2 below table 6

Changes for update V2.2 RC02 to V2.2 public

Page old	Page new	change
cover	cover	Removed notes about restriction for OPEN Technical Member only
footer	footer	Removed confidentiality notes in all footers
cover	cover	Consistency update of title in table from “OPEN Alliance RGMII EPL (Electrical-Physical Layer) Requirements” to “OPEN Alliance RGMII EPL (Electrical-Physical Layer) Recommendations”