Flash Technology:
200-400Mbps and Beyond

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  - Features Enable/Disable
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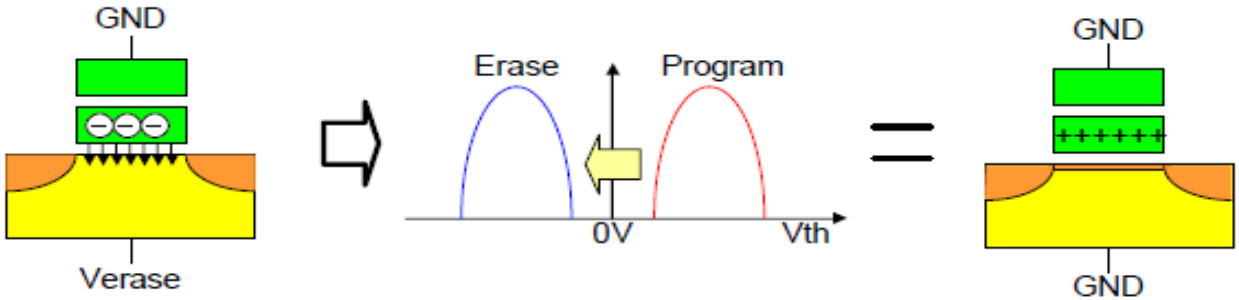
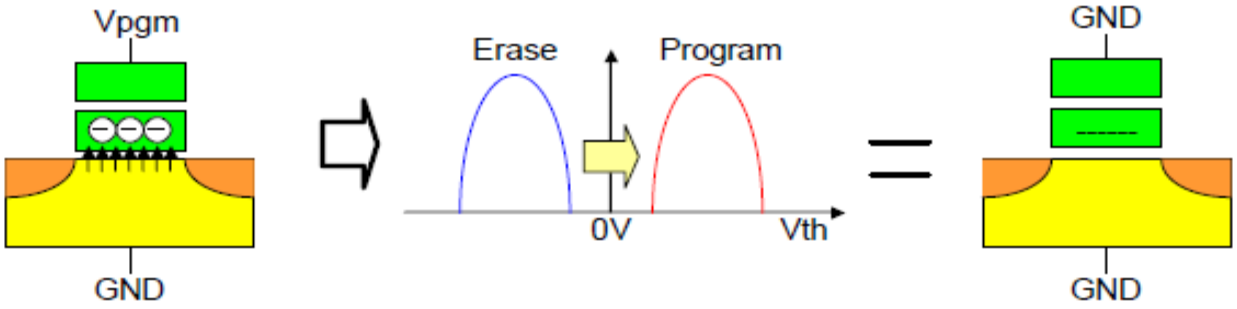
NAND Flash Primer (1/2)

- NAND requires Erase before Programming
  - Erase

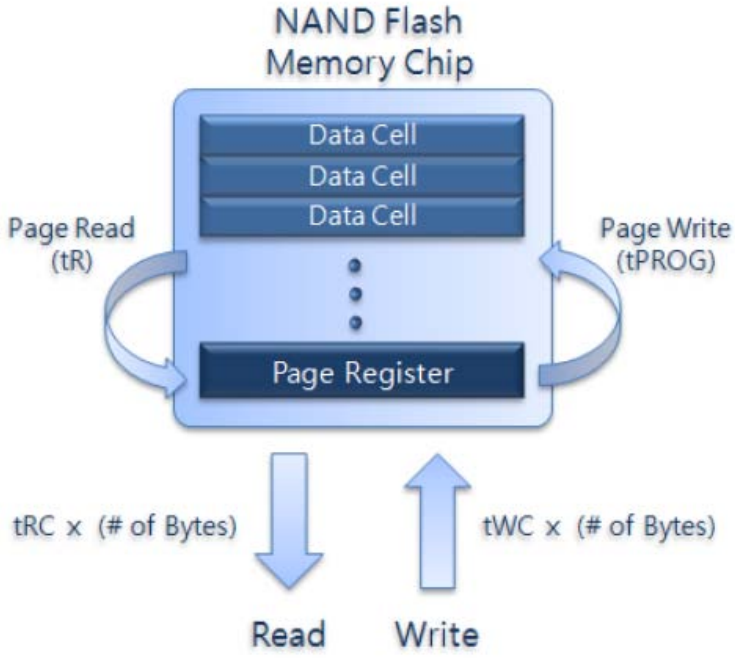


  - Program



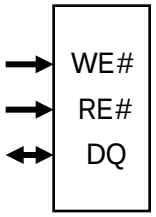
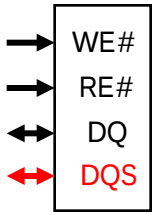
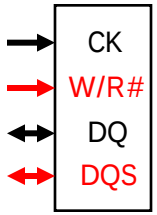
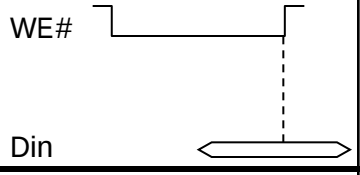
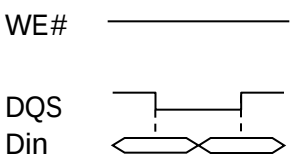
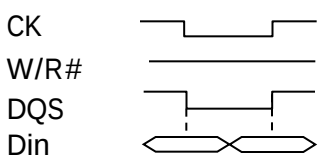
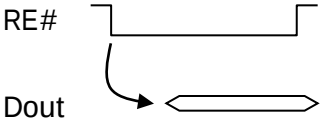
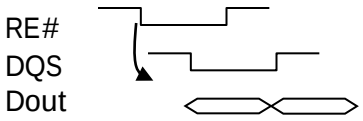
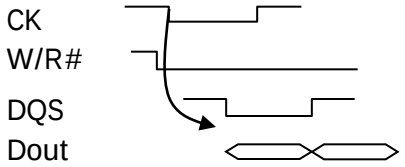
NAND Flash Primer (2/2)

- NAND Flash is page-based for Read & Program Operation
  - The internal data register holds one page of date
  - A Page is the unit of transfer between the data register and the memory array.
    All program and read operations transfer a page of data between the data register and a page in the memory array.



NAND Interface Evolution (~200Mbps)

- As performance requirements increase, the legacy NAND interface(SDR–single data rate) becomes bottleneck, esp. for read performance.
- JEDED NAND Flash I/F specification is scheduled to be ratified by early 2011

	Legacy SDR (~66Mbps)	Toggle-mode DDR (~200Mbps)	Synchronous DDR (~200Mbps)
Pinout			
Writes			
Reads			

Supported interface is identified by Read ID

Growing Need for Higher NAND I/F Speed

- **Conventional NAND Flash memory application**
  - High capacity (low cost), small form factor & low power consumption

    -> Common in most CE devices

- **New CE devices**
  - High performance

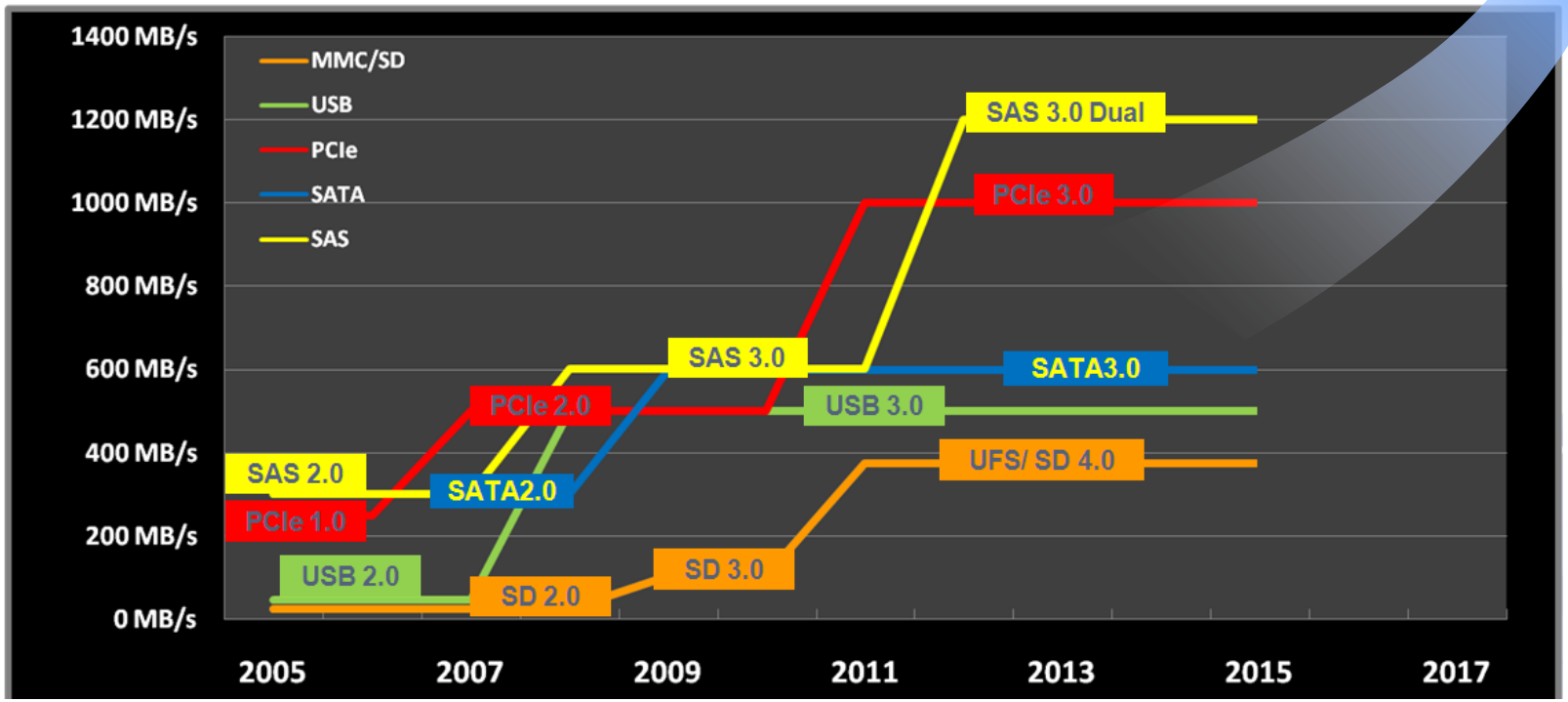
Full browsing

3D gaming

- **System performance devices**
  - High-performance computing
  - Massive data processing

Growing Need for Higher NAND I/F Speed

- Performance demand with the growth of storage interface
- With continuing innovations in such as the NAND architecture and enhanced I/O speed, performance can be achieved.



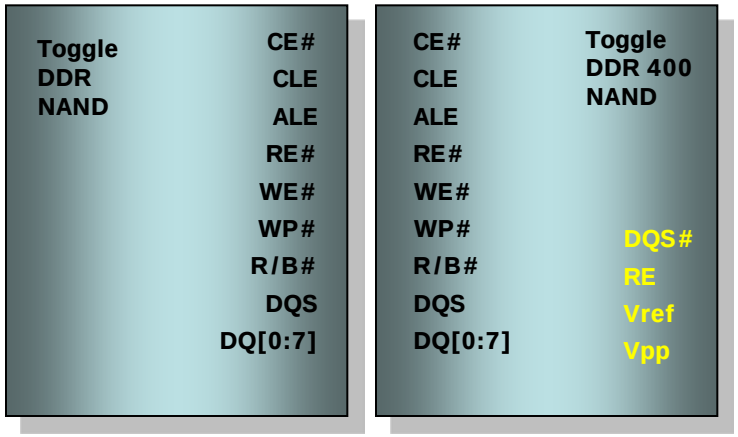
Introducing High-Speed NAND Flash Interface

- New features to enable 400 Mbps
  - Complementary DQS and RE signals
  - Vref (SSTL)
  - On Die Termination
  - DQS latency adjustment

Note: Features are under discussion and subject to change without notice.

Differential Signaling

- Independent enablement of RE and DQS
- Immunity to GND Noise and Cross Talk



Legacy SDR	DDR (Toggle/ Sync)	High-Speed DDR	Type	Description
15	16	20		
ALE	ALE	ALE	I	Address Latch Enable
CLE	CLE	CLE	I	Command Latch Enable
/CE	/CE	/CE	I	Chip Enable
/RE	/RE or W/R#	/RE	I	Read Enable
/WE	/WE or CK	/WE	I	Write Enable
/WP	/WP	/WP	I	Write Protect
R/B	R/B	R/B	O	Ready/Busy
DQ	DQ	DQ	I/O	Data Input/Output
	DQS	**DQS**	**I/O**	**Data Strobe**
		/DQS	**I/O**	**Data Strobe Complement**
		RE	**I**	**Read Enable Complement**
		Vpp	**I**	**External High Voltage**
		Vref	**I**	**Voltage Reference**

Note: Features are under discussion and subject to change without notice.

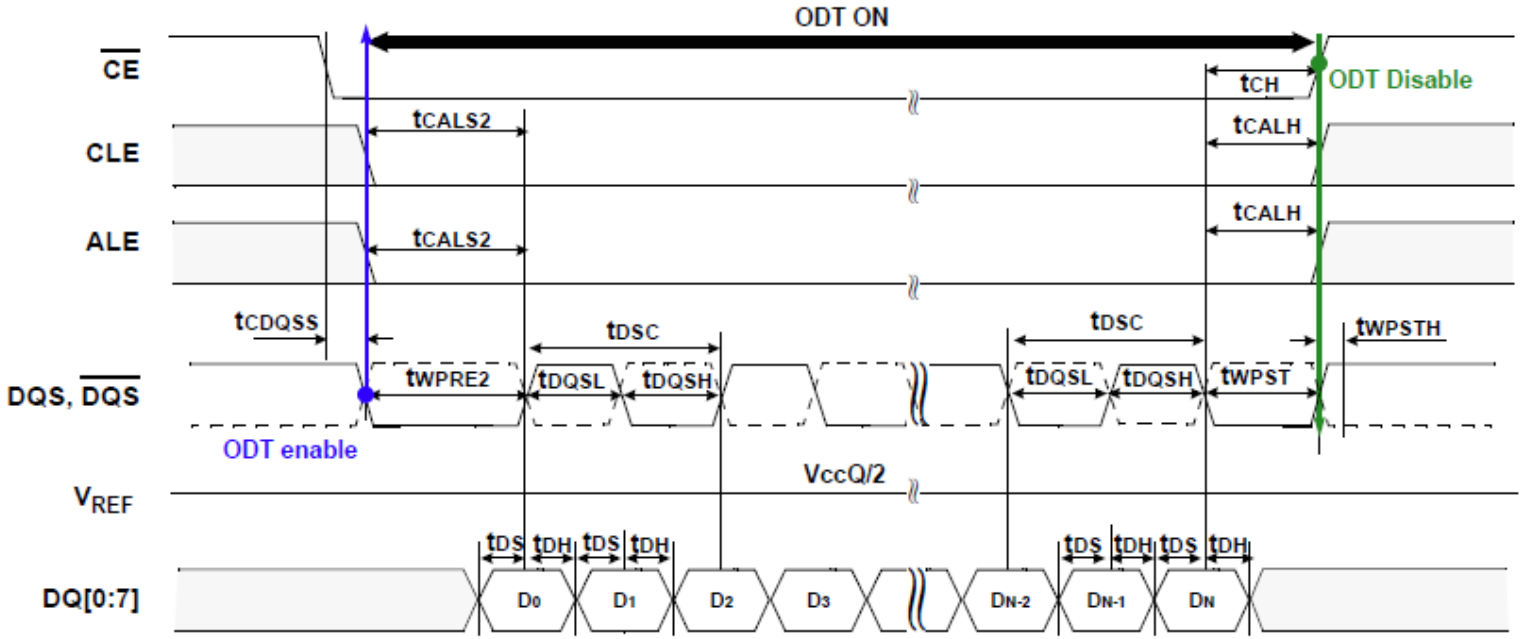
Vref

- SSTL
  - 400 Mbps only supported at 1.8V VccQ
  - Industry standard that is easily adaptable
  - Allows for higher speeds and lower power consumption
- External Vref
  - VccQ/2
  - Allows for tighter setups/holds due to controlled reference
  - Reduces effects from external GND bounce

Note: Features are under discussion and subject to change without notice.

On Die Termination

- Once ODT is enabled by Set Feature, no other operation by host required.
- For example, if program command is issued, ODT is turned on only during data transfer period.



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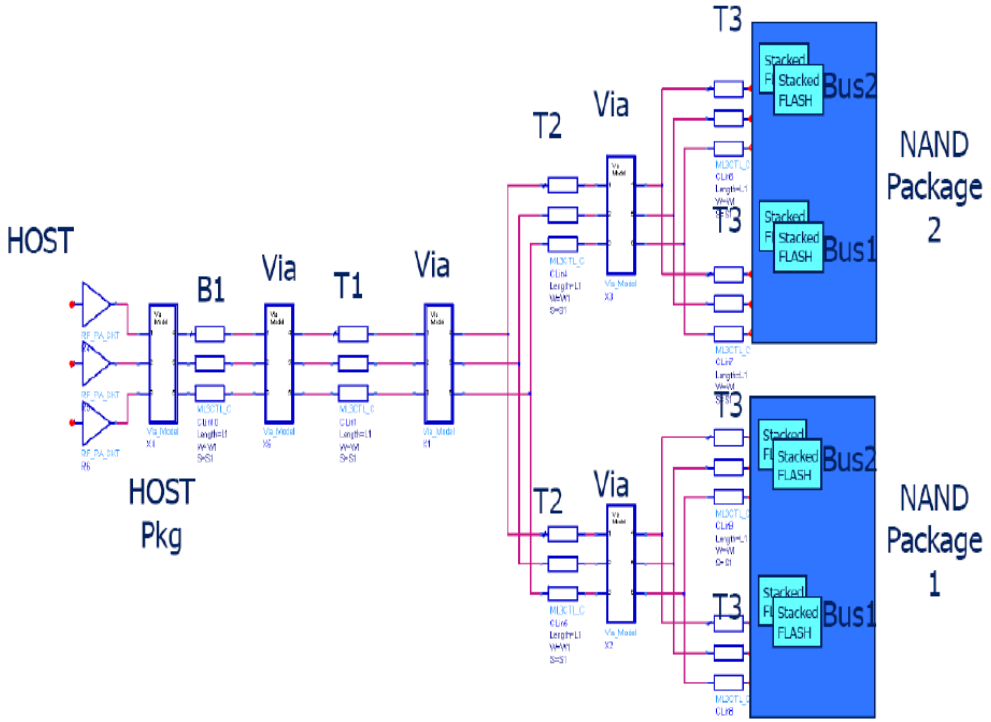
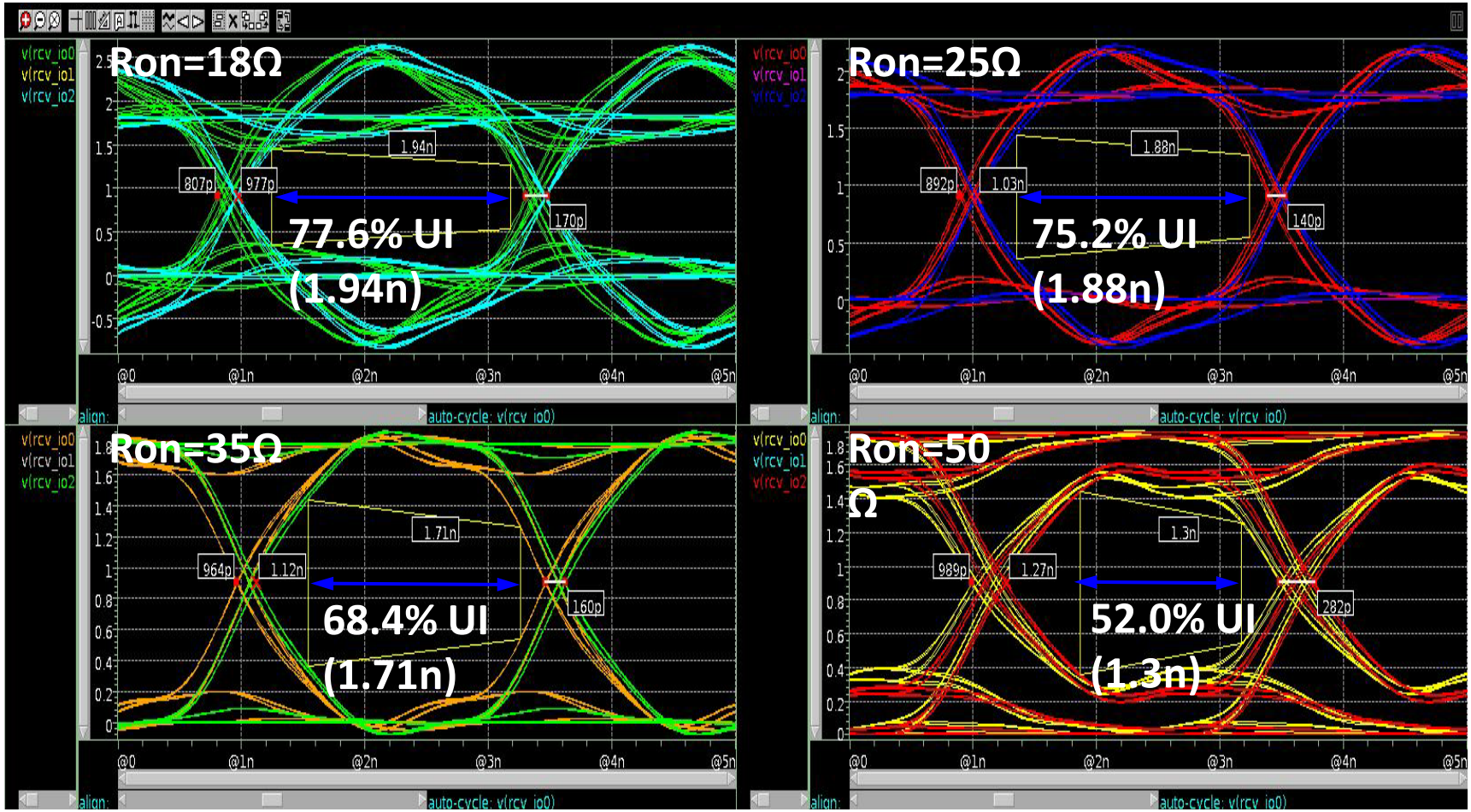
High-Speed Interface Simulation with On Die termination



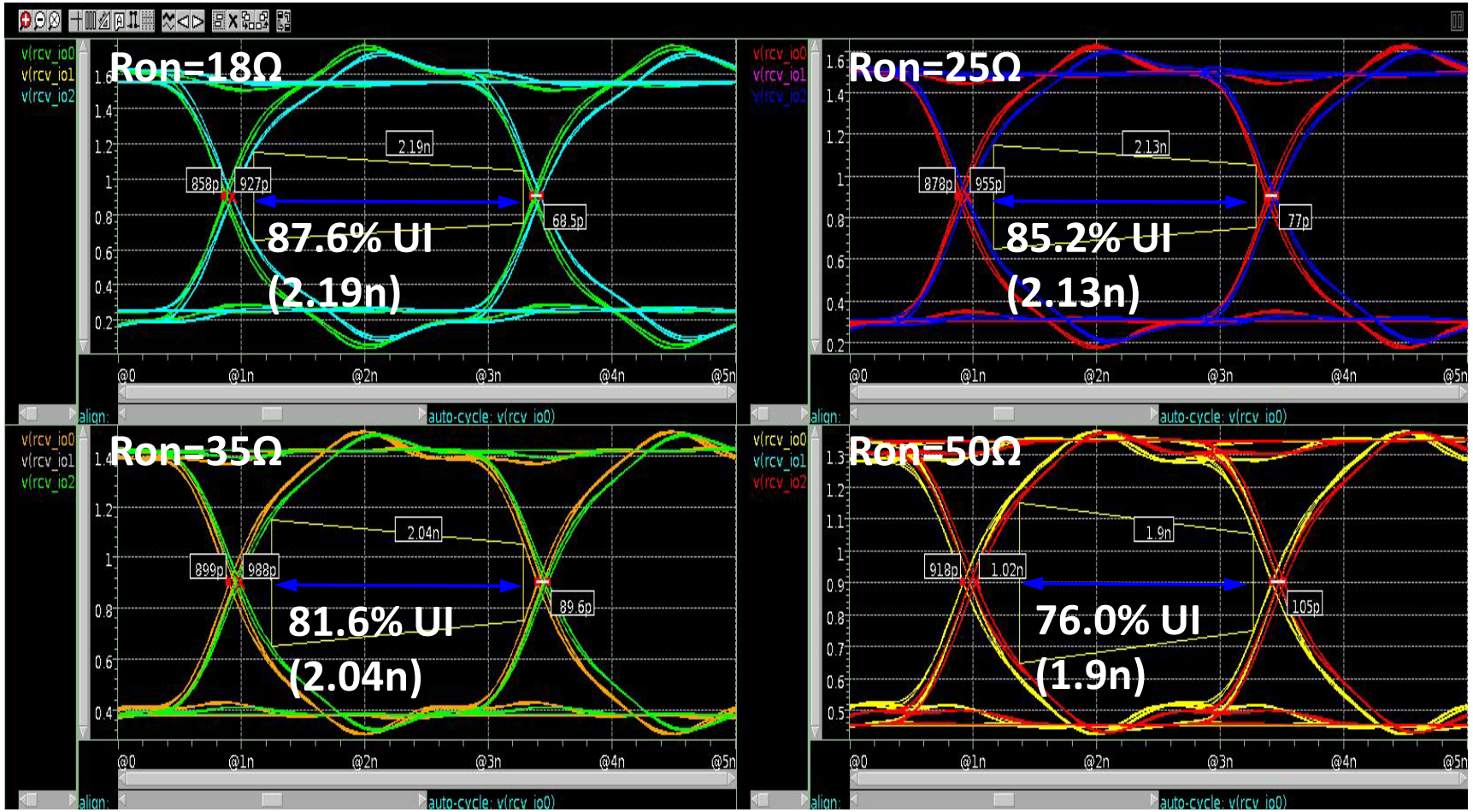
Test Condition

1. Cin : 3.5pF/Die
2. Host Cin: 8pF
3. PKG Cap: 2.03pF
4. VccQ: 1.8V
5. Transmission Line : 50ohm
   (X-talk included)
6. Termination : 100 Ω
7. Freq: 400Mbps(200MHz)

Write Operation without ODT

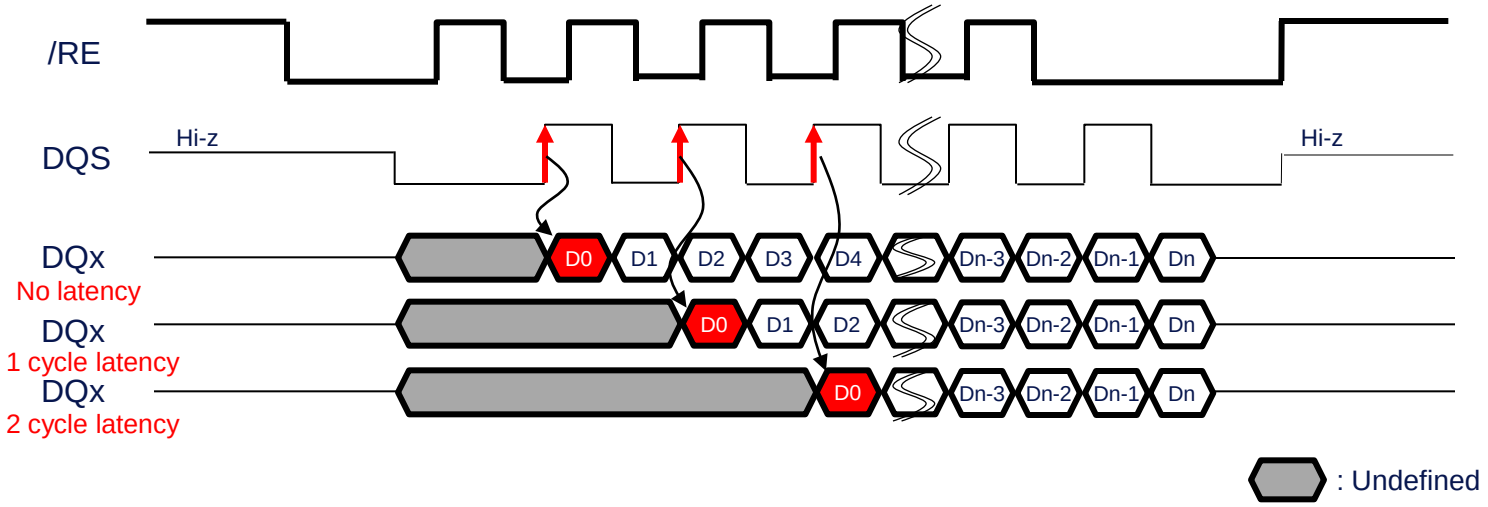


Write Operation with ODT



Latency DQS Cycle

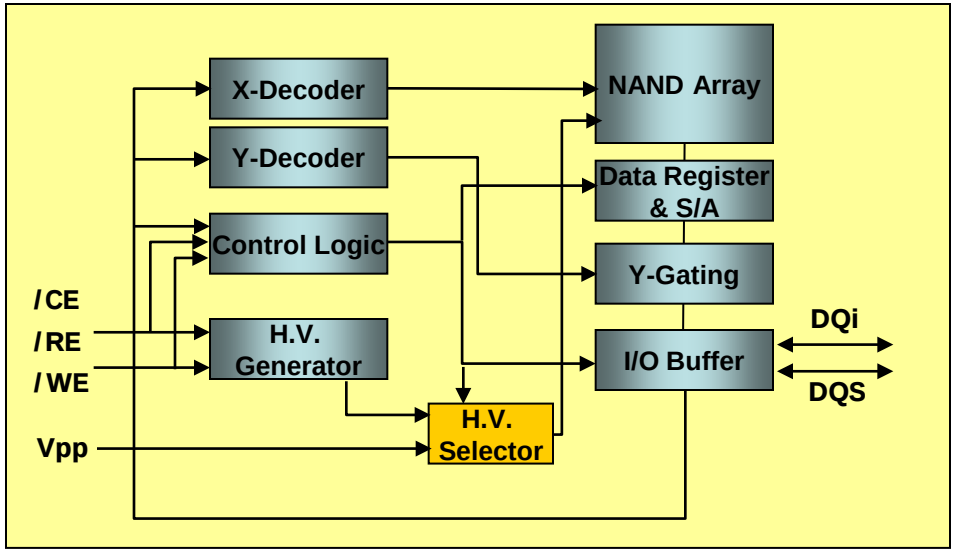
- Pre-toggles of DQS until valid DQS is stabilized
  - Appropriate duty ratio can be obtained
  - Latency provided for current specification is from zero to 4 cycles.
  - Latency DQS Cycle can be programmed for Data In and Data Out respectively.



Note: Features are under discussion and subject to change without notice.

External Vpp for NAND

- Using external power supply reduces current consumption for Program/Read operation
  - On-chip charge pumps have relatively low power efficiency (<30%)
  - In server SSD applications , high voltage source is provided.
  - If NAND can utilize these high voltage source, overall SSD power efficiently can be lowered. (no staggered program operation)



Functional Block Diagram

Parameter	Symbol	Min	Typ.	Max	Unit
External Vpp	Vpp	11.5	12	12.5	V

Note: Features are under discussion and subject to change without notice.

Features Enable / Disable

- New signals and functions can be enabled selectively
  - Features introduced with High-Speed I/F for NAND flash will be available to be enabled or disabled with Feature address 02h.

	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
P0	ODT				Reserved	CMPR	CMPD	Vref
P1	Latency DQS cycles for Data Input (Optional)				Latency DQS cycles for Data Output (Mandatory)			
P2-P3	Reserved(0)							

	Description
Vref	0 : Disabled (default) 1 : Enabled
CMPD (DQS Complement)	0 : Disabled (default) 1 : Enabled
CMPR (RE_n Complement)	0 : Disabled (default) 1 : Enabled
ODT	0000 : Disabled (default) 0001 : Enabled with 150ohm 0010 : Enabled with 100ohm 0011 : Enabled with 75ohm 0100 : Enabled with 50ohm Others reserved for future use
Latency DQS cycles for Data Input /Output	0000 : No latency DQS cycle (default) 0001 : One latency DQS cycle 0010 : Two latency DQS cycle 0011 : Four latency DQS cycle Others reserved for future use

Note: Features are under discussion and subject to change without notice.

Backward Compatibility

- High-Speed NAND Flash supports backward compatibility
  - New signals and functions are user-selective
  - Set feature command is used for changing interface

- ONFi-JEDEC Joint Task Group collaborating to provide a single, industry standard, high-speed NAND interface with backward compatibility.

Join JEDEC for early access to the spec

- For an early and close look at the spec or contribution to standard, please join JEDEC or contact your NAND suppliers

Thank You