a-Si TFT LCD Single Chip Driver with 480RGBx272 resolution and 262K color

CODE Application Notes

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1.BOE4.3 _G8.5(GV043WQQ-N10)-IPS panel

(1) pixel 5-6-5 --8bit and serial interface code

```
Void NV3041A-01_BOE4.3IPS_G8.5__initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);//TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);//TE_ interface_en
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);//00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x01);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x01);//01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);//VBP
NV3041_SPI_Write_data(0x15);//21

NV3041_SPI_Write_cmd(0x45);//VFP
NV3041_SPI_Write_data(0x15);//21

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);//2.07V

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xab);//6.74V/-5.16V

NV3041_SPI_Write_cmd(0xc2);//vgh_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x17);

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);//-10.951

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3a);//35
```

```
NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25); //2e

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x2f);

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x4b);

//NV3041_SPI_Write_cmd(0x7a);// user_vgsp
//NV3041_SPI_Write_data(0x5f);

//test
NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x49);

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
//NV3041_SPI_Write_data(0x4b);
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
//NV3041_SPI_Write_data(0x45);
NV3041_SPI_Write_data(0x1c);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);

////sorce old
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
```

```
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);


NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01-A2,02--A1

//NV3041_SPI_Write_cmd(0x67);
//NV3041_SPI_Write_data(0x33);//01

NV3041_SPI_Write_cmd(0xca);         //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);         //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);         //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);         //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);    //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);
```

```
NV3041_SPI_Write_cmd(0xD1);    //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);    //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);    //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);    //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);    //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);        //DVDD_TRIM
NV3041_SPI_Write_data(0x05);     //1.65        05

NV3041_SPI_Write_cmd(0xe6);        //ESD_CTRL
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x6e);        //LVD_en
NV3041_SPI_Write_data(0x14);

//gammma 01
NV3041_SPI_Write_cmd(0x80);        //gam_vrp0              63
NV3041_SPI_Write_data(0x04);
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0              63
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x81);        //gam_vrp1              62
NV3041_SPI_Write_data(0x07);
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1              62-
NV3041_SPI_Write_data(0x05);

NV3041_SPI_Write_cmd(0x82);        //gam_vrp2              61
NV3041_SPI_Write_data(0x06);
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2              61-
NV3041_SPI_Write_data(0x04);

NV3041_SPI_Write_cmd(0x83);        //gam_vrp3              2
NV3041_SPI_Write_data(0x39);
NV3041_SPI_Write_cmd(0xA3);       //gam_VRN3            2-
NV3041_SPI_Write_data(0x39);

NV3041_SPI_Write_cmd(0x84);        //gam_vrp4              1
NV3041_SPI_Write_data(0x3a);
NV3041_SPI_Write_cmd(0xA4);       //gam_VRN4              1-
NV3041_SPI_Write_data(0x3a);

NV3041_SPI_Write_cmd(0x85);        //gam_vrp5              0
NV3041_SPI_Write_data(0x3f);     //2a~39-0.43
NV3041_SPI_Write_cmd(0xA5);       //gam_VRN5              0-
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x86);        //gam_prp0              50
NV3041_SPI_Write_data(0x2c);     //33
```

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NV3041_SPI_Write_cmd(0xA6);      //gam_PRN0          50-
NV3041_SPI_Write_data(0x2a);     //2a

//NV3041_SPI_Write_cmd(0x87);     //gam_prp1          14
//NV3041_SPI_Write_data(0x46);     //2d
//NV3041_SPI_Write_cmd(0xA7);    //gam_PRN1          14-
//NV3041_SPI_Write_data(0x44);     //2d

NV3041_SPI_Write_cmd(0x87);         //gam_prp1          14
NV3041_SPI_Write_data(0x43);     //2d
NV3041_SPI_Write_cmd(0xA7);         //gam_PRN1          14-
NV3041_SPI_Write_data(0x47);     //2d

NV3041_SPI_Write_cmd(0x88);         //gam_pkp0           59
NV3041_SPI_Write_data(0x08);        //0b
NV3041_SPI_Write_cmd(0xA8);         //gam_PKN0           59-
NV3041_SPI_Write_data(0x08);        //0b

NV3041_SPI_Write_cmd(0x89);         //gam_pkp1          57
NV3041_SPI_Write_data(0x0f);     //14
NV3041_SPI_Write_cmd(0xA9);         //gam_PKN1          57-
NV3041_SPI_Write_data(0x0f);     //14

NV3041_SPI_Write_cmd(0x8a);         //gam_pkp2          54
NV3041_SPI_Write_data(0x17);    //1a
NV3041_SPI_Write_cmd(0xAa);         //gam_PKN2          54-
NV3041_SPI_Write_data(0x17);     //1a

NV3041_SPI_Write_cmd(0x8b);         //gam_PKP3          44
NV3041_SPI_Write_data(0x10);
NV3041_SPI_Write_cmd(0xAb);         //gam_PKN3          44-
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x8c);         //gam_PKP4          38
NV3041_SPI_Write_data(0x16);
NV3041_SPI_Write_cmd(0xAc);         //gam_PKN4          38-
NV3041_SPI_Write_data(0x16);

NV3041_SPI_Write_cmd(0x8d);         //gam_PKP5          32
NV3041_SPI_Write_data(0x14);
NV3041_SPI_Write_cmd(0xAd);    //gam_PKN5          32-
NV3041_SPI_Write_data(0x14);

NV3041_SPI_Write_cmd(0x8e);         //gam_PKP6          26
NV3041_SPI_Write_data(0x11);        //16
NV3041_SPI_Write_cmd(0xAe);         //gam_PKN6          26-
NV3041_SPI_Write_data(0x11);         //13

NV3041_SPI_Write_cmd(0x8f);         //gam_PKP7          20
NV3041_SPI_Write_data(0x14);        //1c
NV3041_SPI_Write_cmd(0xAf);         //gam_PKN7          20-
NV3041_SPI_Write_data(0x14);        //0a

NV3041_SPI_Write_cmd(0x90);         //gam_PKP8          10
NV3041_SPI_Write_data(0x06);
NV3041_SPI_Write_cmd(0xB0);         //gam_PKN8          10-
NV3041_SPI_Write_data(0x06);
```

```
NV3041_SPI_Write_cmd(0x91);          //gam_PKP9          6
NV3041_SPI_Write_data(0x0f);
NV3041_SPI_Write_cmd(0xB1);          //gam_PKN9          6-
NV3041_SPI_Write_data(0x0f);

NV3041_SPI_Write_cmd(0x92);          //gam_PKP10         4
NV3041_SPI_Write_data(0x16);
NV3041_SPI_Write_cmd(0xB2);          //gam_PKN10         4-
NV3041_SPI_Write_data(0x16);

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(200);

NV3041_SPI_Write_cmd(0x29);
Delayms(120);
}
```

(2) pixel 5-6-5 --16bit interface code

```
Void NV3041A-01_BOE4.3IPS_G8.5__initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);//TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);//TE_ interface_en
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);//00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x01);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x03);//01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);//VBP
NV3041_SPI_Write_data(0x15);//21
```

```
NV3041_SPI_Write_cmd(0x45);//VFP
NV3041_SPI_Write_data(0x15);//21

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);//2.07V

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xab);//6.74V/-5.16V

NV3041_SPI_Write_cmd(0xc2);//vgh_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x17);

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);//-10.951

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3a);//35

NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25); //2e

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x6f);//    user_gvdd
NV3041_SPI_Write_data(0x2f);

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x4b);

//NV3041_SPI_Write_cmd(0x7a);// user_vgsp
//NV3041_SPI_Write_data(0x5f);

//test
NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x49);

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
//NV3041_SPI_Write_data(0x4b);
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
//NV3041_SPI_Write_data(0x45);
NV3041_SPI_Write_data(0x1c);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);

////sorce old
```

```
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);


NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01-A2,02--A1
```

```
//NV3041_SPI_Write_cmd(0x67);
//NV3041_SPI_Write_data(0x33);//01

NV3041_SPI_Write_cmd(0xca);         //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);         //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);         //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);         //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);    //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);    //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);    //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);    //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);    //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);    //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);         //DVDD_TRIM
NV3041_SPI_Write_data(0x05);     //1.65       05

NV3041_SPI_Write_cmd(0xe6);         //ESD_CTRL
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x6e);         //LVD_en
NV3041_SPI_Write_data(0x14);

//gammma 01
NV3041_SPI_Write_cmd(0x80);         //gam_vrp0              63
NV3041_SPI_Write_data(0x04);
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0              63
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x81);         //gam_vrp1              62
NV3041_SPI_Write_data(0x07);
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1              62-
NV3041_SPI_Write_data(0x05);

NV3041_SPI_Write_cmd(0x82);         //gam_vrp2              61
NV3041_SPI_Write_data(0x06);
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2              61-
```

```
NV3041_SPI_Write_data(0x04);

NV3041_SPI_Write_cmd(0x83);        //gam_vrp3          2
NV3041_SPI_Write_data(0x39);
NV3041_SPI_Write_cmd(0xA3);        //gam_VRN3          2-
NV3041_SPI_Write_data(0x39);

NV3041_SPI_Write_cmd(0x84);        //gam_vrp4          1
NV3041_SPI_Write_data(0x3a);
NV3041_SPI_Write_cmd(0xA4);        //gam_VRN4          1-
NV3041_SPI_Write_data(0x3a);

NV3041_SPI_Write_cmd(0x85);        //gam_vrp5          0
NV3041_SPI_Write_data(0x3f);     //2a~39-0.43
NV3041_SPI_Write_cmd(0xA5);        //gam_VRN5          0-
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x86);        //gam_prp0          50
NV3041_SPI_Write_data(0x2c);     //33
NV3041_SPI_Write_cmd(0xA6);      //gam_PRN0          50-
NV3041_SPI_Write_data(0x2a);     //2a

//NV3041_SPI_Write_cmd(0x87);      //gam_prp1          14
//NV3041_SPI_Write_data(0x46);     //2d
//NV3041_SPI_Write_cmd(0xA7);    //gam_PRN1          14-
//NV3041_SPI_Write_data(0x44);     //2d

NV3041_SPI_Write_cmd(0x87);        //gam_prp1          14
NV3041_SPI_Write_data(0x43);     //2d
NV3041_SPI_Write_cmd(0xA7);        //gam_PRN1          14-
NV3041_SPI_Write_data(0x47);     //2d

NV3041_SPI_Write_cmd(0x88);        //gam_pkp0          59
NV3041_SPI_Write_data(0x08);       //0b
NV3041_SPI_Write_cmd(0xA8);        //gam_PKN0          59-
NV3041_SPI_Write_data(0x08);       //0b

NV3041_SPI_Write_cmd(0x89);        //gam_pkp1          57
NV3041_SPI_Write_data(0x0f);     //14
NV3041_SPI_Write_cmd(0xA9);        //gam_PKN1          57-
NV3041_SPI_Write_data(0x0f);     //14

NV3041_SPI_Write_cmd(0x8a);        //gam_pkp2          54
NV3041_SPI_Write_data(0x17);    //1a
NV3041_SPI_Write_cmd(0xAa);        //gam_PKN2          54-
NV3041_SPI_Write_data(0x17);     //1a

NV3041_SPI_Write_cmd(0x8b);        //gam_PKP3          44
NV3041_SPI_Write_data(0x10);
NV3041_SPI_Write_cmd(0xAb);        //gam_PKN3          44-
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x8c);        //gam_PKP4          38
NV3041_SPI_Write_data(0x16);
NV3041_SPI_Write_cmd(0xAc);        //gam_PKN4          38-
NV3041_SPI_Write_data(0x16);
```

```
NV3041_SPI_Write_cmd(0x8d);         //gam_PKP5          32
NV3041_SPI_Write_data(0x14);
NV3041_SPI_Write_cmd(0xAd);    //gam_PKN5          32-
NV3041_SPI_Write_data(0x14);

NV3041_SPI_Write_cmd(0x8e);         //gam_PKP6          26
NV3041_SPI_Write_data(0x11);       //16
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6          26-
NV3041_SPI_Write_data(0x11);        //13

NV3041_SPI_Write_cmd(0x8f);         //gam_PKP7          20
NV3041_SPI_Write_data(0x14);       //1c
NV3041_SPI_Write_cmd(0xAf);         //gam_PKN7          20-
NV3041_SPI_Write_data(0x14);       //0a

NV3041_SPI_Write_cmd(0x90);         //gam_PKP8          10
NV3041_SPI_Write_data(0x06);
NV3041_SPI_Write_cmd(0xB0);         //gam_PKN8          10-
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0x91);         //gam_PKP9          6
NV3041_SPI_Write_data(0x0f);
NV3041_SPI_Write_cmd(0xB1);         //gam_PKN9          6-
NV3041_SPI_Write_data(0x0f);

NV3041_SPI_Write_cmd(0x92);         //gam_PKP10         4
NV3041_SPI_Write_data(0x16);
NV3041_SPI_Write_cmd(0xB2);         //gam_PKN10         4-
NV3041_SPI_Write_data(0x16);

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(200);

NV3041_SPI_Write_cmd(0x29);
Delayms(120);
}
```

2. BOE4.3_G6(TT043WQQ-N10)-TN panel

(1) pixel 5-6-5 --8bit and serial interface code

```
Void NV3041A-01_BOE4.3TN_G6__initial (void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);          //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);          //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x00);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x01);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);          //VBP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x45);          //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x13);

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);
```

```
NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x69); //61

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x44);//3F

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x70);     //60

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);

////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
```

```
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);       //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);       //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);       //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);       //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);       //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
```

```
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma
NV3041_SPI_Write_cmd(0x80);       //gam_vrp0
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x82);       //gam_vrp2
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x86);       //gam_prp0
NV3041_SPI_Write_data(0x34);//34
NV3041_SPI_Write_cmd(0xA6);       //gam_PRN0
NV3041_SPI_Write_data(0x34);//34

NV3041_SPI_Write_cmd(0x87);       //gam_prp1
NV3041_SPI_Write_data(0x3C); //3C
NV3041_SPI_Write_cmd(0xA7);       //gam_PRN1
NV3041_SPI_Write_data(0x3D);//3D

NV3041_SPI_Write_cmd(0x83);       //gam_vrp3
NV3041_SPI_Write_data(0x22);//22
NV3041_SPI_Write_cmd(0xA3);       //gam_VRN3
NV3041_SPI_Write_data(0x21);//22
```

```
NV3041_SPI_Write_cmd(0x84);       //gam_vrp4
NV3041_SPI_Write_data(0x20);//20
NV3041_SPI_Write_cmd(0xA4);       //gam_VRN4
NV3041_SPI_Write_data(0x20);//20

NV3041_SPI_Write_cmd(0x85);       //gam_vrp5
NV3041_SPI_Write_data(0x28);//28
NV3041_SPI_Write_cmd(0xA5);       //gam_VRN5
NV3041_SPI_Write_data(0x28);//28
//

NV3041_SPI_Write_cmd(0x88);       //gam_pkp0
NV3041_SPI_Write_data(0x08);//08
NV3041_SPI_Write_cmd(0xA8);       //gam_PKN0
NV3041_SPI_Write_data(0x08);//08

NV3041_SPI_Write_cmd(0x89);       //gam_pkp1
NV3041_SPI_Write_data(0x10); //10
NV3041_SPI_Write_cmd(0xA9);       //gam_PKN1
NV3041_SPI_Write_data(0x10); //10

NV3041_SPI_Write_cmd(0x8a);       //gam_pkp2
NV3041_SPI_Write_data(0x18);//18
NV3041_SPI_Write_cmd(0xAa);       //gam_PKN2
NV3041_SPI_Write_data(0x18);//18

NV3041_SPI_Write_cmd(0x8b);       //gam_PKP3
NV3041_SPI_Write_data(0x13);//13
NV3041_SPI_Write_cmd(0xAb);       //gam_PKN3
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0x8c);       //gam_PKP4
NV3041_SPI_Write_data(0x18);//18
NV3041_SPI_Write_cmd(0xAc);       //gam_PKN4
NV3041_SPI_Write_data(0x18);//18

NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5
NV3041_SPI_Write_data(0x1F);//1F
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5
NV3041_SPI_Write_data(0x0C);//0C

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6
NV3041_SPI_Write_data(0x14);//14
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7
NV3041_SPI_Write_data(0x16);//16
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7
NV3041_SPI_Write_data(0x15);//15

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8
NV3041_SPI_Write_data(0x08);//08
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8
NV3041_SPI_Write_data(0x04);//04
```

```
NV3041_SPI_Write_cmd(0x91);          //gam_PKP9
NV3041_SPI_Write_data(0x0F);//0F
NV3041_SPI_Write_cmd(0xB1);          //gam_PKN9
NV3041_SPI_Write_data(0x0F);//0F

NV3041_SPI_Write_cmd(0x92);          //gam_PKP10
NV3041_SPI_Write_data(0x16);//16
NV3041_SPI_Write_cmd(0xB2);          //gam_PKN10
NV3041_SPI_Write_data(0x15);//15

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

(2) pixel 5-6-5 --16bit interface code

```
  Void NV3041A-01_BOE4.3TN_G6__initial (void)
 {
 //VCI=3.3V
 //---------Reset LCD Driver    -------//
 LCD_RESET=1;
 Delayms( 20 );
 LCD_RESET=0;
 Delayms( 200 );
 LCD_RESET=1;
 Delayms( 120 );

 //---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);          //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);          //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x00);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x03);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);          //VBP
NV3041_SPI_Write_data(0x15);
```

```
NV3041_SPI_Write_cmd(0x45);          //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x13);

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);

NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x69); //61

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x44);//3F

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x70);     //60

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);
```

```
////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
```

```
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);       //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);       //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);       //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);       //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);       //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma
NV3041_SPI_Write_cmd(0x80);       //gam_vrp0
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x82);       //gam_vrp2
```

```
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x86);       //gam_prp0
NV3041_SPI_Write_data(0x34);//34
NV3041_SPI_Write_cmd(0xA6);       //gam_PRN0
NV3041_SPI_Write_data(0x34);//34

NV3041_SPI_Write_cmd(0x87);       //gam_prp1
NV3041_SPI_Write_data(0x3C); //3C
NV3041_SPI_Write_cmd(0xA7);       //gam_PRN1
NV3041_SPI_Write_data(0x3D);//3D

NV3041_SPI_Write_cmd(0x83);       //gam_vrp3
NV3041_SPI_Write_data(0x22);//22
NV3041_SPI_Write_cmd(0xA3);       //gam_VRN3
NV3041_SPI_Write_data(0x21);//22

NV3041_SPI_Write_cmd(0x84);       //gam_vrp4
NV3041_SPI_Write_data(0x20);//20
NV3041_SPI_Write_cmd(0xA4);       //gam_VRN4
NV3041_SPI_Write_data(0x20);//20

NV3041_SPI_Write_cmd(0x85);       //gam_vrp5
NV3041_SPI_Write_data(0x28);//28
NV3041_SPI_Write_cmd(0xA5);       //gam_VRN5
NV3041_SPI_Write_data(0x28);//28
//

NV3041_SPI_Write_cmd(0x88);       //gam_pkp0
NV3041_SPI_Write_data(0x08);//08
NV3041_SPI_Write_cmd(0xA8);       //gam_PKN0
NV3041_SPI_Write_data(0x08);//08

NV3041_SPI_Write_cmd(0x89);       //gam_pkp1
NV3041_SPI_Write_data(0x10); //10
NV3041_SPI_Write_cmd(0xA9);       //gam_PKN1
NV3041_SPI_Write_data(0x10); //10

NV3041_SPI_Write_cmd(0x8a);       //gam_pkp2
NV3041_SPI_Write_data(0x18);//18
NV3041_SPI_Write_cmd(0xAa);       //gam_PKN2
NV3041_SPI_Write_data(0x18);//18

NV3041_SPI_Write_cmd(0x8b);       //gam_PKP3
NV3041_SPI_Write_data(0x13);//13
NV3041_SPI_Write_cmd(0xAb);       //gam_PKN3
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0x8c);       //gam_PKP4
NV3041_SPI_Write_data(0x18);//18
NV3041_SPI_Write_cmd(0xAc);       //gam_PKN4
NV3041_SPI_Write_data(0x18);//18

NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5
NV3041_SPI_Write_data(0x1F);//1F
```

```
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5
NV3041_SPI_Write_data(0x0C);//0C

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6
NV3041_SPI_Write_data(0x14);//14
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7
NV3041_SPI_Write_data(0x16);//16
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7
NV3041_SPI_Write_data(0x15);//15

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8
NV3041_SPI_Write_data(0x08);//08
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8
NV3041_SPI_Write_data(0x04);//04

NV3041_SPI_Write_cmd(0x91);       //gam_PKP9
NV3041_SPI_Write_data(0x0F);//0F
NV3041_SPI_Write_cmd(0xB1);       //gam_PKN9
NV3041_SPI_Write_data(0x0F);//0F

NV3041_SPI_Write_cmd(0x92);       //gam_PKP10
NV3041_SPI_Write_data(0x16);//16
NV3041_SPI_Write_cmd(0xB2);       //gam_PKN10
NV3041_SPI_Write_data(0x15);//15

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

3. Truly4.3(HC261-043T1BDJ)-TN panel

(1) pixel 5-6-5 --8bit and serial interface code

```
Void NV3041A-01_ Truly4.3TN__initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);          //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);          //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x00);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x01);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);          //VBP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x45);          //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgH_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x14);//13

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);
```

```
NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x36); //69

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x34);//44

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x60);     //70

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);

////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
```

```
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);       //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);       //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);       //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);       //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);       //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
```

```
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma     20230606
NV3041_SPI_Write_cmd(0x80);       //gam_vrp0
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x82);       //gam_vrp2
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x86);       //gam_prp0
NV3041_SPI_Write_data(0x3B);//3B
NV3041_SPI_Write_cmd(0xA6);       //gam_PRN0
NV3041_SPI_Write_data(0x28);//28

NV3041_SPI_Write_cmd(0x87);       //gam_prp1
NV3041_SPI_Write_data(0x3C);//3C
NV3041_SPI_Write_cmd(0xA7);       //gam_PRN1
NV3041_SPI_Write_data(0x3B);//3B

NV3041_SPI_Write_cmd(0x83);       //gam_vrp3
NV3041_SPI_Write_data(0x27);//27
NV3041_SPI_Write_cmd(0xA3);       //gam_VRN3
NV3041_SPI_Write_data(0x1d);//1D
```

```
NV3041_SPI_Write_cmd(0x84);       //gam_vrp4
NV3041_SPI_Write_data(0x22);//22
NV3041_SPI_Write_cmd(0xA4);       //gam_VRN4
NV3041_SPI_Write_data(0x1C);//1C

NV3041_SPI_Write_cmd(0x85);       //gam_vrp5
NV3041_SPI_Write_data(0x3f);//3F
NV3041_SPI_Write_cmd(0xA5);       //gam_VRN5
NV3041_SPI_Write_data(0x3f);//3F
//

NV3041_SPI_Write_cmd(0x88);       //gam_pkp0
NV3041_SPI_Write_data(0x0B);//0B
NV3041_SPI_Write_cmd(0xA8);       //gam_PKN0
NV3041_SPI_Write_data(0x05);//05

NV3041_SPI_Write_cmd(0x89);       //gam_pkp1
NV3041_SPI_Write_data(0x12);//12
NV3041_SPI_Write_cmd(0xA9);       //gam_PKN1
NV3041_SPI_Write_data(0x0E);//0E

NV3041_SPI_Write_cmd(0x8a);       //gam_pkp2
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xAa);       //gam_PKN2
NV3041_SPI_Write_data(0x16);//16

NV3041_SPI_Write_cmd(0x8b);       //gam_PKP3
NV3041_SPI_Write_data(0x15);//15
NV3041_SPI_Write_cmd(0xAb);       //gam_PKN3
NV3041_SPI_Write_data(0x11);//11

NV3041_SPI_Write_cmd(0x8c);       //gam_PKP4
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xAc);       //gam_PKN4
NV3041_SPI_Write_data(0x17);//17

NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5
NV3041_SPI_Write_data(0x12);//16
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5
NV3041_SPI_Write_data(0x1A);//16

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6
NV3041_SPI_Write_data(0x14);//14          //
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6
NV3041_SPI_Write_data(0x13);//13          //

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7
NV3041_SPI_Write_data(0x1C);//1C
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8
NV3041_SPI_Write_data(0x0B);//0B
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8
NV3041_SPI_Write_data(0x01);//01
```

```
NV3041_SPI_Write_cmd(0x91);          //gam_PKP9
NV3041_SPI_Write_data(0x12);//12
NV3041_SPI_Write_cmd(0xB1);          //gam_PKN9
NV3041_SPI_Write_data(0x0D);//0D

NV3041_SPI_Write_cmd(0x92);          //gam_PKP10
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xB2);          //gam_PKN10
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

(2) pixel 5-6-5 --16bit interface code

```
Void NV3041A-01_ Truly4.3TN__initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);          //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);          //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x00);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x03);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);          //VBP
NV3041_SPI_Write_data(0x15);
```

```
NV3041_SPI_Write_cmd(0x45);          //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgH_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x14);//13

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);

NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x36); //69

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x34);//44

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x60);     //70

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);
```

```
////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
```

```
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);         //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);         //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);         //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);         //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);         //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);         //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);         //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);         //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);         //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);         //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);         //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);         //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma     20230606
NV3041_SPI_Write_cmd(0x80);         //gam_vrp0
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA0);         //gam_VRN0
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x81);         //gam_vrp1
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA1);         //gam_VRN1
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x82);         //gam_vrp2
```

```
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x86);       //gam_prp0
NV3041_SPI_Write_data(0x3B);//3B
NV3041_SPI_Write_cmd(0xA6);       //gam_PRN0
NV3041_SPI_Write_data(0x28);//28

NV3041_SPI_Write_cmd(0x87);       //gam_prp1
NV3041_SPI_Write_data(0x3C);//3C
NV3041_SPI_Write_cmd(0xA7);       //gam_PRN1
NV3041_SPI_Write_data(0x3B);//3B

NV3041_SPI_Write_cmd(0x83);       //gam_vrp3
NV3041_SPI_Write_data(0x27);//27
NV3041_SPI_Write_cmd(0xA3);       //gam_VRN3
NV3041_SPI_Write_data(0x1d);//1D

NV3041_SPI_Write_cmd(0x84);       //gam_vrp4
NV3041_SPI_Write_data(0x22);//22
NV3041_SPI_Write_cmd(0xA4);       //gam_VRN4
NV3041_SPI_Write_data(0x1C);//1C

NV3041_SPI_Write_cmd(0x85);       //gam_vrp5
NV3041_SPI_Write_data(0x3f);//3F
NV3041_SPI_Write_cmd(0xA5);       //gam_VRN5
NV3041_SPI_Write_data(0x3f);//3F
//

NV3041_SPI_Write_cmd(0x88);       //gam_pkp0
NV3041_SPI_Write_data(0x0B);//0B
NV3041_SPI_Write_cmd(0xA8);       //gam_PKN0
NV3041_SPI_Write_data(0x05);//05

NV3041_SPI_Write_cmd(0x89);       //gam_pkp1
NV3041_SPI_Write_data(0x12);//12
NV3041_SPI_Write_cmd(0xA9);       //gam_PKN1
NV3041_SPI_Write_data(0x0E);//0E

NV3041_SPI_Write_cmd(0x8a);       //gam_pkp2
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xAa);       //gam_PKN2
NV3041_SPI_Write_data(0x16);//16

NV3041_SPI_Write_cmd(0x8b);       //gam_PKP3
NV3041_SPI_Write_data(0x15);//15
NV3041_SPI_Write_cmd(0xAb);       //gam_PKN3
NV3041_SPI_Write_data(0x11);//11

NV3041_SPI_Write_cmd(0x8c);       //gam_PKP4
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xAc);       //gam_PKN4
NV3041_SPI_Write_data(0x17);//17

NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5
NV3041_SPI_Write_data(0x12);//16
```

```
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5
NV3041_SPI_Write_data(0x1A);//16

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6
NV3041_SPI_Write_data(0x14);//14        //
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6
NV3041_SPI_Write_data(0x13);//13        //

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7
NV3041_SPI_Write_data(0x1C);//1C
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8
NV3041_SPI_Write_data(0x0B);//0B
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x91);       //gam_PKP9
NV3041_SPI_Write_data(0x12);//12
NV3041_SPI_Write_cmd(0xB1);       //gam_PKN9
NV3041_SPI_Write_data(0x0D);//0D

NV3041_SPI_Write_cmd(0x92);       //gam_PKP10
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xB2);       //gam_PKN10
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

4. Truly4.3 (SC541)-IPS panel

(1) pixel 5-6-5 --8bit and serial interface code

```
Void NV3041A-01_ Truly4.3 ( SC541)-IPS __initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);          //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);          //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x01);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x01);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);          //VBP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x45);          //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);//0xbb     88             a2

NV3041_SPI_Write_cmd(0xc2);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x13);//05

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);//10

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);    // 35
```

```
NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);    //2e

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x66);

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x37);

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x57);

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);    //0a

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);      //76

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);     //0a

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);       //76

////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
```

```
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//02--A1,01--A2

NV3041_SPI_Write_cmd(0x6e);//lvd
NV3041_SPI_Write_data(0x14);

NV3041_SPI_Write_cmd(0xca);         //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);         //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);      //52

NV3041_SPI_Write_cmd(0xcc);         //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);         //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);         //avcl_mux_st_o[7:0]
```

```
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);       //
NV3041_SPI_Write_data(0x06);    //

NV3041_SPI_Write_cmd(0xf9);       //
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x80);       //gam_vrp0
NV3041_SPI_Write_data(0x08);//00
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0
NV3041_SPI_Write_data(0x08);//00

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1
NV3041_SPI_Write_data(0x06);//05
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1
NV3041_SPI_Write_data(0x05);//03

NV3041_SPI_Write_cmd(0x82);       //gam_vrp2
NV3041_SPI_Write_data(0x02);//02
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2
NV3041_SPI_Write_data(0x01);//02

NV3041_SPI_Write_cmd(0x86);       //gam_prp0
NV3041_SPI_Write_data(0x19);    //2d
NV3041_SPI_Write_cmd(0xA6);       //gam_PRN0
NV3041_SPI_Write_data(0x09);    //1a

NV3041_SPI_Write_cmd(0x87);       //gam_prp1
NV3041_SPI_Write_data(0x2d);     //40
NV3041_SPI_Write_cmd(0xA7);       //gam_PRN1
NV3041_SPI_Write_data(0x2c);     //3f

NV3041_SPI_Write_cmd(0x83);       //gam_vrp3
NV3041_SPI_Write_data(0x35);//38
```

```
NV3041_SPI_Write_cmd(0xA3);       //gam_VRN3
NV3041_SPI_Write_data(0x34);//37

NV3041_SPI_Write_cmd(0x84);       //gam_vrp4
NV3041_SPI_Write_data(0x35);//37
NV3041_SPI_Write_cmd(0xA4);       //gam_VRN4
NV3041_SPI_Write_data(0x35);//36

NV3041_SPI_Write_cmd(0x85);       //gam_vrp5
NV3041_SPI_Write_data(0x28);//28
NV3041_SPI_Write_cmd(0xA5);       //gam_VRN5
NV3041_SPI_Write_data(0x28);//28

NV3041_SPI_Write_cmd(0x88);       //gam_pkp0
NV3041_SPI_Write_data(0x0a);//08
NV3041_SPI_Write_cmd(0xA8);       //gam_PKN0
NV3041_SPI_Write_data(0x02);//04

NV3041_SPI_Write_cmd(0x89);       //gam_pkp1
NV3041_SPI_Write_data(0x13);     //0d
NV3041_SPI_Write_cmd(0xA9);       //gam_PKN1
NV3041_SPI_Write_data(0x07);     //0d

NV3041_SPI_Write_cmd(0x8a);       //gam_pkp2
NV3041_SPI_Write_data(0x1b);//16
NV3041_SPI_Write_cmd(0xAa);       //gam_PKN2
NV3041_SPI_Write_data(0x0f);//14

NV3041_SPI_Write_cmd(0x8b);       //gam_PKP3
NV3041_SPI_Write_data(0x0d);//12
NV3041_SPI_Write_cmd(0xAb);       //gam_PKN3
NV3041_SPI_Write_data(0x0b);//0E

NV3041_SPI_Write_cmd(0x8c);       //gam_PKP4
NV3041_SPI_Write_data(0x11);//15
NV3041_SPI_Write_cmd(0xAc);       //gam_PKN4
NV3041_SPI_Write_data(0x10);//15

NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5
NV3041_SPI_Write_data(0x14);//0e
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5
NV3041_SPI_Write_data(0x0b);//11

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6
NV3041_SPI_Write_data(0x0d);//12
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6
NV3041_SPI_Write_data(0x0d);//11

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7
NV3041_SPI_Write_data(0x16);//19
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7
NV3041_SPI_Write_data(0x0c);//0f

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8
NV3041_SPI_Write_data(0x05);//09
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8
NV3041_SPI_Write_data(0x05);//01
```

```
NV3041_SPI_Write_cmd(0x91);          //gam_PKP9
NV3041_SPI_Write_data(0x0e);//11
NV3041_SPI_Write_cmd(0xB1);          //gam_PKN9
NV3041_SPI_Write_data(0x10);//0d

NV3041_SPI_Write_cmd(0x92);          //gam_PKP10
NV3041_SPI_Write_data(0x15);//19
NV3041_SPI_Write_cmd(0xB2);          //gam_PKN10
NV3041_SPI_Write_data(0x17);//13

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

(2) pixel 5-6-5 --16bit interface code

```
Void NV3041A-01_ Truly4.3 ( SC541)-IPS __initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);          //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);          //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x01);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x03);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);          //VBP
NV3041_SPI_Write_data(0x15);
```

```
NV3041_SPI_Write_cmd(0x45);          //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);//0xbb     88             a2

NV3041_SPI_Write_cmd(0xc2);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x13);//05

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);//10

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);    // 35

NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);    //2e

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x66);

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x37);

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x57);

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);    //0a

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);     //76

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);     //0a

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
```

```
NV3041_SPI_Write_data(0x77);       //76

////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);
```

```
NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//02--A1,01--A2

NV3041_SPI_Write_cmd(0x6e);//lvd
NV3041_SPI_Write_data(0x14);

NV3041_SPI_Write_cmd(0xca);          //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);          //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);       //52

NV3041_SPI_Write_cmd(0xcc);          //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);          //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);          //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);          //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);          //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);          //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);          //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);          //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);          //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);          //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test    mode
NV3041_SPI_Write_cmd(0xf8);          //
NV3041_SPI_Write_data(0x06);     //

NV3041_SPI_Write_cmd(0xf9);          //
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x80);          //gam_vrp0
NV3041_SPI_Write_data(0x08);//00
NV3041_SPI_Write_cmd(0xA0);          //gam_VRN0
NV3041_SPI_Write_data(0x08);//00

NV3041_SPI_Write_cmd(0x81);          //gam_vrp1
NV3041_SPI_Write_data(0x06);//05
NV3041_SPI_Write_cmd(0xA1);          //gam_VRN1
```

```
NV3041_SPI_Write_data(0x05);//03

NV3041_SPI_Write_cmd(0x82);         //gam_vrp2
NV3041_SPI_Write_data(0x02);//02
NV3041_SPI_Write_cmd(0xA2);         //gam_VRN2
NV3041_SPI_Write_data(0x01);//02

NV3041_SPI_Write_cmd(0x86);         //gam_prp0
NV3041_SPI_Write_data(0x19);    //2d
NV3041_SPI_Write_cmd(0xA6);         //gam_PRN0
NV3041_SPI_Write_data(0x09);    //1a

NV3041_SPI_Write_cmd(0x87);         //gam_prp1
NV3041_SPI_Write_data(0x2d);     //40
NV3041_SPI_Write_cmd(0xA7);         //gam_PRN1
NV3041_SPI_Write_data(0x2c);     //3f

NV3041_SPI_Write_cmd(0x83);         //gam_vrp3
NV3041_SPI_Write_data(0x35);//38
NV3041_SPI_Write_cmd(0xA3);         //gam_VRN3
NV3041_SPI_Write_data(0x34);//37

NV3041_SPI_Write_cmd(0x84);         //gam_vrp4
NV3041_SPI_Write_data(0x35);//37
NV3041_SPI_Write_cmd(0xA4);         //gam_VRN4
NV3041_SPI_Write_data(0x35);//36

NV3041_SPI_Write_cmd(0x85);         //gam_vrp5
NV3041_SPI_Write_data(0x28);//28
NV3041_SPI_Write_cmd(0xA5);         //gam_VRN5
NV3041_SPI_Write_data(0x28);//28

NV3041_SPI_Write_cmd(0x88);         //gam_pkp0
NV3041_SPI_Write_data(0x0a);//08
NV3041_SPI_Write_cmd(0xA8);         //gam_PKN0
NV3041_SPI_Write_data(0x02);//04

NV3041_SPI_Write_cmd(0x89);         //gam_pkp1
NV3041_SPI_Write_data(0x13);     //0d
NV3041_SPI_Write_cmd(0xA9);         //gam_PKN1
NV3041_SPI_Write_data(0x07);     //0d

NV3041_SPI_Write_cmd(0x8a);         //gam_pkp2
NV3041_SPI_Write_data(0x1b);//16
NV3041_SPI_Write_cmd(0xAa);         //gam_PKN2
NV3041_SPI_Write_data(0x0f);//14

NV3041_SPI_Write_cmd(0x8b);         //gam_PKP3
NV3041_SPI_Write_data(0x0d);//12
NV3041_SPI_Write_cmd(0xAb);         //gam_PKN3
NV3041_SPI_Write_data(0x0b);//0E

NV3041_SPI_Write_cmd(0x8c);         //gam_PKP4
NV3041_SPI_Write_data(0x11);//15
NV3041_SPI_Write_cmd(0xAc);         //gam_PKN4
NV3041_SPI_Write_data(0x10);//15
```

```
NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5
NV3041_SPI_Write_data(0x14);//0e
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5
NV3041_SPI_Write_data(0x0b);//11

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6
NV3041_SPI_Write_data(0x0d);//12
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6
NV3041_SPI_Write_data(0x0d);//11

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7
NV3041_SPI_Write_data(0x16);//19
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7
NV3041_SPI_Write_data(0x0c);//0f

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8
NV3041_SPI_Write_data(0x05);//09
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8
NV3041_SPI_Write_data(0x05);//01

NV3041_SPI_Write_cmd(0x91);       //gam_PKP9
NV3041_SPI_Write_data(0x0e);//11
NV3041_SPI_Write_cmd(0xB1);       //gam_PKN9
NV3041_SPI_Write_data(0x10);//0d

NV3041_SPI_Write_cmd(0x92);       //gam_PKP10
NV3041_SPI_Write_data(0x15);//19
NV3041_SPI_Write_cmd(0xB2);       //gam_PKN10
NV3041_SPI_Write_data(0x17);//13

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

5. INX4.3 (F043A10-602)-TN panel

(1) pixel 5-6-5 --8bit and serial interface code

```
Void NV3041A-01_ INX4.3 ( F043A10-602)-TN__initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);          //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);          //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x00);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x01);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);          //VBP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x45);          //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgH_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x14);//13

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);
```

```
NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//   VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//   user_vgsp
NV3041_SPI_Write_data(0x1D);//39

NV3041_SPI_Write_cmd(0x6f);//   user_gvdd
NV3041_SPI_Write_data(0x22);//22

NV3041_SPI_Write_cmd(0x78);//   user_gvcl
NV3041_SPI_Write_data(0x4F); //4F

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);


////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);
```

```
NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);       //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);       //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);       //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);       //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);       //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);
```

```
NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma     20230811
NV3041_SPI_Write_cmd(0x80);       //gam_vrp0          0
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0            0-
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1          1
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1            1-
NV3041_SPI_Write_data(0x01);//01

NV3041_SPI_Write_cmd(0x82);       //gam_vrp2          2
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2            2-
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x86);       //gam_prp0          13
NV3041_SPI_Write_data(0x2e);//32
NV3041_SPI_Write_cmd(0xA6);       //gam_PRN0            13-
NV3041_SPI_Write_data(0x26);//22

NV3041_SPI_Write_cmd(0x87);       //gam_prp1            49
NV3041_SPI_Write_data(0x33);//33
NV3041_SPI_Write_cmd(0xA7);       //gam_PRN1            49-
NV3041_SPI_Write_data(0x32);//32

NV3041_SPI_Write_cmd(0x83);       //gam_vrp3           61
NV3041_SPI_Write_data(0x19);//19
NV3041_SPI_Write_cmd(0xA3);       //gam_VRN3             61-
```

```
NV3041_SPI_Write_data(0x15);//15

NV3041_SPI_Write_cmd(0x84);       //gam_vrp4          62
NV3041_SPI_Write_data(0x16);//16
NV3041_SPI_Write_cmd(0xA4);       //gam_VRN4           62-
NV3041_SPI_Write_data(0x11);//11

NV3041_SPI_Write_cmd(0x85);       //gam_vrp5          63
NV3041_SPI_Write_data(0x3f);//3F
NV3041_SPI_Write_cmd(0xA5);       //gam_VRN5           63-
NV3041_SPI_Write_data(0x3f);//3F
//

NV3041_SPI_Write_cmd(0x88);       //gam_pkp0           4
NV3041_SPI_Write_data(0x0B);//0B      //
NV3041_SPI_Write_cmd(0xA8);       //gam_PKN0            4-
NV3041_SPI_Write_data(0x05);//05      //

NV3041_SPI_Write_cmd(0x89);       //gam_pkp1           6
NV3041_SPI_Write_data(0x10);//12
NV3041_SPI_Write_cmd(0xA9);       //gam_PKN1            6-
NV3041_SPI_Write_data(0x10);//0E

NV3041_SPI_Write_cmd(0x8a);       //gam_pkp2           9
NV3041_SPI_Write_data(0x19);//1A
NV3041_SPI_Write_cmd(0xAa);       //gam_PKN2            9-
NV3041_SPI_Write_data(0x17);//16

NV3041_SPI_Write_cmd(0x8b);       //gam_PKP3           19
NV3041_SPI_Write_data(0x15);//15
NV3041_SPI_Write_cmd(0xAb);       //gam_PKN3            19-
NV3041_SPI_Write_data(0x11);//11

NV3041_SPI_Write_cmd(0x8c);       //gam_PKP4           25
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xAc);       //gam_PKN4            25-
NV3041_SPI_Write_data(0x17);//17

NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5            31
NV3041_SPI_Write_data(0x19);//16
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5            31-
NV3041_SPI_Write_data(0x13);//16

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6            37
NV3041_SPI_Write_data(0x14);//14
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6            37-
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7            43
NV3041_SPI_Write_data(0x1C);//1C
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7            43-
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8            53
NV3041_SPI_Write_data(0x0B);//0B
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8          53-
NV3041_SPI_Write_data(0x03);//03
```

```
NV3041_SPI_Write_cmd(0x91);         //gam_PKP9              57
NV3041_SPI_Write_data(0x12);//12
NV3041_SPI_Write_cmd(0xB1);         //gam_PKN9              57-
NV3041_SPI_Write_data(0x0F);//0f

NV3041_SPI_Write_cmd(0x92);         //gam_PKP10         59
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xB2);         //gam_PKN10         59-
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

(2) pixel 5-6-5 --16bit interface code

```
Void NV3041A-01_ INX4.3 ( F043A10-602)-TN__initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);         //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);         //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x00);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x03);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);         //VBP
NV3041_SPI_Write_data(0x15);
```

```
NV3041_SPI_Write_cmd(0x45);         //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgH_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x14);//13

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);

NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//  VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//  user_vgsp
NV3041_SPI_Write_data(0x1D);//39

NV3041_SPI_Write_cmd(0x6f);//  user_gvdd
NV3041_SPI_Write_data(0x22);//22

NV3041_SPI_Write_cmd(0x78);//  user_gvcl
NV3041_SPI_Write_data(0x4F); //4F

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
```

```
NV3041_SPI_Write_data(0x77);


////source
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);
```

```
NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);       //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);       //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);       //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);       //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);       //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma     20230811
NV3041_SPI_Write_cmd(0x80);       //gam_vrp0          0
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0            0-
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1          1
NV3041_SPI_Write_data(0x01);//01
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1            1-
NV3041_SPI_Write_data(0x01);//01
```

```
NV3041_SPI_Write_cmd(0x82);      //gam_vrp2        2
NV3041_SPI_Write_data(0x00);//00
NV3041_SPI_Write_cmd(0xA2);      //gam_VRN2          2-
NV3041_SPI_Write_data(0x00);//00

NV3041_SPI_Write_cmd(0x86);      //gam_prp0        13
NV3041_SPI_Write_data(0x2e);//32
NV3041_SPI_Write_cmd(0xA6);      //gam_PRN0          13-
NV3041_SPI_Write_data(0x26);//22

NV3041_SPI_Write_cmd(0x87);      //gam_prp1          49
NV3041_SPI_Write_data(0x33);//33
NV3041_SPI_Write_cmd(0xA7);      //gam_PRN1          49-
NV3041_SPI_Write_data(0x32);//32

NV3041_SPI_Write_cmd(0x83);      //gam_vrp3          61
NV3041_SPI_Write_data(0x19);//19
NV3041_SPI_Write_cmd(0xA3);      //gam_VRN3          61-
NV3041_SPI_Write_data(0x15);//15

NV3041_SPI_Write_cmd(0x84);      //gam_vrp4          62
NV3041_SPI_Write_data(0x16);//16
NV3041_SPI_Write_cmd(0xA4);      //gam_VRN4          62-
NV3041_SPI_Write_data(0x11);//11

NV3041_SPI_Write_cmd(0x85);      //gam_vrp5          63
NV3041_SPI_Write_data(0x3f);//3F
NV3041_SPI_Write_cmd(0xA5);      //gam_VRN5          63-
NV3041_SPI_Write_data(0x3f);//3F
//

NV3041_SPI_Write_cmd(0x88);      //gam_pkp0          4
NV3041_SPI_Write_data(0x0B);//0B      //
NV3041_SPI_Write_cmd(0xA8);      //gam_PKN0            4-
NV3041_SPI_Write_data(0x05);//05      //

NV3041_SPI_Write_cmd(0x89);      //gam_pkp1          6
NV3041_SPI_Write_data(0x10);//12
NV3041_SPI_Write_cmd(0xA9);      //gam_PKN1            6-
NV3041_SPI_Write_data(0x10);//0E

NV3041_SPI_Write_cmd(0x8a);      //gam_pkp2          9
NV3041_SPI_Write_data(0x19);//1A
NV3041_SPI_Write_cmd(0xAa);      //gam_PKN2            9-
NV3041_SPI_Write_data(0x17);//16

NV3041_SPI_Write_cmd(0x8b);      //gam_PKP3          19
NV3041_SPI_Write_data(0x15);//15
NV3041_SPI_Write_cmd(0xAb);      //gam_PKN3            19-
NV3041_SPI_Write_data(0x11);//11

NV3041_SPI_Write_cmd(0x8c);      //gam_PKP4          25
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xAc);      //gam_PKN4            25-
NV3041_SPI_Write_data(0x17);//17
```

```
NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5          31
NV3041_SPI_Write_data(0x19);//16
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5          31-
NV3041_SPI_Write_data(0x13);//16

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6          37
NV3041_SPI_Write_data(0x14);//14
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6          37-
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7          43
NV3041_SPI_Write_data(0x1C);//1C
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7          43-
NV3041_SPI_Write_data(0x12);//12

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8          53
NV3041_SPI_Write_data(0x0B);//0B
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8      53-
NV3041_SPI_Write_data(0x03);//03

NV3041_SPI_Write_cmd(0x91);       //gam_PKP9          57
NV3041_SPI_Write_data(0x12);//12
NV3041_SPI_Write_cmd(0xB1);       //gam_PKN9          57-
NV3041_SPI_Write_data(0x0F);//0f

NV3041_SPI_Write_cmd(0x92);       //gam_PKP10     59
NV3041_SPI_Write_data(0x1A);//1A
NV3041_SPI_Write_cmd(0xB2);       //gam_PKN10     59-
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
}
```

6. BOE5.0(GV050WQQ-T80)-IPS panel

(1) pixel 5-6-5 --8bit and serial interface code

```
Void NV3041A-01_ BOE5.0(GV050WQQ-T80)-IPS __initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);         //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);         //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);      //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x01);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x01);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);         //VBP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x45);         //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgH_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x14);//13

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);
```

```
NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//  VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//  user_vgsp
NV3041_SPI_Write_data(0x7A);

NV3041_SPI_Write_cmd(0x6f);//  user_gvdd
NV3041_SPI_Write_data(0x49);

NV3041_SPI_Write_cmd(0x78);//  user_gvcl
NV3041_SPI_Write_data(0x57);

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);

NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);

////sorce
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
```

```
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);

NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);       //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);       //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);       //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);       //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);       //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
```

```
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0x6e);//lvd
NV3041_SPI_Write_data(0x14);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma     20230815                          TN            IPS
NV3041_SPI_Write_cmd(0x80);       //gam_vrp0        0             63
NV3041_SPI_Write_data(0x08);//08
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0          0-            63-
NV3041_SPI_Write_data(0x08);//08

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1        1             62
NV3041_SPI_Write_data(0x08);//06
NV3041_SPI_Write_cmd(0xA1);       //gam_VRN1          1-            62-
NV3041_SPI_Write_data(0x08);//05

NV3041_SPI_Write_cmd(0x82);       //gam_vrp2        2             61
NV3041_SPI_Write_data(0x06);//02
NV3041_SPI_Write_cmd(0xA2);       //gam_VRN2          2-            61-
NV3041_SPI_Write_data(0x05);//01

NV3041_SPI_Write_cmd(0x86);       //gam_prp0        13            50
NV3041_SPI_Write_data(0x2b);//19
NV3041_SPI_Write_cmd(0xA6);       //gam_PRN0          13-           50-
NV3041_SPI_Write_data(0x1c);//09

NV3041_SPI_Write_cmd(0x87);       //gam_prp1          49              14
NV3041_SPI_Write_data(0x3a);//2D
NV3041_SPI_Write_cmd(0xA7);       //gam_PRN1          49-           14-
NV3041_SPI_Write_data(0x39);//2C

NV3041_SPI_Write_cmd(0x83);       //gam_vrp3        61              2
```

```
NV3041_SPI_Write_data(0x37);//35
NV3041_SPI_Write_cmd(0xA3);     //gam_VRN3      61-         2-
NV3041_SPI_Write_data(0x36);//34

NV3041_SPI_Write_cmd(0x84);     //gam_vrp4      62          1
NV3041_SPI_Write_data(0x36);//35
NV3041_SPI_Write_cmd(0xA4);     //gam_VRN4      62-         1-
NV3041_SPI_Write_data(0x36);//35

NV3041_SPI_Write_cmd(0x85);     //gam_vrp5      63          0
NV3041_SPI_Write_data(0x28);//28
NV3041_SPI_Write_cmd(0xA5);     //gam_VRN5      63-         0-
NV3041_SPI_Write_data(0x28);//28

NV3041_SPI_Write_cmd(0x88);     //gam_pkp0      4           59
NV3041_SPI_Write_data(0x0a);//0A
NV3041_SPI_Write_cmd(0xA8);     //gam_PKN0      4-          59-
NV3041_SPI_Write_data(0x02);//02

NV3041_SPI_Write_cmd(0x89);     //gam_pkp1      6           57
NV3041_SPI_Write_data(0x12);//13
NV3041_SPI_Write_cmd(0xA9);     //gam_PKN1      6-          57-
NV3041_SPI_Write_data(0x06);//07

NV3041_SPI_Write_cmd(0x8a);     //gam_pkp2      9           54
NV3041_SPI_Write_data(0x1a);//1B
NV3041_SPI_Write_cmd(0xAa);     //gam_PKN2      9-          54-
NV3041_SPI_Write_data(0x0e);//0F

NV3041_SPI_Write_cmd(0x8b);     //gam_PKP3      19          44
NV3041_SPI_Write_data(0x10);//0D
NV3041_SPI_Write_cmd(0xAb);     //gam_PKN3      19-         44-
NV3041_SPI_Write_data(0x0e);//0B

NV3041_SPI_Write_cmd(0x8c);     //gam_PKP4      25          38
NV3041_SPI_Write_data(0x14);//1Q
NV3041_SPI_Write_cmd(0xAc);     //gam_PKN4      25-         38-
NV3041_SPI_Write_data(0x13);//10

NV3041_SPI_Write_cmd(0x8d);     //gam_PKP5      31          32
NV3041_SPI_Write_data(0x17);//14
NV3041_SPI_Write_cmd(0xAd);     //gam_PKN5      31-         32-
NV3041_SPI_Write_data(0x0e);//0B

NV3041_SPI_Write_cmd(0x8e);     //gam_PKP6      37          26
NV3041_SPI_Write_data(0x10);//0D
NV3041_SPI_Write_cmd(0xAe);     //gam_PKN6      37-         26-
NV3041_SPI_Write_data(0x10);//0D

NV3041_SPI_Write_cmd(0x8f);     //gam_PKP7      43          20
NV3041_SPI_Write_data(0x18);//16
NV3041_SPI_Write_cmd(0xAf);     //gam_PKN7      43-         20-
NV3041_SPI_Write_data(0x0e);//0C

NV3041_SPI_Write_cmd(0x90);     //gam_PKP8      53          10
NV3041_SPI_Write_data(0x05);//05
NV3041_SPI_Write_cmd(0xB0);     //gam_PKN8      53-         10-
```

```
NV3041_SPI_Write_data(0x05);//05

NV3041_SPI_Write_cmd(0x91);      //gam_PKP9          57                6
NV3041_SPI_Write_data(0x0d);//0E
NV3041_SPI_Write_cmd(0xB1);      //gam_PKN9        57-                6-
NV3041_SPI_Write_data(0x0f);//10

NV3041_SPI_Write_cmd(0x92);      //gam_PKP10    59                4
NV3041_SPI_Write_data(0x14);//15
NV3041_SPI_Write_cmd(0xB2);      //gam_PKN10    59-               4-
NV3041_SPI_Write_data(0x16);//17

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
 }
```

(2) pixel 5-6-5 --16bit interface code

```
Void NV3041A-01_ BOE5.0(GV050WQQ-T80)-IPS __initial(void)
{
//VCI=3.3V
//---------Reset LCD Driver    -------//
LCD_RESET=1;
Delayms( 20 );
LCD_RESET=0;
Delayms( 200 );
LCD_RESET=1;
Delayms( 120 );

//---------Start Initial Code ------//
NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0xa5);

NV3041_SPI_Write_cmd(0xE7);      //TE_output_en
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0x35);      //TE_ interface_en
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x3A);
NV3041_SPI_Write_data(0x01);     //00---666//01--565

NV3041_SPI_Write_cmd(0x40);
NV3041_SPI_Write_data(0x01);    //01:IPS/00:TN

NV3041_SPI_Write_cmd(0x41);
NV3041_SPI_Write_data(0x03);    //01--8bit//03--16bit

NV3041_SPI_Write_cmd(0x55);
NV3041_SPI_Write_data(0x01);

NV3041_SPI_Write_cmd(0x44);      //VBP
```

```
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x45);         //VFP
NV3041_SPI_Write_data(0x15);

NV3041_SPI_Write_cmd(0x7d);//vdds_trim[2:0]
NV3041_SPI_Write_data(0x03);

NV3041_SPI_Write_cmd(0xc1);//avdd_clp_en avdd_clp[1:0] avcl_clp_en avcl_clp[1:0]
NV3041_SPI_Write_data(0xbb);

NV3041_SPI_Write_cmd(0xc2);//vgH_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x14);//13

NV3041_SPI_Write_cmd(0xc3);//vgl_clp_en vgl_clp[2:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xc6);//avdd_ratio_sel avcl_ratio_sel vgh_ratio_sel[1:0] vgl_ratio_sel[1:0]
NV3041_SPI_Write_data(0x3e);

NV3041_SPI_Write_cmd(0xc7);//mv_clk_sel[1:0] avdd_clk_sel[1:0] avcl_clk_sel[1:0]
NV3041_SPI_Write_data(0x25);

NV3041_SPI_Write_cmd(0xc8);//  VGL_CLK_sel
NV3041_SPI_Write_data(0x11);

NV3041_SPI_Write_cmd(0x7a);//  user_vgsp
NV3041_SPI_Write_data(0x7A);

NV3041_SPI_Write_cmd(0x6f);//  user_gvdd
NV3041_SPI_Write_data(0x49);

NV3041_SPI_Write_cmd(0x78);//  user_gvcl
NV3041_SPI_Write_data(0x57);

NV3041_SPI_Write_cmd(0x73);//osc
NV3041_SPI_Write_data(0x08);

NV3041_SPI_Write_cmd(0x74);
NV3041_SPI_Write_data(0x13);//13

NV3041_SPI_Write_cmd(0xc9);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x67);
NV3041_SPI_Write_data(0x33);

//gate_ed
NV3041_SPI_Write_cmd(0x51);//gate_st_o[7:0]
NV3041_SPI_Write_data(0x4b);

NV3041_SPI_Write_cmd(0x52);//gate_ed_o[7:0]
NV3041_SPI_Write_data(0x7c);

NV3041_SPI_Write_cmd(0x53);//gate_st_e[7:0]
NV3041_SPI_Write_data(0x45);
```

```
NV3041_SPI_Write_cmd(0x54);//gate_ed_e[7:0]
NV3041_SPI_Write_data(0x77);

////sorce
NV3041_SPI_Write_cmd(0x46);//fsm_hbp_o[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x47);//fsm_hfp_o[5:0]
NV3041_SPI_Write_data(0x2a);

NV3041_SPI_Write_cmd(0x48);//fsm_hbp_e[5:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0x49);//fsm_hfp_e[5:0]
NV3041_SPI_Write_data(0x1a);

NV3041_SPI_Write_cmd(0x56);//src_ld_wd[1:0] src_ld_st[5:0]
NV3041_SPI_Write_data(0x43);

NV3041_SPI_Write_cmd(0x57);//pn_cs_en src_cs_st[5:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0x58);//src_cs_p_wd[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x59);//src_cs_n_wd[6:0]
NV3041_SPI_Write_data(0x64);

NV3041_SPI_Write_cmd(0x5a);//src_pchg_st_o[6:0]
NV3041_SPI_Write_data(0x41);

NV3041_SPI_Write_cmd(0x5b);//src_pchg_wd_o[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5c);//src_pchg_st_e[6:0]
NV3041_SPI_Write_data(0x02);

NV3041_SPI_Write_cmd(0x5d);//src_pchg_wd_e[6:0]
NV3041_SPI_Write_data(0x3c);

NV3041_SPI_Write_cmd(0x5e);//src_pol_sw[7:0]
NV3041_SPI_Write_data(0x1f);

NV3041_SPI_Write_cmd(0x60);//src_op_st_o[7:0]
NV3041_SPI_Write_data(0x80);

NV3041_SPI_Write_cmd(0x61);//src_op_st_e[7:0]
NV3041_SPI_Write_data(0x3f);

NV3041_SPI_Write_cmd(0x62);//src_op_ed_o[9:8] src_op_ed_e[9:8]
NV3041_SPI_Write_data(0x21);

NV3041_SPI_Write_cmd(0x63);//src_op_ed_o[7:0]
NV3041_SPI_Write_data(0x07);

NV3041_SPI_Write_cmd(0x64);//src_op_ed_e[7:0]
NV3041_SPI_Write_data(0xe0);
```

```
NV3041_SPI_Write_cmd(0x65);//chopper
NV3041_SPI_Write_data(0x01);//01--A2,02---A1

NV3041_SPI_Write_cmd(0xca);       //avdd_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xcb);       //avdd_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xcc);       //avdd_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xcD);       //avdd_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD0);       //avcl_mux_st_o[7:0]
NV3041_SPI_Write_data(0x20);

NV3041_SPI_Write_cmd(0xD1);       //avcl_mux_ed_o[7:0]
NV3041_SPI_Write_data(0x52);

NV3041_SPI_Write_cmd(0xD2);       //avcl_mux_st_e[7:0]
NV3041_SPI_Write_data(0x10);

NV3041_SPI_Write_cmd(0xD3);       //avcl_mux_ed_e[7:0]
NV3041_SPI_Write_data(0x42);

NV3041_SPI_Write_cmd(0xD4);       //vgh_mux_st[7:0]
NV3041_SPI_Write_data(0x0a);

NV3041_SPI_Write_cmd(0xD5);       //vgh_mux_ed[7:0]
NV3041_SPI_Write_data(0x32);

NV3041_SPI_Write_cmd(0x6e);//lvd
NV3041_SPI_Write_data(0x14);

NV3041_SPI_Write_cmd(0xe5);       //DVDD_TRIM
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xe6);       //ESD_CTRL
NV3041_SPI_Write_data(0x00);

///test   mode
NV3041_SPI_Write_cmd(0xf8);
NV3041_SPI_Write_data(0x06);

NV3041_SPI_Write_cmd(0xf9);
NV3041_SPI_Write_data(0x00);

//gammma     20230815                              TN              IPS
NV3041_SPI_Write_cmd(0x80);       //gam_vrp0          0               63
NV3041_SPI_Write_data(0x08);//08
NV3041_SPI_Write_cmd(0xA0);       //gam_VRN0          0-              63-
NV3041_SPI_Write_data(0x08);//08

NV3041_SPI_Write_cmd(0x81);       //gam_vrp1          1               62
```

```
NV3041_SPI_Write_data(0x08);//06
NV3041_SPI_Write_cmd(0xA1);      //gam_VRN1        1-          62-
NV3041_SPI_Write_data(0x08);//05

NV3041_SPI_Write_cmd(0x82);      //gam_vrp2        2           61
NV3041_SPI_Write_data(0x06);//02
NV3041_SPI_Write_cmd(0xA2);      //gam_VRN2        2-          61-
NV3041_SPI_Write_data(0x05);//01

NV3041_SPI_Write_cmd(0x86);      //gam_prp0        13          50
NV3041_SPI_Write_data(0x2b);//19
NV3041_SPI_Write_cmd(0xA6);      //gam_PRN0        13-         50-
NV3041_SPI_Write_data(0x1c);//09

NV3041_SPI_Write_cmd(0x87);      //gam_prp1        49          14
NV3041_SPI_Write_data(0x3a);//2D
NV3041_SPI_Write_cmd(0xA7);      //gam_PRN1        49-         14-
NV3041_SPI_Write_data(0x39);//2C

NV3041_SPI_Write_cmd(0x83);      //gam_vrp3        61          2
NV3041_SPI_Write_data(0x37);//35
NV3041_SPI_Write_cmd(0xA3);      //gam_VRN3        61-         2-
NV3041_SPI_Write_data(0x36);//34

NV3041_SPI_Write_cmd(0x84);      //gam_vrp4        62          1
NV3041_SPI_Write_data(0x36);//35
NV3041_SPI_Write_cmd(0xA4);      //gam_VRN4        62-         1-
NV3041_SPI_Write_data(0x36);//35

NV3041_SPI_Write_cmd(0x85);      //gam_vrp5        63          0
NV3041_SPI_Write_data(0x28);//28
NV3041_SPI_Write_cmd(0xA5);      //gam_VRN5        63-         0-
NV3041_SPI_Write_data(0x28);//28

NV3041_SPI_Write_cmd(0x88);      //gam_pkp0        4           59
NV3041_SPI_Write_data(0x0a);//0A
NV3041_SPI_Write_cmd(0xA8);      //gam_PKN0        4-          59-
NV3041_SPI_Write_data(0x02);//02

NV3041_SPI_Write_cmd(0x89);      //gam_pkp1        6           57
NV3041_SPI_Write_data(0x12);//13
NV3041_SPI_Write_cmd(0xA9);      //gam_PKN1        6-          57-
NV3041_SPI_Write_data(0x06);//07

NV3041_SPI_Write_cmd(0x8a);      //gam_pkp2        9           54
NV3041_SPI_Write_data(0x1a);//1B
NV3041_SPI_Write_cmd(0xAa);      //gam_PKN2        9-          54-
NV3041_SPI_Write_data(0x0e);//0F

NV3041_SPI_Write_cmd(0x8b);      //gam_PKP3        19          44
NV3041_SPI_Write_data(0x10);//0D
NV3041_SPI_Write_cmd(0xAb);      //gam_PKN3        19-         44-
NV3041_SPI_Write_data(0x0e);//0B

NV3041_SPI_Write_cmd(0x8c);      //gam_PKP4        25          38
NV3041_SPI_Write_data(0x14);//1Q
NV3041_SPI_Write_cmd(0xAc);      //gam_PKN4        25-         38-
```

```
NV3041_SPI_Write_data(0x13);//10

NV3041_SPI_Write_cmd(0x8d);       //gam_PKP5        31              32
NV3041_SPI_Write_data(0x17);//14
NV3041_SPI_Write_cmd(0xAd);       //gam_PKN5        31-             32-
NV3041_SPI_Write_data(0x0e);//0B

NV3041_SPI_Write_cmd(0x8e);       //gam_PKP6        37              26
NV3041_SPI_Write_data(0x10);//0D
NV3041_SPI_Write_cmd(0xAe);       //gam_PKN6        37-             26-
NV3041_SPI_Write_data(0x10);//0D

NV3041_SPI_Write_cmd(0x8f);       //gam_PKP7        43              20
NV3041_SPI_Write_data(0x18);//16
NV3041_SPI_Write_cmd(0xAf);       //gam_PKN7        43-             20-
NV3041_SPI_Write_data(0x0e);//0C

NV3041_SPI_Write_cmd(0x90);       //gam_PKP8        53              10
NV3041_SPI_Write_data(0x05);//05
NV3041_SPI_Write_cmd(0xB0);       //gam_PKN8        53-             10-
NV3041_SPI_Write_data(0x05);//05

NV3041_SPI_Write_cmd(0x91);       //gam_PKP9        57              6
NV3041_SPI_Write_data(0x0d);//0E
NV3041_SPI_Write_cmd(0xB1);       //gam_PKN9        57-             6-
NV3041_SPI_Write_data(0x0f);//10

NV3041_SPI_Write_cmd(0x92);       //gam_PKP10       59              4
NV3041_SPI_Write_data(0x14);//15
NV3041_SPI_Write_cmd(0xB2);       //gam_PKN10       59-             4-
NV3041_SPI_Write_data(0x16);//17

NV3041_SPI_Write_cmd(0xff);
NV3041_SPI_Write_data(0x00);

NV3041_SPI_Write_cmd(0x11);
Delayms(120);

NV3041_SPI_Write_cmd(0x29);
Delayms(20);
```

Revision History

Version No.	Data	Description
V1.0	2023/07/26	New
V1.1	2023/08/16	ADD INX4.3 (F043A10-602)-TN panel ADD BOE5.0(GV050WQQ-T80)-IPS panel
V1.2	2023/10/18	Modified BOE4.3_G8.5(GV043WQQ-N10)-IPS panel