

Overview and Comparison of Modulation and Control Strategies for a Nonresonant Single-Phase Dual-Active-Bridge DC–DC Converter

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Abstract—The nonresonant single-phase dual-active-bridge (NSDAB) dc–dc converter has been increasingly adopted for isolated dc–dc power conversion systems. Over the past few years, significant research has been carried out to address the technical challenges associated with modulations and controls of the NSDAB dc–dc converter. The aim of this paper is to review and compare these recent state-of-the-art modulation and control strategies. First, the modulation strategies for the NSDAB dc–dc converter are analyzed. All possible phase-shift patterns are demonstrated, and the correlation analysis of the typical phases-shift modulation methods for the NSDAB dc–dc converter is presented. Then, an overview of steady-state efficiency-optimization strategies is discussed for the NSDAB dc–dc converter. Moreover, a review of optimized techniques for dynamic responses is also provided. For both the efficiency and dynamic optimizations, thorough comparisons and recommendations are provided in this paper. Finally, to improve both steady-state and transient performances, a combination approach to optimize both the efficiency and dynamics for an NSDAB dc–dc converter based on the reviewed methods is presented in this paper.

Index Terms—Current feedback control, current stress, dual-active-bridge (DAB) converter, dynamic performances, efficiency, observer-based control, power control, power losses, reactive power.

NOMENCLATURE

NSDAB	Nonresonant single-phase dual-active-bridge.	RMS	Root mean square.
EV	Electrical vehicle.	MRMSC	Minimized rms current.
SST	Solid-state transformer.	CSO	Current-stress-optimized.
BTB	Back-to-back.	MCSO	Minimum CSO.
MMDCT	Modular multilevel dc-link solid-state transformer.	NZVS	Non-ZVS.
SPS	Single-phase-shift.	FCSLC	Feedforward compensation strategy with the load current.
ZVS	Zero-voltage-switching.	SLFC	Simplified load-feedforward control.
DPS	Dual-phase-shift.	FTBC	Fast transient boundary control.
EPS	Extended-phase-shift.	ADSM	Asymmetric double-side modulation method.
TPS	Triple-phase-shift.	PCMC	Predictive current-mode control.
		VDPC	Virtual-direct-power control.
		CSC	Current sensorless control.
		NDO	Nonlinear disturbance observer.
		HSDO	Hybrid static and dynamic optimization.
		No.	Number.
		<i>n</i>	Transformer turn ratio.
		<i>i</i> ₀	Inductance current when S ₁ is turned ON.
		<i>i</i> ₁	Inductance current when S ₃ is turned ON.
		<i>i</i> ₂	Inductance current when S ₂ is turned ON.
		<i>i</i> ₃	Inductance current when S ₄ is turned ON.
		<i>i</i> ₄	Inductance current when S ₅ is turned ON.
		<i>i</i> ₅	Inductance current when S ₇ is turned ON.
		<i>i</i> ₆	Simplified inductance current when S ₆ is turned ON.
		<i>i</i> ₇	Simplified inductance current when S ₈ is turned ON.
		<i>i</i> _{0u}	Simplified inductance current when S ₁ is turned ON.
		<i>i</i> _{1u}	Simplified inductance current when S ₃ is turned ON.
		<i>i</i> _{2u}	Simplified inductance current when S ₂ is turned ON.
		<i>i</i> _{3u}	Simplified inductance current when S ₄ is turned ON.
		<i>i</i> _{4u}	Simplified inductance current when S ₅ is turned ON.
		<i>i</i> _{5u}	Simplified inductance current when S ₇ is turned ON.
		<i>i</i> _{6u}	Simplified inductance current when S ₆ is turned ON.
		<i>i</i> _{7u}	Simplified inductance current when S ₈ is turned ON.

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U_o	Output voltage.
U_{ab}	Output voltage generated by primary-side H bridge.
U_{cd}	Output voltage generated by secondary-side H bridge.
i_L	Inductance current.
$ i_L _{\text{avg}}$	Average absolute value of the inductance current.
i_{LRMS}	RMS value of the inductance current.
T_s	Switching period.
f_s	Switching frequency.
ω_s	Radian frequency according to switching frequency.
i_o	Load current.
i_{in}	Input current.
n	Transformer turn ratio.
$k = nU_{\text{in}}/U_o$	Voltage ratio.
i_2	Output current generated by secondary-side H bridge.
I_2	DC component of i_2 .
i_{ac2}	AC component of i_2 .
P	Transferred power.
p	Simplified transferred power.
i_p	Simplified peak current.
C_{in}	Input-side capacitor.
C_o	Output-side capacitor.
C_s	Parallel capacitor for each switch.
m, q	Order of voltage harmonics.
D	Phase-shift ratio for the SPS modulation method.
D_{EP1}	Inner phase-shift ratio for the EPS modulation method at primary side.
D_{ES1}	Inner phase-shift ratio for the EPS modulation method at secondary side.
D_{E2}	Outer phase-shift ratio for the EPS modulation method.
D_{D1}	Inner phase-shift ratio for the DPS modulation method.
D_{D2}	Outer phase-shift ratio for the DPS modulation method.
D_1, D_2, D_3	Phase-shift ratios for TPS modulation with the positive transferred power.
D'_1, D'_2, D'_3	Phase-shift ratios of TPS modulation for the negative transferred power.

I. INTRODUCTION

THE nonresonant single-phase dual-active-bridge (NSDAB) dc–dc converter was first proposed around 1990s for realizing high-efficiency and high-power-density dc–dc power conversions [1], [2]. The topology of an NSDAB is shown in Fig. 1, and its equivalent circuit can be illustrated in Fig. 2. With continuous development over these years, the NSDAB dc–dc converter, which can form series and parallel connections [3], has become one of the most attractive isolated dc–dc power conversion topologies for dc grid [4]–[10], solid-state transformer (SST) [11]–[13], automotive application [14]–[19], energy storage system [20]–[22], and aerospace application [23],

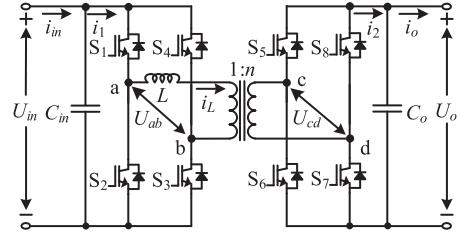


Fig. 1. Topology of an NSDAB dc–dc converter.

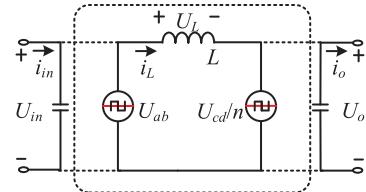


Fig. 2. Equivalent topology of an NSDAB dc–dc converter.

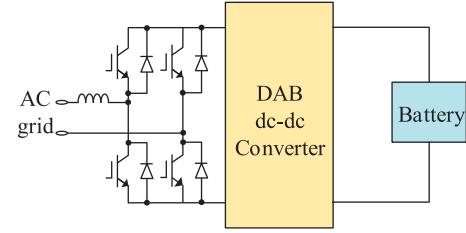


Fig. 3. Topology of an NSDAB-based EV battery charger [15], [19].

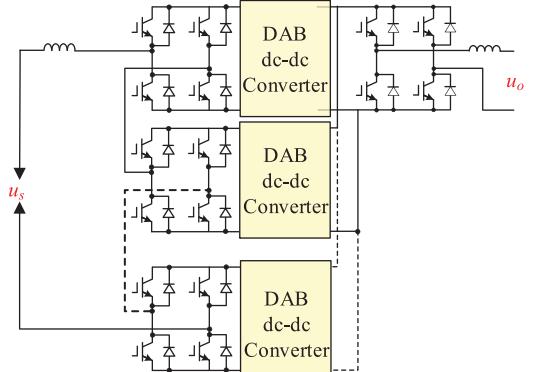


Fig. 4. Cascaded multilevel converter-based three-stage SST topology [25].

[24], e.g., the NSDAB dc–dc converter is a very promising choice for electrical vehicle (EV) charger, as illustrated in Fig. 3 [15], [19]. The NSDAB-based SST, as shown in Fig. 4, has been regarded as one of the main emerging techniques in power distribution system [25]. Moreover, based on the NSDAB dc–dc converter, the back-to-back (BTB) system has been investigated to solve the problem of power flow balancing between ac grids [26], which can be employed to replace the line frequency transformer and shown as Fig. 5. In addition, to connect different dc grids at different voltage levels, the modular multilevel dc-link solid-state transformer (MMDCT) system with NSDAB dc–dc

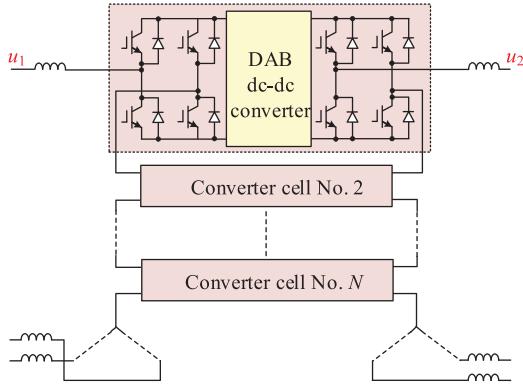


Fig. 5. BTB system in the next-generation medium-voltage power conversion system [26].

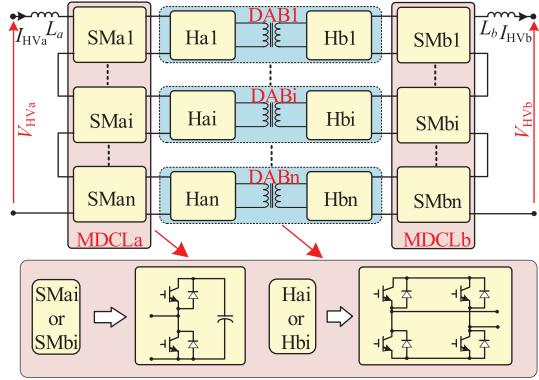


Fig. 6. Modular multilevel dc-link SST system [27].

converters is proposed, as shown in Fig. 6. The MMDCT not only has the same modularity and flexibility but also has good fault handling capacity [27].

Over the past decade, there has been a significant effort toward dealing with the technical challenges for the efficiency optimization and the dynamics improvement of the NSDAB dc–dc converter. However, so far there is a lack of comprehensive analysis and comparison of various operation strategies, making it difficult to decide which method to adopt under different circumstances. Thus, the main intention of this paper is to provide a better understanding of the NSDAB converter control and operation in terms of both the static and dynamic performance, and comprehensively reviews the most recent advancements and contributions on the phase-shift modulations, efficiency-optimization methods, and dynamic-improvement techniques of the NSDAB dc–dc converter. A thorough comparison of different control strategies is also presented in this paper to provide guidance on which method to use under various applications.

The rest of this paper is organized as follows. Section II introduces the typical phase-shift modulations of the NSDAB dc–dc converter. To provide a better understanding of the phase-shift modulation, all possible phase-shift patterns are presented, and the correlation analysis of the typical phase-shift modulation methods is also analyzed. This is followed by a thorough review of latest contributions to the efficiency-optimization strategies for the NSDAB converter. Based on the reviewed optimized

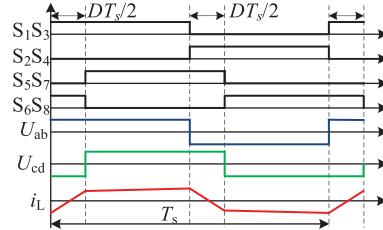


Fig. 7. Waveforms of the SPS modulation method.

schemes, the recommendation is given to address the efficiency issue of an NSDAB dc–dc converter in Section III. Section IV covers the latest dynamic-optimized techniques for the NSDAB converter under different applications and operating conditions. According to specific operating conditions, suggestions for dynamic-improvement strategies are provided in this section. Finally, a general efficiency and dynamic-optimization principle of the NSDAB dc–dc converter is presented in Section V, and a hybrid method that improves both steady-state and transient performances are presented with verification results. The concluding remarks are presented in Section VI.

II. OVERVIEW OF THE PHASE-SHIFT MODULATION METHODS

Generally, the phase-shift modulations have been the most attractive modulation techniques for the NSDAB dc–dc converter. The single-phase-shift (SPS) modulation method, as shown in Fig. 7 (where D is the phase-shift ratio), is presented originally when the NSDAB dc–dc converter is proposed [1], [2]. The performance characteristics of the NSDAB converter under SPS control are reasonably good with less device and component stresses, small filter components, reduced switching losses, bidirectional power flow, buck–boost operation, low sensitivity to parasitic parameters, and simple first-order stable dynamics [26], [28], [29]. Although, the NSDAB dc–dc converter can achieve a good efficiency under the SPS modulation when both side voltages are matched, the SPS modulation method will always result in high-circulating power and limited zero-voltage-switching (ZVS) range when both side voltages are mismatched, which negatively influences the efficiency of an NSDAB dc–dc converter [30]–[37]. Thus, some typical phase-shift modulation methods, including dual-phase-shift (DPS) modulation, extended-phase-shift (EPS) modulation, and triple-phase-shift (TPS) modulation, are proposed in recent years to deal with these challenges and boost the efficiency of an NSDAB dc–dc converter.

A. DPS Modulation Method

The DPS modulation method is an improved phase-shift modulation method for the NSDAB dc–dc converter [30]. As shown in Fig. 8, different from the SPS modulation scheme, an inner phase-shift ratio D_{D1} is added to both side H bridges under the DPS modulation method, and the another phase-shift ratio D_{D2} determines the relative position between the output voltages of the input side and the output side H bridges. As shown in Fig. 8, the DPS modulation usually has two different conditions according to relationship of D_{D1} and D_{D2} . When

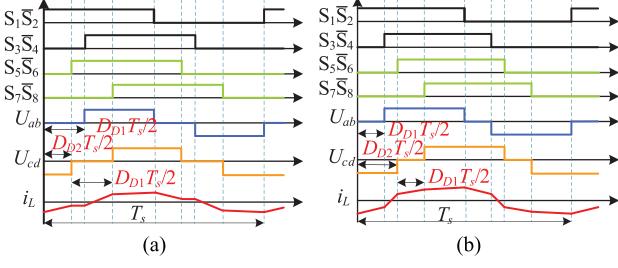


Fig. 8. Waveforms of the DPS modulation method. (a) $0 \leq D_{D2} \leq D_{D1} \leq 1$. (b) $0 \leq D_{D1} < D_{D2} \leq 1$.

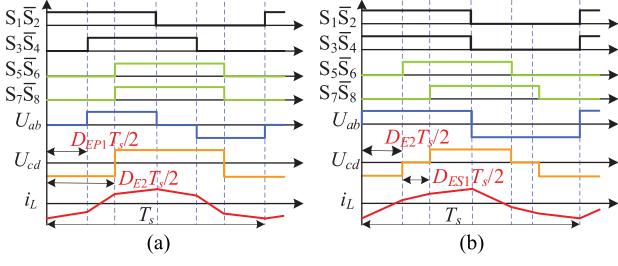


Fig. 9. Waveforms of the EPS modulation method. (a) D_{EP1} at the input-side H bridge. (b) D_{ES1} at the output-side H bridge.

$0 \leq D_{D2} \leq D_{D1} \leq 1$, example waveforms of the DPS modulation can be shown in Fig. 8(a), and when $0 \leq D_{D1} < D_{D2} \leq 1$, example waveforms of the DPS modulation can be shown in Fig. 8(b). Compared with the SPS modulation method, the DPS modulation method can be employed to decrease the current stress, expand the ZVS operation range, and reduce the nonactive power of the NSDAB dc-dc converter [38]–[40].

B. EPS Modulation Method

EPS control is proposed in [31], [35], and [41], and is shown in Fig. 9. Different from the DPS modulation, an inner phase-shift ratio D_{E1} is added to the input-side H bridge or the output-side H bridge. Therefore, there are also two conditions of the EPS modulation according to the position of the inner phase-shift ratio. When D_{EP1} is added to the primary-side H bridge, waveforms of the EPS modulation can be shown in Fig. 9(a), and when D_{ES1} is added to the secondary-side H bridge, waveforms of the EPS modulation can be shown in Fig. 9(b). Similar to the DPS modulation method, the EPS modulation method can also be used to decrease the current stress, expand the ZVS operation range, and reduce the reactive power [42]–[44]. Different from the DPS modulation method, it is worth mentioning that when NSDAB are changed between buck and boost modes, the inner phase-shift ratio of the EPS modulation method should be changed to the high voltage side to boost the efficiency properly.

C. TPS Modulation Method

The TPS modulation method is first emerged in [45] and [46], and it can be shown in Fig. 10, where $i_0, i_1, i_2, i_3, i_4, i_5, i_6$, and i_7 are the boundary inductance currents of the NSDAB dc-dc converter (these boundary inductance currents will be used to

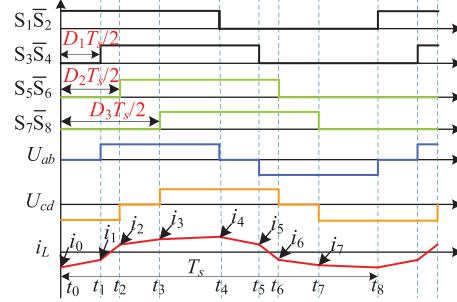


Fig. 10. Waveforms of the TPS modulation method.

determine ZVS performances in Section III). Similar to the DPS modulation method, both sides of the H bridge output voltages contain the inner phase-shift ratios, but these two-inner phase-shift ratios may be different. With three phase-shift ratios D_1, D_2 , and D_3 for the NSDAB converter, the TPS modulation method can obtain the minimum current stress, minimum conducting losses, minimum power losses, and maximum ZVS range [17], [32], [33], [47], [48].

D. Variable-Frequency Modulation Method

Moreover, besides the phase-shift modulation methods, a variable-frequency modulation technique is also a viable choice for the NSDAB dc-dc converter, especially when large power range is required [49], [50]. For the NSDAB dc-dc converter, lower switching frequency allows the transfer of higher power. Steady-state waveforms of the SPS modulation method under different switching frequencies can be shown in Fig. 11, where T_{ss} , T_{ms} , and T_{ls} represent small, medium, and large switching periods, respectively. As shown in Fig. 11, when the phase-shift ratio D is the same, high inductance current and transferred power can be achieved under large switching period [51]. A variable-frequency modulation method for the NSDAB dc-dc converter is proposed to ensure ZVS over a wide power range with lower reactive power [52]. Moreover, variable-frequency variable-phase-shift modulation strategies are proposed for an indirect matrix converter-based ac-dc battery charger with high-quality ac current [53], [54]. Therefore, if the selected switching frequency range does not affect converter filter design and components choices significantly, the variable-frequency modulation can be used to extend transferred power range of the NSDAB dc-dc converter and improve power quality in the conversion systems.

E. All Possible Phase-Shift Modulation Modes

Although the typical phase-shift modulation methods, including the SPS modulation, DPS modulation, EPS modulation, and TPS modulation methods, are discussed widely, there are some phase-shift modulation methods which may be not be analyzed in these typical phase-shift modulation methods [19], [36], [55]. Moreover, 12 kinds of phase-shift modulation conditions for the NSDAB dc-dc converter are illustrated in [34] by configuring different ranges of the phase-shift ratios. However, the ranges

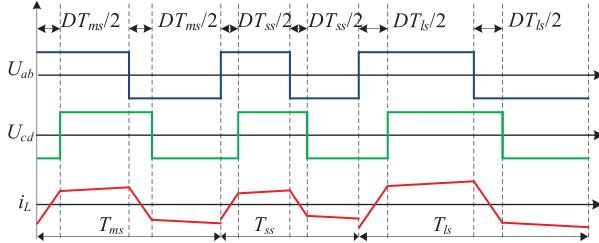


Fig. 11. Steady waveforms of the SPS modulation method under different switching frequencies.

of phase-shift ratios are not illustrated for each mode, and the reason why some phase-shift modes are not adopted for the NSDAB dc–dc converter is also not analyzed. In order to acquire a better understanding of the phase-shift modulation used for the DAB dc–dc converter, the comprehensive analysis of all possible phase-shift modulation modes for the NSDAB dc–dc converter is provided here.

For the NSDAB dc–dc converter, the principle for determining a modulation mode is that the transferred power can be obtained uniquely and expressed by the phase-shift ratios directly. Generally, there are only three possible phase-shift ratios for an NSDAB converter, including one for the input-side H bridge, one for the output-side H bridge, and one between these two H bridges. In addition, the output side and the input side of the NSDAB converter can be changed equivalently because of its symmetrical structure, and D_1 , D_2 , and D_3 can be replaced by D'_1 , D'_2 , and D'_3 , respectively. Moreover, the defined positive direction of the inductance current i_L should also be reversed. Then, 18 modulation modes for the NSDAB dc–dc converter can be drawn in Fig. 12.

As shown in Fig. 12, there are 18 basic phase-shift modulation modes for the NSDAB dc–dc converter. According to the definition of phase-shift modes, Fig. 12(a) has the same waveforms of (p), Fig. 12(b) has the same waveforms of (o), Fig. 12(g) has the same waveforms of (n), Fig. 12(h) has the same waveforms of (m), Fig. 12(i) has the same waveforms of (l), and Fig. 12(j) has the same waveforms of (k). Therefore, there are a total of 12 possible phase-shift modes for the NSDAB dc–dc converter [34]. However, phase-shift modulation modes as shown in Fig. 12(g)–(n) may not be very suitable to transfer power of the NSDAB dc–dc converter, and the reason will be analyzed as follows.

Since the NSDAB dc–dc converter is symmetrical structure, the phase-shift modulation modes based on the phase-shift ratios D_1 , D_2 , D_3 , which have the same reference S_1 , are analyzed, and the analyzed results are also suitable for the phase-shift modulation modes based on the phase-shift ratios D'_1 , D'_2 , and D'_3 . According to Fig. 10, D_1 , D_2 , and D_3 should meet the

relationship as

$$\begin{cases} 0 \leq D_1 \leq 1 \\ 0 \leq D_3 - D_2 \leq 1 \\ 0 \leq D_2 \leq 2 \\ 0 \leq D_3 \leq 2. \end{cases} \quad (1)$$

According to Fig. 12, U_{ab} and U_{cd} are symmetric three-level waveforms, and based on Fourier series, U_{ab} and U_{cd} can be expressed as [56]

$$\begin{cases} U_{ab} = \sum_{m=1,3,5...}^{\infty} \frac{4U_{in}}{m\pi} \cos\left(\pi m \frac{D_1}{2}\right) \sin(2\pi f_s mt) \\ U_{cd} = \sum_{m=1,3,5...}^{\infty} \frac{4U_o}{m\pi} \cos\left(\pi m \frac{D_3-D_2}{2}\right) \sin\left[2\pi m\left(f_s t - \frac{D_3+D_2-D_1}{4}\right)\right]. \end{cases} \quad (2)$$

Then, the transferred active P and the nonactive power Q' determined by U_{ab} and U_{cd} with the same frequency of the NSDAB dc–dc converter [57] can be shown as

$$\begin{cases} P = \sum_{m=1,3,5...}^{\infty} \frac{4U_{in}U_o \cos\left(\pi m \frac{D_1}{2}\right) \cos\left(\pi m \frac{D_3-D_2}{2}\right) \sin\left[\frac{\pi m(D_3+D_2-D_1)}{2}\right]}{n\pi^3 m^3 f_s L} \\ Q' = \sum_{m=1,3,5...}^{\infty} \frac{4U_{in}U_o \cos\left(\pi m \frac{D_1}{2}\right) \cos\left(\pi m \frac{D_3-D_2}{2}\right) \cos\left[\frac{\pi m(D_3+D_2-D_1)}{2}\right]}{n\pi^3 m^3 f_s L} \\ \quad - \frac{4U_o^2 \cos^2\left(\pi m \frac{D_3-D_2}{2}\right)}{n^2 \pi^3 m^3 f_s L}. \end{cases} \quad (3)$$

Moreover, the nonactive power Q'' generated by the different frequency voltages of the NSDAB dc–dc converter [57] can be shown as (4) shown at the bottom of this page.

According to (3) and (4), the transferred power of the NSDAB dc–dc converter is mainly formed by the first-order voltage of U_{ab} and U_{cd} because m^3 and mq^2 are the part of denominator. Then, the transferred power P and the nonactive power Q can be further expressed as

$$\begin{cases} P \approx \frac{4U_{in}U_o \cos\left(\pi \frac{D_1}{2}\right) \cos\left(\pi \frac{D_3-D_2}{2}\right) \sin\left[\frac{\pi(D_3+D_2-D_1)}{2}\right]}{n\pi^3 f_s L} \\ Q \approx \frac{4U_{in}U_o \cos\left(\pi \frac{D_1}{2}\right) \cos\left(\pi \frac{D_3-D_2}{2}\right) \cos\left[\frac{\pi(D_3+D_2-D_1)}{2}\right]}{n\pi^3 f_s L} \\ \quad - \frac{4U_o^2 \cos^2\left(\pi \frac{D_3-D_2}{2}\right)}{n^2 \pi^3 f_s L}. \end{cases} \quad (5)$$

Assuming the power is transferred from the input side to the output side, P should be positive, and the relationships of D_1 , D_2 , and D_3 can be obtained as

$$0 \leq \frac{\pi(D_3 + D_2 - D_1)}{2} = \varphi \leq \pi. \quad (6)$$

$$Q'' = \sum_{m \neq q=1,3,5...}^{\infty} \frac{4U_{ab} \cos\left(\pi m \frac{D_1}{2}\right)}{mq^2 \pi^3 f_s L} \sqrt{\left[\frac{U_{cd}}{n} \cos\left(\pi q \frac{D_3-D_2}{2}\right) \cos\left(\pi q \frac{(D_3+D_2-D_1)}{2}\right) - U_{ab} \cos\left(\pi q \frac{D_1}{2}\right) \right]^2} \\ - \left[\frac{U_{cd}}{n} \cos\left(\pi q \frac{D_3-D_2}{2}\right) \sin\left(\pi q \frac{(D_3+D_2-D_1)}{2}\right) \right]^2 \quad (4)$$

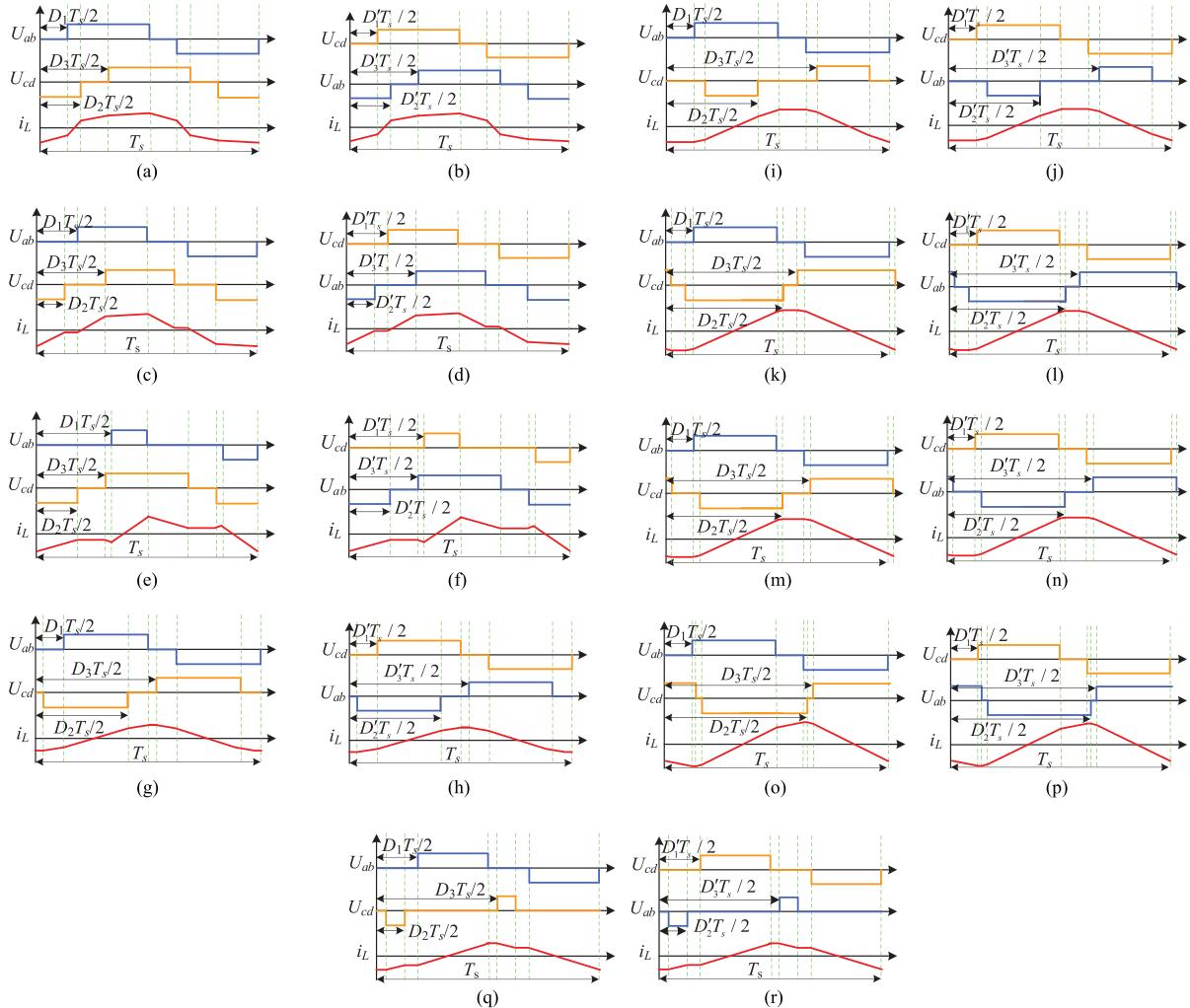


Fig. 12. 18 basic modulation methods for the NSDAB dc-dc converter. (a) $0 \leq D_1 \leq D_2 \leq D_3 \leq 1$. (b) $0 \leq D'_1 \leq D'_2 \leq D'_3 \leq 1$. (c) $0 \leq D_2 \leq D_1 \leq D_3 \leq 1$. (d) $0 \leq D'_2 \leq D'_1 \leq D'_3 \leq 1$. (e) $0 \leq D_2 \leq D_3 \leq D_1 \leq 1$. (f) $0 \leq D'_2 \leq D'_3 \leq D'_1 \leq 1$. (g) $0 \leq D_1 \leq D_2 \leq 1 \leq D_3 \leq 1 + D_1 \leq 2$. (h) $0 \leq D'_1 \leq D'_2 \leq 1 \leq D'_3 \leq 1 + D'_1 \leq 2$. (i) $0 \leq D_1 \leq D_2 \leq 1 \leq 1 + D_1 \leq D_3 \leq 2$. (j) $0 \leq D'_1 \leq D'_2 \leq 1 \leq 1 + D'_1 \leq D'_3 \leq 2$. (k) $0 \leq D_1 \leq 1 \leq D_2 \leq D_3 \leq 1 + D_1 \leq 2$. (l) $0 \leq D'_1 \leq 1 \leq D'_2 \leq D'_3 \leq 1 + D'_1 \leq 2$. (m) $0 \leq D_1 \leq 1 \leq D_2 \leq 1 + D_1 \leq D_3 \leq 2$. (n) $0 \leq D'_1 \leq 1 \leq D'_2 \leq 1 + D'_1 \leq D'_3 \leq 2$. (o) $0 \leq D_1 \leq 1 \leq 1 + D_1 \leq D_2 \leq D_3 \leq 2$. (p) $0 \leq D'_1 \leq 1 \leq 1 + D'_1 \leq D'_2 \leq D'_3 \leq 2$. (q) $0 \leq D_2 \leq D_1 \leq 1 \leq D_3 \leq 1 + D_2 \leq 2$. (r) $0 \leq D'_2 \leq D'_1 \leq 1 \leq D'_3 \leq 1 + D'_2 \leq 2$.

According to (5), when φ is from 0 to $\pi/2$, the maximum power range of the NSDAB dc-dc converter can be obtained, and when $D_1 = 0$ and $D_3 = D_2 = 0.5$, the maximum transferred power can be obtained [33]. In addition, the nonactive power Q can also be expressed as

$$Q = Q_1 - Q_2 \quad (7)$$

where Q_1 and Q_2 can be expressed as

$$\begin{cases} Q_1 = \frac{4U_{in}U_o \cos(\pi \frac{D_1}{2}) \cos(\pi \frac{D_3-D_2}{2}) \cos[\varphi]}{n\pi^3 f_s L} \\ Q_2 = \frac{4U_o^2 \cos^2(\pi \frac{D_3-D_2}{2})}{n^2 \pi^3 f_s L}. \end{cases} \quad (8)$$

Combining (1), (6), and (8), Q_2 is positive, and the sign of Q_1 is decided by the value of φ . When φ is larger than $\pi/2$, Q_1 is negative. When φ is smaller than $\pi/2$, Q_1 is positive. To avoid large Q for low-conducting losses, the signs of Q_1 and

Q_2 should be the same. Thus, φ should be smaller than $\pi/2$. Therefore, these phase-shift modes illustrated as Fig. 12(g)–(n) are usually not employed to improve the efficiency of an NSDAB dc-dc converter since φ of these phase-shift modulation methods is always larger than $\pi/2$. In addition, according to (5), D_1 and $(D_3 - D_2)$ are usually determined as 0 for high power transmission of the NSDAB dc-dc converter. However, when D_1 and $D_3 - D_2$ are close to zero in these phase-shift modulation modes, as shown in Fig. 12(g)–(n), $D_3 + D_2 - D_1$ is always close to two. As a result, P is close to zero. Thus, these phase-shift modulation modes are not very suitable for power transmission.

F. Correlation Analysis of Advanced Phase-Shift Modulation Methods

Although some advanced phase-shift modulation methods, including the EPS modulation method and the DPS modulation

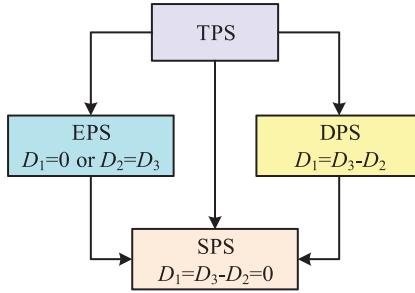


Fig. 13. Correlation diagram of typical phase-shift modulation methods.

method, are proposed first for boosting the efficiency of the NSDAB dc–dc converter, the TPS modulation method can always provide the best efficiency [33], [56], [58]. The reason may be that the EPS and DPS modulation methods can be regarded as the special cases of the TPS modulation method, which can be shown in Fig. 13.

As shown in Fig. 13, when D_1 of the TPS modulation method is equivalent to zero, or D_2 of the TPS modulation method is equivalent to D_3 , the EPS modulation method can be obtained by using the TPS modulation method. Similarly, when D_1 is equivalent to $(D_3 - D_2)$, the TPS modulation method equals the DPS modulation method. Moreover, when D_1 and the difference between D_2 and D_3 are equivalent to zero, the SPS modulation method can be acquired. Therefore, since the SPS, DPS, and EPS modulation methods are contained in the TPS modulation method, the TPS method can always provide the best efficiency for the NSDAB dc–dc converter [33], [56], [58]. Considering efficiency optimization, the recommendation for selecting phase-shift modulation modes will be given in the following section. Moreover, for the convenience of analysis in the following sections, the positions of the phase-shift ratios D_1 , D_2 , and D_3 are determined, as shown in Fig. 10. Then, based on the definition of the phase-shift ratios in the TPS modulation method, the transferred power P , the output current i_o , and the boundary inductance current i_L ($i_0, i_1, i_2, i_3, i_4, i_5, i_6$, and i_7) can be briefly expressed as [26], [30], [33], [39]

$$\begin{cases} P = \frac{U_{in}U_o}{4nf_sL} f_P(D_1, D_2, D_3) \\ i_o = \frac{P}{U_o} = \frac{U_{in}}{4nf_sL} f_P(D_1, D_2, D_3) \\ i_L = \frac{U_o}{4nf_sL} f_{iL}(D_1, D_2, D_3, k). \end{cases} \quad (9)$$

In (9), according to the general equation of P , i_o and P are ternary quadratic equations formed by D_1 , D_2 , and D_3 , and i_L is a ternary linear equation of k , D_1 , D_2 , and D_3 . These expressions can be derived from the articles of the NSDAB dc–dc converter [31], [33], [39], [48]. Finally, the simplified transferred power p , the output current i_{ou} , and the inductance current i_{lu} (i_{0u}, i_{1u} ,

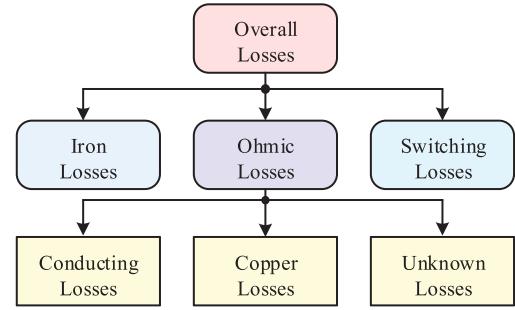


Fig. 14. Classification for the power losses of the NSDAB dc–dc converter [60].

$i_{2u}, i_{3u}, i_{4u}, i_{5u}, i_{6u}$, and i_{7u}) can be expressed as [31], [33]

$$\begin{cases} p = \frac{P}{\frac{U_{in}U_o}{8nf_sL}} = 2f_P(D_1, D_2, D_3) \\ i_{ou} = \frac{i_o}{\frac{U_{in}}{8nf_sL}} = 2f_P(D_1, D_2, D_3) \\ i_{lu} = \frac{i_L}{\frac{U_o}{8nf_sL}} = 2f_{iL}(D_1, D_2, D_3, k). \end{cases} \quad (10)$$

III. OVERVIEW OF EFFICIENCY IMPROVING SCHEMES

For the NSDAB dc–dc converter, the power losses mainly contain switching losses and conduction losses in switching devices, copper losses in transformer and auxiliary inductor, and core losses in auxiliary inductor [18], [26], [29], [59]. When wide-bandgap semiconductors, such as SiC-based switches [6], [60], [61] and GaN-based switches, are applied [53], [62], [63], the switching losses of the NSDAB dc–dc converter can be reduced significantly. In addition, the efficiency of the NSDAB dc–dc converter can also be improved by using efficiency-optimization strategies. Generally, there are five control approaches to boost the efficiency of the NSDAB dc–dc converter, including the power-loss-model-based optimization method, the nonactive power optimization technique, the inductance current optimization strategy, the ZVS range optimization scheme, and burst mode.

A. Power-Loss-Model-Based Optimization Method

Generally, the overall power losses of the NSDAB dc–dc converter can be divided into the following five power loss components: the switching losses, the conduction losses, the copper losses, the iron losses, and the other unknown losses [60], which are shown in Fig. 14. Unknown losses are mainly formed by line-resistor losses, the copper losses caused by skin and proximity effects, the ohmic losses in the dc-link capacitors, and so on. Usually, unknown losses just take up a tiny part in overall power losses. Therefore, power losses optimization strategies always focus on the iron losses, switching losses, copper losses, and conducting losses [17], [35], [59]. Moreover, the accurate-power-loss model for an NSDAB dc–dc converter can also be

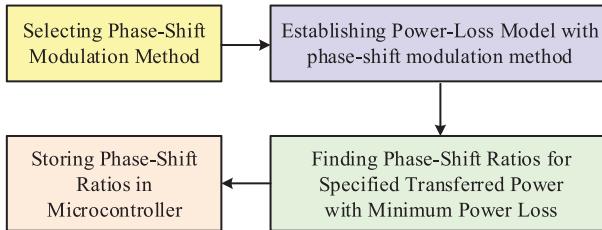


Fig. 15. Procedure for implementing the power-loss-model-based optimization scheme.

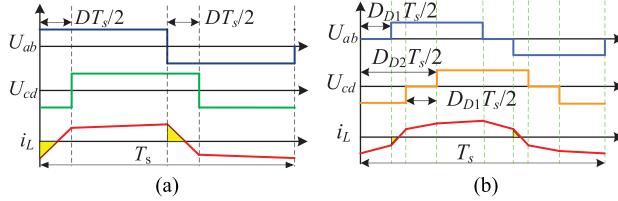


Fig. 16. Waveforms of the phase-shift modulation methods with the reactive power [30]. (a) SPS modulation. (b) DPS modulation.

acquired as shown in [18], where the accurate-power-loss model under the SPS modulation method is analyzed.

Generally, the procedure for implementing power-loss-model-based optimization strategies can be divided into four steps as shown in Fig. 15. First, the phase-shift modulation methods, such as the DPS [59], EPS [35], and TPS [17] methods, should be determined. Then, based on different power-loss elements [18], [60], the corresponding power-loss model can be obtained. Moreover, according to the certain working condition, including the input voltages, the output voltage, and the power requirement, the minimum power loss for the NSDAB dc–dc converter can be obtained by using an enumeration method of different phase-shift ratios in the mathematical software, such as MATLAB and Mathcad. Finally, the optimized phase-shift ratios for different conditions can be stored in the microcontroller or digital signal processor for practical implementation. Therefore, the calculation demand is very high especially under complicated working conditions with varied input voltage, output voltage, and transferred power, and more data should be stored in digital controllers and employed to achieve better continuous online optimization performance.

B. Nonactive Power Optimization Schemes

The original nonactive power also named as backflow power in NSDAB operation is first discussed in [30], and this backflow power may be the main factor contributing to large peak current and large system losses under the SPS modulation method. Waveforms of the SPS modulation method with backflow power can be shown in Fig. 16(a), where yellow areas of the inductance current have opposite direction to the primary-side H bridge output voltage. Therefore, to compensate this backflow power, the transferred power, which is more than the load requirement, will be generated from the input side that will affect the efficiency of an NSDAB dc–dc converter. To reduce this backflow power,

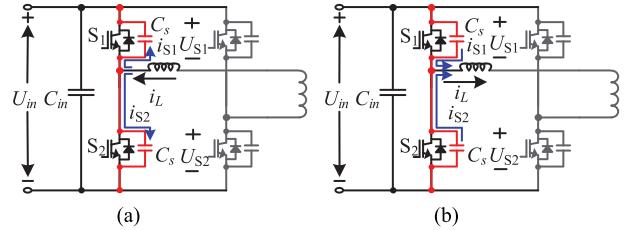


Fig. 17. ZVS performances for the NSDAB dc–dc converter. (a) ZVS for upper switch. (b) ZVS for lower switch.

some advanced phase-shift modulation methods such as the DPS modulation method [see Fig. 16(b)] can be employed, where smaller backflow power can be generated.

The backflow power characteristics in both sides of the NSDAB dc–dc converter are comprehensively analyzed under buck or boost modes [64], and a minimum-backflow-power scheme with the EPS modulation method is proposed to reduce backflow power and to improve the efficiency of this converter. In addition, according to the traditional definition of the nonactive power of ac system [65], a minimum-nonactive-power scheme is proposed to reduce the nonactive power for the NSDAB dc–dc converter on the input side with the TPS modulation method [66]. Similarly, based on an extended TPS modulation method, a minimum-nonactive-power scheme with simplified theoretical calculation and implementation difficulty is proposed to boost the efficiency for an NSDAB dc–dc converter [67]. Essentially, the nonactive power optimization strategy increases the efficiency by indirectly reducing root mean square (rms) value and average absolute value of the inductance current [66]. Therefore, the nonactive power optimization strategies can be used to boost the efficiency of an NSDAB dc–dc converter.

C. ZVS Range Optimization Strategy

The NSDAB dc–dc converter has an excellent potential for ZVS performance [68], [69], and ZVS performance can be implemented by using the parallel parasitic capacitance or by adding a parallel capacitor for each switch to reduce switching losses of switches and boost the efficiency. Usually, ZVS switching performance is achieved by charging or discharging these parallel capacitors to ensure the switches turn ON at zero voltage. Generally, there are two types of ZVS conditions, including upper switch and lower switch for the NSDAB dc–dc converter, which are shown in Fig. 17. ZVS processes of S₁ and S₂ are shown here as examples for the NSDAB dc–dc converter, and the corresponding switching signals, current, and voltage waveforms of S₁ and S₂ are illustrated in Fig. 18. As shown in Fig. 17(a), to implement ZVS for the upper switch S₁, the negative inductance current is required to charge the parallel capacitor of S₂ and discharge the parallel capacitor of S₁; and when U_{S1} becomes negative, the switch S₁ will turn ON at zero voltage, as shown in Fig. 18(a). Similarly, the positive inductance current is required to charge the parallel capacitor of S₁ and discharge the parallel capacitor of S₂ [see Fig. 17(b)], and when

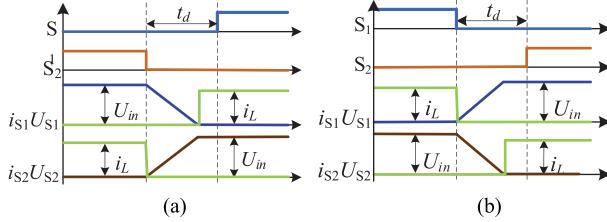


Fig. 18. Working states of S1 and S2 during ZVS performance. (a) Signals for upper-switch ZVS. (b) Signals for lower-switch ZVS.

TABLE I
REQUIREMENTS OF THE INDUCTANCE CURRENT DIRECTION FOR ZVS
PERFORMANCE OF EACH SWITCHES

Switches	Inductance-current directions
S ₁ , S ₃ , S ₆ , S ₈	Negative (i_0, i_1, i_6, i_7)
S ₂ , S ₄ , S ₅ , S ₇	Positive (i_2, i_3, i_4, i_5)

U_{S2} becomes negative, the switch S₂ will turn ON at zero voltage, as shown in Fig. 18(b).

Therefore, ZVS performances of the NSDAB dc–dc converter are determined by the direction of the inductance currents, and combining Figs. 10 and 17, the required directions of the inductance currents to implement ZVS performance of each switch are shown in Table I.

In addition, to implement ZVS performance, the inductance current should be high enough to charge the capacitors. According to previous research [66], [69], when the same value of parallel capacitors are used for each switches, the minimum absolute value of the inductance currents $i_{L_min_p}$ and $i_{L_min_s}$, which are obtained to charge the capacitors completely for primary-side switches and secondary-side switches, can be shown as

$$\begin{cases} i_{L_min_p} = 2\sqrt{\frac{U_{in}U_oC_s}{L}} \\ i_{L_min_s} = 2\sqrt{\frac{U_{in}U_oC_s}{nL}}. \end{cases} \quad (11)$$

Under the SPS modulation method, the ZVS abilities for the NSDAB dc–dc converter under different voltage conditions can be shown in Fig. 19. When both side voltages of the NSDAB dc–dc converter are matched, ZVS performances are very easy to achieve, as shown in Fig. 19(a). However, when $k > 1$, switches S₅, S₇, S₆, and S₈ of secondary-side H bridge are usually switched at non-ZVS (NZVS) conditions, as shown in Fig. 19(b), where the inductance currents i_2 and i_3 are negative. In addition, when $k < 1$, switches S₁, S₃, S₂, and S₄ of primary-side H bridge usually switches at NZVS conditions, as shown in Fig. 19(c), where the inductance currents i_0 and i_1 are positive [36], [66]. Moreover, under the SPS modulation method, ZVS performances of the NSDAB dc–dc converter under different voltage conditions can be shown in Fig. 20 clearly [36].

As shown in Fig. 20, when the voltage ratio k differs from one, the ZVS range of the NSDAB dc–dc converter will become narrower, which results in lower efficiency of the NSDAB dc–dc converter especially on light-load situations. Therefore,

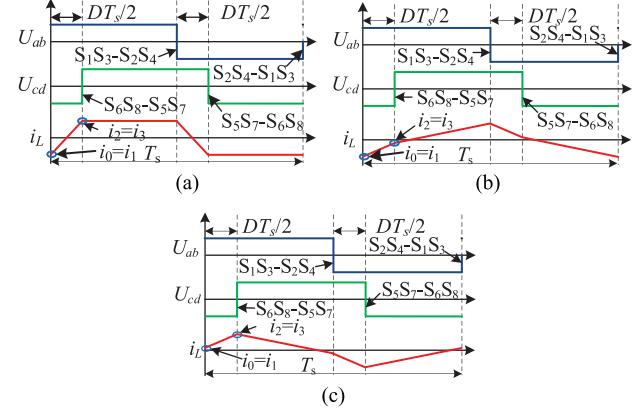


Fig. 19. ZVS abilities for the NSDAB dc–dc converter with different voltage conditions. (a) $k = 1$. (b) $k > 1$. (c) $k < 1$.

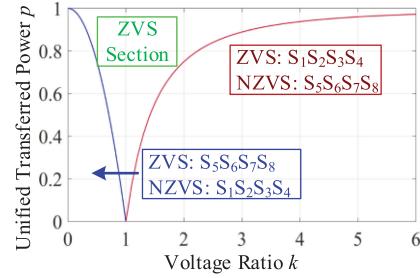


Fig. 20. ZVS conditions of the NSDAB dc–dc converter under the SPS modulation with different voltage ratios k .

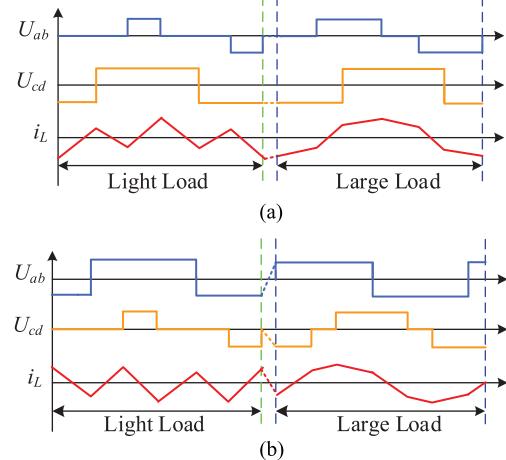


Fig. 21. Phase-shift modulations for the ZVS optimized strategy [36]. (a) Phase-shift modulation methods when $k > 1$. (b) Phase-shift modulation methods when $k < 1$.

an optimized soft-switching strategy for the entire power range is proposed to boost the efficiency of an NSDAB dc–dc converter [36] based on the phase-shift modulation methods, as shown in Fig. 21. Under light-load condition, variants of the phase-shift modulation methods, shown in Fig. 12(e) and (f), are employed to implement ZVS performances, and under heavy-load condition, the EPS modulation methods are selected to obtain ZVS

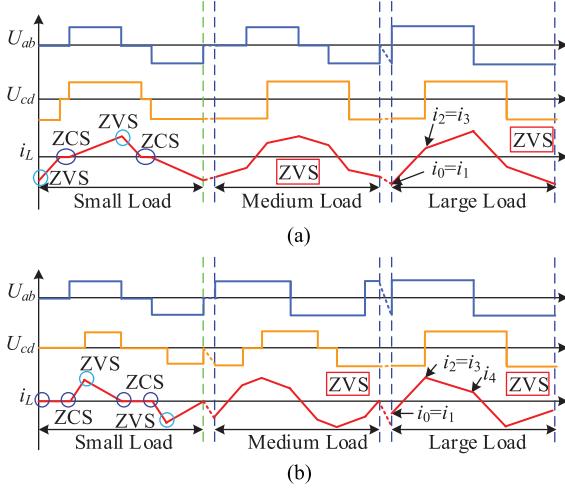


Fig. 22. Phase-shift modulation methods used in the MRMSC scheme under different voltage conditions [34], [48]. (a) Phase-shift modulation methods when $k > 1$. (b) Phase-shift modulation methods when $k < 1$.

performance and to reduce the conducting losses of the NSDAB dc–dc converter. Similarly, some other modulation methods are also proposed to achieve ZVS performance of the NSDAB dc–dc converter [70], [71], and based on these strategies, the ZVS range of the NSDAB dc–dc converter will be extended.

D. Inductance Current Optimization Strategies

Conduction losses, copper losses, and iron losses, which are the main power losses of the NSDAB dc–dc converter, can be determined by the rms or the average absolute value of the inductance current [18], [26], [29], [34], [59]. Small rms value or average absolute value of the inductance current leads to the minimum conduction and copper losses for the NSDAB dc–dc converter. In order to reduce the conduction loss of the NSDAB dc–dc converter, a closed form solution based on the minimum conduction loss modulations for low-power level, medium-power level, and high-power level is proposed to boost the efficiency of an NSDAB dc–dc converter [34]. However, this method may not be suitable in real time for the embedded controller, and a numeric table is required by offline calculation in advance. Therefore, a simple minimized rms current (MRMSC) strategy is proposed to reduce the conduction loss of the NSDAB dc–dc converter significantly [48]. The adopted phase-shift modes under the MRMSC strategy can be shown in Fig. 22. Compared with Fig. 21, under medium-load condition, the MRMSC strategy uses the same phase-shift mode as the ZVS optimized scheme, and at light-load condition, although the ZVS performance cannot be guaranteed under the MRMSC scheme, the zero-current-switching (ZCS) performance can be acquired [72].

Actually, when the input-side voltage is much higher or smaller than the output-side voltage, the waveform of the inductance current is approximately close to a triangle [33], which can be shown in Fig. 23.

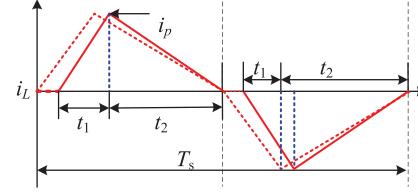


Fig. 23. Approximately equivalent inductance current when both side voltages are not matched [33].

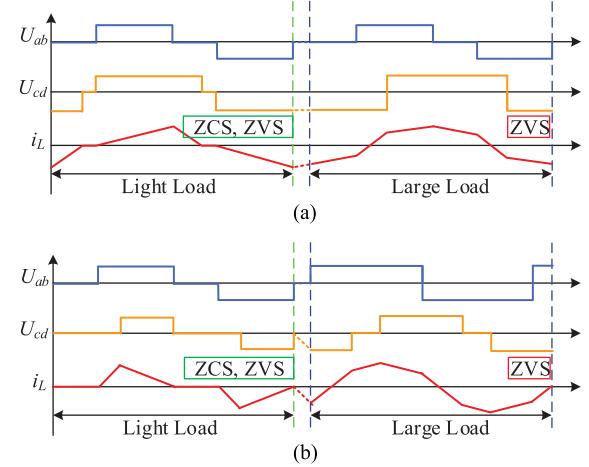


Fig. 24. Phase-shift modulation methods used in the MCSO scheme under different voltage conditions [33], [58], [74]. (a) Phase-shift modulation methods when $k > 1$. (b) Phase-shift modulation methods when $k < 1$.

Therefore, the rms value i_{LRMS} and the average absolute value $|i_L|_{avg}$ of the inductance current can be calculated as

$$\begin{cases} |i_L|_{avg} \approx \frac{(t_1 + t_2)}{2T_s} i_p \\ i_{LRMS} \approx \sqrt{\frac{2(t_1 + t_2)}{3T_s}} i_p \end{cases} \quad (12)$$

where t_1 is the time during increasing of the inductance current and t_2 is the time during decreasing of the inductance current. When large transferred power is required, the sum of t_1 and t_2 is always equivalent to a half of switching period T_s . According to (12), the rms value and average value can be reduced by decreasing the peak-current of the inductance current [33], [56], [58], [73]. Therefore, to boost the efficiency of an NSDAB dc–dc converter, current-stress-optimized (CSO) strategies with the EPS and DPS modulation schemes are proposed in [31] and [73]. Furthermore, based on the TPS modulation method, minimum CSO (MCSO) strategies are proposed to boost the efficiency of an NSDAB dc–dc converter with simple operations [33], [58], [74], and the adopted phase-shift modes can be shown in Fig. 24, where both ZCS and ZVS performance can be guaranteed [58]. Comparing Figs. 22 and 24, when very large transferred power is required, the MRMSC strategy prefers to employ the SPS modulation method, and when the NSDAB dc–dc converter is on light-load or medium-load conditions, the MRMSC and MCSO strategies choose the same phase-shift modes.

TABLE II
COMPARISON OF DIFFERENT EFFICIENCY IMPROVING METHOD

Schemes	Disadvantages	Advantages
Power-loss-model-based optimization method [17, 35, 59]	1. The on-line continues optimizing performance cannot be obtained. 2. The optimizing procedure for a certain condition is complicated. 3. The portability is poor.	With accurate power loss model, the optimized phase-shift ratio for the certain working condition may be obtained for maximum efficiency.
Nonactive power optimization methods [30, 64, 67]	1. The operation is complicated. 2. The off-line calculation may be required for obtaining minimum nonactive power.	The minimum backflow power and nonactive power can be obtained.
ZVS range optimization scheme [36, 75]	1. The optimizing procedure is complicated. 2. The boundary of ZVS performance is complicated to be obtained. 3. The off-line calculation are required.	The ZVS performance of each switch can be guaranteed.
Inductance current optimizing technique [33, 34, 48, 58, 73, 74]	The ZVS performance cannot be guaranteed for each switch at light load.	1. The optimizing operation is simple. 2. The optimizing procedure is simple. 3. The on-line continuous control can be implemented. 4. The ZCS performance can be acquired at light-load condition.

E. Comparison of Efficiency Improving Strategies

When both side voltages are matched, the SPS modulation method will be the best choice for the NSDAB dc–dc converter [31], [33], [48], [58], [73], [74]. However, when the input side and output side voltages are mismatched, there are four approaches to boost the efficiency of an NSDAB dc–dc converter, including the power-loss-model-based optimization schemes [17], [35], [59], nonactive power optimization methods [30], [64], [67], ZVS range optimization strategies [36], [75], and inductance current optimization techniques [33], [34], [48], [58], [74]. The advantages and disadvantages of each efficiency-improving scheme are summarized in Table II.

From Table II, the existing power-loss-model-based optimization methods [17], [35], [59] and the ZVS range optimization scheme [36], [75] maybe not suitable for online optimization [33], [35], [48], [59], since offline calculations are necessary and the implementation is complicated. Moreover, the ZVS soft-switching boundary for the NSDAB dc–dc converter is also a little difficult to be determined, when the minimum inductance current for charging the parallel capacitor of switches is considered [70]. In addition, the nonactive power optimization strategies boost the efficiency by indirectly reducing the rms inductance current [66] because the nonactive power can be calculated as the integral of the output voltage of H bridge and the inductance current. Since the minimum rms inductance current can be achieved directly [34], [48], these nonactive power optimization strategies are considered separately for comparisons here.

The inductance current is always flowing though the transformer, the inductance, and the four switches, which is where the power loss is mainly generated. Thus, it may be more effective to reduce the inductance current directly for boosting the efficiency of an NSDAB dc–dc converter. Moreover, the inductance current optimizing strategies can be implemented in the microcontroller or digital signal processor easily. Therefore, the inductance current optimization technique is recommended to reduce the

power loss and to improve the efficiency for an NSDAB dc–dc converter, and this is also the most popular method for boosting the efficiency of an NSDAB dc–dc converter [31], [33], [34], [40], [48], [58], [73], [74]. Generally, the inductance current optimization technique is divided into the rms current optimization scheme [34], [48] and the CSO strategy [31], [33], [73], [74]. As analyzed in Section II-F, the SPS, DPS, and EPS modulation methods can be regarded as a special case of the TPS modulation method, so the TPS modulation method can always provide the best efficiency for an NSDAB dc–dc converter [33], [56], [58]. Therefore, based on the TPS modulation method, the MRMSC [34], [48] strategy and the MCSO [33], [58], [74] scheme will be compared in detail.

As shown in Figs. 22 and 24, the MRMSC scheme and the MCSO strategy use the same phase-shift modes from light-load condition to medium-load condition. Moreover, when the transferred power is close to the maximum transferred power of the NSDAB dc–dc converter, the EPS modulation method is still employed under the MCSO strategy, but the SPS modulation method is adopted under the MRMSC scheme. In addition, the optimized solutions, which are based on the phase-shift-ratio positions in Fig. 10, of the MRMSC [34], [48] strategy and the MCSO [33], [58], [74] can be given in Tables III and IV, respectively. However, under the MRMSC scheme, D_1 , D_2 , and D_3 cannot be calculated by p directly for medium-load condition since the relationship among the phase-shift ratios D_1 , D_2 , and D_3 is nonlinear [34], [48]. Comparing Tables III and IV, these two optimization strategies have the same phase-shift ratios D_1 , D_2 , and D_3 during small-load condition. Under higher load conditions, although the EPS modulation methods are used in both the MCSO strategy and the MRMSC strategy, optimized solutions of D_1 , D_2 , and D_3 are different. Moreover, the waveforms of the phase-shift ratios D_1 , D_2 , and D_3 versus p under different strategies with different k can be shown in Fig. 25, and the phase-shift ratio D under the SPS modulation method is also presented.

TABLE III
OPTIMIZED SOLUTIONS OF THE MRMSC STRATEGY UNDER DIFFERENT CONDITIONS [48]

Voltage Conditions	Range of p	Middle Variable	Phase-Shift Ratio
$k > 1$	$0 \leq p < 2\frac{k-1}{k^2}$	$D_1 = 1 - \sqrt{\frac{p}{2(k-1)}}$	$\begin{cases} D_2 = (k-1)(1-D_1) \\ D_3 = D_1 \end{cases}$
	$2\frac{k-1}{k^2} \leq p < 2(1-k^2+k\sqrt{k^2-1})$	Hard to Obtain	$\begin{cases} D_2 = \frac{kD_1-k+1+D_1+\sqrt{k^2(D_1-1)^2+(D_1^2-1)}}{2} \\ D_3 = \frac{kD_1-k+1+D_1+\sqrt{k^2(D_1-1)^2+(D_1^2-1)}}{2} \end{cases}$
	$2(1-k^2+k\sqrt{k^2-1}) \leq p \leq 1$	$D_2 = \frac{1}{2} - \sqrt{\frac{1-p}{4}}$	$\begin{cases} D_1 = 0 \\ D_3 = D_2 \end{cases}$
$k \leq 1$	$0 \leq p < 2(k-k^2)$	$D_1 = 1 - \sqrt{\frac{p}{2k(1-k)}}$	$\begin{cases} D_2 = 0 \\ D_3 = kD_1 - k + 1 \end{cases}$
	$2(k-k^2) \leq p < 2(\frac{k^2-1+\sqrt{1-k^2}}{k^2})$	Hard to Obtain	$\begin{cases} D_1 = 0 \\ D_3 = 1+kD_2 - \frac{k}{2} - \sqrt{k^2D_2^2 - k^2D_2 + \frac{k^2}{4} + kD_2 + D_2^2} \end{cases}$
	$2(\frac{k^2-1+\sqrt{1-k^2}}{k^2}) \leq p \leq 1$	$D_2 = \frac{1}{2} - \sqrt{\frac{1-p}{4}}$	$\begin{cases} D_1 = 0 \\ D_3 = D_2 \end{cases}$

TABLE IV
OPTIMIZED SOLUTIONS OF THE MCSO STRATEGY UNDER DIFFERENT CONDITIONS [33], [58], [74]

Voltage Conditions	Range of p	Middle Variable	Phase-Shift Ratio
$k > 1$	$0 \leq p < 2\frac{k-1}{k^2}$	$D_1 = 1 - \sqrt{\frac{p}{2(k-1)}}$	$\begin{cases} D_2 = (k-1)(1-D_1) \\ D_3 = D_1 \end{cases}$
	$2\frac{k-1}{k^2} \leq p \leq 1$	$D_1 = (k-1)\sqrt{\frac{1-p}{k^2-2k+2}}$	$\begin{cases} D_2 = \frac{k-2}{2(k-1)}D_1 + \frac{1}{2} \\ D_3 = \frac{k-2}{2(k-1)}D_1 + \frac{1}{2} \end{cases}$
$k \leq 1$	$0 \leq p < 2(k-k^2)$	$D_1 = 1 - \sqrt{\frac{p}{2k(1-k)}}$	$\begin{cases} D_2 = 0 \\ D_3 = kD_1 - k + 1 \end{cases}$
	$2(k-k^2) \leq p \leq 1$	$D_2 = \frac{1}{2}(1 - \sqrt{\frac{1-p}{2k^2-2k+1}})$	$\begin{cases} D_1 = 0 \\ D_3 = 2kD_2 - D_2 - k + 1 \end{cases}$

As shown in Fig. 25, when k is close to one, the phase-shift ratios D_2 and D_3 of the MRMSC strategy and the MCSO strategy are similar to the phase-shift ratio D of the SPS modulation method because the SPS modulation method is the best choice under matching side voltages for the NSDAB dc–dc converter. Moreover, in the heavy-load situation, the SPS modulation method is selected in the MRMSC scheme. It is worth mentioning that the optimized solutions of D_1 , D_2 , and D_3 under the MCSO strategy [33], [58], [74] and the MRMSC strategy [34], [48] are very close, and gradually become closer with the increase of k when $k > 1$ and the decrease of k when $k < 1$.

In addition, according to Fig. 10 and (10), the simplified boundary inductance current i_{0u} , i_{1u} , i_{2u} , i_{3u} , and i_{4u} and the simplified rms inductance current can be shown in Tables V

and Table VI. Then, the simplified rms current of the NSDAB dc–dc converter under the SPS modulation method, the MRMSC strategy, and the MCSO scheme can be shown in Fig. 26. Compared to the SPS modulation method, the MRMSC scheme and the MCSO scheme can reduce the rms value of the inductance current for the NSDAB dc–dc converter, especially when k is further away from one. Moreover, the MCSO scheme can achieve very similar performances as the MRMSC strategy, and when p is close to one, the MRMSC strategy can achieve a slightly better performance than the MCSO strategy to reduce the rms value of the inductance current.

Therefore, compared to the MRMSC strategy, the MCSO strategy with simpler operations can achieve very similar performance in terms of reducing the rms inductance current of the

TABLE V
SIMPLIFIED RMS INDUCTANCE CURRENT OF THE MRMSC STRATEGY UNDER DIFFERENT CONDITIONS [48]

Voltage Ratio	Range of p	Simplified Inductance Currents	Simplified RMS Inductance Current
$k > 1$	$0 \leq p < 2\frac{k-1}{k^2}$	$\begin{cases} i_{0u} = -4D_2 \\ i_{1u} = i_{2u} = i_{3u} = 0 \\ i_{4u} = 4D_2 \end{cases}$	$\sqrt{\frac{D_2}{3} i_{0u}^2 + \frac{1-D_3}{3} i_{4u}^2}$
	$2\frac{k-1}{k^2} \leq p < 2(1-k^2+k\sqrt{k^2-1})$	$\begin{cases} i_{0u} = 2(1-k+kD_1-2D_2) \\ i_{1u} = 2(1-k+kD_1+2D_1-2D_2) \\ i_{2u} = i_3 = 2(1-k-kD_1+2kD_2) \\ i_{4u} = 2(k-1-kD_1+2D_2) \end{cases}$	$\sqrt{\frac{D_1}{3} (i_{0u}^2 + i_{0u}i_{1u} + i_{1u}^2) + \frac{D_2-D_1}{3} (i_{1u}^2 + i_{1u}i_{2u} + i_{2u}^2) + \frac{1-D_2}{3} (i_{2u}^2 + i_{2u}i_{4u} + i_{4u}^2)}$
	$2(1-k^2+k\sqrt{k^2-1}) \leq p \leq 1$	$\begin{cases} i_{0u} = i_{1u} = 2(1-2D_2-k) \\ i_{2u} = i_{3u} = 2(1-k+2kD_2) \\ i_{4u} = 2(k-1+2D_2) \end{cases}$	$\sqrt{\frac{D_2}{3} (i_{0u}^2 + i_{0u}i_{2u} + i_{2u}^2) + \frac{1-D_2}{3} (i_{2u}^2 + i_{2u}i_{4u} + i_{4u}^2)}$
$k \leq 1$	$0 \leq p < 2(k-k^2)$	$\begin{cases} i_{0u} = i_{1u} = i_{2u} = 0 \\ i_{3u} = 4k(D_3-D_1) \\ i_{4u} = 0 \end{cases}$	$\sqrt{\frac{D_3-D_2}{3} i_{3u}^2 + \frac{1-D_3}{3} i_{4u}^2}$
	$2(k-k^2) \leq p < 2(\frac{k^2-1+\sqrt{1-k^2}}{k^2})$	$\begin{cases} i_{0u} = i_{1u} = 2(1-k-D_2-D_3) \\ i_{2u} = 2(1-k+D_2-D_3+2kD_2) \\ i_{3u} = 2(1-k+D_2-D_3+2kD_3) \\ i_{4u} = 2(k-1+D_2+D_3) \end{cases}$	$\sqrt{\frac{D_2}{3} (i_{0u}^2 + i_{0u}i_{2u} + i_{2u}^2) + \frac{D_3-D_2}{3} (i_{2u}^2 + i_{2u}i_{3u} + i_{3u}^2) + \frac{1-D_3}{3} (i_{3u}^2 + i_{3u}i_{4u} + i_{4u}^2)}$
	$2(\frac{k^2-1+\sqrt{1-k^2}}{k^2}) \leq p \leq 1$	$\begin{cases} i_{0u} = i_{1u} = 2(1-2D_2-k) \\ i_{2u} = i_{3u} = 2(1-k+2kD_2) \\ i_{4u} = 2(k-1+2D_2) \end{cases}$	$\sqrt{\frac{D_2}{3} (i_{0u}^2 + i_{0u}i_{2u} + i_{2u}^2) + \frac{1-D_2}{3} (i_{2u}^2 + i_{2u}i_{4u} + i_{4u}^2)}$

TABLE VI
SIMPLIFIED RMS INDUCTANCE CURRENT OF THE MCSO STRATEGY UNDER DIFFERENT CONDITIONS [33], [58], [74]

Voltage Conditions	Range of p	Simplified Inductance Currents	Simplified RMS Inductance Current
$k > 1$	$0 \leq p < 2\frac{k-1}{k^2}$	$\begin{cases} i_{0u} = -4D_2 \\ i_{1u} = i_{2u} = i_{3u} = 0 \\ i_{4u} = 4D_2 \end{cases}$	$\sqrt{\frac{D_2}{3} i_{0u}^2 + \frac{1-D_3}{3} i_{4u}^2}$
	$2\frac{k-1}{k^2} \leq p \leq 1$	$\begin{cases} i_{0u} = 2(1-k+kD_1-2D_2) \\ i_{1u} = 2(1-k+kD_1+2D_1-2D_2) \\ i_{2u} = i_3 = 2(1-k-kD_1+2kD_2) \\ i_{4u} = 2(k-1-kD_1+2D_2) \end{cases}$	$\sqrt{\frac{D_1}{3} (i_{0u}^2 + i_{0u}i_{1u} + i_{1u}^2) + \frac{D_2-D_1}{3} (i_{1u}^2 + i_{1u}i_{2u} + i_{2u}^2) + \frac{1-D_2}{3} (i_{2u}^2 + i_{2u}i_{4u} + i_{4u}^2)}$
$k \leq 1$	$0 \leq p < 2(k-k^2)$	$\begin{cases} i_{0u} = i_1 = i_2 = 0 \\ i_{3u} = 4k(D_3-D_1) \\ i_{4u} = 0 \end{cases}$	$\sqrt{\frac{D_3-D_2}{3} i_{3u}^2 + \frac{1-D_3}{3} i_{4u}^2}$
	$2(k-k^2) \leq p \leq 1$	$\begin{cases} i_{0u} = i_{1u} = 2(1-k-D_2-D_3) \\ i_{2u} = 2(1-k+D_2-D_3+2kD_2) \\ i_{3u} = 2(1-k+D_2-D_3+2kD_3) \\ i_{4u} = 2(k-1+D_2+D_3) \end{cases}$	$\sqrt{\frac{D_2}{3} (i_{0u}^2 + i_{0u}i_{2u} + i_{2u}^2) + \frac{D_3-D_2}{3} (i_{2u}^2 + i_{2u}i_{3u} + i_{3u}^2) + \frac{1-D_3}{3} (i_{3u}^2 + i_{3u}i_{4u} + i_{4u}^2)}$

NSDAB dc–dc converter. Moreover, the relationship among the phase-shift ratios and load conditions can be obtained clearly, which makes it very convenient when combining with other control methods. Therefore, this MCSO strategy is recommended in [33], [58], and [74], and the optimized solutions can be obtained from Table IV.

Furthermore, burst-mode operation for power converters is a very effective approach to boost the efficiency of converters

at extremely light load [76]–[78], which is beneficial to reduce the switching losses by reducing unnecessary switching actions and by guaranteeing enough current for ZVS performance. Therefore, an advanced switching sequence and the burst-mode strategy, as shown in Fig. 27, are proposed to balance the conduction, switching, and magnetic losses under light-, medium-, and heavy-loading conditions improving the operating efficiency of an NSDAB dc–dc converter [79].

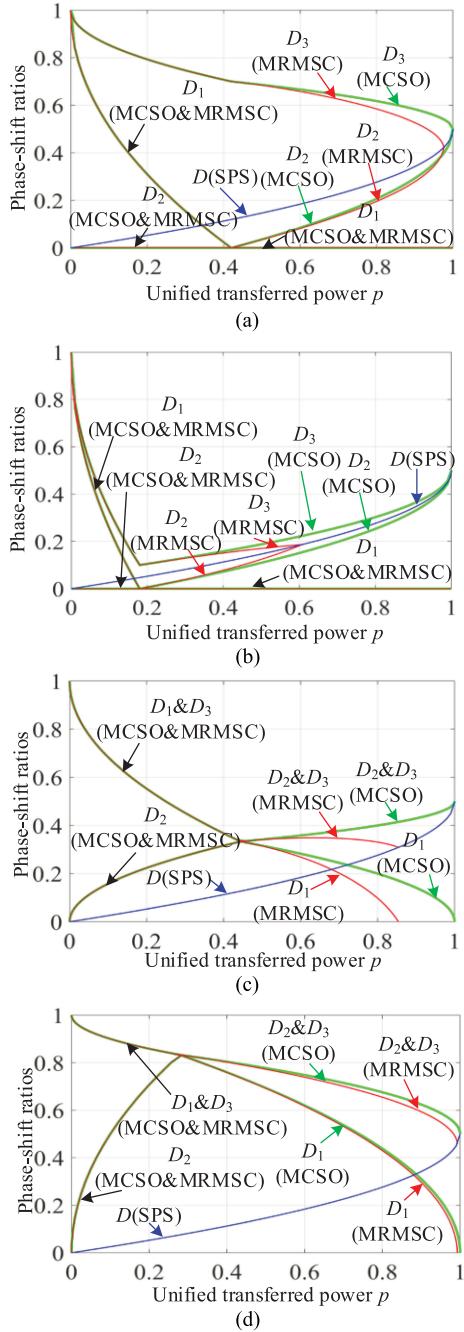


Fig. 25. Phase-shift ratios versus p under different modulation methods with different k . (a) $k = 0.3$. (b) $k = 0.9$. (c) $k = 1.5$. (d) $k = 6$.

As shown in Fig. 27, under light-load condition, the burst-model switching sequence is used to reduce the switching losses of the NSDAB dc–dc converter. The EPS modulation method is used under medium-load conditions for achieving ZVS performances and reducing the conducting losses [36], and the switching frequency is increased inversely with the output current. Moreover, SPS control is used to improve the efficiency of an NSDAB dc–dc converter when the output power is high because the ZVS operating mode is ensured and maximum power transferring ability can be obtained. Therefore, when the

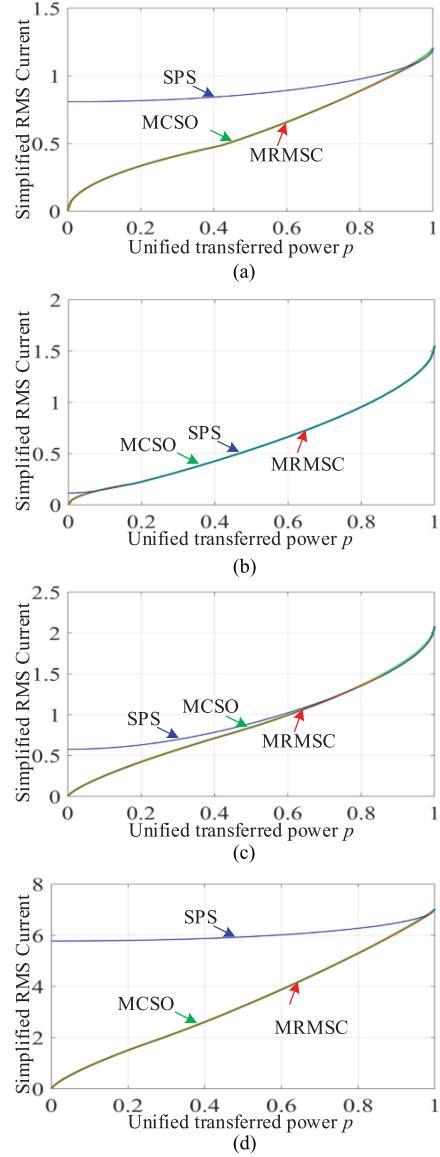


Fig. 26. Simplified rms current in respect of p under different modulation methods with different k . (a) $k = 0.3$. (b) $k = 0.9$. (c) $k = 1.5$. (d) $k = 6$.

NSDAB dc–dc converter works on extremely light load, the burst concept [79] can be combined with the MCSO strategy to reduce gate driver losses for higher efficiency.

IV. OVERVIEW OF DYNAMIC-OPTIMIZATION STRATEGIES

For DAB converter dynamic control [80]–[82], utilize advanced mathematic methods, such as the small-signal modeling and the discrete-time average modeling methods, to describe the dynamic characteristics of the DAB dc–dc converters. Generally, there are three techniques to enhance dynamic performances of the NSDAB dc–dc converter, including the load-current feedforward scheme [83], [84], the direct-inductance-current control strategy [85], [86], and the power-based control methods [87], [88].

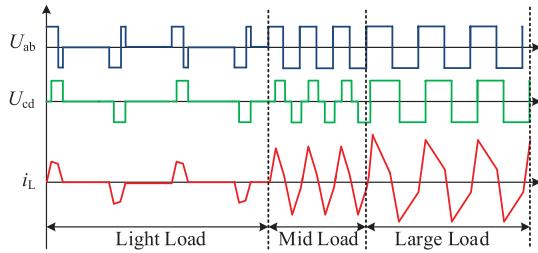


Fig. 27. Waveforms of the advanced switching sequence and burst-mode strategy [79].

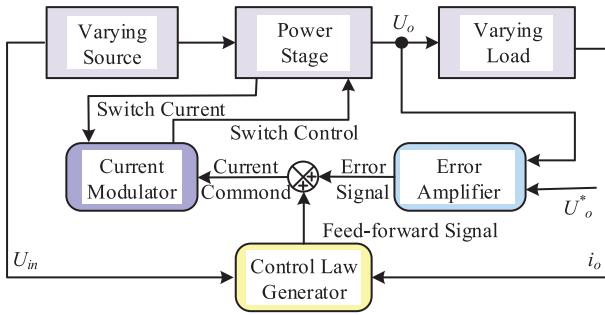


Fig. 28. Block schematic of the current-mode-controlled power converter with feedforward of the input voltage and the output current [89].

A. Load-Current Feedforward Scheme

In order to boost the dynamic responses of the power converters, the feedforward concept of the input voltage and the output current has become a popular choice [89]–[91], because the input voltage and the output current contains the major disturbances which influence the converter dynamics. A block schematic of the general current-mode-controlled power converter with feedforward of the input voltage and the output current is shown in Fig. 28. The input voltage \$U_{in}\$ and the output current \$i_o\$ of power converter can be measured to calculate the feedforward signal by the control law generator that always contains the relationship among the input voltage, the output current, and the switch current, and then by adding the compensation of error amplifier for the desired output voltage, the corresponding switch control of power stage can be implemented to obtain the required output voltage.

Based on this feedforward concept, a feedforward compensation strategy with load current (FCSLC) is proposed to improve the output transient response of the NSDAB dc–dc converter under the load disturbance condition [83], and the control block can be shown in Fig. 29, where the inner current modulator is eliminated.

As shown in Fig. 29, the output current \$i_o\$ is used to directly calculate the phase-shift ratio \$\Delta D\$ [83], and the relationship of \$i_o\$ and \$\Delta D\$ can be expressed as

$$i_o = \frac{16}{\pi^2} U_{in} \left/ n \sum_{j=0}^{\infty} \left(\frac{\sin[2j+1]\Delta D}{[2j+1]^3 \omega_s L} \right) \right. \quad (13)$$

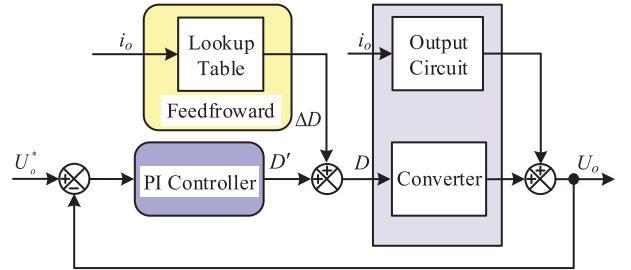


Fig. 29. Block diagram of FCSLC for the NSDAB dc–dc converter [83].

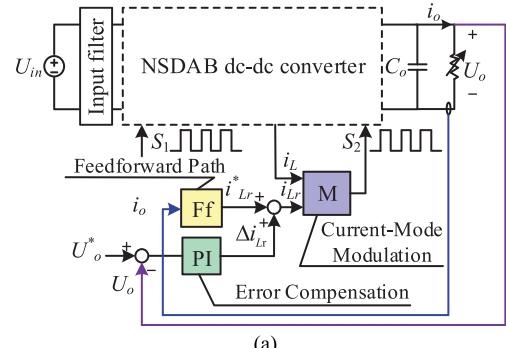


Fig. 30. Block diagram of SLFC for the NSDAB dc–dc converter [84]. (a) Block diagram with the resistive load. (b) Block diagram with the dc voltage bus.

where \$i_o\$ is calculated by each significant harmonic [92], and \$\omega_s = 2\pi f_s\$. According to (13), it is very hard to calculate \$\Delta D\$ online by using microprocessors such as DSP. So, this value needs to be precalculated in a lookup table based on the required \$i_o\$ and the input voltage \$U_{in}\$. Similarly, a simplified load-feedforward control (SLFC) with the current-mode modulation is proposed to improve the dynamic performances of the NSDAB dc–dc converter by establishing the relationship between the load current and the inductance current [84], and the diagram of this strategy is illustrated in Fig. 30 with different load conditions including the resistive load and dc voltage bus.

As shown in Fig. 30(a) and (b), PI controller is used to compensate errors between the converter model and actual converter. Moreover, the current-mode modulator can be used to generate signals to control the switches \$S_5\$, \$S_6\$, \$S_7\$, and \$S_8\$. As shown in Fig. 30(a), when the NSDAB dc–dc converter is connected

to a resistive load, the output voltage becomes the demanded requirement. Then, based on the SPS modulation, i_{Lr}^* can be calculated as

$$i_{Lr}^* = \frac{2ni_o}{1 + \sqrt{1 - \frac{8ni_o L f_s}{U_{in}}}}. \quad (14)$$

Similarly, as shown in Fig. 30(b), when the NSDAB dc–dc converter is connected to the dc voltage bus, i_{Lr}^* can be calculated as

$$i_{Lr}^* = \frac{2ni_o}{1 + \sqrt{1 - \frac{8ni_o^* L f_s}{U_{in}}}}. \quad (15)$$

Different from the resistive load, the output current becomes the demanded requirement. Based on the proposed SLFC [84], the dynamic performances of the NSDAB dc–dc converter can be enhanced significantly.

B. Direct-Inductance-Current Control Strategy

Direct-inductance-current control strategies have become very popular to improve the dynamic performances of buck and boost converters [93], [94]. Similarly, some peak, valley, and even average current-mode controls are proposed to improve the dynamic responses of the NSDAB dc–dc converter [86], [95], [96]. Based on the peak–valley inductance current control technique, a fast transient boundary control (FTBC) for the NSDAB dc–dc converter using the natural switching surface of the inductance current is proposed to boost the dynamic performances [85], and excellent dynamic behaviors can be achieved, such as no overshoot, fast transient response for start-up and load disturbances, and reaching steady state within a few switching actions. However, this strategy needs five sensors to measure the input voltage, primary-side inductance current, secondary-side inductance current, output voltage, and output current. Moreover, by setting the switching signals independently, a novel modulation method is proposed to control the peak and valley inductance current of the NSDAB dc–dc converter to avoid magnetic-flux saturation of the transformer [97]. However, since dynamic responses of this method are reliant on the outer voltage loop, dynamic performances of the NSDAB dc–dc converter are not improved.

Notably, the direct-inductance-current control concept is more suitable for controlling the transferred power by using some novel modulation methods during the dynamic processes between two dc voltage sources [86], [98], [99], and the principle of these modulation methods is to build desired boundary inductance currents in a switching period. An asymmetric double-side modulation (ADSM) method is proposed for fast transient responses of the NSDAB dc–dc converter connected with two dc sources [98], and the diagram of this modulation method showing the increasing phase-shift ratio is presented in Fig. 31.

As shown in Fig. 31, D' is the required phase-shift ratio, d is the added phase-shift ratio, and x is the optimized coefficient,

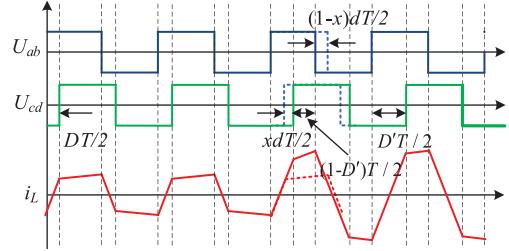


Fig. 31. Block diagram of ADSM for the NSDAB dc–dc converter [98].

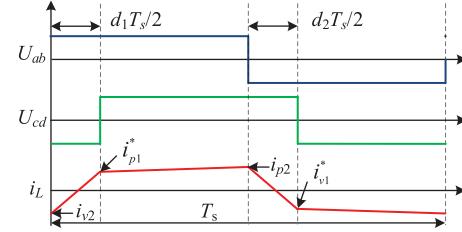


Fig. 32. Duty cycle modulation for voltage-second performance of the NSDAB dc–dc converter [99].

and D' and x can be expressed as

$$\begin{cases} D' = D + d \\ x = \frac{nU_{in}}{nU_{in} + U_o} \end{cases} \quad (16)$$

Similarly, a predictive current-mode control (PCMC) is proposed to enable the NSDAB dc–dc converter to track the current reference within one switching cycle [99]. To reduce the dc offset of the inductance current, a novel modulation method is presented in this paper, and the diagram of this method is shown in Fig. 32. i_{v2} and i_{p2} are measured for each switching period, and i_{p1}^* and i_{v1}^* are the desired value of the inductance current. d_1 and d_2 can be calculated as

$$\begin{cases} d_1 = \frac{2L(i_{p1}^* - i_{v2})}{(U_{in} + U_o/n)T} \\ d_2 = \frac{2L(i_{v1}^* - i_{p2})}{-(U_{in} + U_o/n)T} \end{cases} \quad (17)$$

Obviously, when the NSDAB dc–dc converter reaches steady state, $i_{v2} = -i_{p2}$ and $d_1 = d_2$. Therefore, the desired inductance current can be obtained, and the voltage-second performance can also be achieved. Compared to ADSM [98], the sampling frequency of this duty cycle modulation has to be doubled at the same switching frequency since there are now two desired inductance current values.

C. Power-Based Control Methods

It is well known that direct power control is an efficient strategy to improve the dynamic response of the power converters where fluctuations in the input voltage or the load exist. Direct power control has also been widely applied and reported for the front-active rectifiers and grid-side inverters in renewable

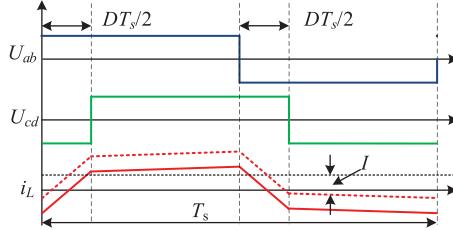


Fig. 33. SPS modulation method with dc bias I of the inductance current.

generation system [100]–[102]. Similarly, power-control concept has been introduced to boost the dynamic of the NSDAB dc–dc converter [87], [88], [103]. Actually, direct power control is very suitable for the NSDAB dc–dc converter, since the initial inductance current does not affect the transmission of power and the transferred power can be obtained in each switching period [104]. The main characteristics waveforms of the SPS modulation method with dc bias I of the inductance current can be shown in Fig. 33.

With dc bias of the inductance current, the transferred power of the NSDAB dc–dc converter under the SPS modulation method can be expressed as

$$\begin{aligned} P &= \frac{1}{T_s} \int_0^{T_s} U_{ab}(t)(i'_L(t) + I)dt \\ &= \frac{1}{T_s} \int_0^{T_s} U_{ab}(t)i'_L(t) + U_{ab}(t)Idt \end{aligned} \quad (18)$$

where $i'_L(t)$ represents the ac component of the inductor current i_L , and I is the dc component of the current i_L . Because the wave shape of the output voltage of H_1 bridge $U_{ab}(t)$ is the symmetrical square-wave during positive and negative half period, and the absolute value of $U_{ab}(t)$ equals the input voltage U_{in} . Therefore, the integral value of component $U_{ab}(t)I$ in the right side of (18) is zero, and the transferred power P is relative to U_{in} , U_o , and D , shown as

$$P = \frac{U_{in}U_oD(1-D)T_s}{2nL}. \quad (19)$$

Similarly, the transferred power of the NSDAB dc–dc converter under other phase-shift modulation methods, such as the DPS, EPS and TPS modulation methods can also be determined by the input voltage, output voltage, and phase-shift ratios. Based on this characteristic, a virtual-direct-power control (VDPC) scheme is proposed to boost the dynamic responses of the NSDAB dc–dc converter [104], and a block diagram of the VDPC strategy is shown in Fig. 34.

As shown in Fig. 34, U_v^* is the virtual desired output voltage with PI compensation to represent the desired output voltage in the control system, and the desired phase-shift ratio D^* can be calculated as

$$D^* = \begin{cases} \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{U_o^*U_v^*i_o}{U_o^2U_{in}}}, & (i_o \geq 0) \\ -\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{U_o^*U_v^*i_o}{U_o^2U_{in}}}, & (i_o < 0). \end{cases} \quad (20)$$

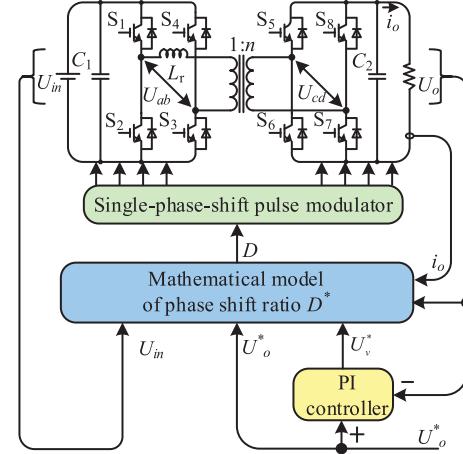


Fig. 34. Block diagram of the VDPC scheme for the NSDAB dc–dc converter [104].

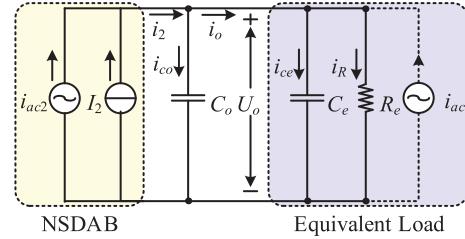


Fig. 35. Simplified output side equivalent circuit of the NSDAB dc–dc converter connected with other converters.

Based on this VDPC scheme, excellent dynamic behaviors can be obtained when the load or the input voltage are suddenly changed. However, it is difficult to measure the load current of the NSDAB dc–dc converter accurately in a switching period in some applications, especially when the NSDAB dc–dc converter is connected with other converters with output capacitors. The simplified output side equivalent circuit of the NSDAB dc–dc converter can be shown in Fig. 35.

In Fig. 35, i_{co} and i_{ce} are the charging currents of the output capacitor C_o and the equivalent load capacitor C_e , respectively, R_e is the equivalent load and i_{ac} is the equivalent ac current caused by other converters. Assuming U_o is unchanged, i_2 can be expressed in (13) as the sum of dc component I_2 and ac component i_{ac2}

$$i_2 = I_2 + i_{ac2} = i_R + i_{ac2}. \quad (21)$$

Then, i_o can be expressed as

$$i_o = i_R + \frac{C_e}{C_o + C_e}(i_{ac2} + i_{ac}). \quad (22)$$

According to (22), it is difficult to measure i_o in a switching period accurately since i_{ac2} , i_{ac} , and C_e may be unknown for the controlling system of the NSDAB dc–dc converter. Therefore, some advanced measuring techniques based on average value circuits and high-frequency acquisition methods should be employed to determine the dc component of i_o . In addition,

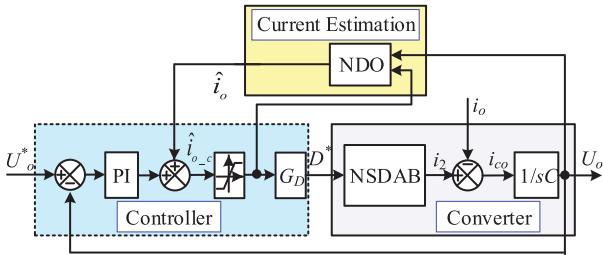


Fig. 36. Block diagram of CSC with estimated load-current feedforward [106].

some current sensorless control (CSC) strategies can also be used to solve this problem [105], [106]. A CSC with estimated load-current feedforward is proposed to improve the dynamic responses for the NSDAB dc-dc converter under the input voltage and load disturbances [106], and the core principle of this method can be expressed as follows:

$$\frac{dU_o}{dt} = \frac{I_2 - i_o}{C_o}. \quad (23)$$

According to (23), the disturbances of capacitor voltage can reflect the changes of load conditions, and I_2 can be calculated as follows:

$$I_2 = \frac{U_{in}D(1-D)T_s}{2nL}. \quad (24)$$

Combining a nonlinear disturbance observer (NDO) [107], [108], the block diagram of the CSC can be shown in Fig. 36.

In Fig. 36, \hat{i}_o is the estimated load current and \hat{i}_{o_c} is the estimated load current with PI compensation. Based on this current sensorless strategy, \hat{i}_o with accurate circuit parameters for the j th switching period can be expressed as

$$\hat{i}_o(j) = z(j) - lU_o(j) \quad (25)$$

where z is the inner state variable of NDO and l is the parameter related to the convergence rate, and $z(j)$ can be expressed as

$$\begin{aligned} z(j) &= \left(1 - \frac{lT_s}{C_o}\right) z(j-1) + \frac{l^2 T_s}{C_o} U_o(j-1) \\ &\quad + \frac{lT_s}{C_o} \hat{i}_{o_c}(j-1). \end{aligned} \quad (26)$$

In addition, D^* for the j th switching period can be expressed as

$$D^*(j) = \begin{cases} \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2nL\hat{i}_{o_c}(j-1)}{T_s U_{in}(k)}}, & (\hat{i}_{o_c} \geq 0) \\ -\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{2nL\hat{i}_{o_c}(j-1)}{T_s U_{in}(k)}}, & (\hat{i}_{o_c} < 0). \end{cases} \quad (27)$$

Based on this CSC scheme, excellent dynamic performances of the NSDAB dc-dc converter can be obtained [106], despite the dynamic performances under load disturbances are a bit influenced compared to the VDPC scheme [104].

D. Comparison of Dynamic-Optimization Strategies

As mentioned earlier, the load-current feedforward scheme [83], [84], [92], the direct-inductance-current control strategy [85], [98], [99], and the power-based control method [104], [106] can be used to improve the dynamic performances of the NSDAB dc-dc converter. Generally, there are two operating conditions for the NSDAB dc-dc converter: connected to the resistive load and connected to the dc power source. Table VII illustrates a comprehensive comparison of these dynamic-optimized strategies.

As given in Table VII, there are five methods for improving the dynamic responses of the NSDAB dc-dc converter connected with the resistive load. Although the FCSLC scheme [83] can obtain good dynamic performances during load disturbances, this method is difficult to be implemented online and requires the use of lookup table. In addition, compared with SLFC for the resistive load [84], FTBC [85], and VDPC [104] strategies can achieve excellent dynamic responses under load disturbances and input voltage disturbances. However, FTBC needs two more current sensors than the VDPC scheme. Moreover, the CSC strategy [106] can estimate the load current and improve the dynamic performances of the NSDAB dc-dc converter with just two voltage sensors, but with slightly worse dynamic responses under load disturbances compared with the VDPC scheme [104]. Therefore, when the load current is easy to measure, the VDPC method [104] is recommended to enhance the dynamic responses of the NSDAB dc-dc converter with the resistive load. When the load current is not easy to acquire, the CSC strategy [106] is recommended to improve the dynamic responses of the NSDAB dc-dc converter.

Moreover, there are three strategies for improving the dynamic responses of the NSDAB dc-dc converter connected with two dc voltage buses. Compared with SLFC for dc voltage bus [84], ADSM [98], and PCMC [99] can obtain the desired inductance current and the output current in a switching period, and the output load sensor can also be saved by using these two methods. Therefore, ADSM [98] and PCMC [99] are recommended when the NSDAB dc-dc converter connected with the dc voltage bus, and this converter just needs to offer the current to dc bus.

V. HYBRID DYNAMIC- AND STATIC-OPTIMIZATION CONCEPT

In Section III, the efficiency-optimizing techniques, including accurate power losses optimizing [17], [18], [35], [59], nonactive power optimizing [30], [64], [66], inductance current optimizing [31], [33], [48], [58], [72], [73], ZVS range optimizing [36], [69], [70], and burst mode [79], for an NSDAB dc-dc converter are analyzed and compared. In addition, load-current feedforward schemes [83], [84], [92], direct-inductance-current control strategies [85], [98], [99], and power-based control methods [104], [106] are analyzed and compared in Section IV for improving the dynamic responses of the NSDAB dc-dc converter. Based on the review and thorough comparisons in previous sections, a hybrid approach to combine the efficiency-optimization strategies and dynamic-optimization schemes is presented in this section. The hybrid approach is shown in Fig. 37.

TABLE VII
COMPREHENSIVE COMPARISON OF DYNAMIC-OPTIMIZED STRATEGIES FOR THE NSDAB DC-DC CONVERTER

Control Strategies	Specific Applications	Sensors	Switching Frequency	Input Voltage Disturbances	Load Disturbances
FCSLC [83]	Resistive Load	2: Output voltage sensor, load current sensor	20 kHz	Without experiments	10 switching periods (267 Ω-57 Ω) 20 switching periods (267 Ω-57 Ω)
SLFC [84]	Resistive load	4: Output voltage sensor, input voltage sensor, load current sensor, inductance current sensor	25 kHz	Without experiments	50 switching periods (18 Ω-4 Ω) & (4 Ω-18 Ω)
	DC voltage bus	4: Output voltage sensor, input voltage sensor, load current sensor, inductance current sensor	25 kHz	Not applicable	12.5 switching periods (1A-6A) & (6A-1A)
FTBC [85]	Resistive load	5: Output voltage sensor, input voltage sensor, load current sensor, primary-side and secondary-side inductance current sensor	22 kHz	Very small, not visible	Very small, not visible
ADSM [98]	DC voltage bus	3: Output voltage sensor, input voltage sensor, inductance current sensor	20 kHz	Not applicable	1 switching period
PCMC [99]	DC voltage bus	3: Output voltage sensor, input voltage sensor, inductance current sensor	10 kHz	Not applicable	1 switching period
VDPC [104]	Resistive Load	3: Output voltage sensor, input voltage sensor, load current sensor	10 kHz	Very small, not visible	Very small, not visible
CSC [106]	Resistive Load	2: Output voltage sensor, input voltage sensor	20 kHz	Very small, not visible	100 switching periods (27 Ω-400 Ω)

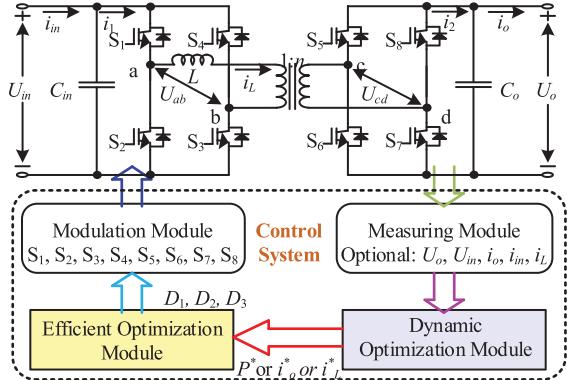


Fig. 37. Block schematic of the hybrid efficiency- and dynamic-optimization concept.

In Fig. 37, the presented hybrid efficiency- and dynamic-optimization strategy contains four modules, including measuring module, dynamic-optimization module, efficiency improving module, and modulation module. Usually, U_o , U_{in} , i_o , i_{in} , and i_L are selected to act as feedforward and feedback variables to improve the dynamic performances of the NSDAB dc-dc converter [84], [87], [88], [98], [99], [104]. Based on the dynamic-optimization module, desired transferred power P^* [104], [109], desired output current i_o^* [83], [84], [106], desired inductance current i_L^* [85], [98], [99], or their simplified values can be acquired to directly calculate the required phase-shift ratio under the SPS modulation method, and then, the steady state of the NSDAB dc-dc converter can be researched quickly. However, these dynamic-optimization methods do not consider

the efficiency-optimization performance of the NSDAB dc-dc converter. Actually, when P^* , i_o^* , and i_L^* are obtained, D_1 , D_2 , and D_3 can be determined to boost the efficiency of the NSDAB dc-dc converter [31], [33], [48], [58], [72], [73], [110], since these efficiency-optimization strategies can give specific relationships of D_1 , D_2 , and D_3 [33]. Moreover, when relationships of D_1 , D_2 , and D_3 are determined, P^* , i_o^* , and i_L^* can be expressed by each other according to (9). Therefore, when the required transferred power P^* , required output current i_o^* , or required inductance current i_L^* are obtained to boost the dynamic responses of the NSDAB dc-dc converter, and combining advanced phase-shift modulation methods, the optimization of static and dynamic performances of the NSDAB dc-dc converter can be achieved.

A. Hybrid Static- and Dynamic-Optimization (HSDO) Strategy for the NSDAB DC-DC Converter

Based on this hybrid efficiency- and dynamic-optimization concept, an HSDO strategy by combining the MCSO method [33] and power-control concept [104] has been proposed to improve the efficiency and robustness at the same time of an NSDAB dc-dc converter [111], which is shown in Fig. 38. In Fig. 38, i_o^* and p^* can be calculated as

$$\begin{cases} i_o^* = \frac{U_o^*}{U_o} i_o \\ p^* = \frac{2f_s L}{nU_{in} U_o} \left[\frac{1}{2} i_o (U_o^* + U_o) \left(\frac{U_o^*}{U_o} + 1 \right) \right. \\ \quad \left. + U' p l i_o \left(\frac{U_o^*}{U_o} + 1 \right) + \lambda f_s C_2 (U_o^* - U_o) (U_o^* + U_o) \right] \end{cases} \quad (28)$$

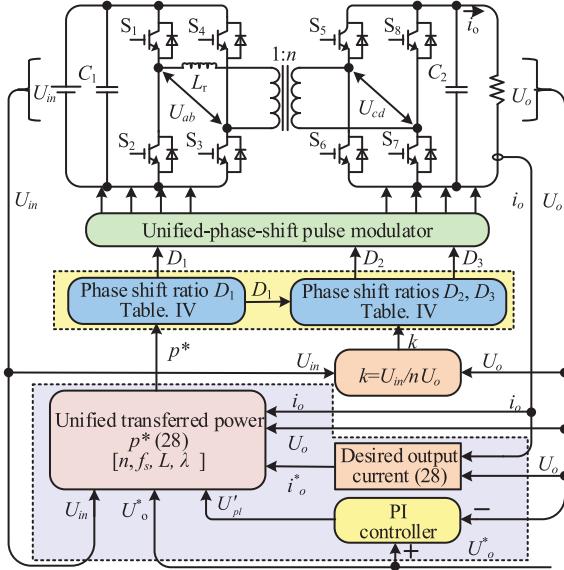


Fig. 38. Block diagram of the HSDO scheme [111].

TABLE VIII
CIRCUIT PARAMETERS OF THE SCALE-DOWN DAB DC-DC PLATFORM

Equivalent Inductance	200 μ H
Switching Frequency	10 kHz
Transformer Turn Ratio	0.5
Switches	STC3080
Output & Input Capacitor	1 mF
Load Resistor	10 Ω or 20 Ω
Desired Output Voltage	40 V

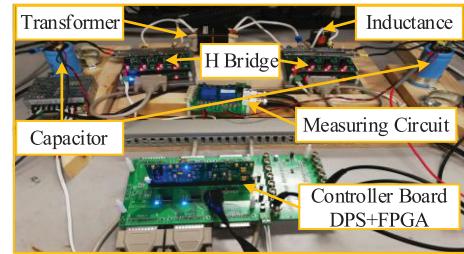


Fig. 39. Experimental platform of the NSDAB dc-dc converter.

where λ is proportional limit value to avoid system instability. According to (28), λ is used to reduce the difference between the output voltage U_o and its desired value U_o^* . Moreover, with the feedback values of the input voltage U_{in} and the load current i_o , the excellent dynamic performance can be provided during disturbances of the input voltage and load resistor. Therefore, small value λ can be employed in controller, and λ can even be equivalent to zero [104].

As shown in Fig. 38, the simplified transferred power of the NSDAB dc-dc converter can be acquired according to (28) first, then combining Table IV, this comprehensive optimizing control strategy can be implemented to increase the efficiency and enhance the dynamic performances of the NSDAB dc-dc converter [111].

B. Experimental Results Among the HSDO Strategy and Other Methods

In this section, based on this HSDO strategy by combining the MCSO method [33] and power-control concept [104], some comparative experiments are carried out to verify the similar efficiency improving performances of the MCS [33] and MRMSC [47] schemes. Based on performances of the HSDO strategy by combining the MCSO method [33] and power-control concept [104], the availability of the presented hybrid efficiency- and dynamic-optimization concept can also be verified. Then, to verify the aforementioned theoretical analysis, a scale-down laboratory prototype is designed, and the main parameters of the NSDAB dc-dc converter are given in Table VIII. Moreover, the picture of the experimental platform of the NSDAB dc-dc converter can be shown in Fig. 39.

When the output voltage is set to 40 V, Fig. 40 shows experimental curves of efficiency with different input voltages under the SPS method, VDPC scheme, MCSO strategy, the MRMSC scheme, and the HSDO strategy. As shown in Fig. 40, no matter load resistor is equivalent

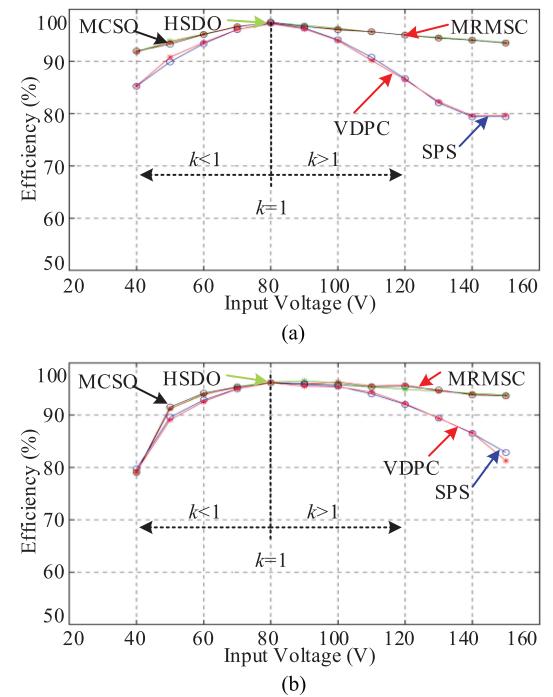


Fig. 40. Experimental curves of the efficiency varied with the input voltage under the SPS method, the VDPC scheme, the MCSO strategy, the MRMSC scheme, and the HSDO strategy. (a) $R = 20 \Omega$. (b) $R = 10 \Omega$.

to 20 or 10 Ω , the MCSO scheme, the HSDO strategy, and the MRMSC method can obtain similar efficiency under different input voltage, which agrees the analysis theoretical analysis of the MRMSC scheme and the MCSO strategy. Compared to the SPS and VDPC methods, these three optimization methods can achieve better efficiency. When k is close to one, these five schemes can achieve similar efficiency for the NSDAB dc-dc converter. Moreover, when k is equivalent to one, the

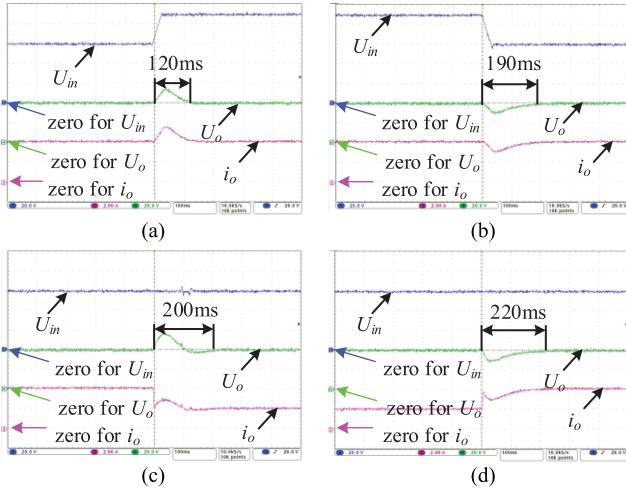


Fig. 41. Experimental results of dynamic responses under voltage PI controller (U_o : 20 V/div; U_{in} : 20 V/div; i_o : 2 A/div; Time: 100 ms/div). (a) U_{in} steps up from 60 to 90 V. (b) U_{in} steps down from 90 to 60 V. (c) R steps up from 10 to 20Ω . (d) R steps down from 20 to 10Ω .

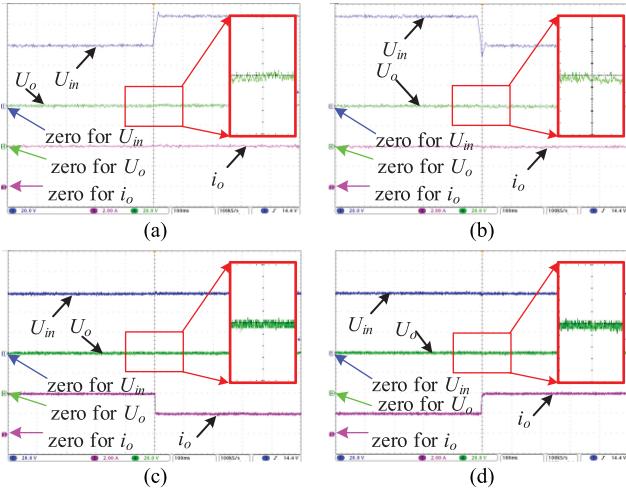


Fig. 42. Experimental results of dynamic responses under the VDPC strategy (U_o : 20 V/div; U_{in} : 20 V/div; i_o : 2 A/div; Time: 100 ms/div). (a) U_{in} steps up from 60 to 90 V. (b) U_{in} steps down from 90 to 60 V. (c) R steps up from 10 to 20Ω . (d) R steps down from 20 to 10Ω .

highest efficiency can be obtained under different load resistor. Therefore, when both side voltages are constant, it may be better to design the NSDAB dc–dc converter with matched voltages. Moreover, the MCSO scheme can provide the similar efficiency to the MRMSC strategy, and the HSDO strategy can inherit the efficiency improving performance of the MCSO scheme.

Moreover, when the desired output voltage is 40 V, Figs. 41–43 show the experimental results of single-voltage-loop control with the SPS modulation method, the VDPC scheme [104], and the HSDO strategy [111] and under disturbances of the input voltage and the load resistor, respectively.

As shown in Fig. 41(a) and (b), when the input voltage is changed between 60 and 90 V, the setting times for researching

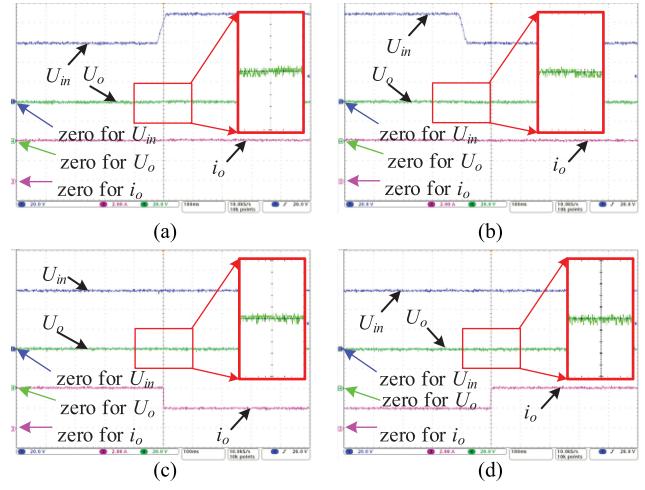


Fig. 43. Experimental results of dynamic responses under the HSDO strategy (U_o : 20 V/div; U_{in} : 20 V/div; i_o : 2 A/div; Time: 100 ms/div). (a) U_{in} steps up from 60 to 90 V. (b) U_{in} steps down from 90 to 60 V. (c) R steps up from 10 to 20Ω . (d) R steps down from 20 to 10Ω .

desired output voltage again under voltage PI controller are over 100 ms. Moreover, when the load resistor is changed between 10 and 20Ω , the transient responses of the output voltage under voltage PI controller are also slow [see Fig. 41(c) and (d)] with setting time over 200 ms. In addition, as shown in Figs. 42 and 43, when the VDPC and HSDO strategies are employed, the output voltage can keep stable under disturbances of the input voltage and load resistor, and excellent dynamic responses can be acquired for the NSDAB dc–dc converter. Therefore, the HSDO strategy can also inherit the excellent dynamic performance from the VDPC method.

Therefore, the excellent performances of the MCSO method [33] and power-control concept [104] can be obtained at the same time by using the HSDO strategy [111]. Therefore, the hybrid efficiency- and dynamic-optimization concept, as shown in Fig. 37, can combine some efficiency improving methods and some dynamic-optimization strategies.

VI. CONCLUSION

An NSDAB dc–dc converter has become one of the most attractive isolated dc–dc power conversion topologies for dc grid, SST, automotive application, energy storage system, and aerospace application. This paper offers a comprehensive overview of modulation methods, efficiency-optimization schemes, and dynamic-optimization strategies of the NSDAB dc–dc converter, and thorough comparisons of different optimization methods are conducted.

- 1) The typical modulation methods, including the advanced phase-shift modulation and the variable-frequency modulation methods, are presented in this paper. Based on all possible 18 phase-shift modulation patterns, the reason why the SPS, DPS, EPS, and TPS modulation schemes are selected for an NSDAB dc–dc converter is analyzed. Moreover, the correlation analysis of typical phase-shift

- modulation methods, including the SPS, DSP, EPS, and TPS modulation methods, is illustrated, which can explain why the TPS modulation method can always provide the best efficiency for an NSDAB dc–dc converter.
- 2) An overview of efficiency-optimization schemes for an NSDAB dc–dc converter, including power-loss-model-based optimization methods, nonactive power optimization techniques, inductance current optimization strategies, ZVS range optimization schemes, and burst mode, is conducted. Under the consideration of both optimized performance and feasibility, the MCSO strategy with simple operation is recommended.
 - 3) This paper also provides an overview of dynamic-optimization strategies for an NSDAB dc–dc converter, including load-current feedforward schemes, direct-inductance-current control strategies, and power-based control methods. When an NSDAB dc–dc converter is connected to resistive load, the VDPC scheme and the CSC strategy are recommended because of excellent dynamic responses. When the NSDAB dc–dc converter is connected to the dc voltage bus, the ADSM and the PCMC for fast transient response of required inductance current are recommended.
 - 4) Finally, this paper presents an idea of hybrid efficiency- and dynamic-optimization concept to improve both steady state and transient performances of an NSDAB dc–dc converter. A static- and dynamic-optimization strategy by combining the minimum-current-stress strategy and power-control concept verifies the feasibility of the presented idea.

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