Instruction Encodings

		M			ZP								R				I				J			
type		00			01								10				11				11			
s		0		1	0				1				-				-				-			
fn		00	An		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
op	000	pfx			(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	sr1	rr1	sr4	rr4	(1)	(1)	(1)	(1)	-	-	-	-
	001	hlt	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	sl1	rl1	sl4	rl4	(1)	(1)	(1)	(1)	-	-	-	-
	010	-	cmp	(1)	cmp	-	cpc	-	(1)	-	(1)	-	cmp	-	cpc	-	cmp	-	cpc	-	-	-	-	-
	011	lp	mov	mov	mov	set	sef	sel	mov	set	sef	sel	mov	set	sef	sel	mov	set	sef	sel	j	-	-	-
	100	-	add	add	add	dad	adc	dac	add	dad	adc	dac	add	dad	adc	dac	add	dad	adc	dac	b+	-	-	-
	101	-	sub	sub	sub	rsb	sbc	dsc	sub	rsb	sbc	dsc	sub	rsb	sbc	dsc	sub	rsb	sbc	dsc	b-	-	-	-
	110	-	and	and	and	or	xor	mvl	and	or	xor	mvl	and	or	xor	mvl	and	or	xor	mvl	-	-	-	jl
	111	-	adt	adt	adt	adf	sbt	sbf	adt	adf	sbt	sbf	adt	adf	sbt	sbf	adt	adf	sbt	sbf	bt+	bf+	bt-	bf-

op: 3 bit opcode for the instruction type
fn: 2 bit function code, for M-Type instructions this is an address register
s : 1 bit field indicating that the instruction is a memory store

(1) Instruction slot not available, will cause undocumented behaviour.
(*) J-Type instructions are regular I-Type instructions that change their name when used with the PC as the destination register.
(*) M-Type instructions with op=000 or fn=00 have special meanings.