

Instruction Encodings

	M			ZP								R				I				J			
type	00			01								10				11				11			
s	0	1		0				1				-				-				-			
fn	Aj			00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
op	000	cmp	(1)	cmp	-	cpc	-	(1)	-	(1)	-	cmp	pfx	cpc	hlt	cmp	-	cpc	-	-	-	-	-
	001	mov	mov	mov	set	sef	sel	mov	set	sef	sel	mov	set	sef	sel	mov	set	sef	sel	j	-	-	-
	010	add	add	add	dad	adc	dac	add	dad	adc	dac	add	dad	adc	dac	add	dad	adc	dac	b+	-	-	-
	011	sub	sub	sub	rsb	sbc	dsc	sub	rsb	sbc	dsc	sub	rsb	sbc	dsc	sub	rsb	sbc	dsc	b-	-	-	-
	100	and	and	and	or	xor	mv1	and	or	xor	mv1	and	or	xor	mv1	and	or	xor	mv1	-	-	-	jl
	101	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	sr1	rr1	sr4	rr4	(1)	(1)	(1)	(1)	-	-	-	-
	110	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	sl1	rl1	sl4	rl4	(1)	(1)	(1)	(1)	-	-	-	-
	111	adt	adt	adt	adf	sbt	sb1	adt	adf	sbt	sb1	adt	adf	sbt	sb1	adt	adf	sbt	sb1	bt+	bf+	bt-	bf-

op: 3 bit opcode for the instruction type

fn: 2 bit function code, for M-Type instructions this is an address register

s : 1 bit field indicating that the instruction is a memory store

(1) Instruction slot not available, will cause undocumented behaviour.

(*) J-Type instructions are regular I-Type instructions that change their name when used with the PC as the destination register.