Full Adder Truth Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Inputs | | | Outputs | |
| CIN | A | B | COUT | S |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Output Equation:

COUT = CIN’AB + CINA’B + CINAB’ + CINAB

S= CIN’A’B + CIN’AB’ + CINA’B’ + CINAB

Karnaugh Mapping:

COUT

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CIN \ AB | AB | | | | |
| CIN |  | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |

(All simplifications for Karnaugh Mappings are identified with circles.)

Resulting Equation:

COUT = AB + CINB + CINA

S

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CIN \ AB | AB | | | | |
| CIN |  | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

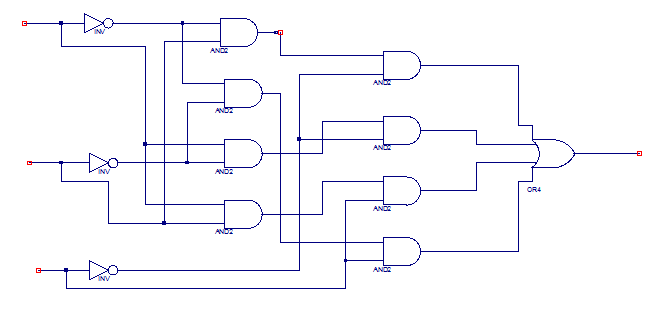
(No possibilities for simplification through Karnaugh Mapping.)

Resulting Equation:

S= CIN’A’B + CIN’AB’ + CINA’B’ + CINAB

Schematics for both outputs:

S:



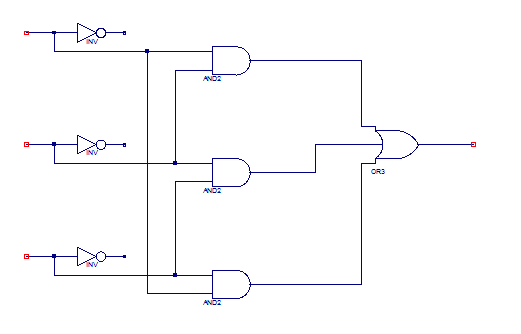
CIN

COUT

B

A

COUT:



CIN

S

B

A

Full Adder interface:

( Inputs )

( S= CIN’A’B + CIN’AB’ + CINA’B’ + CINAB )

A

B

Cin

Sum

Cout

( CarryIn )

( COUT = AB + CINB + CINA )

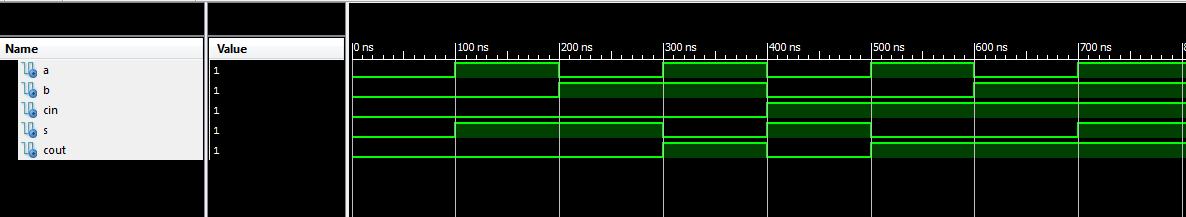
[ VHDL file created and testbench created.]

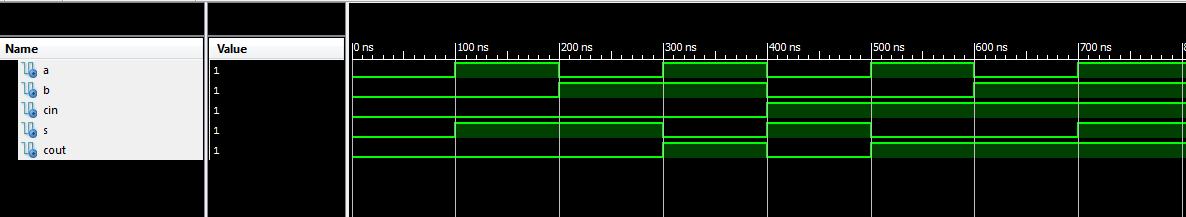
Simulation Results:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Expected Outputs | | Simulation Results | |
| CIN | A | B | COUT | S | COUT | S |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Initially my simulation results were incorrect. My COUT and S outputs were switched. When I looked back on my code I realized that I switched the two outputs. I switched the outputs when labeling my schematic and then created my code off of that schematic. This was a very simple fix as all I had to do was re-label my schematic and the code for my outputs. After correcting my typos, my simulation resulted in the expected outcomes.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | Expected Outputs | | Simulation Results | |
| CIN | A | B | COUT | S | COUT | S |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |





(Above are the simulation results in waveform format. The waveforms match the expected truth table. )

Bugs/Errors Encountered:

Initially I coded my VHDL with switched outputs. My S responded how my COUT while my COUT responded how my S output should have responded. I realized I switched my code. I ran into one other error when I checked the syntax. I misnamed CIN as simply C. Once I corrected this error and correctly labeled my outputs, my code worked as expected.