

# CPU

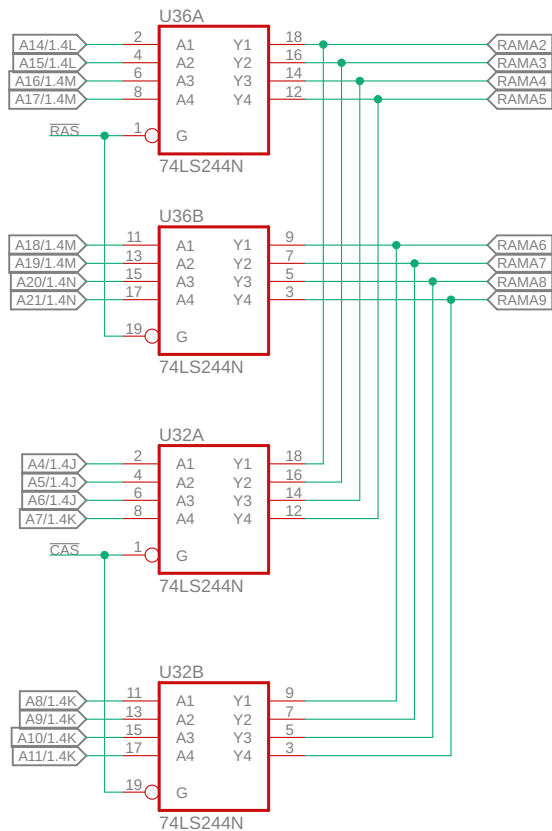
TITLE: schematic

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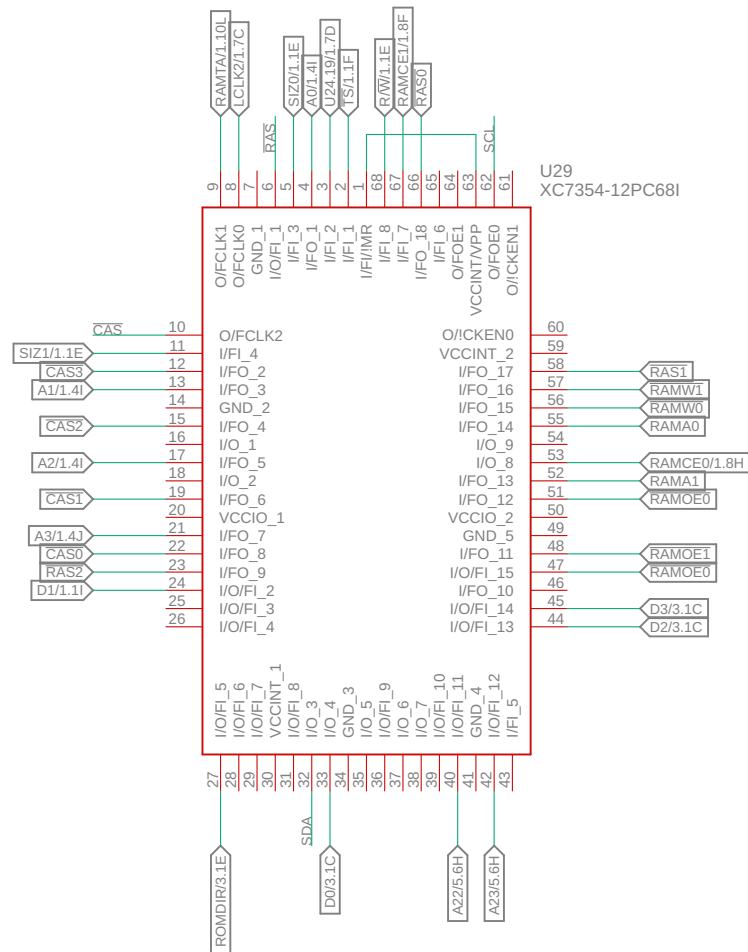
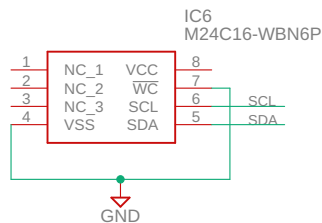
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DRAM banks not shown.

24x 514400 1Mx4 DRAMs organized as 3 rows of 8.  
CAS0:3 ordered least-to-most significant byte.  
RAMOE0:3 ordered least-to-most significant byte.  
RAMW0:1 ordered least-to-most significant word.  
RAS0:2 not ordered.



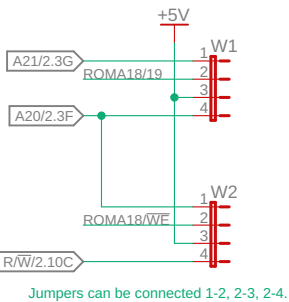
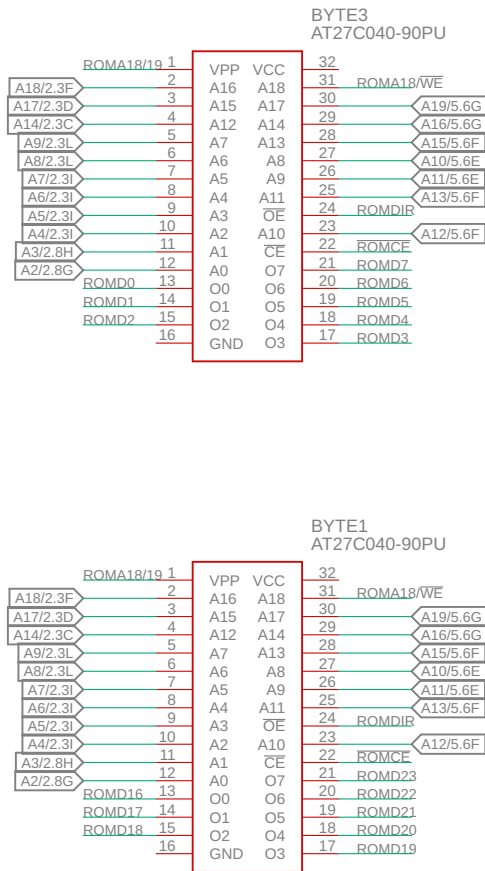
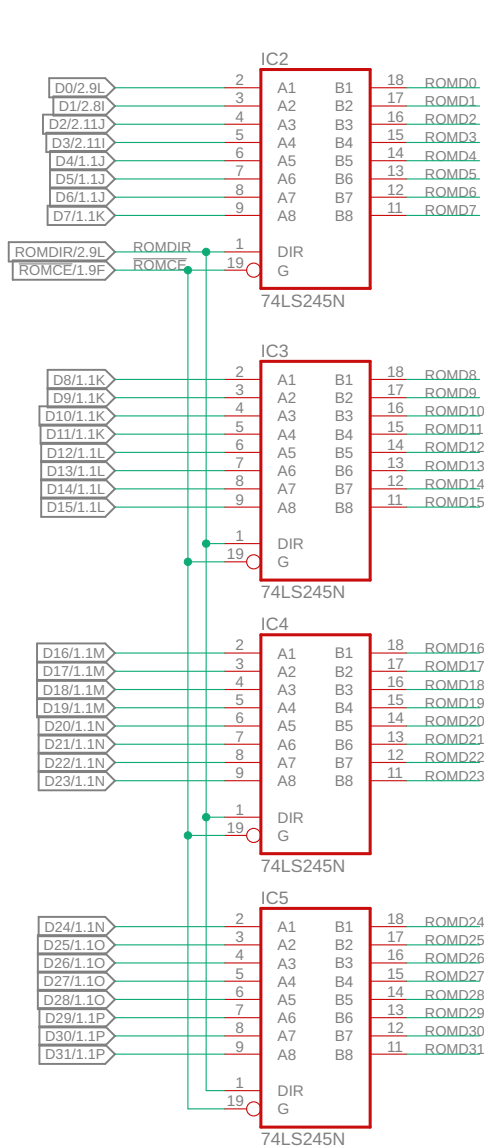
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# ROM

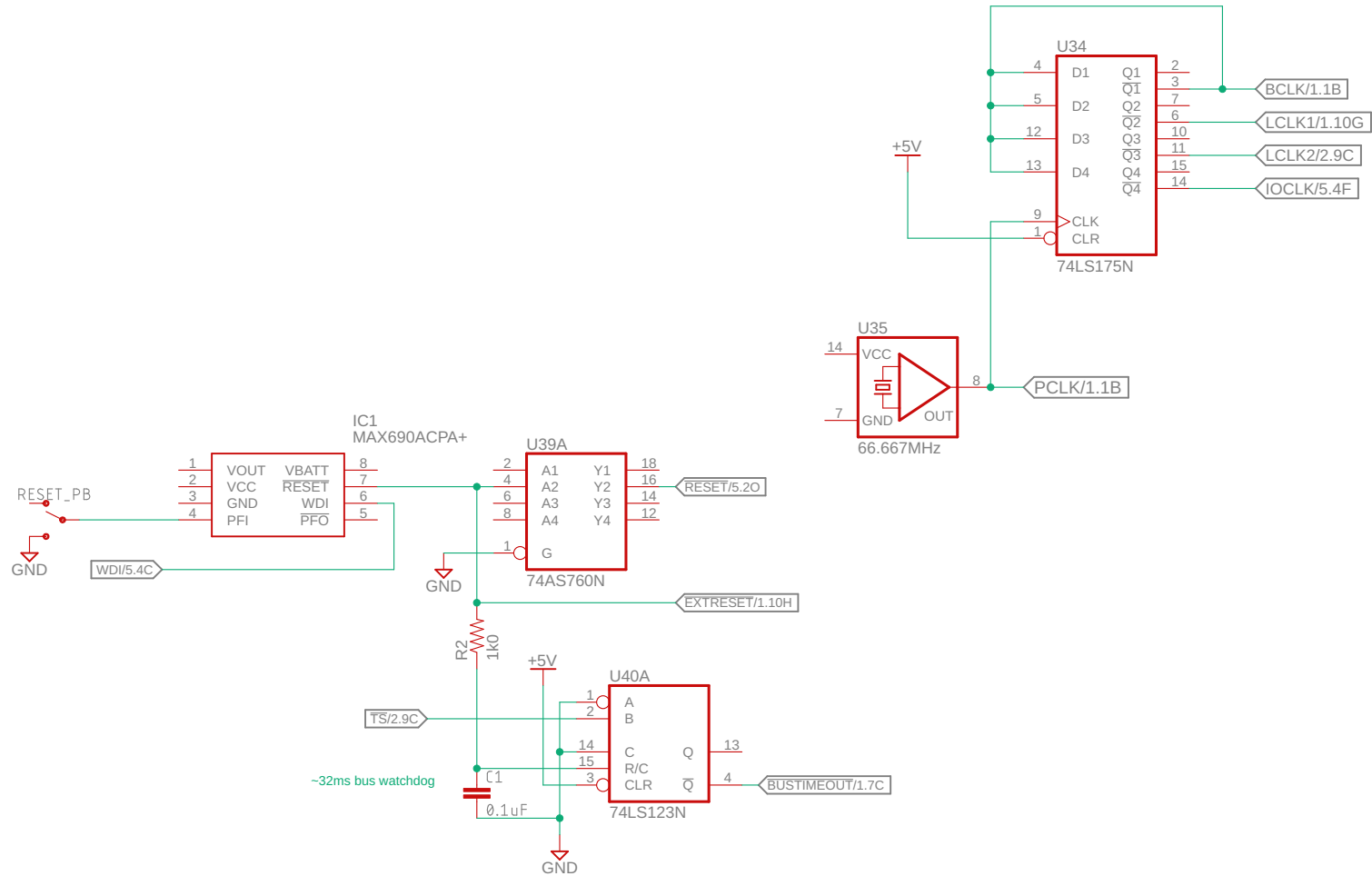
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## Reset & Clock

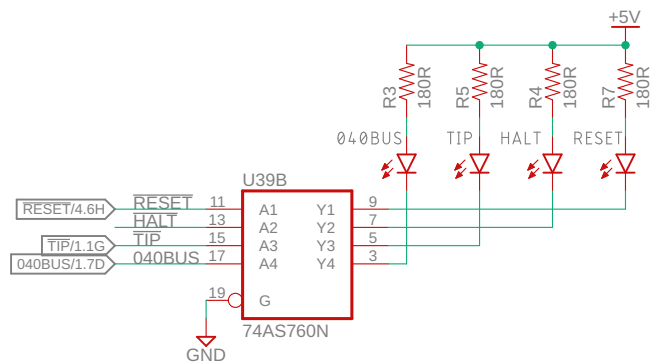
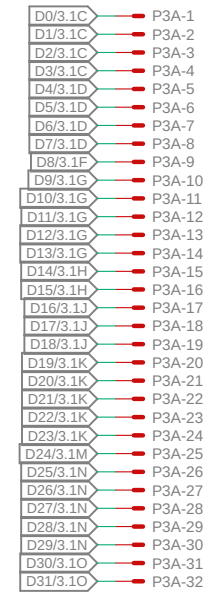
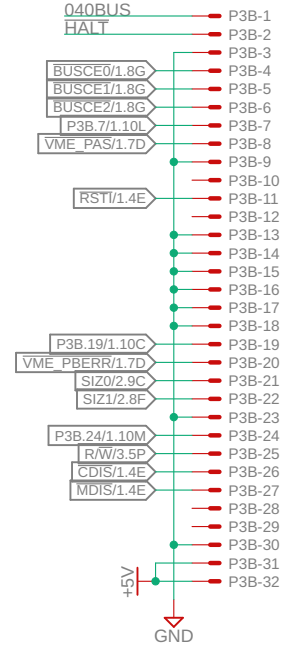
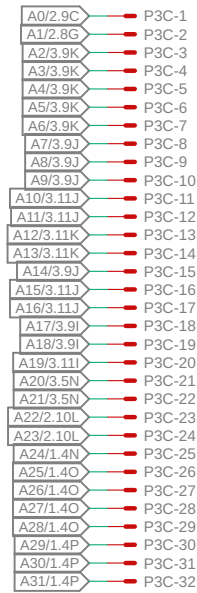
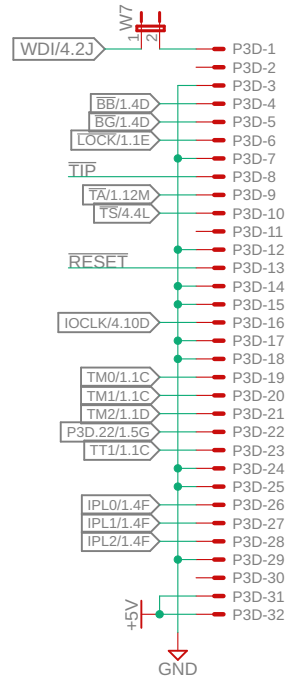
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## Expansion

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