
32-Mbit (x16) Multi-Purpose Flash Plus

The SST39VF3201C and SST39VF3202C devices are 2-Mbit x16, CMOS Multi-Purpose Flash Plus (MPF+) manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF3201C and SST39VF3202C write (Program or Erase) with a 2.7V-3.6V power supply. This device conforms to JEDEC standard pinouts for x16 memories.

Features

- Organized as 2-Mbit x16
- Single Voltage Read and Write Operations:
 - 2.7V-3.6V
- Superior Reliability:
 - Endurance: 100,000 Cycles (Typical)
 - Greater than 100 years Data Retention
- Low-Power Consumption (typical values at 5 MHz):
 - Active Current: 6 mA (typical)
 - Standby Current: 4 μ A (typical)
 - Auto Low-Power Mode: 4 μ A (typical)
- Hardware Block Protection/WP# Input Pin:
 - Top Block Protection (top two 4-KWord blocks) for SST39VF3202C
 - Bottom Block-Protection (bottom two 4-KWord blocks) for SST39VF3201C
- Sector-Erase Capability:
 - Uniform 2-KWord sectors
- Block-Erase Capability:
 - Flexible block architecture
 - Eight 4-KWord blocks, 63 32-KWord blocks
- Chip-Erase Capability
- Erase-Suspend/Erase-Resume Capabilities
- Hardware Reset Pin (RST#)
- Security-ID Feature:
 - Microchip: 128 bits; User: 128 words
- Fast Read Access Time:
 - 70 ns
- Latched Address and Data
- Fast Erase and Word-Program:
 - Sector-Erase Time: 18 ms (typical)
 - Block-Erase Time: 18 ms (typical)
 - Chip-Erase Time: 35 ms (typical)
 - Word-Program Time: 7 μ s (typical)
- Automatic Write Timing:
 - Internal V_{PP} Generation
- End-of-Write Detection:
 - Toggle Bits
 - Data# Polling
 - RY/BY# Pin
- CMOS I/O Compatibility
- JEDEC Standard:
 - Flash EEPROM Pin Assignments
- Temperature Ranges Supported:
 - Industrial (I): -40°C to +85°C
- All devices are RoHS compliant

Packages

- 48-lead TSOP (12 mm x 20 mm)
- 48-ball TFBGA (6 mm x 8 mm)

SST39VF3201C/SST39VF3202C

DESCRIPTION

The SST39VF3201C and SST39VF3202C devices are 2-Mbit x16 CMOS Multi-Purpose Flash Plus (MPF+) manufactured with proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF3201C/SST39VF3202C write (Program or Erase) with a 2.7V-3.6V power supply. These devices conform to JEDEC standard pin assignments for x16 memories.

Featuring high-performance Word Program, the SST39VF3201C/SST39VF3202C devices provide a typical Word Program time of 7 μ sec. These devices use Toggle Bit, Data# Polling or RY/BY# pin to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured and tested for a wide spectrum of applications, these devices are offered with a typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

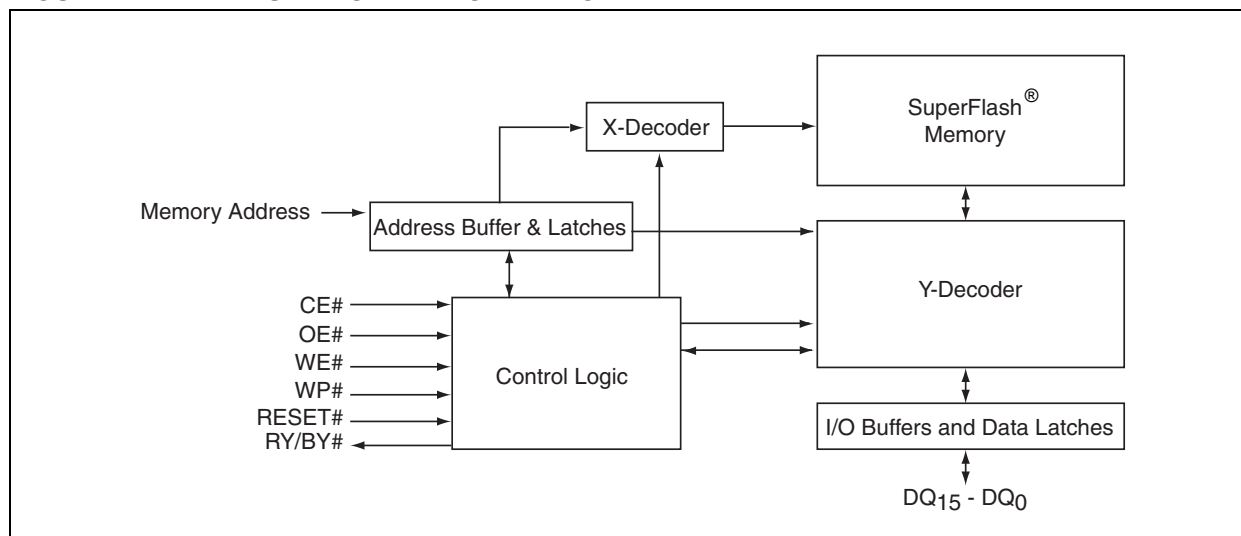
The SST39VF3201C/SST39VF3202C devices are suited for applications that require convenient and economical updating of program, configuration or data memory. For all system applications, they significantly improve performance and reliability while lowering power consumption. They inherently use less energy during Erase and Program than alternative Flash technologies. The total energy consumed is a function of the applied voltage, current and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time. As a result, the total energy consumed during any Erase or Program operation is less than alternative Flash technologies. These devices also improve flexibility while lowering the cost for program, data and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or derated as is necessary with alternative Flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high-density, surface mount requirements, the SST39VF3201C/SST39VF3202C devices are offered in 48-lead TSOP and 48-ball TFBGA packages. See [Figure 2](#) and [Figure 3](#) for pin assignments.

BLOCK DIAGRAM

FIGURE 1: FUNCTIONAL BLOCK DIAGRAM



SST39VF3201C/SST39VF3202C

PIN DESCRIPTION

FIGURE 2: PIN ASSIGNMENTS FOR 48-LEAD TSOP

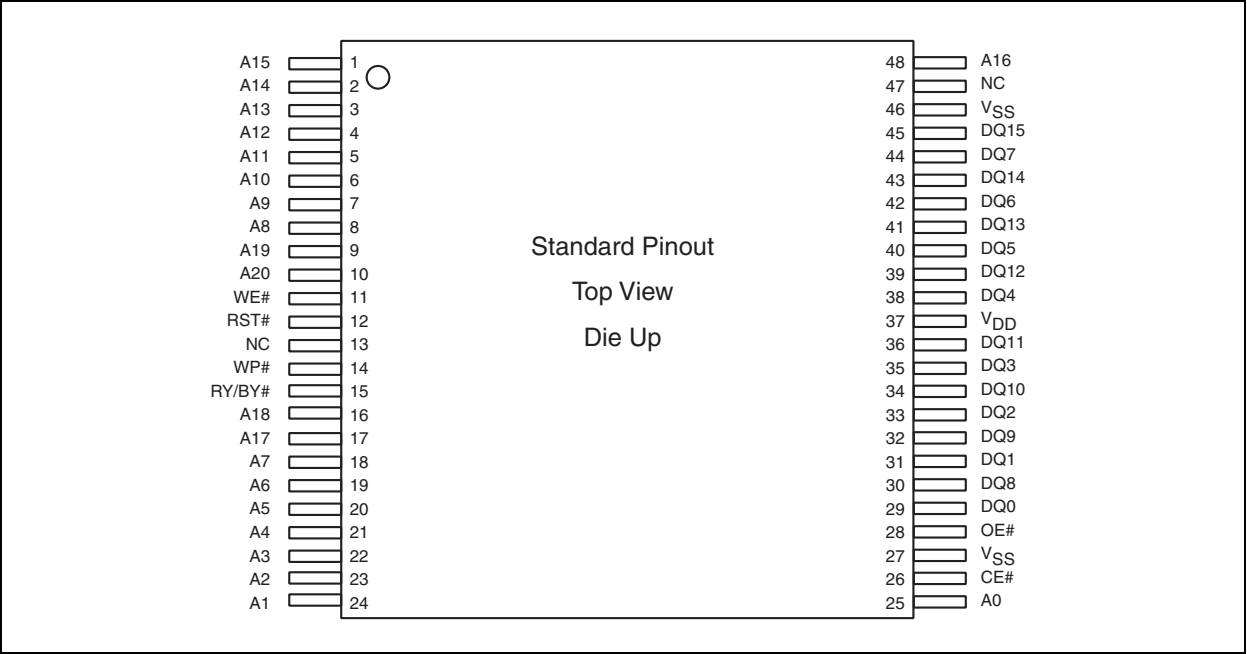
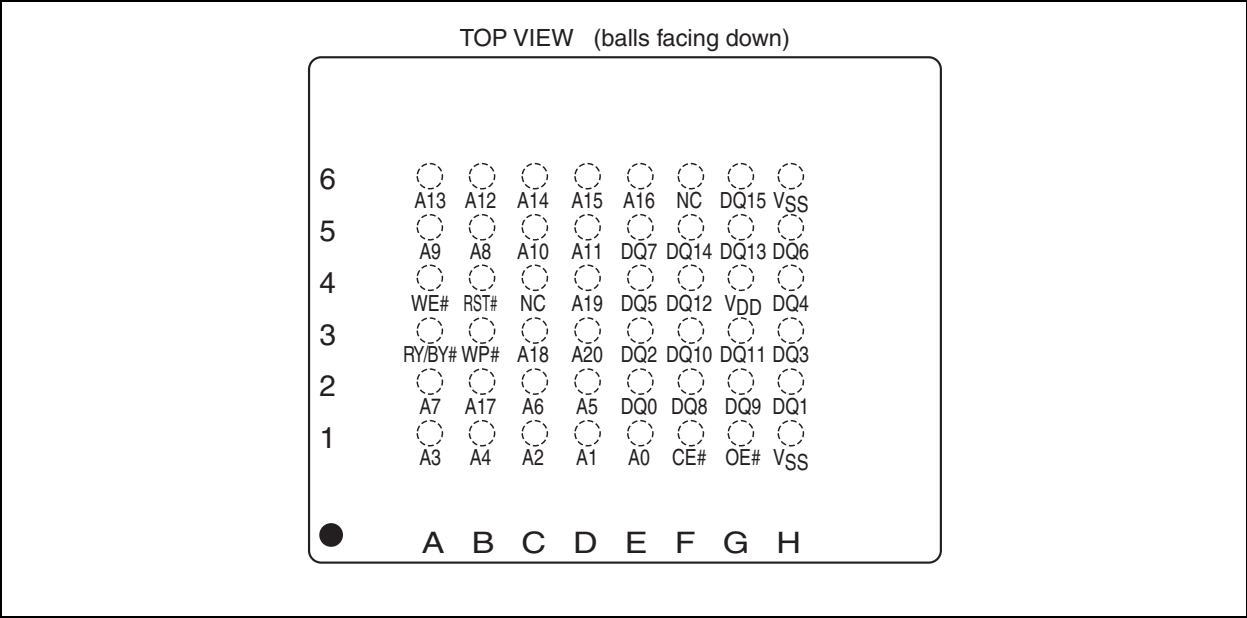


FIGURE 3: PIN ASSIGNMENTS FOR 48-BALL TFBGA



SST39VF3201C/SST39VF3202C

TABLE 1: PIN DESCRIPTION

Symbol	Pin Name	Functions
$A_{MS}^{(1)}-A_0$	Address Inputs	To provide memory addresses. During Sector-Erase $A_{MS}-A_{11}$ address lines will select the sector. During Block-Erase $A_{MS}-A_{15}$ address lines will select the block.
$DQ_{15}-DQ_0$	Data Input/Output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when $OE\#$ or $CE\#$ is high.
$WP\#$	Write-Protect	To protect the top/bottom boot block from Erase/Program operation when grounded.
$RST\#$	Reset	To reset and return the device to Read mode.
$CE\#$	Chip Enable	To activate the device when $CE\#$ is low.
$OE\#$	Output Enable	To gate the data output buffers.
$WE\#$	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide power supply voltage: 2.7V-3.6V
V_{SS}	Ground	
NC	No Connection	Unconnected pins.
$RY/BY\#$	Ready/Busy#	To output the status of a Program or Erase operation. $RY/BY\#$ is a open-drain output, so a 10 KW-100 KW pull-up resistor is required to allow $RY/BY\#$ to transition high indicating the device is ready to read.

Note 1: A_{MS} = Most Significant address
 $A_{MS} = A_{20}$ for SST39VF3201C/SST39VF3202C

TABLE 2: TOP/BOTTOM BOOT BLOCK ADDRESS

Top Boot Block Address SST39VF3202C			Bottom Boot Block Address SST39VF3201C		
#	Size (KWord)	Address Range	#	Size (KWord)	Address Range
70	4	1FF000H-1FFFFFFH	70	32	1F8000H-1FFFFFFH
69	4	1FE000H-1FEFFFFH	69	32	1F0000H-1F7FFFFH
68	4	1FD000H-1FDFFFFH	68	32	1E8000H-1EFFFFH
67	4	1FC000H-1FCFFFFH	67	32	1E0000H-1E7FFFFH
66	4	1FB000H-1FBFFFFH	66	32	1D8000H-1DFFFFH
65	4	1FA000H-1FAFFFFH	65	32	1D0000H-1D7FFFFH
64	4	1F9000H-1F9FFFFH	64	32	1C8000H-1CFFFFH
63	4	1F8000H-1F8FFFFH	63	32	1C0000H-1C7FFFFH
62	32	1F0000H-1F7FFFFH	62	32	1B8000H-1BFFFFH
61	32	1E8000H-1EFFFFH	61	32	1B0000H-1B7FFFFH
60	32	1E0000H-1E7FFFFH	60	32	1A8000H-1AFFFFH
59	32	1D8000H-1DFFFFH	59	32	1A0000H-1A7FFFFH
58	32	1D0000H-1D7FFFFH	58	32	198000H-19FFFFH
57	32	1C8000H-1CFFFFH	57	32	190000H-197FFFFH
56	32	1C0000H-1C7FFFFH	56	32	188000H-18FFFFH
55	32	1B8000H-1BFFFFH	55	32	180000H-187FFFFH
54	32	1B0000H-1B7FFFFH	54	32	178000H-17FFFFH
53	32	1A8000H-1AFFFFH	53	32	170000H-177FFFFH
52	32	1A0000H-1A7FFFFH	52	32	168000H-16FFFFH
51	32	198000H-19FFFFH	51	32	160000H-167FFFFH

SST39VF3201C/SST39VF3202C

TABLE 2: TOP/BOTTOM BOOT BLOCK ADDRESS (CONTINUED)

Top Boot Block Address SST39VF3202C			Bottom Boot Block Address SST39VF3201C		
50	32	190000H-197FFFFH	50	32	158000H-15FFFFFH
49	32	188000H-18FFFFFH	49	32	150000H-157FFFFH
48	32	180000H-187FFFFH	48	32	148000H-14FFFFFH
47	32	178000H-17FFFFFH	47	32	140000H-147FFFFH
46	32	170000H-177FFFFH	46	32	138000H-13FFFFFH
45	32	168000H-16FFFFFH	45	32	130000H-137FFFFH
44	32	160000H-167FFFFH	44	32	128000H-12FFFFFH
43	32	158000H-15FFFFFH	43	32	120000H-127FFFFH
42	32	150000H-157FFFFH	42	32	118000H-11FFFFFH
41	32	148000H-14FFFFFH	41	32	110000H-117FFFFH
40	32	140000H-147FFFFH	40	32	108000H-10FFFFFH
39	32	138000H-13FFFFFH	39	32	100000H-107FFFFH
38	32	130000H-137FFFFH	38	32	0F8000H-0FFFFFH
37	32	128000H-12FFFFFH	37	32	0F0000H-0F7FFFFH
36	32	120000H-127FFFFH	36	32	0E8000H-0EFFFFFH
35	32	118000H-11FFFFFH	35	32	0E0000H-0E7FFFFH
34	32	110000H-117FFFFH	34	32	0D8000H-0DFFFFFH
33	32	108000H-10FFFFFH	33	32	0D0000H-0D7FFFFH
32	32	100000H-107FFFFH	32	32	0C8000H-0CFFFFFH
31	32	0F8000H-0FFFFFH	31	32	0C0000H-0C7FFFFH
30	32	0F0000H-0F7FFFFH	30	32	0B8000H-0BFFFFFH
29	32	0E8000H-0EFFFFFH	29	32	0B0000H-0B7FFFFH
28	32	0E0000H-0E7FFFFH	28	32	0A8000H-0AFFFFFH
27	32	0D8000H-0DFFFFFH	27	32	0A0000H-0A7FFFFH
26	32	0D0000H-0D7FFFFH	26	32	098000H-09FFFFFH
25	32	0C8000H-0CFFFFFH	25	32	090000H-097FFFFH
24	32	0C0000H-0C7FFFFH	24	32	088000H-08FFFFFH
23	32	0B8000H-0BFFFFFH	23	32	080000H-087FFFFH
22	32	0B0000H-0B7FFFFH	22	32	078000H-07FFFFFH
21	32	0A8000H-0AFFFFFH	21	32	070000H-077FFFFH
20	32	0A0000H-0A7FFFFH	20	32	068000H-06FFFFFH
19	32	098000H-09FFFFFH	19	32	060000H-067FFFFH
18	32	090000H-097FFFFH	18	32	058000H-05FFFFFH
17	32	088000H-08FFFFFH	17	32	050000H-057FFFFH
16	32	080000H-087FFFFH	16	32	048000H-04FFFFFH
15	32	078000H-07FFFFFH	15	32	040000H-047FFFFH
14	32	070000H-077FFFFH	14	32	038000H-03FFFFFH
13	32	068000H-06FFFFFH	13	32	030000H-037FFFFH
12	32	060000H-067FFFFH	12	32	028000H-02FFFFFH
11	32	058000H-05FFFFFH	11	32	020000H-027FFFFH
10	32	050000H-057FFFFH	10	32	018000H-01FFFFFH
9	32	048000H-04FFFFFH	9	32	010000H-017FFFFH
8	32	040000H-047FFFFH	8	32	008000H-00FFFFFH
7	32	038000H-03FFFFFH	7	4	007000H-007FFFFH

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TABLE 2: TOP/BOTTOM BOOT BLOCK ADDRESS (CONTINUED)

Top Boot Block Address SST39VF3202C			Bottom Boot Block Address SST39VF3201C		
6	32	030000H-037FFFH	6	4	006000H-006FFFH
5	32	028000H-02FFFFH	5	4	005000H-005FFFH
4	32	020000H-027FFFH	4	4	004000H-004FFFH
3	32	018000H-01FFFFH	3	4	003000H-003FFFH
2	32	010000H-017FFFH	2	4	002000H-002FFFH
1	32	008000H-00FFFFH	1	4	001000H-001FFFH
0	32	000000H-007FFFH	0	4	000000H-000FFFH

DEVICE OPERATION

Comments are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

The SST39VF3201C/SST39VF3202C also have Auto-Low-Power mode which puts the device in a near Standby mode after data has been accessed with a valid Read operation. This reduces the IDD active read current from typically 9 mA to typically 4 μ A. Auto-Low-Power mode reduces the typical IDD active read current to the range of 2 mA/MHz of Read cycle time. The device exits Auto-Low-Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty. Note that the device does not enter Auto-Low-Power mode after power-up with CE# held steadily low, until the first address transition or CE# is driven high.

Read

The Read operation of the SST39VF3201C/SST39VF3202C is controlled by CE# and OE#, both of which have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high-impedance state when either CE# or OE# is high. Refer to [Figure 5](#) for further details.

Word Program Operation

The SST39VF3201C/SST39VF3202C are programmed on a word-by-word basis. Before programming, the sector where the word exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 10 μ s. See [Figure 6](#) and [Figure 7](#) for WE# and CE# controlled Program operation timing diagrams and [Figure 21](#) for a flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored. During the command sequence, WP# should be statically held high or low.

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Sector/Block-Erase Operation

The Sector- (or Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST39VF3201C/SST39VF3202C offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 2 KWord. The Block-Erase mode is based on block sizes of 4 and 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse while the command (50H or 30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See [Figure 11](#) and [Figure 12](#) for timing waveforms and [Figure 25](#) for a flowchart. Any commands issued during the Sector- or Block-Erase operation are ignored. When WP# is low, any attempt to Sector- (Block-) Erase the protected block will be ignored. During the command sequence, WP# should be statically held high or low.

Erase-Suspend/Erase-Resume Commands

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing one byte command sequence with Erase-Suspend command (B0H). The device automatically enters Read mode typically within 10 μ s after the Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ₂ toggling and DQ₆ at '1'. While in Erase-Suspend mode, a Word-Program operation is allowed except for the sector or block selected for Erase-Suspend.

To resume Sector-Erase or Block-Erase operation that has been suspended, the system must issue an Erase Resume command. The operation is executed by issuing one byte command sequence with an Erase Resume command (30H) at any address in the last Byte sequence.

Chip-Erase Operation

The SST39VF3201C/SST39VF3202C provide a Chip-Erase operation, which allows the user to erase the entire memory array to the '1' state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See [Table 7](#) for the command sequence, [Figure 10](#) for timing diagram and [Figure 25](#) for a flowchart. Any commands issued during the Chip-Erase operation are ignored. When WP# is low, any attempt to Chip-Erase will be ignored. During the command sequence, WP# should be statically held high or low.

Write Operation Status Detection

The SST39VF3201C/SST39VF3202C provide two software means to detect the completion of a Write (Program or Erase) cycle to optimize the system write cycle time. The software detection includes two Status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write Detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may get an erroneous result (i.e., valid data may appear to conflict with either DQ₇ or DQ₆). To prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ₇)

When the SST39VF3201C/SST39VF3202C are in the internal Program operation, any attempt to read DQ₇ will produce the complement of the true data. Once the Program operation is completed, DQ₇ will produce true data. Note that even though DQ₇ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent, successive Read cycles after an interval of 1 μ s. During internal Erase operation, any attempt to read DQ₇ will produce a '0'. Once the internal Erase operation is

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completed, DQ₇ will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or CE#) pulse. See [Figure 8](#) for Data# Polling timing diagram and [Figure 22](#) for a flowchart.

Toggle Bits (DQ₆ and DQ₂)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating '1's and '0's (i.e., toggling between '1' and '0'). When the internal Program or Erase operation is completed, the DQ₆ bit will stop toggling. The device is then ready for the next operation. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ₆) is valid after the rising edge of the sixth WE# (or CE#) pulse. DQ₆ will be set to '1' if a Read operation is attempted on an Erase-Suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ₆ will toggle.

An additional Toggle Bit is available on DQ₂, which can be used in conjunction with DQ₆ to check whether a particular sector is being actively erased or erase-suspended. [Table 3](#) shows detailed Status bits information. The Toggle Bit (DQ₂) is valid after the rising edge of the last WE# (or CE#) pulse of Write operation. See [Figure 9](#) for Toggle Bit timing diagram and [Figure 22](#) for a flowchart.

TABLE 3: WRITE OPERATION STATUS

Status		DQ ₇ ⁽¹⁾	DQ ₆ ⁽¹⁾	DQ ₂ ⁽¹⁾	RY/BY#
Normal Operation	Standard Program	DQ ₇ #	Toggle	No Toggle	0
	Standard Erase	0	Toggle	Toggle	0
Erase-Suspend Mode	Read from Erase-Suspended Sector/Block	1	1	Toggle	1
	Read from Non- Erase-Suspended Sector/Block	Data	Data	Data	1
	Program	DQ ₇ #	Toggle	N/A	0

Note 1: DQ₇, DQ₆ and DQ₂ require a valid address when reading status information.

Ready/Busy# (RY/BY#)

The devices include a Ready/Busy# (RY/BY#) output signal. RY/BY# is an open-drain output pin that indicates whether an Erase or Program operation is in progress. Since RY/BY# is an open-drain output, it allows several devices to be tied in parallel to VDD via an external pull-up resistor. After the rising edge of the final WE# pulse in the command sequence, the RY/BY# status is valid.

When RY/BY# is actively pulled low, it indicates that an Erase or Program operation is in progress. When RY/BY# is high (Ready), the devices may be read or left in Standby mode.

Data Protection

The SST39VF3201C/SST39VF3202C provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

VDD Power Up/Down Detection: The Write operation is inhibited when VDD is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST39VF3202C supports top hardware block protection, which protects the top two 4-KWord blocks of the device. The SST39VF3201C supports bottom hardware block protection, which protects the bottom two 4-KWord blocks of the device. The Boot Block address ranges are described in [Table 4](#). Program and Erase operations are prevented on the two 4-KWord blocks when WP# is low. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

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TABLE 4: BOOT BLOCK ADDRESS RANGES

Product	Address Range
Bottom Boot Block SST39VF3201C	000000H-001FFFFH
Top Boot Block SST39VF3202C	1FE000H-1FFFFFFH

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least TRP, any in-progress operation will terminate and return to Read mode. When no internal Program/Erase operation is in progress, a minimum period of TRHR is required after RST# is driven high before a valid Read can take place (see [Figure 17](#)).

The Erase or Program operation that has been interrupted needs to be re-initiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST39VF3201C/SST39VF3202C provide the JEDEC approved Software Data Protection scheme for all data alteration operations (i.e., Program and Erase). Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations (e.g., during system power-up or power-down). Any Erase operation requires the inclusion of six-byte sequence. These devices are shipped with the Software Data Protection permanently enabled. See [Table 7](#) for the specific software command codes. During the SDP command sequence, invalid commands will abort the device to Read mode within TRC. The contents of DQ₁₅-DQ₈ can be VIL or VIH, but no other value, during any SDP command sequence.

Common Flash Memory Interface (CFI)

The SST39VF3201C/SST39VF3202C also contain the CFI information to describe the characteristics of the device. To enter CFI Query mode, the system must write the three-byte sequence, same as product ID entry command with 98H (CFI Query command) to address 555H in the last byte sequence. The system can also enter CFI Query mode by using the one-byte sequence with 55H on Address and 98H on Data Bus. Once the device enters CFI Query mode, the system can read CFI data at the addresses given in [Table 8](#) through [Table 10](#). The system must write the CFI Exit command to return to Read mode from CFI Query mode.

Product Identification

The Product Identification mode identifies the devices as the SST39VF3201C and SST39VF3202C and the manufacturer as Microchip. This mode may be accessed through software operations. Users may use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see [Table 7](#) for software operation, [Figure 13](#) for the Software ID Entry and Read timing diagram and [Figure 23](#) for the Software ID Entry command sequence flowchart.

TABLE 5: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST39VF3201C	0001H	235F
SST39VF3202C	0001H	235E

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Product Identification Mode Exit/CFI Mode Exit

To return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to Read mode. This command may also be used to reset the device to Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally (e.g., not read correctly). Note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See [Table 7](#) for software command codes, [Figure 15](#) for timing waveform and [Figure 23](#) and [Figure 24](#) for flowcharts.

Security ID

The SST39VF3201C/SST39VF3202C devices offer a 136-word Security ID space. The Secure ID space is divided into two segments: one factory-programmed segment and one user-programmed segment. The first segment is programmed and locked at Microchip with a random 128-bit number. The 128-word user segment is left unprogrammed for the customer to program as desired.

To program the user segment of the Security ID, the user must use the Security ID Word-Program command. To detect end-of-write for the SEC ID, read the toggle bits. Do not use Data# Polling. Once this is complete, the Sec ID should be locked using the User Sec ID Program Lock-Out. This disables any future corruption of this space. Note that regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased.

The Secure ID space can be queried by executing a three-byte command sequence with Enter Sec ID command (88H) at address 555H in the last byte sequence. To exit this mode, the Exit Sec ID command should be executed. Refer to [Table 7](#) for further details.

OPERATIONS

TABLE 6: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ	Address
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}	A _{IN}
Program	V _{IL}	V _{IH}	V _{IL}	D _{IN}	A _{IN}
Erase	V _{IL}	V _{IH}	V _{IL}		Sector or block address, XXH for Chip-Erase
Standby	V _{IH}	X	X	High-Z	X
Write Inhibit	X	V _{IL}	X	High-Z/ D _{OUT}	X
	X	X	V _{IH}	High-Z/ D _{OUT}	X
Product Identification					
Software Mode	V _{IL}	V _{IL}	V _{IH}		See Table 7
Note 1: X can be V _{IL} or V _{IH} , but no other value.					

SST39VF3201C/SST39VF3202C

TABLE 7: SOFTWARE COMMAND SEQUENCE

Command Sequence	1 st Bus Write Cycle		2 nd Bus Write Cycle		3 rd Bus Write Cycle		4 th Bus Write Cycle		5 th Bus Write Cycle		6 th Bus Write Cycle	
	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾
Word Program	555H	AAH	2AAH	55H	555H	A0H	WA ⁽³⁾	Data				
Sector Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA _X ⁽⁴⁾	50H
Block Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA _X ⁽⁴⁾	30H
Chip Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Erase Suspend	XXXXH	B0H										
Erase Resume	XXXXH	30H										
Query Sec ID ⁽⁵⁾	555H	AAH	2AAH	55H	555H	88H						
User Security ID Word Program	555H	AAH	2AAH	55H	555H	A5H	WA ⁽⁶⁾	Data				
User Security ID Program Lock-Out	555H	AAH	2AAH	55H	555H	85H	XXH ⁽⁶⁾	0000H				
Software ID Entry ^(7,8)	555H	AAH	2AAH	55H	555H	90H						
CFI Query Entry	555H	AAH	2AAH	55H	555H	98H						
CFI Query Entry	55H	98H										
Software ID Exit ^(9,10) /CFI Exit/Sec ID Exit	555H	AAH	2AAH	55H	555H	F0H						
Software ID Exit ^(9,10) /CFI Exit/Sec ID Exit	XXH	F0H										

SST39VF3201C/SST39VF3202C

TABLE 7: SOFTWARE COMMAND SEQUENCE (CONTINUED)

Command Sequence	1 st Bus Write Cycle		2 nd Bus Write Cycle		3 rd Bus Write Cycle		4 th Bus Write Cycle		5 th Bus Write Cycle		6 th Bus Write Cycle	
	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾	Addr ⁽¹⁾	Data ⁽²⁾
<p>Note 1: Address format A₁₀-A₀ (Hex). Addresses A₁₁-A₂₀ can be V_{IL} or V_{IH}, but no other value, for Command sequence for SST39VF3201C/SST39VF3202C.</p> <p>2: DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, for Command sequence.</p> <p>3: WA = Program Word Address</p> <p>4: SA_X for Sector-Erase; uses A_{MS}-A₁₁ address lines BA_X, for Block-Erase; uses A_{MS}-A₁₅ address lines A_{MS} = Most Significant address A_{MS} = A₂₀ for SST39VF3201C/SST39VF3202C</p> <p>5: With A_{MS}-A₄ = 0; Sec ID is read with A₃-A₀ Microchip ID is read with A₃ = 0 (Address range = 000000H to 000007H) User ID is read with A₃ = 1 (Address range = 000008H to 000087H) Lock Status is read with A₇-A₀ = 0000FFH. Unlocked: DQ₃ = 1 / Locked: DQ₃ = 0</p> <p>6: Valid Word Addresses for Sec ID are from 000000H-000007H and 000008H to 000087H.</p> <p>7: The device does not remain in Software Product ID mode if powered down.</p> <p>8: For Manufacture ID With A_{MS}-A₀ = 0; Microchip Manufacturer ID = 00BFH is read</p> <p>For Device ID Device ID can be read in one cycle (address 01H) One-cycle method - With A_{MS}-A₁ = 0, A₀ = 1; Microchip39VF3201C/3202C Device ID = 235F/235E is read</p> <p>A_{MS} = Most Significant address A_{MS} = A₂₀ for SST39VF3201C/SST39VF3202C</p> <p>9: Both Software ID Exit operations are equivalent.</p> <p>10: If users never lock after programming, Sec ID can be programmed over the previously unprogrammed bits (data=1) using the Sec ID mode again (the programmed '0' bits cannot be reversed to '1'). Valid Word-Addresses for Sec ID are from 000000H-000007H and 000008H to 000087H.</p>												

TABLE 8: CFI QUERY IDENTIFICATION STRING (1) FOR SST39VF3201C/SST39VF3202C

Address	Data	Data
10H	0051H	Query Unique ASCII string "QRY"
11H	0052H	
12H	0059H	
13H	0002H	Primary OEM command set
14H	0000H	
15H	0000H	Address for Primary Extended Table
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM extended Table (00H = none exists)
1AH	0000H	

Note 1: Refer to CFI publication 100 for more details.

SST39VF3201C/SST39VF3202C

TABLE 9: SYSTEM INTERFACE INFORMATION FOR SST39VF3201C/SST39VF3202C

Address	Data	Data
1BH	0027H	V _{DD} Min (Program/Erase); DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts
1CH	0036H	V _{DD} Max (Program/Erase); DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts
1DH	0000H	V _{PP} min. (00H = no V _{PP} pin)
1EH	0000H	V _{PP} max. (00H = no V _{PP} pin)
1FH	0003H	Typical time out for Word-Program 2 ^N μs (2 ³ = 8 μs)
20H	0000H	Typical time out for min. size buffer program 2 ^N μs (00H = not supported)
21H	0004H	Typical time out for individual Sector/Block-Erase 2 ^N ms (2 ⁴ = 16 ms)
22H	0005H	Typical time out for Chip-Erase 2 ^N ms (2 ⁵ = 32 ms)
23H	0001H	Maximum time out for Word-Program 2 ^N times typical (2 ¹ x 2 ³ = 16 μs)
24H	0000H	Maximum time out for buffer program 2 ^N times typical
25H	0001H	Maximum time out for individual Sector/Block-Erase 2 ^N times typical (2 ¹ x 2 ⁴ = 32 ms)
26H	0001H	Maximum time out for Chip-Erase 2 ^N times typical (2 ¹ x 2 ⁵ = 64 ms)

TABLE 10: DEVICE GEOMETRY FOR SST39VF3201C

Address	Data	Data
27H	0016H	Device size = 2 ^N Bytes (16H = 22; 2 ²² = 4 MByte)
28H	0001H	Flash Device Interface description; 0001H = x16-only asynchronous interface
29H	0000H	
2AH	0000H	
2BH	0000H	Maximum number of bytes in multi-byte write = 2 ^N (00H = not supported)
2CH	0002H	Number of Erase Sector/Block sizes supported by device
2DH	0007H	Erase Block1 region information
2EH	0000H	
2FH	0020H	
30H	0000H	
31H	003EH	Erase Block2 region information
32H	0000H	
33H	0000H	
34H	0001H	
35H	0000H	Erase Block3 region information
36H	0000H	
37H	0000H	
38H	0000H	
39H	0000H	Erase Block4 region information
3AH	0000H	
3BH	0000H	
3CH	0000H	

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TABLE 11: DEVICE GEOMETRY FOR SST39VF3202C

Address	Data	Data
27H	0016H	Device size = 2^N Bytes (16H = 22; 2^{22} = 4 MByte)
28H	0001H	Flash Device Interface description; 0001H = x16-only asynchronous interface
29H	0000H	
2AH	0000H	Maximum number of bytes in multi-byte write = 2^N (00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Sector/Block sizes supported by device
2DH	003EH	Erase Block1 region information
2EH	0000H	
2FH	0000H	
30H	0001H	
31H	0007H	Erase Block2 region information
32H	0000H	
33H	0020H	
34H	0000H	
35H	0000H	Erase Block3 region information
36H	0000H	
37H	0000H	
38H	0000H	
39H	0000H	Erase Block4 region information
3AH	0000H	
3BH	0000H	
3CH	0000H	

SST39VF3201C/SST39VF3202C

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias -55°C to +125°C
Storage Temperature -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential..... -2.0V to V_{DD}+0.2V
Voltage on A₉ Pin to Ground Potential -0.5V to 13.2V
Package Power Dissipation Capability (T_A = 25°C)..... 1.0W
Surface Mount Solder Reflow Temperature +260°C for 10 seconds
Output Short Circuit Current⁽¹⁾ 50 mA

Note 1: Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 12: OPERATING RANGES

Range	Ambient Temperature	V _{DD}
Industrial	-40°C to +85°C	2.7V-3.6V

TABLE 13: AC CONDITIONS OF TEST⁽¹⁾

Input Rise/Fall Time	Output Load
5 ns	C _L = 30 pF

Note 1: See [Figure 19](#) and [Figure 20](#).

Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3V in less than 300 ms). If the V_{DD} ramp rate is slower than 1V per 100 ms, a hardware Reset is required. The recommended V_{DD} power-up to RESET# high time should be greater than 100 μs to ensure a proper Reset.

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FIGURE 4: POWER-UP DIAGRAM

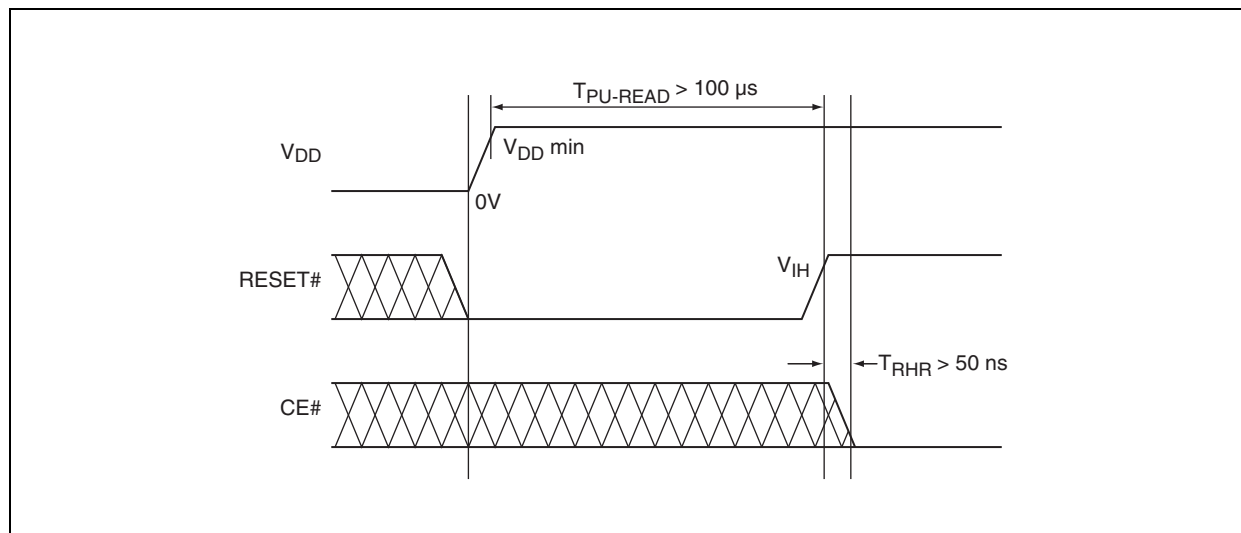


TABLE 14: DC OPERATING CHARACTERISTICS $V_{DD} = 2.7V-3.6V^{(1)}$

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{DD}	Power Supply Current				Address Input = $V_{ILT}/V_{IHT}^{(2)}$ at $f = 5$ MHz, $V_{DD} = V_{DD} \text{ Max}$
	Read ⁽³⁾	—	15	mA	$CE\# = V_{IL}$, $OE\# = WE\# = V_{IH}$, all I/Os open
	Program and Erase	—	45	mA	$CE\# = WE\# = V_{IL}$, $OE\# = V_{IH}$
I_{SB}	Standby V_{DD} Current	—	50	μA	$CE\# = V_{IHC}$, $V_{DD} = V_{DD} \text{ Max}$
I_{ALP}	Auto Low Power	—	50	μA	$CE\# = V_{ILC}$, $V_{DD} = V_{DD} \text{ Max}$ All inputs = V_{SS} or V_{DD} , $WE\# = V_{IHC}$
I_{LI}	Input Leakage Current	—	1	μA	$V_{IN} = \text{GND to } V_{DD}$, $V_{DD} = V_{DD} \text{ Max}$
I_{LIW}	Input Leakage Current on WP# pin and RST#	—	10	μA	$WP\# = \text{GND to } V_{DD}$ or $RST\# = \text{GND to } V_{DD}$
I_{LO}	Output Leakage Current	—	1	μA	$V_{OUT} = \text{GND to } V_{DD}$, $V_{DD} = V_{DD} \text{ Max}$
V_{IL}	Input Low Voltage	—	0.8	V	$V_{DD} = V_{DD} \text{ Min}$
V_{ILC}	Input Low Voltage (CMOS)	—	0.3	V	$V_{DD} = V_{DD} \text{ Max}$
V_{IH}	Input High Voltage	$0.7V_{DD}$	—	V	$V_{DD} = V_{DD} \text{ Max}$
V_{IHC}	Input High Voltage (CMOS)	$V_{DD}-0.3$	—	V	$V_{DD} = V_{DD} \text{ Max}$
V_{OL}	Output Low Voltage	—	0.2	V	$I_{OL} = 100 \mu A$, $V_{DD} = V_{DD} \text{ Min}$
V_{OH}	Output High Voltage	$V_{DD}-0.2$	—	V	$I_{OH} = -100 \mu A$, $V_{DD} = V_{DD} \text{ Min}$

Note 1: Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and $V_{DD} = 3V$. Not 100% tested.

2: See Figure 19.

3: The I_{DD} current listed is typically less than 2 mA/MHz, with $OE\#$ at V_{IH} . Typical V_{DD} is 3V.

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TABLE 15: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
TPU-READ ⁽¹⁾	Power-up to Read Operation	100	μs
TPU-WRITE ⁽¹⁾	Power-up to Program/Erase Operation	100	μs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 16: CAPACITANCE (TA = 25°C, F = 1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
CI/O ⁽¹⁾	I/O Pin Capacitance	V _{I/O} = 0V	10 pF
CIN ⁽¹⁾	Input Capacitance	V _{IN} = 0V	10 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 17: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
NEND ^(1,2)	Endurance	10,000	Cycles	JEDEC Standard A117
TDR ⁽¹⁾	Data Retention	100	Years	JEDEC Standard A103
ILTH ⁽¹⁾	Latch-Up	100 - IDD	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2: NEND endurance rating is qualified as a 10,000 cycle minimum for the whole device, A sector- or block-level rating would result in higher minimum specification.

AC CHARACTERISTICS

TABLE 18: READ CYCLE TIMING PARAMETERS VDD = 2.7V-3.6V

Symbol	Parameter	Min	Max	Units
TRC	Read Cycle Time	70	—	ns
TCE	Chip Enable Access Time	—	70	ns
TAA	Address Access Time	—	70	ns
TOE	Output Enable Access Time	—	35	ns
TCLZ ⁽¹⁾	CE# Low to Active Output	0	—	ns
TOLZ ⁽¹⁾	OE# Low to Active Output	0	—	ns
TCHZ ⁽¹⁾	CE# High to High-Z Output	—	16	ns
TOHZ ⁽¹⁾	OE# High to High-Z Output	—	16	ns
TOH ⁽¹⁾	Output Hold from Address Change	0	—	ns
TRP ⁽¹⁾	RST# Pulse Width	500	—	ns
TRHR ⁽¹⁾	RST# High before Read	50	—	ns
TRY ^(1,2)	RST# Pin Low to Read Mode	—	20	μs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2: This parameter applies to Sector-Erase, Block-Erase and Program operations. This parameter does not apply to Chip-Erase operations.

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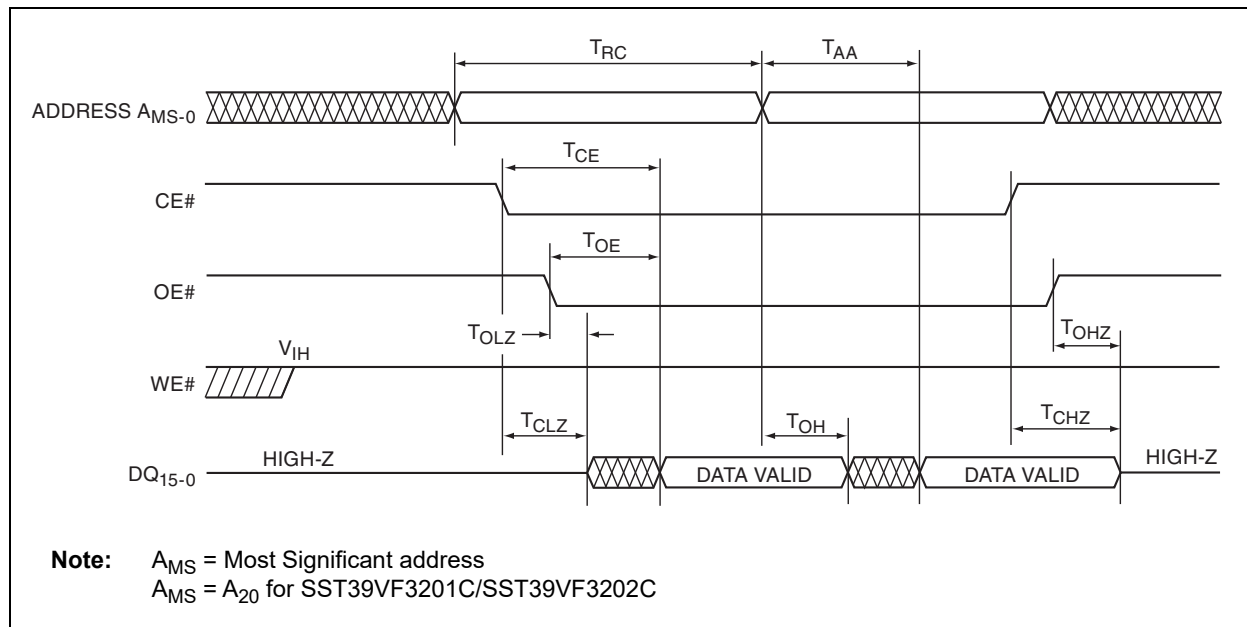
TABLE 19: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
TBP	Word-Program Time	—	10	μs
TAS	Address Setup Time	0	—	ns
TAH	Address Hold Time	30	—	ns
TCS	WE# and CE# Setup Time	0	—	ns
TCH	WE# and CE# Hold Time	0	—	ns
TOES	OE# High Setup Time	0	—	ns
TOEH	OE# High Hold Time	10	—	ns
TCP	CE# Pulse Width	40	—	ns
TWP	WE# Pulse Width	40	—	ns
TWPH ⁽¹⁾	WE# Pulse Width High	30	—	ns
TCPH ⁽¹⁾	CE# Pulse Width High	30	—	ns
TDS	Data Setup Time	30	—	ns
TDH ⁽¹⁾	Data Hold Time	0	—	ns
TIDA ⁽¹⁾	Software ID Access and Exit Time	—	150	ns
TSE	Sector-Erase	—	25	ms
TBE	Block-Erase	—	25	ms
TSCE	Chip-Erase	—	50	ms
TBY ^(1,2)	RY/BY# Delay Time	90	—	ns
TBR ⁽¹⁾	Bus Recovery Time	—	0	μs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2: This parameter applies to Sector-Erase, Block-Erase and Program operations.

FIGURE 5: READ CYCLE TIMING DIAGRAM



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FIGURE 6: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

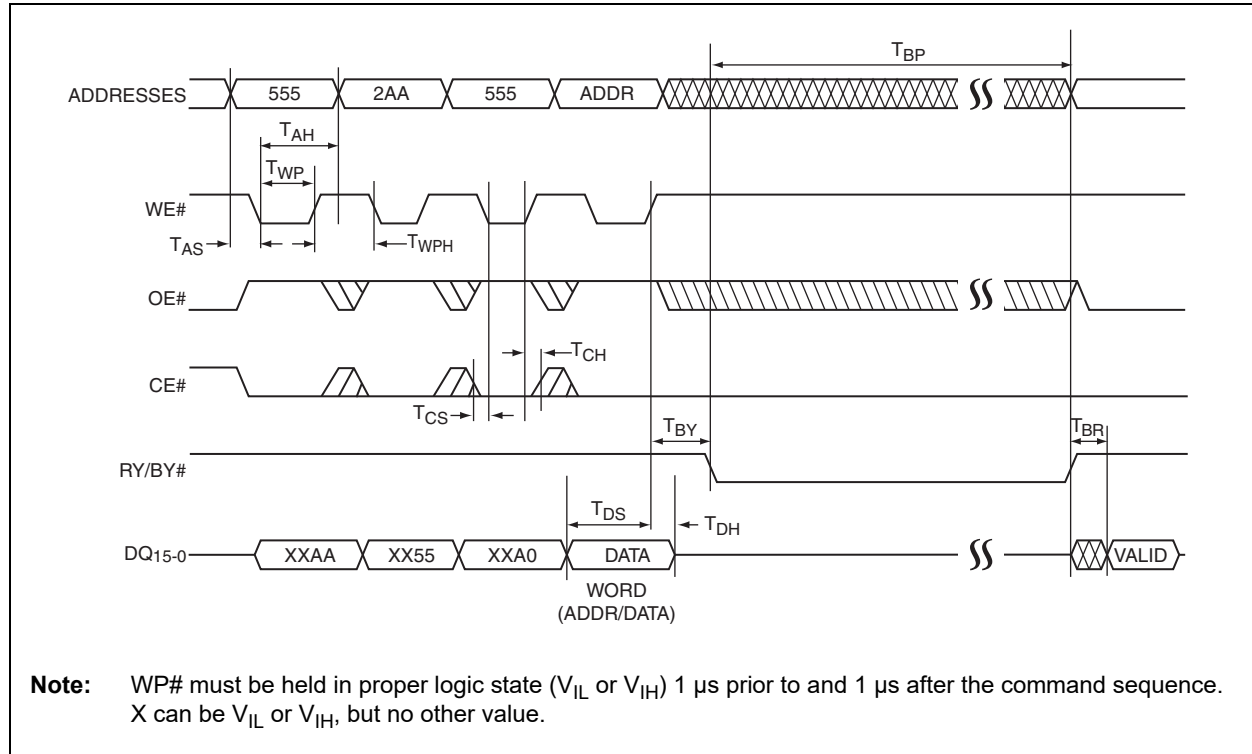
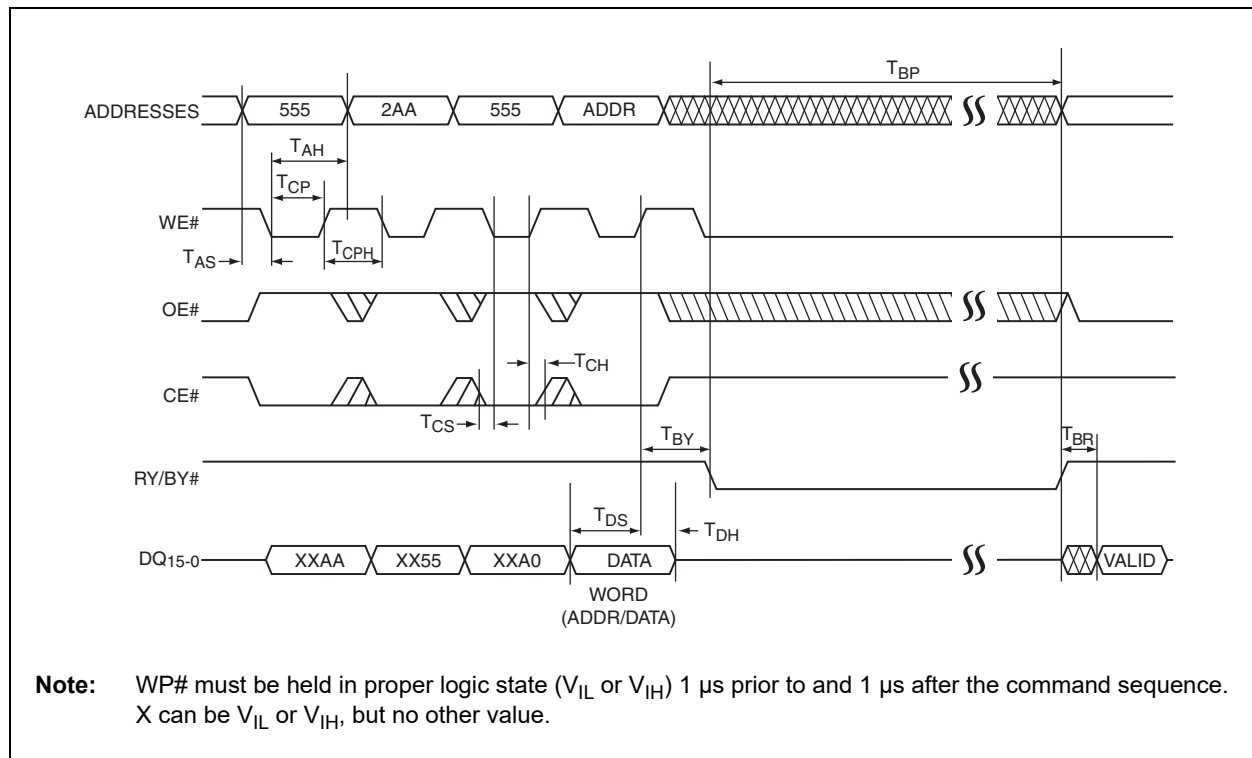


FIGURE 7: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



SST39VF3201C/SST39VF3202C

FIGURE 8: DATA# POLLING TIMING DIAGRAM

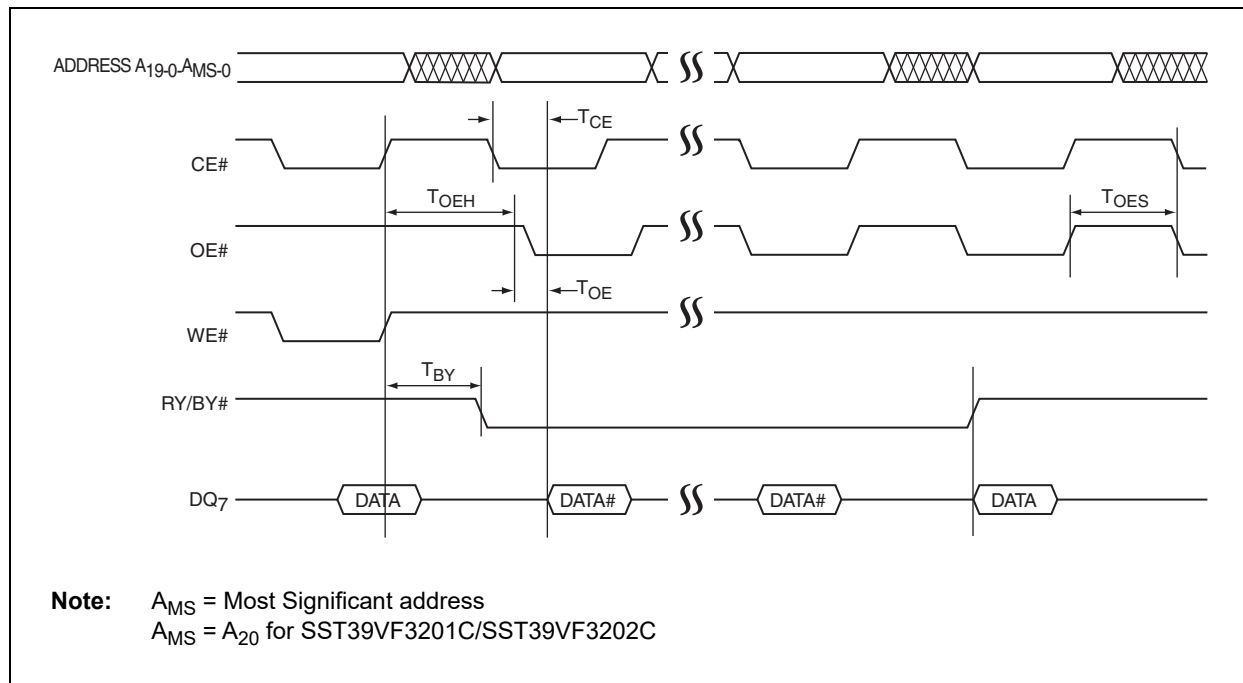
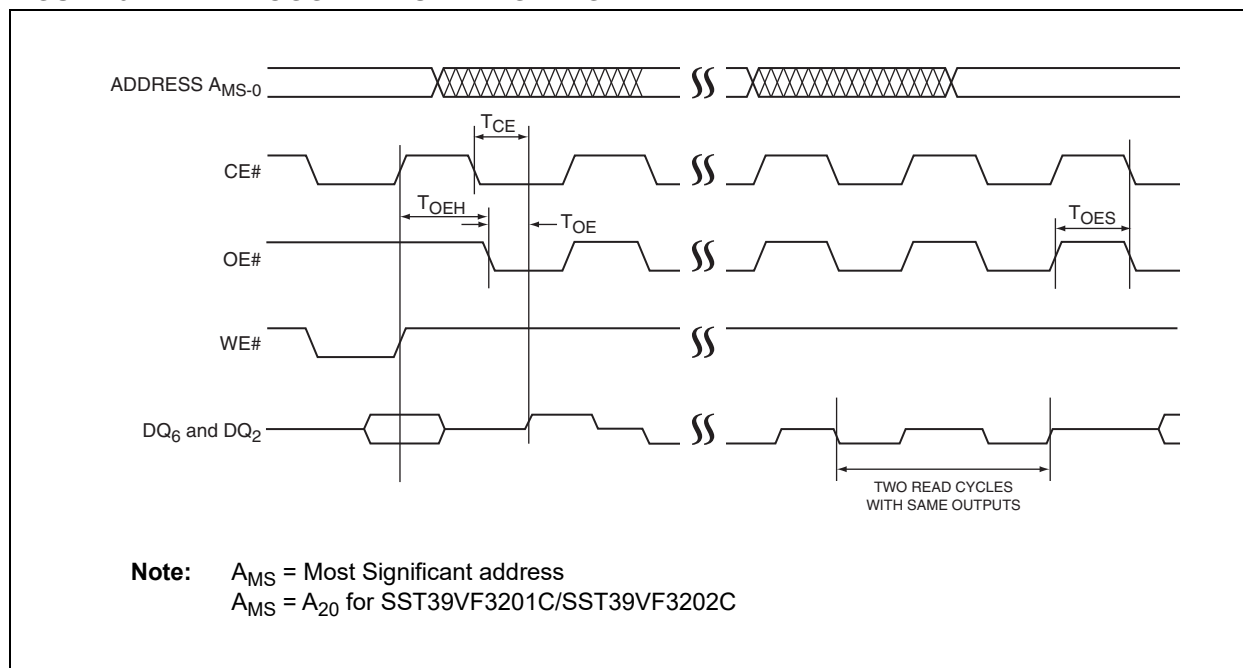


FIGURE 9: TOGGLE BITS TIMING DIAGRAM



SST39VF3201C/SST39VF3202C

FIGURE 10: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM

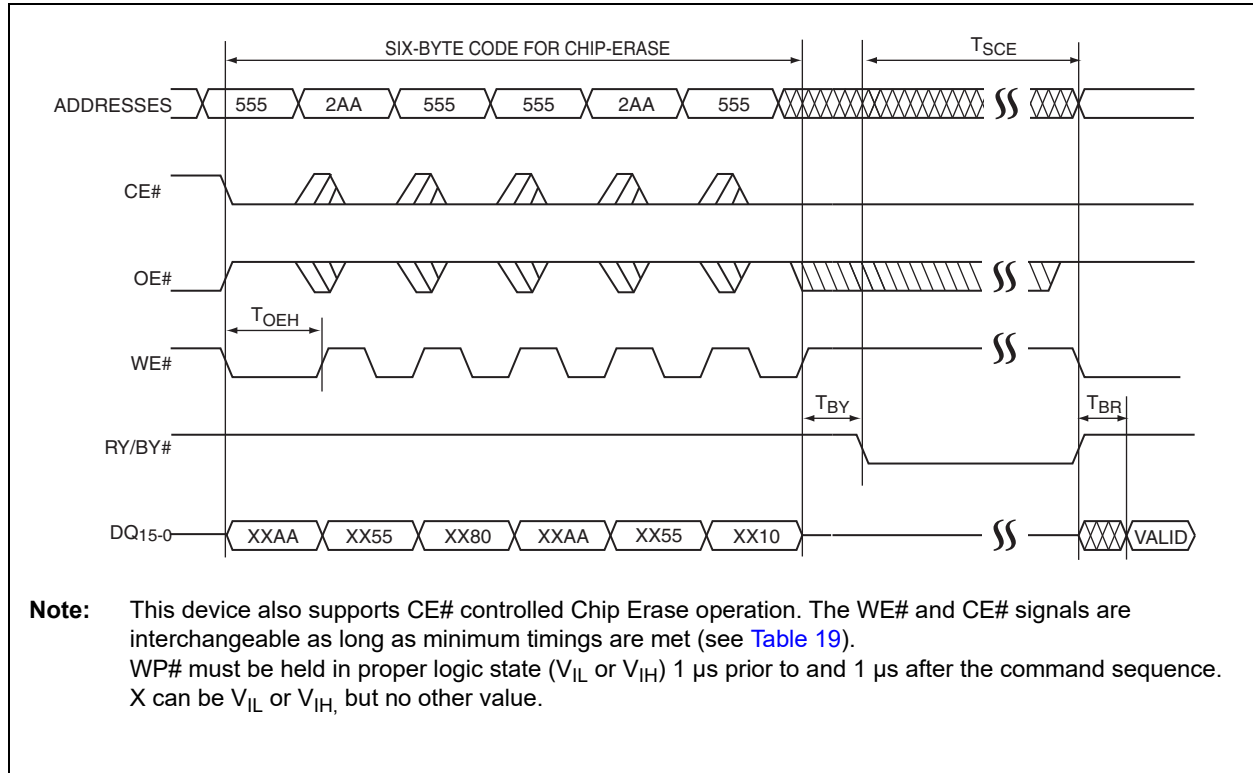
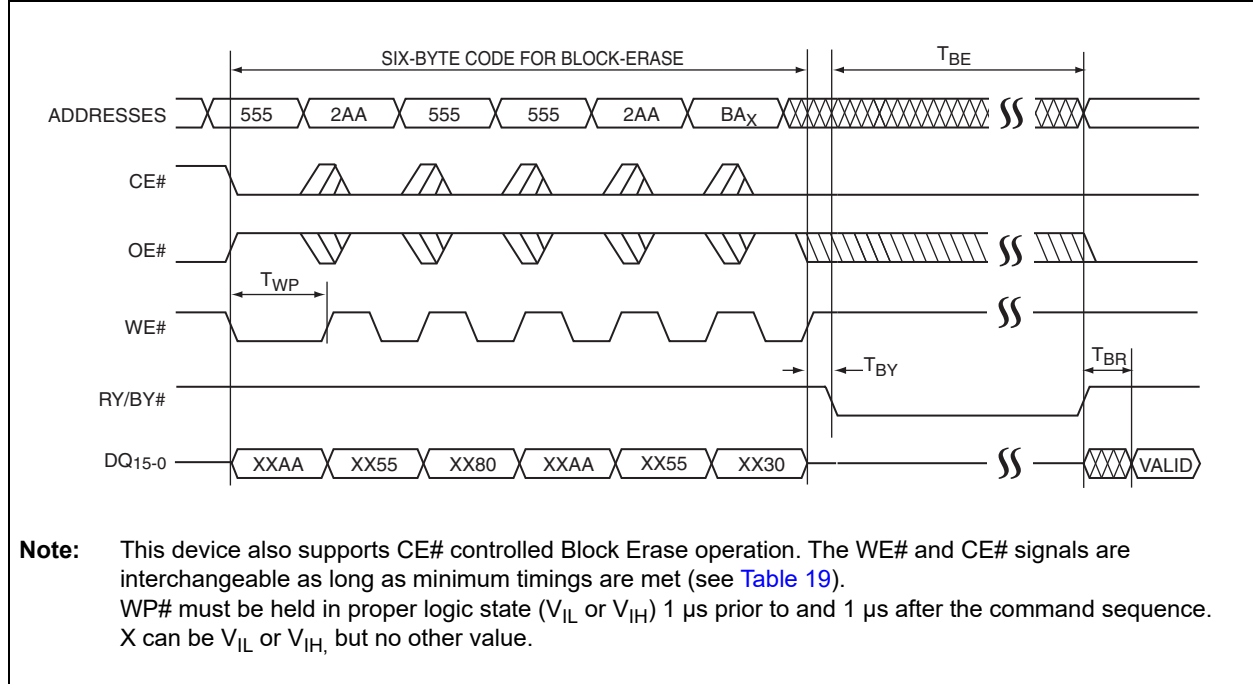


FIGURE 11: WE# CONTROLLED BLOCK ERASE TIMING DIAGRAM



SST39VF3201C/SST39VF3202C

FIGURE 12: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM

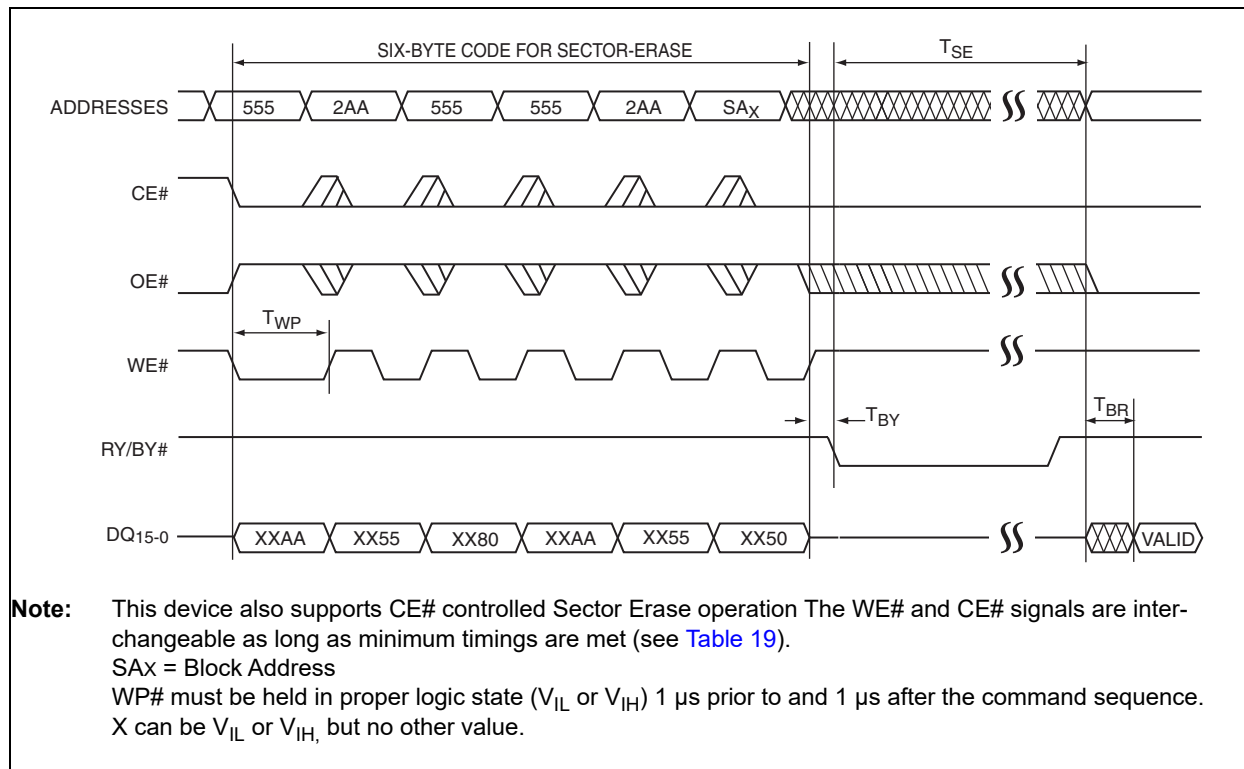
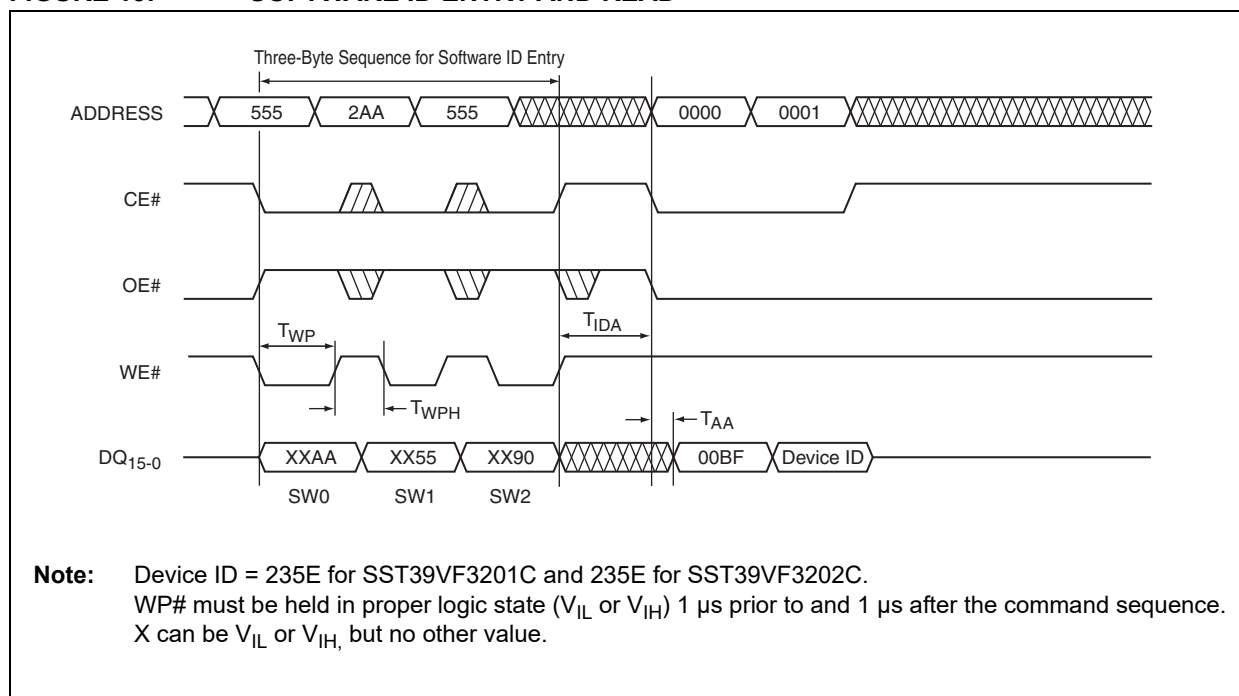


FIGURE 13: SOFTWARE ID ENTRY AND READ



SST39VF3201C/SST39VF3202C

FIGURE 14: CFI QUERY AND READ

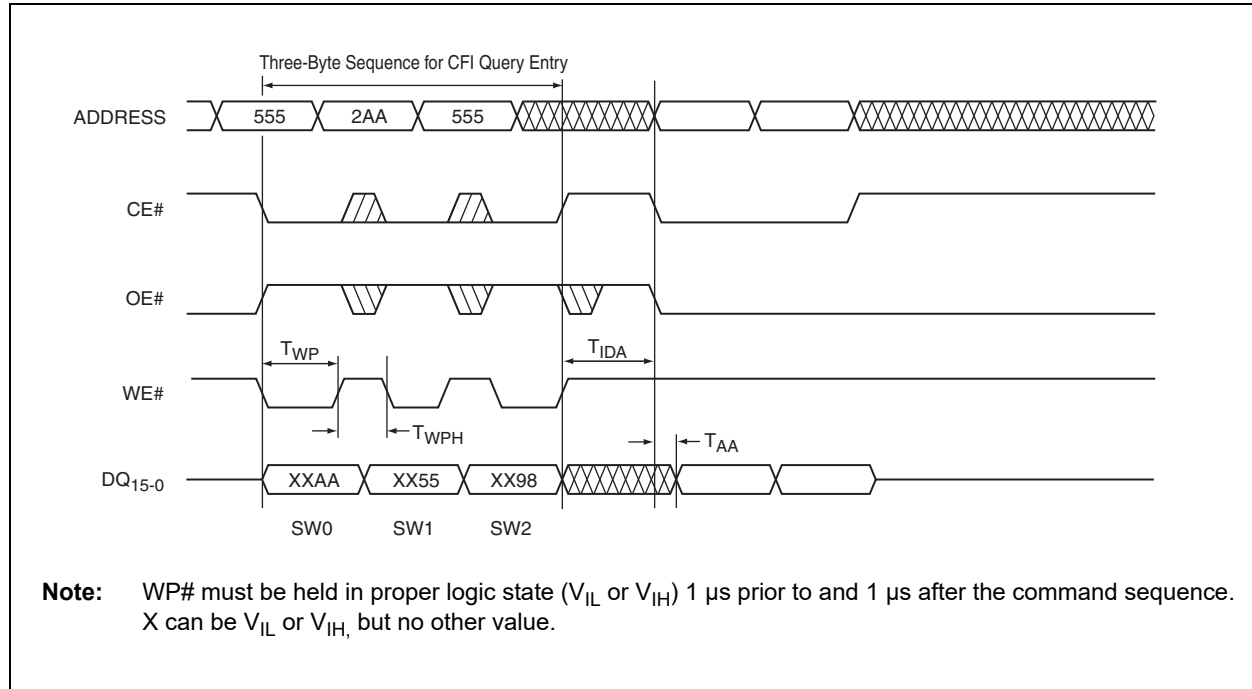
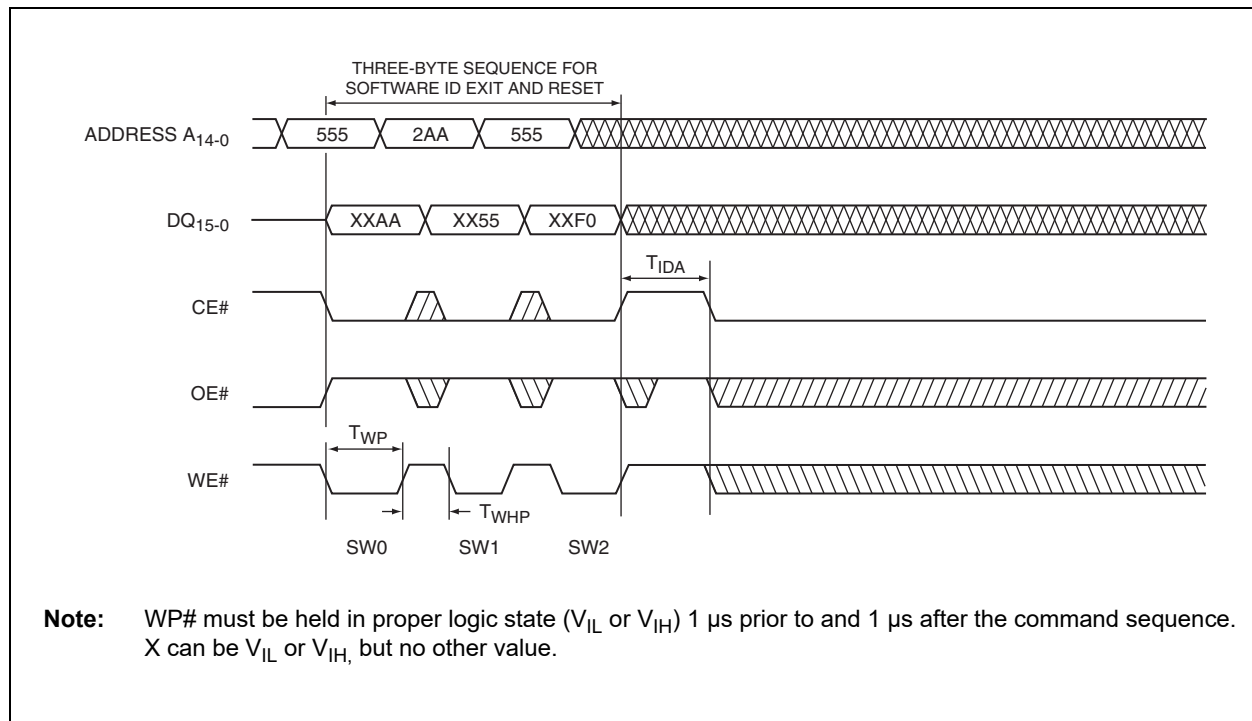


FIGURE 15: SOFTWARE ID EXIT/CFI EXIT



SST39VF3201C/SST39VF3202C

FIGURE 16: SEC ID ENTRY

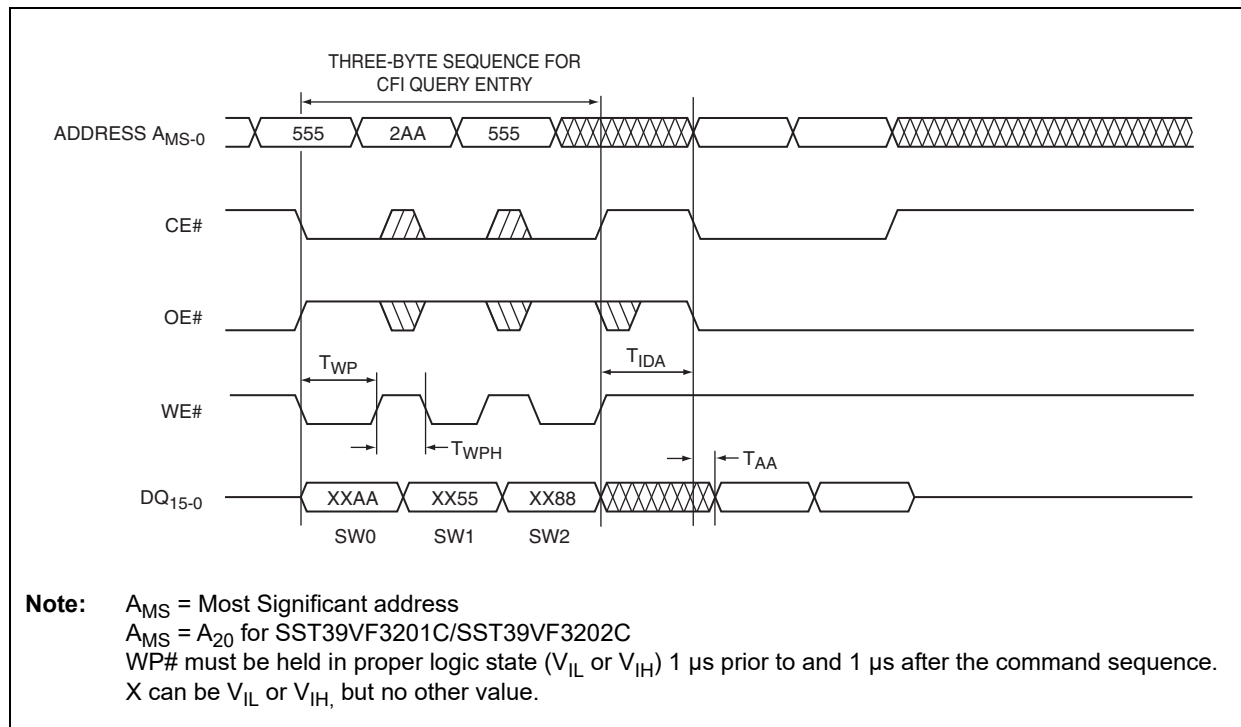
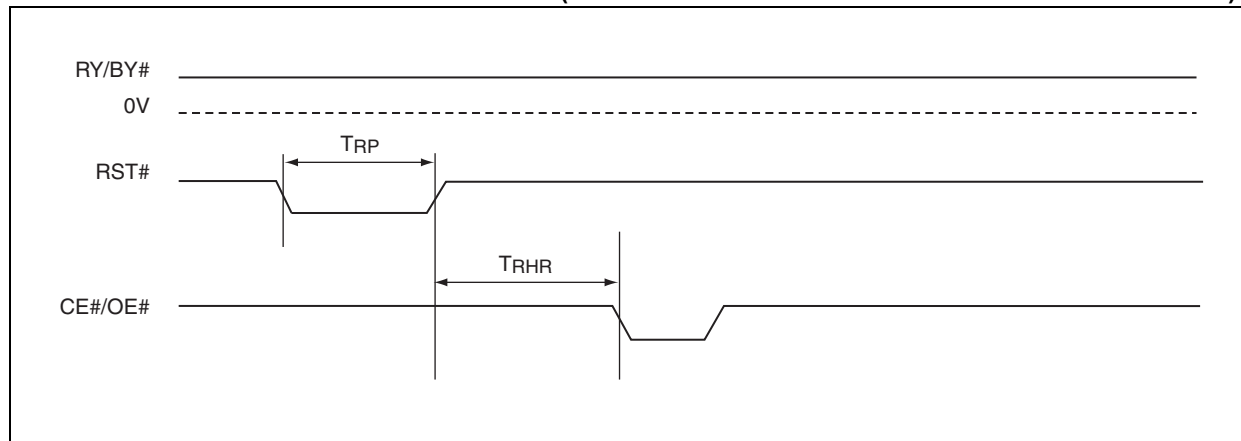


FIGURE 17: RST# TIMING DIAGRAM (WHEN NO INTERNAL OPERATION IS IN PROGRESS)



SST39VF3201C/SST39VF3202C

FIGURE 18: RST# TIMING DIAGRAM (DURING PROGRAM OR ERASE OPERATION)

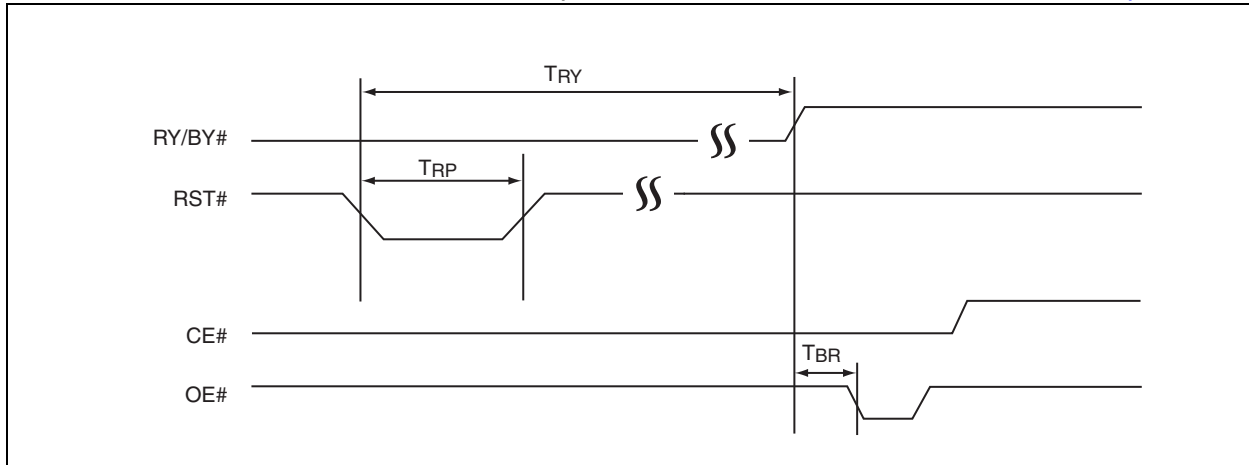


FIGURE 19: AC INPUT/OUTPUT REFERENCE WAVEFORMS

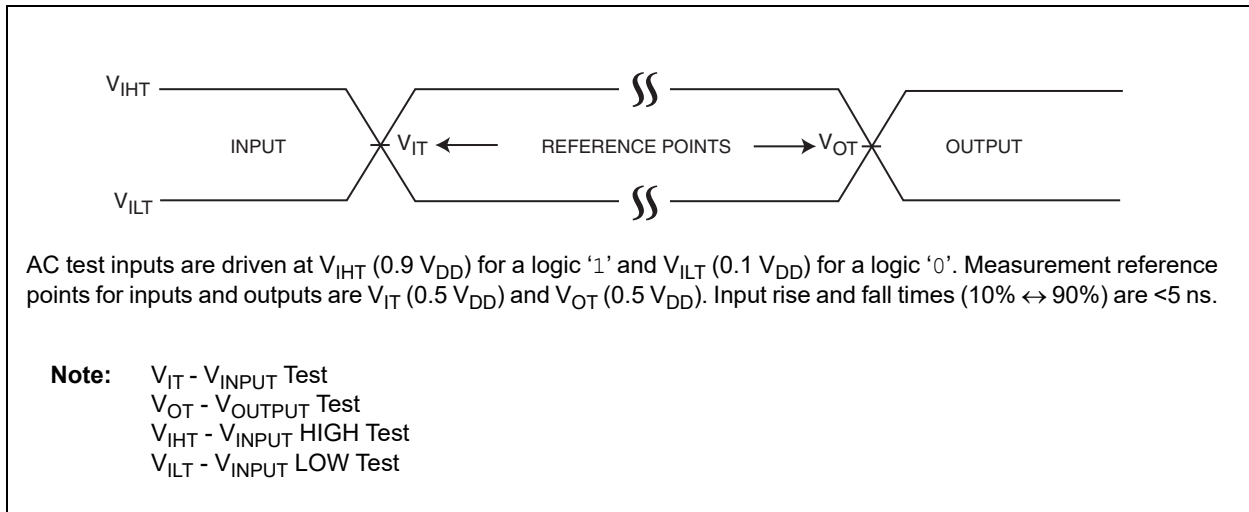
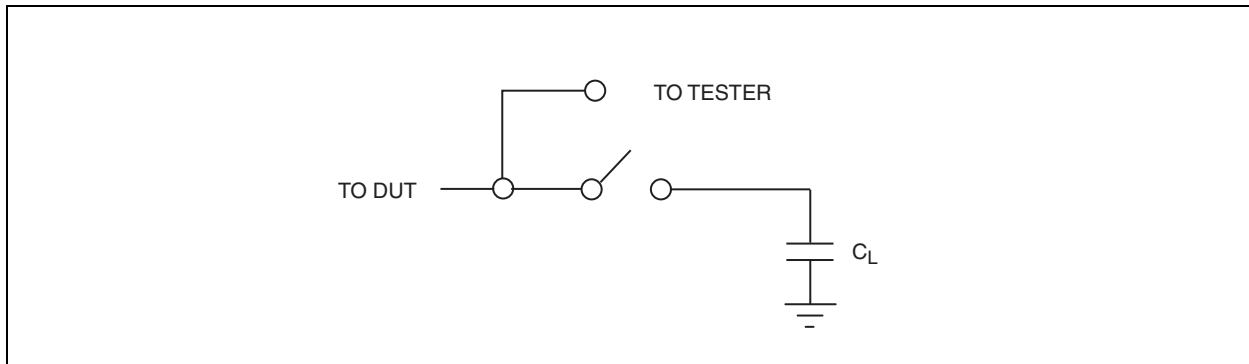
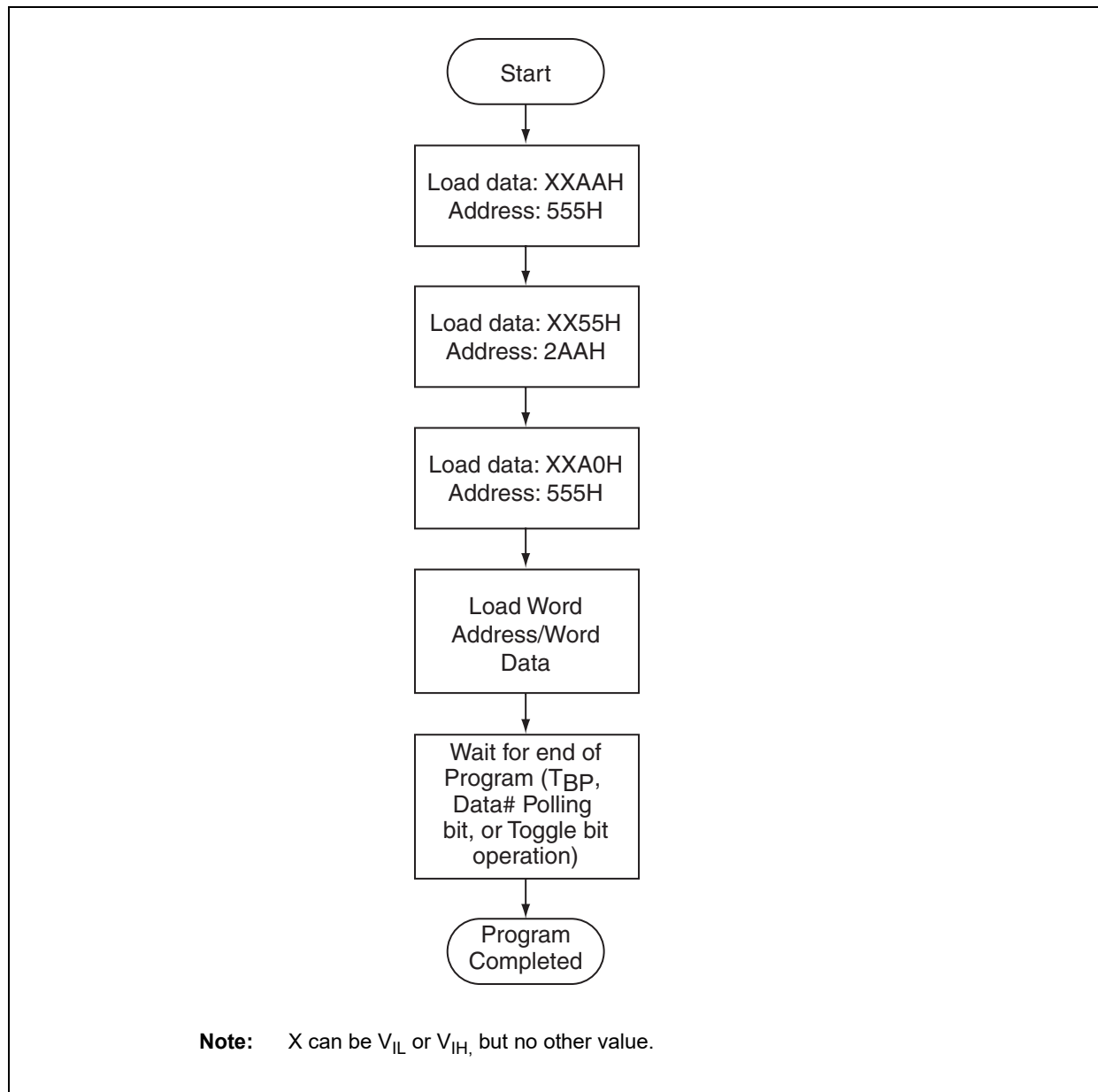


FIGURE 20: A TEST LOAD EXAMPLE



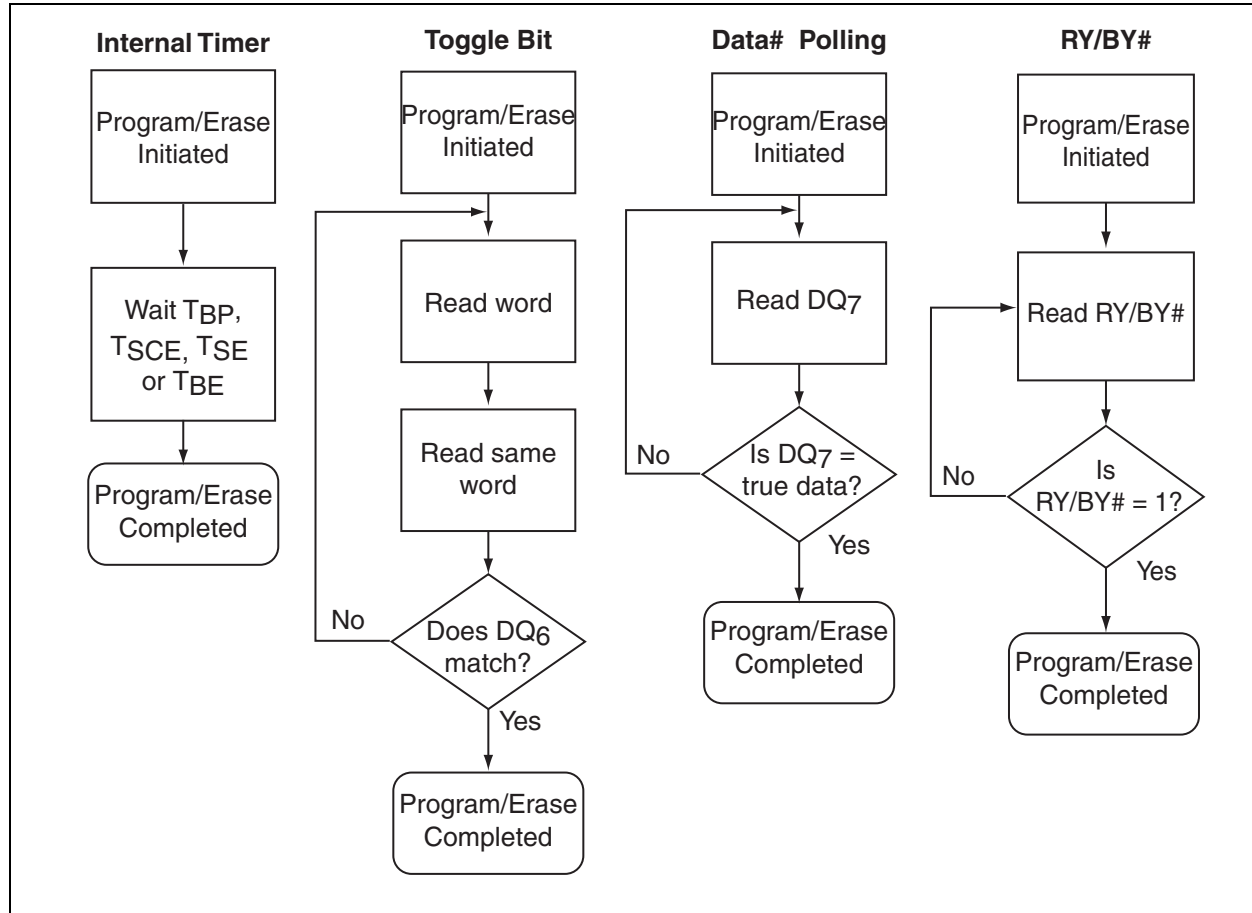
SST39VF3201C/SST39VF3202C

FIGURE 21: WORD PROGRAM ALGORITHM



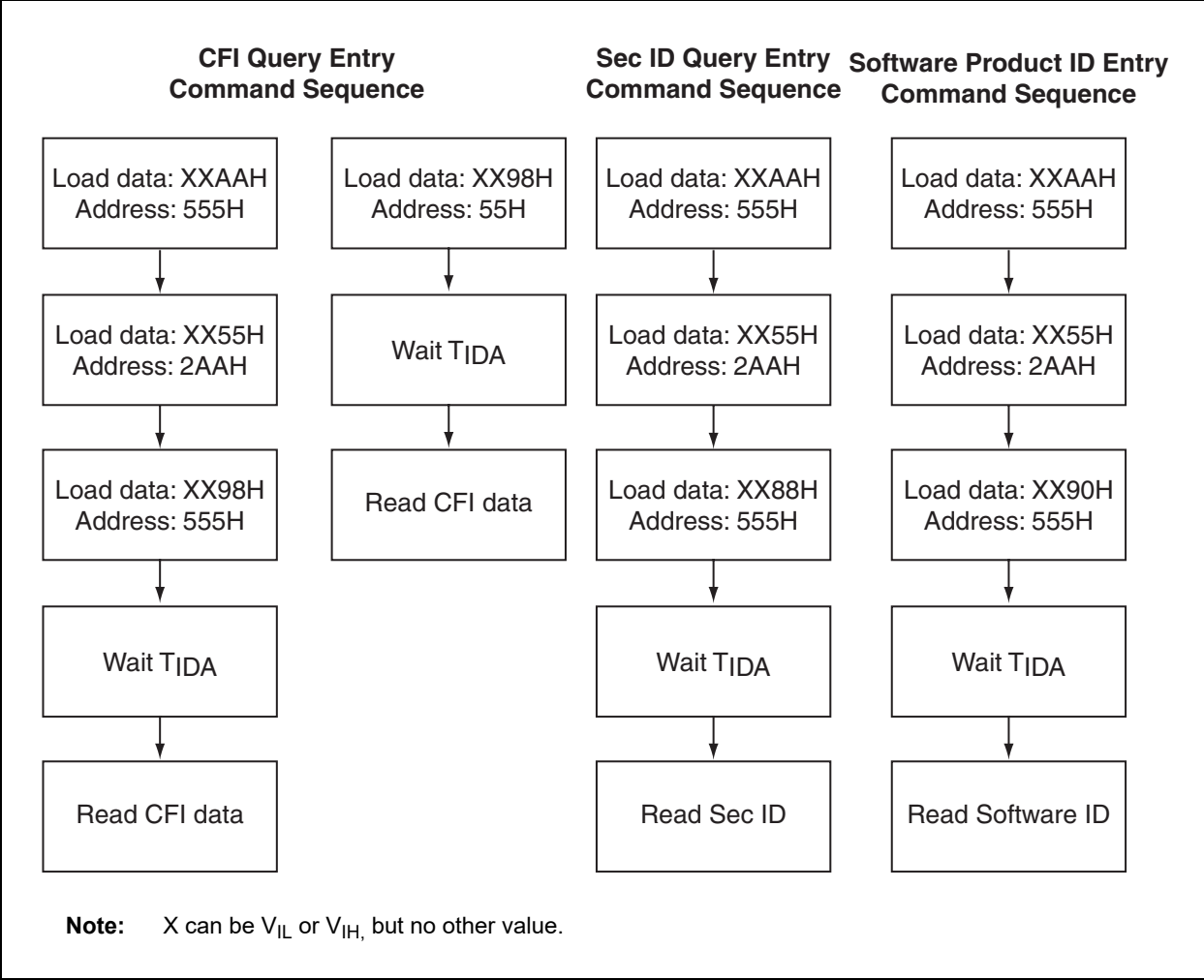
SST39VF3201C/SST39VF3202C

FIGURE 22: WAIT OPTIONS



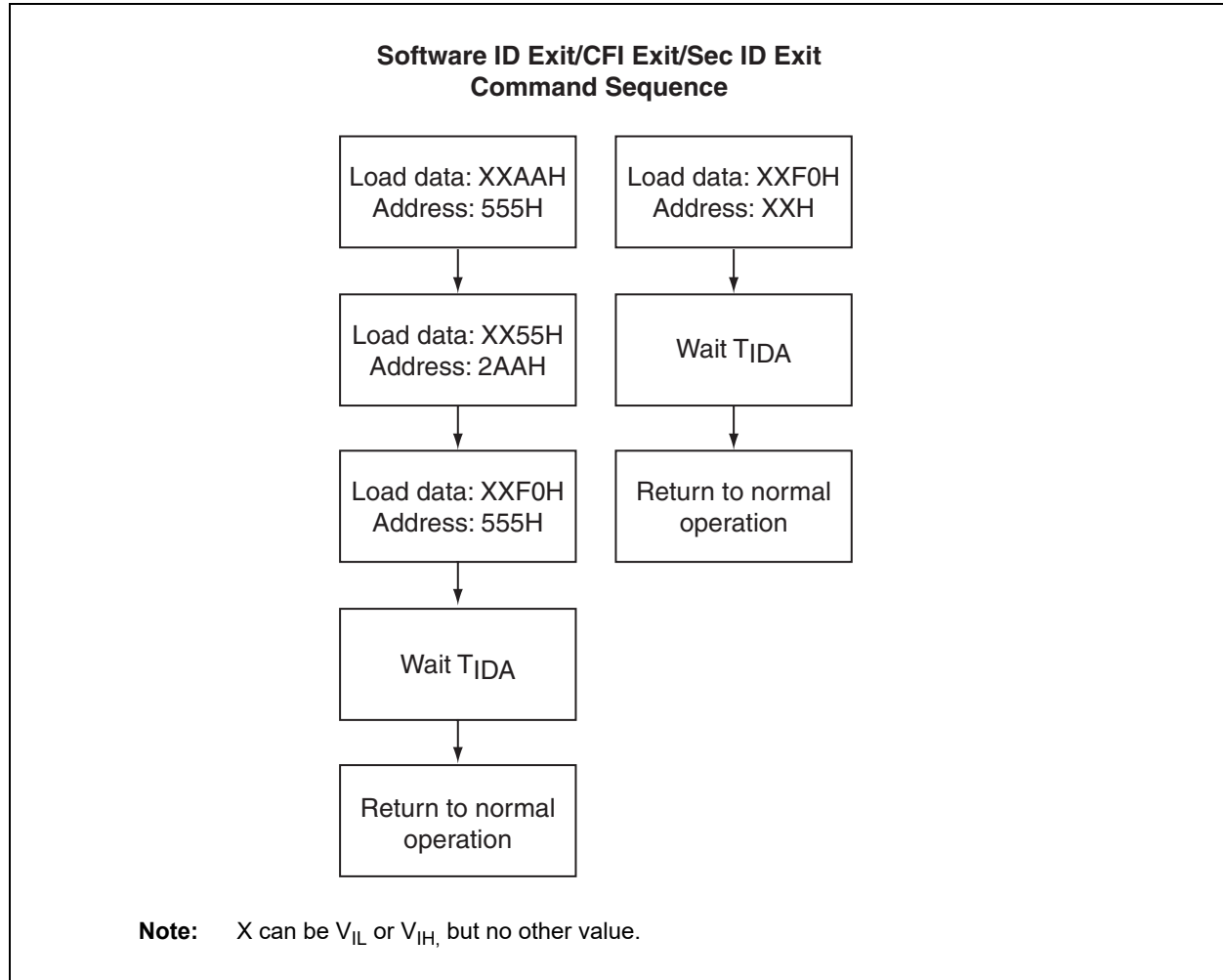
SST39VF3201C/SST39VF3202C

FIGURE 23: SOFTWARE ID/CFI ENTRY COMMAND FLOWCHARTS



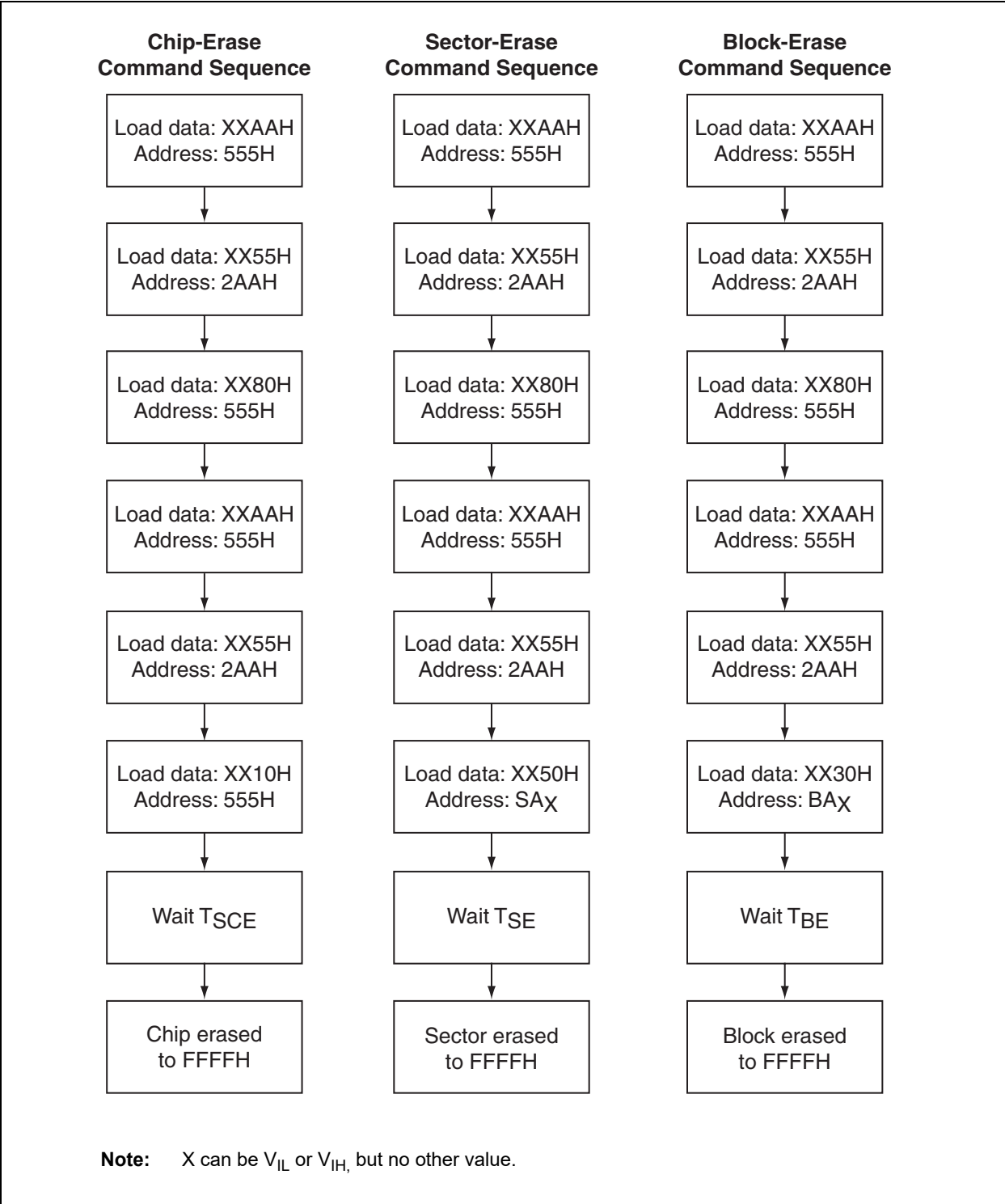
SST39VF3201C/SST39VF3202C

FIGURE 24: SOFTWARE ID/CFI EXIT COMMAND FLOWCHARTS



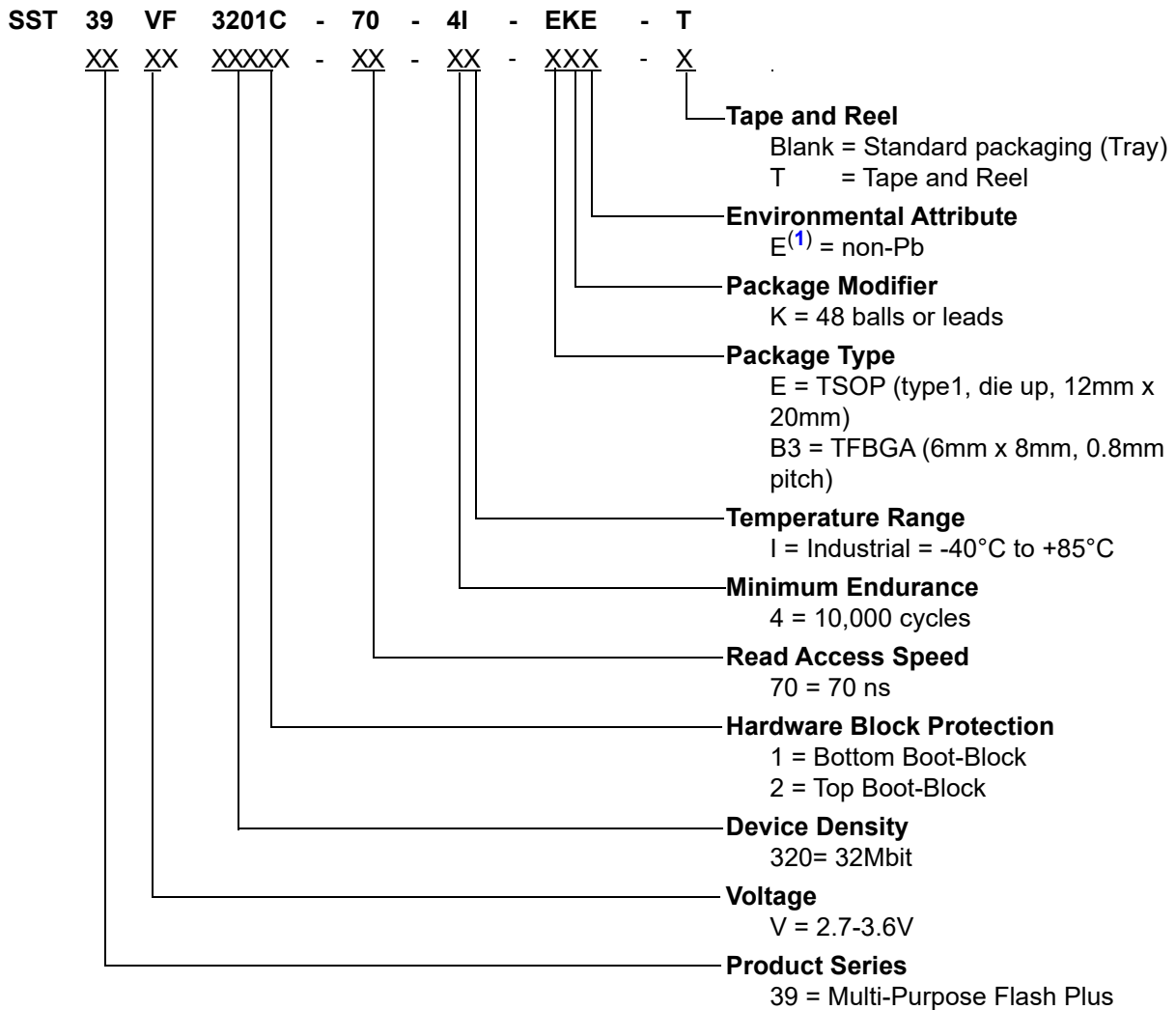
SST39VF3201C/SST39VF3202C

FIGURE 25: ERASE COMMAND SEQUENCE



SST39VF3201C/SST39VF3202C

PRODUCT ORDERING INFORMATION



Note 1: Environmental suffix “E” denotes non-Pb solder; non-Pb solder devices are “RoHS Compliant”.

VALID COMBINATIONS FOR SST39VF3201C

SST39VF3201C-70-4I-EKE SST39VF3201C-70-4I-B3KE
SST39VF3201C-70-4I-EKE-T SST39VF3201C-70-4I-B3KE-T

VALID COMBINATIONS FOR SST39VF3202C

SST39VF3202C-70-4I-EKE SST39VF3202C-70-4I-B3KE
SST39VF3202C-70-4I-EKE-T SST39VF3202C-70-4I-B3KE-T

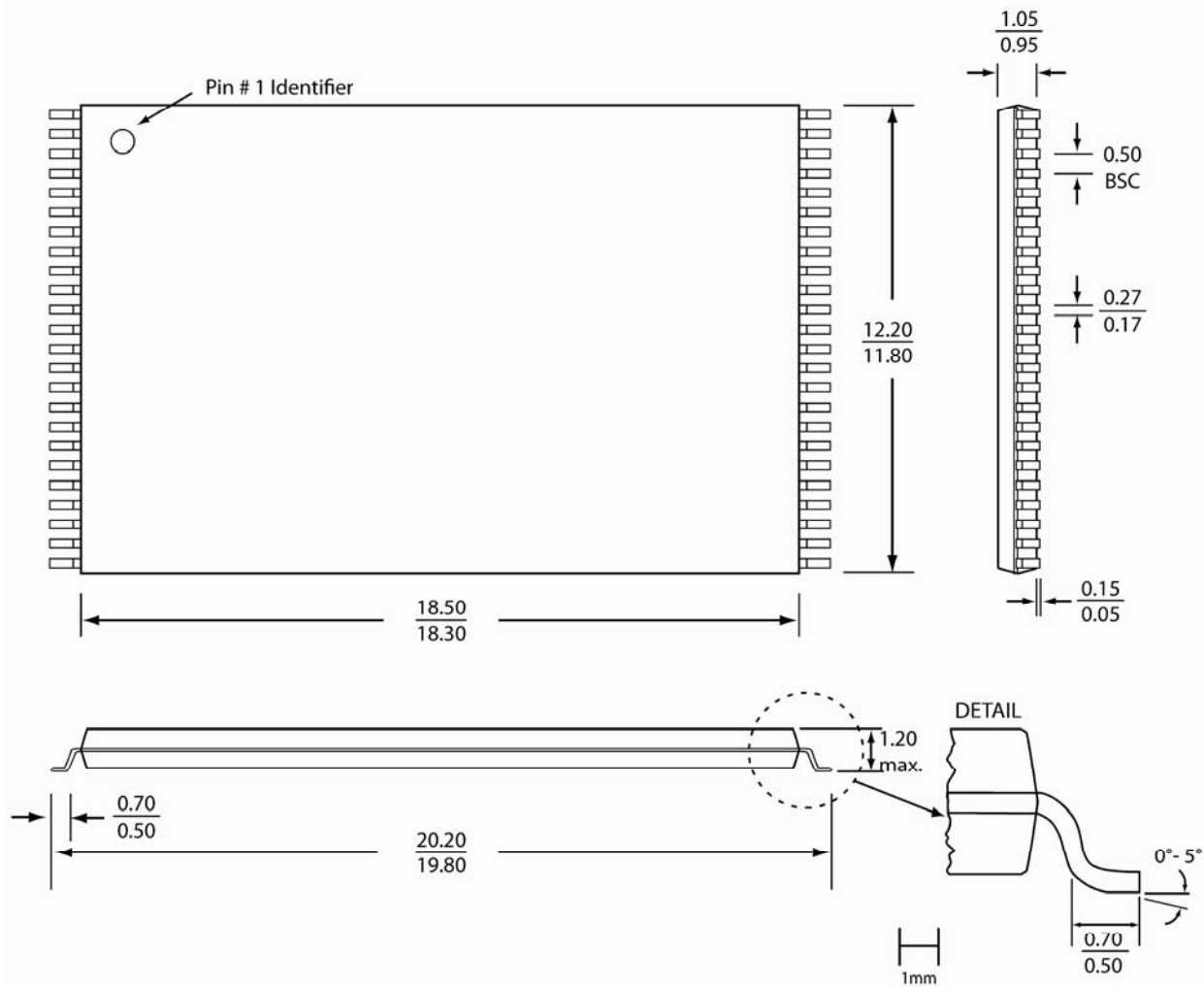
Note: Valid combinations are those products in mass production or will be in mass production. Consult your Microchip sales representative to confirm availability of valid combinations and to determine availability of new combinations.

SST39VF3201C/SST39VF3202C

Packaging Diagrams

48-Lead Thin Small Outline Package (EKE/F) - [TSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



48-tsop-EK-8

Note:

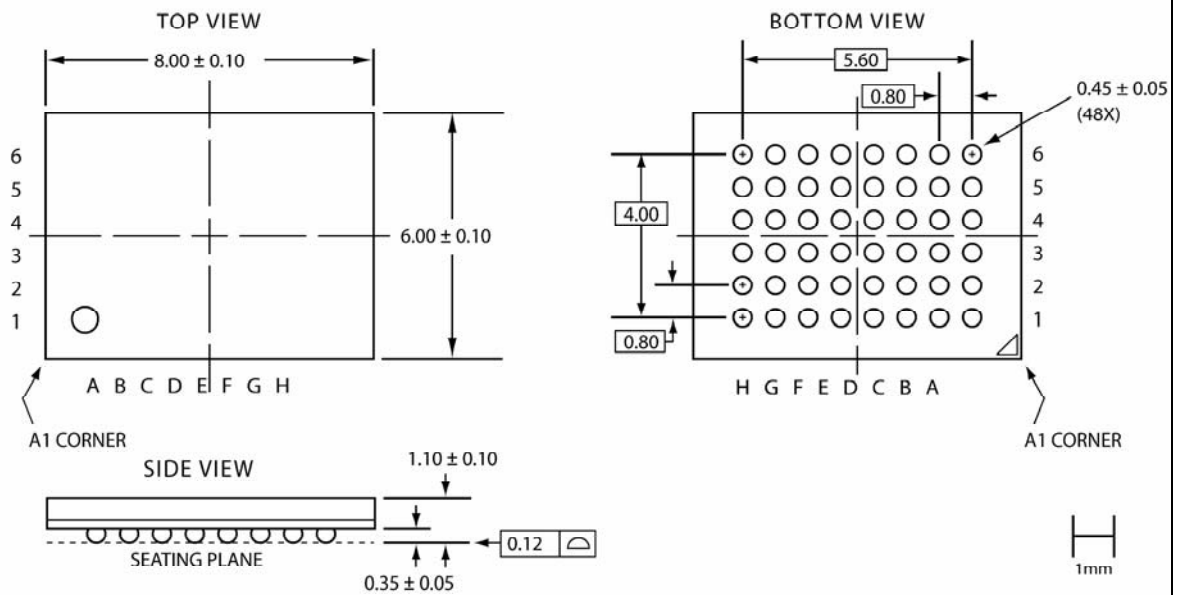
1. Complies with JEDEC publication 95 MO-142 DD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

Microchip Technology Drawing C04-14036A Sheet 1 of 1

SST39VF3201C/SST39VF3202C

48-Lead Thin Fine-Pitch Ball Grid Array (B3KE/F) - 6x8 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



48-tfbga-B3K-6x8-450mic-5

Note:

1. Complies with JEDEC Publication 95, MO-210, variant 'AB-1', although some dimensions may be more stringent.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (± 0.05 mm)

SST39VF3201C/SST39VF3202C

APPENDIX A: REVISION HISTORY

Number	Description	Date
D	<ul style="list-style-type: none">Updated Table 10 for SST39VF3201CAdded Table 11 for SST39VF3202CRemoved Commercial option	Feb 2023
C	<ul style="list-style-type: none">Revised Note 8 in Table 7	April 2020
B	<ul style="list-style-type: none">Updated document status to Data Sheet	Jul 2014
A	<ul style="list-style-type: none">Applied new document formatReleased document under letter revision systemUpdated spec number from S71410 to DS25020	Jun 2011
01	<ul style="list-style-type: none">Revised I_{SB} and I_{ALP} in Table 14 on page 16	Aug 2010
00	<ul style="list-style-type: none">Initial release	Nov 2009

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