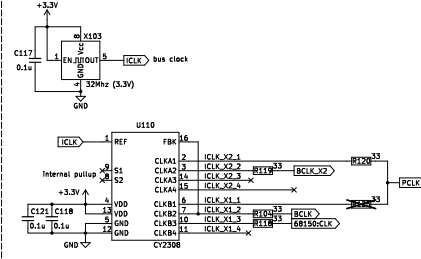


External sheets

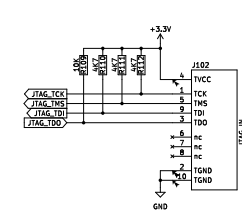
Power
File: power1.cad_sch
Local32
File: local32.cad_sch
Local16
File: local16.cad_sch
ISA
File: isa1.cad_sch
Misc
File: misc1.cad_sch

Device interrupt requests

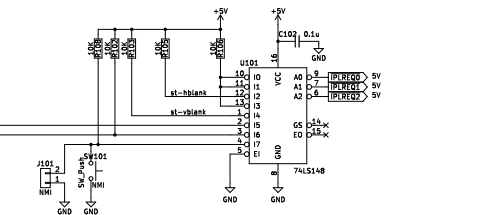
Clock



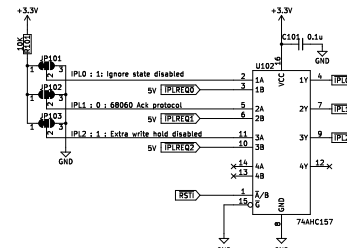
JTAG



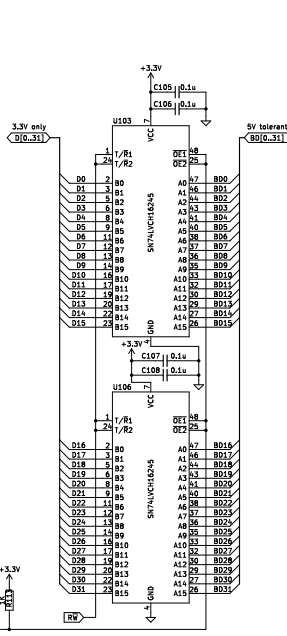
5V



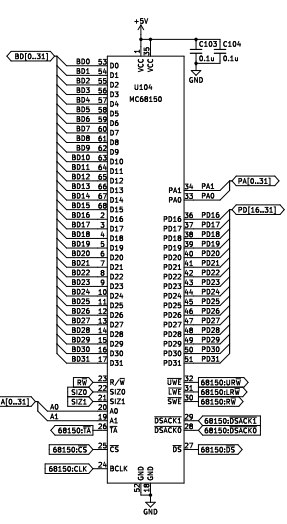
CPU interrupt trigger + startup config



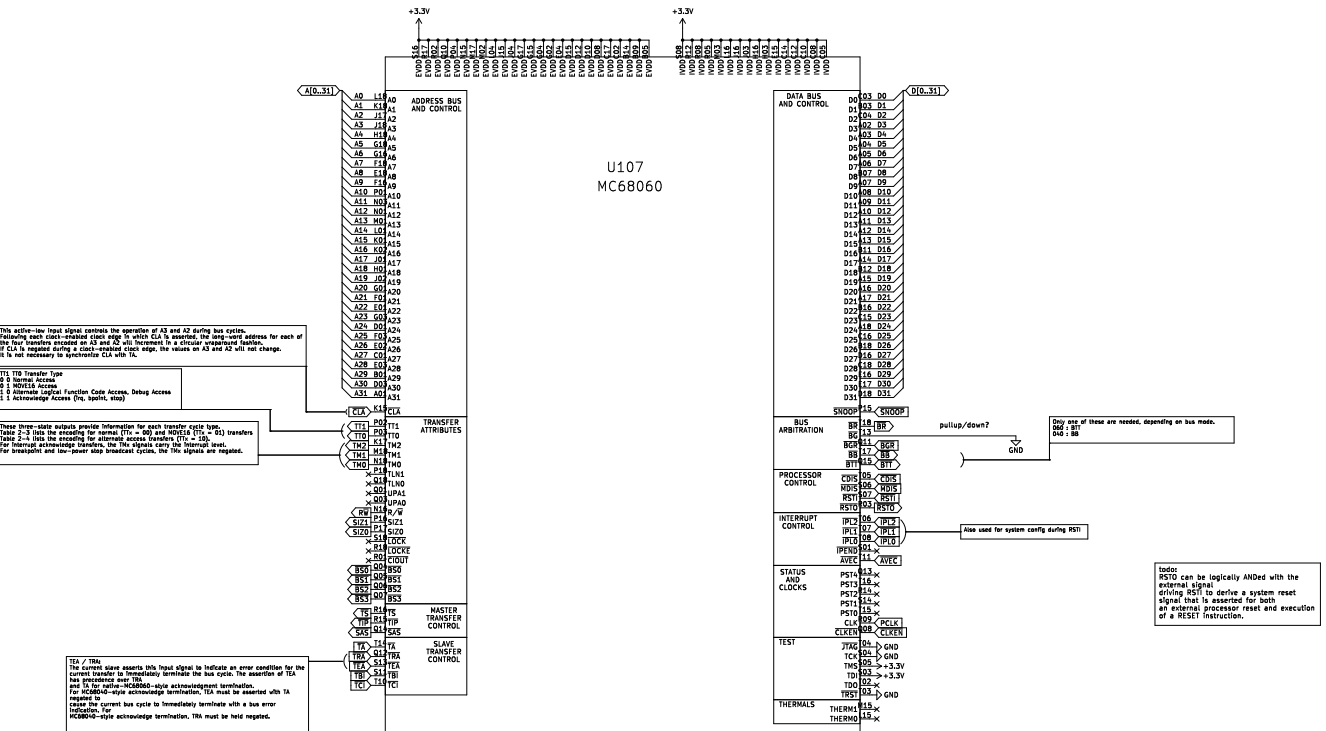
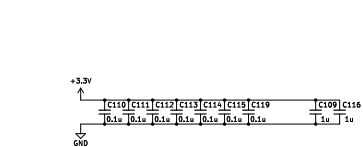
5V data bus



8/16 bit bus sizer



5V



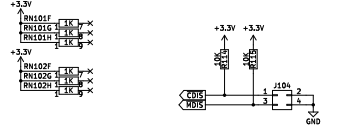
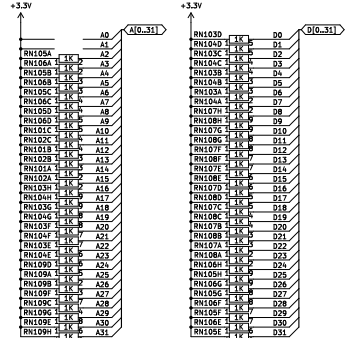
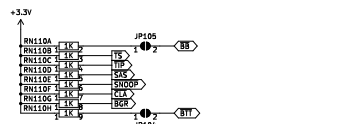
This active-low input signal controls the operation of A16 and A17 during bus cycles. Relatively each clock-edge (clock edge is when CLK is sampling, the next-most address for each of the two transfer cycles) at A16 and A17 will be updated. In a circular address buffer, if A16 is updated during a clock-edge (clock edge), the values on A16 and A17 will not change. It is not necessary to synchronize CLK with A16.

TS Transfer Type
0: Normal Transfer
1: Acknowledge Access
2: Acknowledge Access (Data Cache Access, Data Access)
3: Acknowledge Access (Data Cache Access, Data Access)

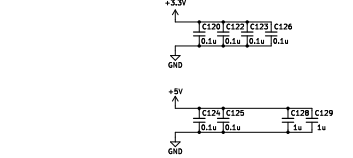
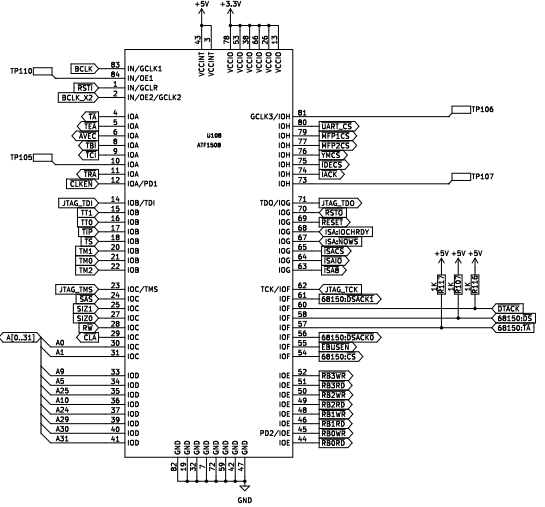
These three-state outputs provide information for each transfer cycle. The TS transfer type is 0 for normal transfer, 1 for acknowledge access, and 2 for acknowledge access (data cache access, data access). The TS transfer type is 0 for normal transfer, 1 for acknowledge access, and 2 for acknowledge access (data cache access, data access).

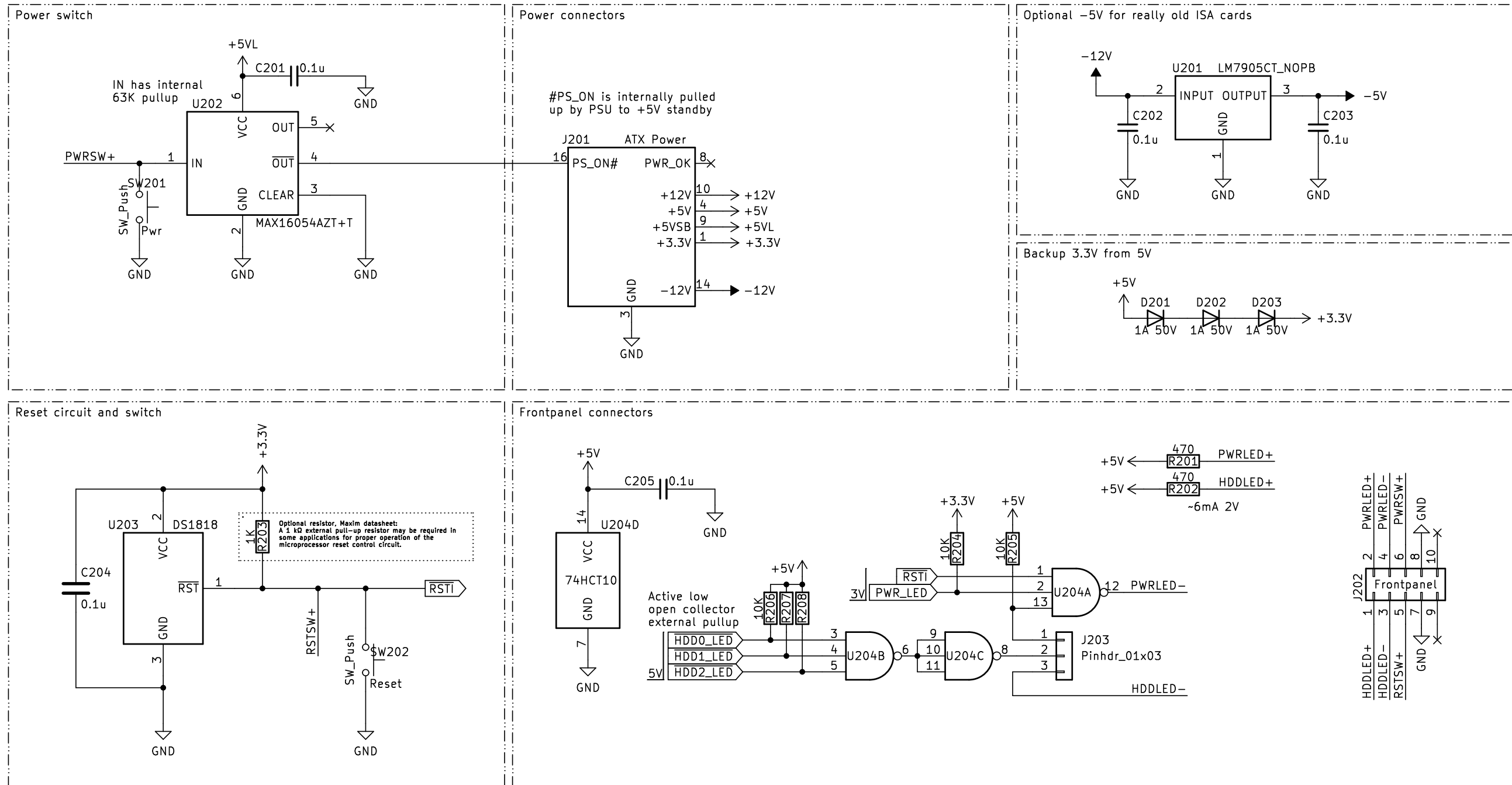
TS Transfer Type
0: Normal Transfer
1: Acknowledge Access
2: Acknowledge Access (Data Cache Access, Data Access)
3: Acknowledge Access (Data Cache Access, Data Access)

These three-state outputs provide information for each transfer cycle. The TS transfer type is 0 for normal transfer, 1 for acknowledge access, and 2 for acknowledge access (data cache access, data access). The TS transfer type is 0 for normal transfer, 1 for acknowledge access, and 2 for acknowledge access (data cache access, data access).



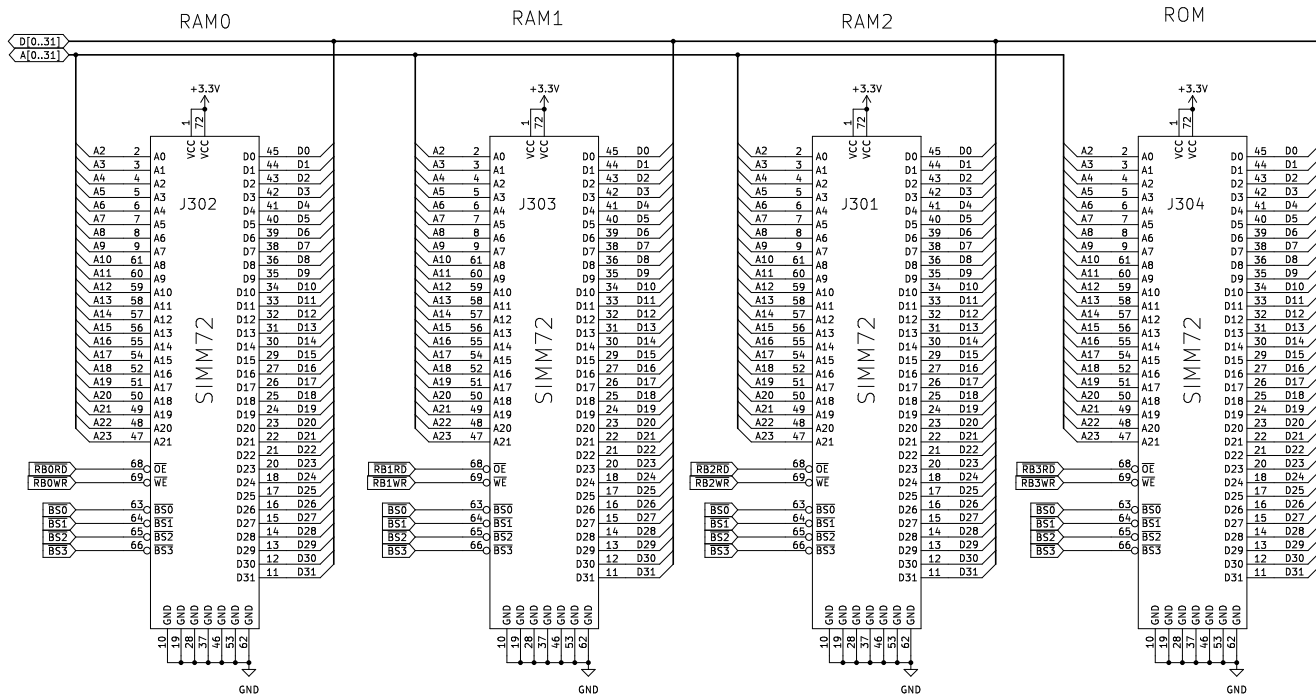
The AT1508MS device has two sets of VCC pins, viz. VCCINT and VCCIO. VCCINT pins must always be connected to a 5.0V power supply. VCCIO pins are for input buffers and are "compatible" with both 3.3V and 5.0V inputs. VCCIO pins are for I/O output drivers and can be connected for 3.3V/5.0V power supply.





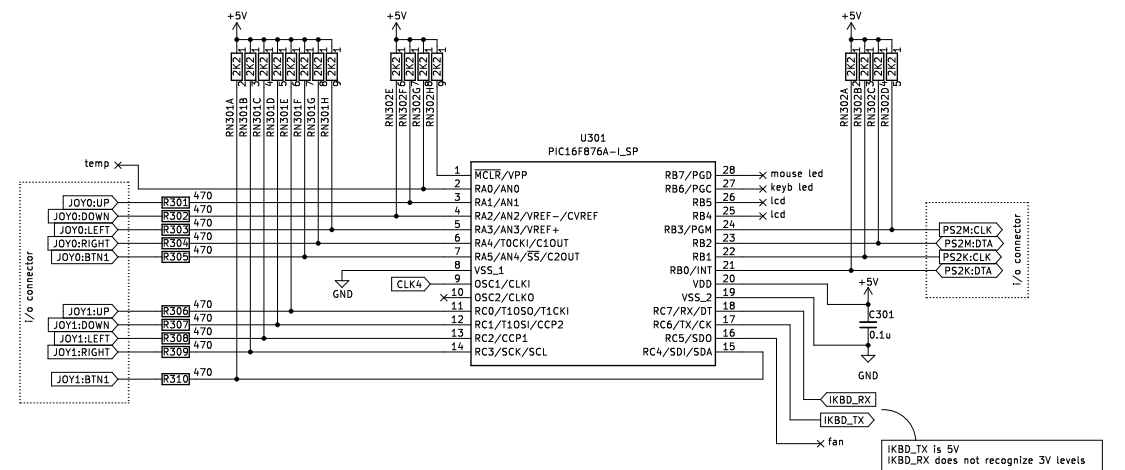
32bit local bus

SIMM slots for ram and rom

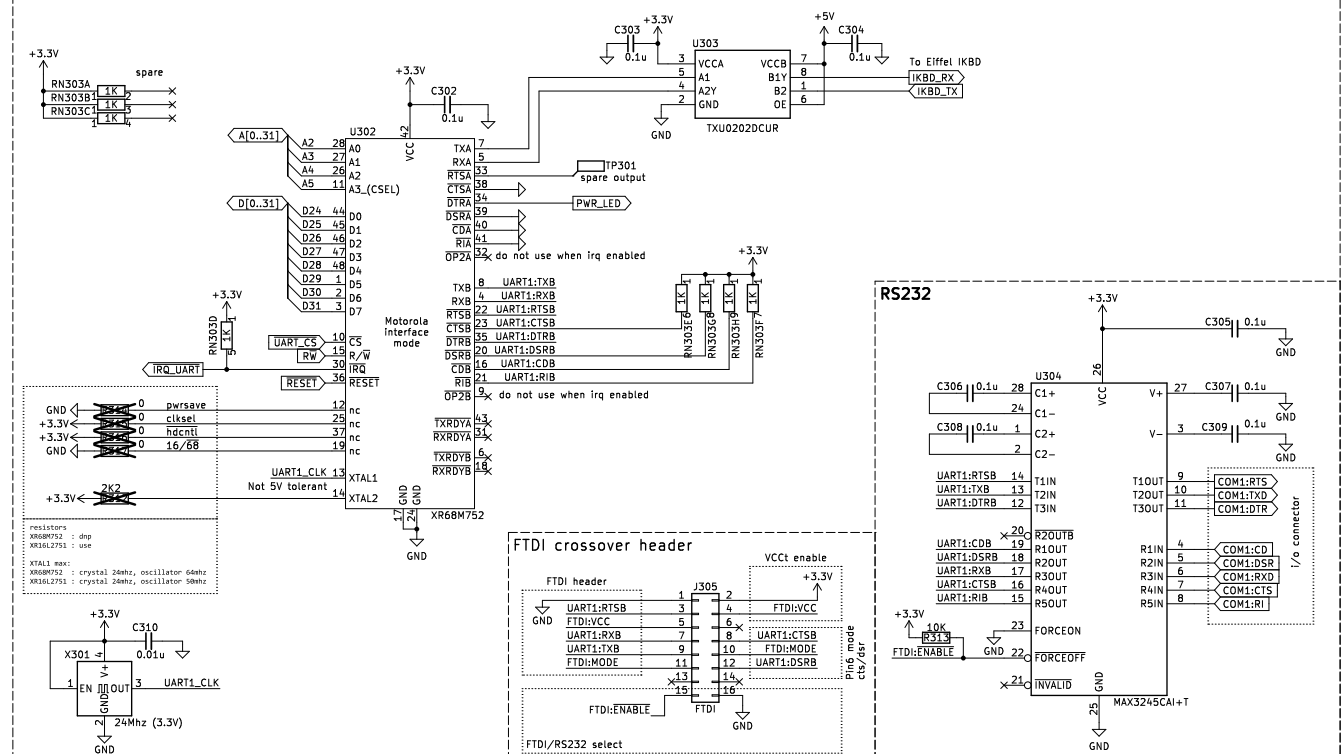


Keyboard, mouse, joystick
Eiffel IKBD

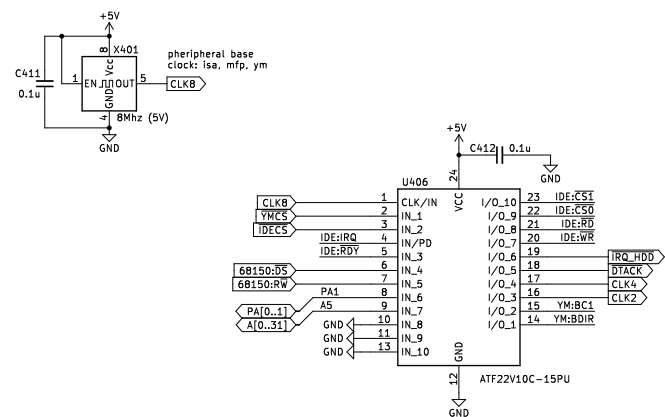
5V



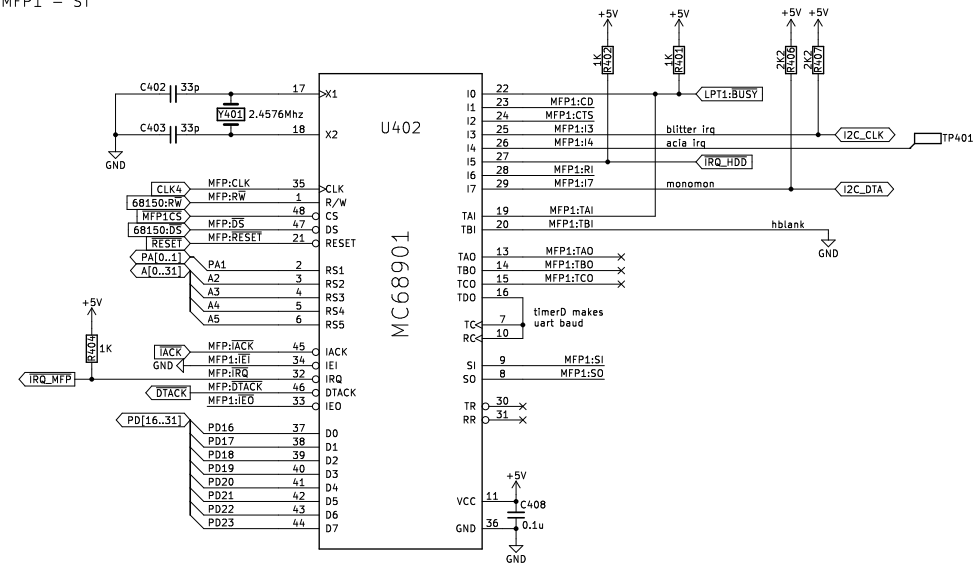
UART



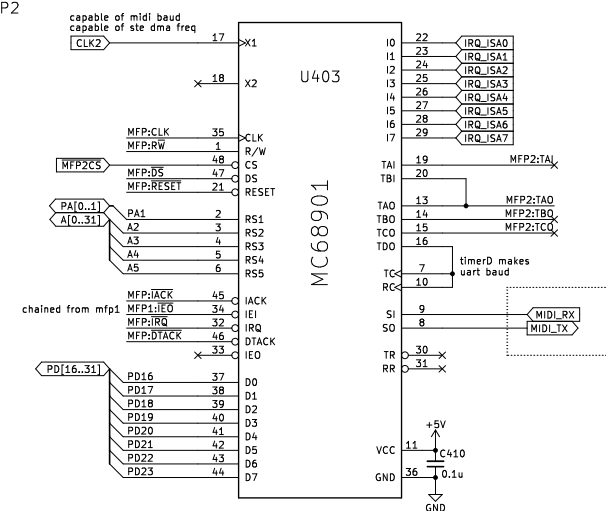
Clocks & Glue logic



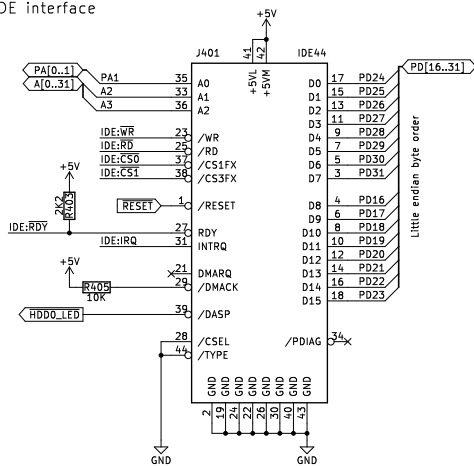
MFP1 - ST



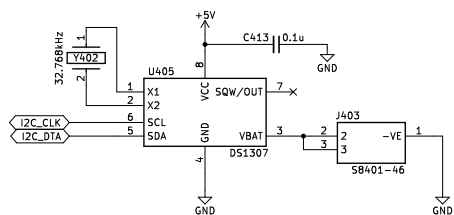
MFP2



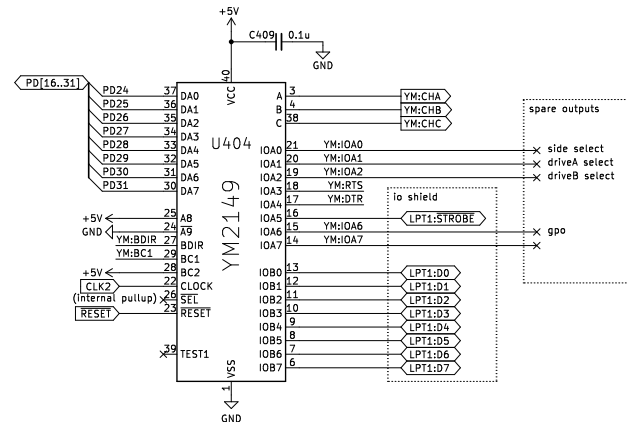
IDE interface



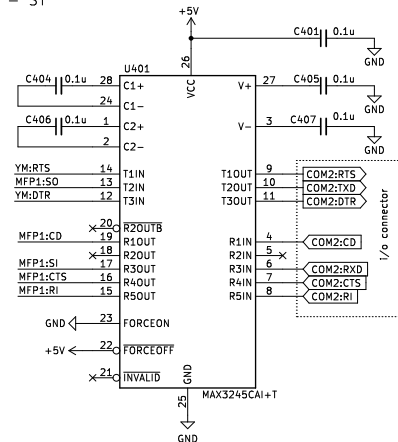
Realtime clock



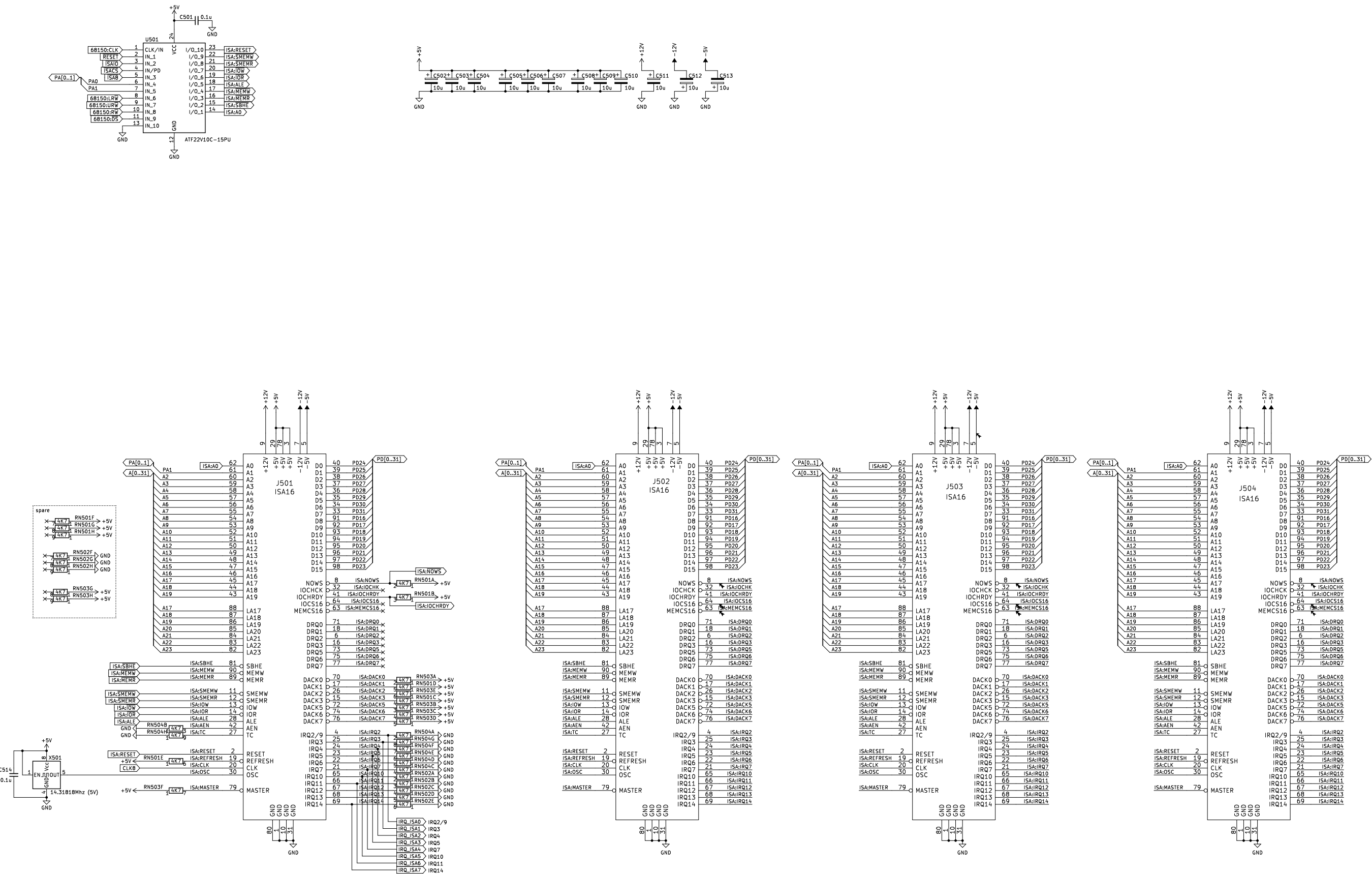
YM2149



RS232 - ST

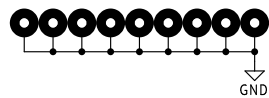


ISA Expansion slots

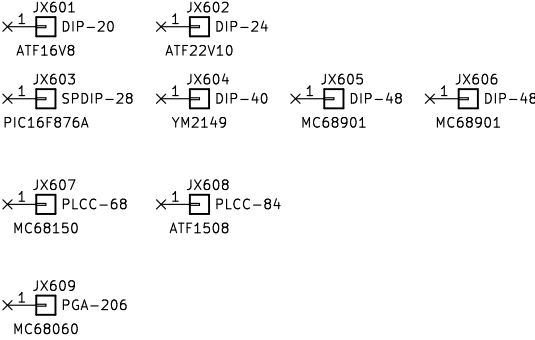


Misc / Connectors

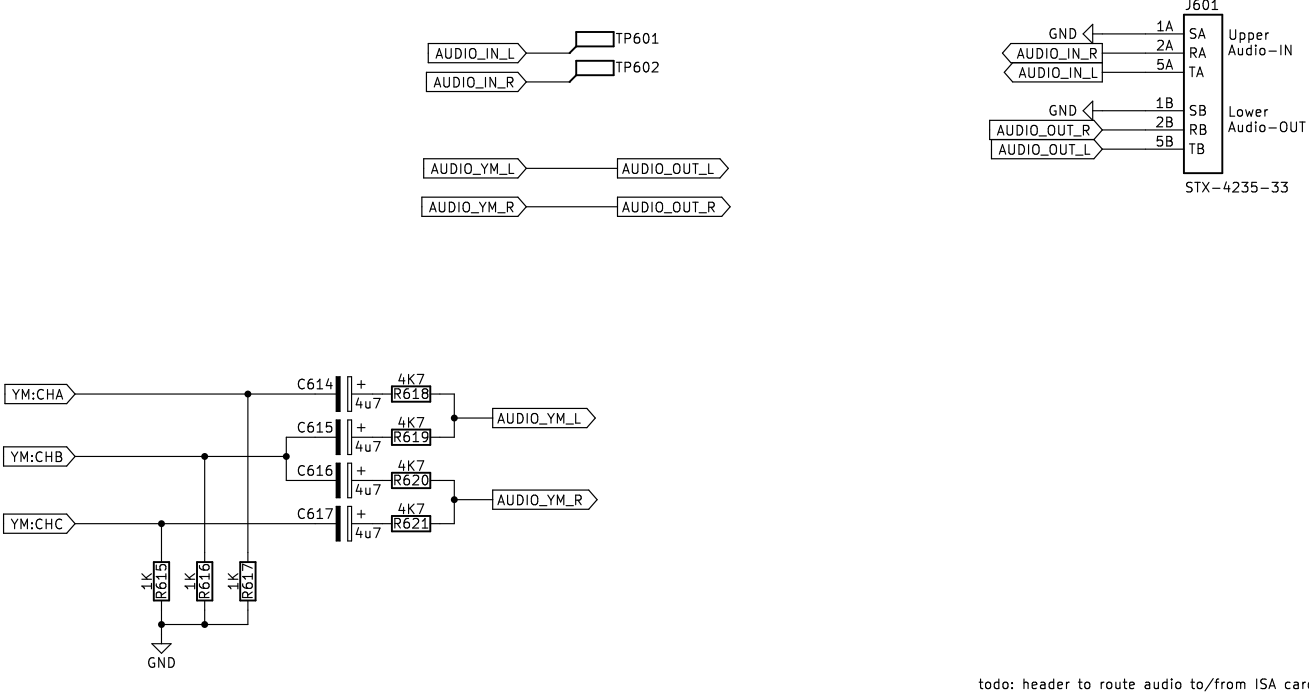
Mounting Holes



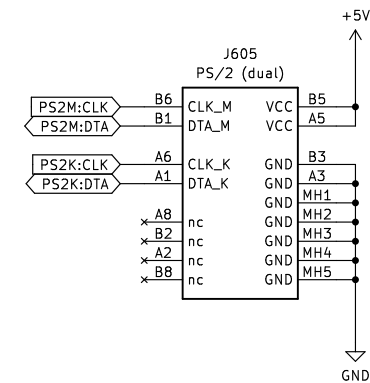
IC Sockets



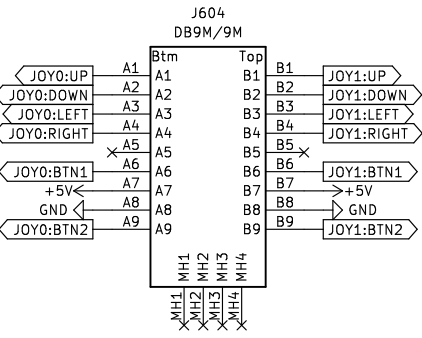
Audio



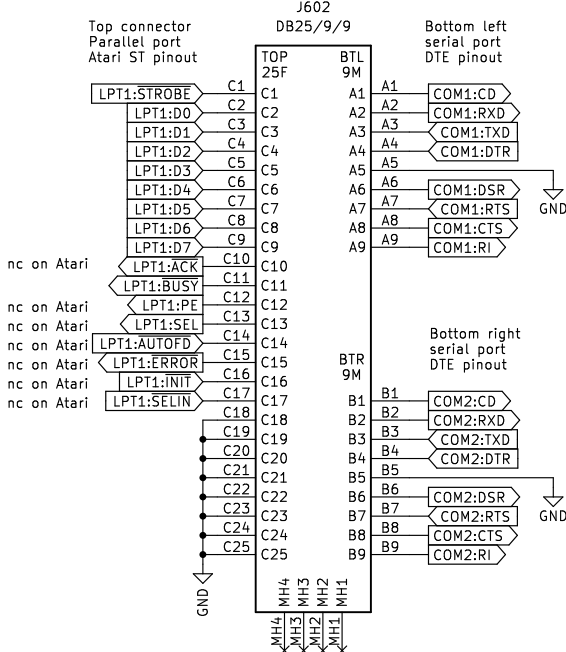
PS2 Keyboard + Mouse



Joystick x2



Parallel / Serial / Serial



Midi - TRS Type A

