Com S 321 Homework 11 Due: Thursday, Nov 30 by midnight

1. Consider a cache with four block frames and a fully associative mapping policy. Find the hit ratio for the following **Block** reference string for replacement policies of FIFO (First-In-First-Out), LRU (Least Recently Used), and MRU (Most Recently Used). In each case assume the cache is initially empty.

Block Reference String: 0, 1, 2, 3, 4, 0, 1, 5, 0, 1, 2, 3, 4, 5, 4

2. Suppose you have the following word addressable cached memory system:

Block size = 4 words
Main memory size = 1024 blocks
Cache memory size = 4 block frames
Time to read a block from main memory to cache = 400 ns
t_c = 50 ns
No read-through policy
In each case below, assume the cache is initially empty

The observed string of **WORD** addresses for instruction fetches for a certain program is:

Word Reference String: 2, 6, 11, 14, 1, 17, 5, 9, 22, 19, 12, 3, 21, 4, 18, 15

First convert the above Word reference string to a block reference string.

(a) Consider a direct mapped cache. Compute the total access time for instruction fetches for the above program (ignore data reads and writes). Because there is no read-through policy, all 16 references have to be accessed from the cache, each with time t_c.

Time for instruction fetches can be computed as: 16 * t_c + (No. of block misses * 400)

(b) Consider a fully associative cache. Compute the total access time for instruction fetches using a FIFO replacement policy to replace a cache block frame (ignore data reads and writes).

(c) Consider a fully associative cache. Compute the total access time for instruction fetches using a LRU replacement policy to replace a cache block frame (ignore data reads and writes).

(d) Consider a fully associative cache. Compute the total access time for instruction fetches using a MRU replacement policy to replace a cache block frame (ignore data reads and writes).

3. Consider the following reference string given as WORD addresses:

1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17.

Assume a Direct-Mapped cache with 16 one-word block frames that is initially empty. When this reference string is processed, label each reference as a Hit or Miss, and pictorially show the state

of the cache as each word address is processed. The state of the cache at the end should be the final state after the last word is processed.

4. Using the same reference string as in Problem 3, indicate the Hits and Misses and show the state of the cache after each address including the final contents for a Direct-Mapped cache with 4-word block frames and a total cache size of 16 words. Assume the cache is initially empty.

5. Using the same reference string as in Problem 3, indicate the Hits and Misses and show the state of the cache after each address including the final contents for a Set Associative cache with a total size of 16 words, a Block frame size of one-word and a Set size of 2 (that is, 2 block frames per set). Within a Set, assume an LRU (Least Recently Used) policy for block replacement. Assume the cache is initially empty.

6. Repeat Problem 5 with a FIFO (First In First Out) policy for block replacement.

7. Repeat Problem 5 with an MRU (Most Recently Used) policy for block replacement.