1.

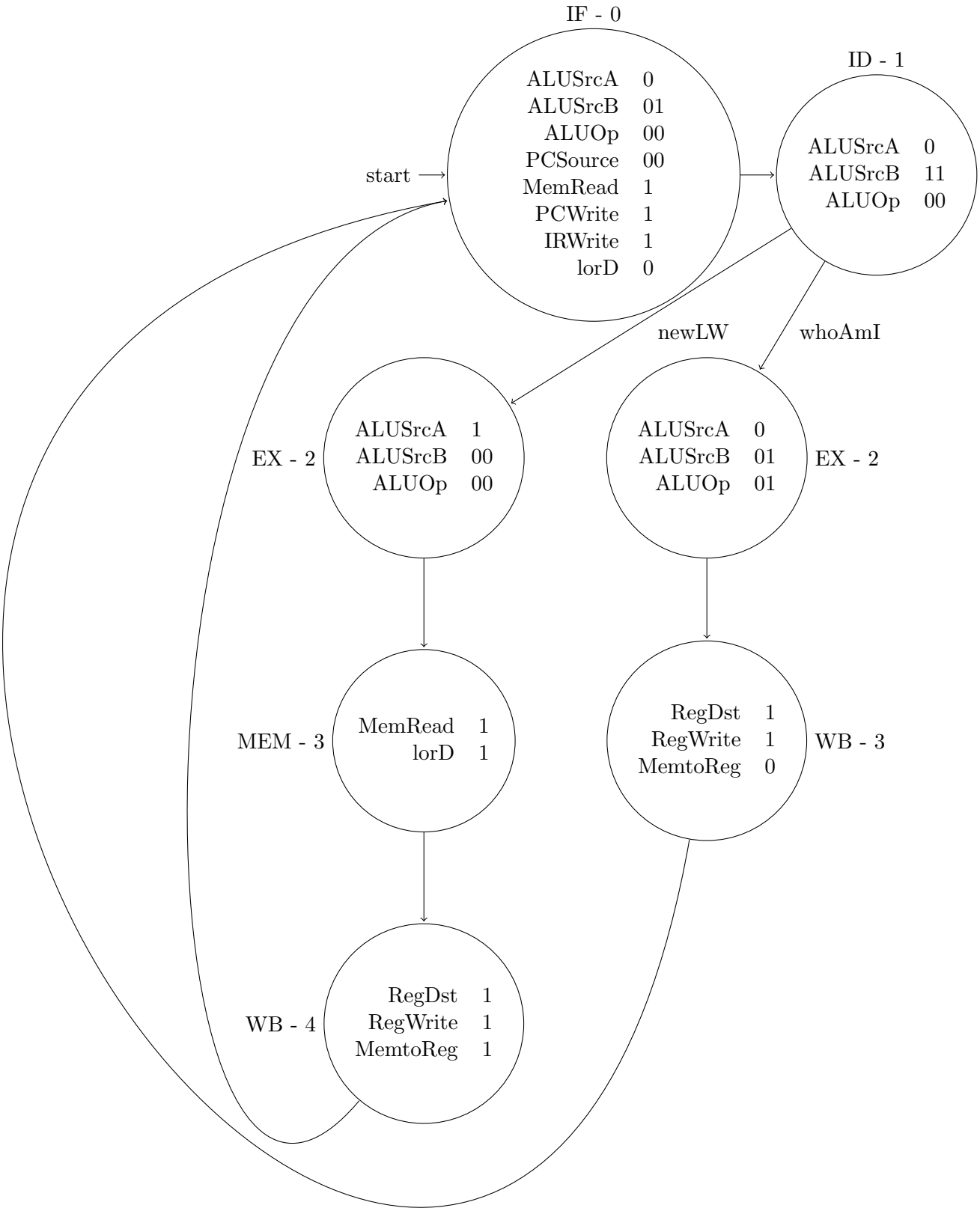
	Add	Sub	LW	SW	BEQ	Addi
RegDst	1	1	0	D	D	0
ALUSrc	0	0	1	1	0	1
MemToReg	0	0	1	D	0	0
RegWrite	1	1	1	0	0	1
PCSrc	0	0	0	0	1	0
MemWrite	0	0	0	1	0	0
MemRead	0	0	1	0	0	0
ALUOp	Add	Sub	Add	Add	Sub	Add

2.

No changes would need to be made to the diagram.

RegDst	1
AluSrc	0
PCSrc	0
MemToReg	1
MemRead	1
MemWrite	0

3.


IF - 0
ALUSrcA 0
ALUSrcB 01
ALUOp 00
PCSource 00
MemRead 1
PCWrite 1
IRWrite 1
lorD 0
start
ID - 1
ALUSrcA 0
ALUSrcB 11
ALUOp 00
newLW
whoAmI
EX - 2
ALUSrcA 1
ALUSrcB 00
ALUOp 00
ALUSrcA 0
ALUSrcB 01
ALUOp 01
EX - 2
MEM - 3
MemRead 1
lorD 1
RegDst 1
RegWrite 1
MemtoReg 0
WB - 3
WB - 4
RegDst 1
RegWrite 1
MemtoReg 1

4.

a)

I would add a mux in front of the read 1 input that on a 1 would select the low order 5 bits called ReadA and I would add a Mux to the read 2 input that on a 1 would select 15-11 called ReadB

b)