

1. Suppose you have a word addressable cached memory system with the following parameters:

$$t_m = 1000\text{ns}$$

$$h = 0.90$$

$$t_c = 100\text{ns}$$

$$\text{Block size} = 8 \text{ words}$$

(a) Calculate the effective memory access time, if upon a cache miss the word is directly read from main memory (i.e., there is a read through policy implemented).

(b) Calculate the effective memory access time with no read through policy. Upon a cache miss, a block is first written to main memory (one word at a time), then the desired block is read from main memory into the cache (one word at a time), and finally the word is read from the cache.

(c) Consider the following options to improve the effective memory access time in part (b):

- (1) Make main memory twice as fast
- (2) Maintain $t_m = 1000\text{ns}$, but make the main memory to cache connection 4 words wide

Which of these two options is better, assuming each costs the same? Justify your answer.

2. Suppose you have a word-addressable cached memory system with the following parameters:

$$\text{Hit ratio} = h$$

$$\text{Block size} = B \text{ words}$$

$$\text{Main memory cycle time} = t_m$$

$$\text{Cache cycle time} = t_c$$

$$\text{Main memory to cache connection} = c \text{ words}$$

$$\text{Fraction of Write accesses} = W$$

No read through policy

Write through policy for write hits

No-write allocate for write misses

Upon a read miss, a block is read from memory to cache and the word is accessed from the cache by the CPU.

The average memory access time, T_{avg} , can be expressed as follows:

$$T_{avg} = h [\text{Total ReadHitTime} + \text{Total WriteHitTime}] + (1 - h) [\text{Total ReadMissPenalty} + \text{Total WriteMissPenalty}]$$

Give general expressions for each of the quantities in square brackets.

- (a) Total ReadHitTime
- (b) Total WriteHitTime
- (c) Total ReadMissPenalty
- (d) Total WriteMissPenalty

3. Suppose we have a cached system with the following parameters:

$t_c = 100 \text{ ns}$ $t_m = 1000 \text{ ns}$
 $h = 0.90$ Block size = 8 words
Main memory to cache connection = 2 words

- (a) Calculate the effective memory access time if a read through policy is used.
- (b) Calculate the effective memory access time if no read through policy is used. Assume that, upon a cache miss, the replaced cache block is first transferred to main memory, the requested block is then loaded into the cache, and then the selected word is accessed from the cache.
- (c) Same as part (b) except that a *no write allocate* policy is used on a write miss. That is, the word is modified in main memory but the block is not loaded into the cache. Assume 30% of all accesses are writes. Recall that *no write allocate* does not imply anything about policies on write hits – all it says is what happens upon a cache miss.

4. Suppose we have a cached system with the following parameters:

$t_c = 100 \text{ ns}$ $t_m = 1000 \text{ ns}$
 $h = 0.95$ Block size = 8 words
Main memory to cache connection = 4 words

- (a) Calculate the effective memory access time if a read through policy is used.
- (b) Calculate the effective memory access time if no read through policy is used. Assume that, upon a cache miss, the replaced cache block is first transferred to main memory, the requested block is then loaded into the cache, and then the selected word is accessed from the cache.
- (c) Same as part (b) except that a *no write allocate* policy is used on a write miss. That is, the block is modified in main memory but not loaded into the cache. Assume 25% of all accesses are writes. Recall that *no write allocate* does not imply anything about policies on write hits – all it says is what happens on a cache write miss.
- (d) In this case a write through policy is also implemented for write hits. That is, the cache implements write through with *no write allocate* as in part (c). Because of the write-through policy, upon a cache read miss a block does not need to be written to main memory. The requested block is just loaded from main memory into the cache and the addressed word is then accessed by the CPU from the cache (assume no read through).