Com S 321 Homework 9 Due: Mon, Nov. 13, By Midnight

1. A computer has a main memory of size 8M words and a cache size of 64K words.

(a) Give the address format for a direct mapped cache with a block size of 32 words.

(b) Give the address format for a fully associative cache with a block size of 2^m words.

(c) Give the address format for a set associative cache with a block size of 64 words and a set size of 4 (i.e., 4 block frames per set).

2. Suppose you have a word addressed memory hierarchy system with the following parameters:

Block size = 16 words
Main memory size = 64 blocks (note the units, it is not words)
Cache size = 8 blocks
Block placement policy: direct mapping

The tag values in the cache directory are:

Tag	Cache Block Frame #
000	0
101	1
100	2
010	3
101	4
011	5
100	6
110	7

(a) Give the address format for the memory system.

(b) Will main memory address 37A (hex) be a cache hit? Explain your answer.

(c) Will main memory address 22C (hex) be a cache hit? Explain your answer.

(d) Will main memory address 1B9 (hex) be a cache hit? Explain your answer.

3. Suppose your cache from Problem 2 is set associative with a set size of 2 (i.e., 2 block frames per set). Assume the following tag values:

Tag	Cache Block Frame #	Set #
0000	0	0
0100	1	0
1000	2	1
1001	3	1
1100	4	2
1000	5	2
0110	6	3
1101	7	3

Do parts (a) through (d) given in Problem 2.

4. Suppose you have a cached computer system with 1M words in main memory and a cache size of 4K words. Assume main memory is divided into blocks with each block containing 16 words. Assume word addressing.

(a) If the cache uses direct mapping, what cache frame does the physical (hex) address 0x949DA map into? What value needs to be in that cache frame's tag to get a cache hit?

(b) Assume a set associative cache with 64 sets of 4 block frames per set. What set does the physical (hex) address 0x949DA map into? How many bits are there in each cache tag? What is the cache tag (in hex) for this physical address?

(c) If the cache is fully associative, what is the cache tag for the physical (hex) address 0x949DA?

5. Suppose you have a cached computer system with a main memory size of 32K words and a cache size of 4K words. The cache is fully associative with a block size of 8 words. Assume word addressing.

(a) How many hardware comparators are needed to support the fully associative cache?

(b) What is the size of the tag field?

(c) How many hardware comparators would be needed to support a direct mapped cache? What would be the size of the tag field with a direct mapped cache?

6. Suppose you have a word-addressable cache memory system with the following parameters:

8K **blocks** in main memory (note the units, it is not words)
512 **block frames** in cache memory
8 words in a **block**

(a) How many bits are there in a main memory address?

(b) Given the memory address 0x**CA49** (hex), give the 3-bit offset of the word within the block that is being referenced.

(c) In a direct mapped cache, give the cache block frame number to which the above referenced address is mapped to. Give your answer in decimal. Give the number and width of hardware comparators that will be needed to determine if the reference is a hit.

(d) In a set associative cache with four block frames per set, give the set number to which the above referenced address is mapped to. Give your answer in decimal. Give the number and width of hardware comparators that are needed.