

1.

	Add	Sub	LW	SW	BEQ	Addi
RegDst	1	1	0	D	D	0
ALUSrc	0	0	1	1	0	1
MemToReg	0	0	1	D	0	0
RegWrite	1	1	1	0	0	1
PCSrc	0	0	0	0	1	0
MemWrite	0	0	0	1	0	0
MemRead	0	0	1	0	0	0
ALUOp	Add	Sub	Add	Add	Sub	Add

2.

No changes would need to be made to the diagram.

RegDst	1
AluSrc	0
PCSrc	0
MemToReg	1
MemRead	1
MemWrite	0

3.

