J-Link ↔ Infineon XC164 (OCDS JTAG) Cheat-Sheet

with Pull-up / Pull-down & Series Resistor Recommendations

J-Link 20-pin Header

Pin 1 : Vref
Pin 3 : nTRST
Pin 5 : TDI
Pin 7 : TMS
Pin 9 : TCK
Pin 13: TDO
Pin 15: nRESET
Pin 2 : GND
Pin 4 : GND
Pin 6 : GND
Pin 8 : GND
Pin 10: GND
Pin 12: GND
Pin 14: GND
Pin 16: GND
Pin 18: GND
Pin 20: GND

Infineon XC164 (OCDS JTAG)

Vref : VDDP (5.0 V) → tie to board VDD
nTRST : TRST (Pin 36) → 4.7kΩ pull-down
TDI : P3.3 → 4.7kΩ pull-up
TMS : P3.4 → 4.7kΩ pull-up
TCK : P3.7 → 33Ω series (optional)
TDO : P3.6 → 33Ω series (optional)
nRESET: RSTIN (Pin 1) → 4.7kΩ pull-up

Quick Checklist

- Power board externally at 5.0 V (preferred). Tie J-Link Vref to VDDP.
- J-Link can source power, but current is limited. Verify first.
- Pull-ups: TMS, TDI, RESET (4.7kΩ to Vref).
- Pull-down: TRST (4.7kΩ to GND).
- Series resistors: 33Ω on TCK, TDO if signal integrity issues.
- Ensure target clock (XTAL) is running.
- Use 'Connect under Reset' in J-Flash/MemTool if attach fails.
- If flash read-protected: external bus capture or chip adapter required.