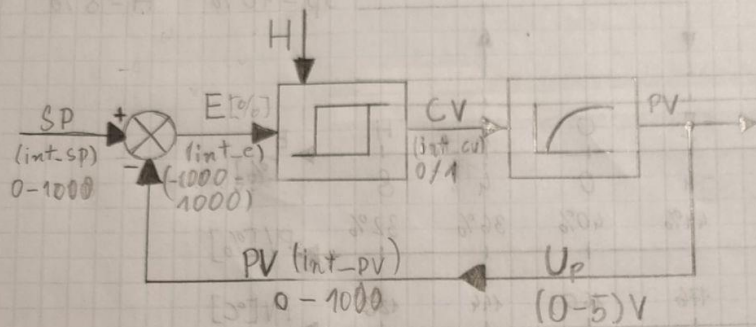


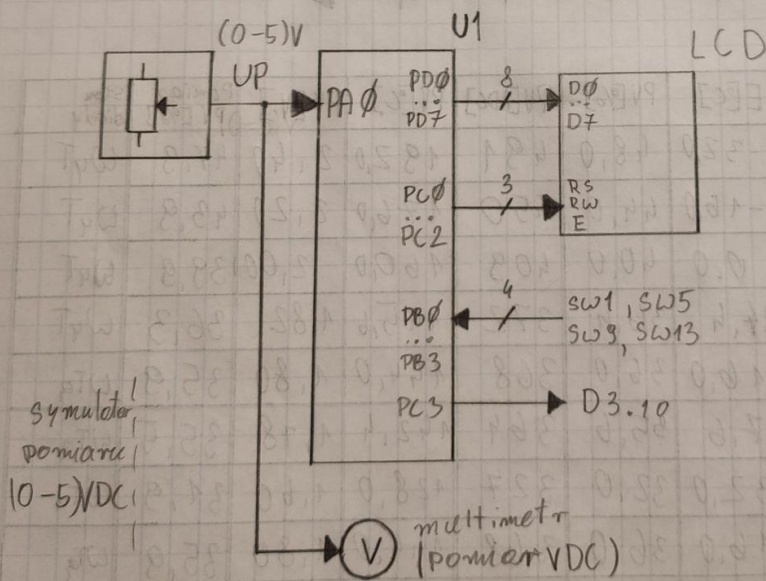
Borys Staszko 24.8.95

Temat: Badanie regulatora dwustopniowego

1. Schemat blokowy typowego układu regulacji



2. Schemat blokowy podłączenia sygnałów w układzie do badania regulatora

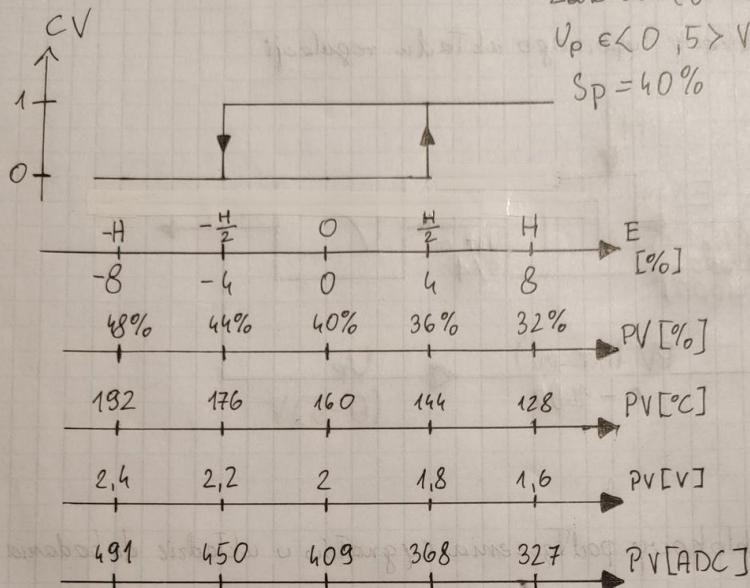


3. Charakterystyka regulatora dwustawnego

Zakres: $(0 - 400)^\circ\text{C}$

$U_p \in \langle 0, 5 \rangle \text{ V}$

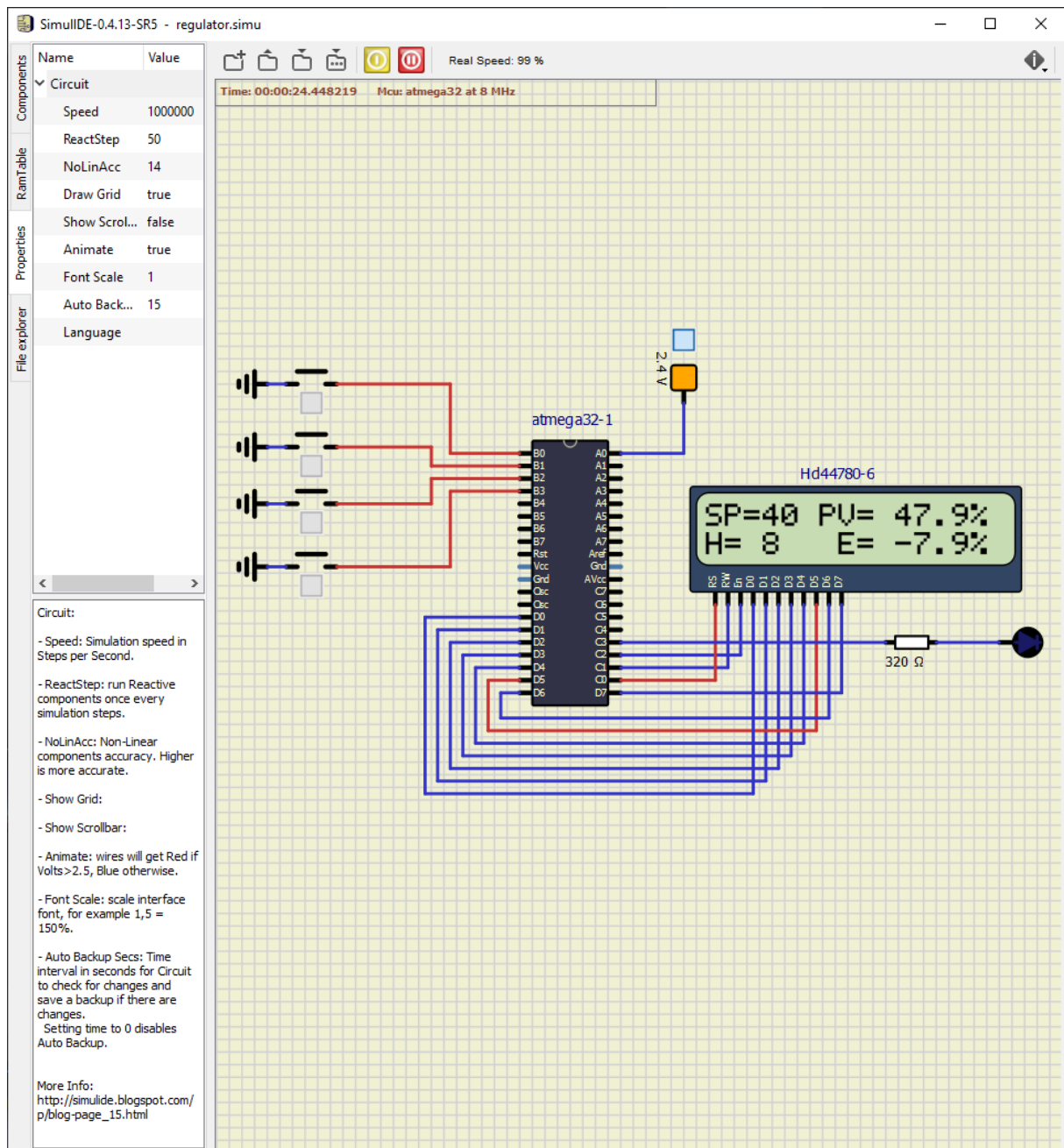
$S_p = 40\% \quad H = 8\%$



4.

$E[H]$	$E[\%]$	$E[^\circ\text{C}]$	$PV[\%]$	$PV[\text{ADC}]$	$PV[^\circ\text{C}]$	$PV[\text{V}]$	Pomiar $PV[\%]$	Stan diody
-1,00	-8,00	-32,0	48,0	491	182,0	2,40	47,9	W_{YT}
-0,50	-4,00	-16,0	44,0	450	176,0	2,20	43,9	W_{YT}
0,00	0,00	0,0	40,0	409	160,0	2,00	39,9	W_{YT}
0,45	3,60	14,4	36,4	372	145,6	1,82	36,3	W_{YT}
0,50	4,00	16,0	36,0	368	144,0	1,80	35,9	W_{Tq}
0,55	4,40	17,6	35,6	364	142,4	1,78	35,5	W_{Tq}
1,00	8,00	32,0	32,0	327	128,0	1,60	31,9	W_{Tq}
0,50	4,00	16,0	36,0	368	144,0	1,80	35,9	W_{Tq}
0,00	0,00	0,0	40,0	409	160,0	2,00	39,9	W_{Tq}
-0,45	-3,60	-14,4	43,6	446	174,4	2,18	43,5	W_{YT}
-0,50	-4,00	-16,0	44,0	450	176,0	2,20	43,9	W_{YT}
-0,55	-4,40	-17,6	44,4	454	177,6	2,22	44,3	W_{YT}
-1,00	-8,00	-32,0	48,0	491	182,0	2,40	47,9	W_{YT}

Bonyś Stanisław 248958




```

93 // Set point (in %)
94 int set_point = 40;
95 // Histereza (in %)
96 int _h = 8;
97 // Error value
98 int _e;
99 // Integer part of the error
100 int int_e;
101 // Decimal value of the error
102 int dec_e;
103 // Whole process value (in 0-1023 range)
104 float process_value;
105 // Process value with decimal part
106 int full_process_value;
107 // Integer part of process value
108 int int_process_value;
109 // Decimal part of process value
110 int dec_process_value;
111
112 int main(void)
113 {
114     char tmp[16];
115
116     int i;
117
118     DDRD = 0xff;
119     PORTD = 0x00;
120     DDRC = 0xff;
121     PORTC = 0x00;
122     DDRB = 0x00;
123     PORTB = 0xff;
124
125     _delay_ms(500);
126
127     LCD2x16_init();
128     LCD2x16_clear();
129
130     ADMUX = 0x40;
131     ADCSRA = 0xe0;
132
133     while (1)
134     {
135         // Start an ADC conversion by setting ADSC bit (bit 6)
136         ADCSRA = ADCSRA | (1 << ADSC);
137
138         // Wait until the ADSC bit has been cleared
139         while (ADCSRA & (1 << ADSC))
140             ;
141
142         process_value = ADC;
143
144         full_process_value = (process_value / 1023.0) * 1000;
145         int_process_value = full_process_value / 10;
146         dec_process_value = full_process_value % 10;
147

```

```

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```

```

_e = (set_point * 10) - full_process_value;
int_e = _e / 10;
dec_e = _e % 10;

// LED On
if (_e > (_h / 2))
{
    PORTC = ~(0x01 << 5);
}

// LED Off
if (_e < -(_h / 2))
{
    PORTC = (0x01 << 5);
}

if (!(PINB & (8 << PB0)))
{
    set_point = 50;
}
if (!(PINB & (4 << PB0)))
{
    set_point = 40;
}
if (!(PINB & (2 << PB0)))
{
    _h = 8;
}
if (!(PINB & (1 << PB0)))
{
    _h = 10;
}

LCD2x16_pos(1, 1);
sprintf(tmp, "SP=%2d PV=%3d.%1d%% ", set_point, int_process_value, abs(dec_process_value));
for (i = 0; i < 16; i++)
{
    LCD2x16_putchar(tmp[i]);
}

LCD2x16_pos(2, 1);
sprintf(tmp, "H=%2d E=%3d.%1d%% ", _h, int_e, abs(dec_e));
for (i = 0; i < 16; i++)
{
    LCD2x16_putchar(tmp[i]);
}
delay_ms(500);
}

return 0;
}

```