**CDA 4213/CIS 6930 CMOS VLSI**

**Fall 2018**

**Final Project**

**Due date**

**11:59PM, Sunday, 18th November**

|  |  |
| --- | --- |
| Today’s Date: | 11/15/18 |
| Your Team Name: | *Creative B* |
| Team Members: | Mary Mouro, Henry Cates, John Adams |
| Work Distribution | Explain in detail, who has done what. Each team member’s grade will be based on their overall contribution.  1) Mary: Full adder w/ AND and registers  2) Henry: Multiplier Array  3) John: Reports, Testing, and Debugging |
| No. of Hours Spent: | ∞ |
| Exercise Difficulty:  (Easy, Average, Hard) | ROCK HARD |
| Any Feedback: | 😊 |

##### (1) **(10 pts)**

###### Proposed Design – Bit slice design

1. List all module bit-slices you have used for your design.

Full Adder

Full Adder with AND gate

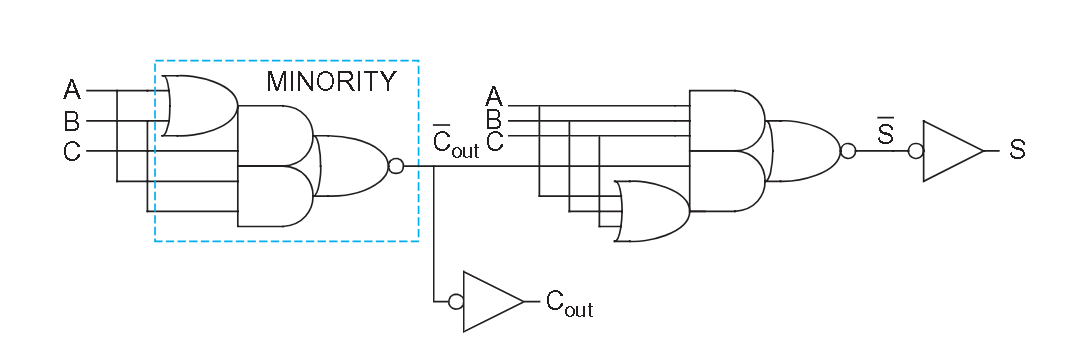
Shift Registers

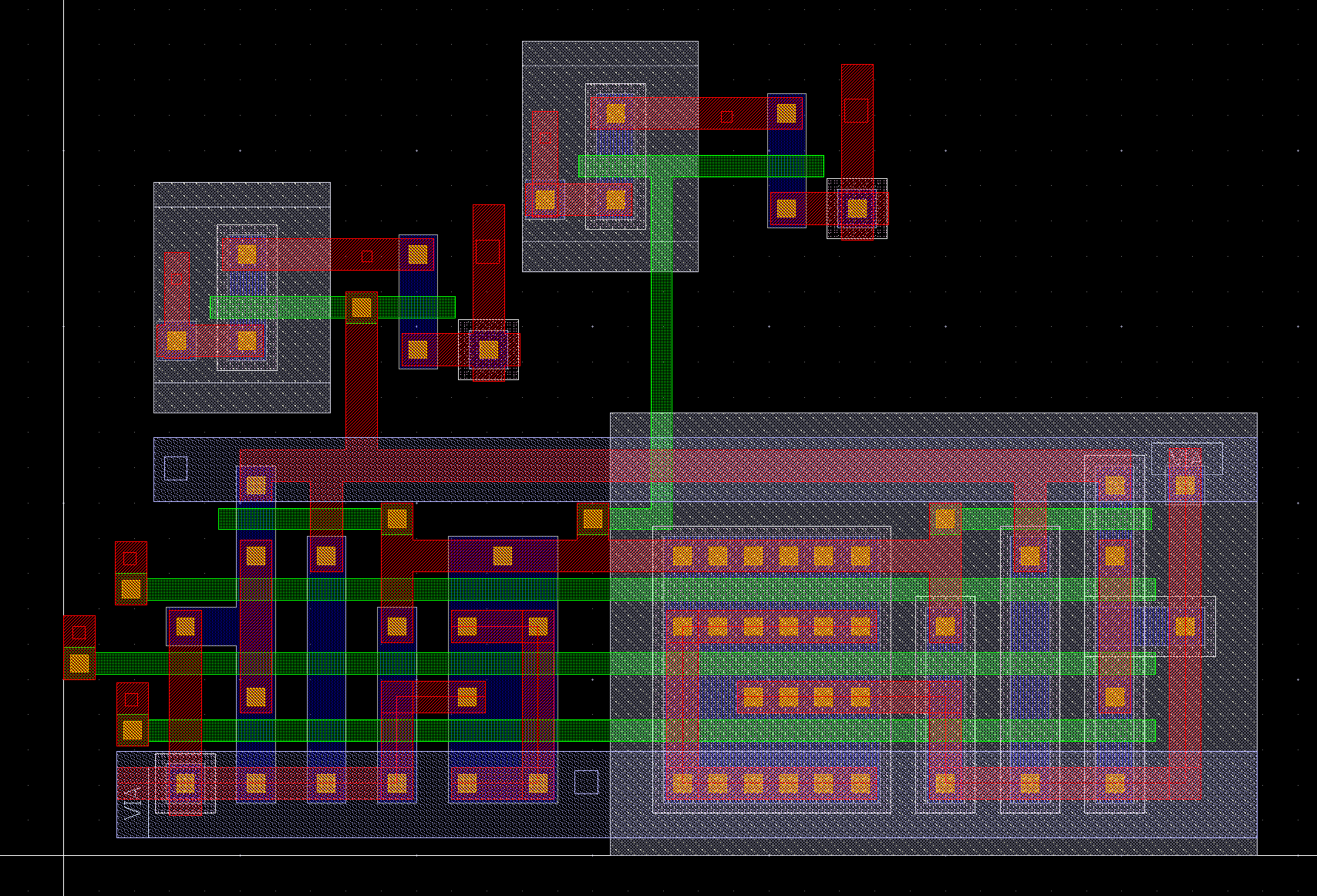
Multiplexer

AND gate

Inverter

1. For each bit slice, show the gate-level design and layout design. For layout, include the snapshot from Cadence Virtuoso. If you have used any other blocks, include them as well.
2. Full Adder:





1. Full Adder with AND gate:

A close up of a map

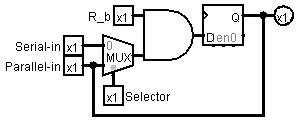
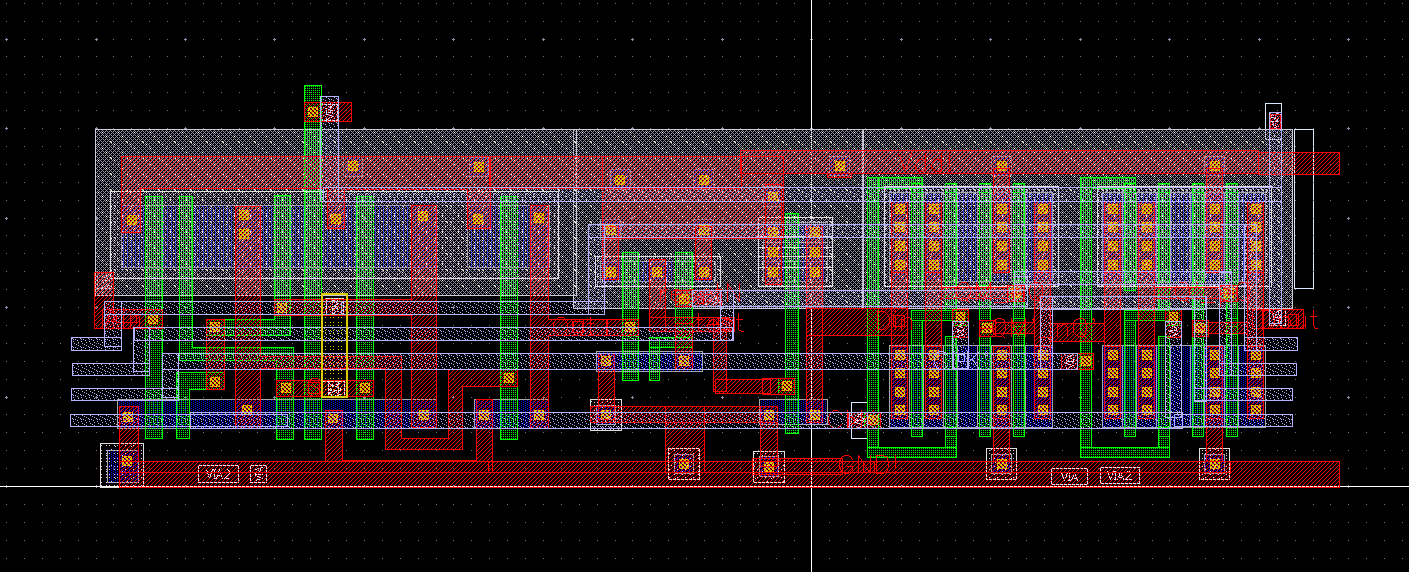
Description automatically generated

A circuit board

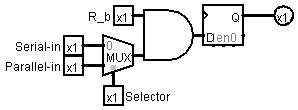
Description automatically generated

1. Registers (Inputs and Output):

INPUT one BIT:



OUTPUT one BIT:



A circuit board

Description automatically generated

1. Ring Oscillator (If used): N/A

##### (2) **(15 pts)**

###### Show the layout of your multiplier with the registers (outside the padframe).

###### Explain the design and functionality of your multiplier.

A screenshot of a computer

Description automatically generated

Input registers are to the left (X)(X0 to X7)(from top to bottom) and top (Y)(labeled left to right Y7 to Y0 (far right of the top shifter)), the longer portions are the chained MUX to AND to D FF, times 8 which explains their length. The input registers have a loop back that holds the value when the selector is set. The input registers take serial input and pass (parallel) it to the multipler which is the large cascading mass in the middle of the design. The multiplier is made up of full adders with INV(s) and AND gates attached to each. All rows and columns contain this same setup except the last row which is only full adders themselves. The output registers are copies of the inputs but without the looping mechanism and receive their input from the multiplier . The entire design is outlined in M3 which is ground, and the M3 that goes from to right is ground and the large internal block of M3 is VDD which feeds from right to left. When the TestMode bit is set the input registers are connected serially and have a MUX in between that is activated via the TestMode pin. At the end of the Y shifter in test is a AND gate that combines the test mode and Y serial output together in order to shift into the output registers. We have found that our clock is best set at 17n with a period of 7.5n. All reset,select, clock, clock bar and serial are connected to each other so only one pin set is required. We have not noticed any signal degradation with our design so we did not place buffers on the clock signal. These will be added in the final desgin that goes into the pad frame.

D FF = D Flip Flop, AND = AND gate, MUX = 2 bit Mutliplexor, INV = inverter

##### (3) **(25pts)** Simulation Results (without padframe):

1. (5 pts total) Individual cells:

###### Full Adder:

A close up of a map

Description automatically generated

###### Full Adder with AND gate:



###### Registers (Test Mode):



###### Ring Oscillator (If used): N/A

1. (20 pts) The final multiplier:

Before or after the shifter ???

##### (4) **(10 pts)**

###### Layout of the final design (with padframe):

(5) **(20 pts)**

###### Simulation waveforms for the final design (with padframe):