t4_21 Project Status			
Project File:	TestingAndFaultToleranceInDigitalSystems.xise	**Parser Errors:**	No Errors
Module Name:	t4_21	**Implementation State:**	New
Target Device:	xc6slx45-3csg324	**• Errors:**	
Product Version:	ISE 14.7	**• Warnings:**	
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:		**• Final Timing Score:**	

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report					
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**

Date Generated: 04/16/2019 - 18:22:56