**CPE301 – SPRING 2019**

Design Assignment 2B

Student Name: John Galanza

Student #: 5002981771

Student Email: galanj1@unlv.nevada.edu

Primary Github address: <https://github.com/JohnGalanza>

Directory: <https://github.com/JohnGalanza/supersmashjoe>

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

* Atmega328p
* Multifunctional Shield
* USB cable
* Headphones

1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1**

**Task 1 (Initial code used from previous DA)**

; DA2T2.asm

;

CBI DDRC,2 ;makes PC2 an input

LDI R19, 0x04

OUT DDRB, R19 ;makes PB2 an output port

L1: SBIC PINC,2 ;Skip if bit PB2 is LOW

RJMP L1 ;checks if bit is 0

SBI PORTB,2 ;turns on port b

CALL Delay ;delays for 1.250s

CBI PORTB,2 ;clears port b

RJMP HERE

Delay:

LDI R16,102

LDI R17,118

LDI R18,194

L2: DEC R18

BRNE L2

DEC R17

BRNE L2

DEC R16

BRNE L2

HERE:RJMP HERE

1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**

**Task 1 in assembly (Modified for interrupts using INT0 and PD2)**

; DA2B\_A.asm

.include<m328pdef.inc>

.ORG 0

JMP MAIN

.ORG 0x02

JMP EX0\_ISR

MAIN:

SBI DDRB,2 ;Port B2 an output

SBI PORTB,2 ;Turn led off

SBI PORTD,2 ;activate pull up

LDI R20, 0x2 ;Int0 falling edge

STS EICRA,R20

LDI R20, HIGH(RAMEND) ;setup stack

OUT SPH, R20

LDI R20, LOW(RAMEND)

OUT SPL, R20

LDI R20, 1<<INT0

OUT EIMSK, R20

SEI ;checks INT0 if changed

RJMP MAIN ;Repeats

EX0\_ISR:

CBI PORTB, 2 ;turn led on

LDI R16,102 ;Start of delay for 1.25s

LDI R17,118

LDI R18,194

L2: DEC R18

BRNE L2

DEC R17

BRNE L2

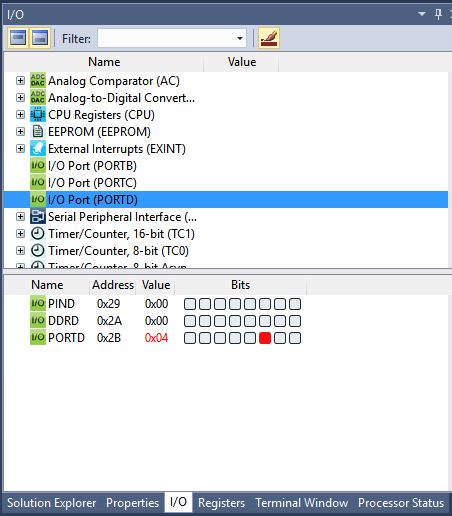
DEC R16

BRNE L2

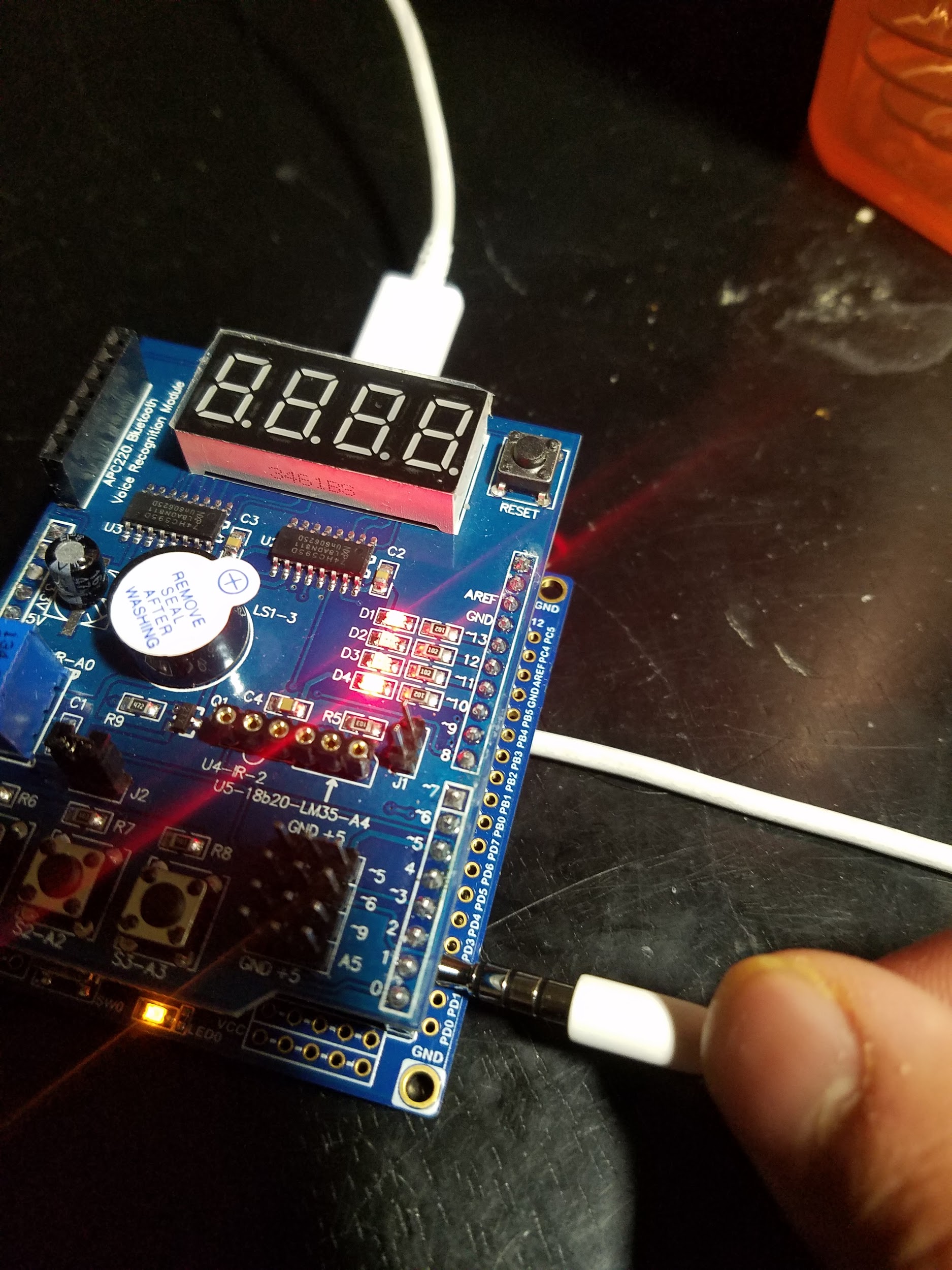
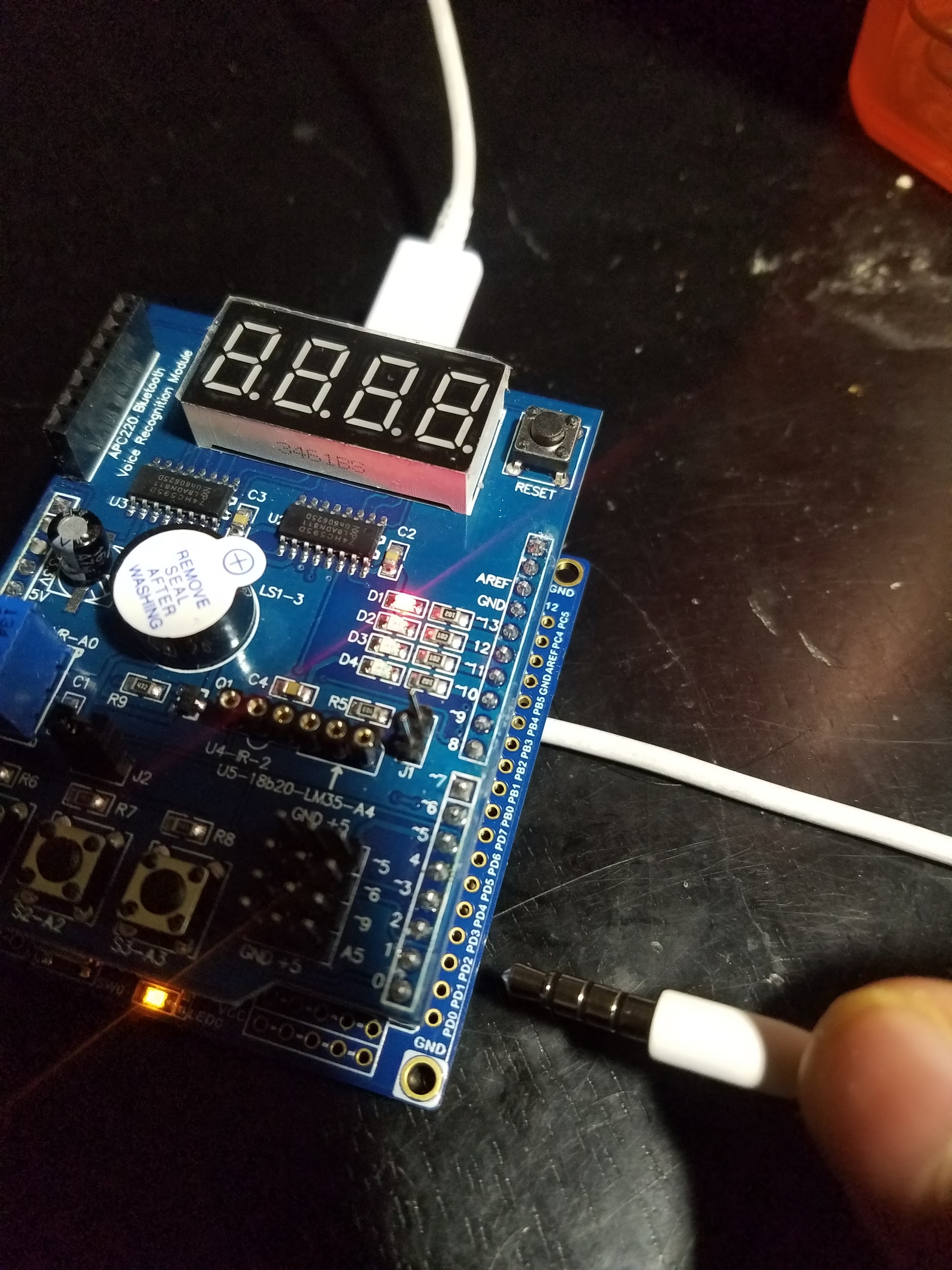
RETI

1. **SCHEMATICS**

Use fritzing.org

1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)** 

This shows PD2 active

1. **SCREENSHOT OF EACH DEMO (BOARD SETUP** 
2. **VIDEO LINKS OF EACH DEMO**

https://youtu.be/XxjnjKpVzEc

1. **GITHUB LINK OF THIS DA**

https://github.com/JohnGalanza/supersmashjoe/tree/master/DA2B

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“*This assignment submission is my own, original work*”.

John GalanzaT