Features

- **Interfaces Directly to Instrument Hardware**
  - **Keyboard Velocity Scanner (Up to 88 Keys, 64 µs Time Accuracy, Log Timescale)**
  - **Switch Scanner (Up to 176 Switches)**
  - **LED Display Controller (Up to 88 LEDs)**
  - **Slider Scanner (Built-in ADC, Up to 16 Sliders)**
  - **LCD Display (8-bit Interface)**
- **Crisp Musical Response**
  - **45 MHz Built-in 16-bit Microcontroller**
  - **Interface with Keyboard/Switches through Built-in Shared Memory**
- **High-quality Sound**
  - **64-slot Digital Sound Synthesizer/Processor**
  - **Multi-algorithm: PCM with Dynamic LP Filter, FM, Delay Lines for Effects, Equalizer, Surround, Digital Audio-in Processing**
  - **Compatible with ATSAM97xx Sounds and Firmware**
  - **44.1 kHz Sampling Rate**
  - **Up to 16 MB x 16 ROM/RAM for Firmware, Orchestration and PCM Data**
  - **Up to 4 Channels Audio-out, 2 Channels Audio-in**
- **Top Technology**
  - **144-lead TQFP Space-saving Package**
  - **Single 11.2896 MHz Crystal Operation, Built-in PLL Minimizes RFI**
- **Available Soundbanks for General MIDI® (GM)[1] or High-quality Piano**
  - **CleanWave® 1-Mbyte and 4-Mbyte Sample Sets (Free License)**
  - **High-quality 2-Mbyte Piano and Strings Sample Sets**
  - **Other Sample Sets Available Under Special Licensing Conditions**
- **Quick Time-to-market**
  - **Proven Reliable Synthesis Drivers**
  - **In-circuit Emulation with CodeView Debugger for Easy Prototype Development**
  - **Built-in External Flash Programming Algorithm, Allows On-board Flash Programming**
  - **All Existing ATSAM97xx Tools Available for Sound and Sound-bank Development**

Note: 1. General MIDI requires a license from Midi Manufacturers Association.

Description

The ATSAM9753 integrates into a single chip an ATSAM97xx core (64-slot DSP and 16-bit processor), a 32K x 16 RAM, an LCD display interface and a scanner, allowing direct connection to velocity-sensitive keyboards, switches, LEDs and sliders. With the addition of a single external ROM or Flash and a stereo DAC, a complete low-cost musical instrument can be built that includes reverb and chorus effects, parametric equalizer, surround effects, orchestrations, pitch-bend and wheel controller, without compromising on sound quality. The ATSAM9753 is packaged in a standard 144-lead TQFP package.

Sound Synthesis

ATSAM9753 Integrated Digital Music Instrument

Rev. 1774D–DRMSD–11/02

Figure 1. Typical Application for the ATSAM9753

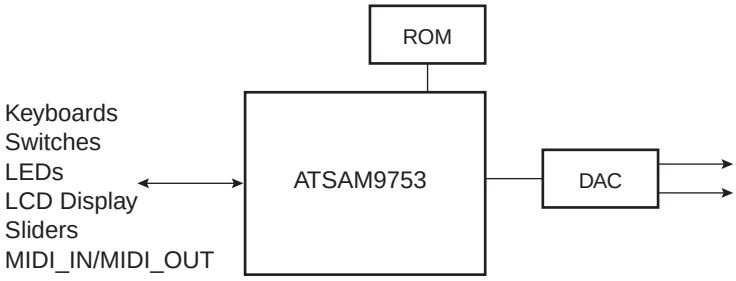
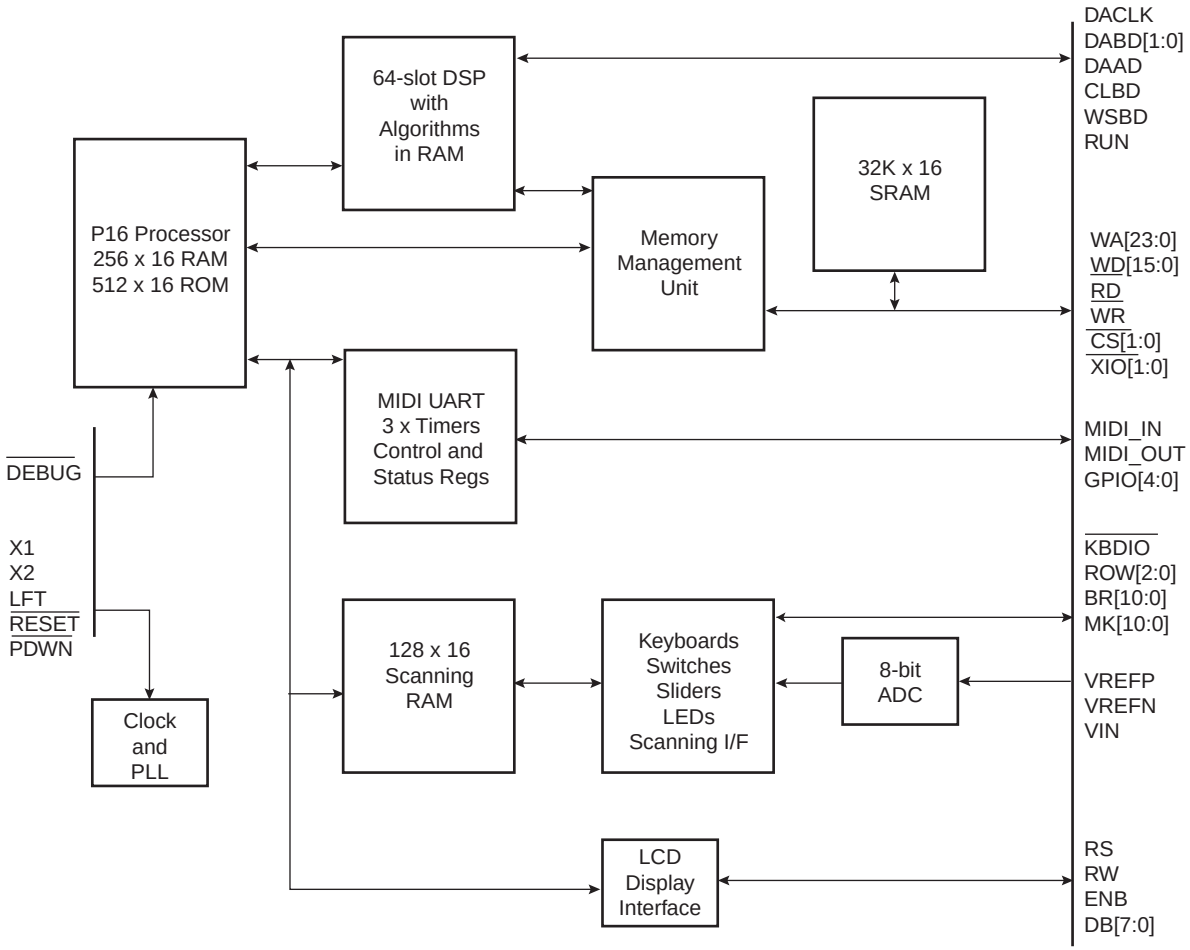


Figure 2. ATSAM9753 Block Diagram



Pin Description

Table 1. Pin Description by Function

Pin Name	Pin Number	Type	Function
Power Supply(1)			
GND	4, 17, 24, 32, 42, 52, 56, 65, 77, 90, 97, 102, 110, 125, 130, 140	PWR	Digital Ground All pins should be connected to a ground plane.
AGND	103	PWR	Analog Ground for the ADC
VCC	5, 18, 31, 41, 51, 66, 78, 91, 111, 126, 139	PWR	Power Supply, 3.3V/5V ± 10% All pins should be connected to a V_{CC} plane.
VC3	23, 55, 96, 101, 129	PWR	Core power, +3.3V nominal (3.3V ± 10%). All V_{C3} pins should be returned to +3.3V.
AVC3	107	PWR	Analog power for the ADC, +3.3V nominal (3.3V ± 10%)
Serial MIDI			
MIDI_IN	94	IN	Serial MIDI_IN
MIDI_OUT	95	OUT	Serial MIDI_OUT
External PCM ROM/RAM/I/O			
WA[23:0]	47 - 50, 53, 54, 57 - 64, 67 - 76	OUT	External memory I/O address. Up to 16M x 16 for direct ROM/RAM connection.
WD[15:0]	19 - 22, 25 - 30, 33 - 38	I/O	External memory I/O data. Data is read (input) when $\overline{RD}$ is low, written (output) when $\overline{WR}$ is low.
$\overline{RD}$	39	OUT	External ROM/RAM/peripherals read
$\overline{WR}$	40	OUT	External RAM/peripherals write
$\overline{CS[1:0]}$	43, 44	OUT	Programmable chip selects. Can be configured to handle several ROMs or mixed RAM/ROM/FLASH.
$\overline{XIO[1:0]}$	45, 46	OUT	External peripherals chip select. Each peripheral maps onto 4K bytes address space for optional further decoding.
Keyboard, Switches, LEDs, Sliders, Scanning			
$\overline{KBDIO}$	119	OUT	If 1: BR[10:0] and MK[10:0] hold keyboard contact input data. If 0: BR[10:0] holds switch status input, MK[10:0] holds LED data output.
ROW[2:0]	115 - 117	OUT	Row select: Keyboard, switches/LEDs, external slider analog multiplexer (4051) channel select. Eight rows combined with eleven BR/MK columns allow to control 88 keys, 88 switches, 88 LEDs and 8 sliders. The programmable bit GPIO0 allows control to be extended to 176 switches and 16 sliders when programmed as ROW3.

Table 1. Pin Description by Function (Continued)

Pin Name	Pin Number	Type	Function
BR[10:0]	1 - 3, 135 - 138, 141 - 144	IN	Keyboard contact 1/switch status. When $\overline{\text{KBDIO}}$ = 1 then BR[10:0] holds the keyboard key-off or first contact status. This can be configured as normally closed (spring type), normally open (rubber type), common anode or common cathode contact diodes. When $\overline{\text{KBDIO}}$ = 0 then BR[10:0] holds the switch status from ROW[2:0] or ROW[3:0].
MK[10:0]	120 - 124,127, 128, 131 - 134	I/O	Keyboard contact 2/LED data. When $\overline{\text{KBDIO}}$ =1 then MK[10:0] holds the keyboard key-on or second contact status. This can be configured as common anode or common cathode contact diodes.When $\overline{\text{KBDIO}}$ = 1 then MK[10:0] holds the led data from ROW[2:0].
VREFP	106	ANA	Positive reference voltage. Should normally be connected to a clean AV_{C3} supply.
VREFN	105	ANA	Negative reference voltage. Should normally be connected to a clean AGND.
VIN	104	ANA	Slider analog input. Ranges from VREFN to VREFP. Should hold the ROW[2:0] or ROW[3:0] slider voltage. Multiple sliders should be connected through external analog multiplexer(s) like 4051.
LCD Display Interface(2)			
RS	16	OUT	Select instruction (LOW) or data (HIGH).
RW	15	OUT	Select write (LOW) or read (HIGH).
ENB	14	OUT	Enable, active high.
DB[7:0]	6 - 13	I/O	Bi-directional data bus.
Digital Audio Group(3)			
DACLK	93	OUT	Master clock for sigma-delta DAC (256 x Fs).
DABD[1:0]	89, 92	OUT	Serial data for two stereo output channels.
DAAD	88	IN	Serial data for one stereo input channel.
CLBD	86	OUT	Digital audio bit clock.
WSBD	87	OUT	Digital audio left/right select.
Miscellaneous Pins			
GPIO[4:0]	108, 109, 112 - 114	I/O	These pins can be used individually as general-purpose I/Os or as alternate functions. When used as general-purpose I/Os, they can be individually configured as inputs or outputs. When used as alternate functions their meaning changes as follows: GPIO0 = ROW3 expands switches to 176, sliders to 16 GPIO2 = DBCLK (input) GPIO3 = DBACK (output) GPIO4 = DBDATA (I/O) (DBDATA input = DBIN, DBDATA output = DBOUT) DBCLK, DBACK, DBDATA are used for debugging or external Flash memory programming when $\overline{\text{DEBUG}}$ is low
$\overline{\text{DEBUG}}$	85	IN	Configuration pin, low for CodeView debugging/external Flash memory programming. Should be tied to V_{CC} for normal operation.
$\overline{\text{RESET}}$	83	IN	Reset input, active low. This is a Schmitt trigger input, allowing direct connection of a RC network.
RUN	118	OUT	Indicates that the DSP is up and running. Can be used as external DAC reset.

Table 1. Pin Description by Function (Continued)

Pin Name	Pin Number	Type	Function
$\overline{\text{PDWN}}$	84	IN	Power down, active low. When power down is active, all output pins are floating except GPIO1. The crystal oscillator is stopped. To exit from power-down mode, $\overline{\text{PDWN}}$ should be high and $\overline{\text{RESET}}$ applied.
X1 X2	98, 99	–	11.2896 MHz (nominal) crystal connection. An external clock can also be used at X1.
TEST[3:0]	79 - 82	IN	Test pins, should be grounded
LFT	100	–	PLL external RC network

Notes:
1. Like all high-speed HCMOS ICs proper decoupling is mandatory for reliable operation and RFI reduction. The recommended decoupling is 100 nF at each corner of the IC with an additional 10 µF bulk capacitor close to the X1, X2 pins.
2. The LCD display interface signals are controlled by firmware, therefore, their timing relationship is determined by firmware only.
3. The ATSAM9753 connects to a variety of stereo DACs or Codecs from 16 to 20 bits, with Japanese or I^2S format. This includes AD1857JRS, AK4352, AK4393, AK4528, PCM1718, PCM1739, PCM3001, TDA1543, TDA1545 . When Japanese format is used, only 16 bits is supported without external circuitry.

Table 2. Pinout by Pin Number

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	BR8	37	WD1	73	WA3	109	GPIO1
2	BR9	38	WD0	74	WA2	110	GND
3	BR10	39	$\overline{RD}$	75	WA1	111	VCC
4	GND	40	$\overline{WR}$	76	WA0	112	GPIO2
5	VCC	41	VCC	77	GND	113	GPIO3
6	DB7	42	GND	78	VCC	114	GPIO4
7	DB6	43	$\overline{CS1}$	79	TEST0	115	ROW0
8	DB5	44	$\overline{CS0}$	80	TEST1	116	ROW1
9	DB4	45	$\overline{XIO1}$	81	TEST2	117	ROW2
10	DB3	46	$\overline{XIO0}$	82	TEST3	118	RUN
11	DB2	47	WA23	83	$\overline{RESET}$	119	$\overline{KBDIO}$
12	DB1	48	WA22	84	$\overline{PDWN}$	120	MK10
13	DB0	49	WA21	85	$\overline{DEBUG}$	121	MK9
14	ENB	50	WA20	86	CLBD	122	MK8
15	RW	51	VCC	87	WSBD	123	MK7
16	RS	52	GND	88	DAAD	124	MK6
17	GND	53	WA19	89	DABD0	125	GND
18	VCC	54	WA18	90	GND	126	VCC
19	WD15	55	VC3	91	VCC	127	MK5
20	WD14	56	GND	92	DABD1	128	MK4
21	WD13	57	WA17	93	DACLK	129	VC3
22	WD12	58	WA16	94	MIDI_IN	130	GND
23	VC3	59	WA15	95	MIDI_OUT	131	MK3
24	GND	60	WA14	96	VC3	132	MK2
25	WD11	61	WA13	97	GND	133	MK1
26	WD10	62	WA12	98	X1	134	MK0
27	WD9	63	WA11	99	X2	135	BR0
28	WD8	64	WA10	100	LFT	136	BR1
29	WD7	65	GND	101	VC3	137	BR2
30	WD6	66	VCC	102	GND	138	BR3
31	VCC	67	WA9	103	AGND	139	VCC
32	GND	68	WA8	104	VIN	140	GND
33	WD5	69	WA7	105	VREFN	141	BR4
34	WD4	70	WA6	106	VREFP	142	BR5
35	WD3	71	WA5	107	AVC3	143	BR6
36	WD2	72	WA4	108	GPIO0	144	BR7

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (All Voltages with Respect to 0V, GND = 0V)

Ambient Temperature (Power Applied).....-40°C to + 85°C Storage Temperature.....-65°C to + 150°C Voltage on any pin (except X1).....-0.5V to V_{CC} + 0.5V Voltage on X1 pin .....-0.5V to V_{C3} + 0.5V V_{CC} Supply Voltage.....-0.5V to + 6.5V V_{C3} Core Supply Voltage.....-0.5V t0 +4.5V AV_{C3} Supply Voltage.....-0.5V t0 +4.5V Maximum I_{OL} per I/O pin.....10mA	*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage (I/O)	3	3.3/5.0	5.5	V
V_{C3}	Supply voltage (Core)	3	3.3	3.6	V
AV_{C3}	Supply voltage (Analog)	3	3.3	3.6	V
t_A	Operating ambient temperature	0		70	°C

DC Characteristics

Table 5. DC Characteristics (T_A = 25°C, V_{CC} = 5V ± 10%, V_{C3} = 3.3V ± 10%)

Symbol	Parameter	VCC	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage	3.3 5.0	-0.5 -0.5		1.0 1.7	V
V_{IH}	High-level input voltage	3.3 5.0	2.3 3.3	3	V_{CC} + 0.5 V_{CC} + 0.5	V
V_{OL}	Low-level output voltage at I_{OL} = 3.2 mA(1)	3.3 5.0			0.45 0.45	V
V_{OH}	High-level output voltage at I_{OH} = -0.8 mA (2)	3.3 5.0	2.8 4.5			V
I_{CC} Core I_{CC} I/O	Power supply current (Crystal frequency = 11.2896 MHz)	3.3 5.0		60 20	80 30	mA
	Power down supply current			1	2	µA

Notes: 1. I_{OL}: Low-level output current.
2. I_{OH}: High-level output current.

Product Overview

The ATSAM9753 is part of a new generation of integrated solutions for electronic musical instruments. The device includes all key circuitry on a single silicon chip: sound synthesizer/processor, 16-bit control processor, interface with keyboards, switches, sliders, LEDs, LCD display, etc.

The synthesis/sound processing core of the ATSAM9753 is taken from the ATSAM97xx series, the quality of which has already been demonstrated through dozens of different musical products: electronic pianos, home keyboards, professional keyboards, classical organs and sound expanders. The maximum polyphony is 64 voices without effects. A typical application is 38-voice polyphony with reverb, chorus, 4-band equalizer and surround.

The ATSAM9753 is directly compatible with most available musical keyboards. This includes configuration options for spring- or rubber-type contacts and for common anode- or common cathode-type matrices. A 64 µs timing accuracy for velocity detection provides a very reliable dynamic response even with low-cost unweighted keyboards. The time between contacts is coded with 256 steps on a logarithmic time scale, then converted by software to a 128-step MIDI scale according to the type of keyboard and selected keyboard sensitivity.

The ATSAM9753 can handle directly up to 176 switches. Switches, organized in matrix form, require only a serial diode. Up to 88 LEDs can be directly controlled by the ATSAM9753 in a time-multiplexed way. Additional LEDs can be connected through additional external shift registers using the GPIO lines (general-purpose I/O lines) of the ATSAM9753. The built-in analog-to-digital converter of the ATSAM9753 allows connection of continuous controllers like pitch-bend wheel, modulation, volume sliders, tempo sliders, etc. Up to 16 sliders can be connected.

The ATSAM9753 can be directly connected to most LCD displays through an 8-bit dedicated data bus and three control signals.

Configuration options allow the ATSAM9753 to cover a wide range of musical products, from the lowest-cost keyboard to the high-range digital piano, thanks to flexible memory and I/O organization: built-in 64K bytes of RAM and up to 32M bytes of external memory for firmware, orchestration and PCM data. The external memory can be ROM, RAM or Flash. Memory types can be mixed, but for most applications there is no need for external RAM memory as the built-in 64K bytes of RAM is enough to handle firmware variables and reverb delay lines. External Flash memory can be programmed on-board from a host processor through the ATSAM9753.

The ATSAM9753 operates from a single 11.2896 MHz crystal. A built-in PLL raises the frequency to 45.2 MHz for internal processing. This allows radio frequency interference (RFI) to be minimized, making it easier to comply with FCC, CSA and CE standards.

A power-down feature is also included which can be controlled externally ($\overline{\text{PDWN}}$ pin). This makes the ATSAM9753 very suitable for battery-operated instruments.

The ATSAM9753 was designed with a rapid time-to-market in mind. The ATSAM9753 product development program includes key features to minimize product development efforts:

- Specialized debug interface, allowing on-target software development with a source code “CodeView” debugger
- Standard sound generation/processing firmware
- Standard orchestration firmware
- Windows® tools for sounds, soundbanks and orchestration developments
- Standard soundbanks
- Strong technical support available directly from Dream®

Architectural Overview

The highly integrated architecture from ATSAM9753 combines a specialized high-performance RISC-based digital signal processor (DSP) and a general-purpose 16-bit CISC-based control processor (P16). An on-chip memory management unit (MMU) allows the DSP and the control processor to share an internal 32K x 16 RAM as well as external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the on-chip MIDI UART and three timers, with minimum intervention from the control processor. A keyboard/switches/sliders/LEDs autonomous scanning interface handles the specific musical instrument peripherals, including accurate keyboard velocity detection and communicates with the control processor through a dedicated 128 x 16 dual-port RAM. An LCD display interface allows direct connection to common LCD displays.

DSP Engine

The DSP engine operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is itself divided into 16 micro-instructions known as algorithms. Up to 32 DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications.

The DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24 dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical musical instrument application will use a little more than half the capacity of the DSP engine for synthesis, thus providing state-of-the-art 38-voice synthesis polyphony. The remaining processing power may be used for typical functions such as reverberation, chorus, surround effect, equalizer, etc.

Frequently-accessed DSP parameter data are stored into five banks of on-chip RAM memory. Sample data or delay lines that are accessed relatively infrequently are stored in external ROM, or in the built-in 32K x 16 RAM. The combination of localized microprogram memory and localized parameter data allows micro-instructions to execute in 22 ns (45 MIPS). Separate buses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to six simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 270 million operations per second (MOPS).

P16 Control Processor and I/O Functions

The P16 control processor is a general-purpose 16-bit CISC processor core, which runs from external memory. A debug ROM is included on-chip for easy development of firmware directly on the target system. This ROM also contains the necessary code to directly program externally connected Flash memory. The P16 includes 256 words of local RAM data memory for use as registers, scratchpad data and stack.

The P16 control processor writes to the parameter RAM blocks within the DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the scanning interface and then controls the DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the scanning interface through specialized “intelligent” peripheral I/O logic. This I/O logic

automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single ROM device to serve as sample memory storage for the DSP and as program storage for the P16 control processor. An internal 32K x 16 RAM is also connected to the MMU, allowing RAM resources to be shared between the DSP for delay lines and the P16 for program data.

Scanning Interface

The scanning interface consists of hardwired logic. It time-multiplexes keyboards, switches and LED connections, thus minimizing the amount of wiring required. It communicates with the P16 through an 128 x 16 dual-port RAM and a few control registers. When a new incoming event is detected, such as key-on, key-off or switch change, the scanning interface will notify the P16 by indicating the type of event. The P16 then simply reads the dual-port RAM to get the corresponding parameter, such as velocity or switch status. Conversely, the P16 simply writes into the dual-port RAM the LED states to be displayed and the scanning interface will then take care of time-multiplexing the display.

The scanning interface uses an unique key velocity detect scheme with a pseudo-logarithmic time scale. This allows velocities to be accurately detected, even when keyboard keys are pressed very softly.

Finally, a built-in 8-bit analog-to-digital converter (ADC) allows the connection of up to 16 continuous controllers through external analog multiplexers such as the 4051.

LCD Display Interface

The LCD display interface uses a dedicated bi-directional data bus (DB[7:0]), an instruction/data control (RS), a read/write signal (R/W) and an enable signal (ENB). Built-in features are included to accommodate even the slowest LCD displays.

Flash Programming

The ATSAM9753 enables Flash memory programming in three different ways:

- Blank Flash programming is done by the debug interface. This mode is very slow and should be reserved for the initial boot sector programming.
- Program update. All the Flash content can be re-programmed. The ATSAM9753 cannot play music during the Flash erase and programming. A specific firmware is used to program Flash with the DSP.
- Parameter update, e.g., in keyboard applications, backup parameter and sequencer song. If the Flash enables concurrent read while program/erase, it is possible to backup parameters in the upper memory plane while the microprocessor firmware is running on the lower plane. The ATSAM9753 cannot play music during the parameter backup because sound samples are stored in both memory planes.

Flash Features

- 3.3V or 5V: In case of 3.3V, the I/O voltage V_{CC} should be supplied by 3.3V and all the external components (MIDI, DAC, ...) should be 3.3V
- Access time: 100 ns (for 11.2896 MHz crystal)
- Bottom boot
- Dual plane with concurrent read while program/erase recommended for parameters backup

Timing Diagrams

All timings are relative to 11.2896 MHz crystal between X1 and X2.

Figure 3. Scanning Timings (Keyboard, Switches, LEDs and Sliders) Timing Diagram

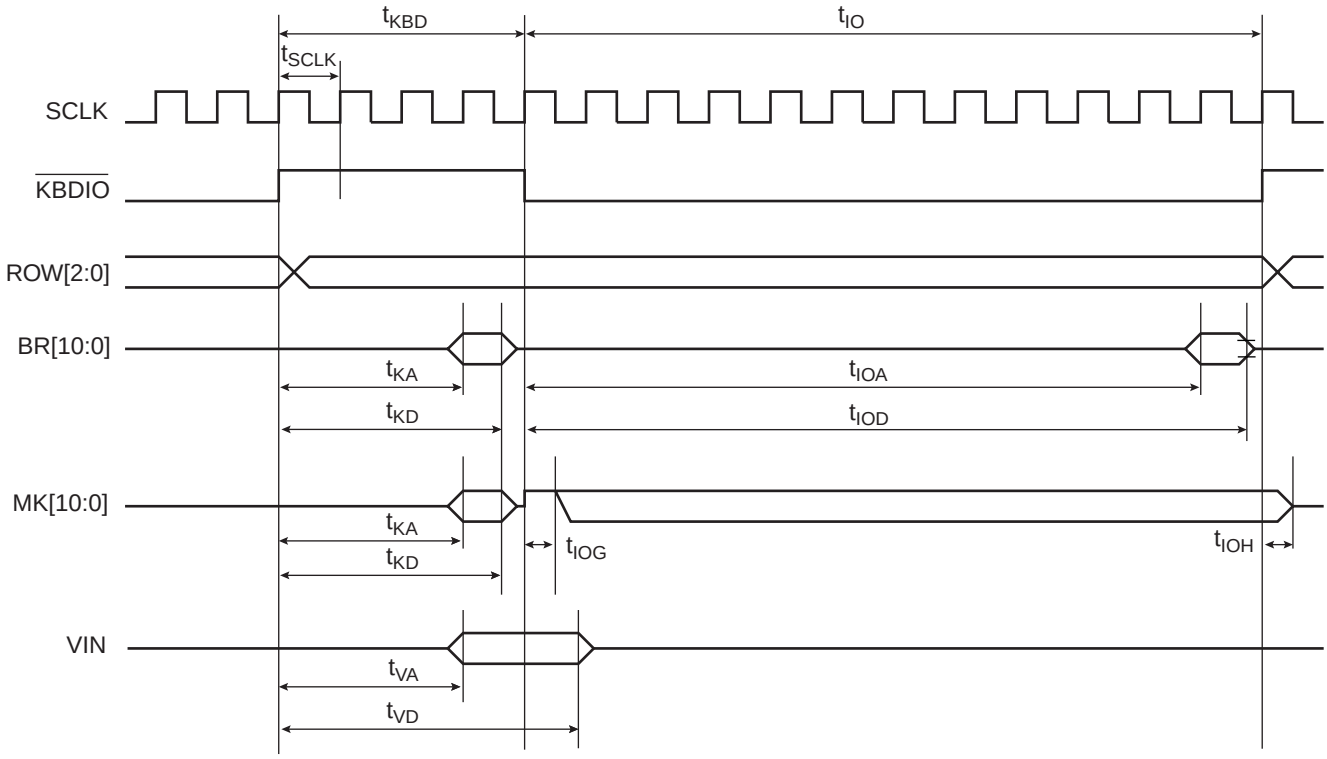


Table 6. Scanning Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{KBD}	Keyboard access ($\overline{KBDIO}$ high time)		1.4		µs
t_{IO}	Switches/leds access ($\overline{KBDIO}$ low time)		4.3		µs
t_{SCLK}	Internal scanning clock period		354		ns
t_{KA}	Break (contact1) and Make (contact2) data from keyboard valid from rising $\overline{KBDIO}$			1.2	µs
t_{KD}	Break (contact1) and Make (contact2) data from Keyboard floating from rising $\overline{KBDIO}$	1.3		1.6	µs
t_{IOA}	Switch data valid from falling $\overline{KBDIO}$			4	µs
t_{IOD}	Switch data floating from falling $\overline{KBDIO}$	4.1		4.4	µs
t_{IOG}	LED data MK guard time	177		27	ns
t_{IOH}	LED data floating from rising $\overline{KBDIO}$	0		88	ns
t_{VA}	Analog V_{IN} sample start time from ROW change (Start sample and hold voltage follow mode)	1			µs
t_{VD}	Analog V_{IN} sample end time from ROW change (Switch to hold mode)			2.2	µs

External Memory (16 bits)

Figure 4. External ROM, RAM, I/O Timing Diagram

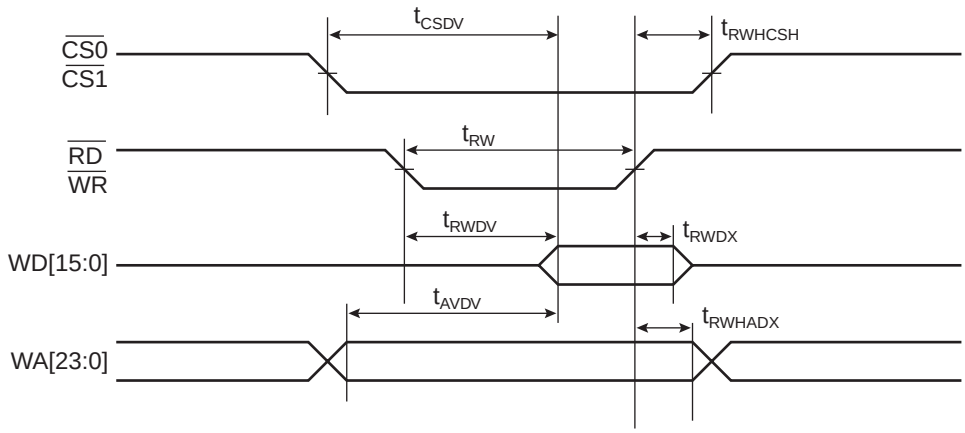


Table 7. External ROM, RAM, I/O Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSDV}	Access time from $\overline{CSx}$ low	106			ns
t_{RWDV}	Access time from $\overline{RD}$, $\overline{WR}$ low	61			ns
t_{AVDV}	Access time from address valid	106			ns
t_{RW}	$\overline{RD}$, $\overline{WR}$ pulse width		89		ns
t_{RWHCSH}	$\overline{CSx}$ high from rising $\overline{RD}$ or $\overline{WR}$	10			ns
t_{RWHADX}	Address valid after rising $\overline{RD}$ or $\overline{WR}$	10			ns
t_{RWDX}	Data hold time from rising $\overline{RD}$ or $\overline{WR}$	10			ns

Digital Audio

Figure 5. Digital Audio Timing Diagram

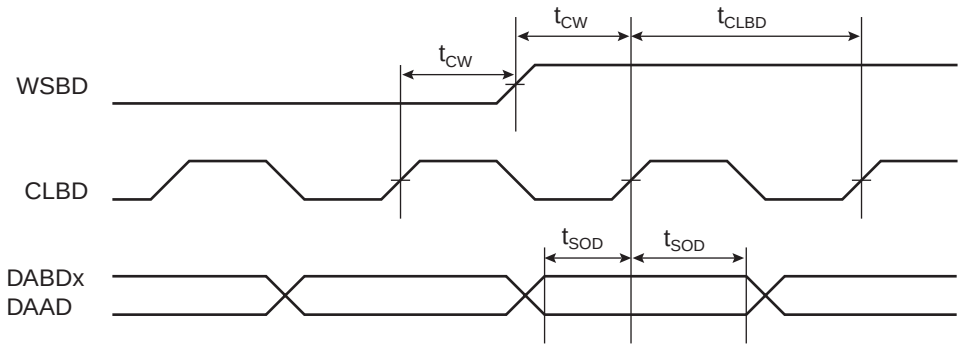
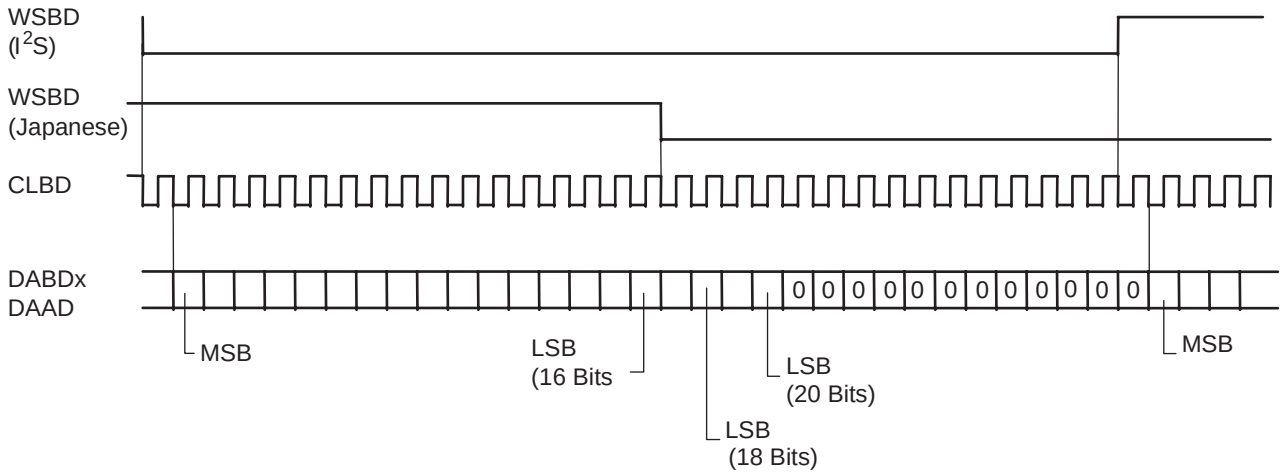


Table 8. Digital Audio Timing Parameters

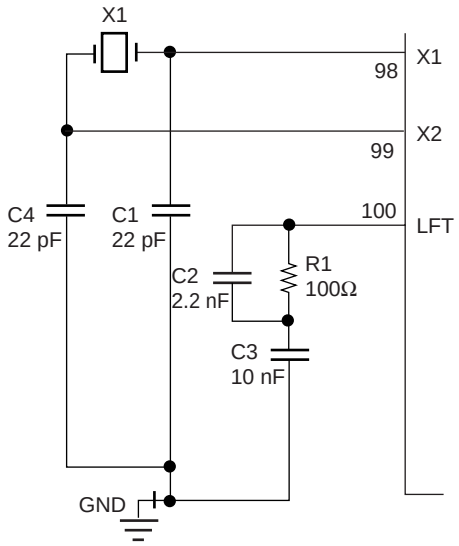
Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD rising to WSBD change	167			ns
t_{SOD}	DABDx valid prior to/after CLBD rising	167			ns
t_{CLBD}	CLBD cycle time		354		ns

Figure 6. Digital Audio Frame



Crystal Compensation and LFT Filter

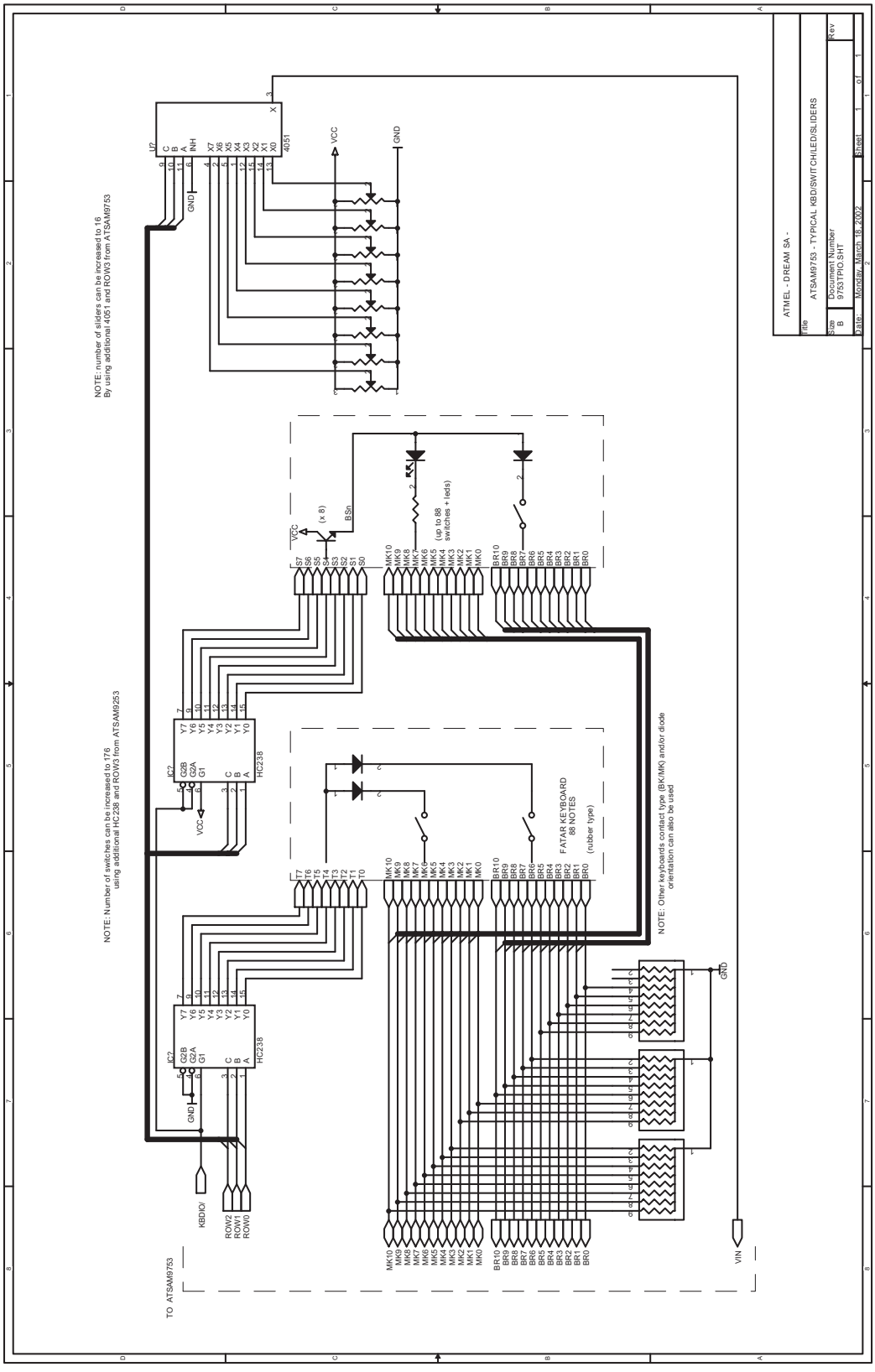
Figure 7. Recommended Crystal Compensation and LFT Filter [1], [2], [3], [4]



Notes:
1. All GND pins should be connected to GND plane below IC.
2. All VCC pins should be connected to VCC plane below IC.
3. X1, C1, C2, C3, C4, R1 connections should be short and shielded. The GND return from C1, C4, C3, should be the GND plane from ATSAM9753.
4. 0.1 µF decoupling caps should be placed at each corner of the IC. An additional 10 µF capacitor should be placed close to X1.

Reference Design

Typical Keyboard, Switch LED and Slider Connections



ATSAM9753 Operation

The reader is assumed to be familiar with the functioning of the ATSAM97xx series. Refer to the ATSAM9707 product development kit “prgdvkit.pdf” document. This document can be obtained under special conditions from Atmel.

This section describes operation and registers specific to ATSAM9753.

Memory Mapping

Table 9. Memory Mapping

Size (in words)	Address Low	Address High	Access
256	000:0000	000:00FF	ATSAM97xx standard routine ROM
768	000:0100	000:03FF	Built in debug ROM
32M - 1K	000:0400	1FF:FFFF	External ROM/Flash ($\overline{CS0}$)
32K	200:0000	200:7FFF	Built in SRAM
4K	200:8000	200:8FFF	External memory page XIO0 ($\overline{XIO0}$)
4K	200:9000	200:9FFF	External memory page XIO1 ($\overline{XIO1}$)
216K	200:A000	203:FFFF	Not used
32M - 256K	204:0000	2FF:FFFF	External SRAM ($\overline{CS1}$)

I/O Mapping

The I/O Mapping Table refers to the ATSAM9707 product development kit “prgdvkit.pdf” available from Atmel.

Table 10. I/O Mapping

Write	Read	Access
00 - 09	00 - 09	Standard ATSAM97xx I/O (Refer to prgdvkit.pdf)
0A	0A	LCD port
0B	X	Keyboard configuration
0C - 0E	0C - 0E	Scanning port ADD0 - 2
0F	0F	GPIO control/status

LCD Interface

The ATSAM9753 can be directly connected to most LCD displays.

The ATSAM9753 provides an 8-bit data bus (DB[7:0]) and three output control pins RS, RW and ENB.

All the LCD pins are controlled by I/O access ADD OAH. The I/O reads only the 8-bit data bus. The I/O writes into the 11-bit LCD_Reg. Refer to Table 11 and Table 12.

Table 11. LCD Interface

LCD_Reg[7:0]	DB[7:0]
LCD_Reg[8]	RS
LCD_Reg[9]	RW
LCD_Reg[10]	ENB

Table 12. LCD Interface

I/O Access	I/O Data	LCD_Reg[10:0]	DB[7:0]	R/W	
Write	IOD[10:0] (IOD[9]=0)	IOD[10:0] LCD_Reg[9]=0	IOD[7:0] output	0	Set LCD in write mode
Write	IOD[10:0] (IOD[9]=1)	IOD[10:0] LCD_Reg[9]=1	LCD_D[7:0] input	1	Set LCD in read mode
Read	xx	LCD_Reg[9]=0	LCD_Reg[7:0] output	0	Invalid read from LCD in write mode
Read	xxx, LCD_D[7:0]	LCD_Reg[9]=1	LCD_D[7:0] input	1	Read from LCD

Keyboard Configuration Register

The configuration register allows the user to work with a variety of keyboards. This write-only 2-bit register is mapped to the address OBH in the I/O space.

Reg[0] = contact type 0 for rubber type contact

1 for spring type contact

Reg[1] = diode wiring 0 for common anode wiring

1 for common cathode wiring

The default configuration (power-up) is common anode (Reg[1] = 0) and rubber contact (Reg[0] = 0) which corresponds to most popular keyboards.

Scanning Interface

The ATSAM9753 has built-in specialized hardware that allows the following functions:

- Scanning of up to 88 keys from an external keyboard, with key-on and key-off velocity measurement (time between contacts)
- Scanning of up to 176 switches
- Time multiplex control of up to 88 LEDs
- Analog-to-digital conversion of up to 16 analog sources

The P16 interfaces with the scanning using a three-address port located at 0CH to 0EH in the I/O mapping.

This port enables access to the keyboard RAM. This 128 x 11 RAM is mapped as shown in Table 13.

Table 13. Keyboard RAM Mapping

Address	Content
00H to 57H	Key velocity and status
58H to 5FH	LED data
60H to 6FH	Switch status
70H to 7FH	ADC value

Keyboard Status

(I/O address OCH read-only)

D[7] KRQ flag = 1 indicates that a key-on or key-off has been detected and that the P16 service is requested. This flag is automatically cleared by writing to data H for the detected key.

D[6:0] specifies which keyboard key is requesting the service, valid only if KRQ flag = 1. Key number ranges from 0 to 87.

RAM Address

(I/O address OCH write-only)

D[6:0] RAM address css

D[7] don't care

Table 14. RAM Address

Address	Index	Content
00H to 57H	8 x i + ROW[2:0]	Key velocity and status
58H to 5FH	ROW[2:0]	LED data
60H to 6FH	ROW[3:0]	Switch status
70H to 7FH	ROW[3:0]	ADC value

“i” refers to the MKi or BRi signal number that ranges from 0 to 10. For example, the information regarding the key at ROW3, column MK5/BR5, is found at RAM address 8*5+3 = 43.

The scanning hardware cycles the ROW[2:0] signals from 0 to 7 to the output pins in 45 µs (5.7 µs per row). If the alternate function ROW3 is not used, then the switch status and ADC value information are aliased (data from 68H to 6FH = data from 60H to 6FH, data from 78H to 7FH = data from 70H to 77H).

RAM Data	DataL[7:0]	I/O address ODH, Data[7:0]
	DataH[2:0]	I/O address OEH, Data[10:8]
	DataH[7:3]	don't care

Table 15. Scanning RAM Data Format

	Bit										
	10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Key Velocity and Status	SRQ	ON	BUSY	TIME							
LED Data	MK10	MK9	MK8	MK7	MK6	MK5	MK4	MK3	MK2	MK1	MK0
Switch Data	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
ADC Status	X	X	X	ADC DATA							

- Key Velocity and Status:
  - SRQ: If 1, indicates that the velocity detection is complete and that this key requests attention from the P16. In this case BUSY = 0, ON and TIME hold valid information.
  - ON: 1 indicates key-on, 0 indicates key-off. Valid only if SRQ = 1.
  - BUSY: Used internally by the scanning hardware, indicates “velocity detection in progress”.
  - TIME: From 0 to 255, valid only if SRQ = 1, indicates the time between contacts in multiples of 45 µs. Set to 255 if the time is greater or equal to 256*45 µs.
- LED Data: The P16 should write to these locations the MK information which should appear to the MK[10:0] pins at ROW[2:0] time.
- Switch Data: These fields hold the BR information read from the BR[10:0] pins at ROW[3:0] time.
- ADC Status: These fields represent the analog voltage at VIN pin at ROW[3:0] time, from 0 (VIN = VREFN) to 0FFH (VIN = VREFP).

GPIO

The pins GPIO[3:0] in normal mode are controlled by the ATSAM97xx configuration and control/status registers (refer to prgdvkit.pdf).

The ATSAM9753 additional GPIO control/status register controls GPIO[3:0] alternate mode and GPIO4 normal and alternate mode.

The GPIO register is located at address 0xF in the I/O mapping.

Table 16. GPIO Mapping

7	X	x
6	GPIO4 Output Enable	x
5	GPIO1 Alt	x
4	GPIO0 Alt	x
3	GPIO4 Data	Debug/ pin
2	GPIO4 Alt data (DBOUT)(1)	GPIO4 pin (DBDATA)(1)
1	GPIO3 Alt data (DBACK)(1)	GPIO Reg[1] (DBACK)(1)
0	GPIO4 Output Enable(1)	GPIO4 Input Enable(1)

Note: 1. Only available in Debug Mode.

Table 17. GPIO0

	Normal Input Mode	Normal Output Mode	Alt Output Mode(1)
ATSAM97xx_config_Reg[0] (I/O add0)	0	1	1
ATSAM9753_GPIO_Reg[4] (I/O addF)	x	0	1

Note: 1. In alternate output mode, GPIO0 = ROW3.
Refer to description of pins ROW[2:0] in Table 1 on page 3.

Table 18. GPIO1

	Normal Input Mode	Normal Output Mode	Alt Output Mode(1)
ATSAM97xx_config_Reg[1]	0	1	1
ATSAM9753_GPIO_Reg[5]	x	0	1

Table 19. GPIO2

	Normal Input Mode	Normal Output Mode	Alt Output Mode(1)
ATSAM97xx_config_Reg[2]	0	1	x
$\overline{\text{DEBUG}}$ Pin	1	1	0

Note: 1. In alternate output mode, GPIO2 is configured as input and assumed as DBCLK (ATSAM9753_GPIO[0]).

Table 20. GPIO3

	Normal Input Mode	Normal Output Mode	Alt Output Mode(1)
ATSAM97xx_config_Reg[3]	0	1	x
$\overline{\text{DEBUG}}$ Pin	1	1	0

Note: 1. In alternate output mode, GPIO3 is configured as output and GPIO3 = DBACK (ATSAM9753_GPIO_reg[1]).

Table 21. GPIO4

	Normal Input Mode	Normal Output Mode	Alt Output Mode(1)	Alt Output Mode(1)
ATSAM9753_GPIO_Reg[6]	0	1	x	x
ATSAM9753_GPIO_Reg[0]	x	x	0	1
$\overline{\text{DEBUG}}$ Pin	1	1	0	0

Note: 1. In alternate mode, GPIO4 is used for serial debug data:
In input, ATSAM9753_GPIO[2] (DBIN) = GPIO4
In output, GPIO4 = ATSAM9753_GPIO_Reg[2] (DBOUT).

Mechanical Dimensions

Figure 8. 144-lead TQFP Package Drawing

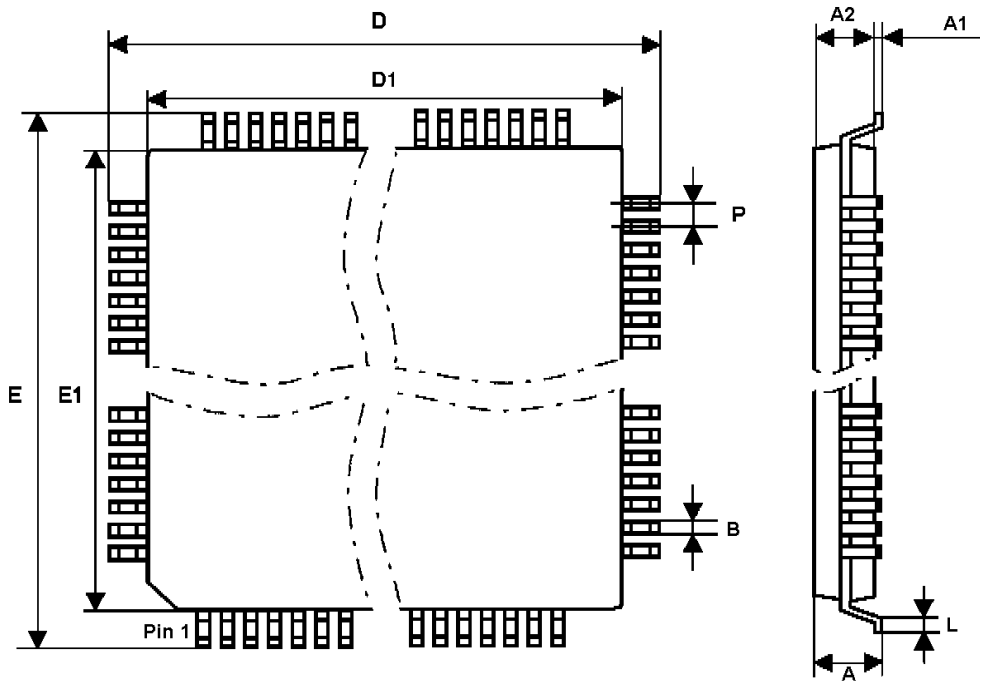


Table 22. 144-lead TQFP Package Dimensions (in millimeters)

	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	21.90	22.00	22.10
D1	19.90	20.00	20.10
E	21.90	22.00	22.10
E1	19.90	20.00	20.10
L	0.45	0.60	0.75
P		0.50	
B	0.17	0.22	0.27

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