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CMOS VLSI Lab 3

Intro & Background:

In this lab we were tasked with creating the schematic and layout for Bit-Slice Adder/Subtractor, Bit-Slice Magnitude Comparator,2-to-1 MUX and 2-to-1 XOR.We have had exposure to all of these gates in previous labs and classes but this is the first time that we are creating a layout for them

Below is a brief description of each of them:

Bit Slice Adder/Subtractor- A bit slice adder is an adder that works on one bit only, that can be combined with other bit slice adders in a chain to form an adder of arbitrary length. To do this, the adder needs information from the previous bit slice in the chain, in this case the carry bit from the previous stage. We also needed a bit to select between subtraction and addition, subtraction being done by performing a two's complement on the second input, inverting and adding one.

Bit-Slice Magnitude Comparator- The magnitude comparator, likewise needed to take two one-bit inputs and information from the previous stage in the chain in order to make a correct decision on whether or not the current bit made one number smaller, larger, or equal to the other. This required the bit slice stage to take in the three outputs from the previous lab as well as the two inputs to compare, and to deliver three outputs to the next stage, namely equality, less than, and greater than.

2-to-1 MUX- The MUX is also referred to as the data selector. For a multiplexer of 2^N inputs there are n select lines.It is the converse of a demux or demultiplexer.

2-to-1 XOR- Also known as a exclusive OR. An Exclusive OR gate has an output of of 1 when one of the two inputs is 1 and a 0 otherwise. These unique characteristics make it very useful in implementing binary addition since 1 plus 1 in binary is 0 with a carry out, 0 plus 1 is 1 and 0 plus 0 is 0.

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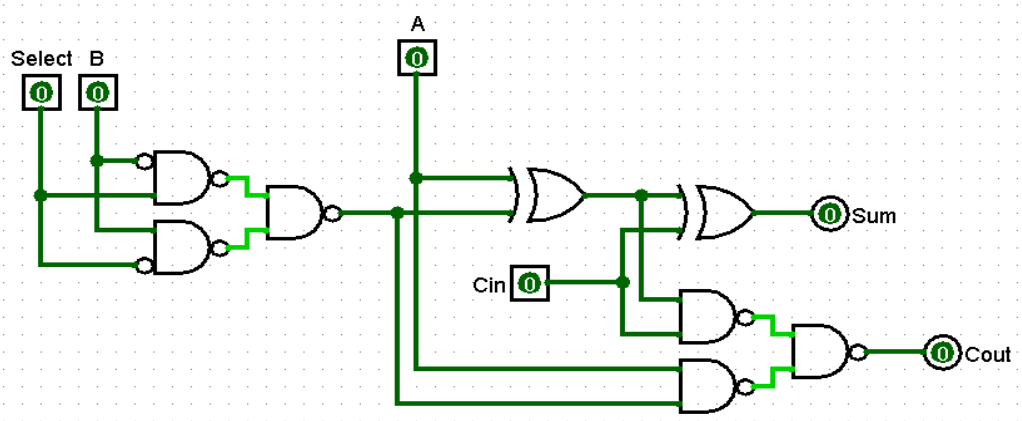
Design Process & Flow:

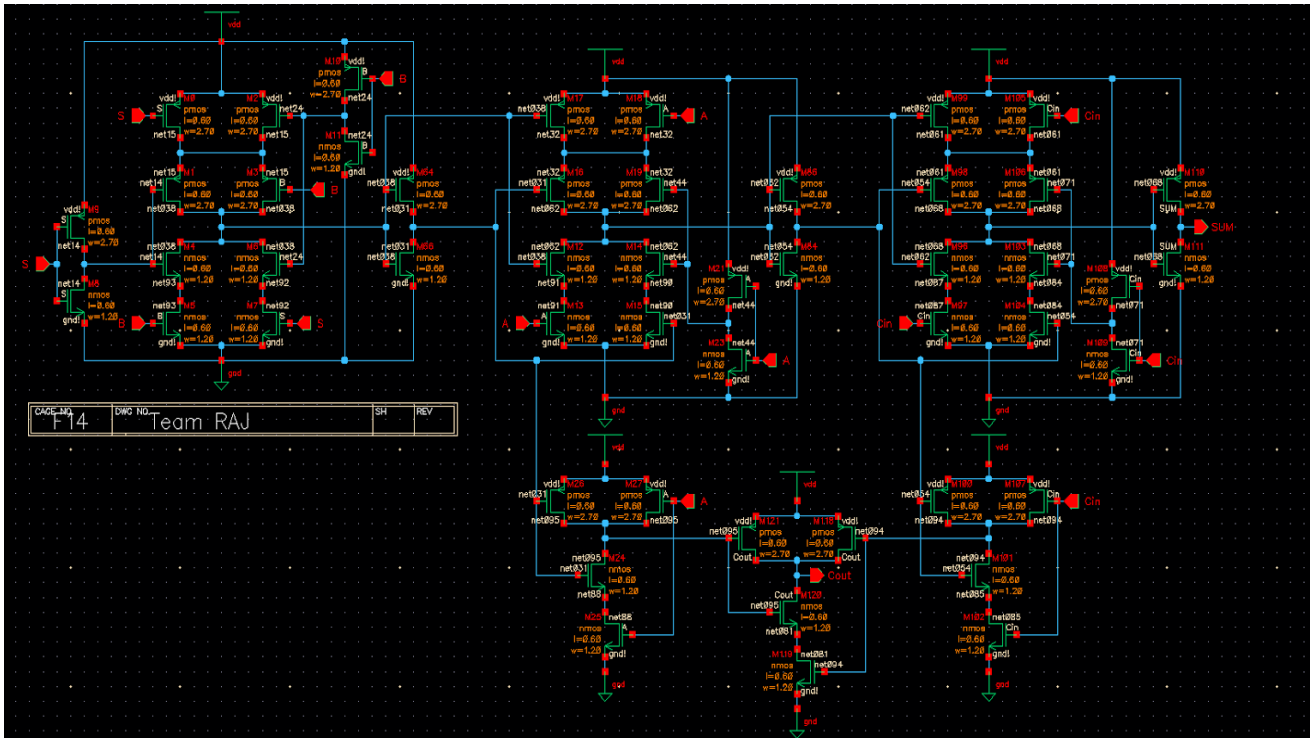
For the Adder/Subtractor and the Bit Slice Magnitude Comparator we created the gate level logic in Logisim to make sure the logic was correct. However we did not do that for the XOR and MUX since those equations are commonly known. For the MUX we used the equation Z= (AS')+(BS). For the XOR we used the equations AB'+ A'B or (A+B)(A'+B') both of which are logically equivalent.

Adder/ Subtractor

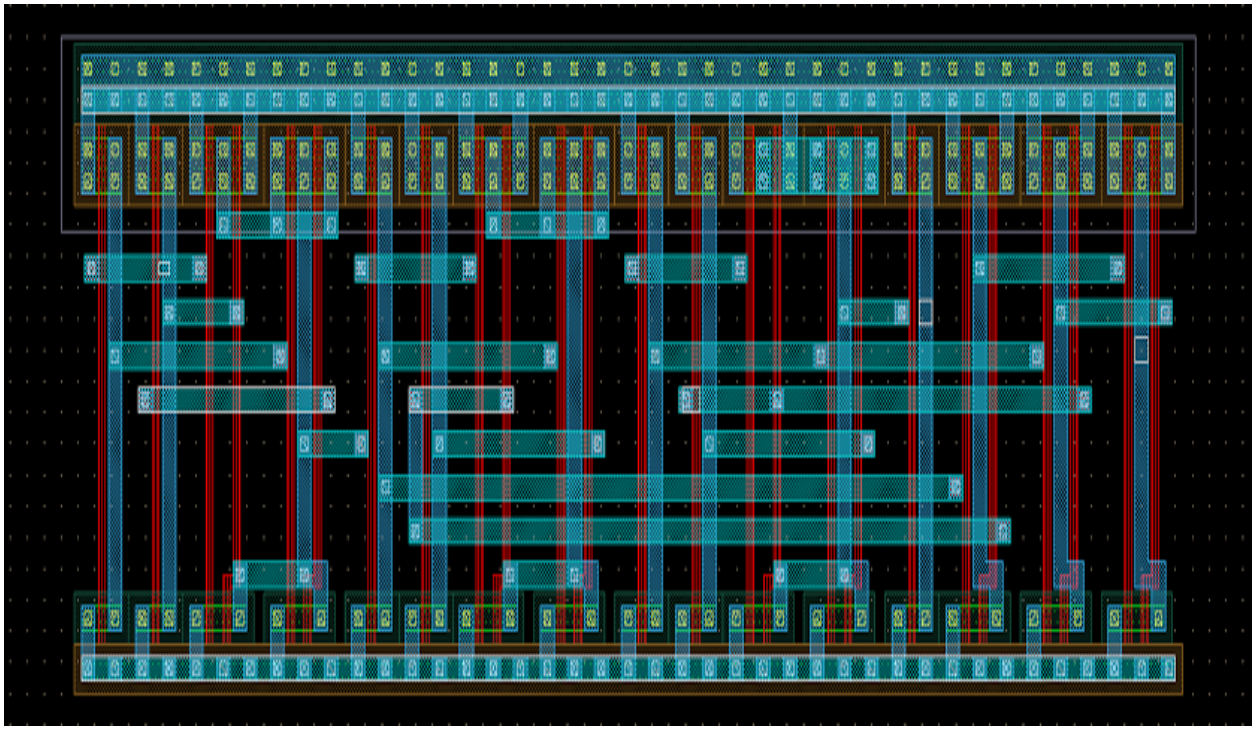
Logisim (Gate level) Adder/Subtractor



Schematic Bit-Slice Adder/Subtractor

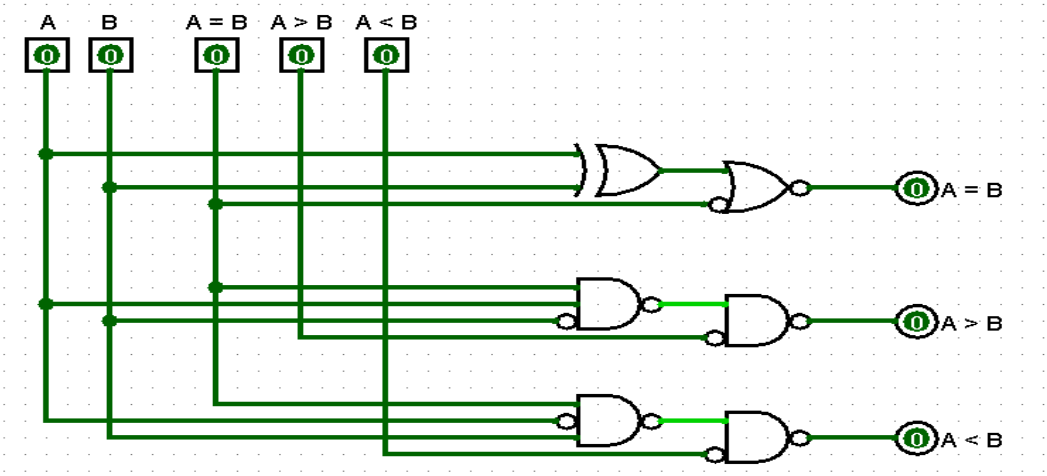


Layout Bit-Slice Adder/Subtractor

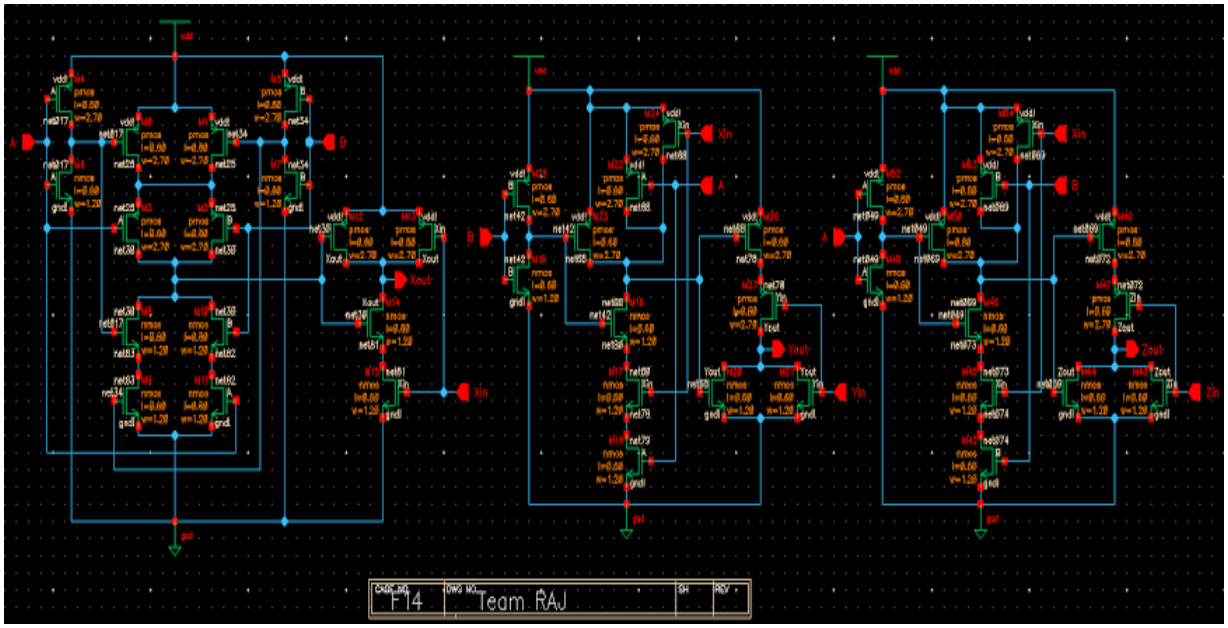


Bit Slice Magnitude Comparator

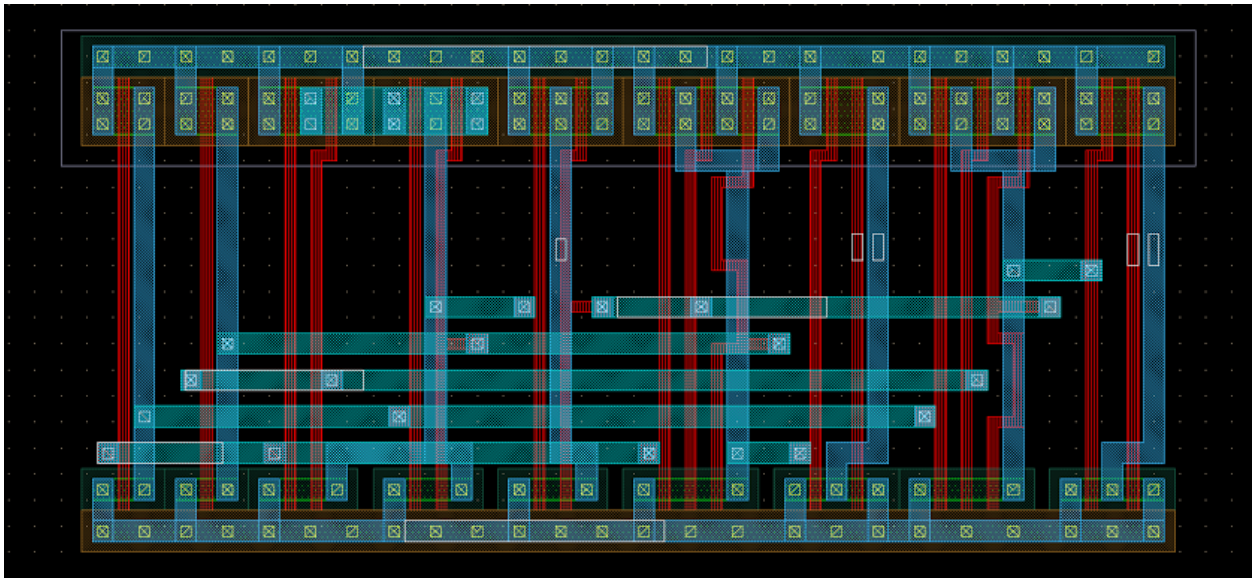
Logisim (Gate level) Bit- Slice Magnitude Comparator



Schematic Bit-Slice Magnitude Comparator

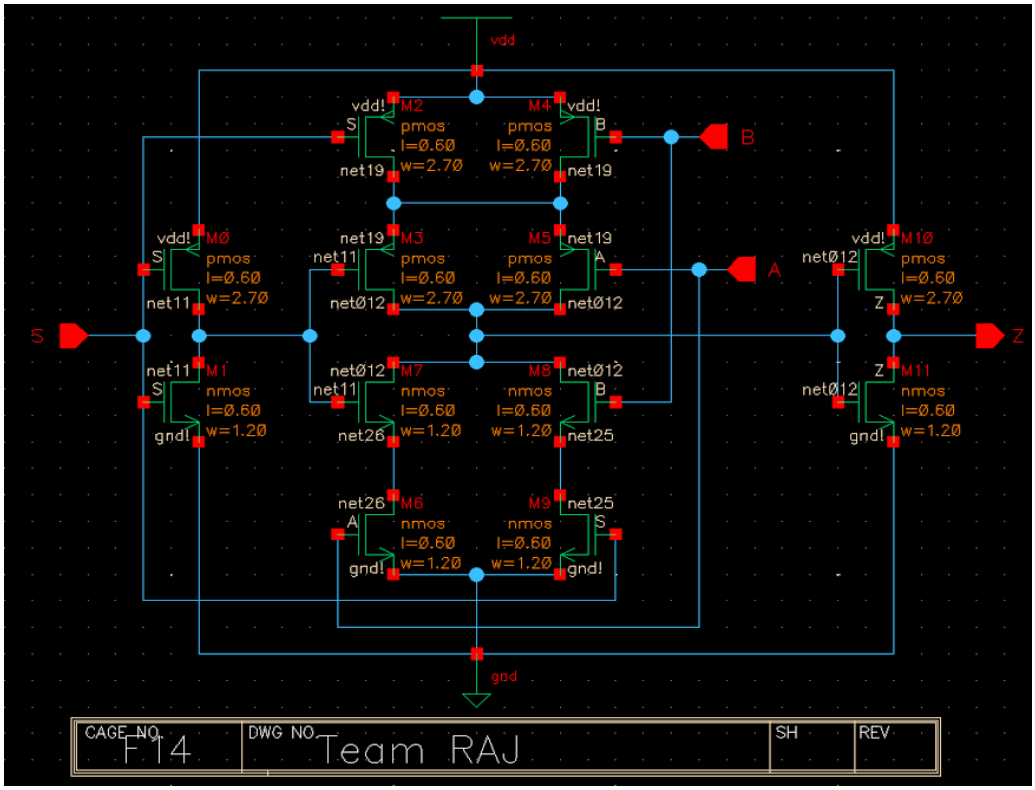


Layout Bit-Slice Magnitude Comparator

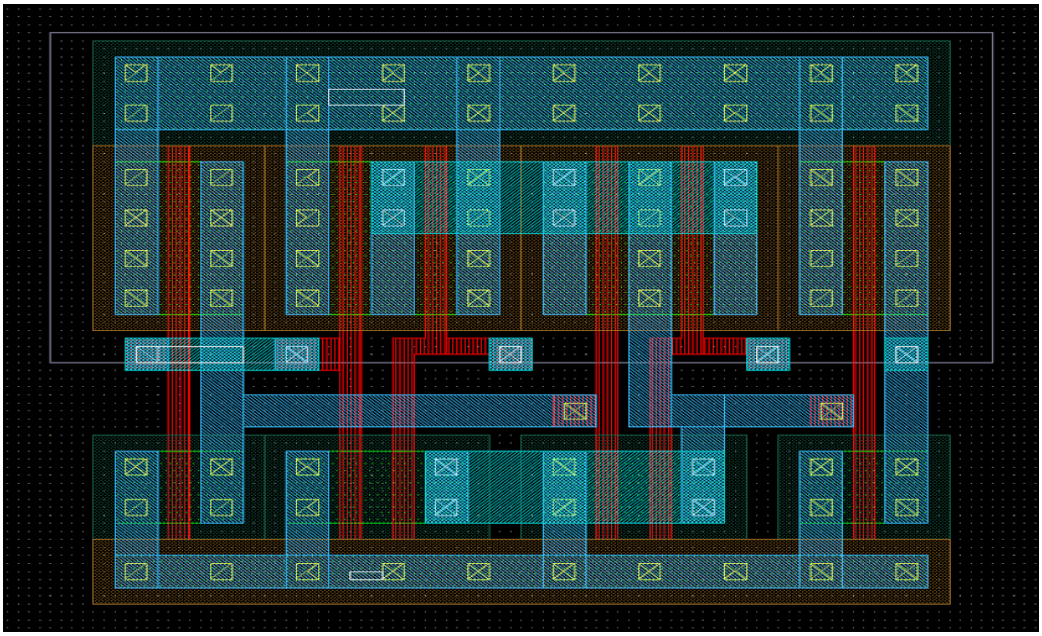


2-to-1 MUX

Schematic 2-to-1 MUX

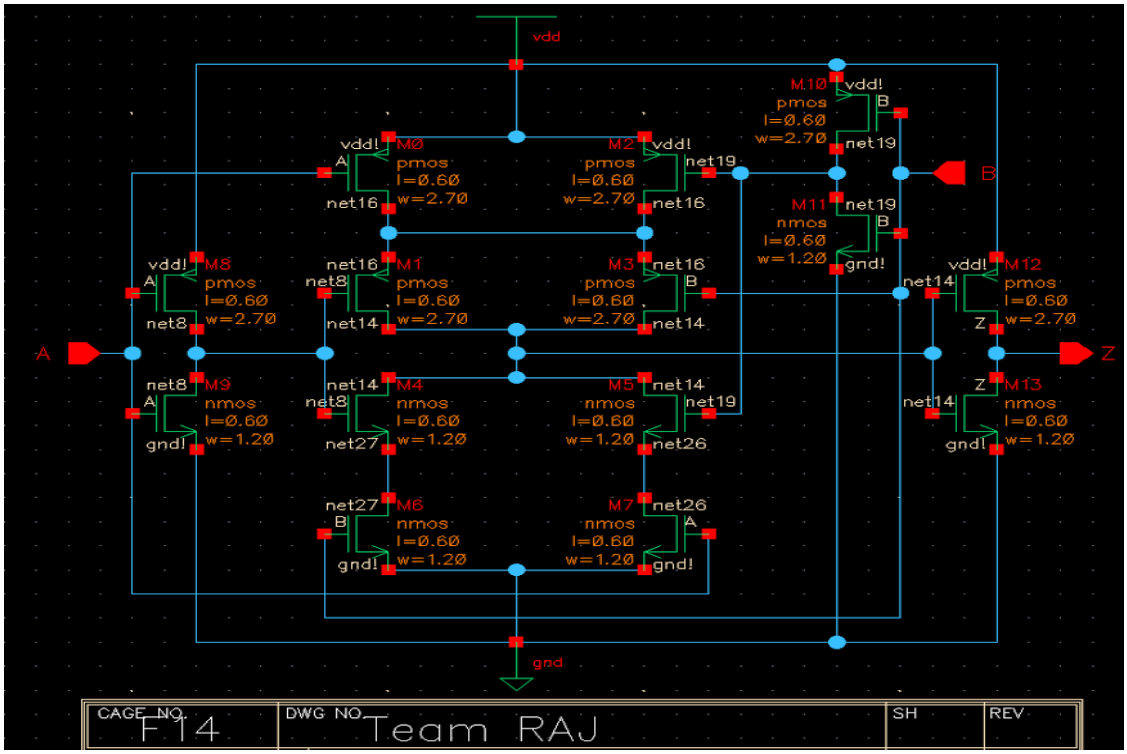


Layout 2-to-1 MUX

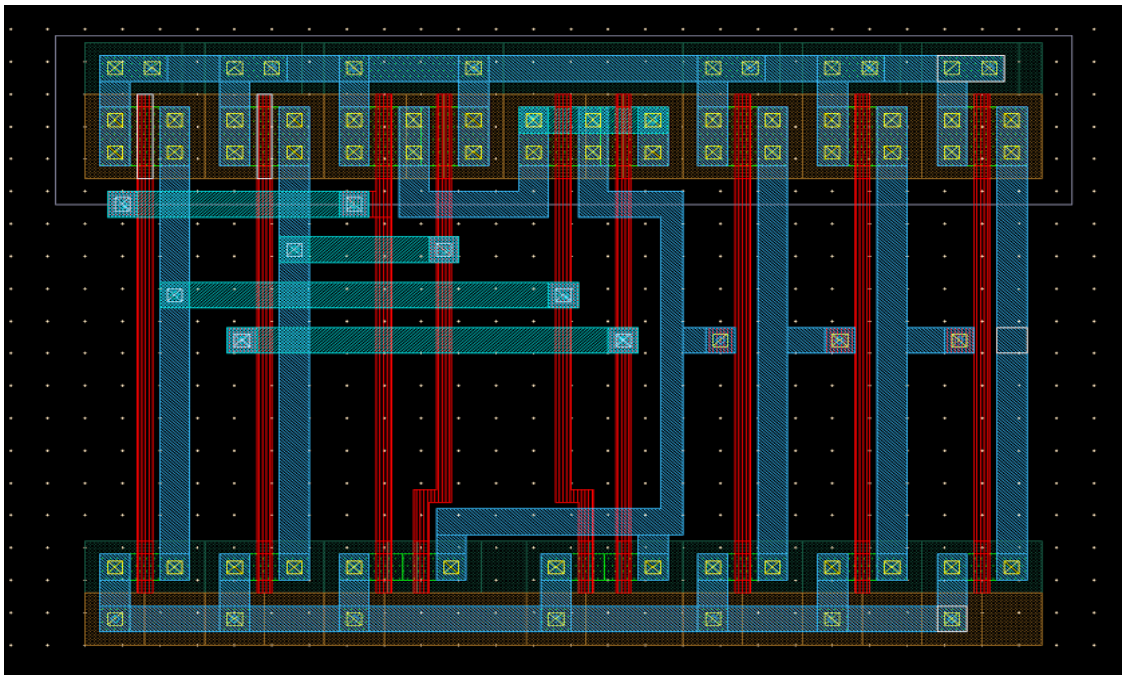


XOR

Schematic 2-Input XOR



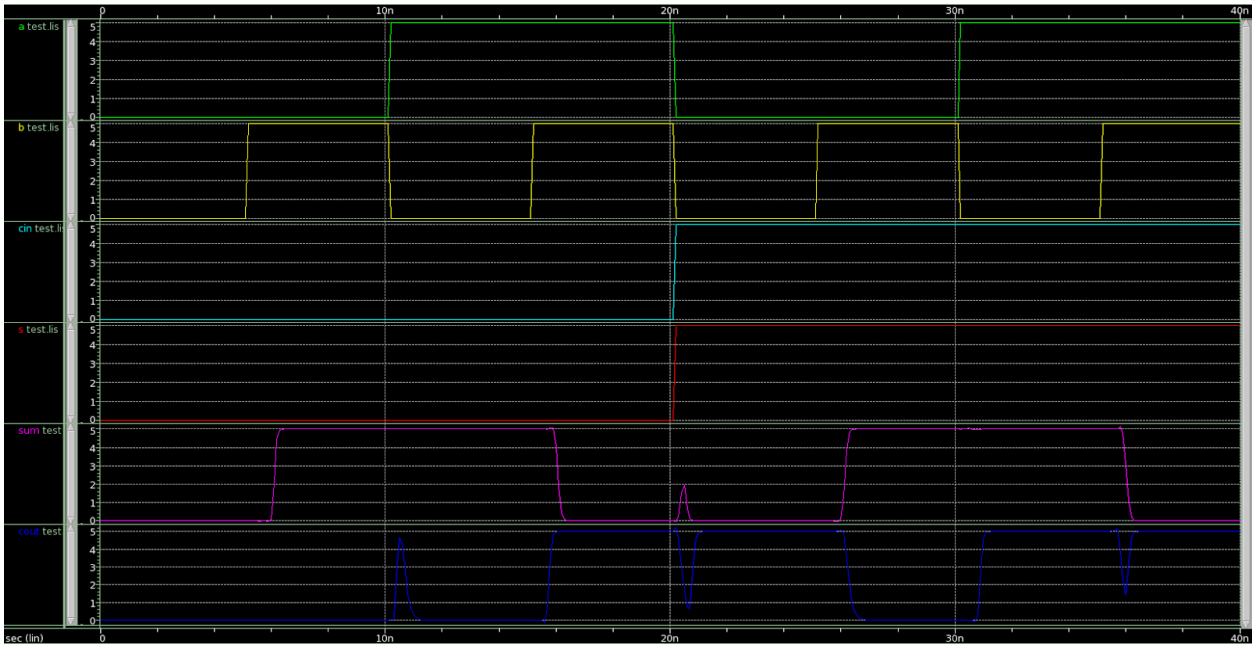
Layout 2-to-1 XOR



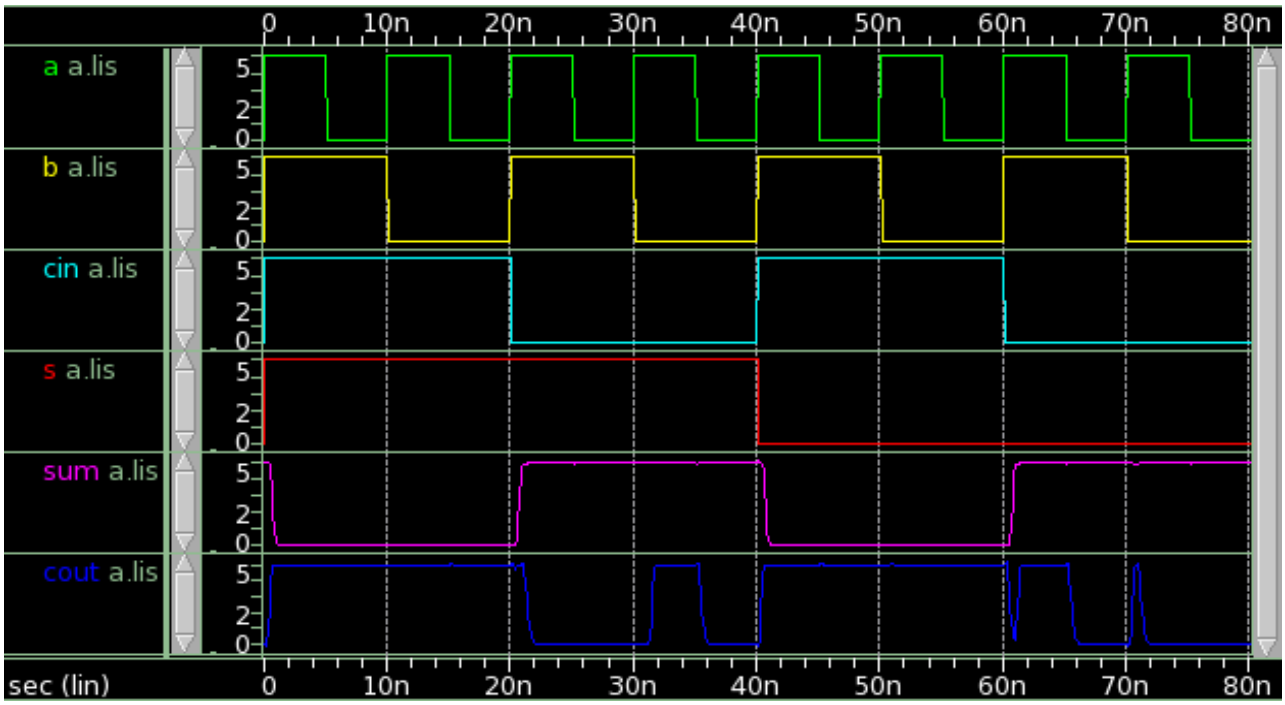
Testing Process & Results:

Adder/ Subtractor

Schematic Bit-Slice Adder/Subtractor Waveform



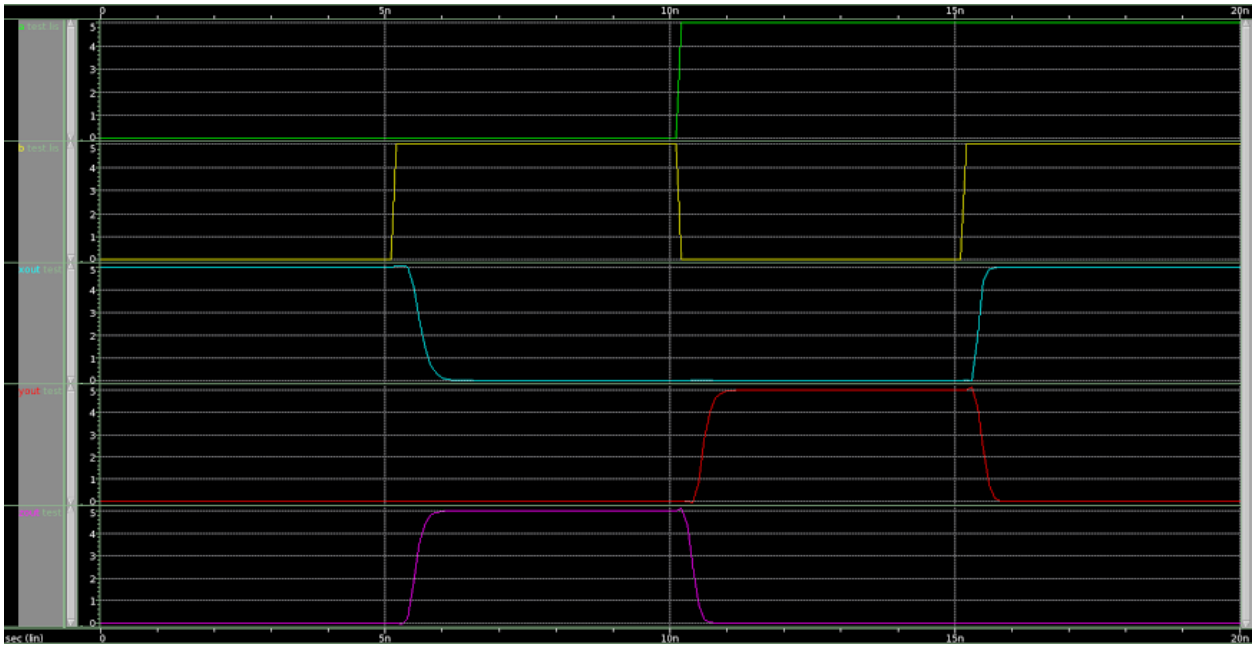
Layout Bit-Slice Adder/Subtractor Waveform



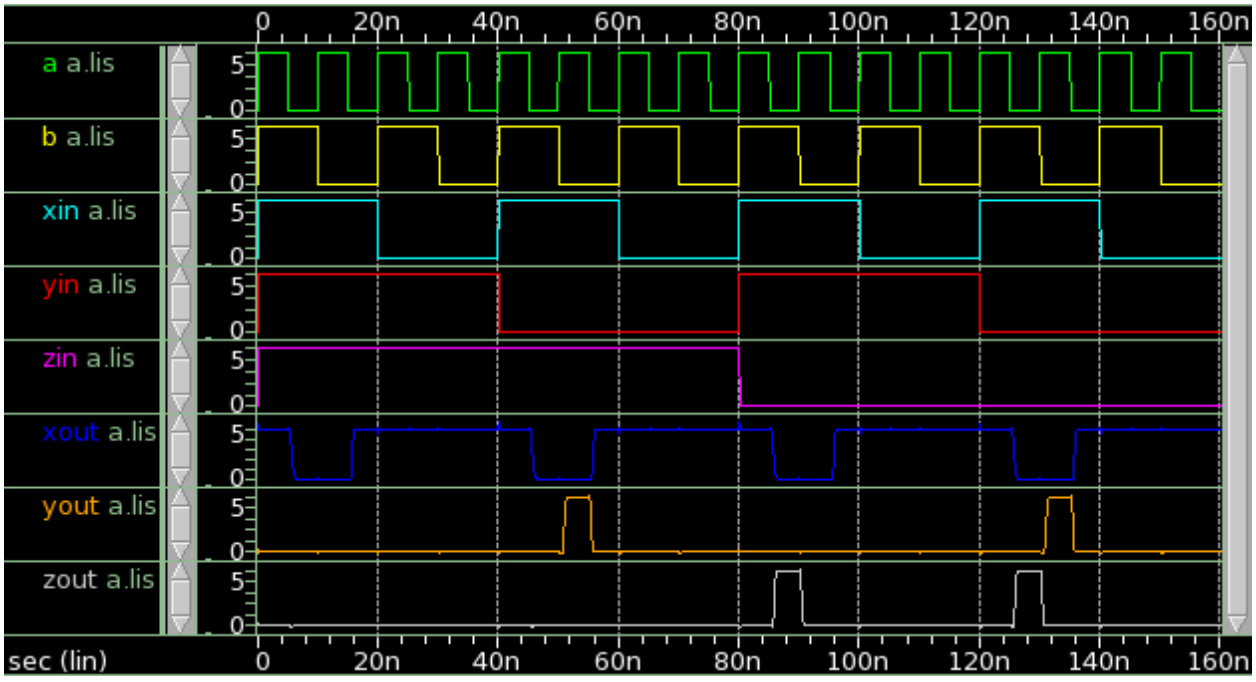
We tested all input combinations and observed that the output is accurate, minus a few glitches.

Magnitude Comparator

Schematic Bit-Slice Magnitude Comparator Waveform



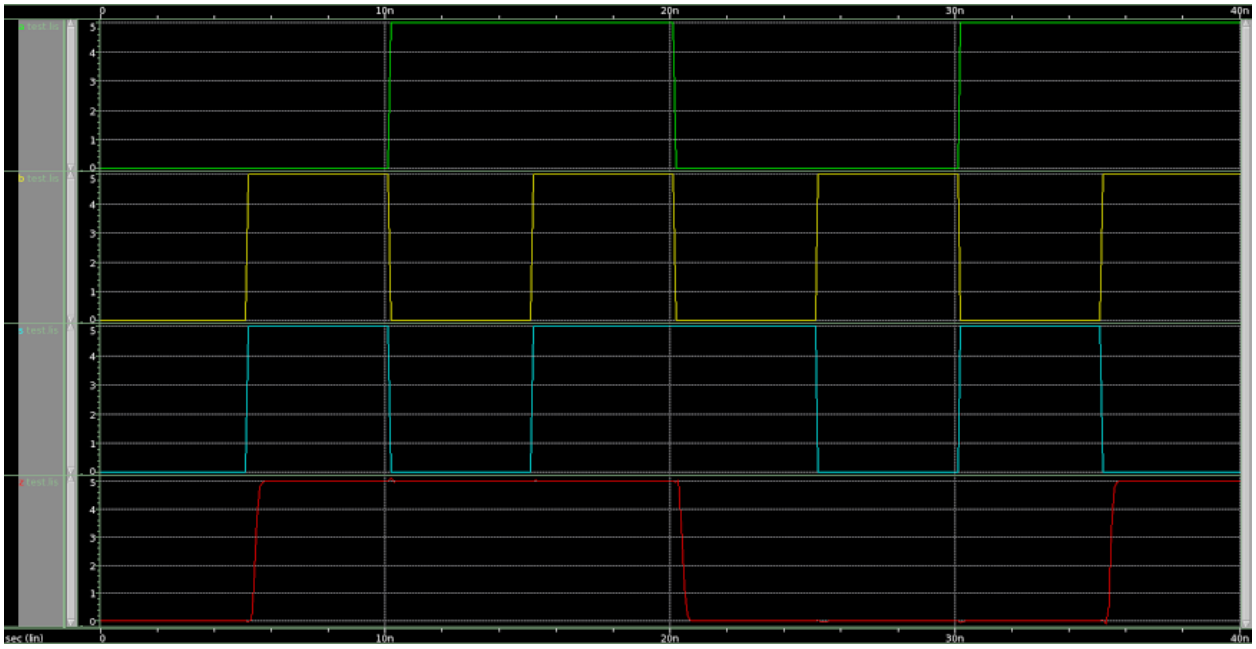
Layout Bit-Slice Magnitude Comparator Waveform



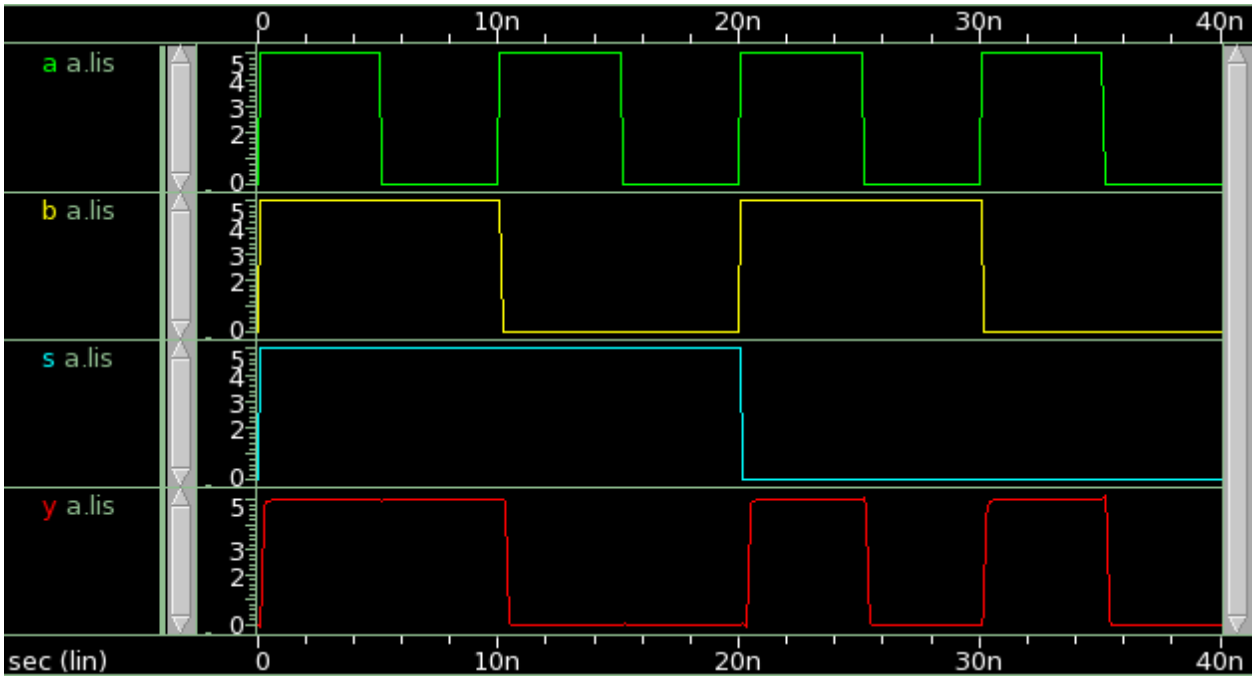
Again, we can see that the output is accurate, though the layout waveform, as a result of looping through all possible combinations, tests some invalid inputs from the previous bit slice. The valid input combinations are accurate and output only one description of the condition.

2-to-1 MUX

Schematic 2-to-1 MUX Waveform



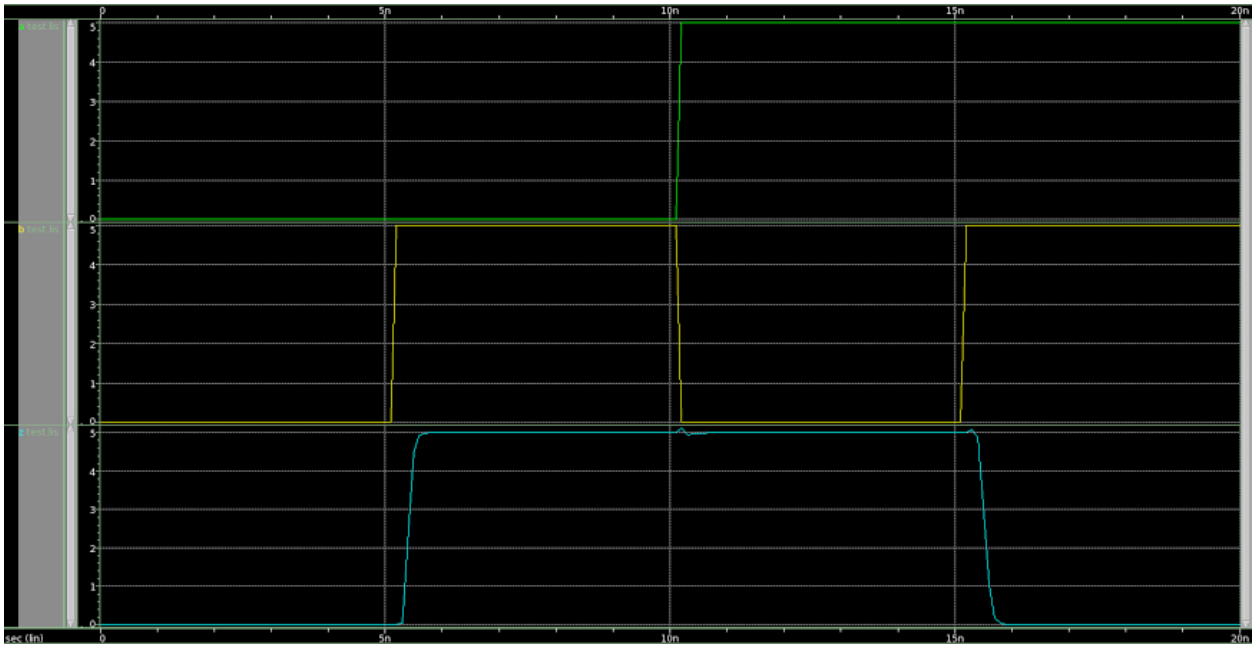
Layout 2-to-1 MUX Waveform



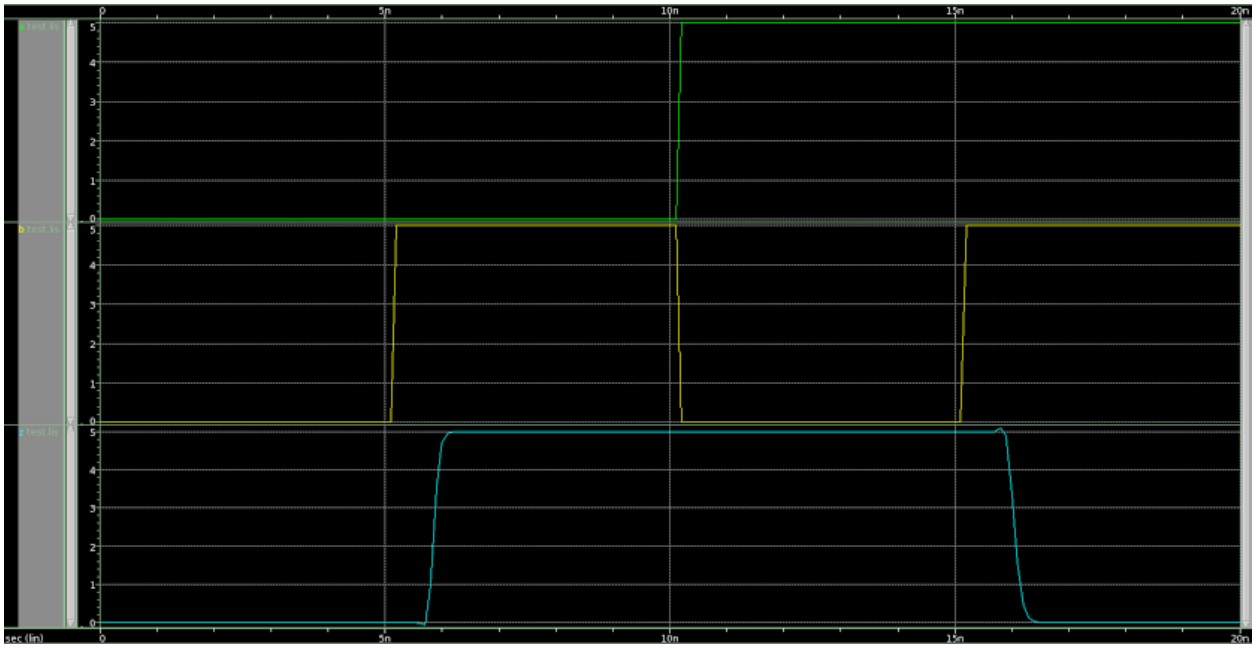
We looped through all eight combinations and observed that the output was correct and smooth, accurately reproducing the truth table we established in previous labs.

XOR

Schematic 2-Input XOR



Layout 2-to-1 XOR



Likewise, we looped through four input combinations for the XOR and established that the correct output was being passed with an expected delay from buffering to smooth glitches.

Conclusion & Feedback:

We were able to get the schematic done fairly quickly in order to establish the logical elements of the circuit early on. This would give us plenty of time to investigate schemes for minimizing our physical layout, and to refine our logic. The layout did give us some trouble, as layouts that were minimalistic and on occasion strayed into metal 3 tended to give invalid outputs. We were fairly close to the bounding areas provided to us and in the case of the MUX we were actually able to make it smaller than the given specifications while making the transistors larger to reduce delays. with practise I believe we will be able to meet the specified bounding areas a lot easier since this was the first lab where we truly had to create a layout of different gates,

Bounding Area for Our Circuits

Name	Width	Length
Adder/Subtractor	**31.5**	**100.8**
Magnitude Comparator	**30**	**65.4**
2-to-1 MUX	**21.3**	**28.4**
XOR	**28.2**	**40.2**

Bounding Area for Your Circuits

Name	Width	Length
Adder/Subtractor	**30**	**96**
Magnitude Comparator	**30**	**25.2**
2-to-1 MUX	**30**	**28.8**
XOR	**30**	**31.2**