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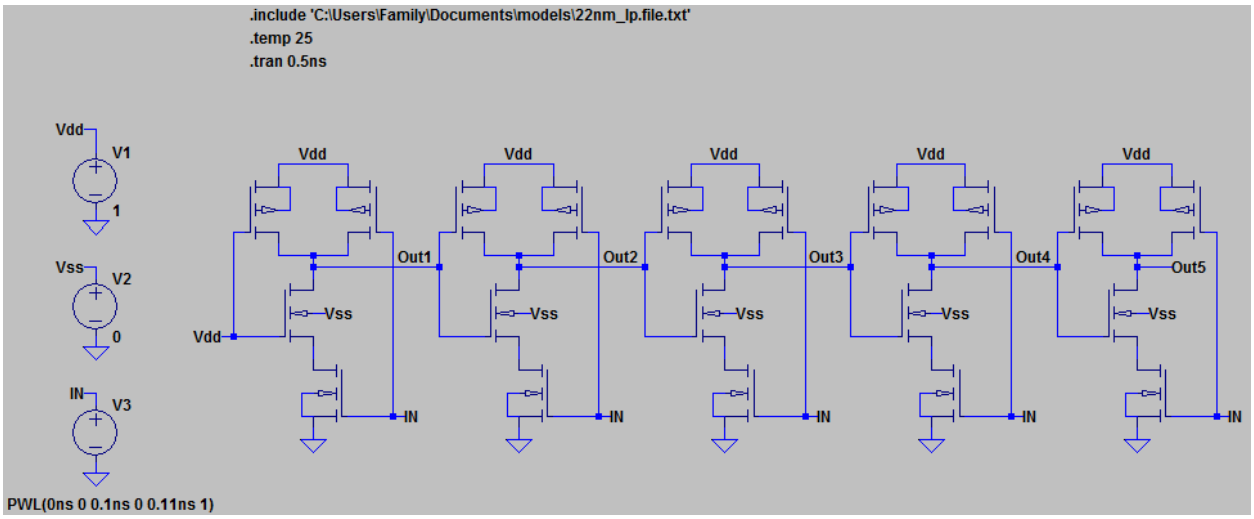
Low Power VLSI
CIS 4930, Fall 2015

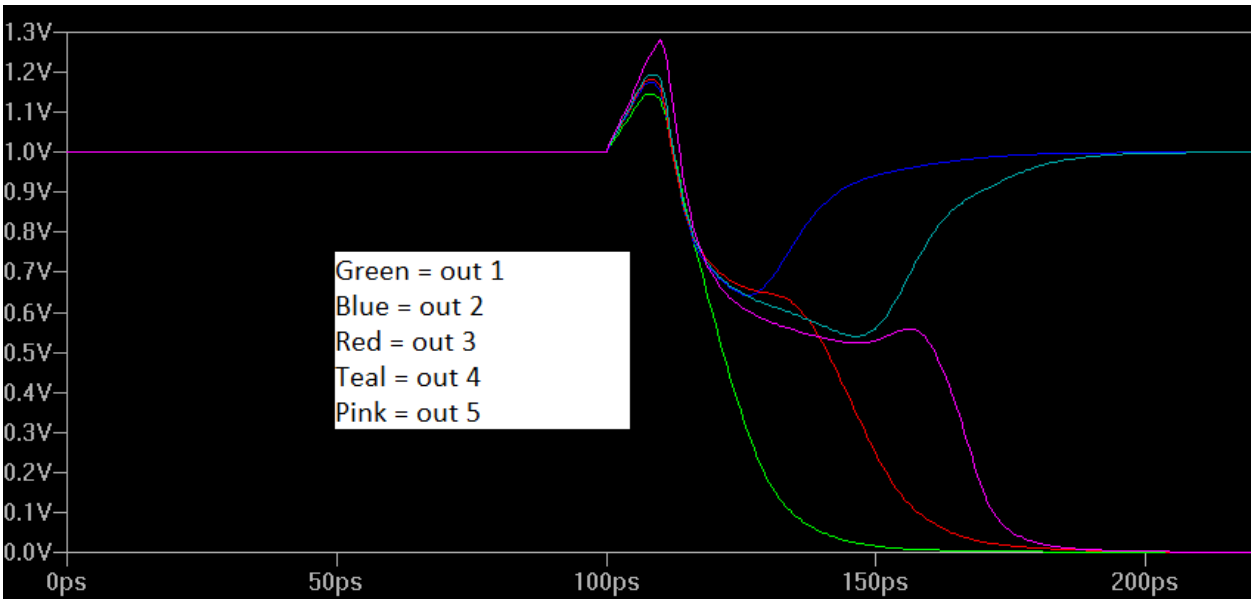
Homework #3

Q1.

Schematic for Part A & B



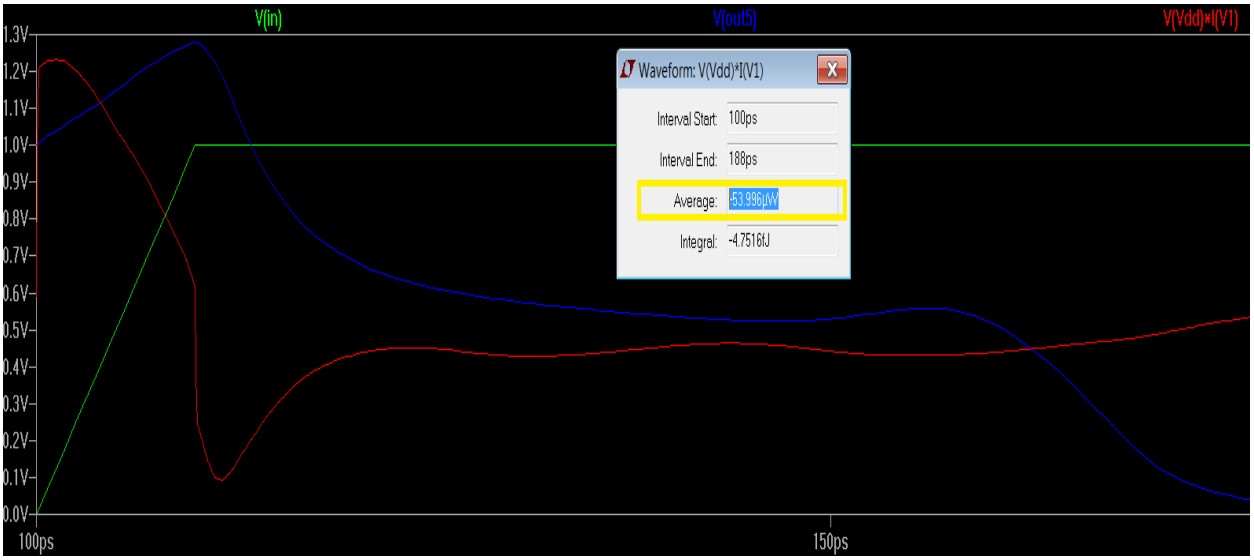
Waveform A



From the waveform it can be seen that the chain (re-convergence) of NAND gates leads to “glitches” in the intermediate/final outputs (out1, out2, etc...). This characteristic of the circuit is due to the delay of

a single input signal (time-dependent inputs) in each stage. Therefore the delay of an input signal to one stage can be summarized as the “sum of propagation delay of all NAND gates previous”.

Waveform B



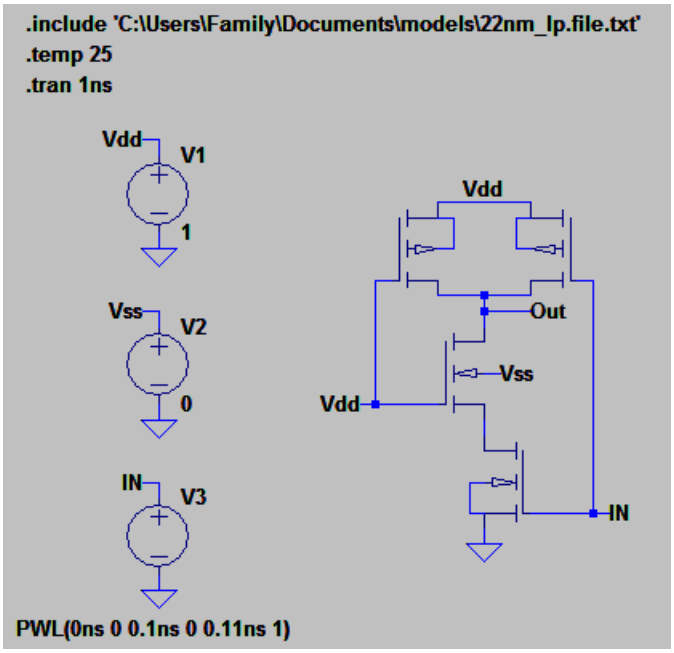
The average power for the interval from 100ps to 188ps is *53.996* microwatts for the NAND gate chain.

Schematic Part C

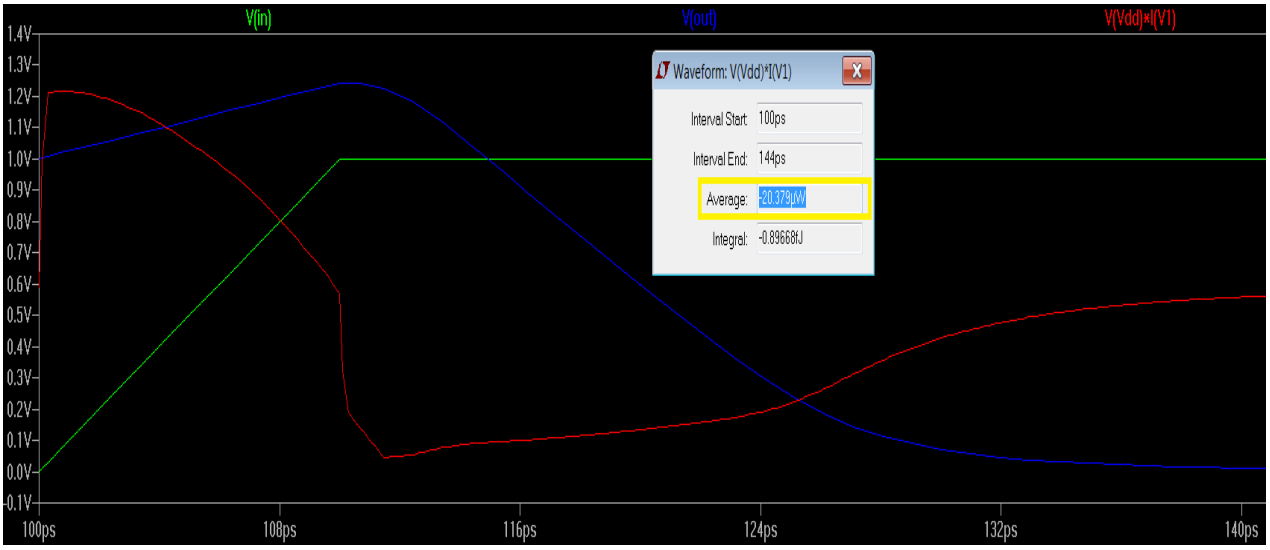
One technique to reduce the power of the NAND gate chain is to re-design the circuit so that no input is “time-dependent”, such that no input will arrive earlier than any other for a given stage.
In re-designing the circuit I first made a truth table to express the function of the NAND gate chain schematic.

Input	Output 5
0	1
1	0

As noted, the current NAND gate chain is fundamentally an inverter, therefore the schematic can be simplified to a single NAND gate (one input is HIGH and the other is given by the input transition).



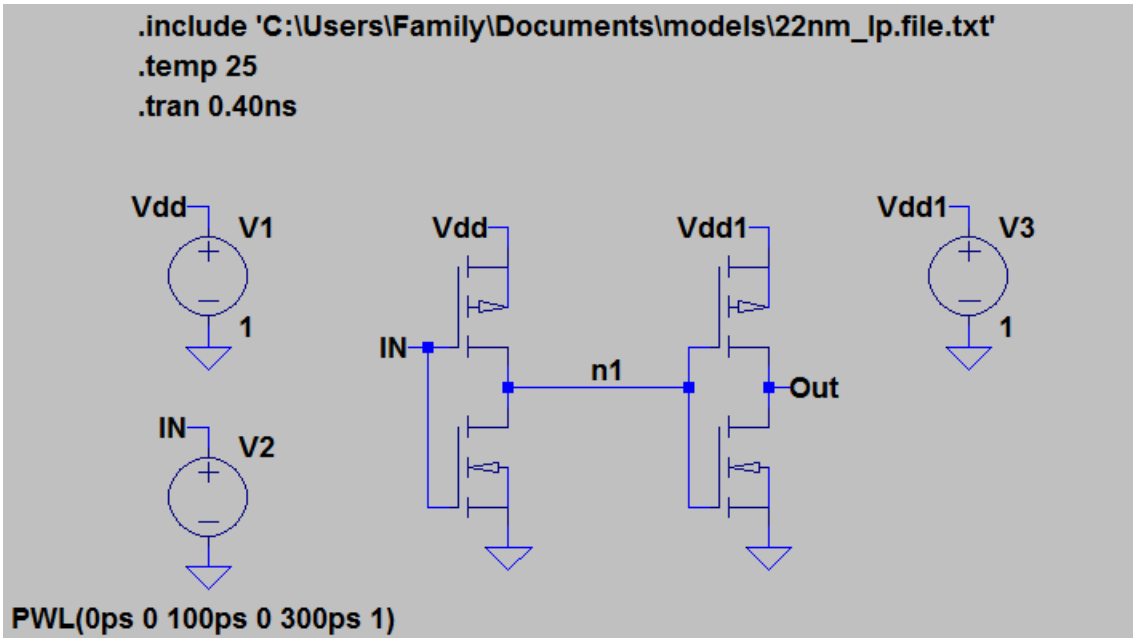
Waveform C



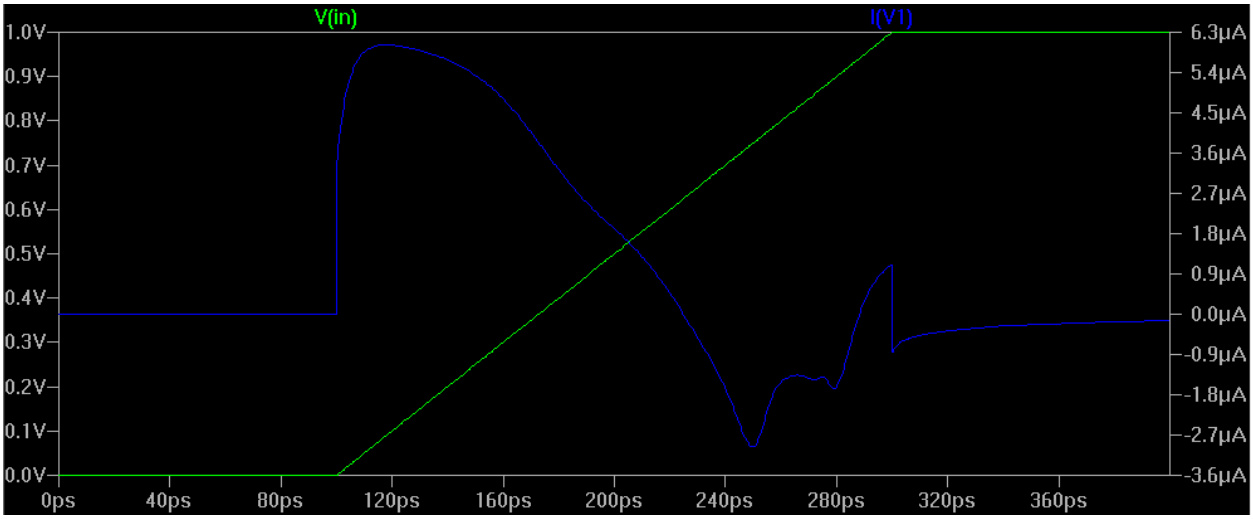
By re-designing the combinational logic of the circuit while keeping the same functionality I was able to reduce the average power consumption to *20.379* microwatts as shown in the time span from 100ps (begin transition) to 144ps (output settles) .

Q2.

Schematic Part A

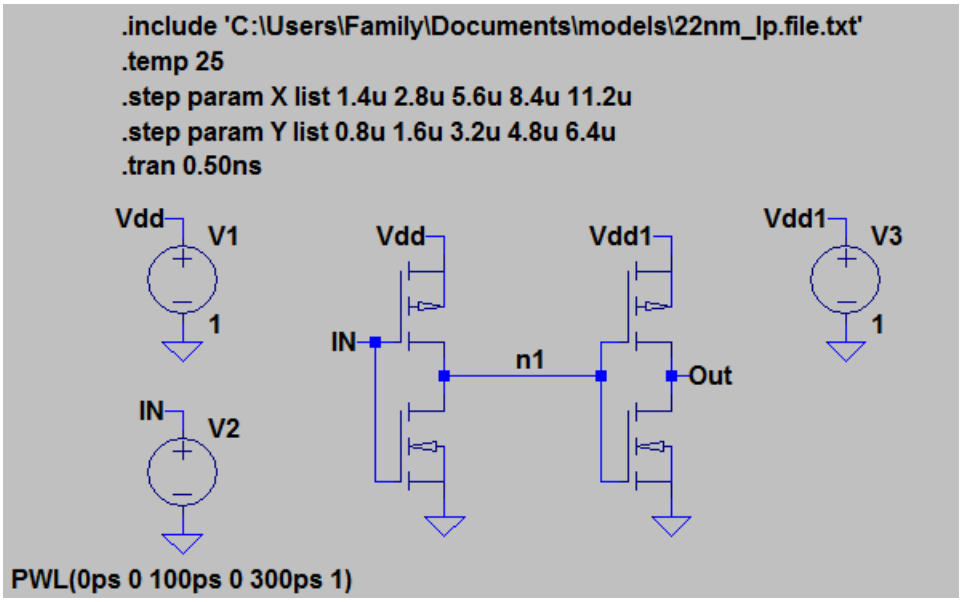


Waveform A

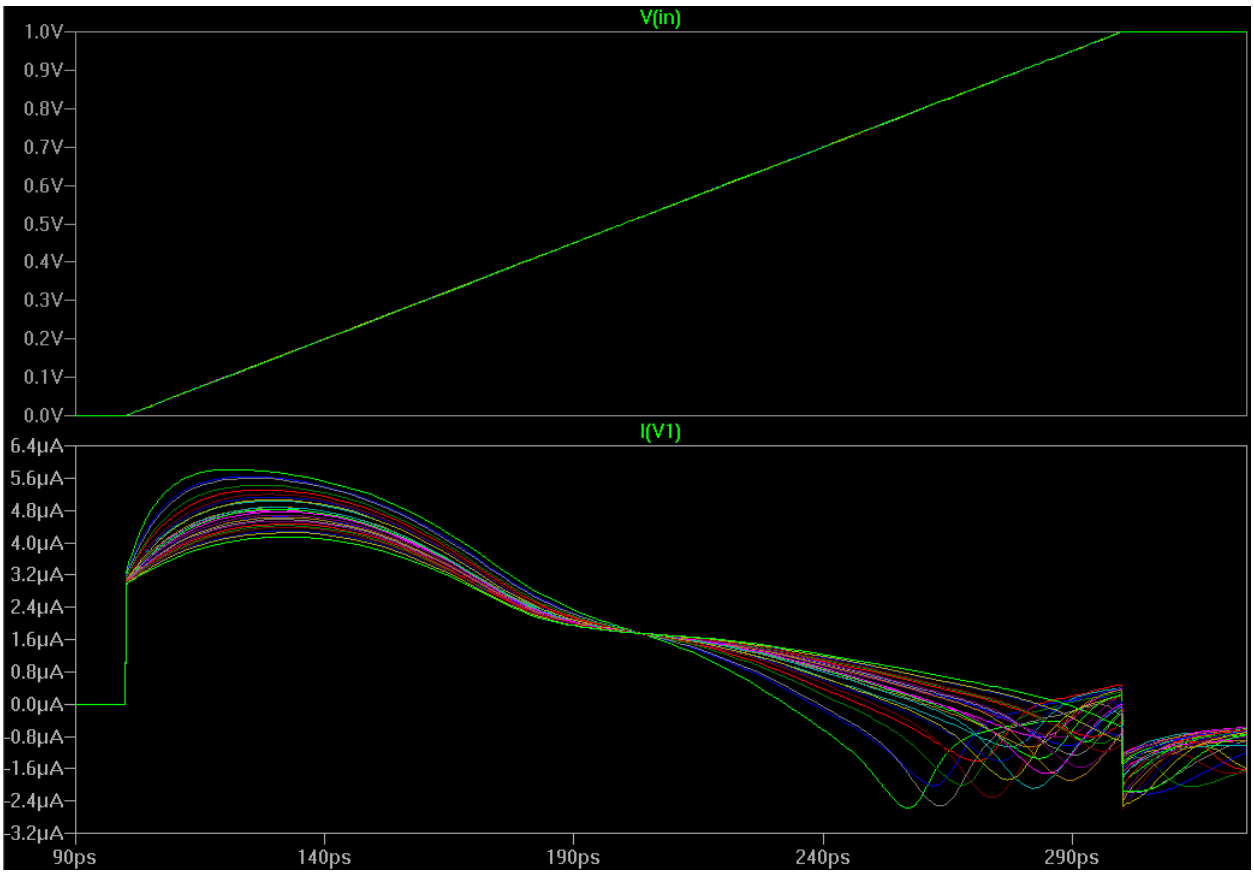


This waveform shows the occurrence of “short-circuit” in an inverter. Notice when the input is transitioning from 0 to 1 the current rises as both transistors are partially “on”. To get a 160ps rise time between 10% and 90% a total of 200ps rise time for the input was implemented using a PWL of the input voltage source.

Schematic B



Waveform B



This waveform shows that increasing the channel-width of the second inverter (increasing the *load* on the first inverter) will decrease the effects of “short circuit”. From Ohm’s Law, V=IR, it can be noted that as the capacitive load is increased the resistance from Vdd to n1 is also increased therefore reducing the amount of current (I = V/R) that can be sourced from Vdd for a given time period (essentially reducing the voltage potential between Vdd and n1).