CIS4930.002

VLSI Design Automation

Summer C – 2015

Midterm Exam

Notes:

(1) Attached HW solutions receive the grade previously assigned, i.e., half-credit on the HW is half-credit on the exam.

(2) To receive full-credit, for a HW problem which received half-credit, the problem must be attached and completed/corrected in the problem space on the exam.

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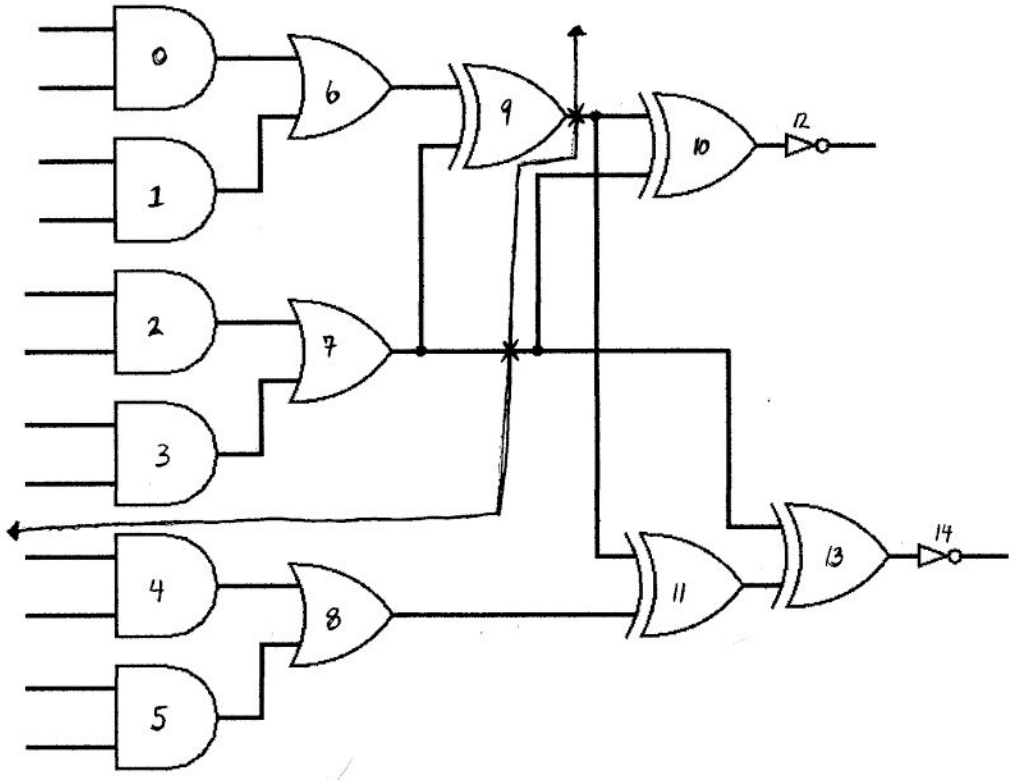
Q# (Max)	Score
1 (10)	10
2 (10)	10
3 (20)	20
4 (10)	9
5 (10)	9
6 (10)	10
7 (10)	6
8 (10)	0
9 (10)	0
Total (100)	68 + 14 = 82

(4) 10pts: Given the following circuit, perform Two-Way Partitioning.



(A) 2pts: Draw a possible cut on the circuit above and number gates (starting with 0).

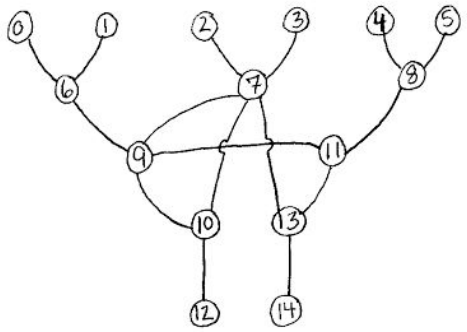
(B) 2pts: List the resulting partition sets and their sizes.

A = { 0, 1, 2, 3, 6, 7, 9 } Size = 7 components

B = { 4, 5, 8, 10, 11, 12, 13, 14 } Size = 8 components

(4) 10pts: Continued...

(C) 2pts: Draw the corresponding connectivity graph of the circuit.



(D) 2pts: Complete the connectivity matrix below.

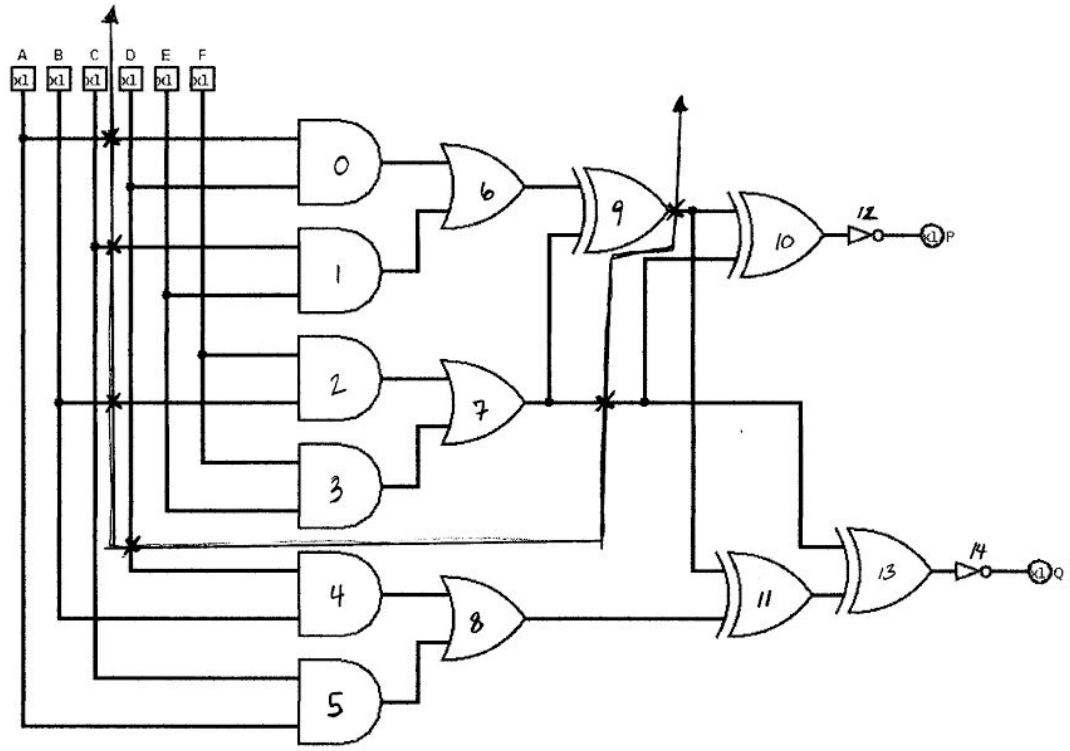
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
0							1								
1							1								
2								1							
3								1							
4									1						
5									1						
6	1	1								1					
7			1	1						1	1			1	
8					1	1						1			
9							1	1			1	1			
10								1		1			1		
11									1	1				1	
12											1				
13								1				1			1
14														1	

(4) 10pts: Continued...

(E) 2pts: Compute the External and Internal Costs of each partition completing the table below.

$I_A =$	6
$I_B =$	10
$E_A = E_B =$	2

(5) 10pts: Given the following circuit, perform Two-Way Partitioning.



(A) 2pts: Draw a possible cut on the circuit above and number gates (starting with 0).

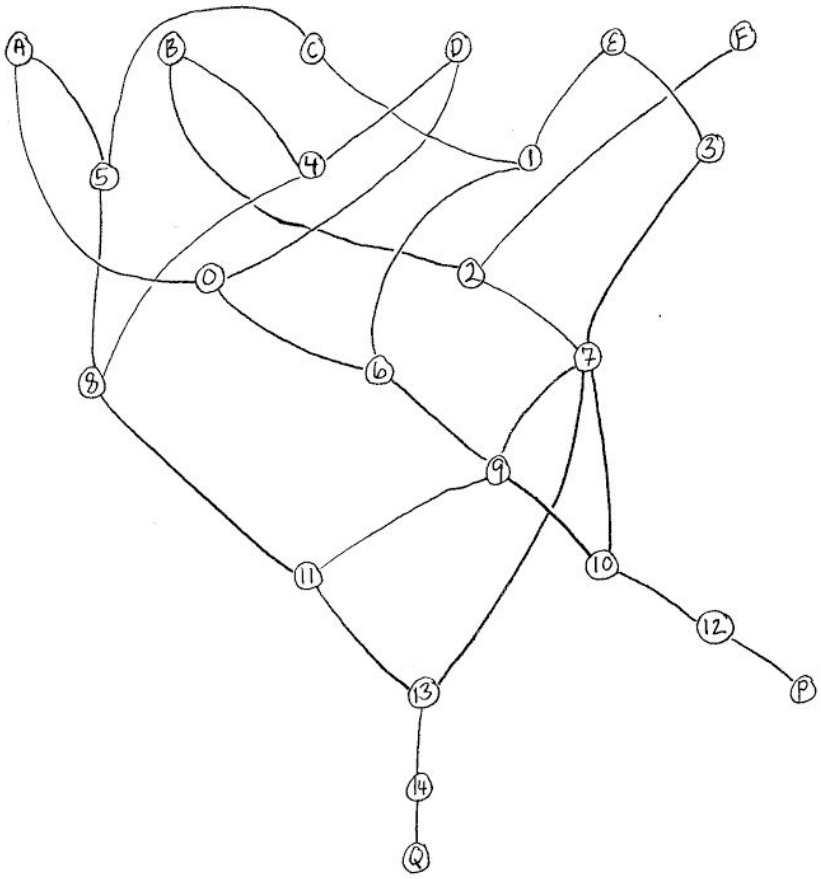
(B) 2pts: List the resulting partition sets and their sizes.

A = { A, B, C, 4, 5, 8, 10, 11, 12, 13, 14, P, Q } Size = 13 components

B = { D, E, F, 0, 1, 2, 3, 6, 7, 9 } Size = 10 components

(5) 10pts: Continued...

(C) 2pts: Draw the corresponding connectivity graph of the circuit.



(5) 10pts: Continued...

(D) 2pts: Complete the connectivity matrix below.

	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	P	Q
A							1					1											
B									1		1												
C								1				1											
D							1				1												
E								1		1													
F									1	1													
0	1			1									1										
1			1		1								1										
2		1				1								1									
3					1	1								1									
4		1		1											1								
5	1		1												1								
6							1	1								1							
7									1	1						1	1			1			
8											1	1						1					
9													1	1			1	1					
10														1		1			1				
11															1	1				1			
12																	1					1	
13														1				1			1		
14																							1
P																			1				
Q																					1		

(E) 2pts: Compute the External and Internal Costs of each partition completing the table below.

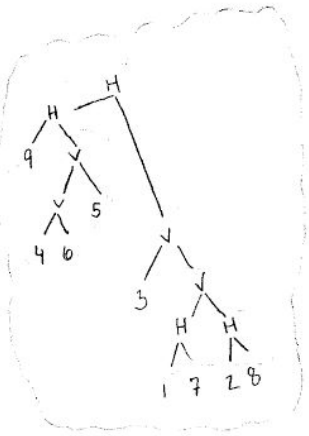
$I_A =$	14
$I_B =$	16
$E_A = E_B =$	6

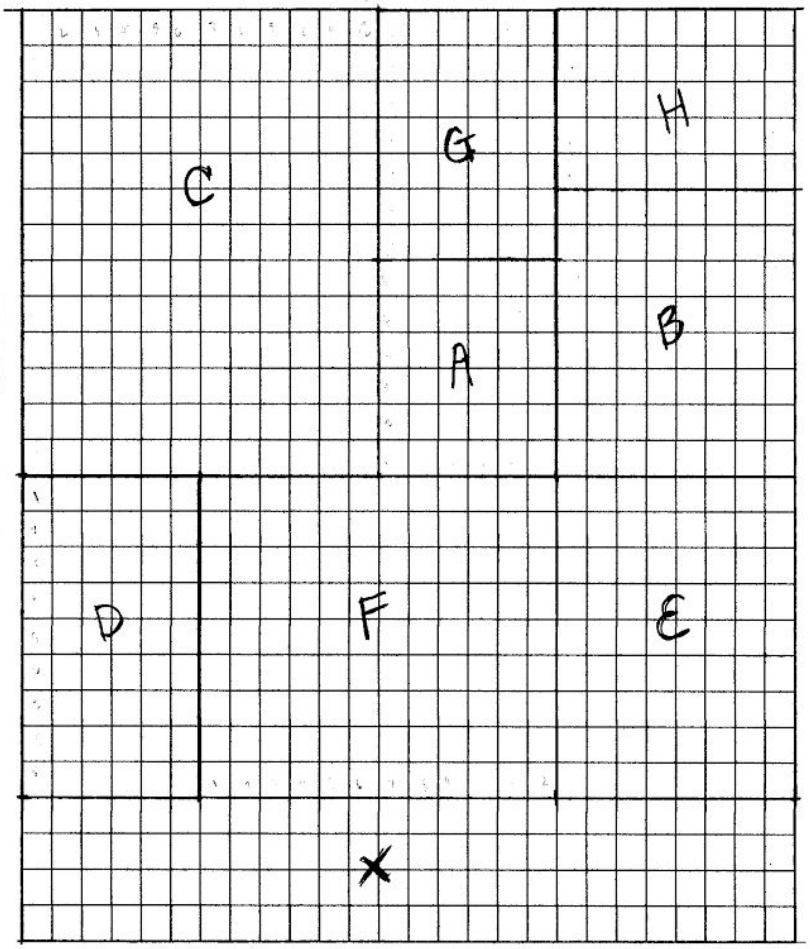
(7) 10pts: Given the following modules, perform floorplanning given the *constraint shape* below, provide the solution in Polish format.

Module	Width	Height
A	6	6
B	8	8
C	13	12
D	9	6
E	9	8
F	9	12
G	7	6
H	5	8
X	4	26

* let { A=1, B=2, C=3, D=4, E=5, F=6, G=7, H=8, X=9 }

(A) 5pts: Show a possible Floorplan given the constraint shape of 26x26.





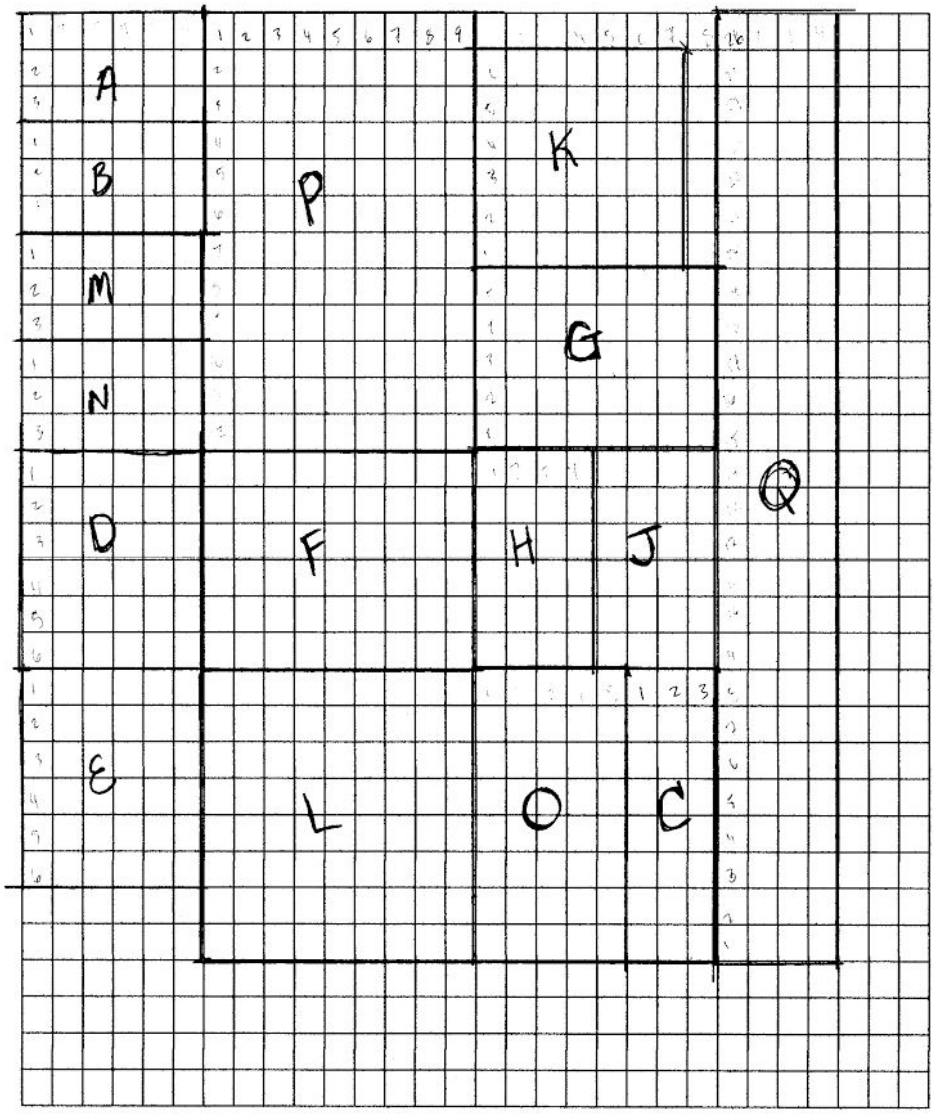
(B) 5pts: Polish representation of Floorplan solution:

46V5V9H 17H 28HV3VH

(8) 10pts: Given the following modules, perform floorplanning given the working space below (which is not a constraint shape), provide the solution in Polish format.

Module	Width	Height
A	6	3
B	6	3
C	3	8
D	6	6
E	6	6
F	9	6
G	5	8
H	4	6
J	4	6
K	7	6
L	9	8
M	3	6
N	3	6
O	5	8
P	9	12
Q	4	26

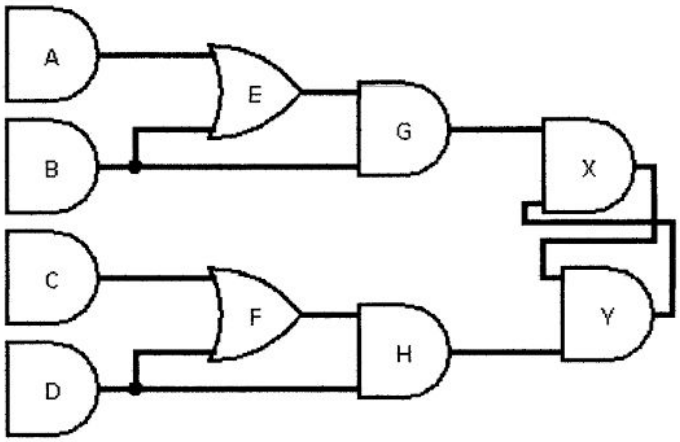
(8) 10pts: Continued...
(B) 4pts: Show a possible Floorplan.



(B) 5pts: Polish representation of Floorplan solution:

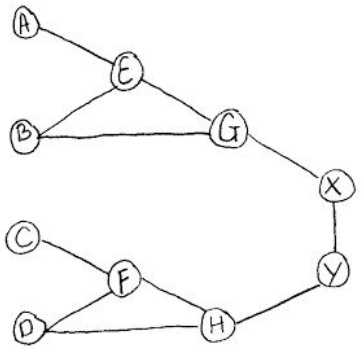
EDh NMh h BAh h LFh Ph V OC V HJ V h GKh h Q V

(9) 10pts: Given the following circuit and gate information, perform floorplanning using the *Dual Graph Technique* in given the working space below (which is not a constraint shape), provide the solution in Polish format and show all work.



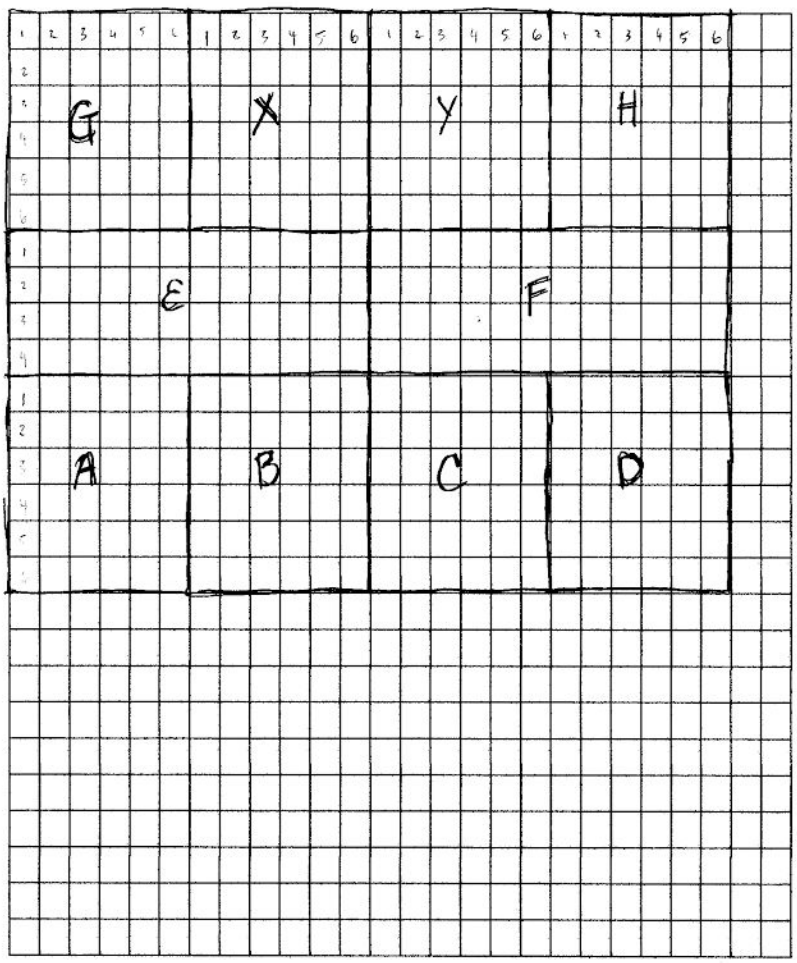
Module	Width	Height
AND	6	6
OR	12	4

(A) 2pts: Show the corresponding circuit graph below.



(9) 10pts: Continued...

(B) 4pts: Show a possible Floorplan.



(C) 4pts: Polish representation of Floorplan solution:

AB v CD v v EF v h GX v YH v v h