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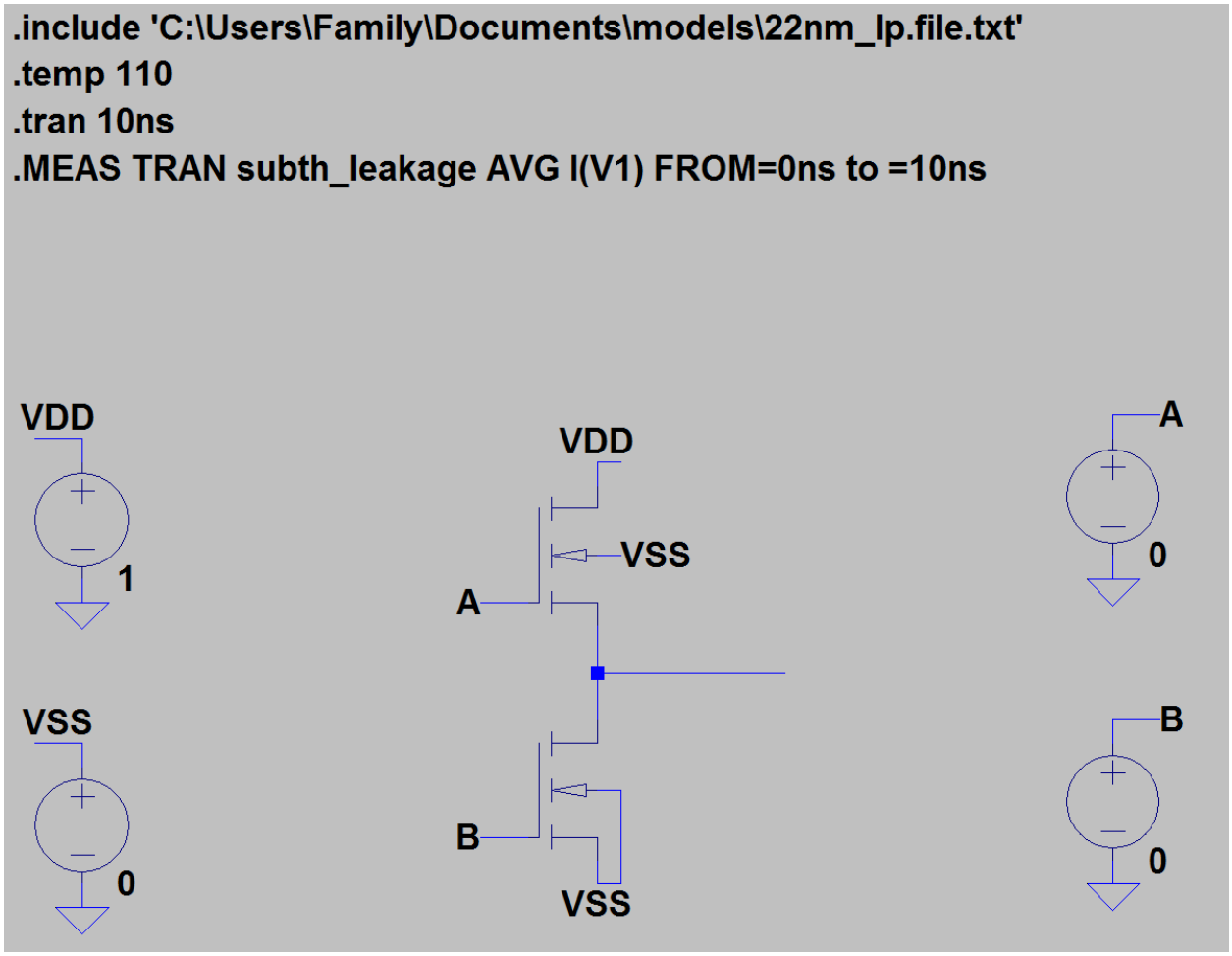
Homework #4

Low Power VLSI Design

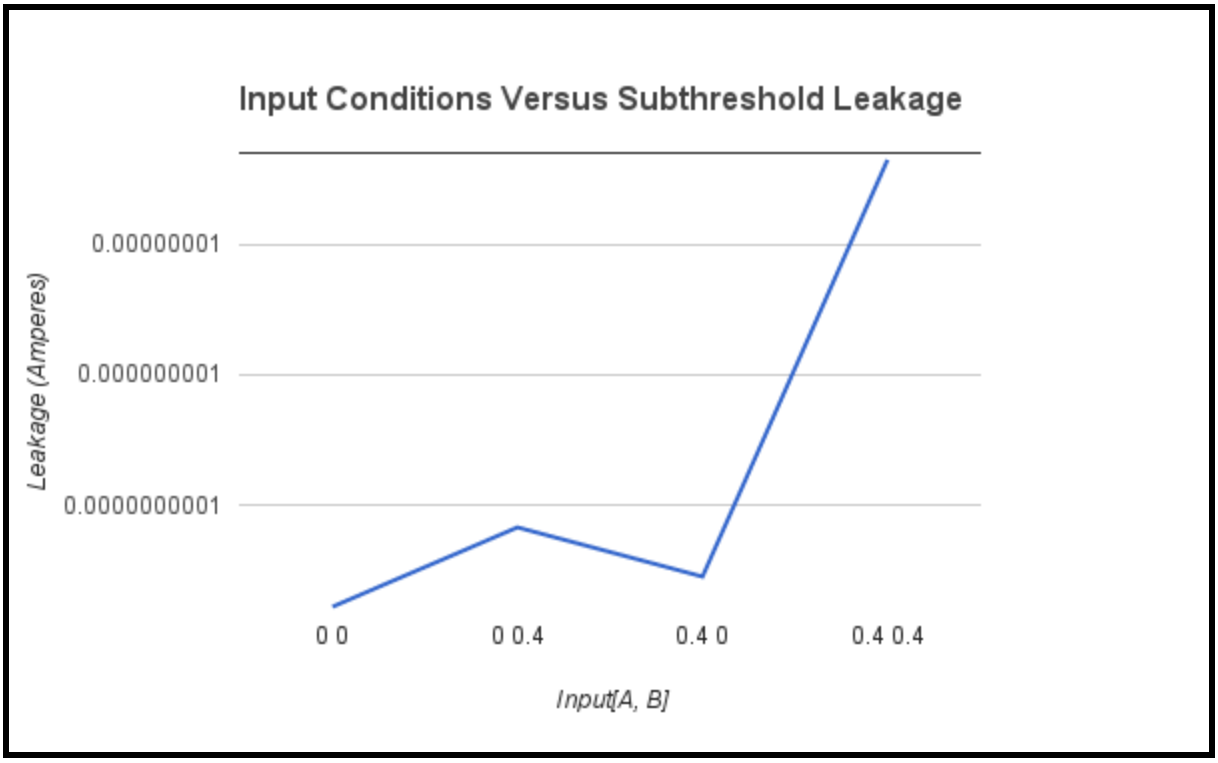
Question 1

Part A : Minimize subthreshold leakage

Schematic



Plot



It can be observed that the input combination when A=0 and B=0 results in the lowest subthreshold leakage (approx. 1.64834e-11 amps) for the stacked NMOS transistors.

To find the subthreshold leakage values for the stacked NMOS transistors the gate voltages remained below the threshold voltage of 0.46v. The following table shows the input combinations…

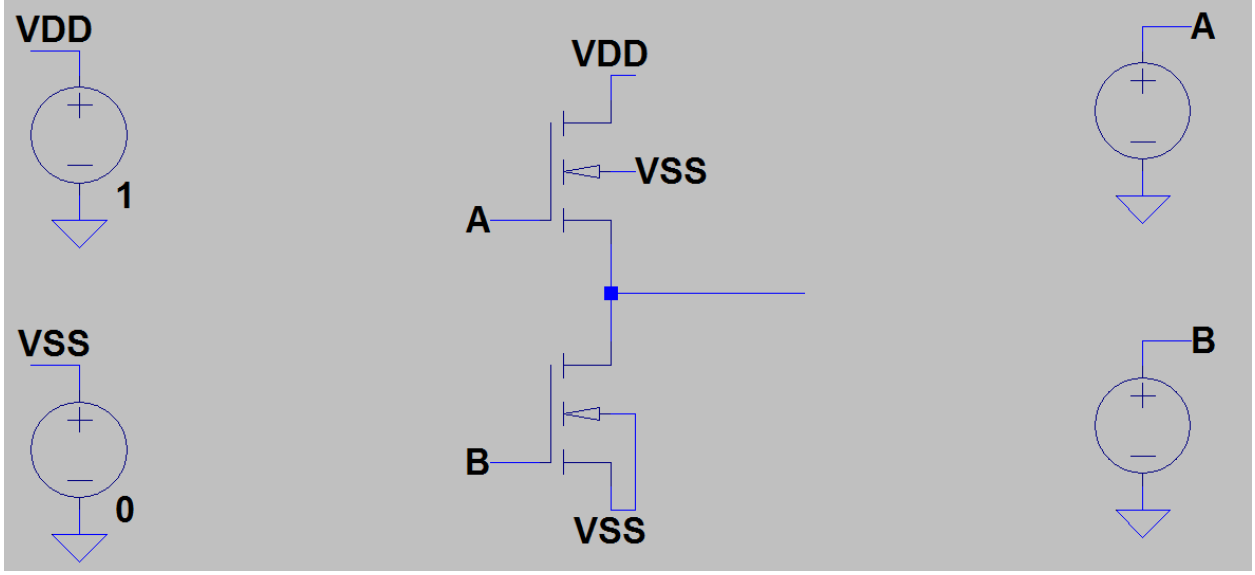
Given 0 < Vgs < Vth

A (Vgs)	B (Vgs)
0	0
0	0.4
0.4	0
0.4	0.4

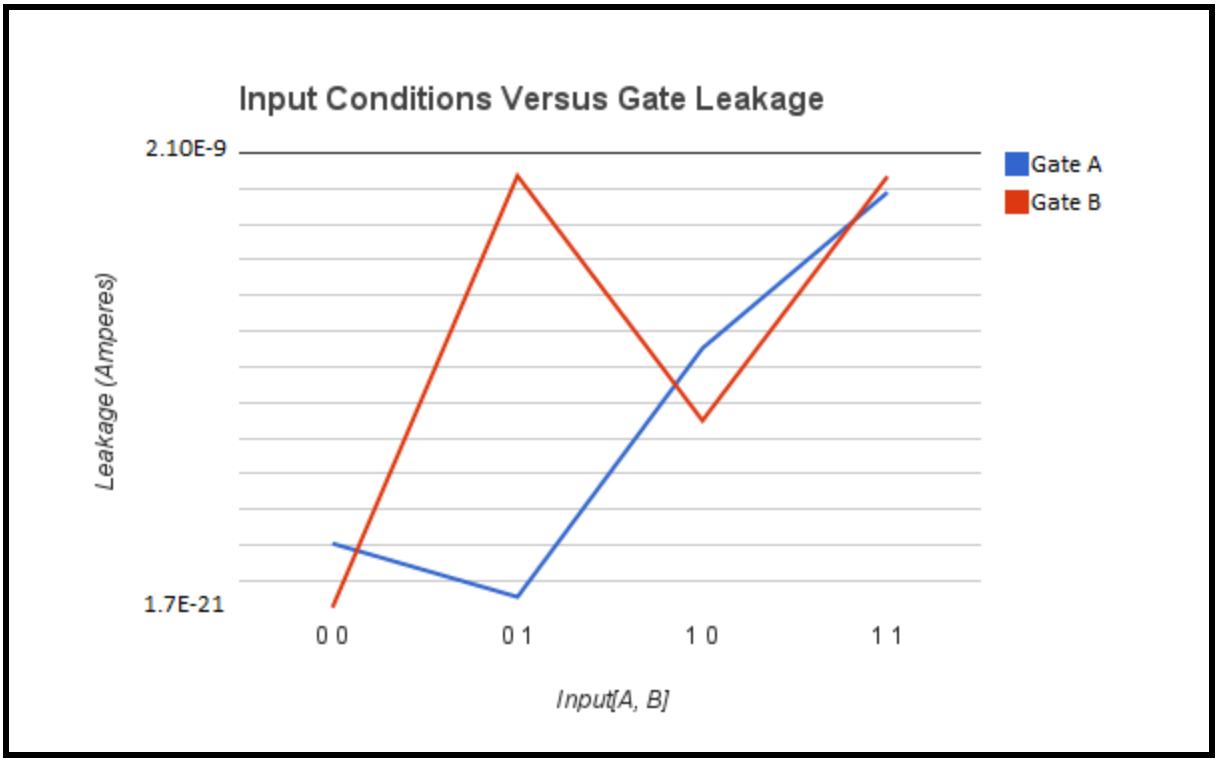
Part B : Minimize gate leakage

Schematic

```
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN gateA_leakage AVG I(V3) FROM=0ns to =10ns
.MEAS TRAN gateB_leakage AVG I(V4) FROM=0ns to =10ns
```



Plot

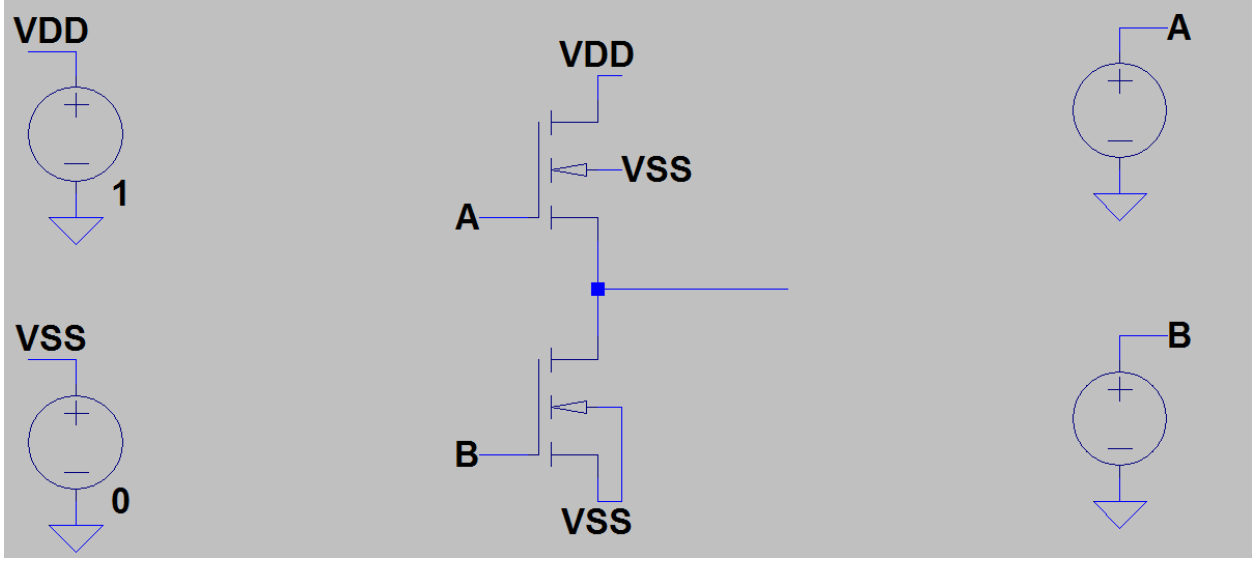


It can be observed that the input combination when A=0 and B=0 results in the lowest gate leakages (approx. 1.08711e-19 amps for A and 1.74224e-21 amps for B) for the stacked NMOS transistors.

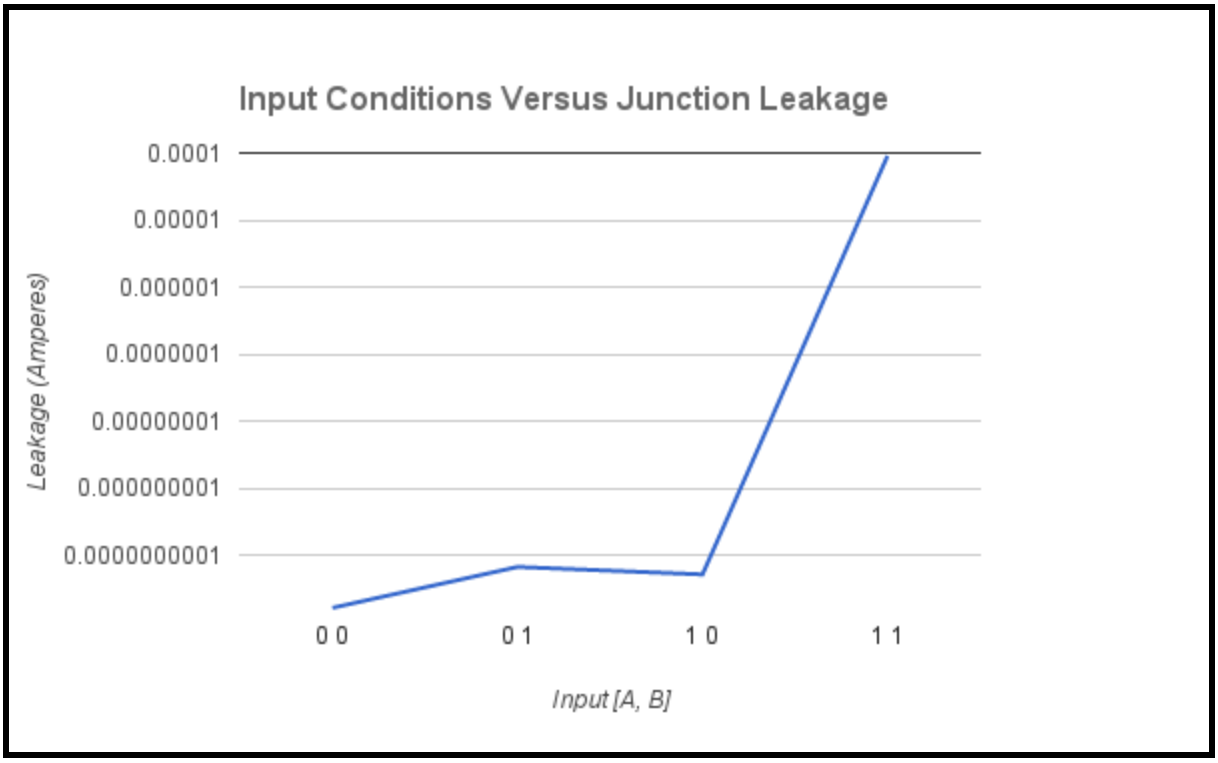
Part C : Minimize junction leakage

Schematic

```
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN junction_leakage AVG I(V1) FROM=0ns to =10ns
```



Plot

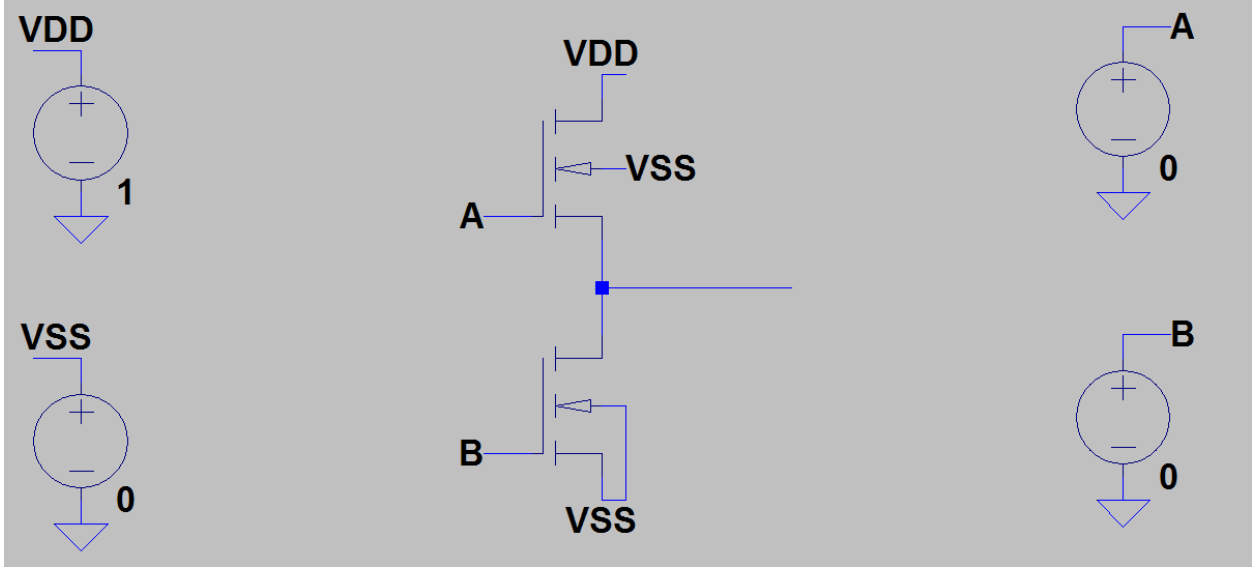


It can be observed that the input combination when A=0 and B=0 results in the lowest junction leakage (approx. 1.64834e-11 amps) for the stacked NMOS transistors.

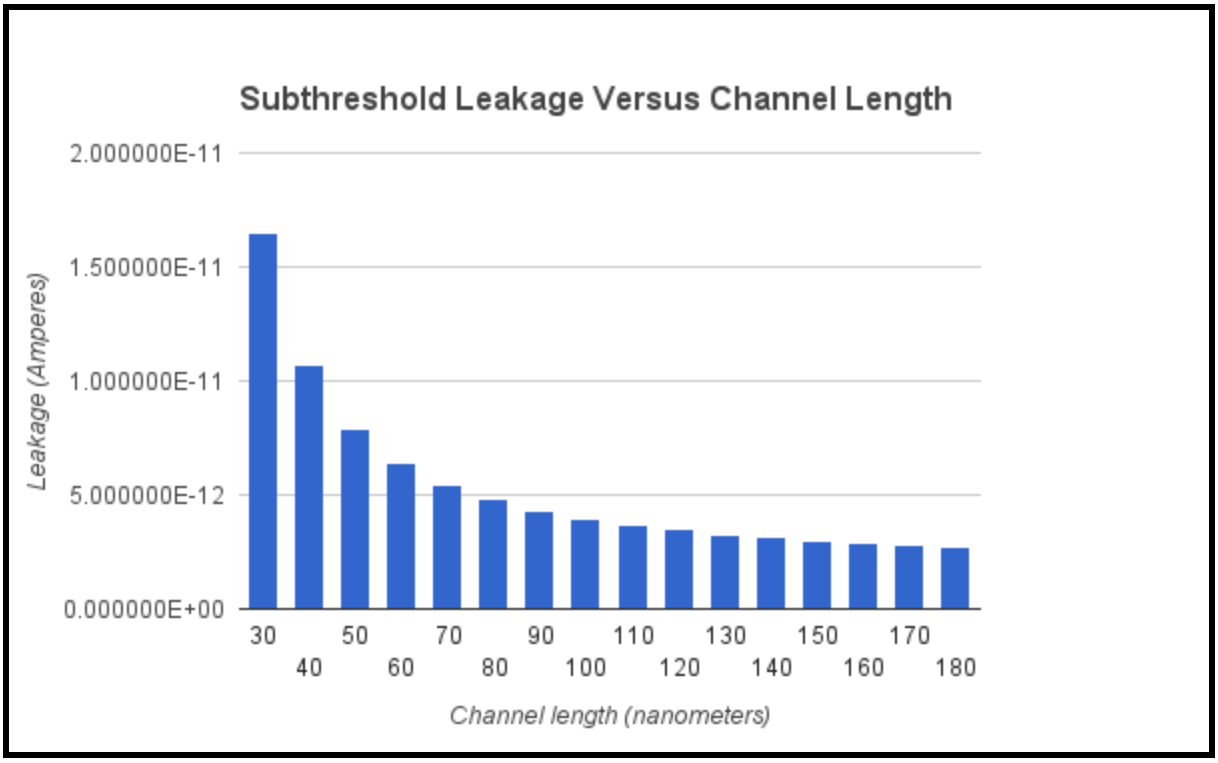
Part D : Sweep channel length and find subthreshold leakage

Schematic

```
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.step param X 30nm 180nm 10nm
```



Plot



It can be observed that the subthreshold leakage diminishes as the channel length of the NMOS transistors increases. This information aligns with the knowledge gained from lecture, more specifically the implementation of long length transistors to reduce subthreshold leakage as used by Intel.

Question 2

A. Between static and dynamic logic, which one is good for low power and why?

In reading the section titled “Dynamic Versus Static Logic” it would appear as if both classes of logic styles have their advantages surrounding low power. However, if one were to judge soley on the author’s decision of the better logic style it seems they favor Dynamic logic for 3 out of 5 logic based occurences.

On the contrary I believe registered Static logic would be a better choice than Dynamic Logic. Following the author’s comments on switching activity it is clearly shown how drastic switching probabilities for a simple NOR gate differ amongst Static and Dynamic logic, favoring Static switching probability of 3/16 to Dynamic switching probability of 3/4.

As an aside, Intel has been using registered Static logic implementations where possible in their low power designs [1].

*[1]
Title: The Dark Knight: Intel’s Core i7
Section: Is Nehalem Efficient?
Author: Anand Lai Shimpi, Gary Key
Date: November 3, 2008
Url: http://www.anandtech.com/show/2658/9

B. For low power should we increase the transistor sizing or reduce it? Explain the tradeoff.

Increasing a transistor’s sizing ratio of W/L does not help reduce energy consumed but instead has the opposite effect assuming an activity factor less than 1 according to Figure 6. Therefore in the realm of low power using the smallest W/L ratio will provide the best sizing.

The tradeoff to choosing a small W/L ratio is that “an ‘optimal’ supply voltage is necessary in minimizing power consumption” according to the author.

C. How logic duplication helps in lowering the power consumption? Explain with power equation and example.

Logic duplication (parallel architecture) allows the designer to lower supply voltage and speed requirements while still maintaining original throughput of the higher vdd, speed requirement single logic block. However, there is an increase in effective capacitance and circuit area.

Given the original equation for power…

$P_{ref} = C_{ref} \times V^2_{ref} \times f_{ref}$

Power for parallel path…

$P_{par} = C_{par} \times V^2_{par} \times f_{par}$

where $f_{par} = f_{ref} / 2$, $V^2_{par} << V^2_{ref}$, $C_{par} > C_{ref}$

D. How pipelining helps in lowering the power consumption? Explain with power equation and example.

Pipelining allows the designer to lower supply voltage while still maintaining original throughput using intervalic latches between logic components/blocks. It's obvious this technique shares advantages of logic duplication however it exceeds logic duplication in minimizing extra effective capacitance and area overhead without having to reduce operating frequency.

Given the original equation for power…

$P_{ref} = C_{ref} \times V^2_{ref} \times f_{ref}$

Power for pipelining path…

$P_{pipe} = C_{pipe} \times V^2_{pipe} \times f_{pipe}$

where $f_{pipe} = f_{ref}$, $V^2_{pipe} << V^2_{ref}$, $C_{pipe} > C_{ref}$

E. Is it possible to continue logic duplication infinitely to keep lowering voltage and reduce power? If not, what sets the limits for logic duplication?

No, it's not feasible to continue logic duplication and lowering of supply voltage to reduce power "as supply voltages approach[ing] device thresholds, the gate delays increase rapidly" as stated by the author. In accordance with extremely low voltages near device thresholds the amount of logic duplication necessary to maintain desired throughput reaches a point where the extra circuitry overhead will neglect any gains seen in power reduction.

Appendix

A=0 & B=0 Subthreshold Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-1.64834e-011 FROM 0 TO 1e-008


Date: Fri Apr 10 21:24:11 2015
Total elapsed time: 0.109 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2090
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.3/2.0/[1.6]
Matrix Compiler2: off  [1.9]/2.1/2.1
```

A=0 & B=0 Subthreshold Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0
V4 B 0 0
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```

A=0 & B=0.4 Subthreshold Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-6.70723e-011 FROM 0 TO 1e-008


Date: Fri Apr 10 21:28:08 2015
Total elapsed time: 0.109 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2096
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.3/2.9/[1.6]
Matrix Compiler2: off  [2.0]/2.2/2.1
```

A=0 & B=0.4 Subthreshold Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0
V4 B 0 0.4
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```

A=0.4 & B=0 Subthreshold Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-2.80848e-011 FROM 0 TO 1e-008


Date: Fri Apr 10 21:31:37 2015
Total elapsed time: 0.094 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2096
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.4/2.2/[1.6]
Matrix Compiler2:     136 opcodes  2.0/[2.0]/2.2
```

A=0.4 & B=0 Subthreshold Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0.4
V4 B 0 0
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```

A=0.4 & B=0.4 Subthreshold Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-4.43832e-008 FROM 0 TO 1e-008


Date: Fri Apr 10 21:33:42 2015
Total elapsed time: 0.109 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2096
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.3/2.2/[1.7]
Matrix Compiler2: off  [2.0]/2.1/2.1
```

A=0.4 & B=0.4 Subthreshold Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part A\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0.4
V4 B 0 0.4
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```

A=0 & B=0 Gate Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc

Direct Newton iteration for .op point succeeded.

gatea_leakage: AVG(i(v3))=1.08711e-019 FROM 0 TO 1e-008
gateb_leakage: AVG(i(v4))=-1.74224e-021 FROM 0 TO 1e-008


Date: Fri Apr 10 17:49:45 2015
Total elapsed time: 0.102 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2090
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.3/2.0/[1.6]
Matrix Compiler2: off  [1.8]/2.2/2.1
```

A=0 & B=0 Gate Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0
V4 B 0 0
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN gateA_leakage AVG I(V3) FROM=0ns to =10ns
.MEAS TRAN gateB_leakage AVG I(V4) FROM=0ns to =10ns
.backanno
.end
```

A=0 & B=1 Gate Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc

Direct Newton iteration for .op point succeeded.

gatea_leakage: AVG(i(v3))=-3.44982e-021 FROM 0 TO 1e-008
gateb_leakage: AVG(i(v4))=-2.28458e-009 FROM 0 TO 1e-008


Date: Fri Apr 10 17:53:09 2015
Total elapsed time: 0.099 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2088
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.4/2.1/[1.6]
Matrix Compiler2: 1.79 KB object code size  3.1/2.1/[2.0]
```

A=0 & B=1 Gate Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0
V4 B 0 1
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN gateA_leakage AVG I(V3) FROM=0ns to =10ns
.MEAS TRAN gateB_leakage AVG I(V4) FROM=0ns to =10ns
.backanno
.end
```

A=1 & B=0 Gate Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc

Direct Newton iteration for .op point succeeded.

gatea_leakage: AVG(i(v3))=-3.30162e-014 FROM 0 TO 1e-008
gateb_leakage: AVG(i(v4))=3.07588e-016 FROM 0 TO 1e-008


Date: Fri Apr 10 17:55:54 2015
Total elapsed time: 0.102 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2089
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.4/2.1/[1.7]
Matrix Compiler2: 1.79 KB object code size  2.0/2.1/[2.0]
```

A=1 & B=0 Gate Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 1
V4 B 0 0
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN gateA_leakage AVG I(V3) FROM=0ns to =10ns
.MEAS TRAN gateB_leakage AVG I(V4) FROM=0ns to =10ns
.backanno
.end
```

A=1 & B=1 Gate Leakage Errorlog

```
Circuit: * C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc

Direct Newton iteration for .op point succeeded.

gatea_leakage: AVG(i(v3))=-7.82133e-010 FROM 0 TO 1e-008
gateb_leakage: AVG(i(v4))=-2.19726e-009 FROM 0 TO 1e-008


Date: Fri Apr 10 17:54:50 2015
Total elapsed time: 0.097 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2089
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.4/2.1/[1.8]
Matrix Compiler2: 1.79 KB object code size  1.9/2.2/[2.0]
```

A=1 & B=1 Gate Leakage Netlist

```
* C:\Users\Family\Desktop\Low Power HW4\Q1 Part B\HW4 Q1 part B.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 1
V4 B 0 1
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN gateA_leakage AVG I(V3) FROM=0ns to =10ns
.MEAS TRAN gateB_leakage AVG I(V4) FROM=0ns to =10ns
.backanno
.end
```

A=0 & B=0 Junction Leakage Errorlog

```
Circuit: * C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-1.64834e-011 FROM 0 TO 1e-008


Date: Fri Apr 10 15:21:30 2015
Total elapsed time: 0.094 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2090
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.3/2.0/[1.6]
Matrix Compiler2:     136 opcodes  1.9/[1.9]/2.0
```

A=0 & B=0 Junction Leakage Netlist

```
* C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0
V4 B 0 0
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```

A=0 & B=1 Junction Leakage Errorlog

```
Circuit: * C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-6.71652e-011 FROM 0 TO 1e-008


Date: Fri Apr 10 15:24:56 2015
Total elapsed time: 0.094 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2088
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.4/2.0/[1.6]
Matrix Compiler2: 1.79 KB object code size  1.8/1.9/[1.9]
```

A=0 & B=1 Junction Leakage Netlist

```
* C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 0
V4 B 0 1
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```

A=1 & B=0 Junction Leakage Errorlog

```
Circuit: * C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-5.19164e-011 FROM 0 TO 1e-008


Date: Fri Apr 10 15:28:23 2015
Total elapsed time: 0.140 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2089
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.4/2.0/[1.6]
Matrix Compiler2: 1.79 KB object code size  1.8/2.0/[1.8]
```

A=1 & B=0 Junction Leakage Netlist

```
* C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 1
V4 B 0 0
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```

A=1 & B=1 Junction Leakage Errorlog

```
Circuit: * C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc

Direct Newton iteration for .op point succeeded.

subth_leakage: AVG(i(v1))=-9.02435e-005 FROM 0 TO 1e-008


Date: Fri Apr 10 15:29:51 2015
Total elapsed time: 0.093 seconds.

tnom = 27
temp = 110
method = modified trap
totiter = 2089
traniter = 2082
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 17
fillins = 0
solver = Normal
Matrix Compiler1: 1.16 KB object code size  2.5/2.1/[1.9]
Matrix Compiler2: off  [1.9]/2.1/4.1
```

A=1 & B=1 Junction Leakage Netlist

```
* C:\Program Files (x86)\LTC\LTspiceIV\HW4 Q1 part A.asc
M1 VDD A N001 VSS NMOS l=0.03u w=1u
M2 N001 B VSS VSS NMOS l=0.03u w=1u
V1 VDD 0 1
V2 VSS 0 0
V3 A 0 1
V4 B 0 1
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 110
.tran 10ns
.MEAS TRAN subth_leakage AVG I(V1) FROM=0ns to =10ns
.backanno
.end
```