Homework #2

Due Jan 30, 2015

CIS 4930/6930, Fall 2015

Low Power VLSI Design

Notes:

1. The homework will be done and the report submitted individually.

2. Submit your files in a single zip folder with name_HW2 as folder name.

3. Submit the screenshots of waveforms and Error log files in .png file format

4. Default operating temperature is 25C and Vdd=1V

Perform transistor-level circuit simulations using LTspice of NMOS transistor using 22nm CMOS process technology. Keep channel length= 0.03u for all simulations.

Q1. Using SPICE, generate the family of I-V curves for an NMOS transistor with the following parameters:

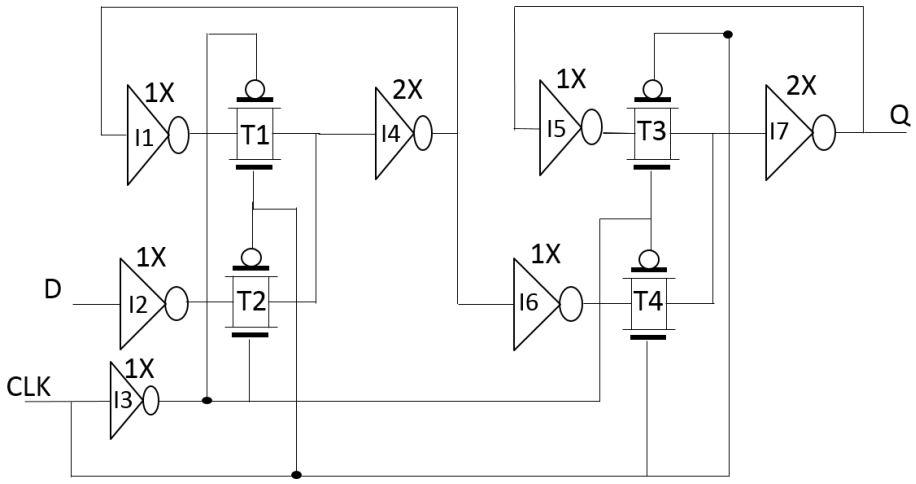
W/L = 1u/0.03u use VSB=0V.
Sweep VDS from 0V to 1.0V in 0.1V increments
Sweep VGS from 0V to 1.0V in 0.2V increments
Report your plot (you can use excel to plot the results).

Hint: You can use DC sweep to change both drain and source voltage using following LTspice setting.
Simulate -> Edit Simulation cmd -> DC Sweep

(20+20 points)

Q2. Using inverters and pass transistors, design a master slave flip flop with VDD = 1V. Note that master and slave stages are identical so if you size one stage then you should reuse the same for other stage.
(a) Demonstrate the operation of flip-flop by writing a 0 and 1 with a clock frequency of 2GHz.
(b) Report the setup time, hold time and CLK-2-Q delay.

(30+30 points)



NOTE: For 1X: Wn=0.4u Wp=0.7u and for 2X: Wn=0.8u Wp=1.4u. The mux size is Wp=1.4u and Wn=0.8u.

BONUS QUESTION:

In Q2, scale the voltage from 0.1V-1V in the step 0.1V. Plot the trend of energy and CLK-2-Q delay of the MS flip flop with voltage.

10 points