Team Low Power Rangers
CIS 4930 Sec 001 Spring 2015
Due: 3/23/2015

Chris Frazier
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Low Power VLSI Project: Stage 1 Report

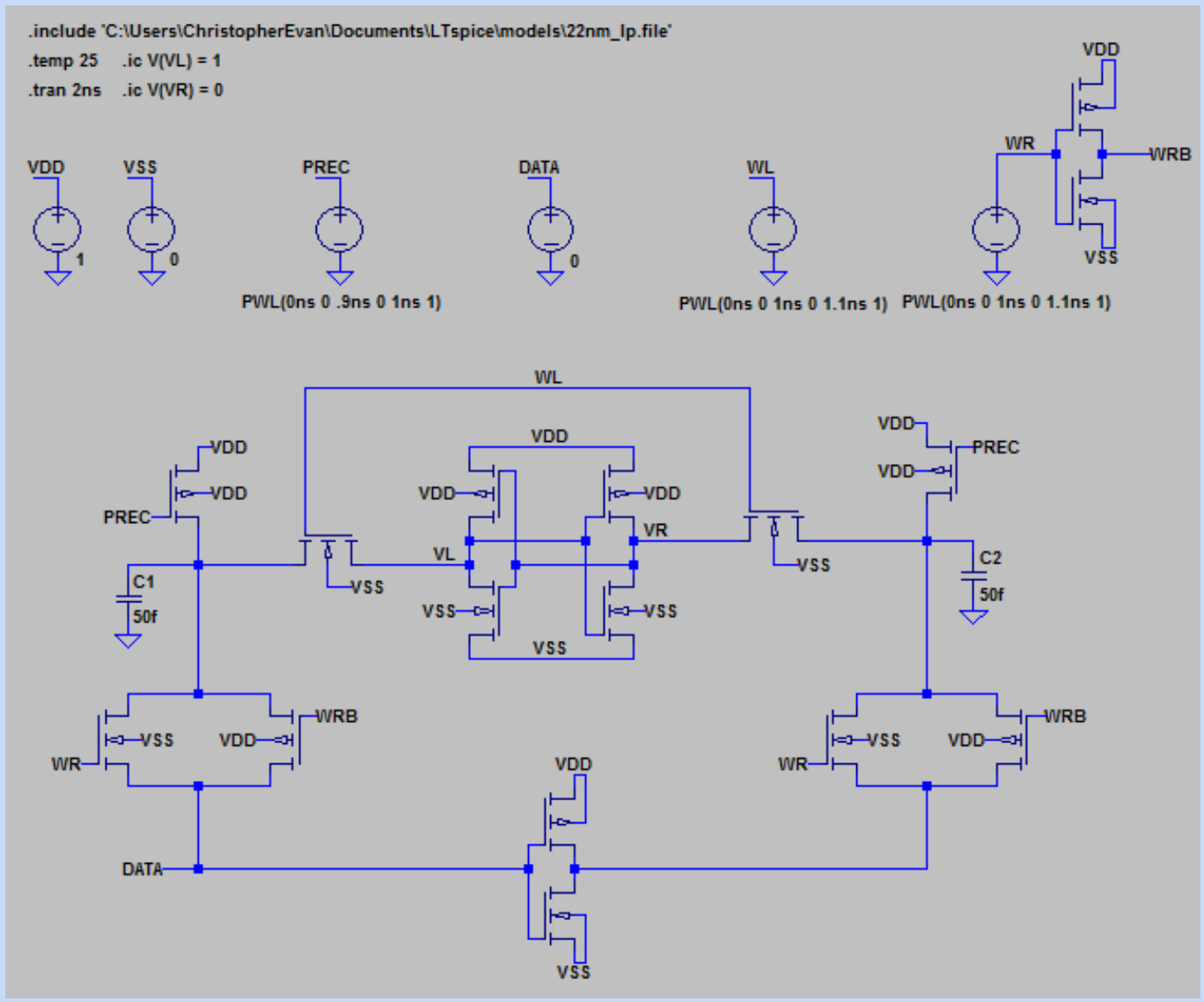
Work Division

Chris Frazier:	33%
Bassam Saed:	33%
John Gangemi:	33%

(**a**) Design a SRAM cell as shown in Fig. 1 with transistor sizes of (W/L)p0= (W/L)p1=0.7um/30nm, (W/L)n0=(W/L)n1=0.4um/30nm, and access transistors (W/L)n2=(W/L)n3=0.8um/30nm.

Schematics

Write 0



Team Low Power Rangers
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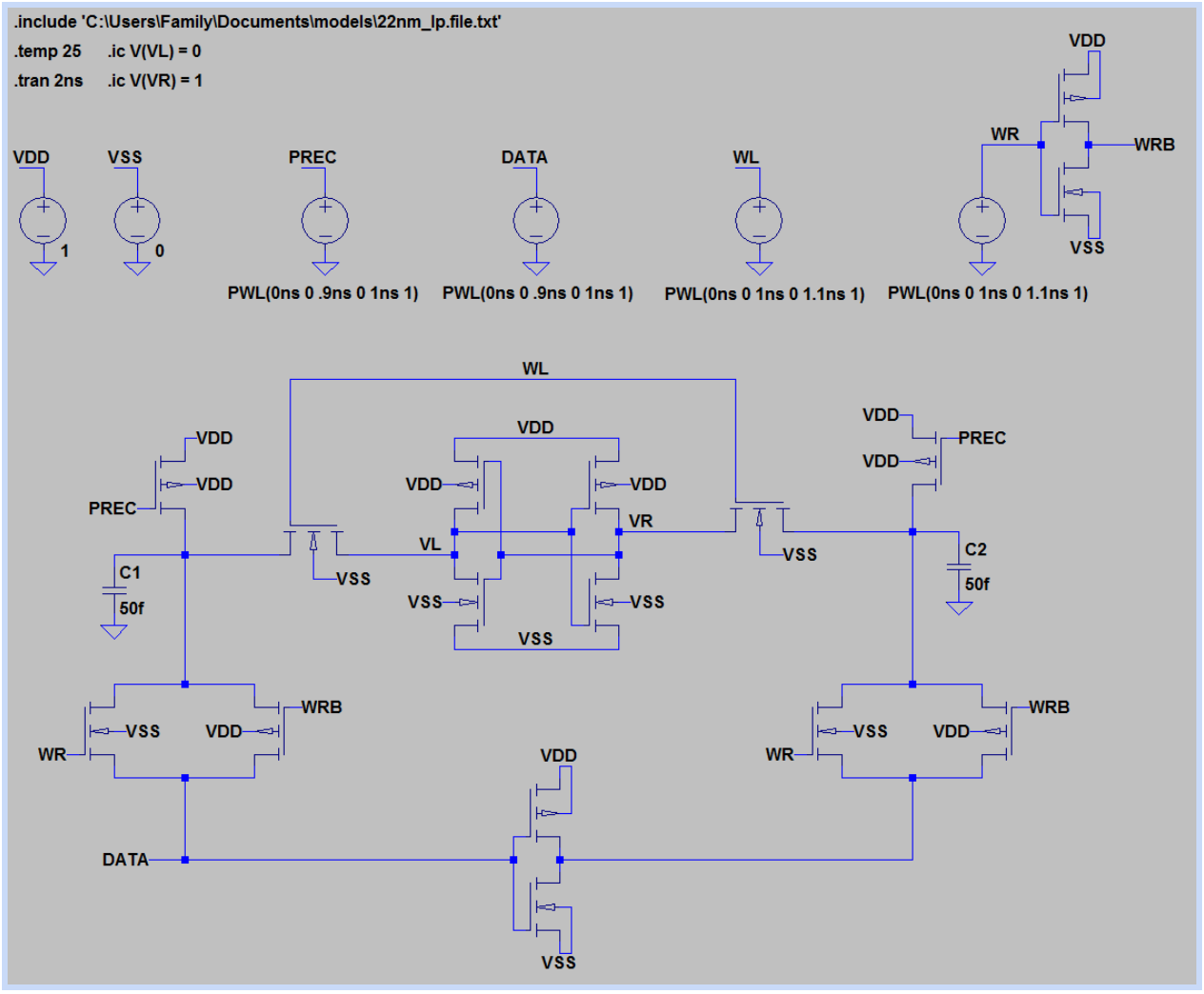
Write 1



Team Low Power Rangers
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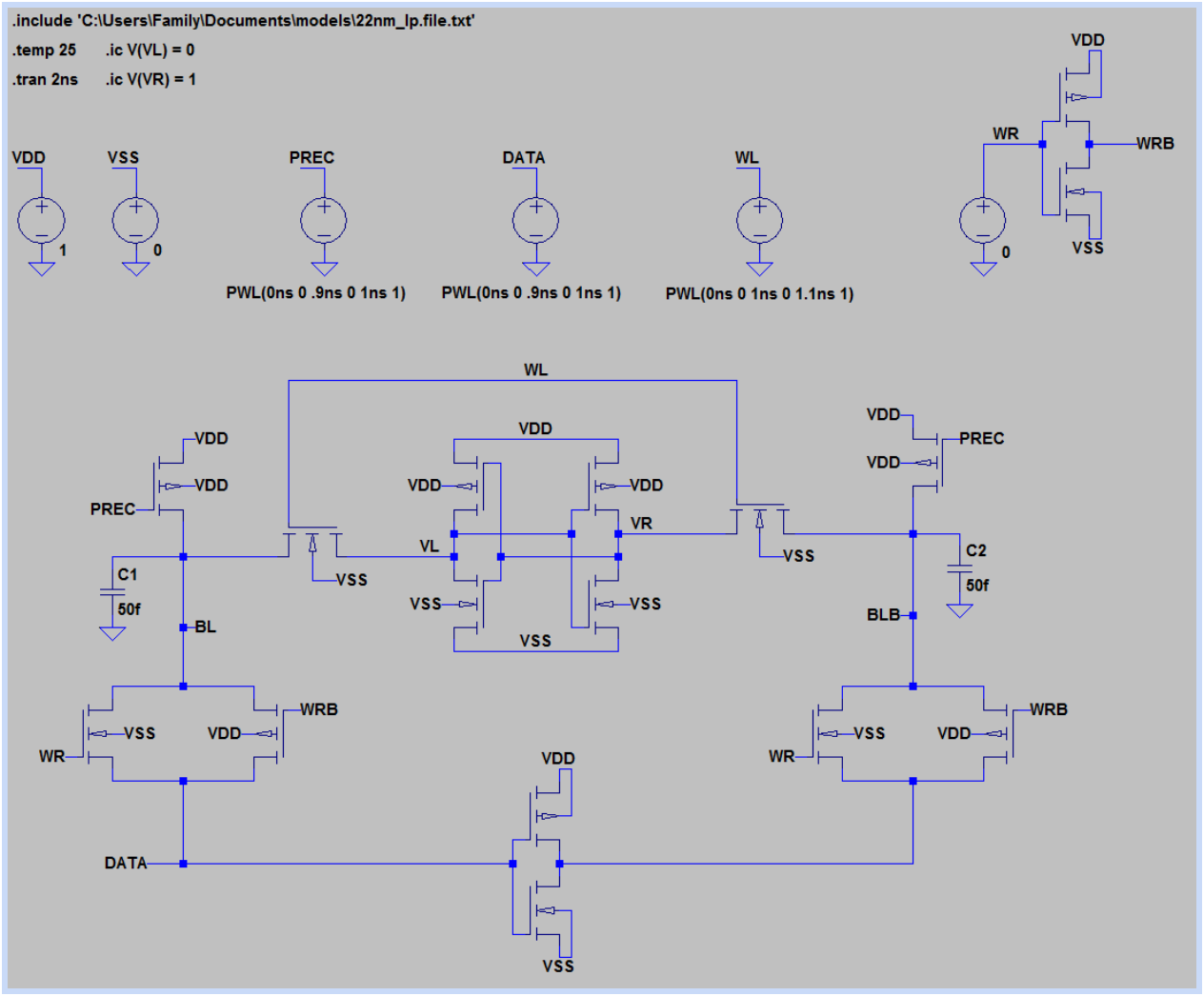
Read



(**b**) Measure read delay and read energy for 100mV sense margin, write delay and write energy to write Data=0 and Data=1.

Write: Timing diagram in Fig. 1 illustrates the write operation to write data=1.
Read: Timing diagram in Fig. 1 illustrates the read operation with the control signals and bit line voltages when data=1.

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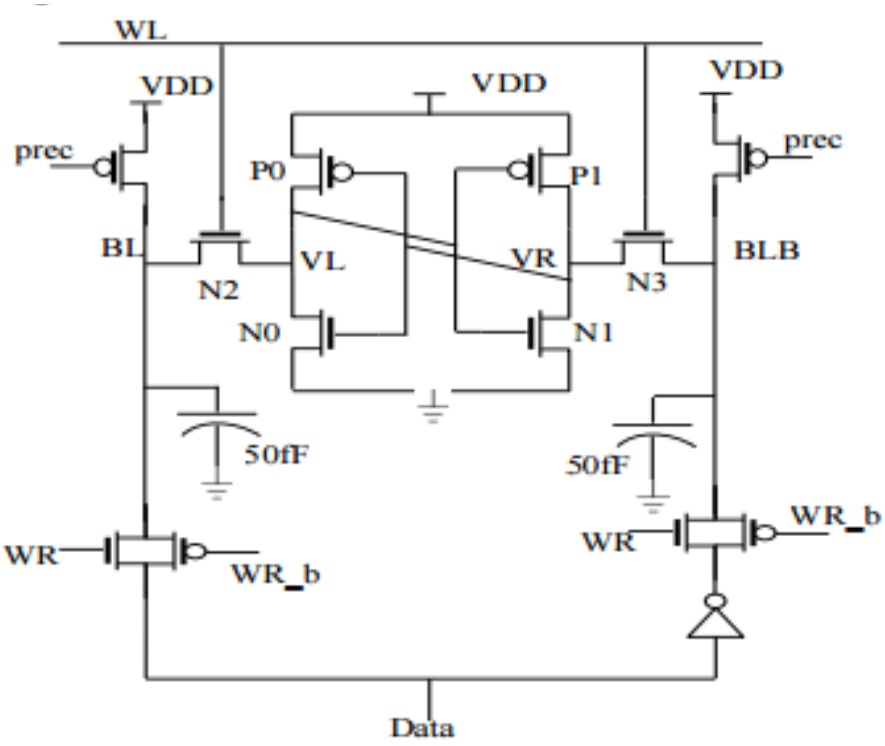
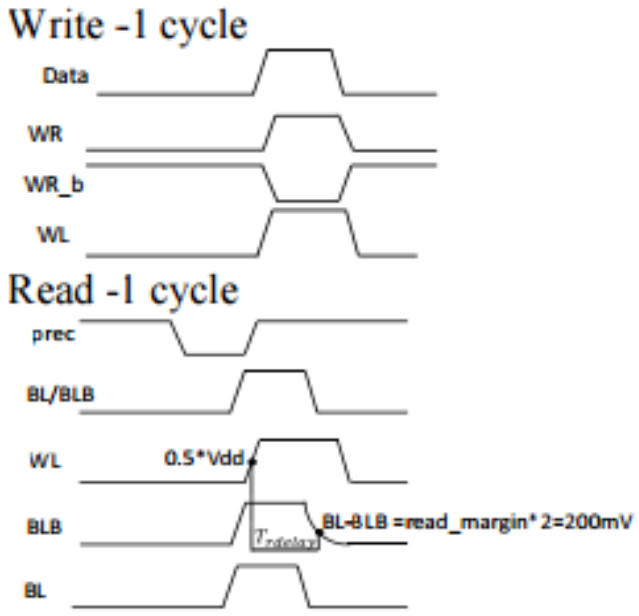
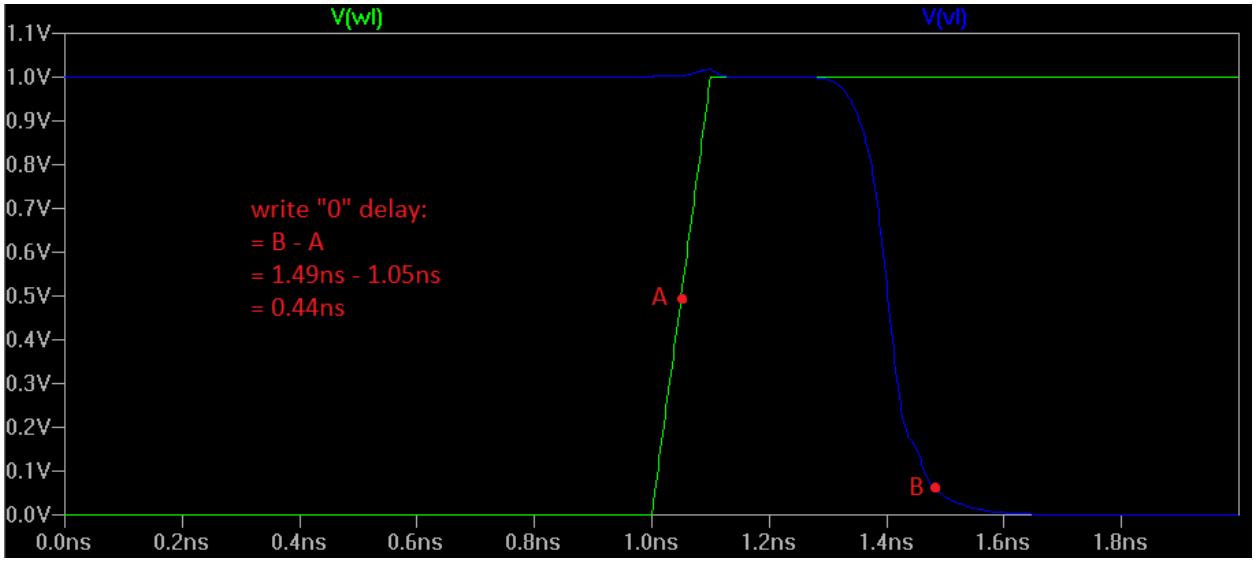
Fig. 1 SRAM cell





Write

Write 0 Delay



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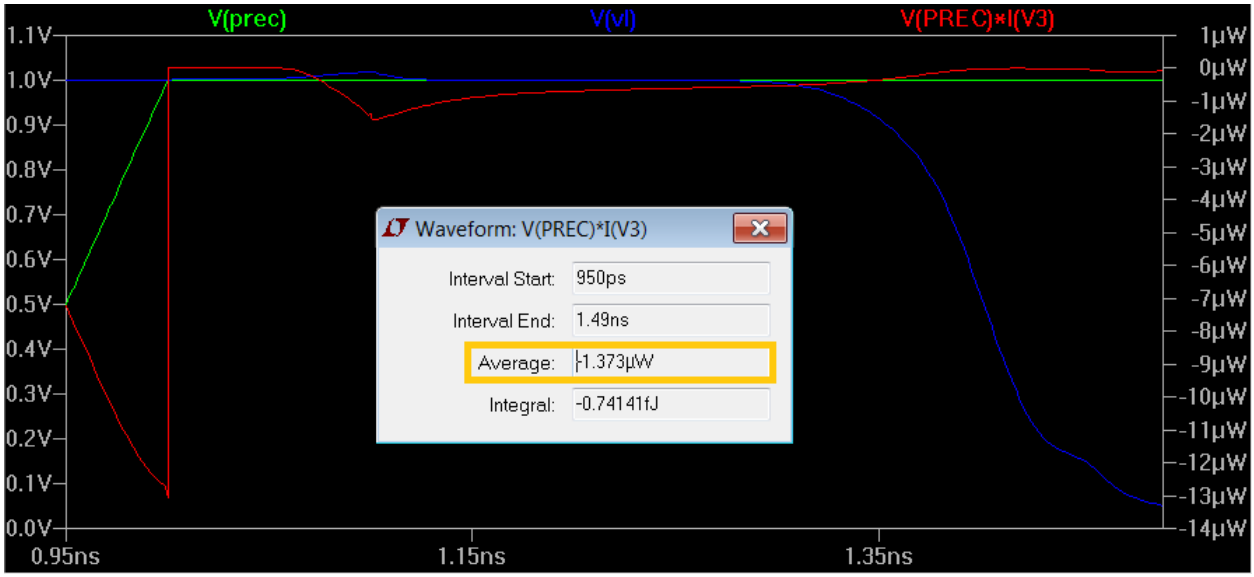
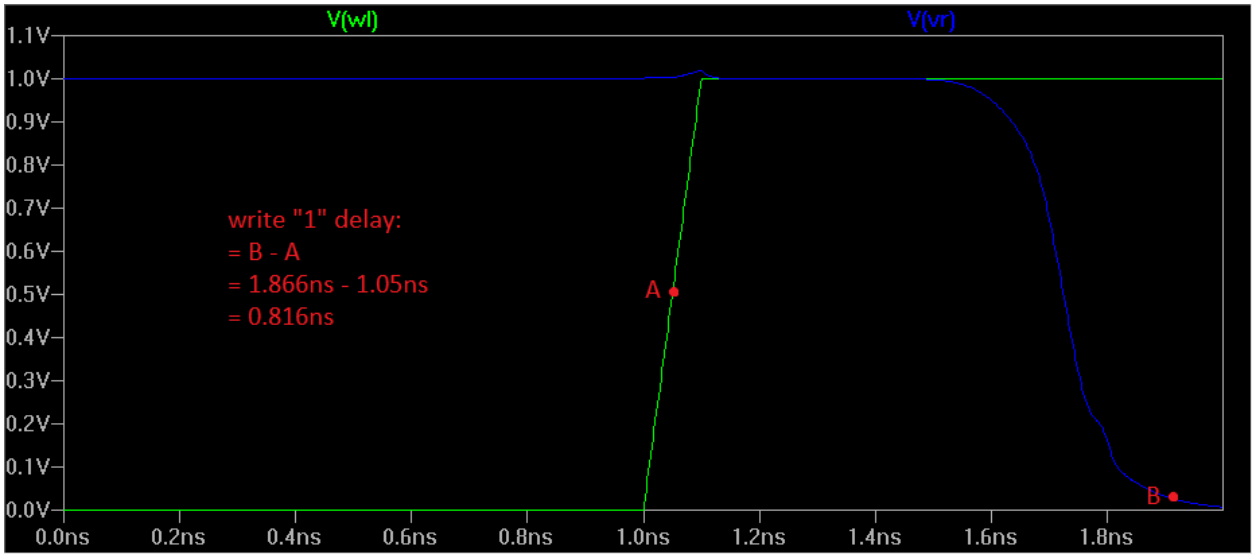
To find the write “0” delay one must measure the time interval when the write line (WL, point A) is at 50% VDD and signal VL (point B) is at 0.05 VDD.

Write 0 Energy



To find the write “0” energy one must measure the power dissipated in the time interval when precharge signal is at 50% VDD and signal VL is at 0.05 VDD. The time interval is approximately 0.44 ns in length.

Write 1 Delay



To find the write “1” delay one must measure the time interval when the write line (WL, point A) is at 50% VDD and signal VR (point B) is at 0.05 VDD.

Team Low Power Rangers
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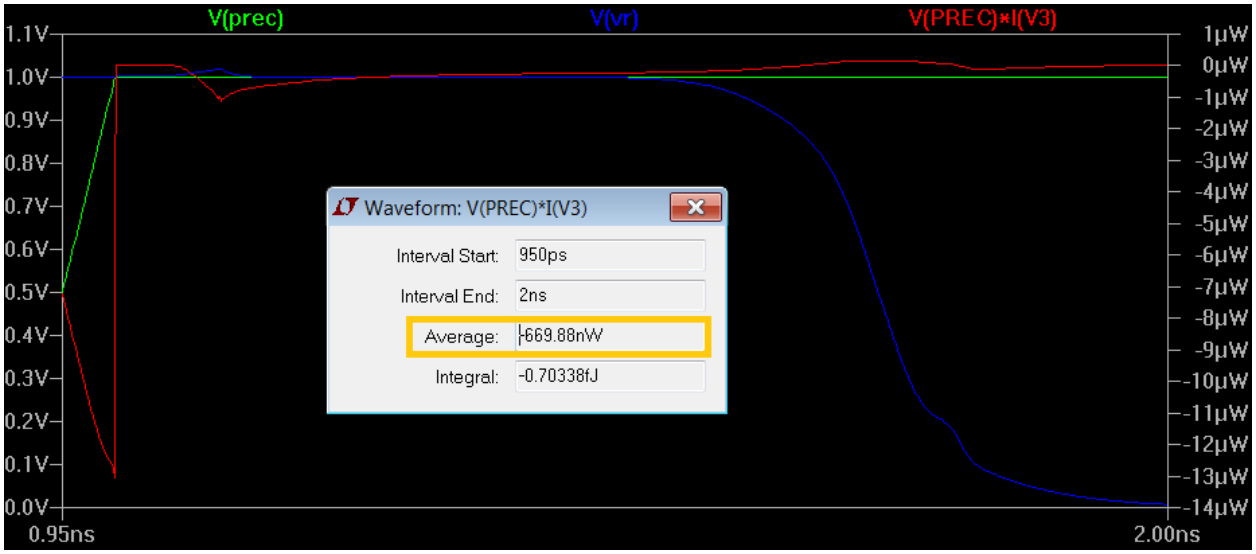
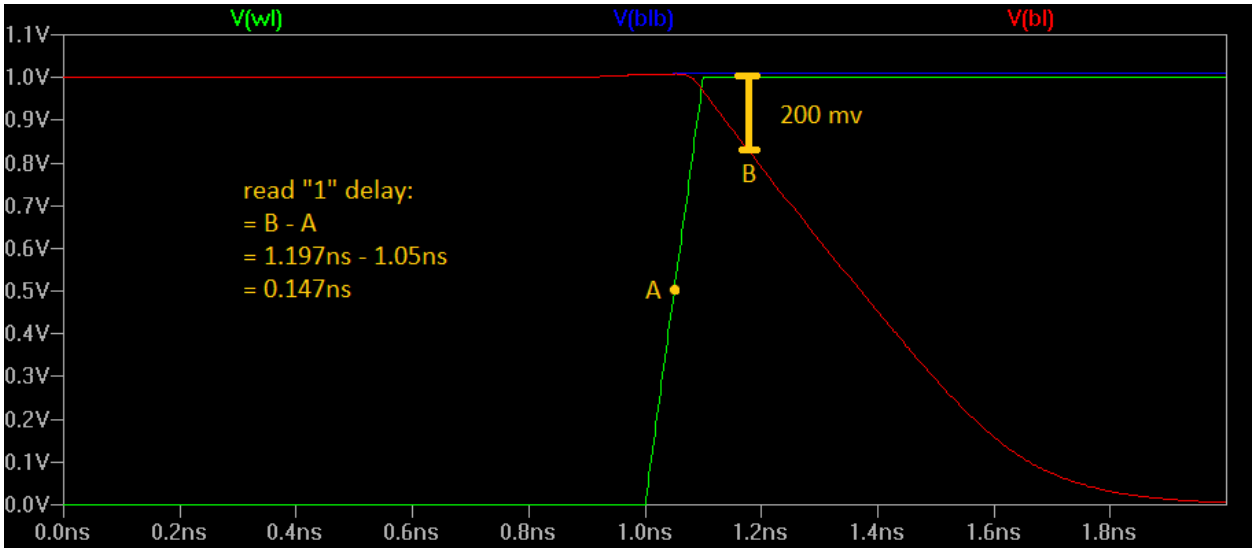
Write 1 Energy



To find the write “1” energy one must measure the power dissipated in the time interval when precharge signal is at 50% VDD and signal VR is at 0.05 VDD. The time interval is approximately 0.816 ns in length.

Read

Read Delay



To find the read delay of the SRAM circuit one must measure the interval when signal WL (point A) is at 50% VDD and the difference between BLB/BL is 200 mv (point B). This interval is 0.147ns in length.

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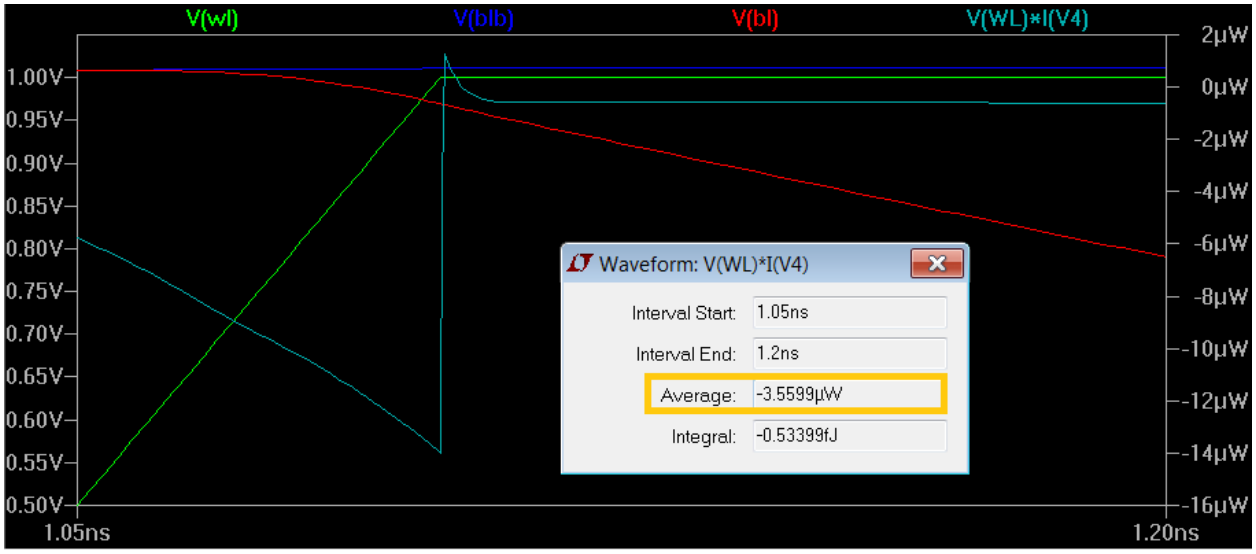
Read Energy



To find the read energy of the SRAM circuit one must measure the power dissipated when signal WL (point A) is at 50% VDD and the difference between BLB/BL is 200 mv (point B).

Appendix

Write 0 Error Log

```
Circuit: * C:\Users\Family\Desktop\Low Power Stage 1\Write\Stage 1 Write 0.asc

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Direct Newton iteration for .op point succeeded.

Date: Mon Mar 23 13:17:22 2015
Total elapsed time: 0.499 seconds.

tnom = 27
temp = 25
method = modified trap
totiter = 2152
traniter = 2138
tranpoints = 1051
accept = 1051
rejected = 0
matrix size = 82
fillins = 4
solver = Normal
Matrix Compiler1: 10.6 KB object code size  8.8/7.1/[4.5]
Matrix Compiler2: 11.3 KB object code size  4.6/5.7/[3.5]
```

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Write 0 Netlist

```
* C:\Users\Family\Desktop\Low Power Stage 1\Write\Stage 1 Write 0.asc
M1 VL VR VDD VDD PMOS l=0.03u w=0.7u
M2 VDD VL VR VDD PMOS l=0.03u w=0.7u
M3 VSS VR VL VSS NMOS l=0.03u w=0.4u
M4 VR VL VSS VSS NMOS l=0.03u w=0.4u
V1 VDD 0 1
V2 VSS 0 0
M5 DATA WRB N002 VDD PMOS l=0.03u w=0.7u
M6 N002 WR DATA VSS NMOS l=0.03u w=0.4u
M7 N003 WRB N001 VDD PMOS l=0.03u w=0.7u
M8 N001 WR N003 VSS NMOS l=0.03u w=0.4u
M9 VDD DATA N003 VDD PMOS l=0.03u w=0.7u
M10 N003 DATA VSS VSS NMOS l=0.03u w=0.4u
M11 VDD PREC N002 VDD PMOS l=0.03u w=0.7u
M12 N001 PREC VDD VDD PMOS l=0.03u w=0.7u
M13 VL WL N002 VSS NMOS l=0.03u w=0.8u
M14 N001 WL VR VSS NMOS l=0.03u w=0.8u
C1 N002 0 50f
C2 N001 0 50f
V3 PREC 0 PWL(0ns 0 .9ns 0 1ns 1)
V4 WL 0 PWL(0ns 0 1ns 0 1.1ns 1)
V5 WR 0 PWL(0ns 0 1ns 0 1.1ns 1)
M15 VDD WR WRB VDD PMOS l=0.03u w=0.7u
M16 WRB WR VSS VSS NMOS l=0.03u w=0.4u
V6 DATA 0 0
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 25
.tran 2ns
.ic V(VL) = 1
.ic V(VR) = 0
.backanno
.end
```

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Write 1 Error Log

```
Circuit: * C:\Users\Family\Desktop\Low Power Stage 1\Write\Stage 1 Write 1.asc

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Direct Newton iteration for .op point succeeded.

Date: Mon Mar 23 13:19:26 2015
Total elapsed time: 0.483 seconds.

tnom = 27
temp = 25
method = modified trap
totiter = 2157
traniter = 2143
tranpoints = 1051
accept = 1051
rejected = 0
matrix size = 82
fillins = 4
solver = Normal
Matrix Compiler1: 10.6 KB object code size  8.1/7.0/[4.1]
Matrix Compiler2: 11.3 KB object code size  4.6/5.9/[3.4]
```

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Write 1 Netlist

```
* C:\Users\Family\Desktop\Low Power Stage 1\Write\Stage 1 Write 1.asc
M1 VL VR VDD VDD PMOS l=0.03u w=0.7u
M2 VDD VL VR VDD PMOS l=0.03u w=0.7u
M3 VSS VR VL VSS NMOS l=0.03u w=0.4u
M4 VR VL VSS VSS NMOS l=0.03u w=0.4u
V1 VDD 0 1
V2 VSS 0 0
M5 DATA WRB N002 VDD PMOS l=0.03u w=0.7u
M6 N002 WR DATA VSS NMOS l=0.03u w=0.4u
M7 N003 WRB N001 VDD PMOS l=0.03u w=0.7u
M8 N001 WR N003 VSS NMOS l=0.03u w=0.4u
M9 VDD DATA N003 VDD PMOS l=0.03u w=0.7u
M10 N003 DATA VSS VSS NMOS l=0.03u w=0.4u
M11 VDD PREC N002 VDD PMOS l=0.03u w=0.7u
M12 N001 PREC VDD VDD PMOS l=0.03u w=0.7u
M13 VL WL N002 VSS NMOS l=0.03u w=0.8u
M14 N001 WL VR VSS NMOS l=0.03u w=0.8u
C1 N002 0 50f
C2 N001 0 50f
V3 PREC 0 PWL(0ns 0 .9ns 0 1ns 1)
V4 WL 0 PWL(0ns 0 1ns 0 1.1ns 1)
V5 WR 0 PWL(0ns 0 1ns 0 1.1ns 1)
M15 VDD WR WRB VDD PMOS l=0.03u w=0.7u
M16 WRB WR VSS VSS NMOS l=0.03u w=0.4u
V6 DATA 0 PWL(0ns 0 .9ns 0 1ns 1)
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 25
.tran 2ns
.ic V(VL) = 0
.ic V(VR) = 1
.backanno
.end
```

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Read Error Log

```
Circuit: * C:\Users\Family\Desktop\Low Power Stage 1\Write\Stage 1 Read.asc

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Direct Newton iteration for .op point succeeded.

Date: Mon Mar 23 22:52:03 2015
Total elapsed time: 0.500 seconds.

tnom = 27
temp = 25
method = modified trap
totiter = 2133
traniter = 2119
tranpoints = 1051
accept = 1051
rejected = 0
matrix size = 82
fillins = 4
solver = Normal
Matrix Compiler1: 10.6 KB object code size  8.0/7.3/[4.0]
Matrix Compiler2: 11.3 KB object code size  4.7/5.9/[3.5]
```

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Read Netlist

```
* C:\Users\Family\Desktop\Low Power Stage 1\Write\Stage 1 Read.asc
M1 VL VR VDD VDD PMOS l=0.03u w=0.7u
M2 VDD VL VR VDD PMOS l=0.03u w=0.7u
M3 VSS VR VL VSS NMOS l=0.03u w=0.4u
M4 VR VL VSS VSS NMOS l=0.03u w=0.4u
V1 VDD 0 1
V2 VSS 0 0
M5 DATA WRB BL VDD PMOS l=0.03u w=0.7u
M6 BL WR DATA VSS NMOS l=0.03u w=0.4u
M7 N001 WRB BLB VDD PMOS l=0.03u w=0.7u
M8 BLB WR N001 VSS NMOS l=0.03u w=0.4u
M9 VDD DATA N001 VDD PMOS l=0.03u w=0.7u
M10 N001 DATA VSS VSS NMOS l=0.03u w=0.4u
M11 VDD PREC BL VDD PMOS l=0.03u w=0.7u
M12 BLB PREC VDD VDD PMOS l=0.03u w=0.7u
M13 VL WL BL VSS NMOS l=0.03u w=0.8u
M14 BLB WL VR VSS NMOS l=0.03u w=0.8u
C1 BL 0 50f
C2 BLB 0 50f
V3 PREC 0 PWL(0ns 0 .9ns 0 1ns 1)
V4 WL 0 PWL(0ns 0 1ns 0 1.1ns 1)
V5 WR 0 0
M15 VDD WR WRB VDD PMOS l=0.03u w=0.7u
M16 WRB WR VSS VSS NMOS l=0.03u w=0.4u
V6 DATA 0 PWL(0ns 0 .9ns 0 1ns 1)
.include 'C:\Users\Family\Documents\models\22nm_lp.file.txt'
.temp 25
.tran 2ns
.ic V(VL) = 0
.ic V(VR) = 1
.backanno
.end
```