Homework #5

Due April 24, 2014

CIS 4930/6930: Low Power VLSI Design

Notes:

1. **The homework will be done and the report must be submitted individually.**
2. **Submit schematics, measurement files, netlist, plot of signals to get full credit**

Voltage scaling is the best knob to reduce the dynamic and leakage power in digital circuits. Unfortunately the minimum voltage at which a functional block (register file, SRAM cache, execution units) performs correctly is different. Therefore a single voltage is not optimal in terms of power. Today's micro-processors employ more than 10 voltage domains for different components. Since these domains talk to each other an intermediate interfacing module called level-shifter or level-converter is needed to convert signals from one voltage domain to the voltage in another domain. This assignment will motivate the need for level-shifters and then provide step-by-step instruction to move to a level-shifter design.

Q1. Consider a scenario when an inverter at 0.7V is driving another inverter at 1V (Fig. 1)
(a) What is the issue in this circuit? Analyze both conditions i.e., primary input is high and low.
(10 Points)
(b) Measure the delay and power consumed in this circuit (both for 0->1 and 1->0 transition)**.**
(10 Points)

Q2. Now consider another circuit (Fig.2) that includes a PMOS circuit which pulls the output of 1st inverter from 0.7V to 1V.
(a) Discuss the advantages and disadvantages as compared to the level shifter circuit in Q1.
(10 Points)
(b) Measure the delay and power consumed in this circuit (both for 0->1 and 1->0 transition)**.**
(10 Points)

Q3. Consider the standard level-shifter circuit (Fig. 3). Use minimum sized inverter (0.7u PMOS and 0.4u NMOS).
(a) Discuss the advantages and disadvantages as compared to the level shifter circuit in Q2.
(10 Points)

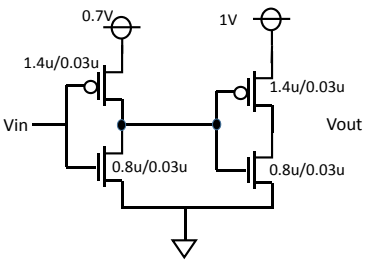

Fig. 1

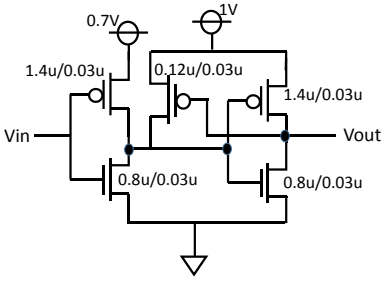

Fig. 2

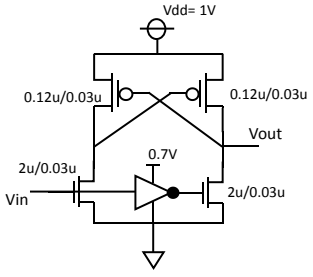

Fig. 3

(b) Measure the delay and power consumed in this circuit (both for 0->1 and 1->0 transition)**.**

(10 Points)

Q4. Read the paper "Design Challenges of Technology Scaling" posted in canvas and answer following questions:

(a) Explain how technology scaling affects the performance, transistor density and power consumption (Be specific and make your point by using equations but don't write thesis).

(b) Explain the impact of technology scaling on interconnects.

(c) Explain the impact of technology scaling on subthreshold leakage. What is the tradeoff to maintain low subthreshold leakage?

(d) Explain the impact of technology scaling on circuit reliability.

(15+7.5+10+7.5)