Homework #3

Due Feb 16, 2015

CIS 4930/6930, Fall 2015

Low Power VLSI Design

Notes:

1. The homework will be done and the report submitted individually.

2. Submit your files in a single zip folder with name_HW3 as folder name.

3. Submit the screenshots of waveforms and Error log files in .png file format

4. Default operating temperature is 25C and Vdd=1V

Perform transistor-level circuit simulations using LTspice of NMOS transistor using 22nm CMOS process technology. Keep channel length= 0.03u for all simulations.

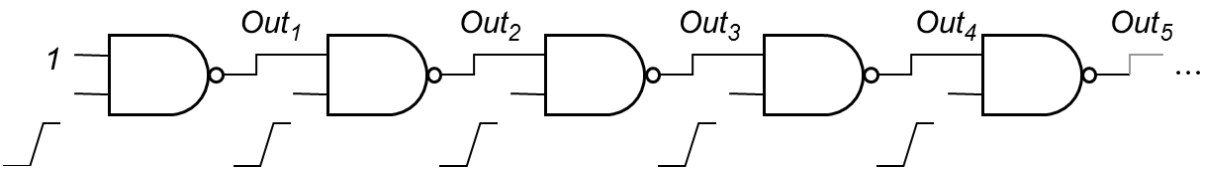
Q1. Draw a chain of NAND gates as shown below in LTspice. The schematic of NAND gate also depicted. Keep the PMOS width=0.7u and NMOS width=0.8u.

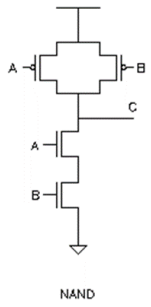
(a) Apply input transitions as shown below simultaneously to all inputs except the top input of first NAND that is fixed to '1'. Plot Out1 to out5. Do you see any problem with the circuit? If so, report your observation.

(b) Measure the power between the beginning of input rising transition and end of out5 transition.

(c) Employ one technique to fix the issue. Show your new schematic, waveform of internal nets and report the new power.

(25+10+25 points)





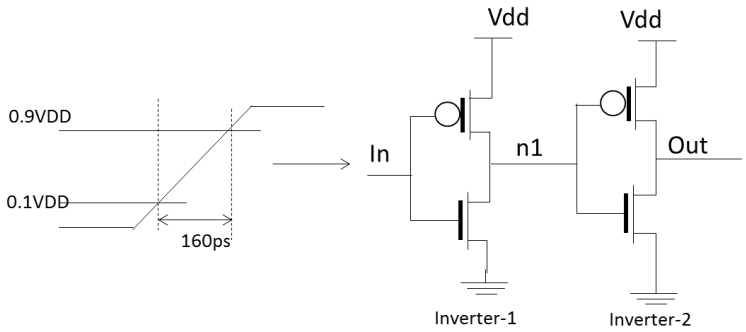
NAND

Q2. Draw two 1X size (PMOS width=0.7u and NMOS width=0.4u) series connected inverters. Apply an input transition with 10% to 90% rise time =160ps to inverter-1. You can use different power supplies for Vdd of inverter-1 and inverter-2.

(a) Plot the current drawn by inverter-1 from the supply during input transition. Do you observe any issue?

(b) Sweep the inverter-2 size (both PMOS and NMOS) by 2X, 4X, 8X, 12X and 16X. Plot the current drawn by inverter-1 from supply during input transition. Did the current magnitude change? If so why?

(10+30 points)



BONUS QUESTION:

In Q2(a), how can you fix the problem? Discuss your approach and simulation results to demonstrate it works.

10 points