Team Low Power Rangers

CIS 4930 Sec 001 Spring 2015

Due: 4/1/2015

Low Power VLSI Project: Stage 2 Report

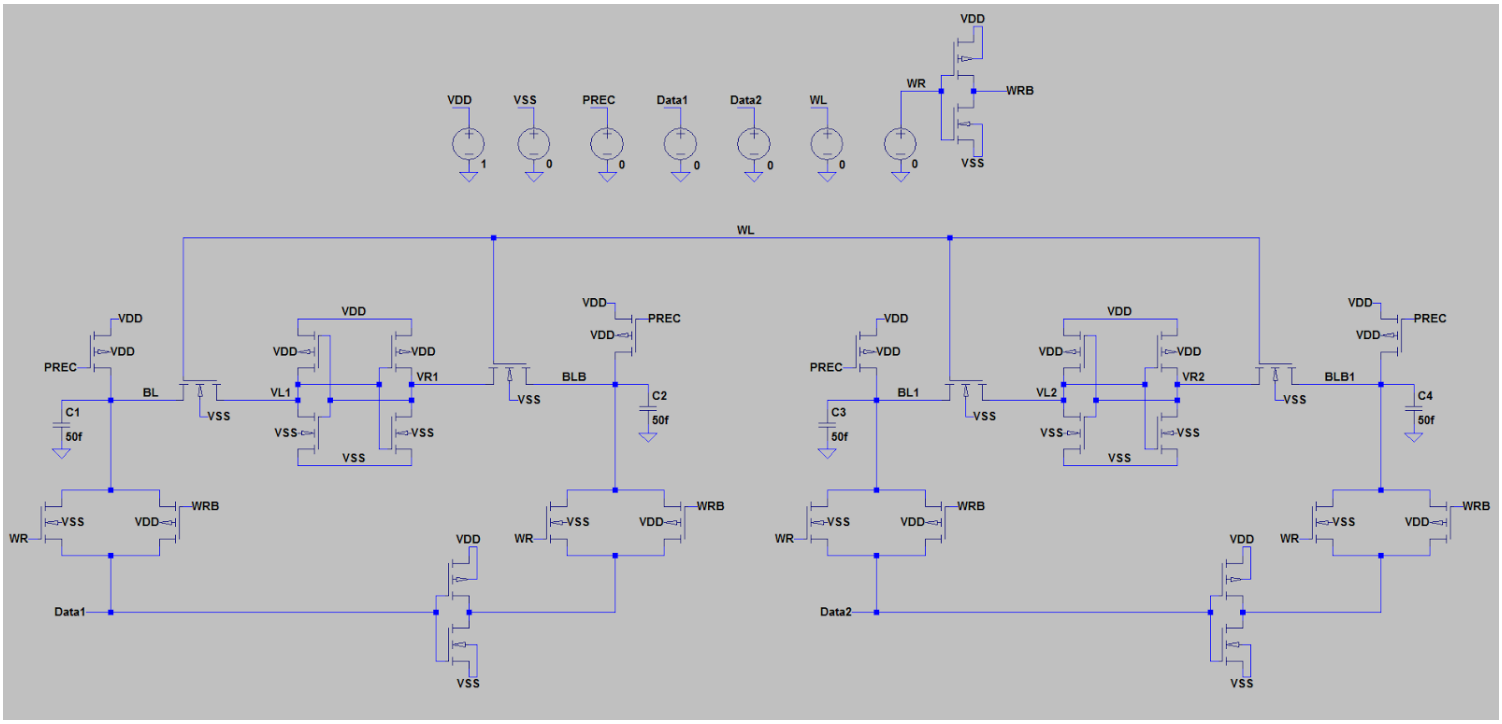
Work Division

Chris Frazier: 33%

Bassam Saed: 33%

John Gangemi: 33%

(**a**) Create 1Kbits of memory as shown in Fig. 2. The SRAM bit on the left hand side provides the load equivalent to 999 SRAM bit cells. Scale Precharge and transmission gate transistors 999 times. Note: increase the width keeping the length minimum 30nm.



(**b**) For the given SRAM memory design use the footer switch to save maximum leakage with less degradation in performance. Use the circuit shown in Fig. 3.

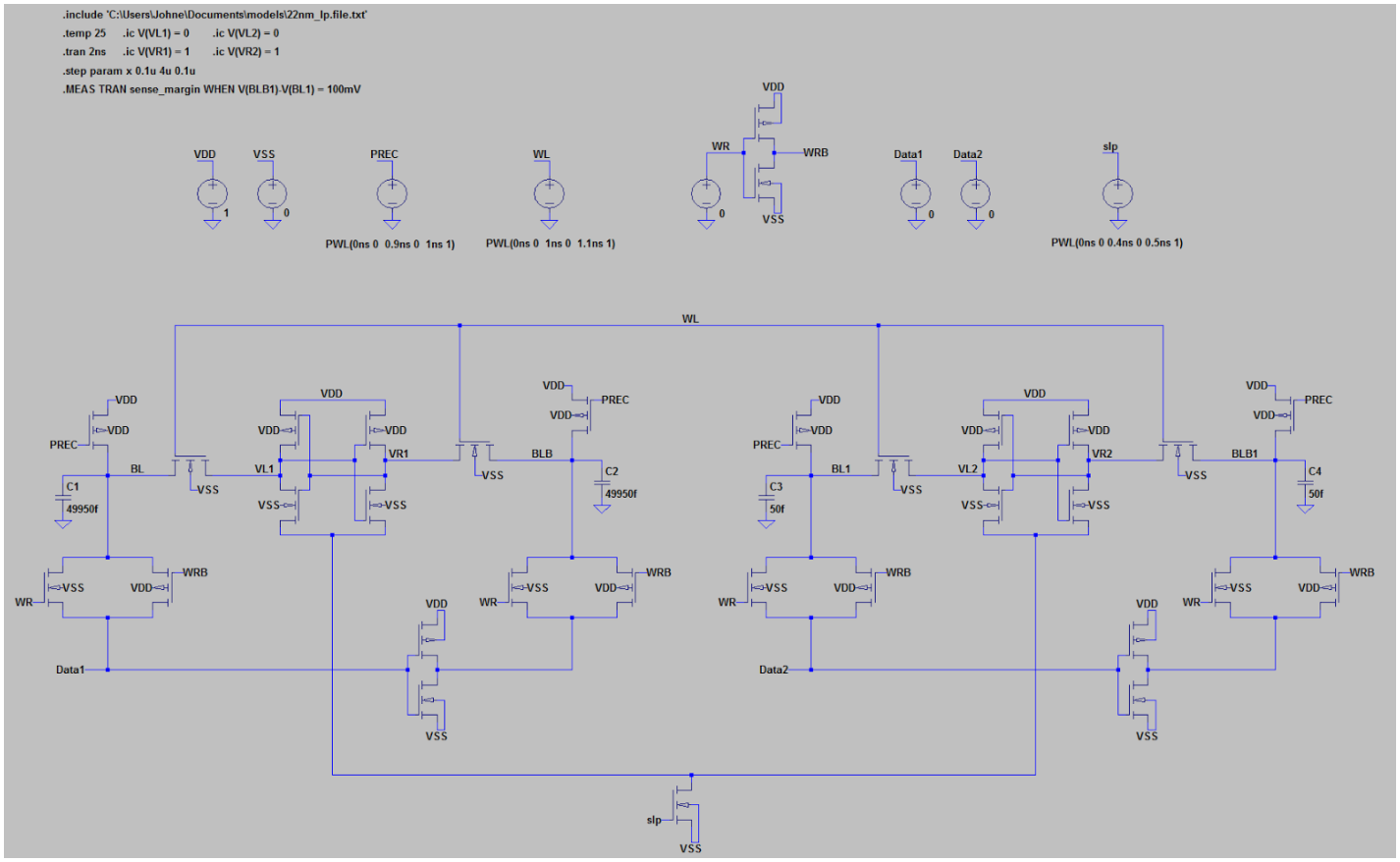
To measure delay:
Turn the footer transistor ON (slp=1).Measure the read delay as the time to develop 100mV sense margin. Measure write delay as the time to write 1/0 to change the state of the bit cell. Plot delay vs sleep transistor size.

To measure leakage:
Keep the footer transistor OFF (slp =0) and keep all the primary inputs disabled. Sweep the footer transistor size in the range of size [0.1u to 4u] in step of 0.1u and measure current drawn from supply. Plot leakage vs sleep transistor size.

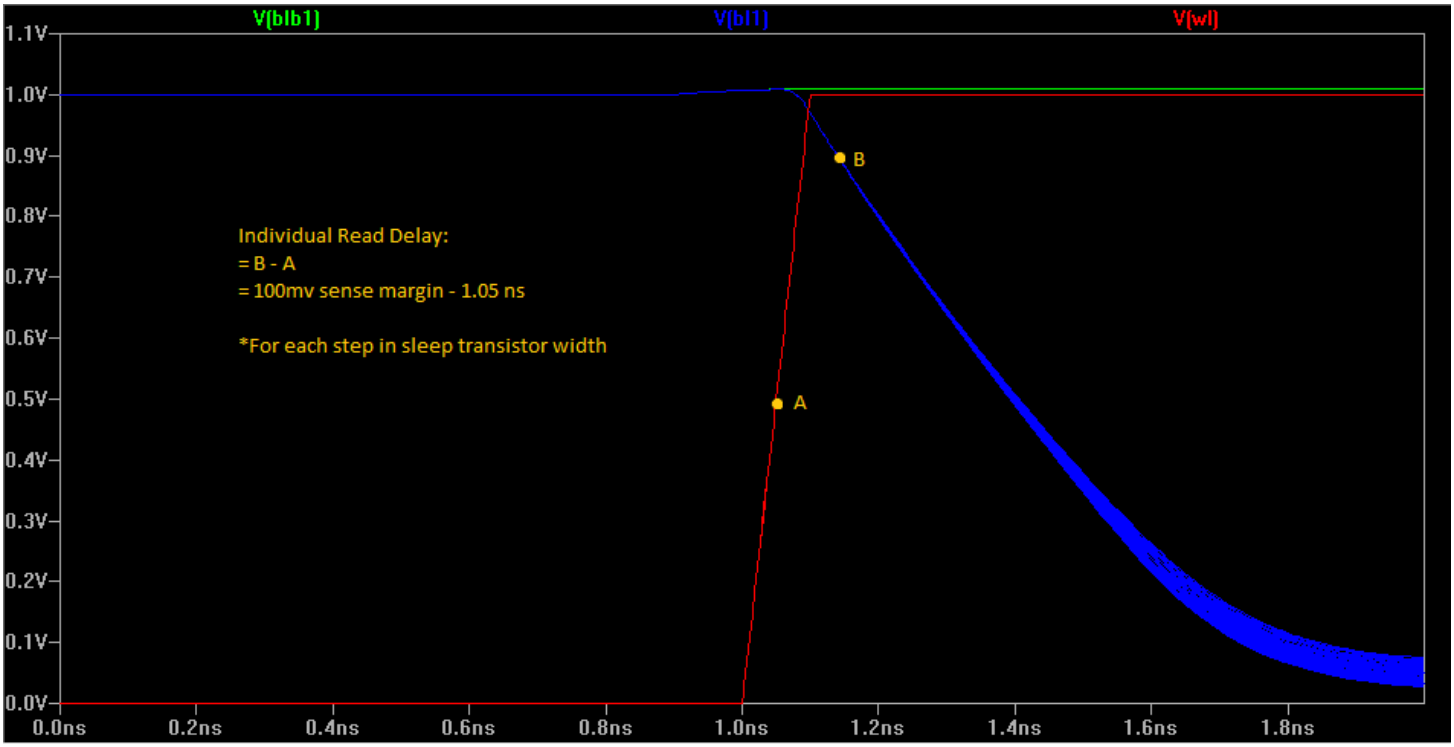
Plot leakage vs delay and determine the optimum transistor size (knee point of the curve).

<u>Read Delay</u>

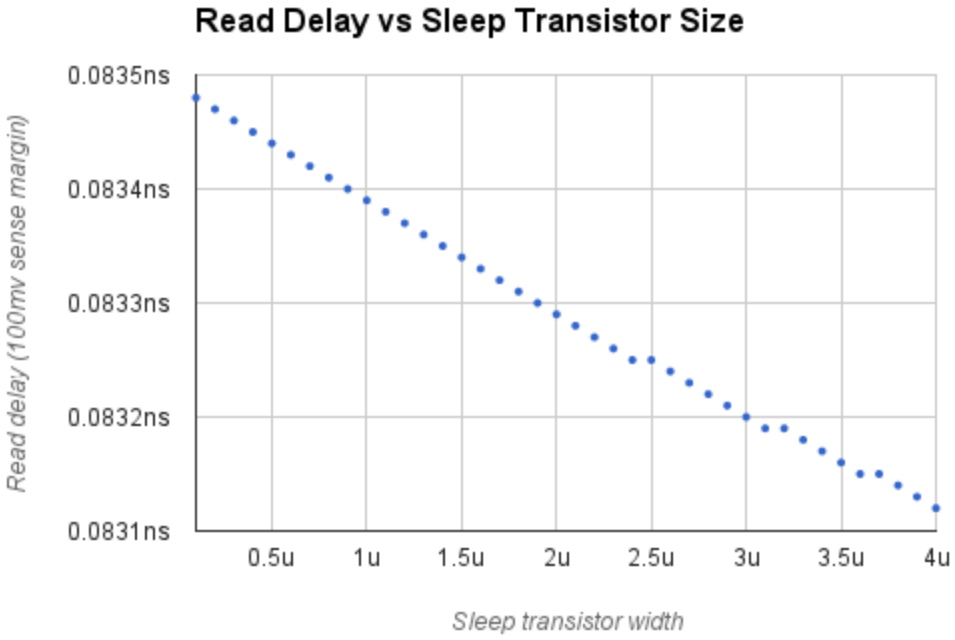
Read Delay Schematic



Read Delay Waveform



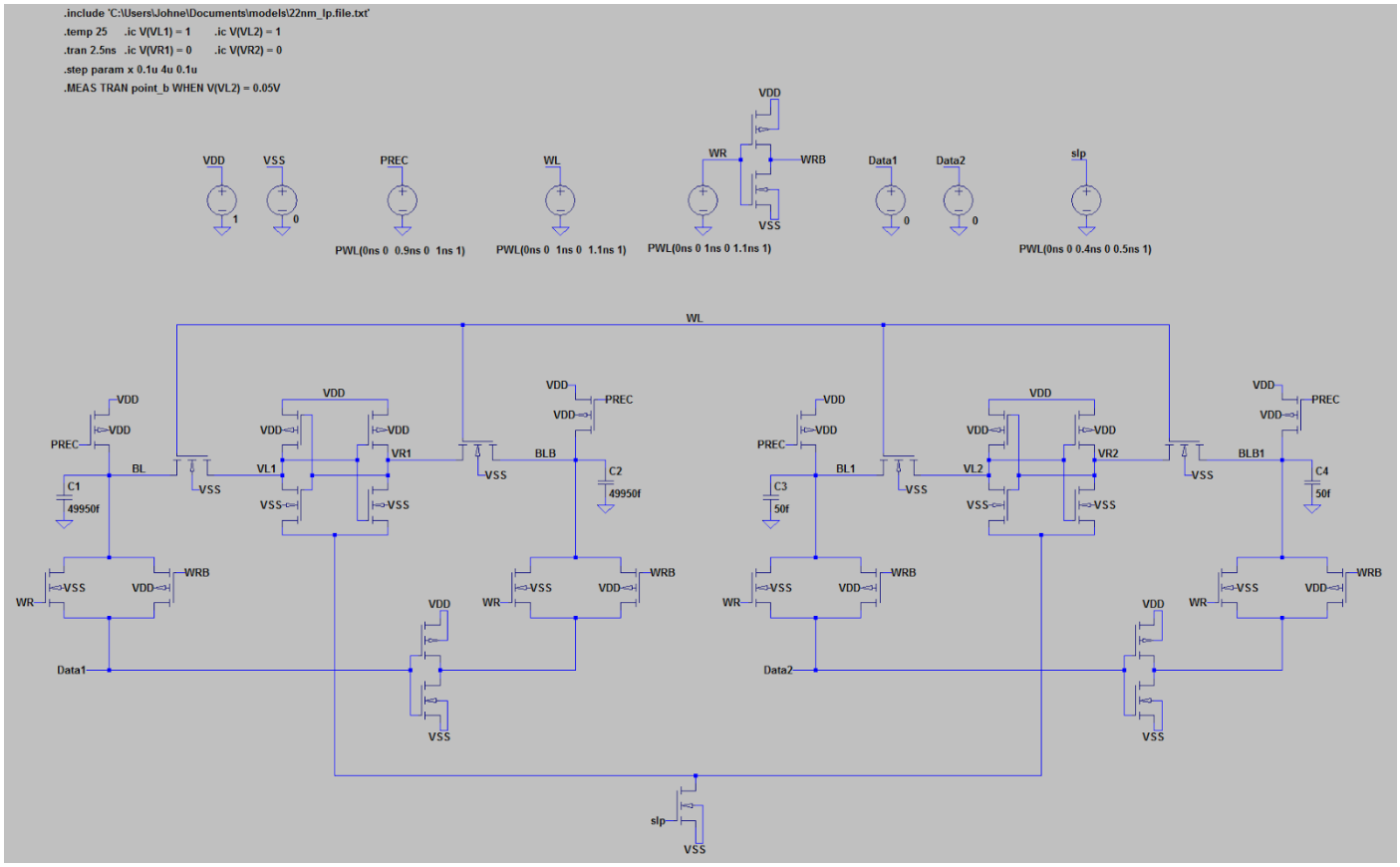
Read Delay Plot



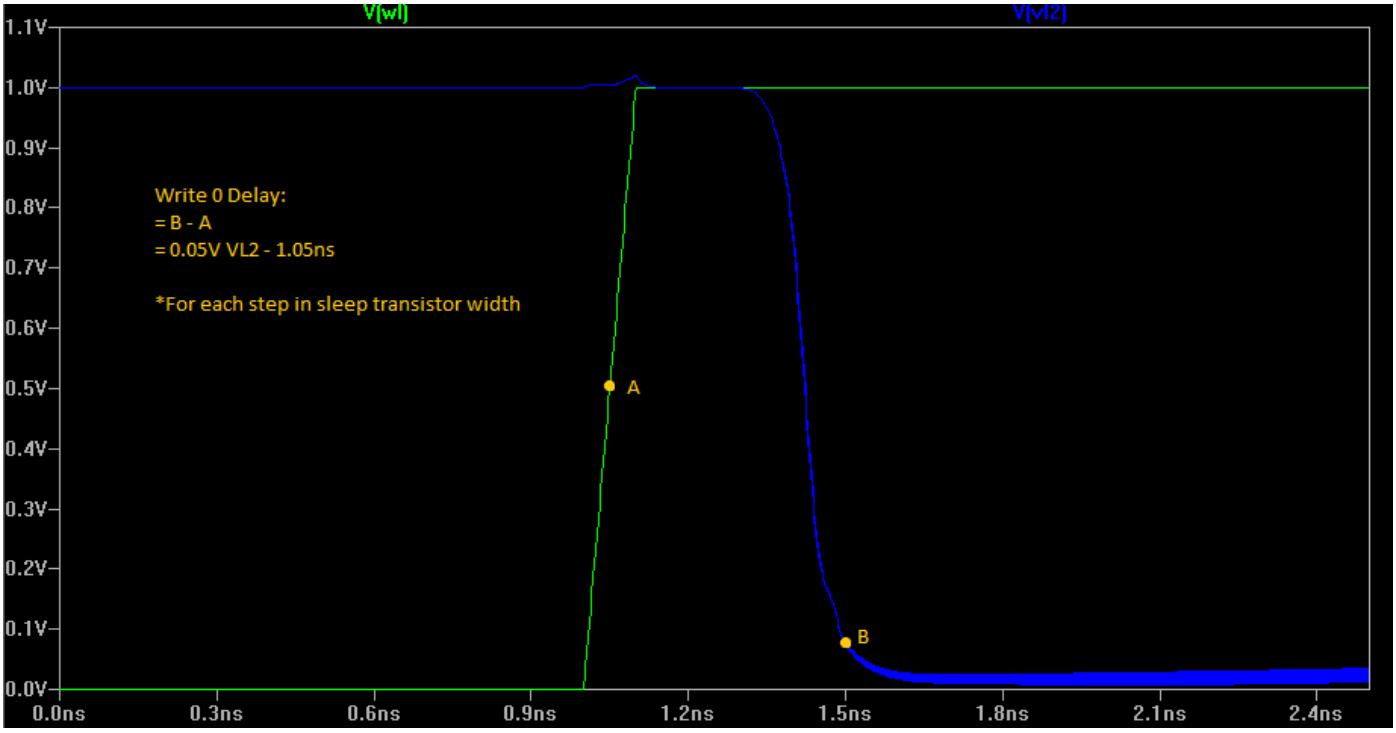
After having analyzed the “read delay” waveform and plot it can be concluded that delay incurred when reading the last 6T SRAM cell of a 1Kbit memory will decrease as the sleep transistor width increases. The reduction in delay is linear and has a negative slope when plotted against sleep transistor width.

Write 0 Delay

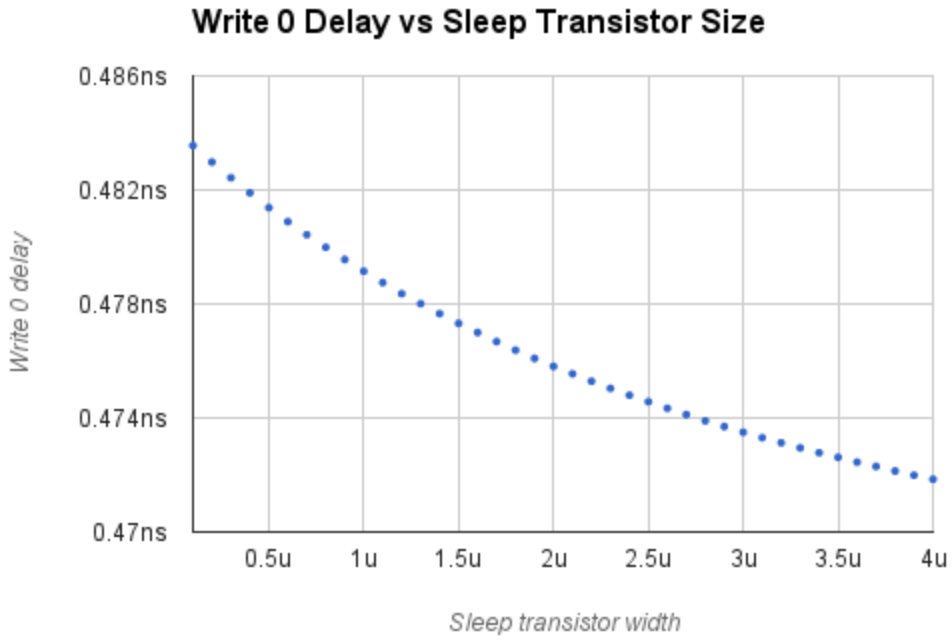
Write 0 Delay Schematic



Write 0 Delay Waveform



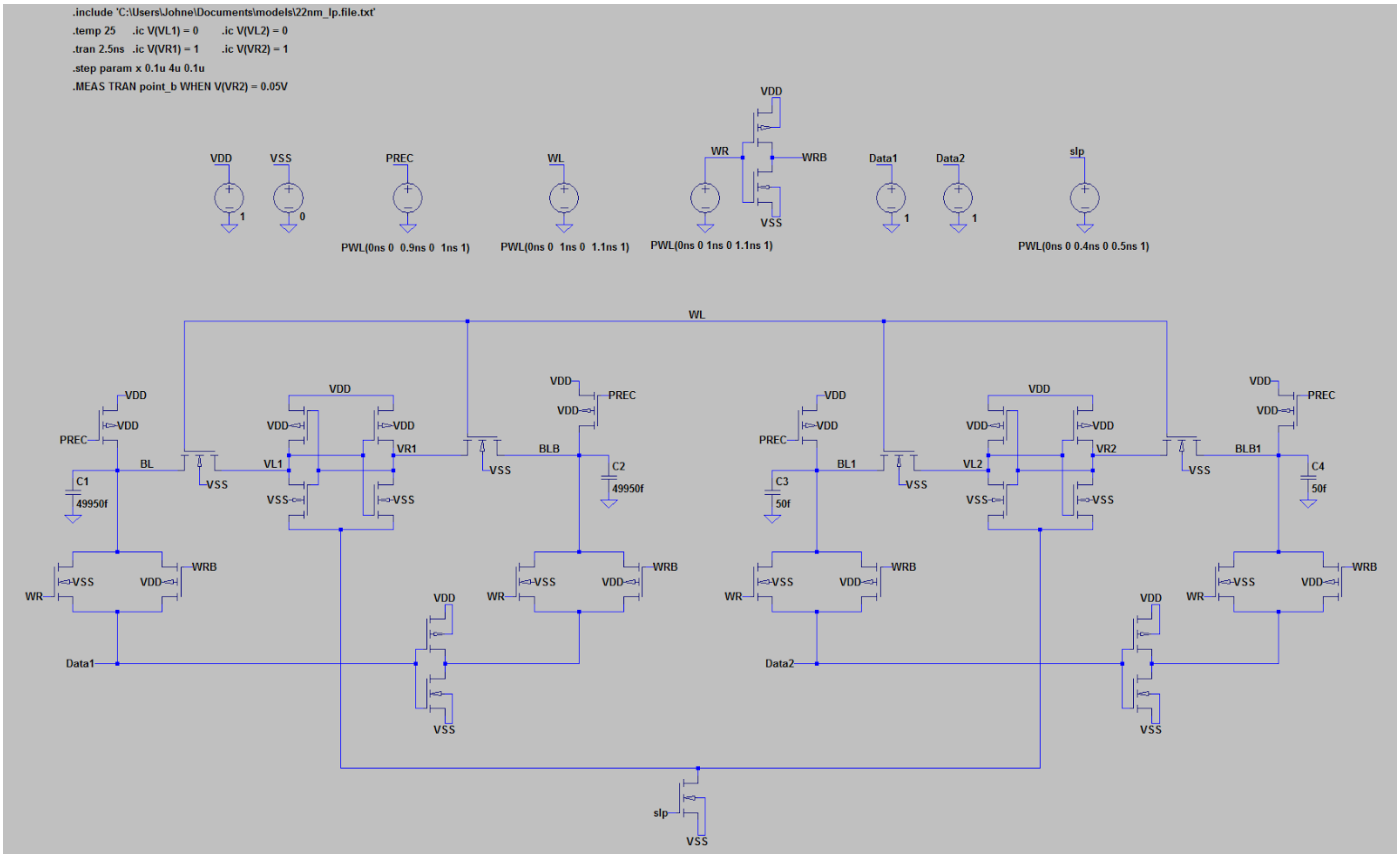
Write 0 Delay Plot



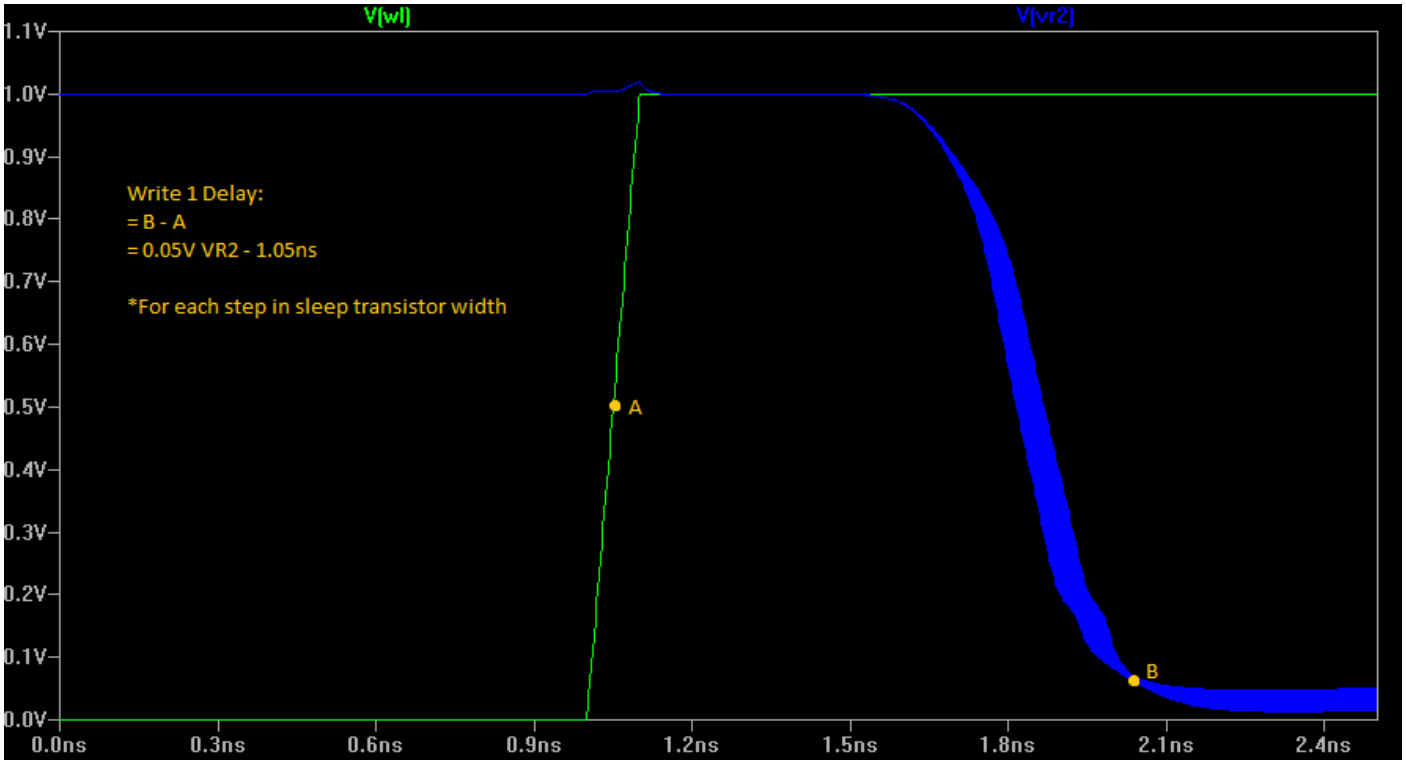
The waveform and plot for “write 0 delay” show a decrease in write delay for the 6T SRAM cell as sleep transistor width is increased.

Write 1 Delay

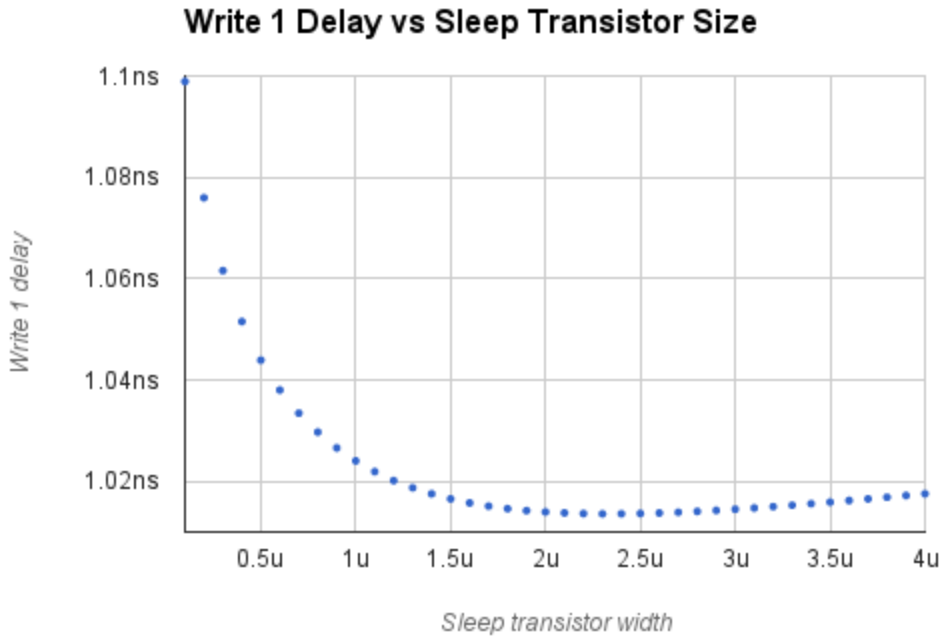
Write 1 Delay Schematic



Write 1 Delay Waveform



Write 1 Delay Plot

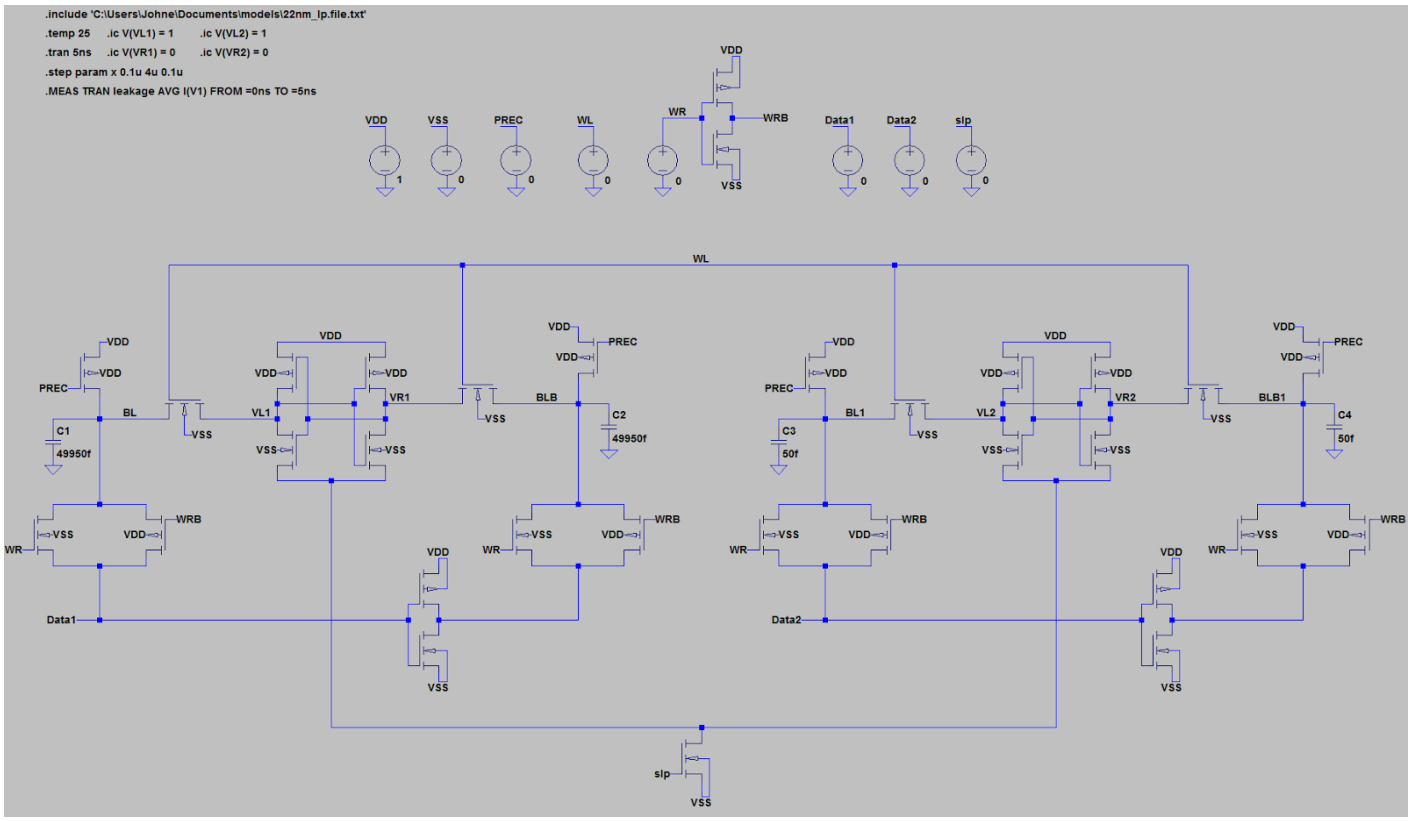


Similar to the “write 0 delay” observations the “write 1 delay” waveform and plot display a decrease in write delay as sleep transistor width is increased. However if you may have noticed that the trend is not linear but rather exponential. It’s interesting that after a sleep transistor width of 2.5 micrometers the write delay begins to increase slightly.

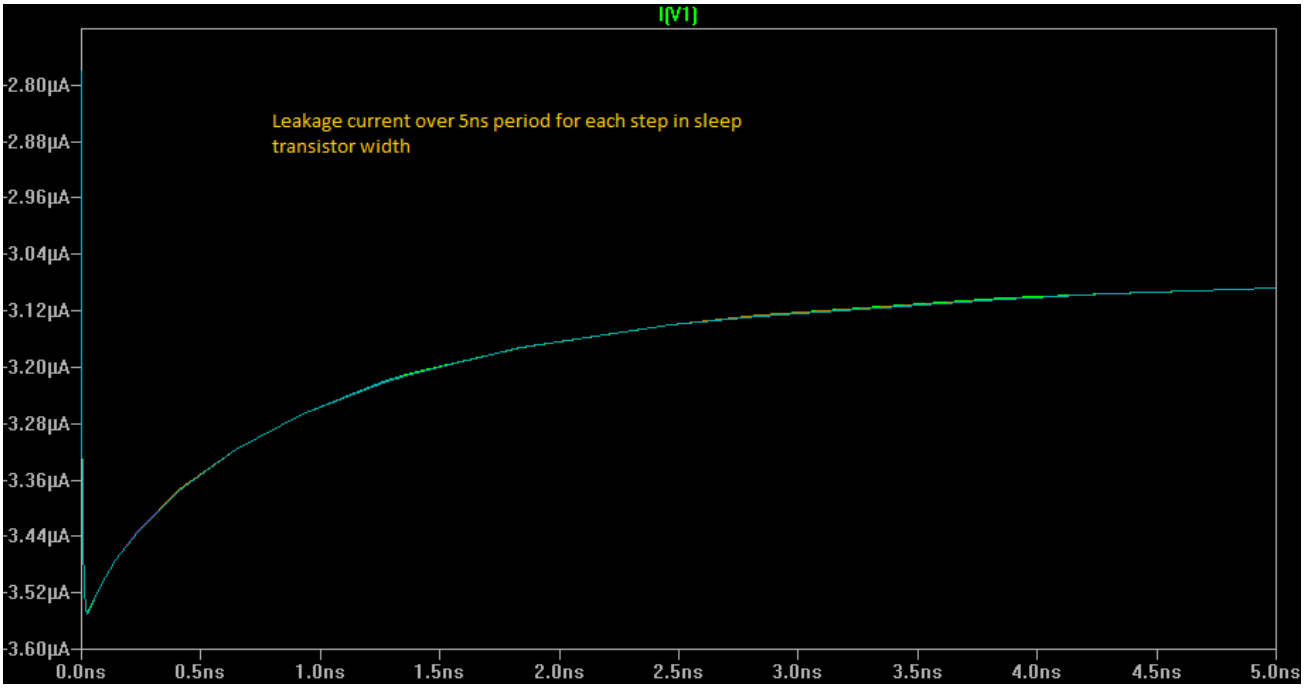
Having observed the influence of sleep transistor width on read and write delay one can conclude that read and write performance favors a larger sleep transistor width.

Leakage Current

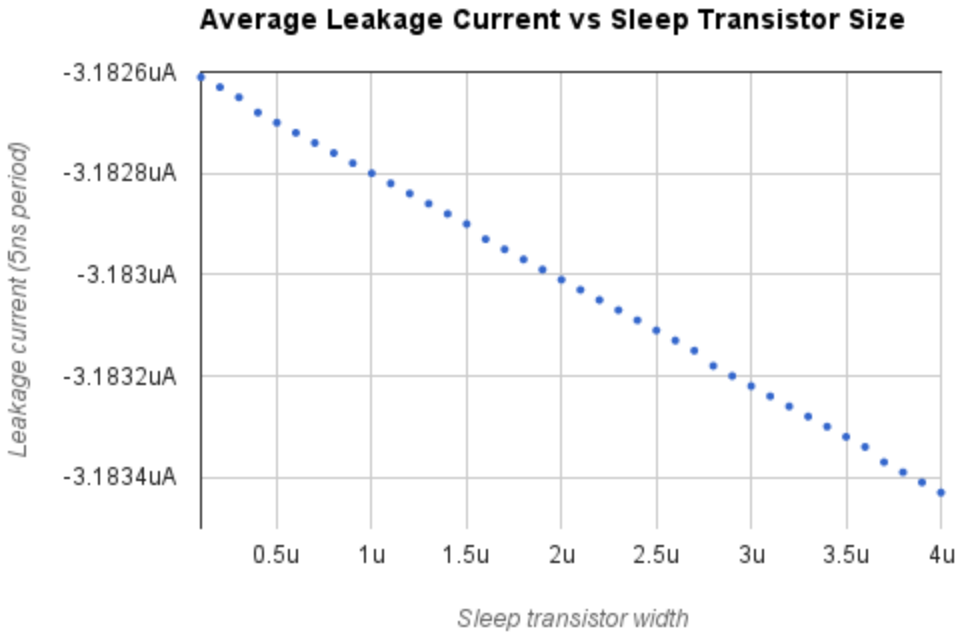
Leakage Current Schematic



Leakage Current Waveform



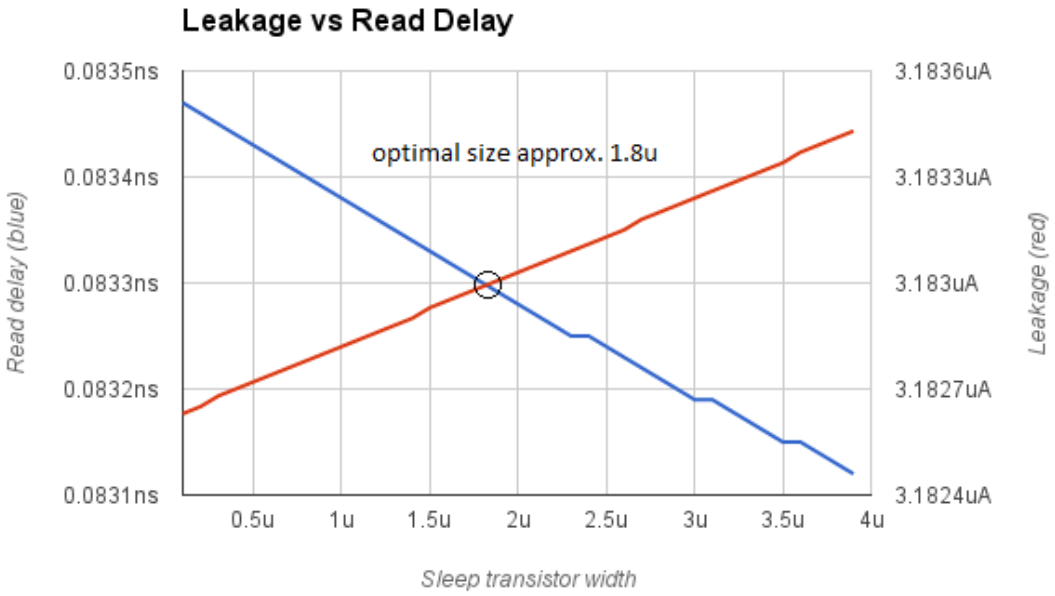
Leakage Current Plot



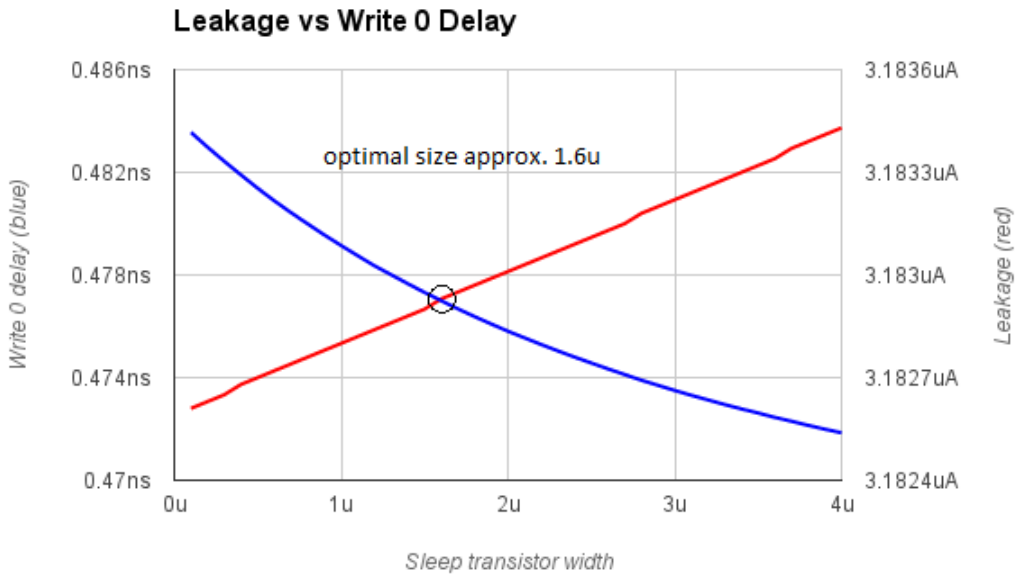
Pertaining to leakage current, an increase in sleep transistor width will increase the amount of wasted current in the 6T SRAM cell. Therefore maximum power saving is realized when the sleep

transistor width is made as small as possible. However, it was observed earlier that a smaller sleep transistor width hinders performance therefore when sizing the sleep transistor width a balance between leakage current and delay must be considered.

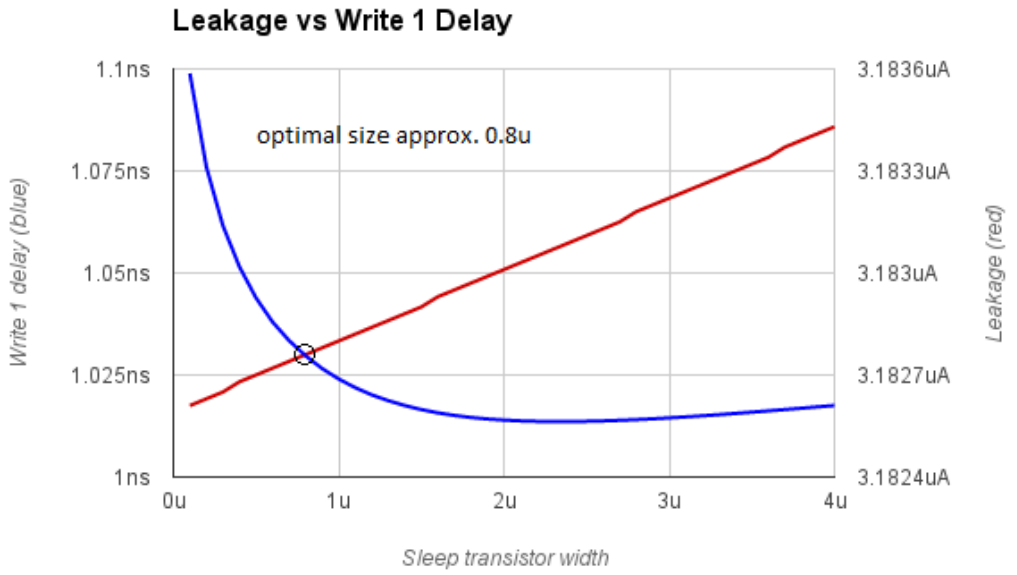
Leakage Current and Read Delay Plot



Leakage Current and Write 0 Delay



Leakage Current and Write 1 Delay



Appendix

Read Delay Netlist

```
* C:\Users\Johne\Documents\Computer Engineering Courses\Spring 201
M1 VL1 VR1 VDD VDD PMOS l=0.03u w=699.3u
M2 VDD VL1 VR1 VDD PMOS l=0.03u w=699.3u
M3 N001 VR1 VL1 VSS NMOS l=0.03u w=399.6u
M4 VR1 VL1 N001 VSS NMOS l=0.03u w=399.6u
V1 VDD 0 1
V2 VSS 0 0
M5 Data1 WRB BL VDD PMOS l=0.03u w=699.3u
M6 BL WR Data1 VSS NMOS l=0.03u w=399.6u
M7 N002 WRB BLB VDD PMOS l=0.03u w=699.3u
M8 BLB WR N002 VSS NMOS l=0.03u w=399.6u
M9 VDD Data1 N002 VDD PMOS l=0.03u w=699.3u
M10 N002 Data1 VSS VSS NMOS l=0.03u w=399.6u
M11 VDD PREC BL VDD PMOS l=0.03u w=699.3u
M12 BLB PREC VDD VDD PMOS l=0.03u w=699.3u
M13 VL1 WL BL VSS NMOS l=0.03u w=799.2u
M14 BLB WL VR1 VSS NMOS l=0.03u w=799.2u
C1 BL 0 49950f
C2 BLB 0 49950f
V3 PREC 0 PWL(0ns 0 0.9ns 0 1ns 1)
V4 WL 0 PWL(0ns 0 1ns 0 1.1ns 1)
V5 WR 0 0
M15 VDD WR WRB VDD PMOS l=0.03u w=0.7u
M16 WRB WR VSS VSS NMOS l=0.03u w=0.4u
V6 Data2 0 0
M17 VL2 VR2 VDD VDD PMOS l=0.03u w=0.7u
M18 VDD VL2 VR2 VDD PMOS l=0.03u w=0.7u
M19 N001 VR2 VL2 VSS NMOS l=0.03u w=0.4u
M20 VR2 VL2 N001 VSS NMOS l=0.03u w=0.4u
M21 Data2 WRB BL1 VDD PMOS l=0.03u w=0.7u
M22 BL1 WR Data2 VSS NMOS l=0.03u w=0.4u
M23 N003 WRB BLB1 VDD PMOS l=0.03u w=0.7u
M24 BLB1 WR N003 VSS NMOS l=0.03u w=0.4u
M25 VDD Data2 N003 VDD PMOS l=0.03u w=0.7u
M26 N003 Data2 VSS VSS NMOS l=0.03u w=0.4u
M27 VDD PREC BL1 VDD PMOS l=0.03u w=0.7u
M28 BLB1 PREC VDD VDD PMOS l=0.03u w=0.7u
M29 VL2 WL BL1 VSS NMOS l=0.03u w=0.8u
M30 BLB1 WL VR2 VSS NMOS l=0.03u w=0.8u
C3 BL1 0 50f
C4 BLB1 0 50f
V7 Data1 0 0
M31 N001 slp VSS VSS NMOS l=0.03u w=x
V8 slp 0 PWL(0ns 0 0.4ns 0 0.5ns 1)
.include 'C:\Users\Johne\Documents\models\22nm_lp.file.txt'
.temp 25
.tran 2ns
.ic V(VL1) = 0
.ic V(VR1) = 1
.ic V(VL2) = 0
.ic V(VR2) = 1
.step param x 0.1u 4u 0.1u
.MEAS TRAN sense_margin WHEN V(BLB1)-V(BL1) = 100mV
.backanno
.end
```

Read Delay Errorlog

```
circuit: * C:\Users\Johne\Documents\Computer Engineering Courses\Spring 2015\Low

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Direct Newton iteration for .op point succeeded.
.step x=1e-007
.step x=2e-007
.step x=3e-007
.step x=4e-007
.step x=5e-007
.step x=6e-007
.step x=7e-007
.step x=8e-007
.step x=9e-007
.step x=1e-006
.step x=1.1e-006
.step x=1.2e-006
.step x=1.3e-006
.step x=1.4e-006
.step x=1.5e-006
.step x=1.6e-006
.step x=1.7e-006
.step x=1.8e-006
.step x=1.9e-006
.step x=2e-006
.step x=2.1e-006
.step x=2.2e-006
.step x=2.3e-006
.step x=2.4e-006
.step x=2.5e-006
.step x=2.6e-006
.step x=2.7e-006
.step x=2.8e-006
.step x=2.9e-006
.step x=3e-006
.step x=3.1e-006
.step x=3.2e-006
.step x=3.3e-006
.step x=3.4e-006
.step x=3.5e-006
.step x=3.6e-006
.step x=3.7e-006
.step x=3.8e-006
.step x=3.9e-006
.step x=4e-006
```

```
Measurement: sense_margin
  step             v(blb1)-v(bl1)=100mv
     1             1.13348e-009
     2             1.13347e-009
     3             1.13346e-009
     4             1.13345e-009
     5             1.13344e-009
     6             1.13343e-009
     7             1.13342e-009
     8             1.13341e-009
     9             1.1334e-009
    10             1.13339e-009
    11             1.13338e-009
    12             1.13337e-009
    13             1.13336e-009
    14             1.13335e-009
    15             1.13334e-009
    16             1.13333e-009
    17             1.13332e-009
    18             1.13331e-009
    19             1.1333e-009
    20             1.13329e-009
    21             1.13328e-009
    22             1.13327e-009
    23             1.13326e-009
    24             1.13325e-009
    25             1.13325e-009
    26             1.13324e-009
    27             1.13323e-009
    28             1.13322e-009
    29             1.13321e-009
    30             1.1332e-009
    31             1.13319e-009
    32             1.13319e-009
    33             1.13318e-009
    34             1.13317e-009
    35             1.13316e-009
    36             1.13315e-009
    37             1.13315e-009
    38             1.13314e-009
    39             1.13313e-009
    40             1.13312e-009


Date: Tue Mar 31 17:27:44 2015
Total elapsed time: 5.677 seconds.

tnom = 27
temp = 25
method = modified trap
totiter = 2138
traniter = 2122
tranpoints = 1057
accept = 1057
rejected = 0
matrix size = 152
fillins = 56
solver = Normal
Thread vector: 97.6/42.8[3] 12.7/4.8[3] 3.8/2.4[3] 1.0/1.3[1]  2592/500
Matrix Compiler1: 32.1 KB object code size  7.5/2.8/[2.1]
Matrix Compiler2:    1618 opcodes  2.4/[2.1]/2.6
```

Write 0 Delay Netlist

```
* C:\Users\Johne\Documents\Computer Engineering Courses\Spring 201
M1 VL1 VR1 VDD VDD PMOS l=0.03u w=699.3u
M2 VDD VL1 VR1 VDD PMOS l=0.03u w=699.3u
M3 N001 VR1 VL1 VSS NMOS l=0.03u w=399.6u
M4 VR1 VL1 N001 VSS NMOS l=0.03u w=399.6u
V1 VDD 0 1
V2 VSS 0 0
M5 Data1 WRB BL VDD PMOS l=0.03u w=699.3u
M6 BL WR Data1 VSS NMOS l=0.03u w=399.6u
M7 N002 WRB BLB VDD PMOS l=0.03u w=699.3u
M8 BLB WR N002 VSS NMOS l=0.03u w=399.6u
M9 VDD Data1 N002 VDD PMOS l=0.03u w=699.3u
M10 N002 Data1 VSS VSS NMOS l=0.03u w=399.6u
M11 VDD PREC BL VDD PMOS l=0.03u w=699.3u
M12 BLB PREC VDD VDD PMOS l=0.03u w=699.3u
M13 VL1 WL BL VSS NMOS l=0.03u w=799.2u
M14 BLB WL VR1 VSS NMOS l=0.03u w=799.2u
C1 BL 0 49950f
C2 BLB 0 49950f
V3 PREC 0 PWL(0ns 0 0.9ns 0 1ns 1)
V4 WL 0 PWL(0ns 0 1ns 0 1.1ns 1)
V5 WR 0 PWL(0ns 0 1ns 0 1.1ns 1)
M15 VDD WR WRB VDD PMOS l=0.03u w=0.7u
M16 WRB WR VSS VSS NMOS l=0.03u w=0.4u
V6 Data2 0 0
M17 VL2 VR2 VDD VDD PMOS l=0.03u w=0.7u
M18 VDD VL2 VR2 VDD PMOS l=0.03u w=0.7u
M19 N001 VR2 VL2 VSS NMOS l=0.03u w=0.4u
M20 VR2 VL2 N001 VSS NMOS l=0.03u w=0.4u
M21 Data2 WRB BL1 VDD PMOS l=0.03u w=0.7u
M22 BL1 WR Data2 VSS NMOS l=0.03u w=0.4u
M23 N003 WRB BLB1 VDD PMOS l=0.03u w=0.7u
M24 BLB1 WR N003 VSS NMOS l=0.03u w=0.4u
M25 VDD Data2 N003 VDD PMOS l=0.03u w=0.7u
M26 N003 Data2 VSS VSS NMOS l=0.03u w=0.4u
M27 VDD PREC BL1 VDD PMOS l=0.03u w=0.7u
M28 BLB1 PREC VDD VDD PMOS l=0.03u w=0.7u
M29 VL2 WL BL1 VSS NMOS l=0.03u w=0.8u
M30 BLB1 WL VR2 VSS NMOS l=0.03u w=0.8u
C3 BL1 0 50f
C4 BLB1 0 50f
V7 Data1 0 0
M31 N001 slp VSS VSS NMOS l=0.03u w=x
V8 slp 0 PWL(0ns 0 0.4ns 0 0.5ns 1)
.include 'C:\Users\Johne\Documents\models\22nm_lp.file.txt'
.temp 25
.tran 2.5ns
.ic V(VL1) = 1
.ic V(VR1) = 0
.ic V(VL2) = 1
.ic V(VR2) = 0
.step param x 0.1u 4u 0.1u
.MEAS TRAN point_b WHEN V(VL2) = 0.05V
.backanno
.end
```

Write 0 Delay Errorlog

```
Circuit: * C:\Users\Johne\Documents\Computer Engineering Courses\Spring 2015\L

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignored.
Direct Newton iteration for .op point succeeded.
.step x=1e-007
.step x=2e-007
.step x=3e-007
.step x=4e-007
.step x=5e-007
.step x=6e-007
.step x=7e-007
.step x=8e-007
.step x=9e-007
.step x=1e-006
.step x=1.1e-006
.step x=1.2e-006
.step x=1.3e-006
.step x=1.4e-006
.step x=1.5e-006
.step x=1.6e-006
.step x=1.7e-006
.step x=1.8e-006
.step x=1.9e-006
.step x=2e-006
.step x=2.1e-006
.step x=2.2e-006
.step x=2.3e-006
.step x=2.4e-006
.step x=2.5e-006
.step x=2.6e-006
.step x=2.7e-006
.step x=2.8e-006
.step x=2.9e-006
.step x=3e-006
.step x=3.1e-006
.step x=3.2e-006
.step x=3.3e-006
.step x=3.4e-006
.step x=3.5e-006
.step x=3.6e-006
.step x=3.7e-006
.step x=3.8e-006
.step x=3.9e-006
.step x=4e-006
```

```
Measurement: point_b
  step             v(vl2)=0.05v
     1             1.53356e-009
     2             1.53298e-009
     3             1.53243e-009
     4             1.5319e-009
     5             1.53138e-009
     6             1.53089e-009
     7             1.53043e-009
     8             1.52999e-009
     9             1.52956e-009
    10             1.52915e-009
    11             1.52875e-009
    12             1.52836e-009
    13             1.52801e-009
    14             1.52766e-009
    15             1.52732e-009
    16             1.527e-009
    17             1.52668e-009
    18             1.52638e-009
    19             1.52609e-009
    20             1.52581e-009
    21             1.52555e-009
    22             1.52529e-009
    23             1.52504e-009
    24             1.5248e-009
    25             1.52457e-009
    26             1.52434e-009
    27             1.52412e-009
    28             1.5239e-009
    29             1.5237e-009
    30             1.5235e-009
    31             1.52331e-009
    32             1.52313e-009
    33             1.52295e-009
    34             1.52278e-009
    35             1.52262e-009
    36             1.52245e-009
    37             1.5223e-009
    38             1.52214e-009
    39             1.52199e-009
    40             1.52185e-009


Date: Tue Mar 31 19:51:25 2015
Total elapsed time: 6.613 seconds.

tnom = 27
temp = 25
method = modified trap
totiter = 2147
traniter = 2133
tranpoints = 1057
accept = 1057
rejected = 0
matrix size = 152
fillins = 57
solver = Normal
Thread vector: 98.4/42.0[3] 12.4/4.7[3] 3.8/2.5[3] 1.0/1.4[1]  2592/500
Matrix Compiler1: 32.7 KB object code size  7.9/2.9/[2.2]
Matrix Compiler2: 21.7 KB object code size  2.4/2.1/[1.4]
```

Write 1 Delay Netlist

```
* C:\Users\Johne\Documents\Computer Engineering Courses\Spring 201
M1 VL1 VR1 VDD VDD PMOS l=0.03u w=699.3u
M2 VDD VL1 VR1 VDD PMOS l=0.03u w=699.3u
M3 N001 VR1 VL1 VSS NMOS l=0.03u w=399.6u
M4 VR1 VL1 N001 VSS NMOS l=0.03u w=399.6u
V1 VDD 0 1
V2 VSS 0 0
M5 Data1 WRB BL VDD PMOS l=0.03u w=699.3u
M6 BL WR Data1 VSS NMOS l=0.03u w=399.6u
M7 N002 WRB BLB VDD PMOS l=0.03u w=699.3u
M8 BLB WR N002 VSS NMOS l=0.03u w=399.6u
M9 VDD Data1 N002 VDD PMOS l=0.03u w=699.3u
M10 N002 Data1 VSS VSS NMOS l=0.03u w=399.6u
M11 VDD PREC BL VDD PMOS l=0.03u w=699.3u
M12 BLB PREC VDD VDD PMOS l=0.03u w=699.3u
M13 VL1 WL BL VSS NMOS l=0.03u w=799.2u
M14 BLB WL VR1 VSS NMOS l=0.03u w=799.2u
C1 BL 0 49950f
C2 BLB 0 49950f
V3 PREC 0 PWL(0ns 0 0.9ns 0 1ns 1)
V4 WL 0 PWL(0ns 0 1ns 0 1.1ns 1)
V5 WR 0 PWL(0ns 0 1ns 0 1.1ns 1)
M15 VDD WR WRB VDD PMOS l=0.03u w=0.7u
M16 WRB WR VSS VSS NMOS l=0.03u w=0.4u
V6 Data2 0 1
M17 VL2 VR2 VDD VDD PMOS l=0.03u w=0.7u
M18 VDD VL2 VR2 VDD PMOS l=0.03u w=0.7u
M19 N001 VR2 VL2 VSS NMOS l=0.03u w=0.4u
M20 VR2 VL2 N001 VSS NMOS l=0.03u w=0.4u
M21 Data2 WRB BL1 VDD PMOS l=0.03u w=0.7u
M22 BL1 WR Data2 VSS NMOS l=0.03u w=0.4u
M23 N003 WRB BLB1 VDD PMOS l=0.03u w=0.7u
M24 BLB1 WR N003 VSS NMOS l=0.03u w=0.4u
M25 VDD Data2 N003 VDD PMOS l=0.03u w=0.7u
M26 N003 Data2 VSS VSS NMOS l=0.03u w=0.4u
M27 VDD PREC BL1 VDD PMOS l=0.03u w=0.7u
M28 BLB1 PREC VDD VDD PMOS l=0.03u w=0.7u
M29 VL2 WL BL1 VSS NMOS l=0.03u w=0.8u
M30 BLB1 WL VR2 VSS NMOS l=0.03u w=0.8u
C3 BL1 0 50f
C4 BLB1 0 50f
V7 Data1 0 1
M31 N001 slp VSS VSS NMOS l=0.03u w=x
V8 slp 0 PWL(0ns 0 0.4ns 0 0.5ns 1)
.include 'C:\Users\Johne\Documents\models\22nm_lp.file.txt'
.temp 25
.tran 2.5ns
.ic V(VL1) = 0
.ic V(VR1) = 1
.ic V(VL2) = 0
.ic V(VR2) = 1
.step param x 0.1u 4u 0.1u
.MEAS TRAN point_b WHEN V(VR2) = 0.05V
.backanno
.end
```

Write 1 Delay Errorlog

```
Circuit: * C:\Users\Johne\Documents\Computer Engineering Courses\Spring 201

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignore
Direct Newton iteration for .op point succeeded.
.step x=1e-007
.step x=2e-007
.step x=3e-007
.step x=4e-007
.step x=5e-007
.step x=6e-007
.step x=7e-007
.step x=8e-007
.step x=9e-007
.step x=1e-006
.step x=1.1e-006
.step x=1.2e-006
.step x=1.3e-006
.step x=1.4e-006
.step x=1.5e-006
.step x=1.6e-006
.step x=1.7e-006
.step x=1.8e-006
.step x=1.9e-006
.step x=2e-006
.step x=2.1e-006
.step x=2.2e-006
.step x=2.3e-006
.step x=2.4e-006
.step x=2.5e-006
.step x=2.6e-006
.step x=2.7e-006
.step x=2.8e-006
.step x=2.9e-006
.step x=3e-006
.step x=3.1e-006
.step x=3.2e-006
.step x=3.3e-006
.step x=3.4e-006
.step x=3.5e-006
.step x=3.6e-006
.step x=3.7e-006
.step x=3.8e-006
.step x=3.9e-006
.step x=4e-006
```

Measurement: point_b

step	v(vr2)=0.05v
1	2.14891e-009
2	2.12596e-009
3	2.11158e-009
4	2.10153e-009
5	2.09391e-009
6	2.08801e-009
7	2.08345e-009
8	2.07971e-009
9	2.07659e-009
10	2.07404e-009
11	2.07191e-009
12	2.07014e-009
13	2.06872e-009
14	2.06753e-009
15	2.06653e-009
16	2.06573e-009
17	2.0651e-009
18	2.0646e-009
19	2.06422e-009
20	2.06395e-009
21	2.06376e-009
22	2.06364e-009
23	2.06358e-009
24	2.06359e-009
25	2.06365e-009
26	2.06375e-009
27	2.06389e-009
28	2.06406e-009
29	2.06426e-009
30	2.06449e-009
31	2.06474e-009
32	2.065e-009
33	2.06528e-009
34	2.06558e-009
35	2.06589e-009
36	2.06621e-009
37	2.06653e-009
38	2.06686e-009
39	2.0672e-009
40	2.06753e-009

Date: Tue Mar 31 19:11:20 2015
Total elapsed time: 6.432 seconds.

tnom = 27
temp = 25
method = modified trap
totiter = 2141
traniter = 2123
tranpoints = 1057
accept = 1057
rejected = 0
matrix size = 152
fillins = 70
solver = Normal
Thread vector: 95.8/48.2[3] 14.2/5.3[3] 5.1/1.7[3] 1.0/1.4[1] 2592/500
Matrix Compiler1:   1841 opcodes 9.3/3.6/[3.3]
Matrix Compiler2: 21.9 KB object code size 3.1/2.8/[1.4]

Leakage Current Netlist

```
* C:\Users\Johne\Documents\Computer Engineering Courses\Spring 201
M1 VL1 VR1 VDD VDD PMOS l=0.03u w=699.3u
M2 VDD VL1 VR1 VDD PMOS l=0.03u w=699.3u
M3 N001 VR1 VL1 VSS NMOS l=0.03u w=399.6u
M4 VR1 VL1 N001 VSS NMOS l=0.03u w=399.6u
V1 VDD 0 1
V2 VSS 0 0
M5 Data1 WRB BL VDD PMOS l=0.03u w=699.3u
M6 BL WR Data1 VSS NMOS l=0.03u w=399.6u
M7 N002 WRB BLB VDD PMOS l=0.03u w=699.3u
M8 BLB WR N002 VSS NMOS l=0.03u w=399.6u
M9 VDD Data1 N002 VDD PMOS l=0.03u w=699.3u
M10 N002 Data1 VSS VSS NMOS l=0.03u w=399.6u
M11 VDD PREC BL VDD PMOS l=0.03u w=699.3u
M12 BLB PREC VDD VDD PMOS l=0.03u w=699.3u
M13 VL1 WL BL VSS NMOS l=0.03u w=799.2u
M14 BLB WL VR1 VSS NMOS l=0.03u w=799.2u
C1 BL 0 49950f
C2 BLB 0 49950f
V3 PREC 0 0
V4 WL 0 0
V5 WR 0 0
M15 VDD WR WRB VDD PMOS l=0.03u w=0.7u
M16 WRB WR VSS VSS NMOS l=0.03u w=0.4u
V6 Data2 0 0
M17 VL2 VR2 VDD VDD PMOS l=0.03u w=0.7u
M18 VDD VL2 VR2 VDD PMOS l=0.03u w=0.7u
M19 N001 VR2 VL2 VSS NMOS l=0.03u w=0.4u
M20 VR2 VL2 N001 VSS NMOS l=0.03u w=0.4u
M21 Data2 WRB BL1 VDD PMOS l=0.03u w=0.7u
M22 BL1 WR Data2 VSS NMOS l=0.03u w=0.4u
M23 N003 WRB BLB1 VDD PMOS l=0.03u w=0.7u
M24 BLB1 WR N003 VSS NMOS l=0.03u w=0.4u
M25 VDD Data2 N003 VDD PMOS l=0.03u w=0.7u
M26 N003 Data2 VSS VSS NMOS l=0.03u w=0.4u
M27 VDD PREC BL1 VDD PMOS l=0.03u w=0.7u
M28 BLB1 PREC VDD VDD PMOS l=0.03u w=0.7u
M29 VL2 WL BL1 VSS NMOS l=0.03u w=0.8u
M30 BLB1 WL VR2 VSS NMOS l=0.03u w=0.8u
C3 BL1 0 50f
C4 BLB1 0 50f
V7 Data1 0 0
M31 N001 slp VSS VSS NMOS l=0.03u w=x
V8 slp 0 0
.include 'C:\Users\Johne\Documents\models\22nm_lp.file.txt'
.temp 25
.tran 5ns
.ic V(VL1) = 1
.ic V(VR1) = 0
.ic V(VL2) = 1
.ic V(VR2) = 0
.step param x 0.1u 4u 0.1u
.MEAS TRAN leakage AVG I(V1) FROM =0ns TO =5ns
.backanno
.end
```

Leakage Current Errorlog

```
Circuit: * C:\Users\Johne\Documents\Computer Engineering Courses\Spring 201

Warning: toxe, toxp and dtox all given and toxe != toxp + dtox; dtox ignore
Direct Newton iteration for .op point succeeded.
.step x=1e-007
.step x=2e-007
.step x=3e-007
.step x=4e-007
.step x=5e-007
.step x=6e-007
.step x=7e-007
.step x=8e-007
.step x=9e-007
.step x=1e-006
.step x=1.1e-006
.step x=1.2e-006
.step x=1.3e-006
.step x=1.4e-006
.step x=1.5e-006
.step x=1.6e-006
.step x=1.7e-006
.step x=1.8e-006
.step x=1.9e-006
.step x=2e-006
.step x=2.1e-006
.step x=2.2e-006
.step x=2.3e-006
.step x=2.4e-006
.step x=2.5e-006
.step x=2.6e-006
.step x=2.7e-006
.step x=2.8e-006
.step x=2.9e-006
.step x=3e-006
.step x=3.1e-006
.step x=3.2e-006
.step x=3.3e-006
.step x=3.4e-006
.step x=3.5e-006
.step x=3.6e-006
.step x=3.7e-006
.step x=3.8e-006
.step x=3.9e-006
.step x=4e-006
```

Measurement: leakage

step	AVG(i(v1))	FROM	TO
1	-3.18261e-006	0	5e-009
2	-3.18263e-006	0	5e-009
3	-3.18265e-006	0	5e-009
4	-3.18268e-006	0	5e-009
5	-3.1827e-006	0	5e-009
6	-3.18272e-006	0	5e-009
7	-3.18274e-006	0	5e-009
8	-3.18276e-006	0	5e-009
9	-3.18278e-006	0	5e-009
10	-3.1828e-006	0	5e-009
11	-3.18282e-006	0	5e-009
12	-3.18284e-006	0	5e-009
13	-3.18286e-006	0	5e-009
14	-3.18288e-006	0	5e-009
15	-3.1829e-006	0	5e-009
16	-3.18293e-006	0	5e-009
17	-3.18295e-006	0	5e-009
18	-3.18297e-006	0	5e-009
19	-3.18299e-006	0	5e-009
20	-3.18301e-006	0	5e-009
21	-3.18303e-006	0	5e-009
22	-3.18305e-006	0	5e-009
23	-3.18307e-006	0	5e-009
24	-3.18309e-006	0	5e-009
25	-3.18311e-006	0	5e-009
26	-3.18313e-006	0	5e-009
27	-3.18315e-006	0	5e-009
28	-3.18318e-006	0	5e-009
29	-3.1832e-006	0	5e-009
30	-3.18322e-006	0	5e-009
31	-3.18324e-006	0	5e-009
32	-3.18326e-006	0	5e-009
33	-3.18328e-006	0	5e-009
34	-3.1833e-006	0	5e-009
35	-3.18332e-006	0	5e-009
36	-3.18334e-006	0	5e-009
37	-3.18337e-006	0	5e-009
38	-3.18339e-006	0	5e-009
39	-3.18341e-006	0	5e-009
40	-3.18343e-006	0	5e-009

Date: Tue Mar 31 21:53:09 2015
Total elapsed time: 6.930 seconds.

tnom = 27
temp = 25
method = modified trap
totiter = 2097
traniter = 2083
tranpoints = 1042
accept = 1042
rejected = 0
matrix size = 152
fillins = 52
solver = Normal
Thread vector: 98.2/43.5[3] 12.3/4.4[3] 3.7/2.0[3] 1.0/1.4[1] 2592/500
Matrix Compiler1: 30.8 KB object code size 7.5/2.7/[2.0]
Matrix Compiler2: 21.8 KB object code size 2.3/2.1/[1.4]