

CDA 3201 Computer Logic Design

Homework 1

Due to: Tuesday 06/09/2014

Complete all of the following problems clearly showing all intermediate steps – *calculators with number conversion functions should not be used. Turning in assignments in class in hard copy format.*

Part A: Number Representation, Base Conversions, and Basic Logic Design

1.1 (4 pt.) Convert the following numbers to base 10:

a) $(00101110)_2$

b) $(1001)_8$

c) $(CDA)_{16}$

1.2 (4 pt.) Convert the following numbers from decimal to target base

a) 65 to base 2

b) 255 to base 8

c) 3201 to base 16

1.3 (4 pt.) Convert from Base 2 to Base 16:

$(1111101100010100110)_2$

1.4 (4 pt.) Convert from Base 16 to Base 2:

$(ADC)_{16}$

1.5 (4 pt.) Convert from Base 8 to Base 16:

$(21024)_8$

1.6 (4 pt.) Convert from Base 16 to Base 3:

$(123)_{16}$

1.7 (4 pt.) Addition/Subtraction in Different Bases

a) $(20)_5 - (14)_5 = (xxx)_5$

b) $(A13)_{16} + (201)_8 = (xxx)_{16}$

c) $(77)_{10} + (110)_3 = (xxx)_3$

1.8 (4 pt.) Sign-Magnitude Representation in 7 bits:

-33

1.9 (4 pt.) Ones complement representation:

-30

1.10 (4 pt.) Twos complement representation:

-30

1.11 (4 pt.) Compute arithmetic operations in two's complement representation

- a) $-5 + 0$
- b) $-7 + 20$
- c) $30 + -9$

1.12 (4 pt.) Add following numbers in binary-coded decimal (BCD) representation:

$\square (1001\ 0111)_{BCD} + (0101\ 1001)_{BCD}$

2. (4 pts.) How long does it take to charge a gate input from 0 to 4.7 V through a switch to 5 V with a resistance of $1K\Omega$ and a capacitance of 350 nF?

3. (8 pts.) Show the arrangement of transistors needed to construct the following gates:

- a) 2-input XOR
- b) 2-input AND
- c) $Z = AB + CD$
- d) $Z = (A + B) CD$

5. (8 pts.) Design a digital system that inputs a 4-bit number (assume input in parallel) and determines whether the number is a multiple of 4.

Part B: Combinational Logics

Total Points: 40 point

1. Draw the schematic for the following functions using NOR gates only: (5 points)

a. $x \cdot y + z'$

b. $xy + xz'$

2. Draw the schematic for the following functions using NAND gates only: (5 points)

a. $x \cdot y + z'$

b. $xy + xz'$

3. Exercise: 2.22 (only part a to d) (12 points)

4. Determine the minimized realization of the following functions in the sum-of-products form: (5 points)

a. $f(a, b, c, d) = \sum m(1, 7, 11, 13) + \sum d(0, 5, 10, 15)$

b. $f(a, b, c, d) = \prod M(2, 5, 6, 8, 9, 10) * \prod D(4, 11, 12)$

5. Use K-Maps to derive minimum expressions for the functions for C_0 and C_4 in Figure 2.33 from textbook. (5 points)

6. Derive the Boolean expressions for 2-bit Adder. Each output bit should be represented by a different Boolean expression. (8 points)