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VLSI Design Automation, Summer C 2015
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Homework 1

1. **In your own words, define Design Automation. Why is Design Automation important?**

   Design Automation is the utilization of computers to completely automate the tasks/procedures associated with VLSI design of sophisticated and complex circuits for which a human implementation would increase design time and errors.

   Design Automation has become increasingly more important due to the increased complexity of silicon chips. With the growth of the number of transistors on a single silicon chip increasing every 18 months the industry must adapt accordingly which leads to the automation of designs.

2. **What is High-Level Synthesis? How does it relate to Design Automation?**

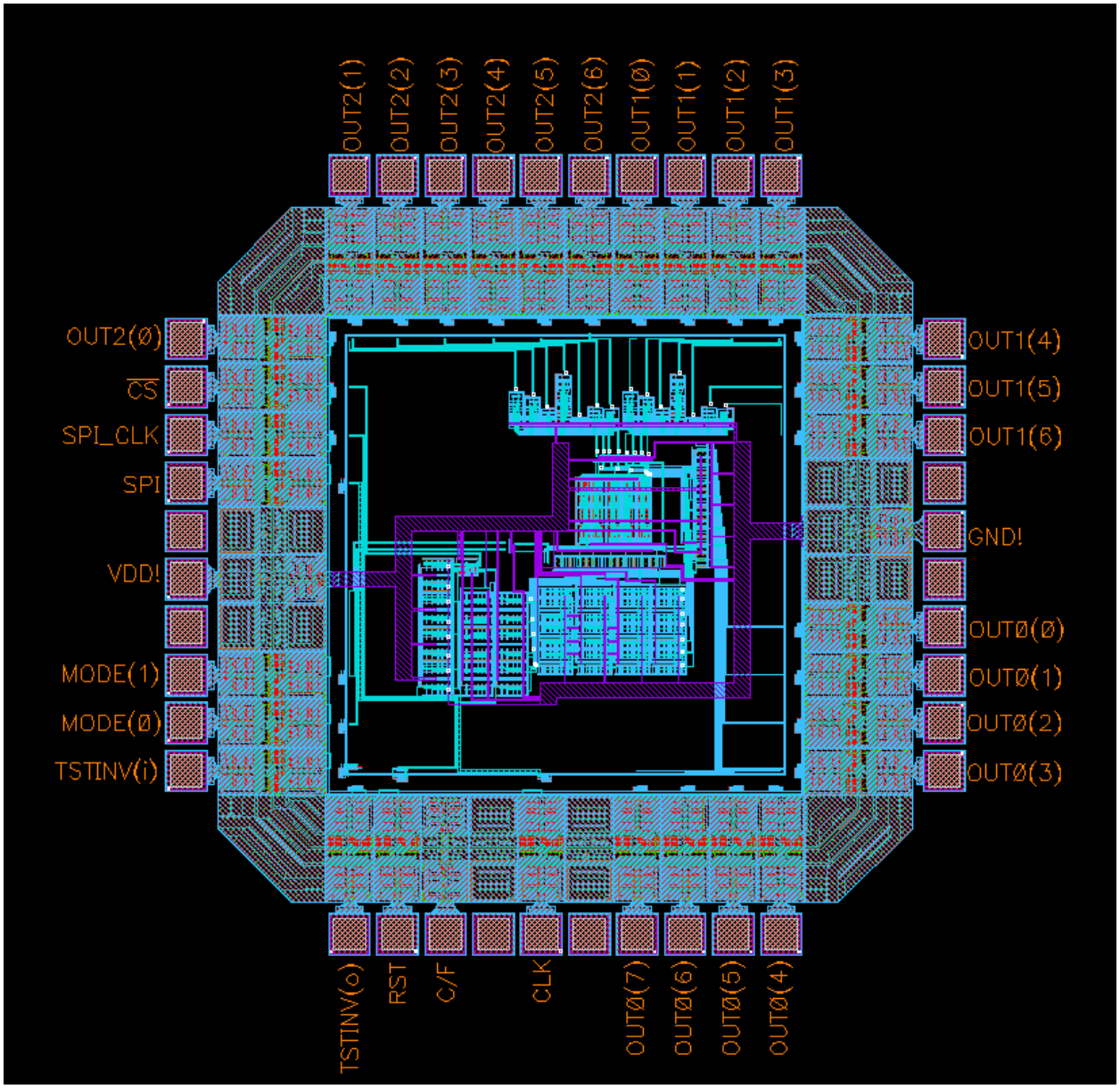
   Data path and Control path design done automatically using computer program(s).

   High-Level synthesis is a computer-aided procedure pertaining to the Architectural Design process which is a subset of the VLSI Design process in which Design Automation is applied. In essence High-Level synthesis is one of the key aspects of Design Automation.

3. **What are 6 types of layout styles? Briefly describe and illustrate, with an example, each style.**

a. <u>Full Custom</u>

   An arduous approach to layout involving many man-hours but with the benefit of optimized area and performance, usually meant for mass produced chips.



* Digital Thermometer for CMOS-VLSI Fall 2014 based on MOSIS fabrication process

b. Gate-Array

A 2D array of transistors prefabricated on a chip where by the appropriate metal connections will form a specific design. This reduces design time and cost but increases difficulty in automatic wiring as there is limited wiring space.

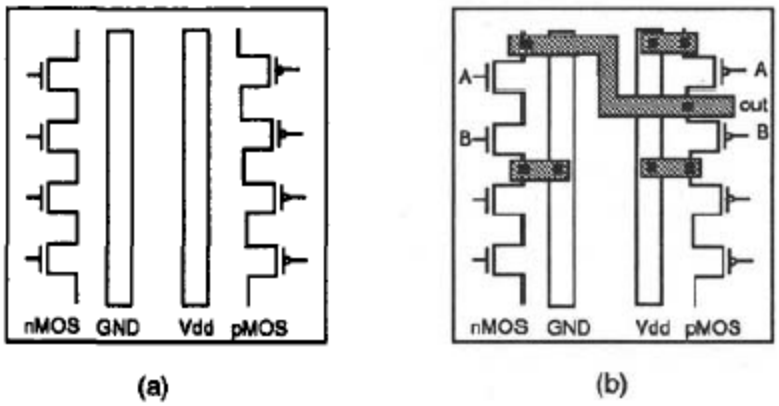


Fig. 1.3 (a) Example of a basic cell in a gate-array. (b) Cell personalized as a two-input NAND gate.

* Source: VLSI Design Automation, Yousef and Sait

c. Standard Cell

A standard function implemented using specific library rules. Standard cells belong to libraries in which the height of each cell is fixed and every function is defined by its name, functionality, and i/o structure for a particular node size.

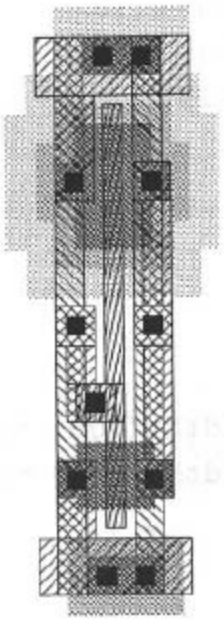


Fig. 1.6 Layout of standard-cell ils.

* Source: VLSI Design Automation, Yousef and Sait

d. Macro Cell

Cell based design with no limits on cell size allowing for complex cell designs in a library. However this approach is difficult to process with automatic layout tools.

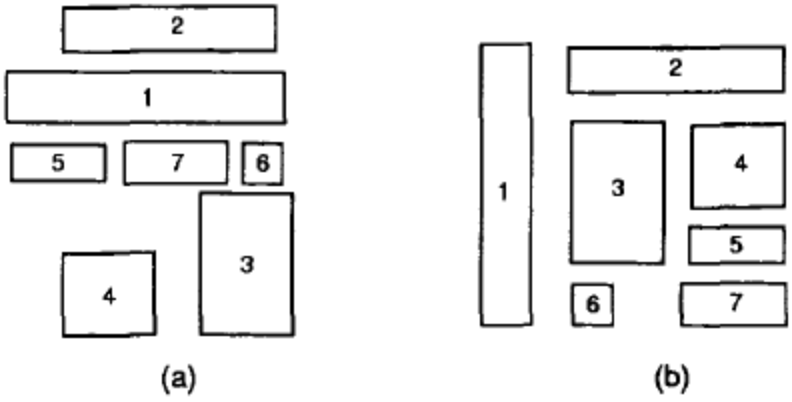


Fig. 1.8 (a) Cells of varying heights and widths placed in a row-based floorplan. (b) A more compact floorplan for the same circuit.

* Source: VLSI Design Automation, Yousef and Sait

e. PLA

A method of implementing two-level sum of products design expressions. There exists an array of AND gates and an array of OR gates in which the appropriate connections for a given expression are realized.

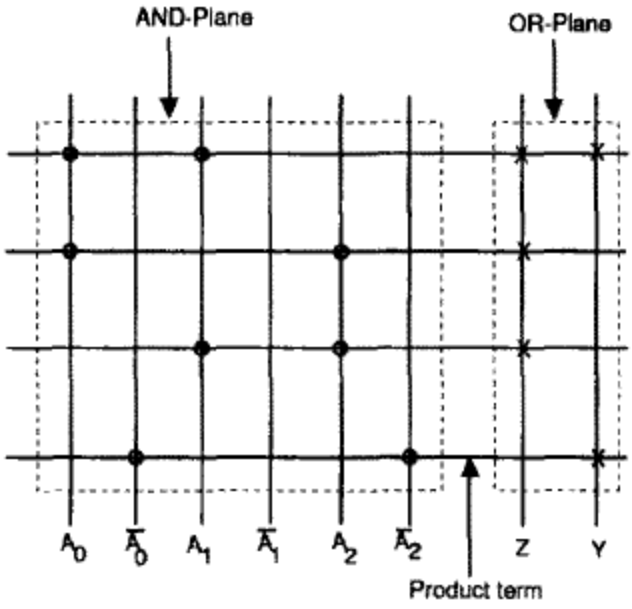


Fig. 1.9 A PLA to implement functions Y and Z. There are 4 rows corresponding to four product terms. There are 6 columns in the AND plane, two for each of the inputs. There are two columns in the OR plane, one for each output.

* Source: VLSI Design Automation, Yousef and Sait

f. FPGA

Field Programmable Arrays use configurable logic blocks (CLB) to implement a design. Look-up tables provide a convenient way to realize functions. Routing between CLBs is achieved via switch boxes. FPGAs are great for prototyping designs before committing to chip.

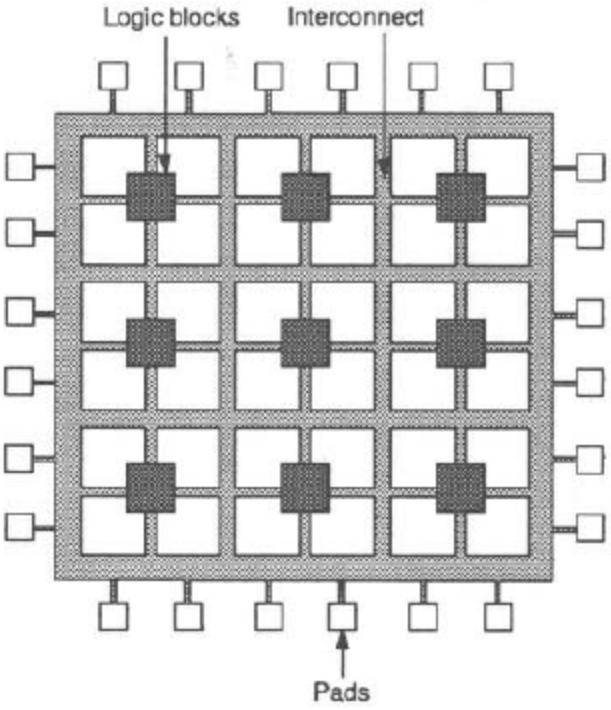


Fig. 1.10 Diagram of a typical FPGA.

* Source: VLSI Design Automation, Yousef and Sait

4. What are the 7 subdivisions of problems in VLSI Physical Design? Briefly describe each problem.

a. Circuit Partitioning

Necessary when a design is too large for a chip with predefined size constraints.

b. Floorplanning

Arranging macro cells so that area utilized is optimized.

c. Circuit Placement

Circuits are placed strategically to reduce wiring area.

d. Global Routing

Routing for each net in terms of the channels to be used.

e. Channel Ordering

Since channels are dependent on each other a ordering must be realized to satisfy the pin requirements of each channel.

f. Detailed Routing of Power and Ground Nets

Applying the appropriate connections to each circuit for power and ground, while adhering to the special constraints imposed by power and ground nets.

g. Channel and Switchbox Routing

Assigning wires to different circuit components.

5. Complete the table below.

Design Style	*Application*	*Design Time*	*Fab Effort*	*Cost*	*Performance*
Full Custom	High volume	High	High	High	High
Gate Array	ASIC	Low	Low	Low	Low
Standard Cell	ASIC	Low	Low	Low	High
Macro Cell	General	High	High	Low	High
FPGA	ASIC	Low	-	Low	Low