CDA 3201 - Computer Logic Design

Homework Assignment 3 (Total: 100 Points)

Due to: Tuesday 07/08/2014

Turn in as hardcopy format in class

10 bonus points for typed homework

Question 9 has 20 points. 1-8 have 10 points each

1. (8 points) Given a four input Boolean function $F(a,b,c,d)=\sum m(0,3,5,7,11,12,13,15)$

   a. Implement the function using 8:1 multiplexer with A,B,C as multiplexer control inputs and D, D' as data inputs.
   b. Implement the function using a 4:1 multiplexer with C and D as control inputs and one XOR gate to form one of the inputs to the multiplexer.

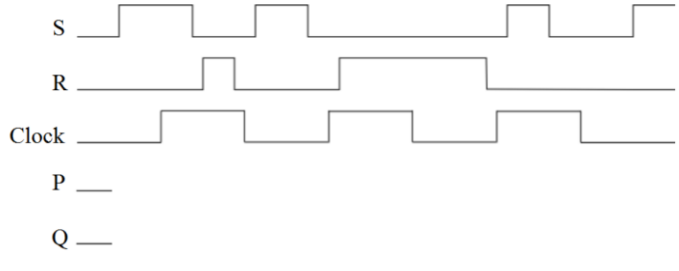
2. Implement following function using 8:1 multiplexer
   a. $F(a,b,c,d,e)=\sum m(1,3,6,15,19,25)$

3. Exercise 4.12 from the text book.
4. Exercise 4.15 from the text book.
5. Exercise 4.14 from the text book. (Only part c and d)

6. (Clocking Issues) Given the sequential-logic circuit in Figure 6.19 (page 303 of textbook), where the flip-flops have worst case setup times of 25 ns, propagation delays of 15 ns, and hold times of 5 ns, answer the following questions:

   a. Assuming 0 propagation delay through the combinational logic block, what is the maximum allowable frequency of the clock that controls this subsystem?
   b. Assuming a typical combinational-logic delay of 80 ns and a worst-case delay of 110 ns, how does your answer to part (a) change?

7. Given the input clock transition below, indicate the outputs of a negative edge triggered R-S master slave flip-flop. *P* is the output of the master and *Q* is the output of the slave (refer to the left half of figure 6.19 on page 269 to find outputs *P* and *Q*).



8. Exercise 6.4 from the textbook.
9. Exercise 6.26 from the textbook.