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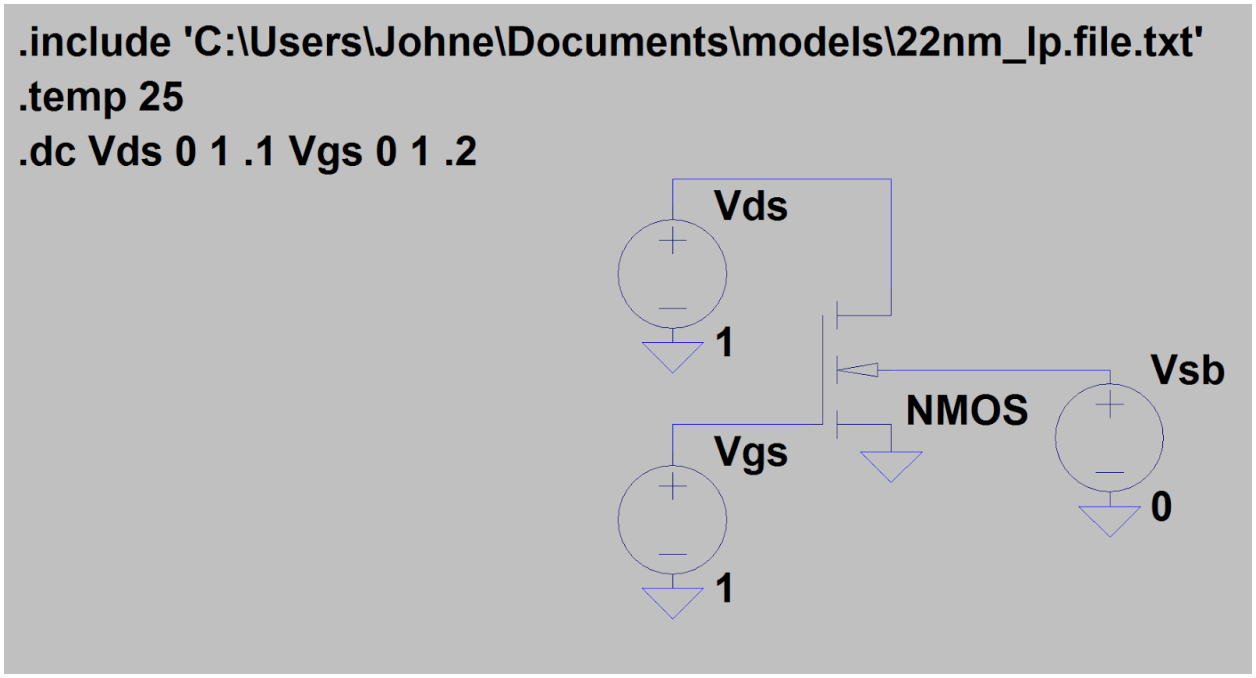
CIS 4930 Fall 2015

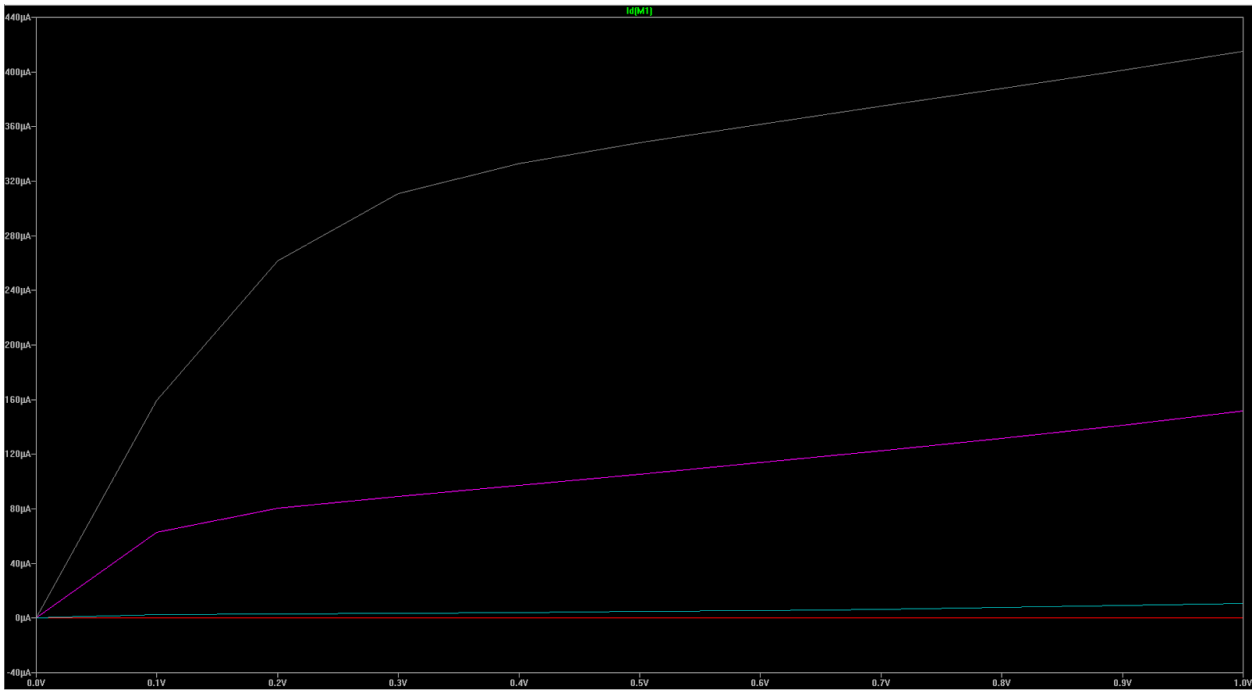
Homework #2

Question 1
Characteristic I-V curves for NMOS transistor

Schematic



Waveform



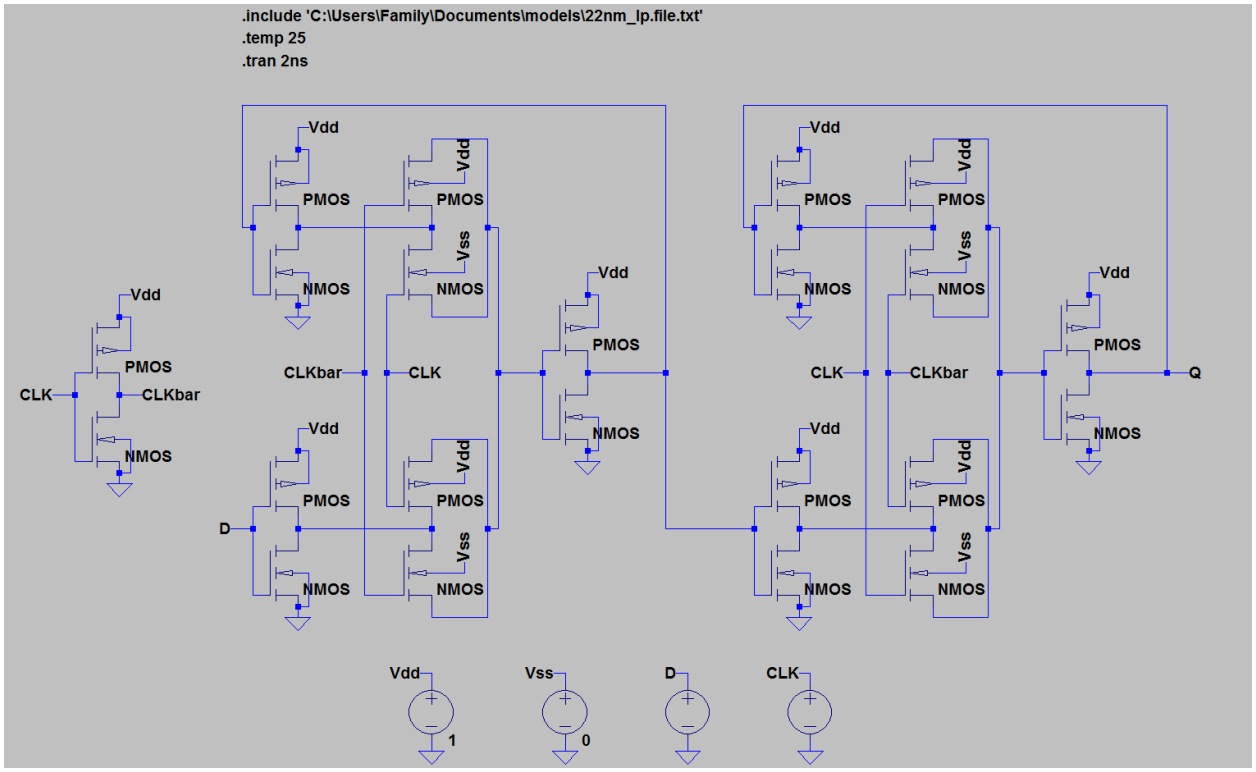
The characteristic curves do not begin to fully develop until both the gate-source and drain-source voltages approach Vdd (1 volt).

Question 2

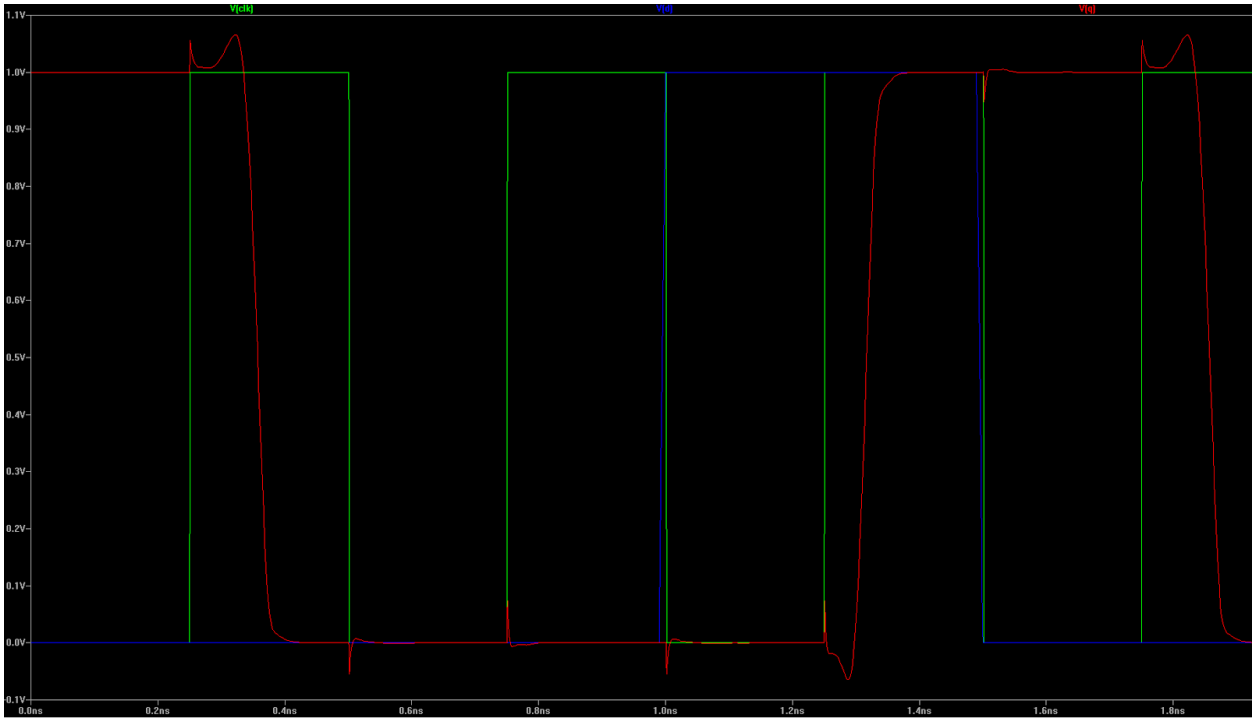
A. Demonstrate the operation of a flip-flop by writing a 0 and 1 with a clock frequency of 2 GHz

Clock cycle time for a 2 GHz clock was obtained using the formula, period = 1 / frequency, therefore the period in seconds is equal to $1 / 2 \times 10^9$. Multiplying by 1×10^9 gives a clock cycle time of *0.5 nanoseconds*.

Schematic



Waveform

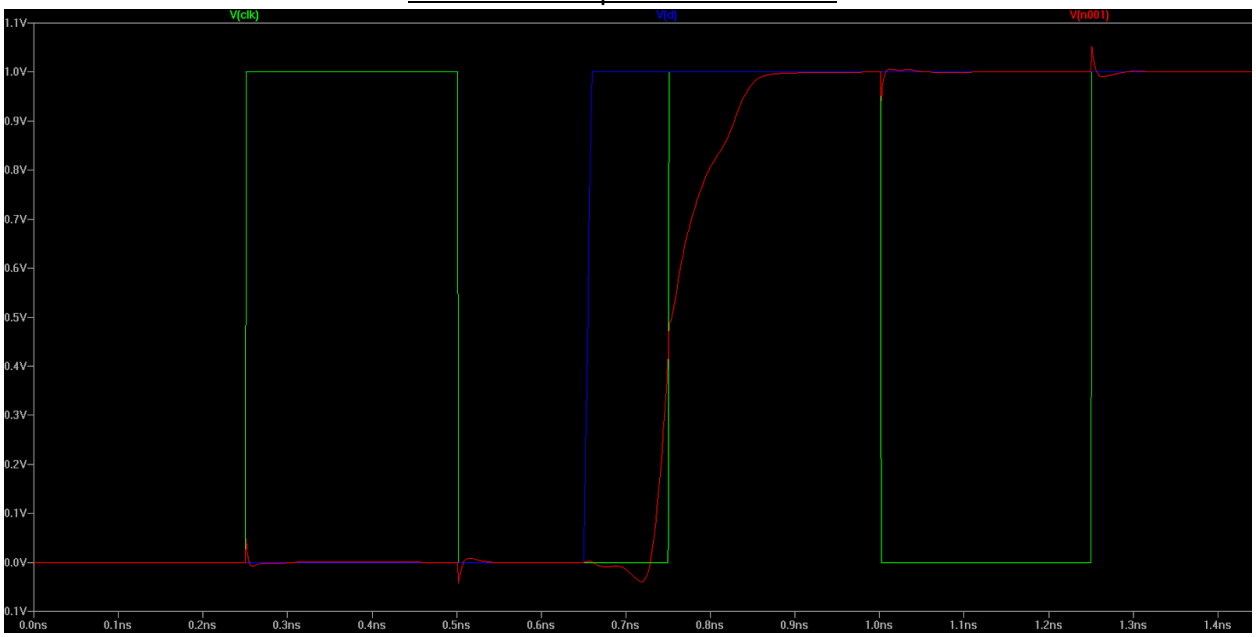


In this image the flip flop starts in an indeterminate state so the input is ignored for the first clock cycle to allow time for the output to settle. On the rising-edge of the 2nd and 4th clock

cycles an input of 0 is purposely written where the output is shown to update as desired. For the rising edge of the 3rd clock cycle the input is set to 1 and the output changes accordingly.

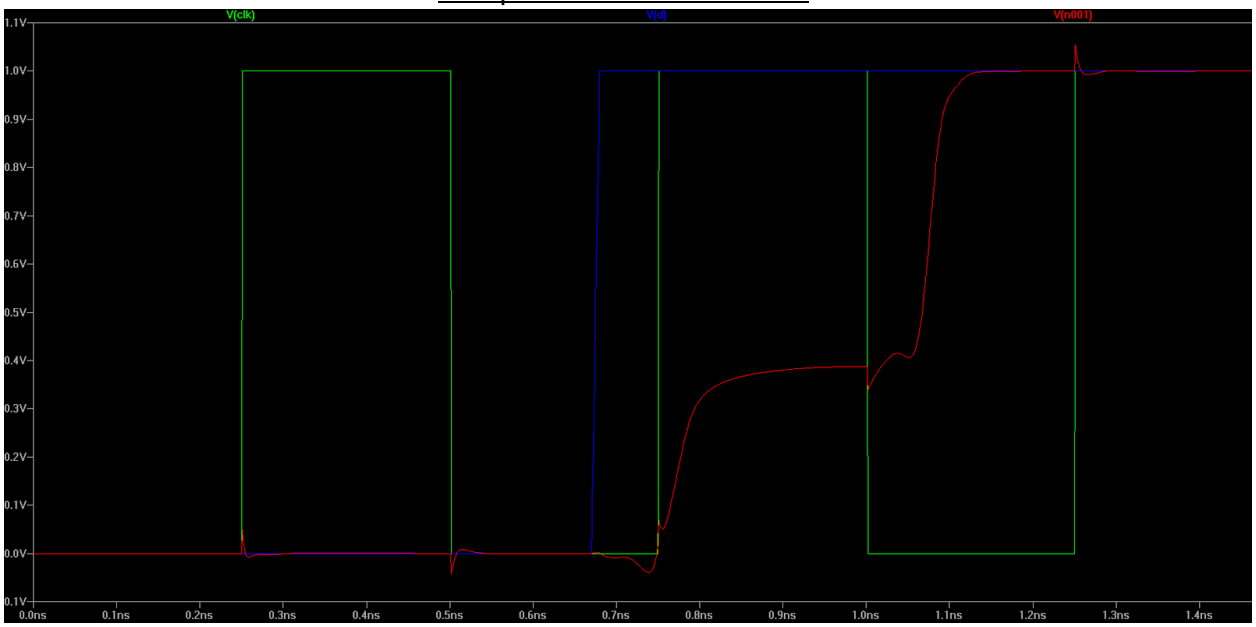
B. Report setup time, hold time, and clock to q delay

Minimum Setup Time Waveform



This image shows a minimum setup time of around 90 ps for the master stage.

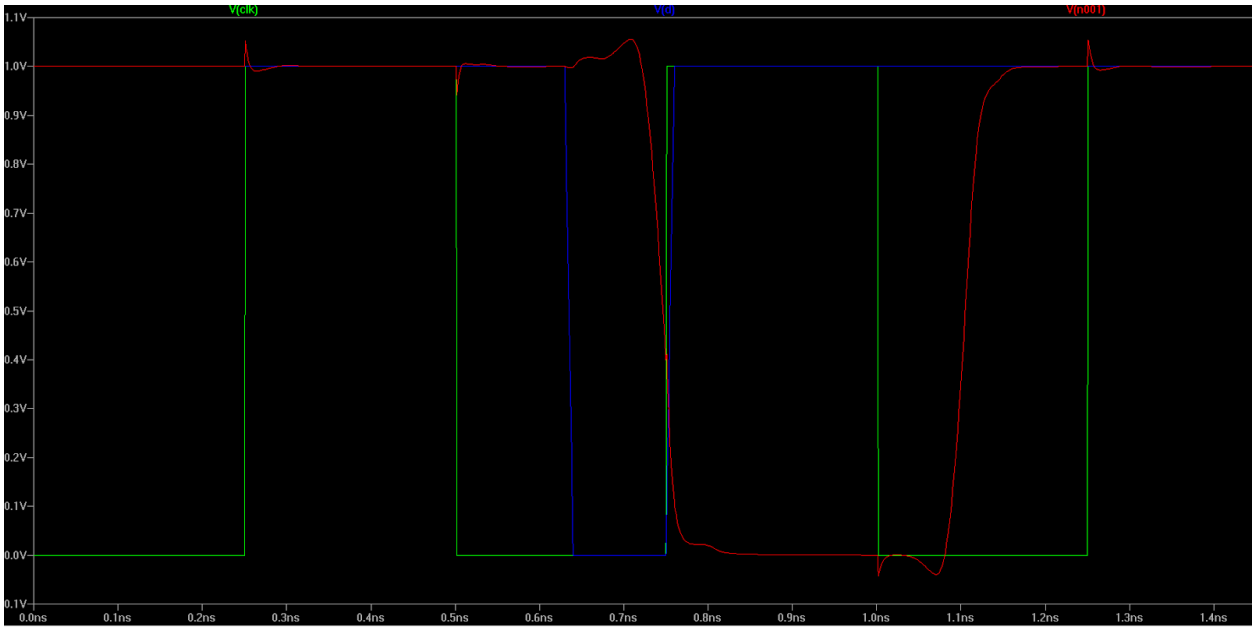
Setup Time Limit Waveform



This image shows an invalid setup time of 70 ps where the 22nm CMOS flip flop fails to latch the input within a desired timeframe for the master stage.

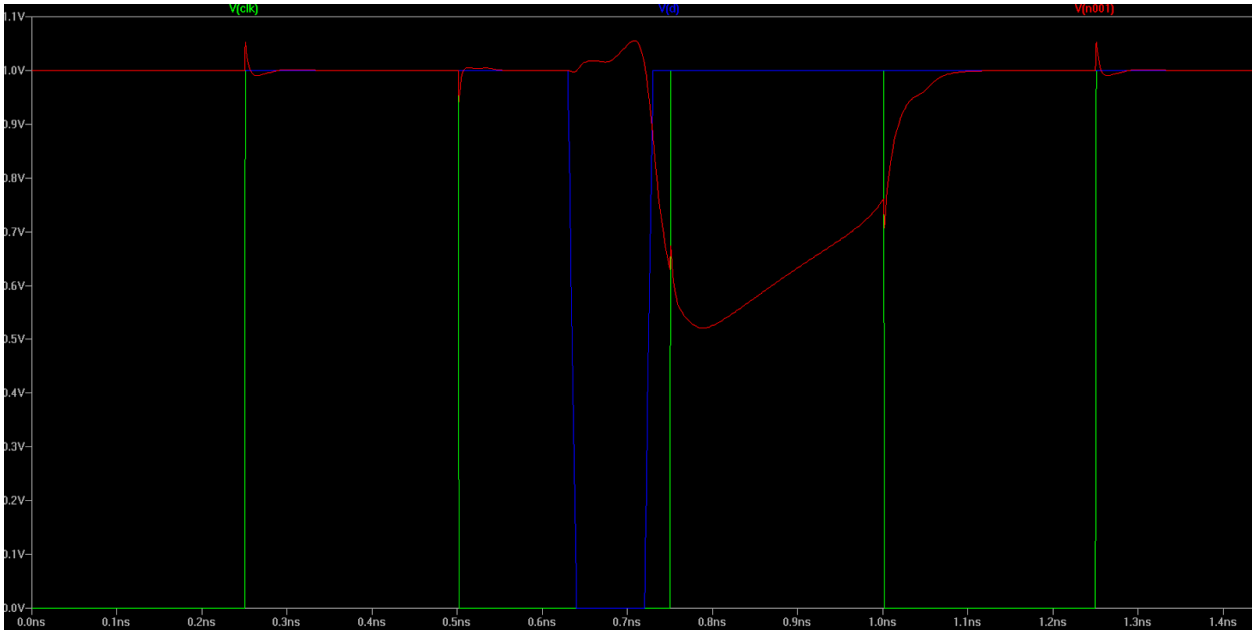
By observing the minimum and limit setup time waveforms one can make the assumption that propagation delay *increases* as the setup time *decreases*. Thus any setup time greater than or equal to 90 ps will allow the master stage to perform as expected.

Minimum Hold Time Waveform



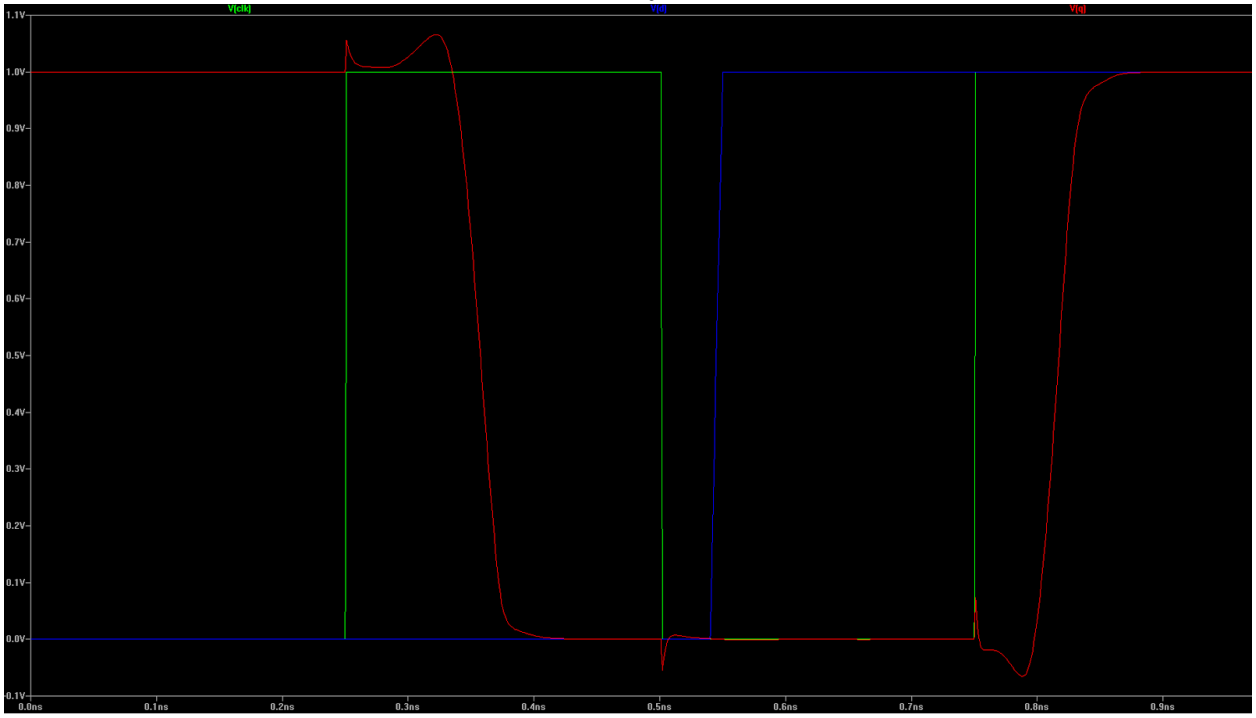
This image shows a minimum hold time of around 10 ps, any less and the input would not have been held long enough for the rising edge of the clock to latch the correct input into the master stage.

Hold Time Limit Waveform



This image shows a hold time of around -20 ps, a value too small to trigger the appropriate behavior of the flip flop master stage on the rising edge of the clock. This image also shows the possibility of having a negative hold time where the input can transition before the rising edge of the clock given an appropriate setup time.

Clock to Q Delay Waveform



Based off the rising edge of the second clock cycle around 750 ps (.75 ns) and when the output first plateaus around 875 ps (.875 ns) then the clock to Q delay is approximately 125 ps for the master-slave flip flop.