Low Power VLSI Design
CIS4930 S15
4/22/2015

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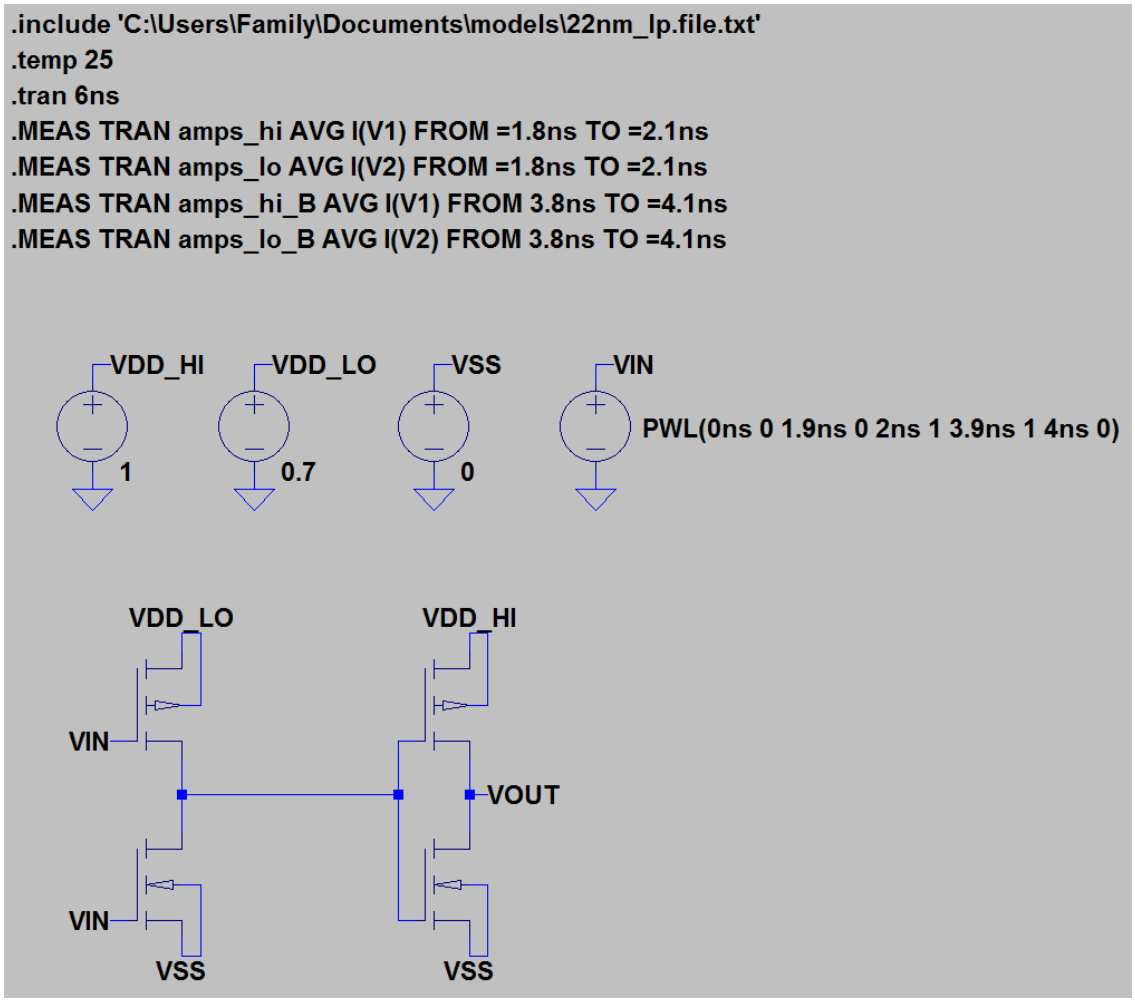
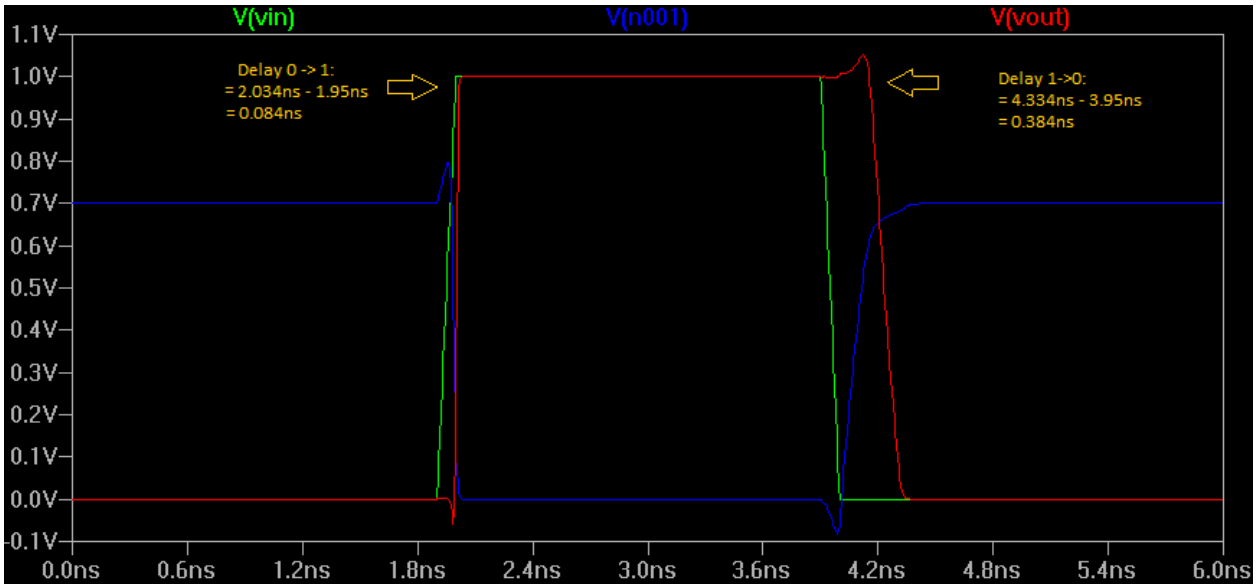
Assignment #5

Question 1

Schematic



Plot



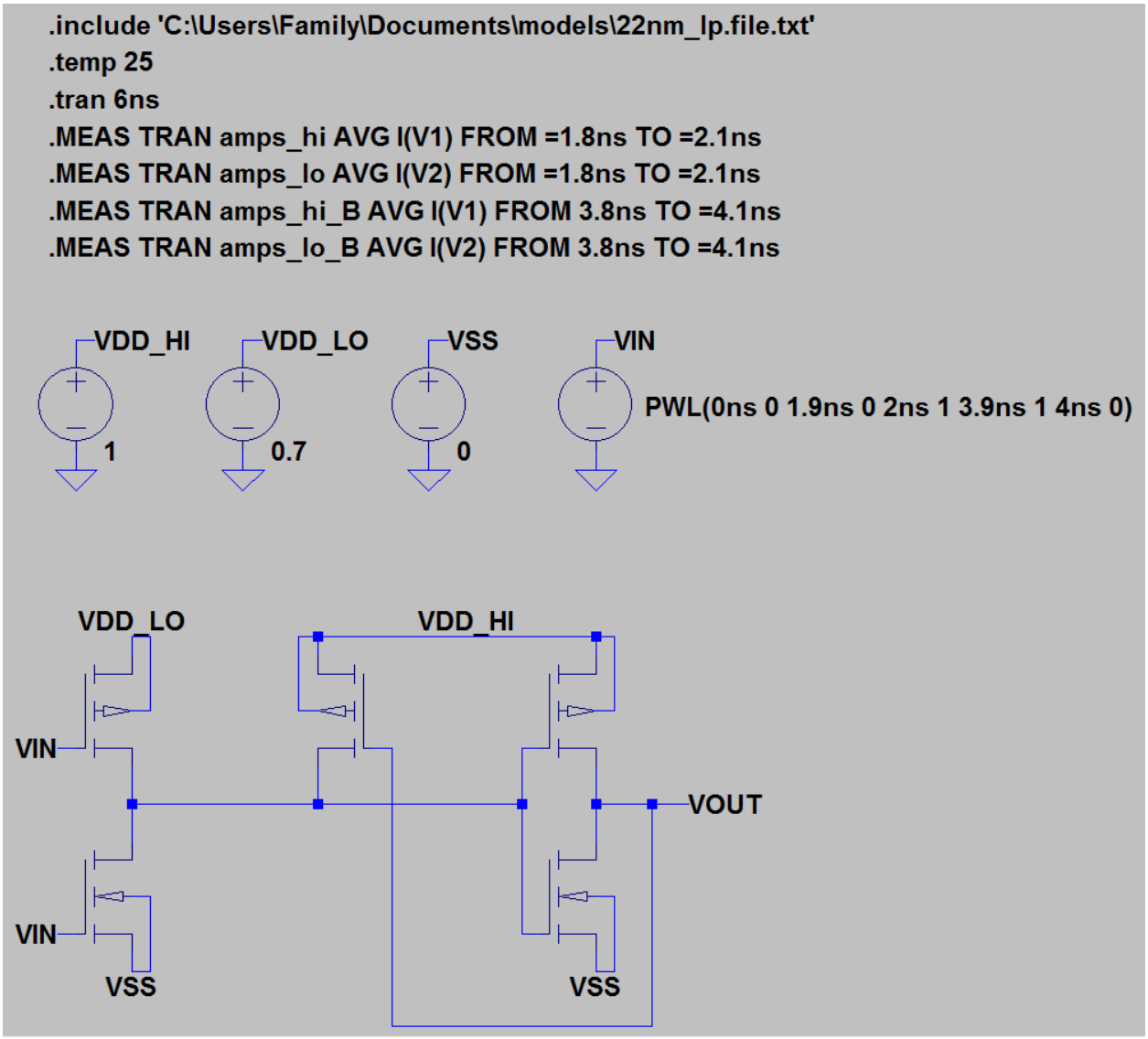
A) The output of the first inverter never reaches 1V instead it tops out at 700mV when the primary input is 0. Also there is greater propagation delay when transitioning from high to low compared to a low to high transition.

B) Delay for 0->1 transition = 0.084ns
Delay for 1->0 transition = 0.384ns

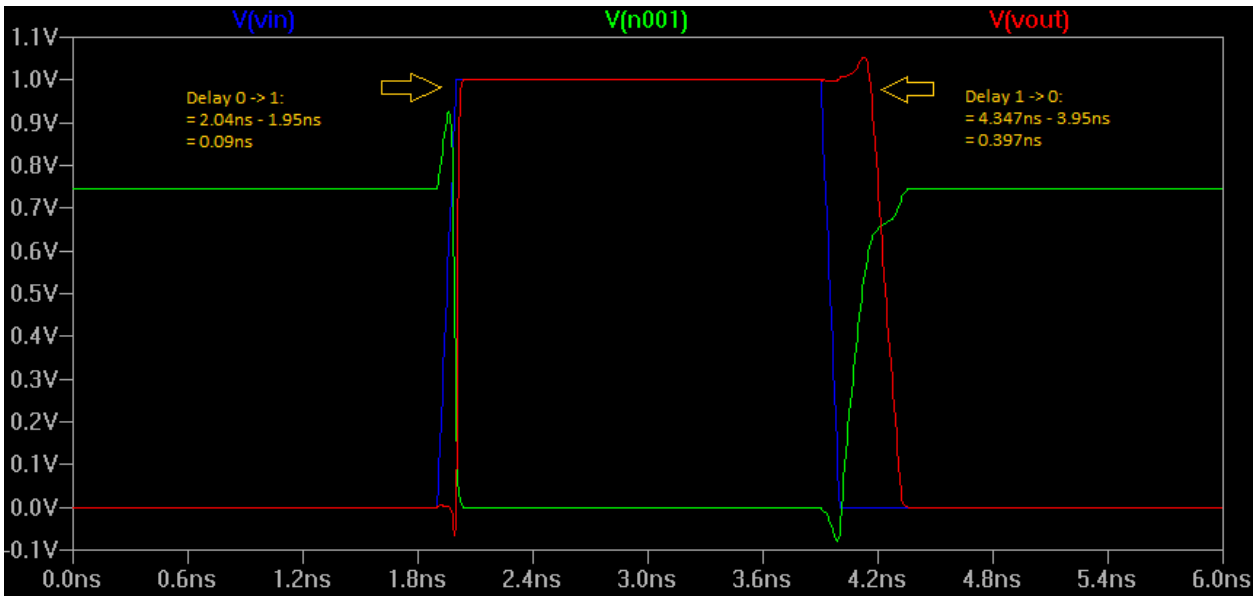
Question 1 Power Consumption for Transistions		
0 -> 1		
current @ 1V	current @ 0.7V	Power: (1V * current @ 1V) + (0.7V * current @ 0.7V)
8.56E-06	4.45E-07	8.86876E-06
1 -> 0		
current @ 1V	current @ 0.7V	Power: (1V * current @ 1V) + (0.7V * current @ 0.7V)
3.12E-06	1.02E-05	1.02634E-05

Question 2

Schematic



Plot



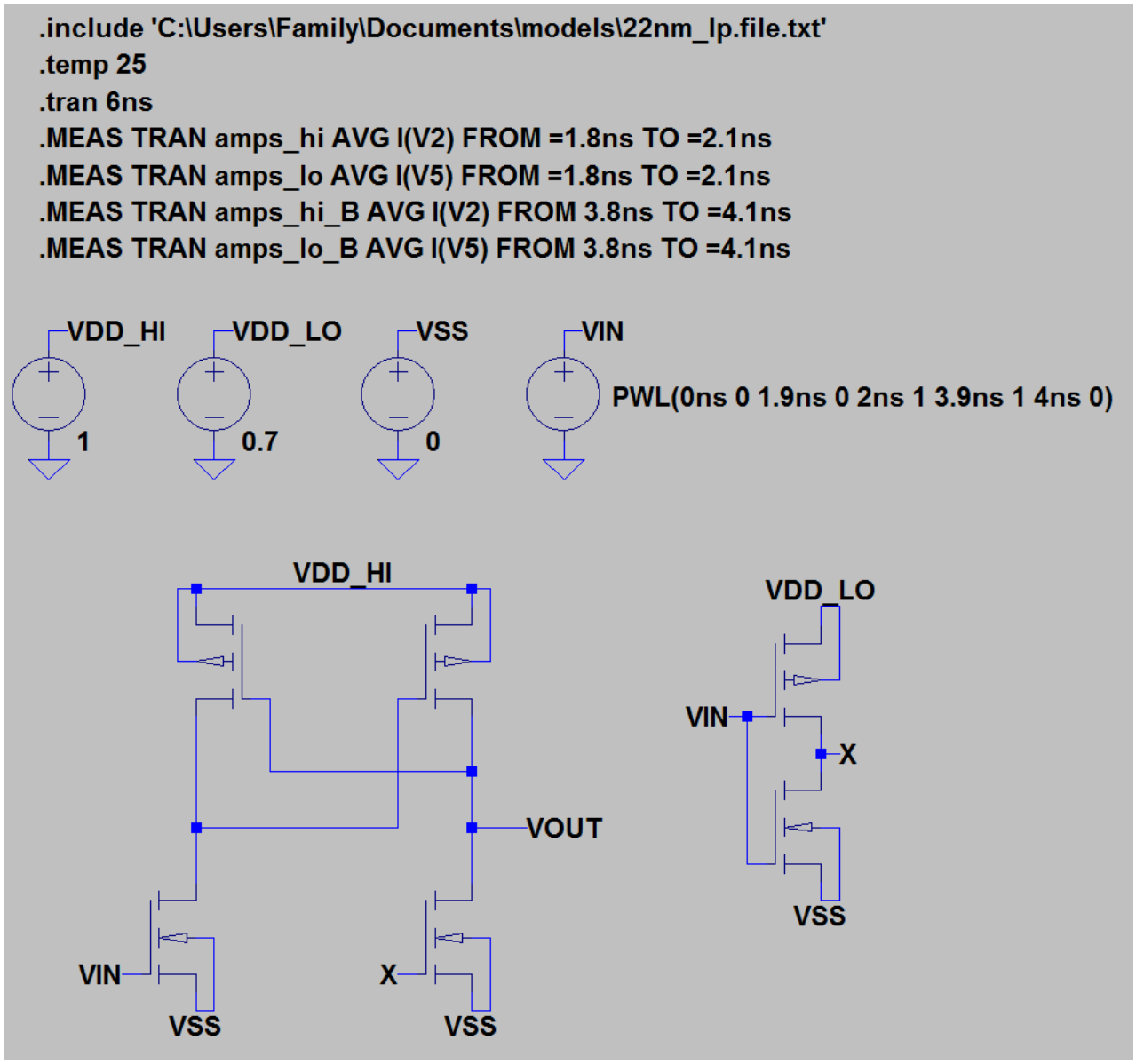
A) Advantage to this design is that the output of the first inverter is increased to 750mV, although that is not really an improvement. One disadvantage would be the increase in propagation delay when transitioning from high to low.

B) Delay for 0->1 transition = 0.09ns
Delay for 1->0 transition = 0.397ns

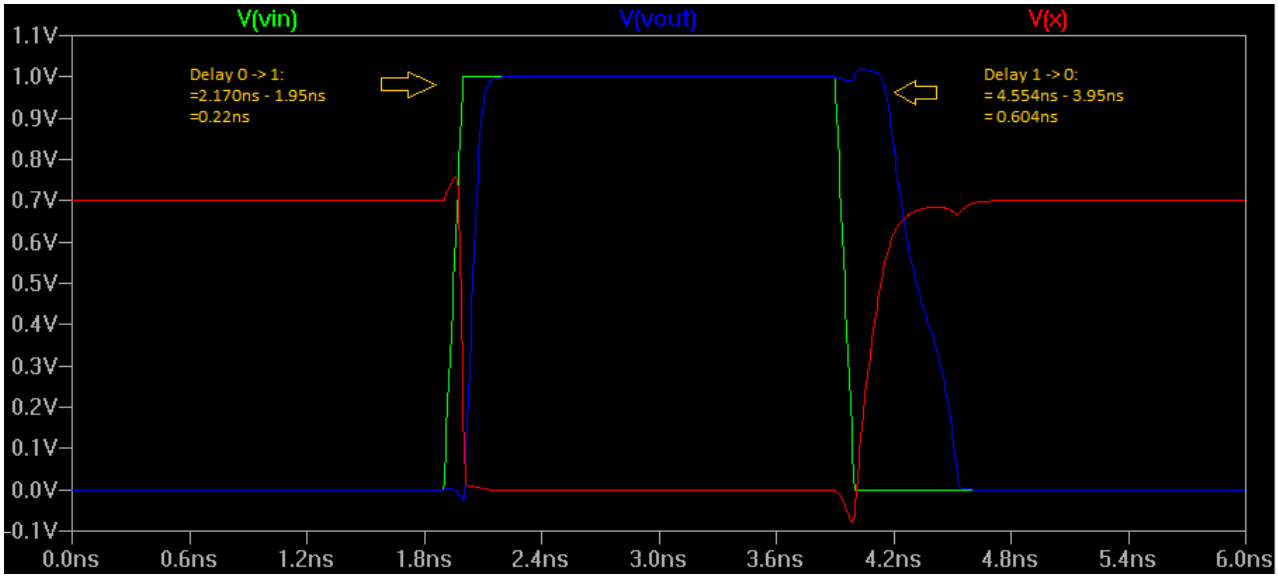
Question 2 Power Consumption for Transistions		
0 -> 1		
current @ 1V	current @ 0.7V	Power: (1V * current @ 1V) + (0.7V * current @ 0.7V)
1.82E-05	5.66E-06	2.21949E-05
1 -> 0		
current @ 1V	current @ 0.7V	Power: (1V * current @ 1V) + (0.7V * current @ 0.7V)
3.19E-06	1.03E-05	1.03838E-05

Question 3

Schematic



Plot



A) The first inverter output was increased to a full 1V which is far better than the previous two implementations; however propagation delay has increased for both transitions as well.

B) Delay for 0->1 transition = 0.22ns
Delay for 1->0 transition = 0.604ns

Question 3 Power Consumption for Transistions		
0 -> 1		
current @ 1V	current @ 0.7V	Power: (1V * current @ 1V) + (0.7V * current @ 0.7V)
1.10E-05	1.49E-07	1.10816E-05
1 -> 0		
current @ 1V	current @ 0.7V	Power: (1V * current @ 1V) + (0.7V * current @ 0.7V)
2.84E-07	5.23E-06	3.94521E-06

Question 4

A) Technology scaling each generation improves operating frequency primarily due to reduced number of gates and advanced circuit techniques, logic transistor density has been decreasing for new microarchitectures, and “microprocessors ported to next-generation technologies with constant voltage scaling do not show a decrease in power; the power remains constant. On the other hand, microprocessors ported to technologies using constant electric field scaling decrease in power” (Borkar, Shekar).

B) In terms of technology scaling, “interconnect distribution does not change significantly with advances in microarchitecture” (Borkar, Shekar).

C) As technology scales each generation the subthreshold leakage will increase by a factor of 5. To maintain low subthreshold leakage it’s possible to reduce die temperature.

D) As technology scales circuit designers will face greater challenges in scaling threshold to satisfy performance demand and reduce leakage power. Circuit techniques such as “domino” offer an advantage in increasing performance but this technique’s benefit over static logic will continue to decrease with technology scaling.