Homework #4

Due April 11, 2015

CIS 4930/6930: Low Power VLSI Design

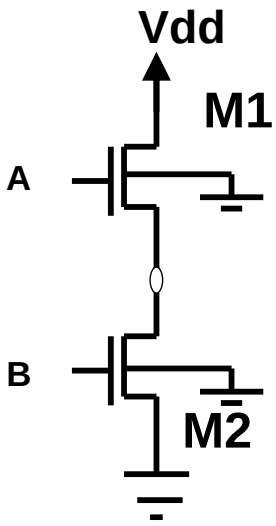
Notes:

1. **The homework will be done and the report must be submitted individually.**
2. **Submit schematics, measurement files, netlist, plot of signals to get full credit**

Q1. Input vector control for leakage power reduction: This exercise will focus on input conditioning for low power. Assume two stacked NMOS transistors of size 1u/0.03u each and Vdd=1V as shown below. For the simulations assume temperature=110C

(a) Find input conditions A and B that minimizes the subthreshold leakage.
(b) Find input conditions A and B that minimizes the gate leakage.
(c) Find input conditions A and B that minimizes the junction leakage.
To get full credit in above questions plot leakages for all four combinations of A and B (00,01,10,11). Any plotting software (excel, matlab, gnuplot) can be used.
(d) Fix A=0 and B=0. Next sweep the channel length of both transistors from 30nm to 180nm in steps of 10nm and plot subthreshold leakage vs channel length. Explain the observation.

(10+10+10+20)



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Q2. Read the paper "low power CMOS digital design" posted in canvas and answer following questions:

(a) Between static and dynamic logic, which one is good for low power and why? (Be specific but don't write thesis).
(b) For low power should we increase the transistor sizing or reduce it? Explain the tradeoff.
(c) How logic duplication helps in lowering the power consumption? Explain with power equation and example.
(d) How pipelining helps in lowering the power consumption? Explain with power equation and example.
(e) Is it possible to continue logic duplication infinitely to keep lowering voltage and reduce power? If not, what sets the limits for logic duplication?

(10+10+10+10+10)