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CMOS VLSI Lab # 6

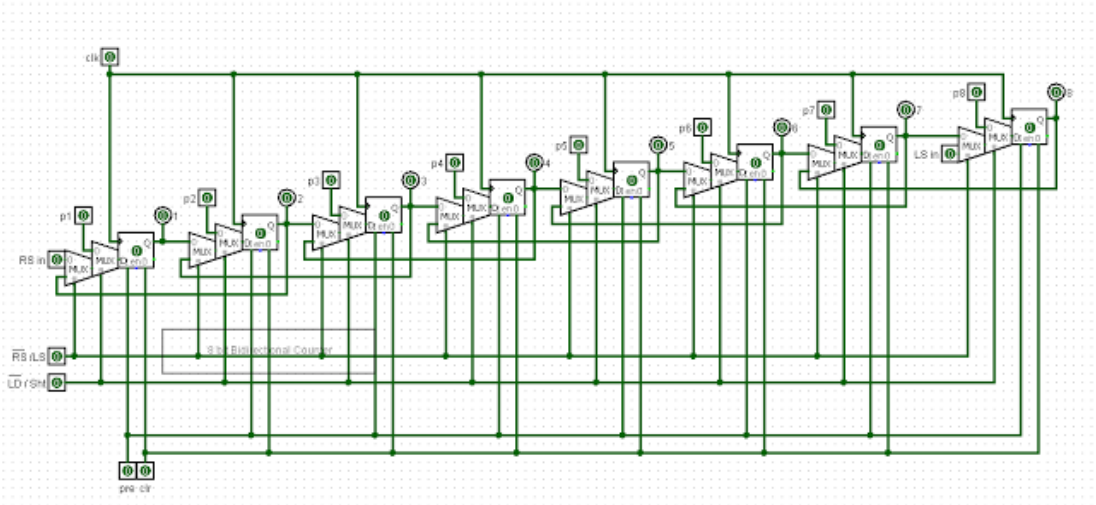
Introduction & Background

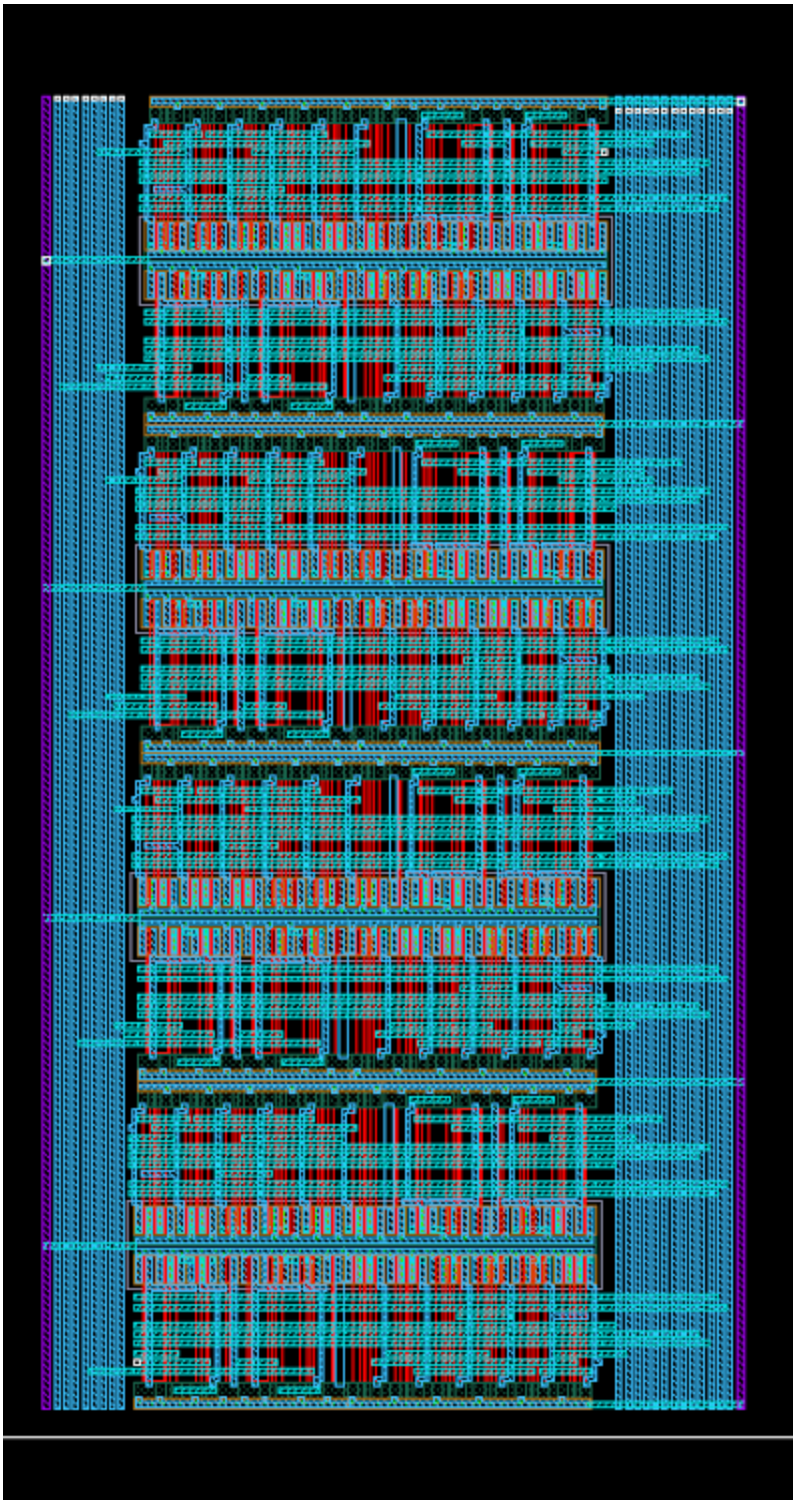
In this lab we were tasked with creating CMOS layouts of different 8 bit sequential logic circuits. More specifically an 8-Bit Bidirectional Shift registers, 8 Bit bidirectional counter, and lastly 8 bit serial adder/subtractor. Each of the circuit is described below in detail. For some circuits we went as far as to name them since we felt we got to know them pretty well.

Design & Layout

8-Bit Bidirectional Shift registers-

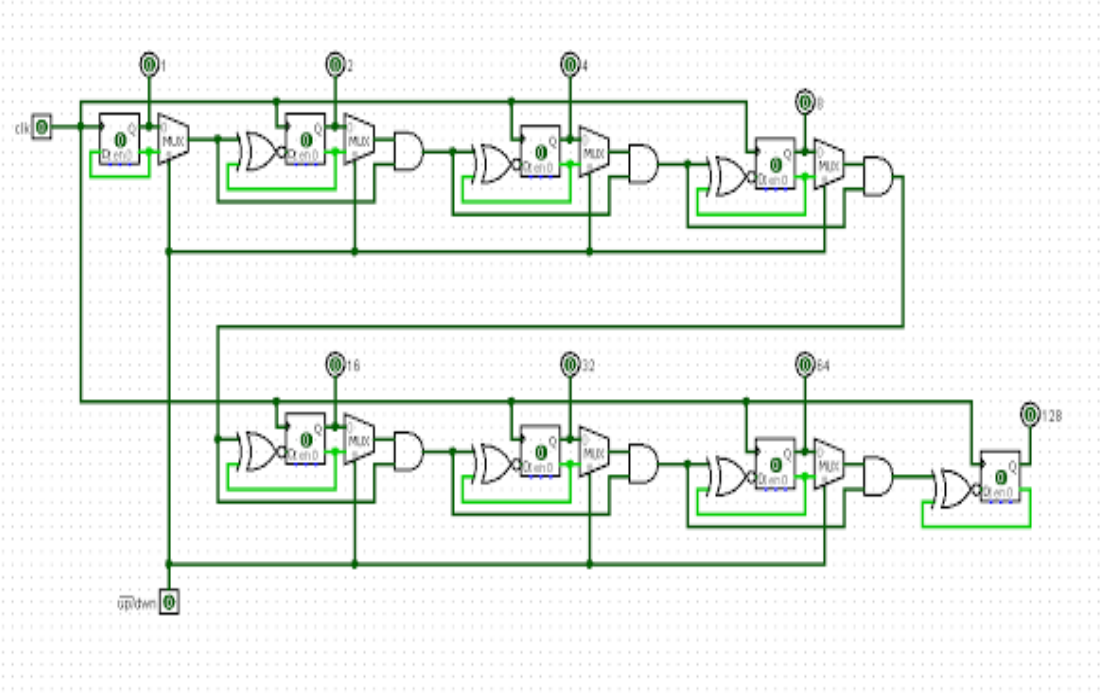
A shift register is a circuit that shifts the array of bits in either the left or right direction (depending on the implementation) one bit at a time. They are commonly used in signal processing application to store and delay data. A 8 bit bidirectional shift register specifically is able to shift in both directions: L- > R or R -> L. We call our 8 Bit Bidirectional shift register **"Shifty Shifterson"**. For our implementation of the circuit we used 8 bit sliced registers which feature parallel in/serial in/serial out/parallel out.Below are both the gate level and layout representation**.**

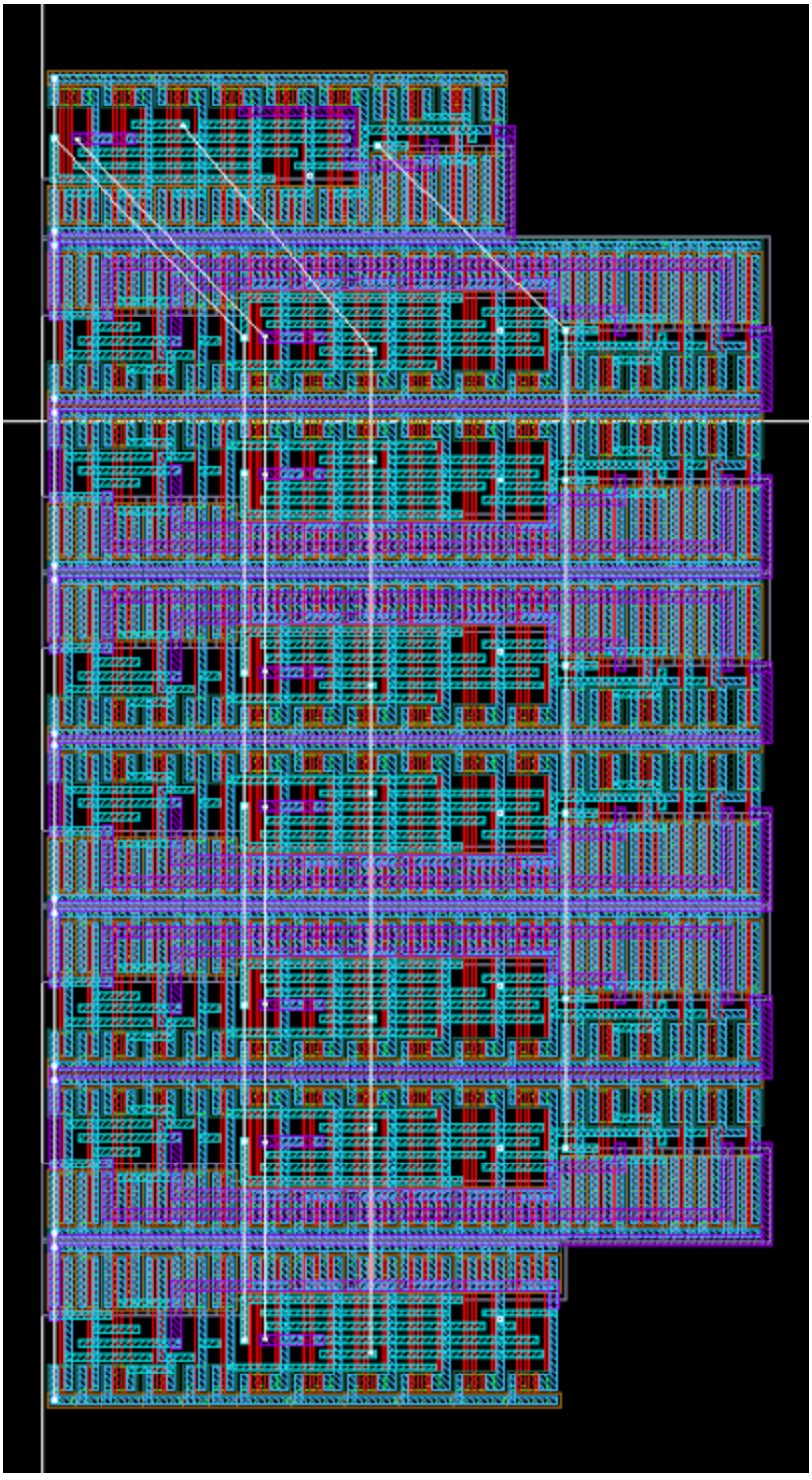




8 Bit Bidirectional Counter-

A bidirectional counter is a digital circuit which is able to count up or down. We call our 8 Bit Bidirectional Counter **"Count Chocula**" For our implementation of the circuit we first created a bit slice. The bit slice contains a flip flop an XNOR gate, a MUX and an AND gate. These bit slices are used for the middle six bits of the counter the remaining bits are stripped down version of the bit slice because some functionality is not needed on the ends. Our design is synchronous, and each bit changes on a single clock, rather than the traditional design with the clock input of one bit being fed by the data output of another. Below are both the gate level and layout representation.



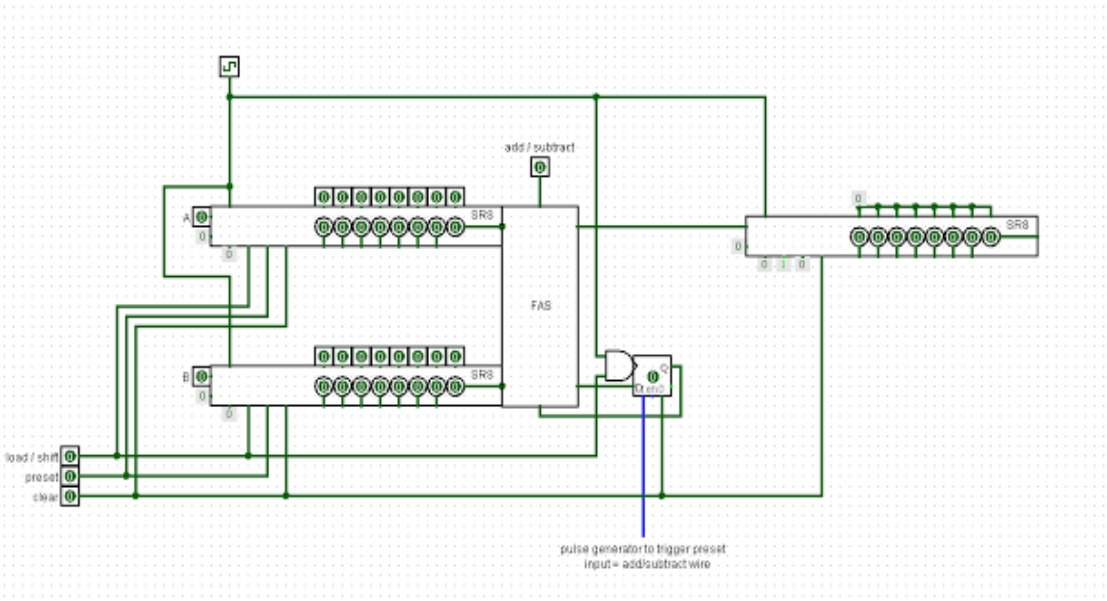


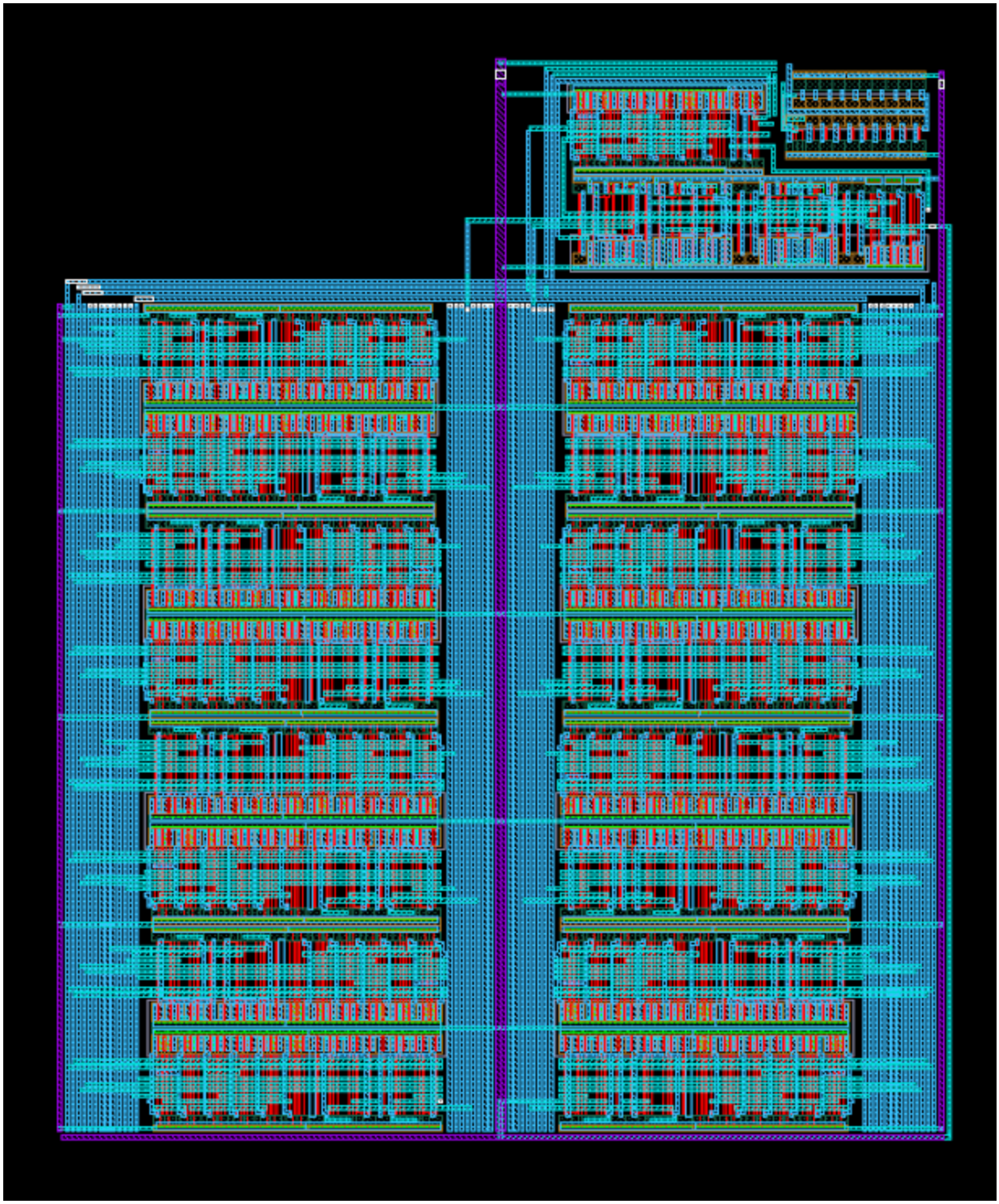
8 Bit Serial Adder/Subtractor-

A adder is a circuit which is able to add two numbers of size n bits and calculate a sum of size n+1 which depending on how you do your logic and implementation can be truncated to n bits. A subtractor is a similar circuit but take the difference of two numbers. A simple adder/subtractor is a circuit that has both an adder and a subtractor and is able to switch between the two. More specifically a serial adder/subtractor is a digital circuit which takes in an 8 bit number one bit at a time and performs either subtraction or addition on the two numbers.We call our 8 bit serial Adder/subtractor **"Serial Mathist"**.For our implementation of the circuit we had to use a pulse generator more specifically " a one shot" to carry in a one to our full adder and subtrator when asserting the add and subtract control line. Essentially the D flip flop will be asynchronously loaded with one. In the gate level the FAS circuit block is the custom implementation of our bit slice adder and subtractor and the SR8 circuit block is the custom implementation of our 8 bit shift register. However the circuit block for our pulse generator "one shot" can not be designed properly in logisim due to fundamental issues with the program.

The design of the "one shot" circuit is comprised of 19 inverters chained together and a nand gate whom share a common input.The propagation delay from the inverters causes a static hazard such that the output of the "one shot" will pulse for a finite time specified by the number of inverter stages.In our case through extensive testing it was determined that a one to two nanosecond pulse required approximately 9 inverters thus to insure a timely pulse that will confidently trigger a D flip flop when tested in microseconds.

Below are both the gate level and layout representation.

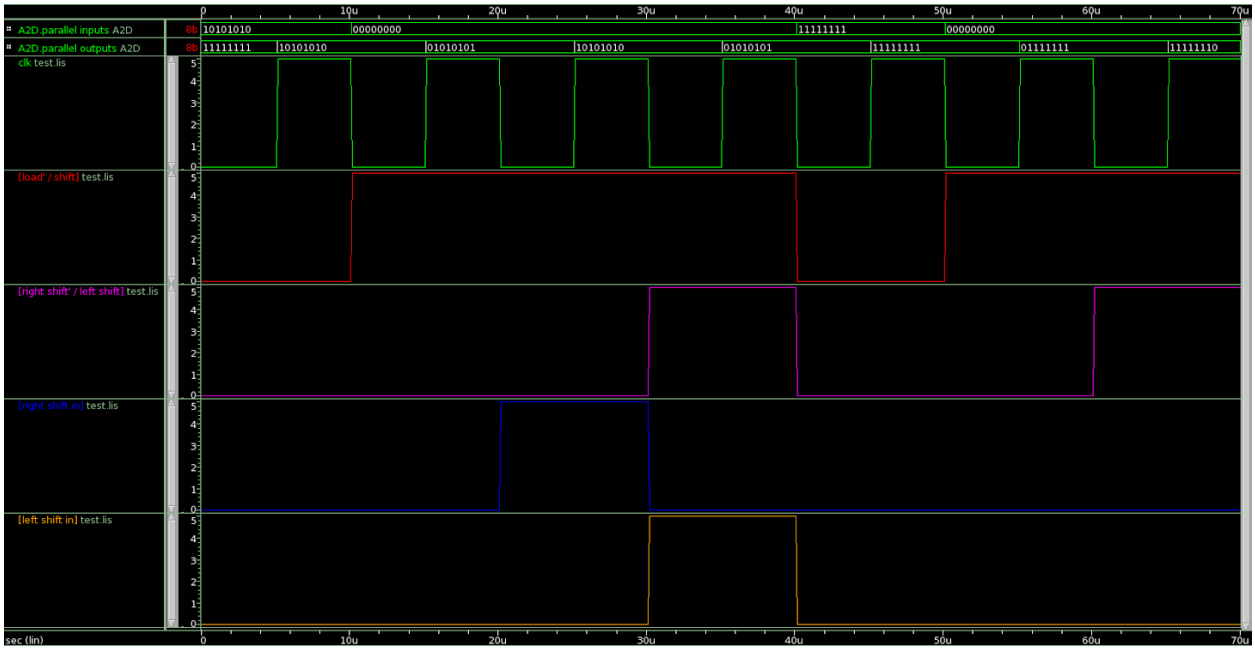

add / subtract
A
B
SR8
SR8
SR8
FAS
load / shift
preset
clear
pulse generator to trigger preset
input = add/subtract wire



Testing & Results

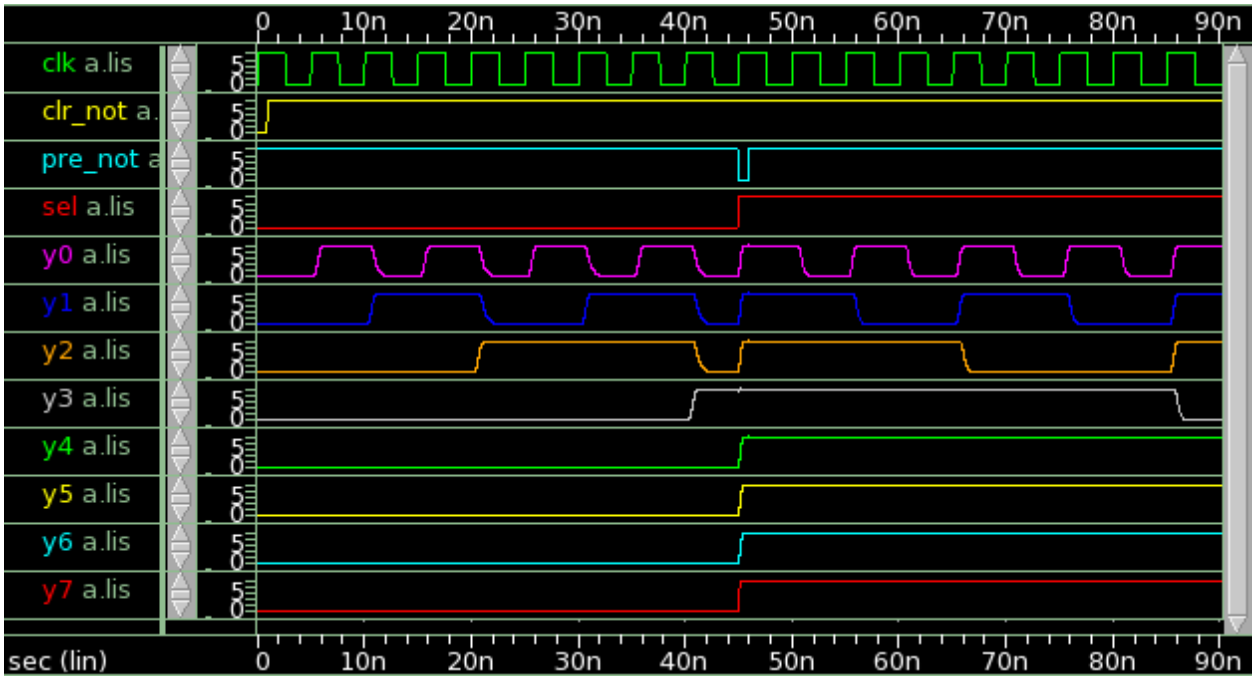
In order to test the shift register, we loaded parallel inputs and clocked a few times to show that each bit is being shifted properly.

8-Bit Bidirectional Shift registers-



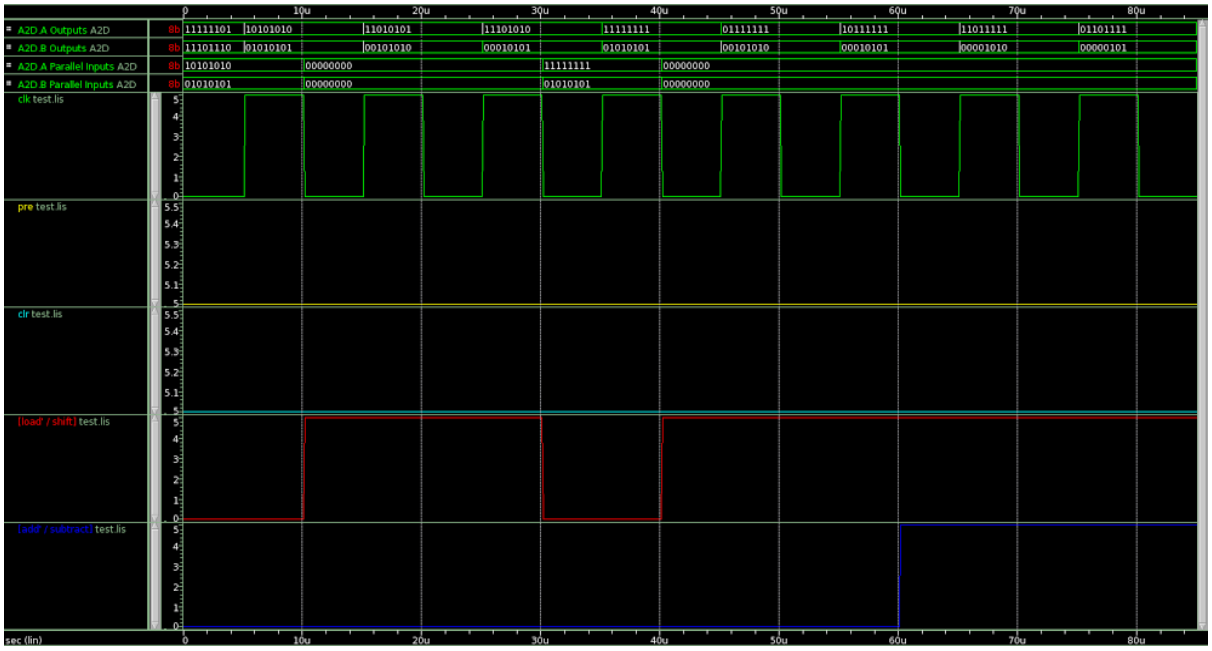
8 Bit Bidirectional Counter-

The bidirectional counter we tested by clearing, letting the counter count for some time, then doing a preset and count direction change and letting the counter count down for an equal amount of time. This demonstrates preset, clear, and the ability to change count direction.



8 Bit Serial Adder/Subtractor-

Likewise, we tested the adder/subtractor by running through a few loads and tests of the serial capability. This demonstrates that, while we didn't include a final shift register, which was optional, our design for the remainder performs correctly.



Conclusion & Feedback

We consider the lab a success since all the designs work.

The bounding areas for out circuits are :

390.6(width)x 324(length) - Serial Mathist
239.1(width)x 129.6 (length) - Count Chocula
160.8 (width)x 300 (length) - Shifty Shifterson