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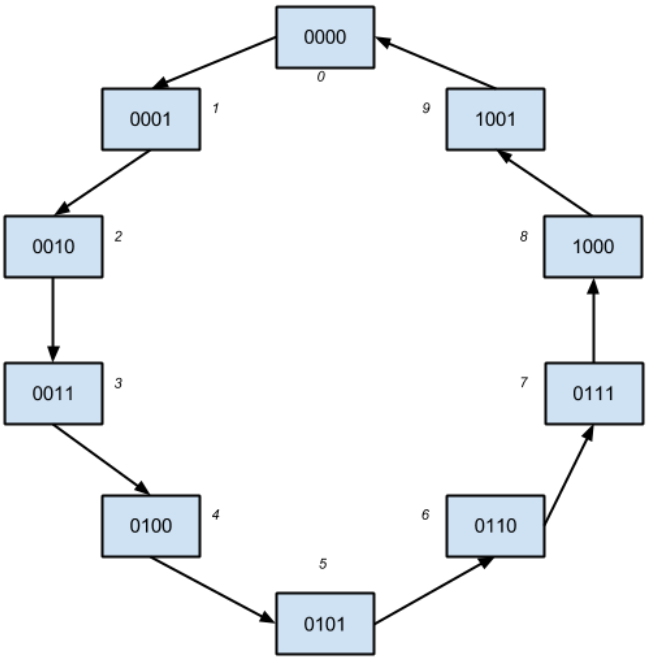
Homework 4

1. Design a 4-bit mod-10 up counter

A) Draw the Moore state diagram and next-state table



	Present State				Next State			
	A	B	C	D	A+	B+	C+	D+
0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	0
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	1	0	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	1	0
6	0	1	1	0	0	1	1	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	0	0	0	0

B) Implement the counter using T Flip-Flops

Flip-Flop Inputs

Ta	Tb	Tc	Td
0	0	0	1
0	0	1	1
0	0	0	1
0	1	1	1
0	0	0	1
0	0	1	1
0	0	0	1
1	1	1	1
0	0	0	1
1	0	0	1

Unused States

A	B	C	D	
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Ta

	A'B'	A'B	AB	AB'
C'D'			x	
C'D			x	1
CD		1	x	x
CD'			x	x

Tb

	A'B'	A'B	AB	AB'
C'D'			x	
C'D			x	
CD	1	1	x	x
CD'			x	x

Tc

	A'B'	A'B	AB	AB'
C'D'			x	
C'D	1	1	x	
CD	1	1	x	x
CD'			x	x

Next State Expressions

Ta = AD + BCD

Tb = CD

Tc = A'D

Td = 1

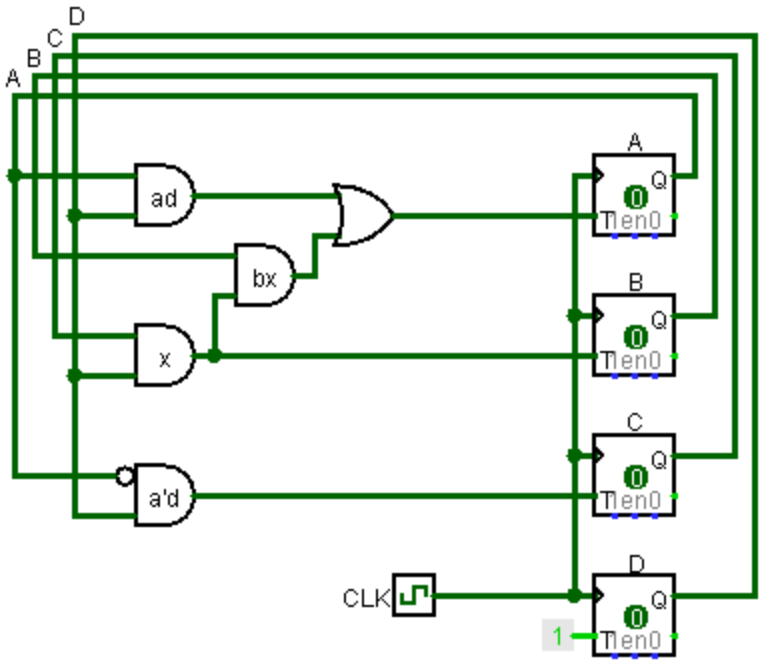
Let X = CD

Ta = AD + BX

Tb = X

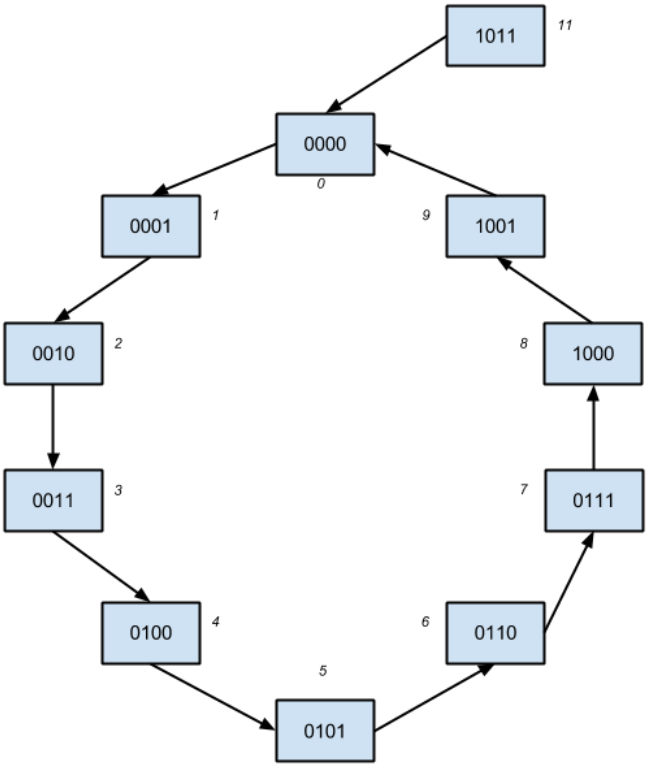
Tc = A'D

Td = 1



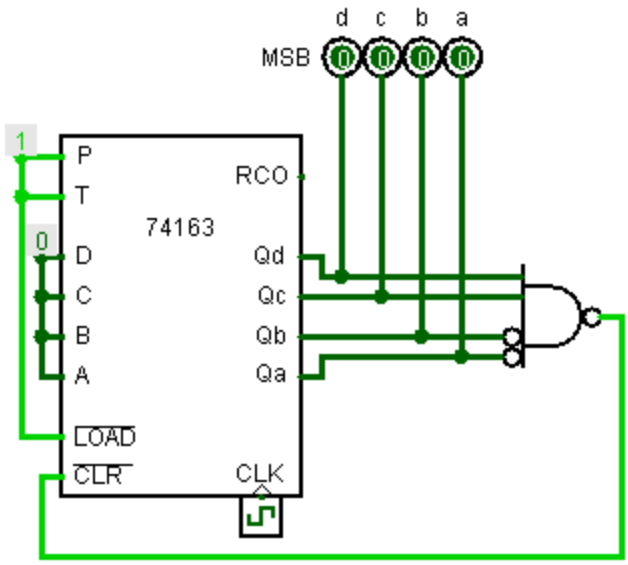
C) This specific counter implementation is a non-self starting counter due to the fact that not every possible state for a 4-bit binary word has a sequence of transitions that leads to a valid state, meaning there exists “unused” states. To avoid the possibility of the counter entering an invalid state upon start-up there needs to be an asserted “reset” to each of the four T Flip-Flops.

D) Draw a state diagram in which the circuit starts in the *unused* state 1011



2. Implement a base 13 up-counter using 74163

Given the value range for base 13 is 0 to 12 and the 74163 has a value range from 0 to 15 then the counter design should adhere to that of a “cutoff limit counter” where the combinational logic detects the 4-bit binary number 1100 and asserts an active low signal to the clear input of the 74163.

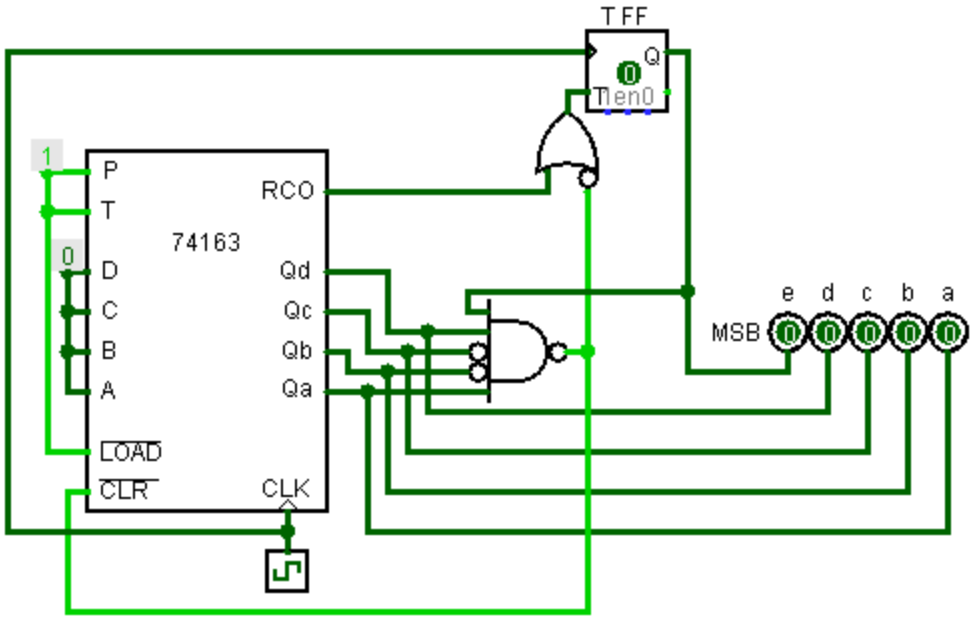


3. Implement a base 26 up-counter using a single 74163

The design for the circuit requires a total of 5-bits to detect the highest value of 25 (base 26 is 0 to 25) but the 74163 package is only 4-bits, thus the only valid states for the circuit would be those from 0 to 15. In order to represent all 5-bits an extra register is required to hold the data value of the most significant bit.

The MSB register's input should be driven by two special cases where the ripple carry output has been asserted high or the combinational logic that detects the value of 25 is asserted low. When the decimal value of the circuit exists in some state between 0 and 15 inclusive the output of the MSB register should be a logic "0" and when the decimal value of the circuit exists in some state between 16 and 25 inclusive the output of the MSB register should be a logic "1". To facilitate the toggle-like behavior of the MSB register a T Flip-Flop was introduced to the circuit.

The combinational logic that detects the decimal value of 25 is asserted low only when the current state of the MSB register is a logic "1" and the binary value of 1001 is present at the outputs Qd, Qc, Qb, and Qa.



4. Implement a 5-bit up/down, even/odd counter

For this circuit, the following logical values have been associated with the corresponding functionality.

Up = 1 / Down = 0
Even = 1 / Odd = 0

D Flip-Flops were chosen as the storage elements for the required 5-bits and each of their inputs is driven by an 8:1 multiplexer. The 8:1 MUX is controlled by three signals namely Reset, S1 (Up/Down), and S0 (Even/Odd). The inclusion of a reset signal ensures the D Flip-Flops are set to valid state when switching modes and when the reset signal is asserted high the D Flip-Flops perform a synchronous parallel load.

D Flip-Flop Inputs using 8:1 Multiplexer

Control Lines			Output	
RESET	S1	S0	Function	
0	0	0	DOWN, ODD	
0	0	1	DOWN, EVEN	
0	1	0	UP, ODD	
0	1	1	UP, EVEN	
1	0	0	LOAD 1 1 1 1 1	31
1	0	1	LOAD 1 1 1 1 0	30
1	1	0	LOAD 0 0 0 0 1	1
1	1	1	LOAD 0 0 0 0 0	0

Down / Odd Function

	Present State					Next State				
	E	D	C	B	A	E+	D+	C+	B+	A+
31	1	1	1	1	1	1	1	1	0	1
29	1	1	1	0	1	1	1	0	1	1
27	1	1	0	1	1	1	1	0	0	1
25	1	1	0	0	1	1	0	1	1	1
23	1	0	1	1	1	1	0	1	0	1
21	1	0	1	0	1	1	0	0	1	1
19	1	0	0	1	1	1	0	0	0	1
17	1	0	0	0	1	0	1	1	1	1
15	0	1	1	1	1	0	1	1	0	1
13	0	1	1	0	1	0	1	0	1	1
11	0	1	0	1	1	0	1	0	0	1
9	0	1	0	0	1	0	0	1	1	1
7	0	0	1	1	1	0	0	1	0	1
5	0	0	1	0	1	0	0	0	1	1
3	0	0	0	1	1	0	0	0	0	1
1	0	0	0	0	1	1	1	1	1	1

E+

E = 0

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A	1			
BA				
BA'	x	x	x	x

E = 1

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A		1	1	1
BA	1	1	1	1
BA'	x	x	x	x

D+

E = 0

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A	1		1	
BA			1	1
BA'	x	x	x	x

E = 1

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A	1		1	
BA			1	1
BA'	x	x	x	x

C+

E = 0

B'A' \ D'C'	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A	1			1
BA		1	1	
BA'	x	x	x	x

E = 1

B'A' \ D'C'	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A	1			1
BA		1	1	
BA'	x	x	x	x

Next State Expressions

E+ = E'D'C'B' + EB + EC + ED
D+ = D'C'B' + DC + DB
C+ = C'B' + CB
B+ = B'
A+ = 1

Let X = D'C'B'

E+ = E'D'C'B' + EB + EC + ED = E'X + EX' = E XOR X
D+ = D'C'B' + DC + DB = X + D(C + B)
C+ = C'B' + CB = C XNOR B
B+ = B'
A+ = 1

Down / Even Function

	Present State					Next State				
	E	D	C	B	A	E+	D+	C+	B+	A+
30	1	1	1	1	0	1	1	1	0	0
28	1	1	1	0	0	1	1	0	1	0
26	1	1	0	1	0	1	1	0	0	0
24	1	1	0	0	0	1	0	1	1	0
22	1	0	1	1	0	1	0	1	0	0
20	1	0	1	0	0	1	0	0	1	0
18	1	0	0	1	0	1	0	0	0	0
16	1	0	0	0	0	0	1	1	1	0
14	0	1	1	1	0	0	1	1	0	0
12	0	1	1	0	0	0	1	0	1	0
10	0	1	0	1	0	0	1	0	0	0
8	0	1	0	0	0	0	0	1	1	0
6	0	0	1	1	0	0	0	1	0	0
4	0	0	1	0	0	0	0	0	1	0
2	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	0

E+

E = 0

	D'C'	D'C	DC	DC'
B'A'	1			
B'A	x	x	x	x
BA	x	x	x	x
BA'				

E = 1

	D'C'	D'C	DC	DC'
B'A'		1	1	1
B'A	x	x	x	x
BA	x	x	x	x
BA'	1	1	1	1

D+

E = 0

	D'C'	D'C	DC	DC'
B'A'	1		1	
B'A	x	x	x	x
BA	x	x	x	x
BA'			1	1

E = 1

	D'C'	D'C	DC	DC'
B'A'	1		1	
B'A	x	x	x	x
BA	x	x	x	x
BA'			1	1

C+

E = 0

	D'C'	D'C	DC	DC'
B'A'	1			1
B'A	x	x	x	x
BA	x	x	x	x
BA'		1	1	

E = 1

	D'C'	D'C	DC	DC'
B'A'	1			1
B'A	x	x	x	x
BA	x	x	x	x
BA'		1	1	

Next State Expressions

E+ = E'D'C'B' + EB + EC + ED

D+ = D'C'B' + DC + DB

C+ = C'B' + CB

B+ = B'

A+ = 0

Let X = D'C'B'

E+ = E'D'C'B' + EB + EC + ED = E'X + EX' = E XOR X

D+ = D'C'B' + DC + DB = X + D(C + B)

C+ = C'B' + CB = C XNOR B

B+ = B'

A+ = 0

Up / Odd Function

	Present State					Next State				
	E	D	C	B	A	E+	D+	C+	B+	A+
1	0	0	0	0	1	0	0	0	1	1
3	0	0	0	1	1	0	0	1	0	1
5	0	0	1	0	1	0	0	1	1	1
7	0	0	1	1	1	0	1	0	0	1
9	0	1	0	0	1	0	1	0	1	1
11	0	1	0	1	1	0	1	1	0	1
13	0	1	1	0	1	0	1	1	1	1
15	0	1	1	1	1	1	0	0	0	1
17	1	0	0	0	1	1	0	0	1	1
19	1	0	0	1	1	1	0	1	0	1
21	1	0	1	0	1	1	0	1	1	1
23	1	0	1	1	1	1	1	0	0	1
25	1	1	0	0	1	1	1	0	1	1
27	1	1	0	1	1	1	1	1	0	1
29	1	1	1	0	1	1	1	1	1	1
31	1	1	1	1	1	0	0	0	0	1

E+

E = 0

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A				
BA			1	
BA'	x	x	x	x

E = 1

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A	1	1	1	1
BA	1	1		1
BA'	x	x	x	x

D+

E = 0

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A			1	1
BA		1		1
BA'	x	x	x	x

E = 1

	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A			1	1
BA		1		1
BA'	x	x	x	x

C+

E = 0

B'A' \ D'C'	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A		1	1	
BA	1			1
BA'	x	x	x	x

E = 1

B'A' \ D'C'	D'C'	D'C	DC	DC
B'A'	x	x	x	x
B'A		1	1	
BA	1			1
BA'	x	x	x	x

Next State Expressions

E+ = E'DCB + EC' + ED' + EB'
D+ = D'CB + DB' + DC'
C+ = C'B + CB''
B+ = B'
A+ = 1

Let X = DCB
Let Y = CB

E+ = E'DCB + EC' + ED' + EB' = E'X + EX' = E XOR X
D+ = D'CB + DB' + DC' = D'Y + DY' = D XOR Y
C+ = C'B + CB' = C XOR B
B+ = B'
A+ = 1

Up / Even Function

	Present State					Next State				
	E	D	C	B	A	E+	D+	C+	B+	A+
0	0	0	0	0	0	0	0	0	1	0
2	0	0	0	1	0	0	0	1	0	0
4	0	0	1	0	0	0	0	1	1	0
6	0	0	1	1	0	0	1	0	0	0
8	0	1	0	0	0	0	1	0	1	0
10	0	1	0	1	0	0	1	1	0	0
12	0	1	1	0	0	0	1	1	1	0
14	0	1	1	1	0	1	0	0	0	0
16	1	0	0	0	0	1	0	0	1	0
18	1	0	0	1	0	1	0	1	0	0
20	1	0	1	0	0	1	0	1	1	0
22	1	0	1	1	0	1	1	0	0	0
24	1	1	0	0	0	1	1	0	1	0
26	1	1	0	1	0	1	1	1	0	0
28	1	1	1	0	0	1	1	1	1	0
30	1	1	1	1	0	0	0	0	0	0

E+

E = 0

	D'C'	D'C	DC	DC'
B'A'				
B'A	x	x	x	x
BA	x	x	x	x
BA'			1	

E = 1

	D'C'	D'C	DC	DC'
B'A'	1	1	1	1
B'A	x	x	x	x
BA	x	x	x	x
BA'	1	1		1

D+

E = 0

	D'C'	D'C	DC	DC'
B'A'			1	1
B'A	x	x	x	x
BA	x	x	x	x
BA'		1		1

E = 1

	D'C'	D'C	DC	DC'
B'A'			1	1
B'A	x	x	x	x
BA	x	x	x	x
BA'		1		1

C+

E = 0

B'A' \ D'C'	D'C'	D'C	DC	DC'
B'A'		1	1	
B'A	x	x	x	x
BA	x	x	x	x
BA'	1			1

E = 1

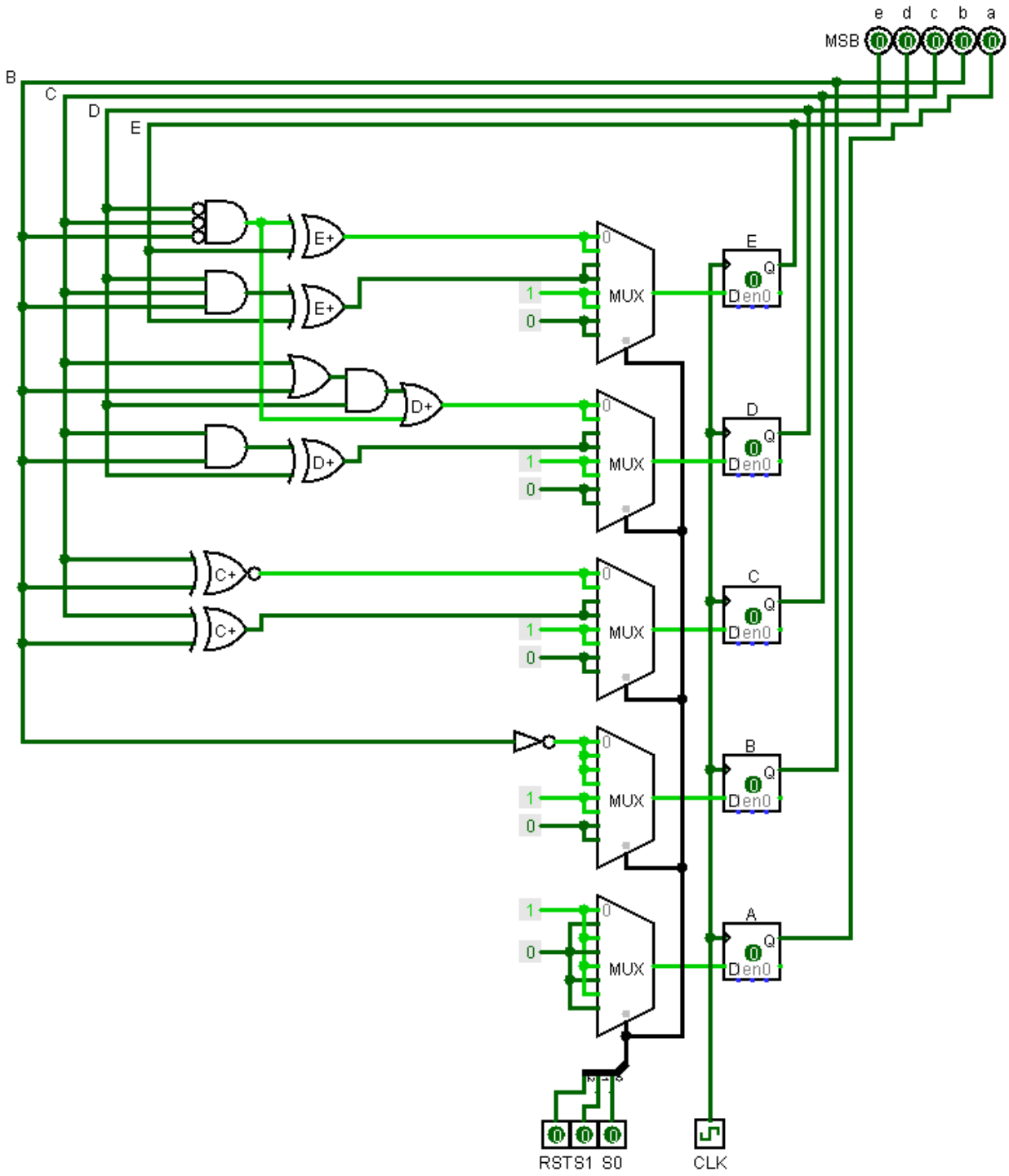
B'A' \ D'C'	D'C'	D'C	DC	DC'
B'A'		1	1	
B'A	x	x	x	x
BA	x	x	x	x
BA'	1			1

Next State Expressions

E+ = E'DCB + EC' + ED' + EB'
D+ = D'CB + DB' + DC'
C+ = C'B + CB''
B+ = B'
A+ = 0

Let X = DCB
Let Y = CB

E+ = E'DCB + EC' + ED' + EB' = E'X + EX' = E XOR X
D+ = D'CB + DB' + DC' = D'Y + DY' = D XOR Y
C+ = C'B + CB' = C XOR B
B+ = B'
A+ = 0


e d c b a
MSB
B
C
D
E
E+
E+
D+
D+
C+
C+
MUX
MUX
MUX
MUX
MUX
1
0
E
D
C
B
A
Q
Den0
RST
S1
S0
CLK

5. Provide the state diagram for a Moore machine with inputs X1 & X2 and output Z following the specifications listed on the assignment document.

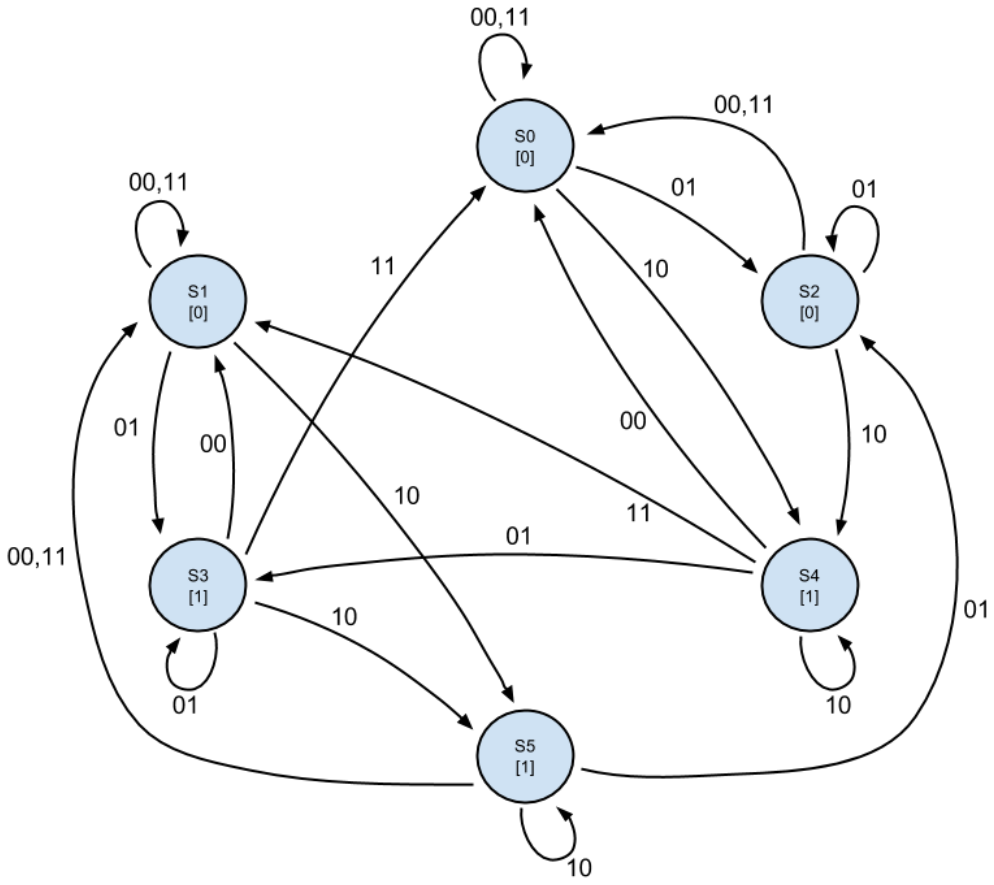
State Definitions

Inputs		Output	State
X1	X2	Z	
0	0	0	S0
0	0	1	S1
0	1	0	S2
0	1	1	S3
1	0	0	S4
1	0	1	S5
1	1	0	S0
1	1	1	S1

Note that the conditions in which the inputs do not change the current state of the output are given by states S0 and S1 and occur twice in the state definitions table.

State Table

Present State	X1+	X2+	Next State
S0	0	0	S0
	0	1	S2
	1	0	S4
	1	1	S0
S1	0	0	S1
	0	1	S3
	1	0	S5
	1	1	S1
S2	0	0	S0
	0	1	S2
	1	0	S4
	1	1	S0
S3	0	0	S1
	0	1	S3
	1	0	S5
	1	1	S0
S4	0	0	S0
	0	1	S3
	1	0	S4
	1	1	S1
S5	0	0	S1
	0	1	S2
	1	0	S5
	1	1	S1



6. A sequential circuit has one input and one output, provide the Mealy state diagram for each of the following cases.

A) Output Z toggles if the total number of logic ones is odd

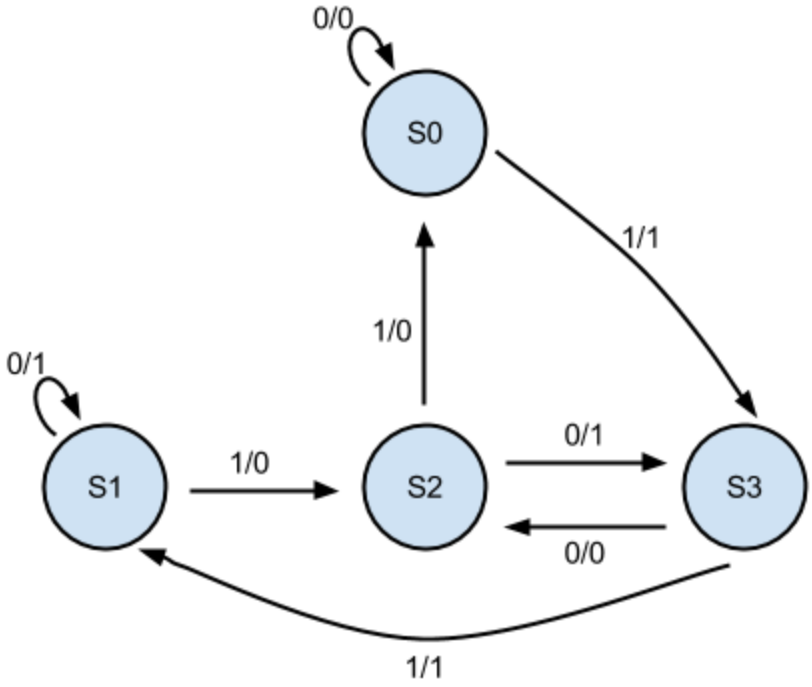
State Definitions

X	Z	State
0	0	S0
0	1	S1
1	0	S2
1	1	S3

X : 0 is even, 1 is odd

State Table

Present State	X+	Next State	Output Z
S0	0	S0	0
	1	S3	1
S1	0	S1	1
	1	S2	0
S2	0	S3	1
	1	S0	0
S3	0	S2	0
	1	S1	1



B) Output Z = 1 if and only if the total number of logic ones is divisible by 2

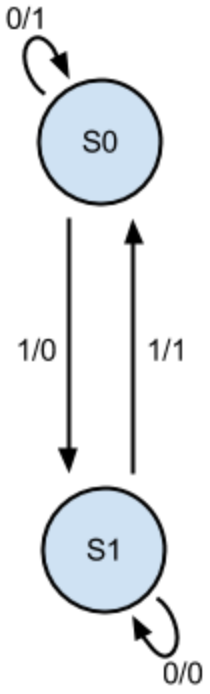
State Definitions

X	Z	State
0	1	S0
1	0	S1

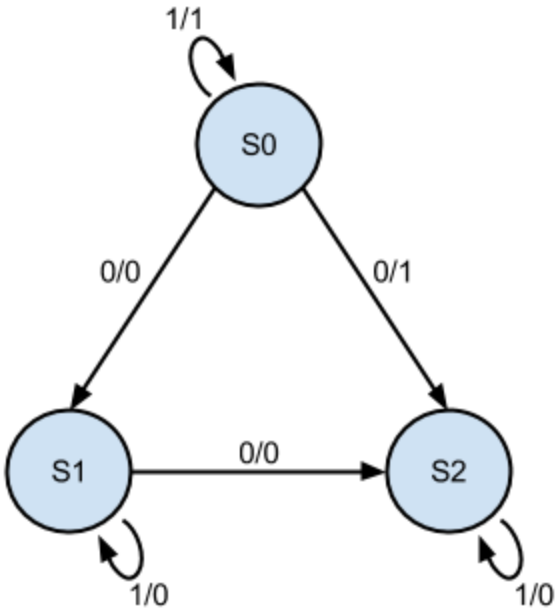
X : 0 is yes, 1 is no

State Table

Present State	X+	Next State	Output Z
S0	0	S0	1
	1	S1	0
S1	0	S1	0
	1	S0	1



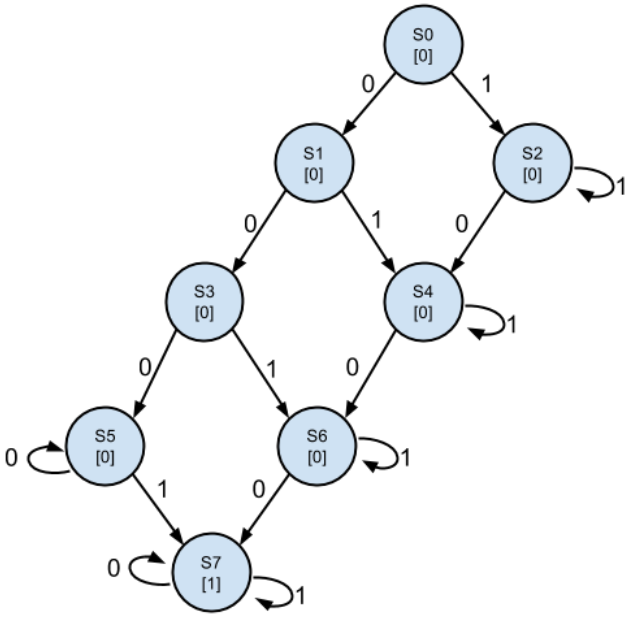
C) Output Z = 1 if the total number of logic zeros is divisible by 3.



7. A finite state machine has one input and one output. Implement the specifications as a Moore machine and provide a state diagram along with a state transition table.

State Table

Present State	X+	Next State	Output (Z)
S0	0	S1	0
	1	S2	0
S1	0	S3	0
	1	S4	0
S2	0	S4	0
	1	S2	0
S3	0	S5	0
	1	S6	0
S4	0	S6	0
	1	S4	0
S5	0	S5	0
	1	S7	0
S6	0	S7	0
	1	S6	0
S7	0	S7	1
	1	S7	1


S0
[0]
S1
[0]
S2
[0]
S3
[0]
S4
[0]
S5
[0]
S6
[0]
S7
[1]
0
1