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CMOS-VLSI DESIGN LAB 02

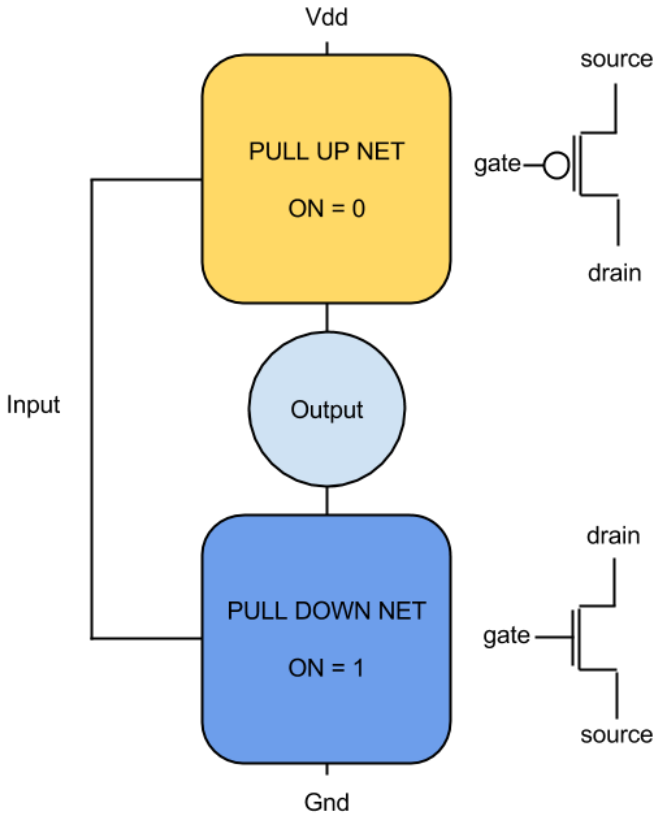
Introduction & Background

Designing VLSI systems with CMOS technology can be accomplished efficiently and accurately using computer-aided design software such as Cadence's Virtuoso Designer Suite, a highly sophisticated software package used predominantly throughout the semiconductor industry to synthesize and simulate integrated circuits.

To be proficient in the design and verification of CMOS circuits it is necessary to fully understand the key features of Virtuoso, specifically the "Schematic Capture" and "Layout" modes.

In this lab it was required that both a schematic design and layout design be produced and then verified using the DRC rules listed in the lab documentation "Deus Ex". After design verification, a netlist of the circuit was created and implemented with HSPICE simulation algorithms using hand generated SPICE decks and vector files, if appropriate.

Before beginning the design process of the lab a fundamental understanding of the CMOS design scheme was necessary. A diagram was drawn to facilitate the learning process and use as reference. The diagram lists the key concepts of a complementary pair of transistors, a pull-down and pull-up network, output in the middle, inclusion of voltage source and circuit ground, etc…

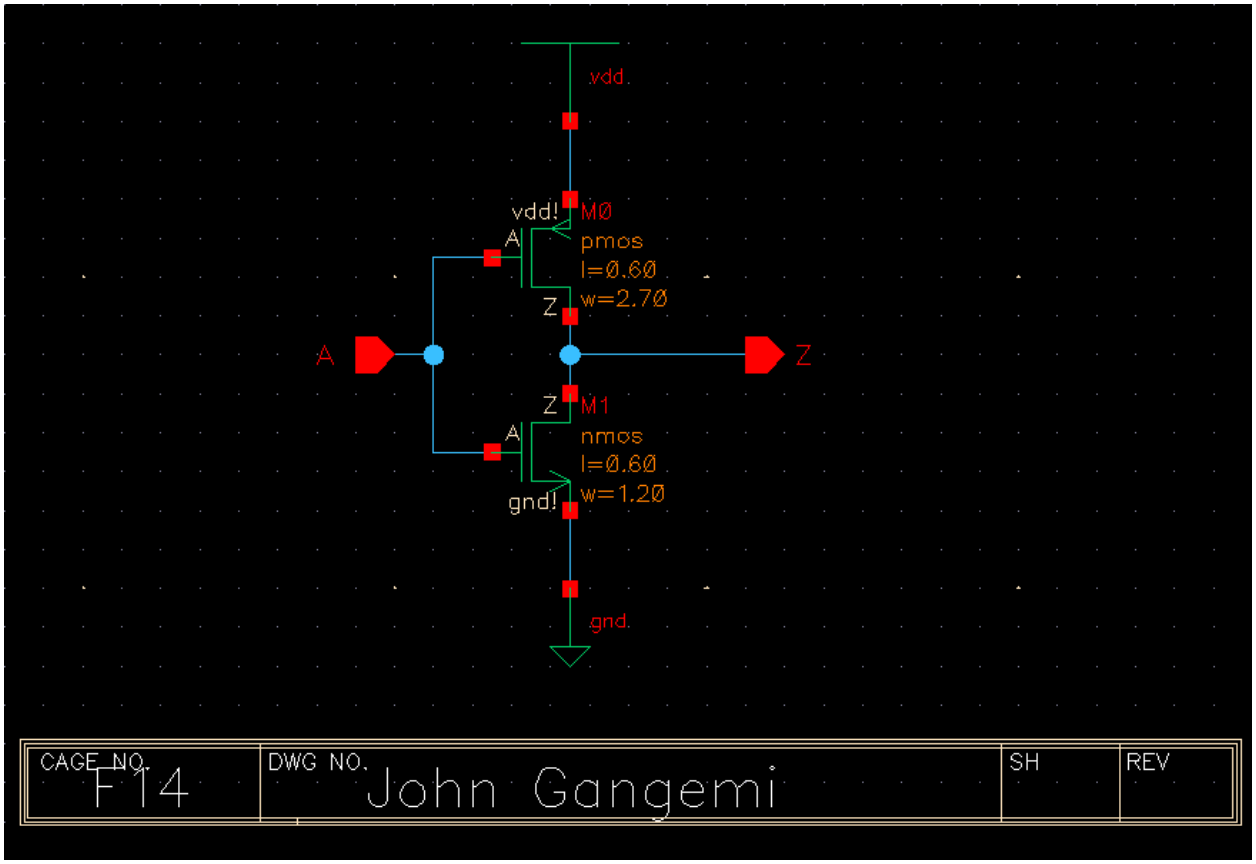


Design Process

Inverter Schematic

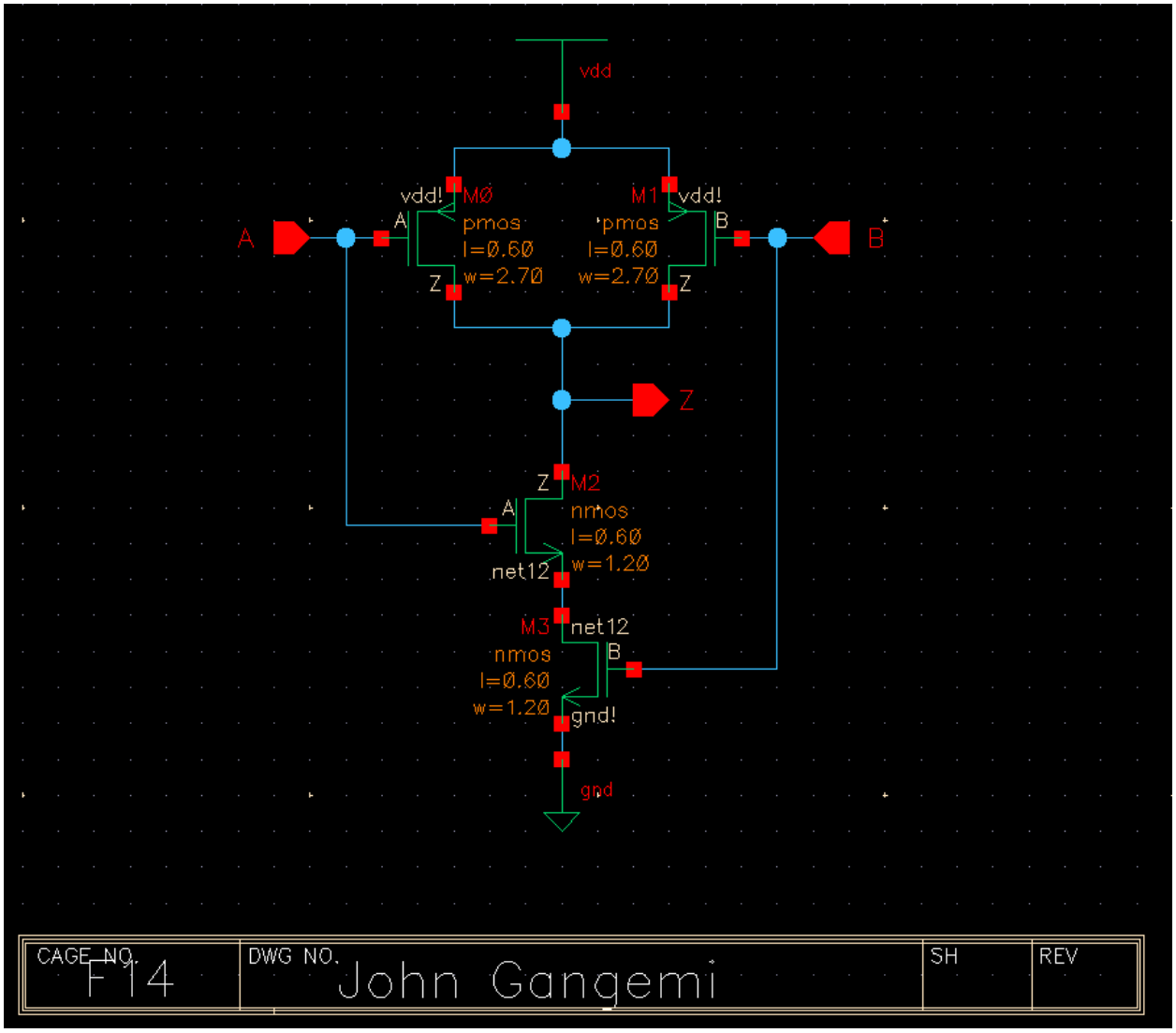
Figuring out how to use transistors to represent an inverter in a complementary process is a rather simple solution. It was observed that for both the pull-up and pull-down networks of the complementary process the circuit is either sourcing (passing through Vdd) or sinking (exposing path to ground) current.

Therefore the inverter schematic is a complementary pair of transistors with a common input (gate voltage).



2-NAND Schematic

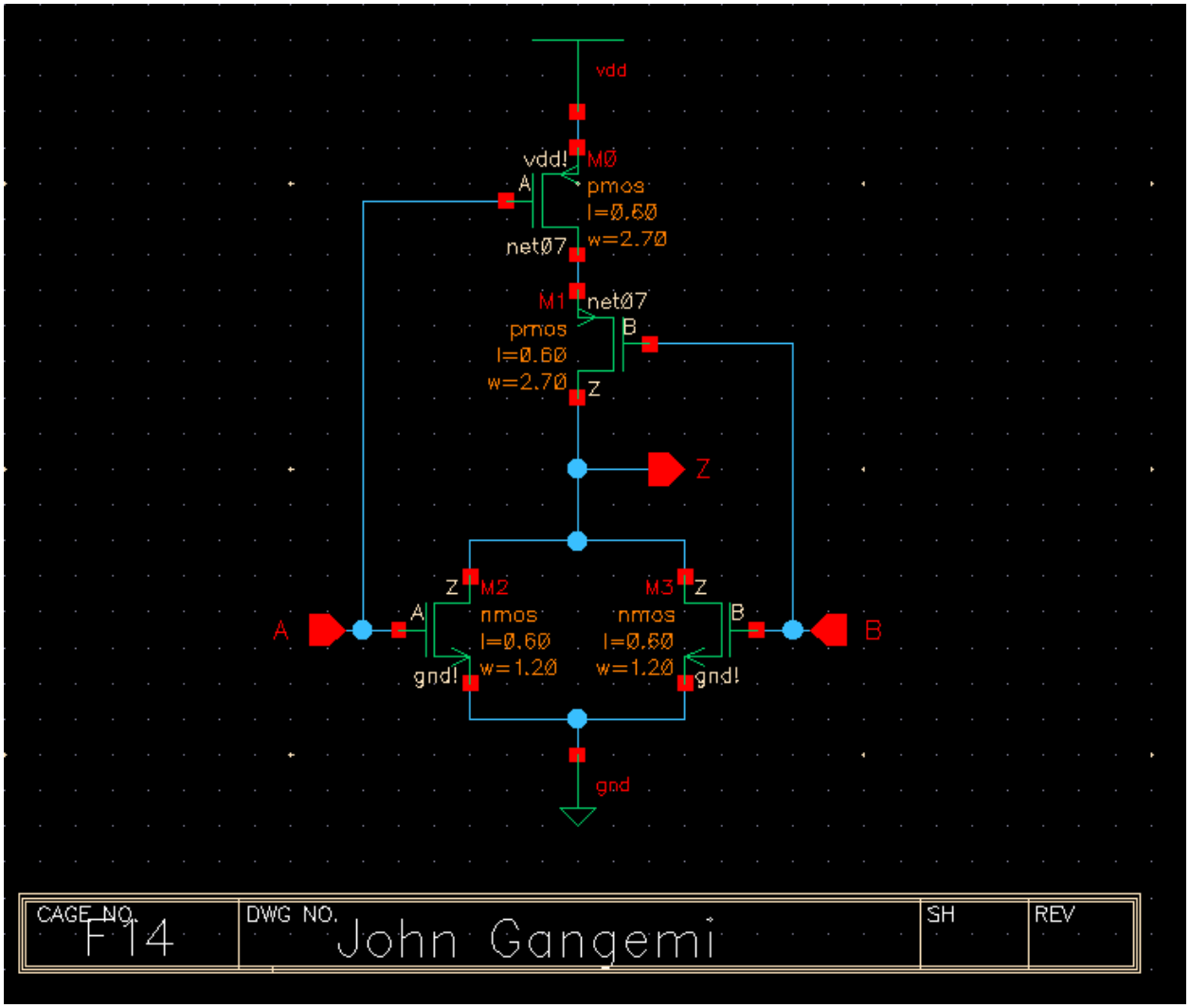
For a two input NAND gate the output logic is false (circuit will sink current) only in which both inputs (gate voltages) are logic 1 (high gate voltage). This dependent nature between the two gates describes a “series” characteristic in the pull-down network, therefore the corresponding compliment in the pull-up network is a “parallel” characteristic.



The two inputs in this schematic are labeled A and B whereas the output node is labeled Z. The parallel transistors in the pull-up network source current when either input is logic 0 (low gate voltage).

2-NOR Schematic

For a two input NOR gate the output logic is true (circuit will source current) only in which both inputs (gate voltages) are logic 0 (low gate voltage). This dependent nature between the two gates describes a “series” characteristic in the pull-up network, therefore the corresponding compliment in the pull-down network is a “parallel” characteristic.

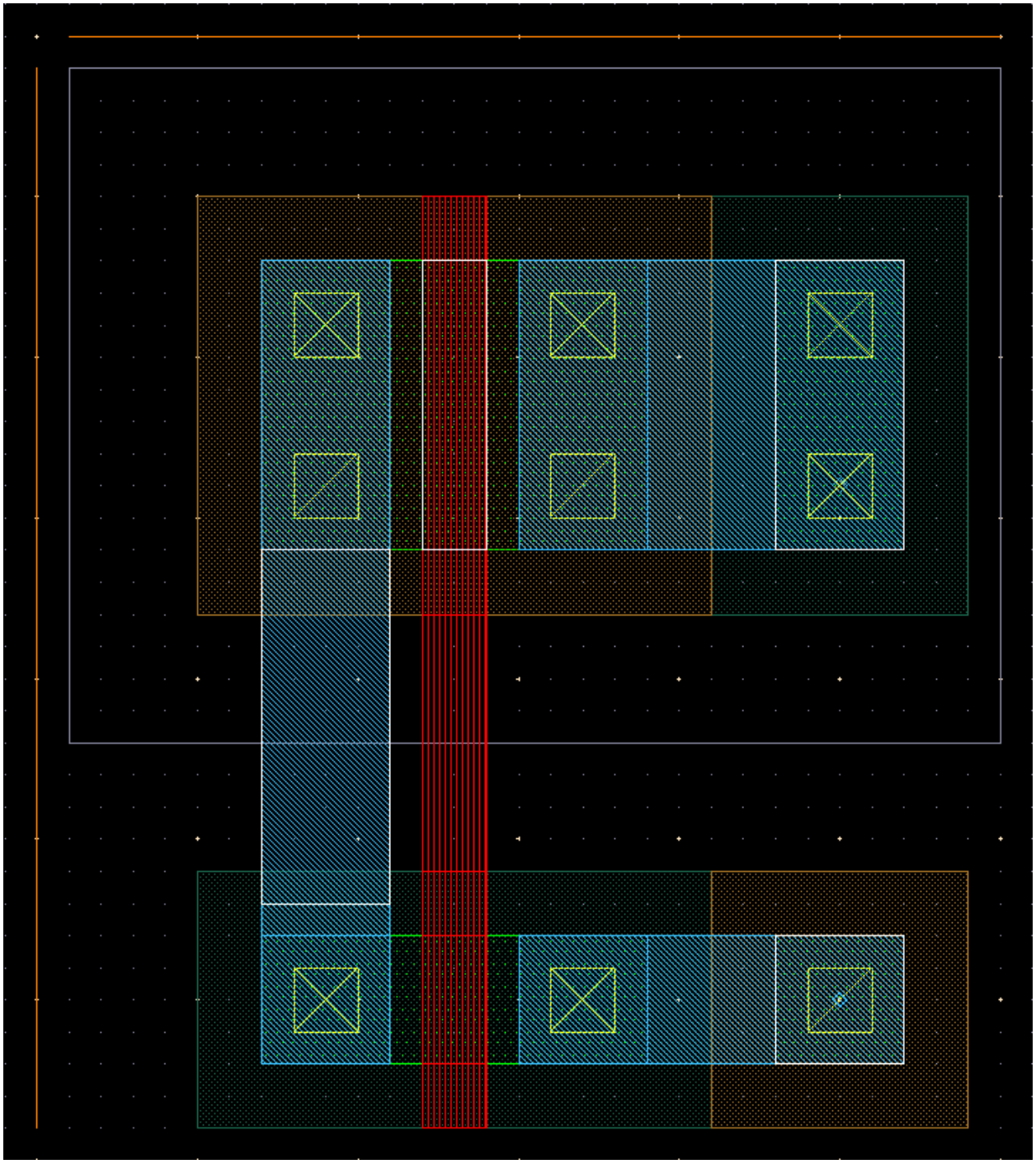


The two inputs in this schematic are labeled A and B whereas the output node is labeled Z. The parallel transistors in the pull-down network sink current when either input is logic 1 (high gate voltage).

Inverter Layout

Per instruction from the lab assistants and the design documentation “Deus Ex” the process of creating a “top-down” view of the pMOS and nMOS transistor was accomplished by using the pre designed library models provided with little modification necessary.

The metal interconnects between the transistors were established and the correct placement of the circuit pins (inputs/output/sources) drawn using the appropriate material layer.

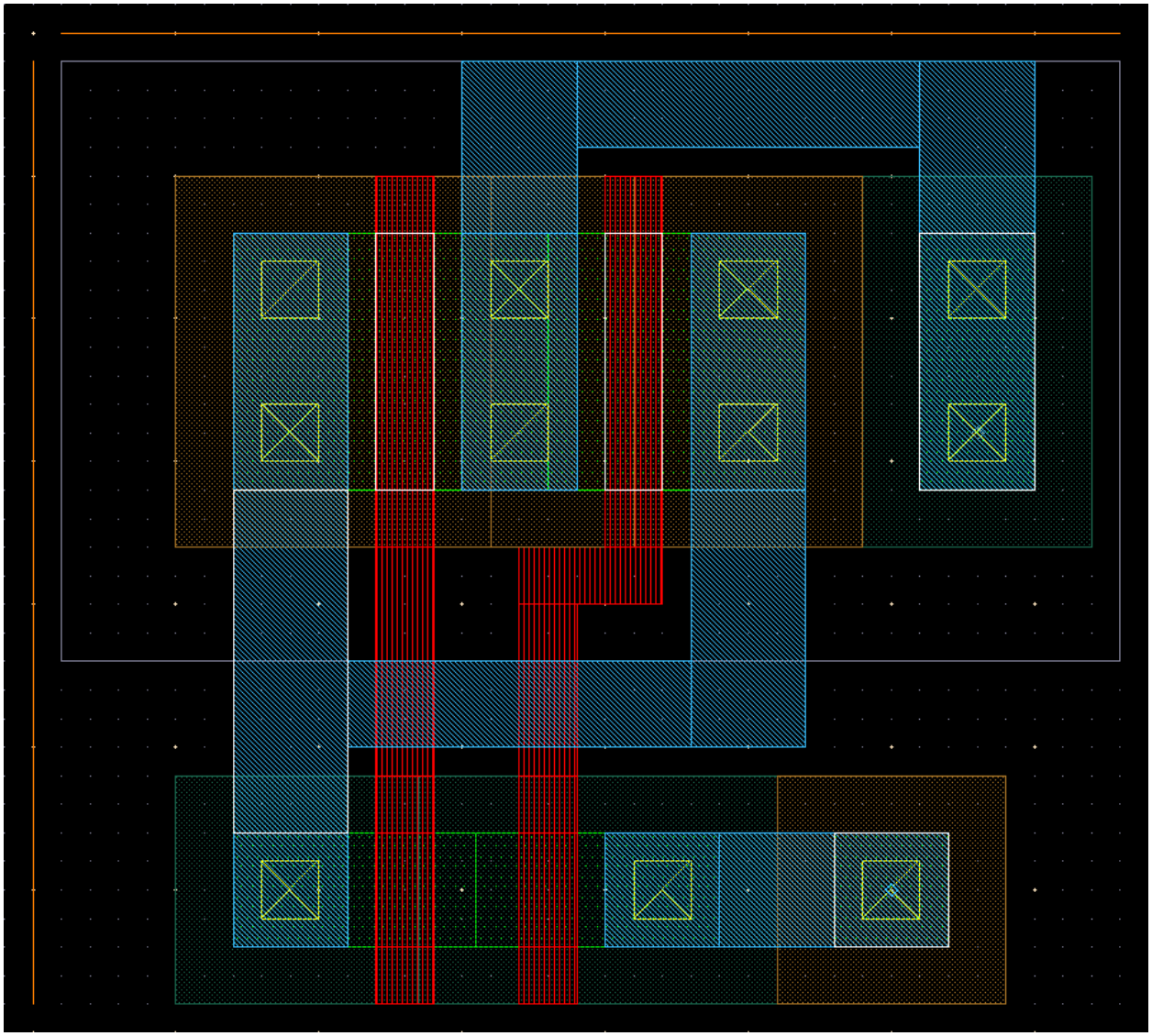


The layout pictured above is built on top of a p-type bulk (black background) where the pMOS is in the top half and the nMOS is in the lower half. Accordingly the pMOS is surrounded by a n-well that is sized to comply with the DRC rules. Both a p-tap (nMOS) and n-tap (pMOS) show the connections to ground and vdd respectively. Blue rectangles represent the metal layer, where the metal interconnect between the two transistors is the drain of both, likewise the output pin is placed in this area. The red layer is the poly-silicon and represent the transistors' input. A subtle green layer is the active region the transistor.

This active region is a “path” from source to drain and represents the flow of holes in pMOS and the flow of electrons in nMOS devices given the gate voltage is greater than or equal to the transistor’s threshold voltage.

The bounding area of this particular design is 8.7 units in length and 9.9 units in width.

2-NAND Layout



First procedure for the layout was to create the pMOS transistor in compliance with the DRC rules, this particular transistor required a large n-well thus the limiting factor in miniaturization of the circuit for the length.

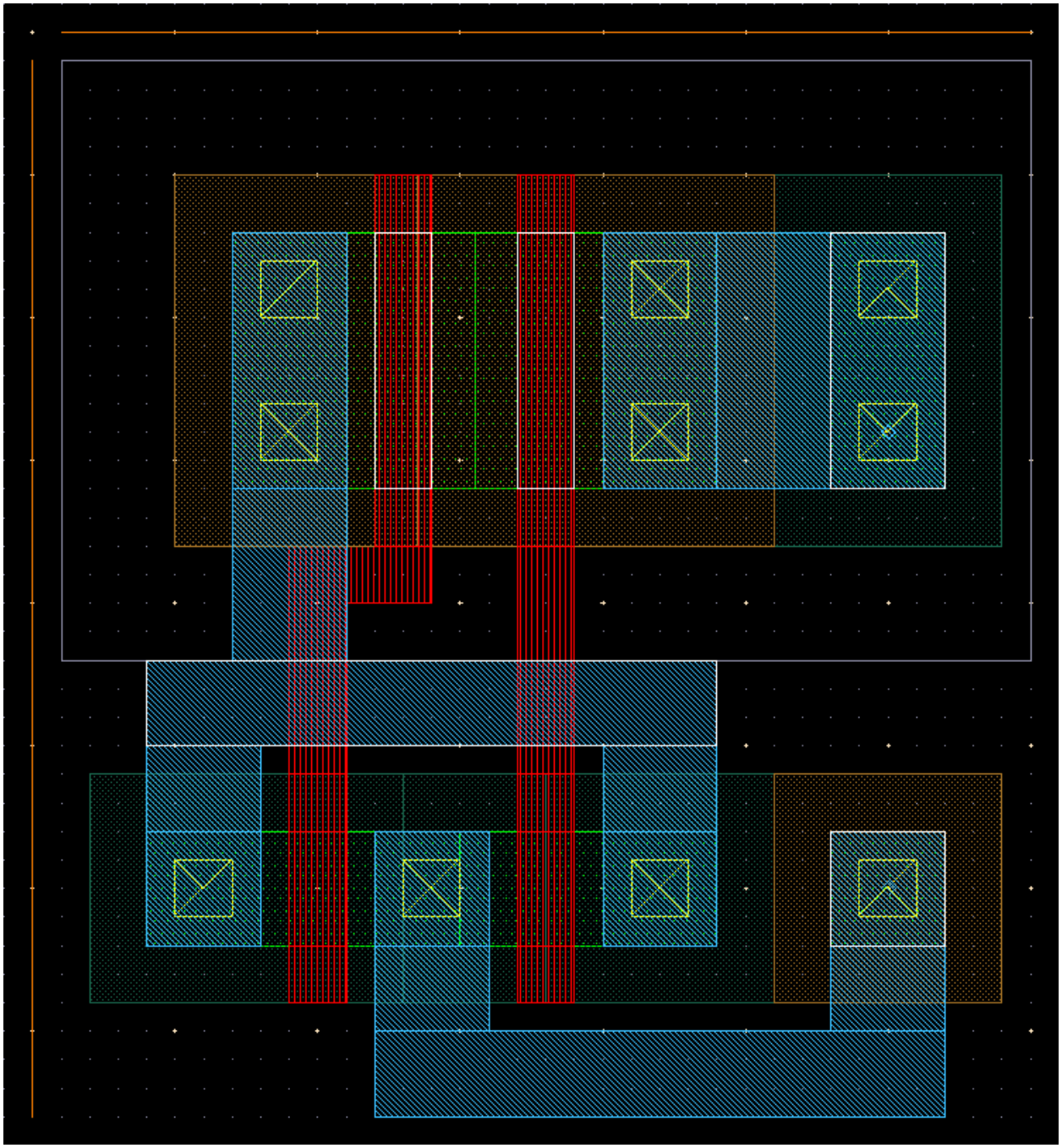
The next task was to complete the implementation of the nMOS transistor. The nMOS n+ layer must be at least 4 lambda from the n-well of the pMOS to meet the minimum

bounding length listed for the lab, however an issue with the spacing of metal interconnects arises. In order to solve the dilemma between metal interconnects being too close to each other they were made only 3 lambda wide (minimum spec). This solution was only necessary for the connection between the two drain wells of the pMOS and the n-tap to the source well of the pMOS.

It is clearly shown that the gate layers for the nMOS are in series and source from the p-tap which is connected to the circuit ground by a metal1 layer pin. This provides the corresponding logic 0 when both gate voltages are high.

The bounding area of this particular design is 11.1 units in length and 9.9 units in width.

2-NOR Layout



The layout for the NOR circuit is the exact opposite of the layout for the NAND circuit. Likewise the n-well of the pMOS transistor is the limiting factor in the size of the complete circuit. Also certain metal layer connections needed to be adjusted to the minimum spec of 3 lambda to avoid DRC issues.

In the pull-up network it can be observed that the gate layers are in series as this leads to the desired output logic 1 when both gate voltages are high.

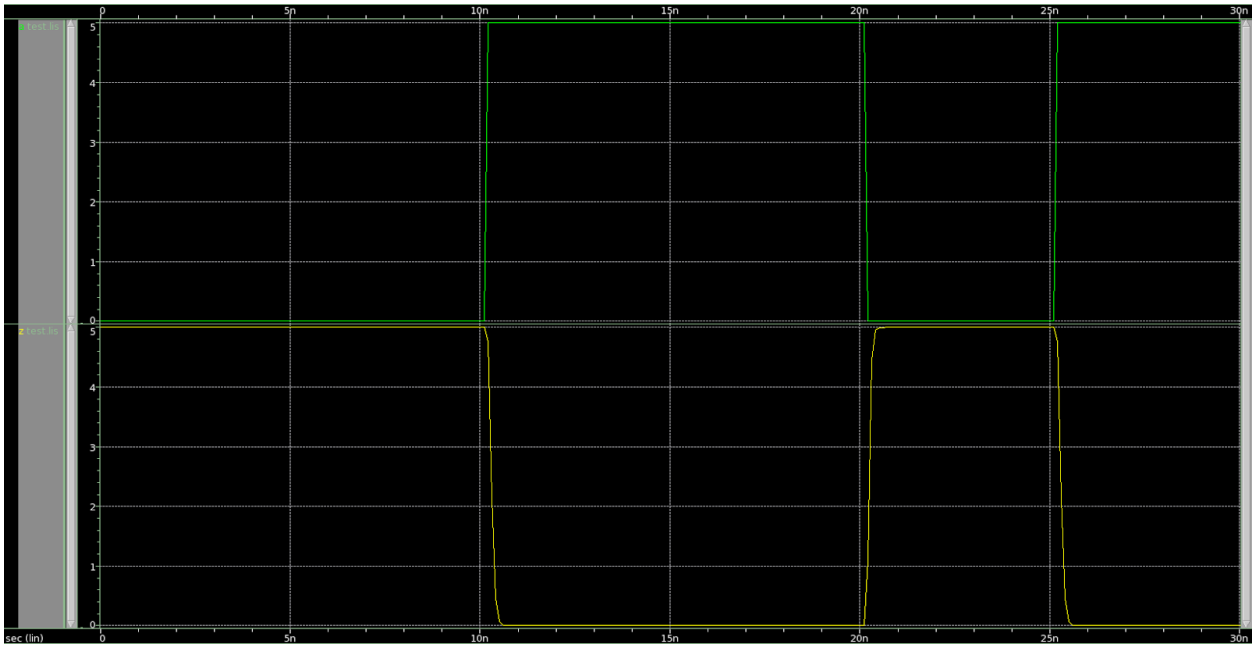
The bounding area of this particular design is 10.2 units in length and 11.2 units in width.

Testing Process

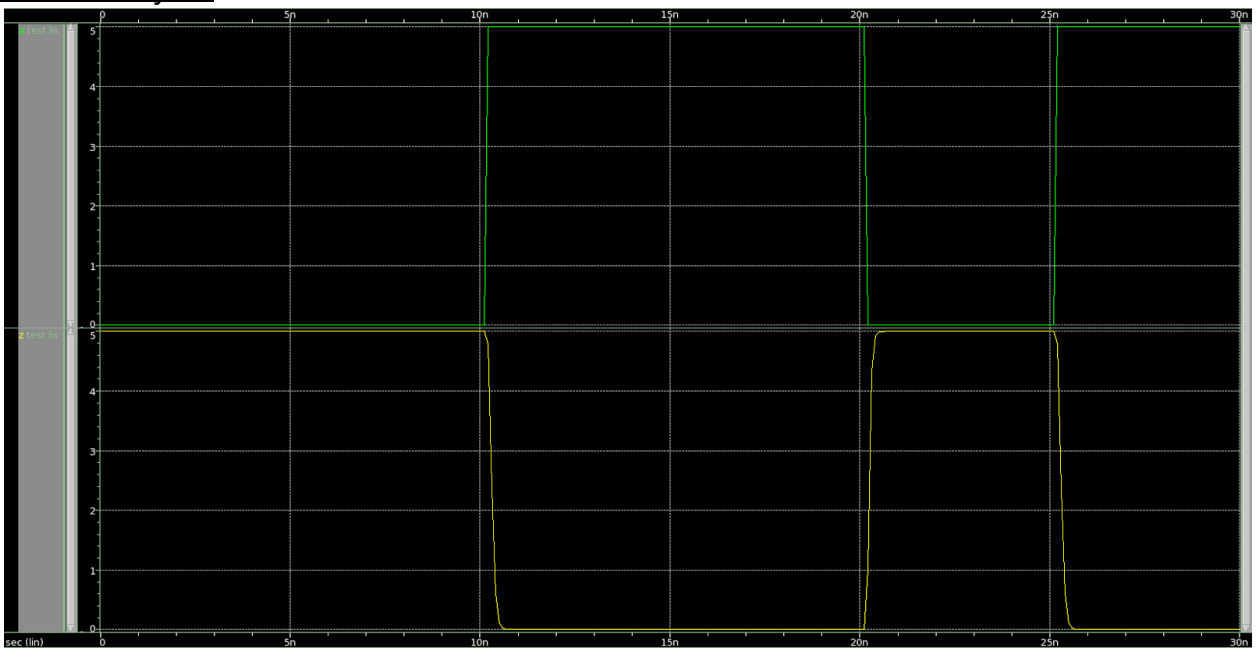
All tests performed with HSPICE were done so using a vector stimulus and the data provided for the vector described each particular circuit's truth table with 5 and 10 nanosecond intervals.

The test were performed in such a manner as this allowed exhaustive testing of each circuit, meaning each possible combination of inputs were tested. Given below are the waveforms for both schematic and layout implementations of each circuit.

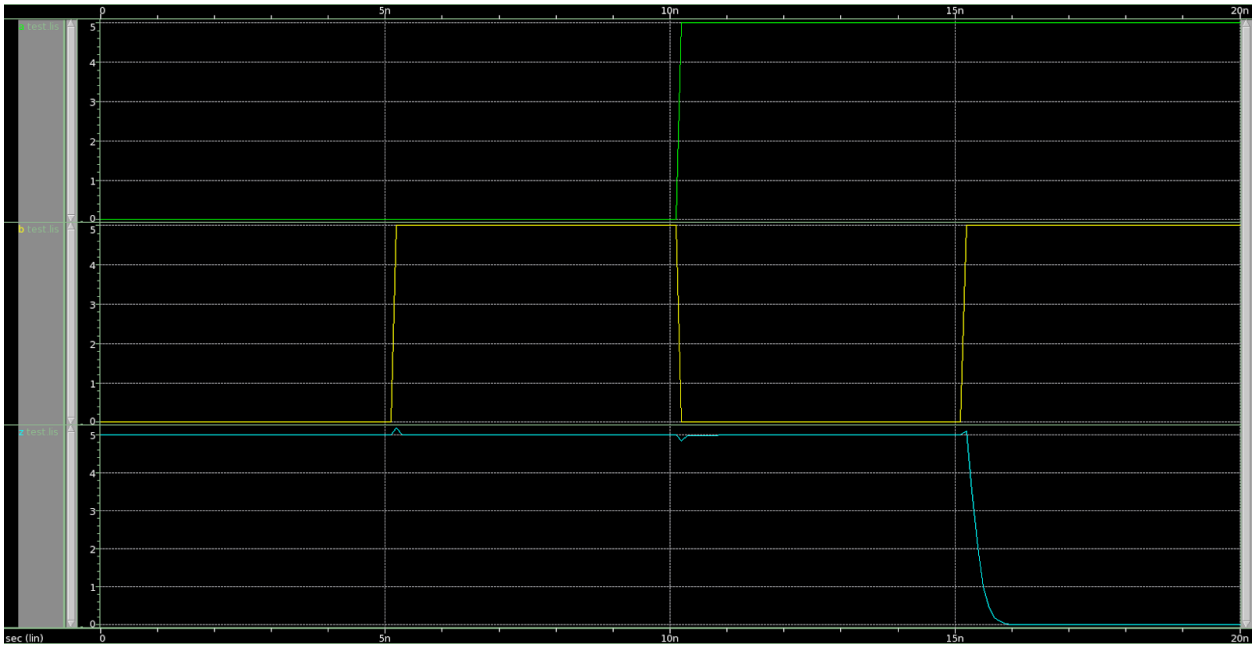
Inverter Schematic



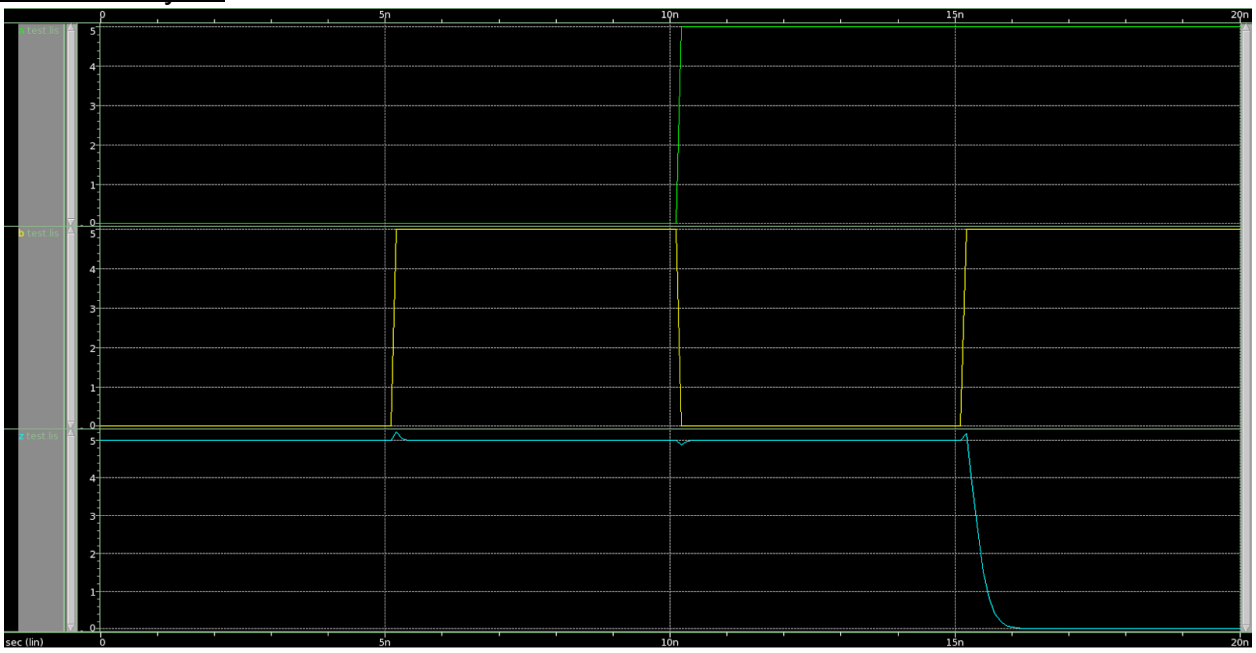
Inverter Layout



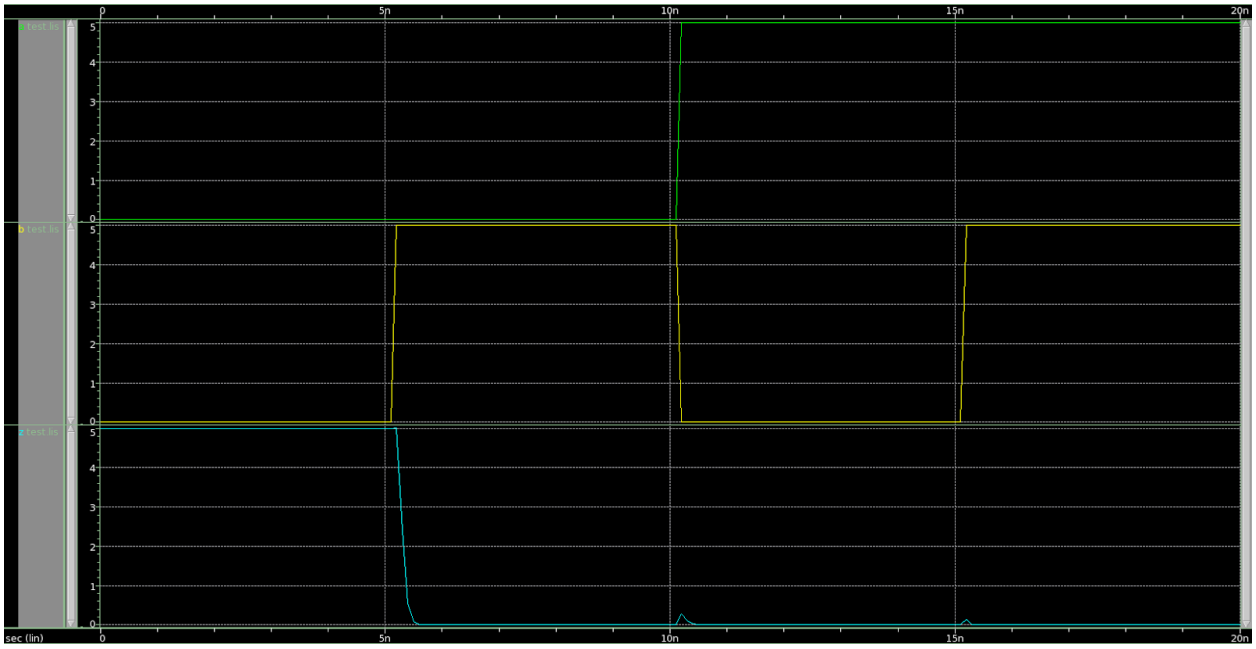
2-NAND Schematic



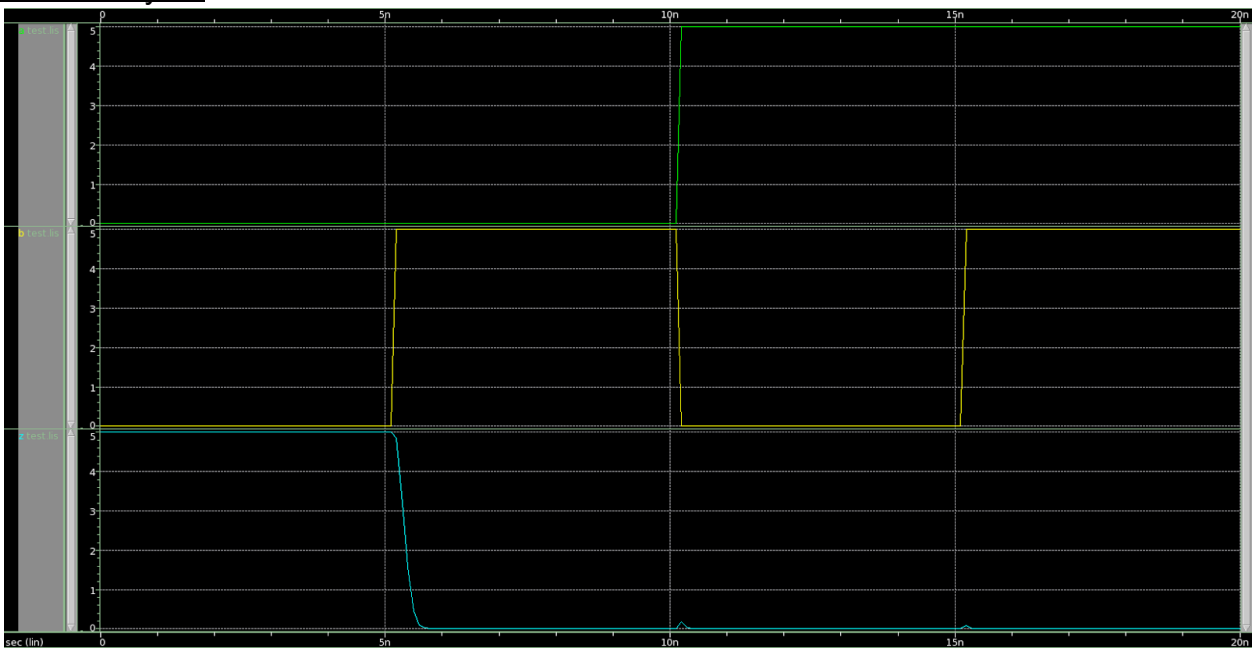
2-NAND Layout



2-NOR Schematic



2-NOR Layout



All waveforms exhibit the correct transitions in the output given the inputs. There are some very small glitches in the output for each that occur when both inputs are changing their state.

Note: The blue waveform for the NAND and NOR is the output, the yellow waveform for the Inverter is the output.

Discussion

Each circuit created in the schematic and layout modes were verified to be in accordance with the DRC rules and lead to successful netlist generation. The netlist gave desired results when stimulated using a vector table created based on the circuits truth table.

In doing the lab it was noticed that the CMOS structure of the NAND and NOR circuits are exact opposites in terms of their designs. Also the simplified nature of the NAND and NOR circuits leads to the suggestion that all future circuits be NAND/NOR only implementations.

Having finished all the layouts prior to the discussion post in Canvas regarding bounding areas, it was noticed there was room for improvement. Managing to get all circuits within the guidelines was a real accomplishment for this engineer.

In regard to the schematic and layout waveforms generated being identical, or practically identical in terms of nanoseconds it is reassurance that the designs for each circuit are correct.

Bounding area is important in the realm of layout as it is preferred to have circuits as minimal in size (both and length and width) as possible. This design ideology provides the possibility of instancing more circuits in a given space, thus reducing cost and improving transistor count per chip.