CIS4930.002
VLSI Design Automation
Summer C – 2015

Term Project: Part A

Due: *Friday, June 12th, 2015*
Submit Code to Canvas by 11:59 PM

Demo: *Friday, June 12th, 2015*
During Class

Maximum Group Size: TBD

Project Description:

You will be provided sizing guides for VLSI circuits that were made using the On-Semiconductor 0.5μ CMOS fabrication technology (AMI05), used in the CMOS-VLSI Design course. In addition to the sizing guides for these cells, you will be provided a basic information about the padframe (Tanner-EDA Hi-ESD Padframe) used for implementation and fabrication of CMOS-VLSI Design Lab circuits.

In order to complete the project you will be provided the following files: (1) cell library information (Length, Width, Pin I/O, etc...), (2) padframe information (Area, wire rules, etc...) and (3) a structural netlist composed of cell names from (1).

The requirements for this project are:

- Design the Data Structures Needed to Represent the Information from (1), (2), and (3).
- Perform Design Partitioning on (3) using Two-Way Partitioning.*

*Note: The choice of algorithm to implement is at the discretion of the group.

Files (1) and (2) can be found on canvas along with several example files for (3).