CIS4930.002
VLSI Design Automation
Summer C – 2015

Term Project: Part B

Due: *Friday, July 17th, 2015*
Submit Code to Canvas by 11:59 PM

Demo: *Friday, July 17th, 2015*
During Class

Maximum Group Size: TBD

Project Description:

You will be provided sizing guides for VLSI circuits that were made using the On-Semiconductor 0.5μ CMOS fabrication technology (AMI05), used in the CMOS-VLSI Design course. In addition to the sizing guides for these cells, you will be provided a basic diagram of the padframe (Tanner-EDA Hi-ESD Padframe) used for implementation and fabrication of CMOS-VLSI Design Lab circuits.

In order to complete Part B of the term project you will continue to build your code from Part A.

The requirements for this project are:

- Using the Partitions Created in Part A and Gate Sizes, perform Floorplanning for both the slices and padframe*
- Perform placement of the floorplans.
- Generate resulting data.

*Note: The criteria for Floorplanning optimization will be (1) Minimize Area.
The criteria for the placement of partitions within padframe slices should be to (1) Minimize the Wire Length for Routing. Placement of padframe slices into the padframe should consider both of these metrics.

Examples of the resulting data that should be generated can be found on canvas.