CDA 3201L – CLD Laboratory
Final Lab Project: 3-story Elevator Controller
(Due July 17th, 2014)

Objective:

Design and implement a finite state machine that controls the operation of an elevator in a 3-story building. The finite state machine (FSM) has 5 inputs: reset (takes device to idle state), start (enables operation of elevator), up (moves up one floor at a time), down (moves down one floor at a time), setAlarm, and run (extra credit). The FSM has three outputs: door (if door == 0, door is closed, if door == 1, door is open), alarm, floor (display floor is the elevator is currently on). The operation of the device is as follows:

- The device must begin in an idle state in which the elevator is on the first floor with the door open and the elevator alarm disabled. After the start input is set, the device will be enabled for operation. Until then, the device must stay on the first floor with the door open, alarm off.
- Setting the start input will enable the device for operation.
- Setting either the up or down inputs will trigger 3 events:
    1. The door must close
    2. The elevator will move up/down one floor
    3. Once it reaches the next floor, the door must remain open.
    - Note: This is not a magical elevator and cannot wrap around from the third floor to the first floor or vice-versa.
- Setting the reset input will asynchronously put the elevator back in its idle state (see first bullet).
- Setting the setAlarm input will have two effects:
    - The elevator door must close, and the elevator will remain on that floor until the alarm is disabled.
    - An alarm light will begin to flash.
- **Extra Credit** (+5 pts): Setting the run input will trigger the following events:
    - The door (if open) will close.
    - The elevator will traverse to the next floor (can start going either up or down)
    - The door will open
    - The door will close
    - The elevator will traverse to the next floor
        - If it is the top or bottom floor, it will reverse directions and continue repeating this same pattern.
- The floor that the elevator currently resides will be displayed on a 7-segment display and Binary-BCD Decoder (74LS247N).
- The (flashing) alarm light will be displayed on an LED.

Note: When testing your circuit on the breadboard, use the SLOWEST clock possible.

Deliverables:

1) You must demonstrate the functional correctness of this lab on the breadboard, per usual, to get full credit for this portion. Do yourself a favor and build this design in Logisim and simulate before spending your time implementing it on the breadboard.

2) *Optionally*, you may submit a draft of your design, along with any questions or issues that you

might have, and you will receive feedback from the instructor. The draft is due on Sunday July 6th, and you must submit it through Canvas.

3) You must implement this elevator controller in Verilog (without the binary – BCD display component). You will have to create a test bench for this program – use the test bench from last week's lab as a reference. Please comment your code. Submit a working Verilog simulation program file with your report.

4) You will submit a final report (per usual) in the same format as other lab assignments. In the Purpose/Objective section, thoroughly describe (in your own words, DO NOT copy paste from the assignment document) the objective and purpose of this assignment. In the Design section, Show all design details: truth tables, logic-level diagrams, Logisim screenshots, state machine diagrams, transition tables, K-maps, timing diagrams, verbal descriptions of your design intentions, etc. BE THOROUGH! Also, please be sure to include all of your test cases verified and any pertinent observations regarding the functional operation of your design.
Important: Always state your assumptions. If you make an assumption in your design (for example, if the specification does not cover a certain scenario), state the assumption and justify your reasoning as to why your design decision makes sense. Finally, pay special attention to your conclusion. In it, you should summarize your experiment, the lessons learnt, and possibly talk about experiments/circuits you would like to work on in the future.

Grade Distribution:

Final Lab Demonstration: 50%
Verilog Simulation: 10%
Final Report 40%
Extra Credit (run state): 5%
Total Possible: 105%

DO NOT WAIT UNTIL THE LAST MINUTE TO START!!!