Assignment #1

Due January 16, 2015

CIS 4930/6930: Low Power VLSI Design

Notes:

1. **The homework will be done and the report must be submitted individually.**
2. **Submit schematics, error log, netlist, plot of signals to get full credit**

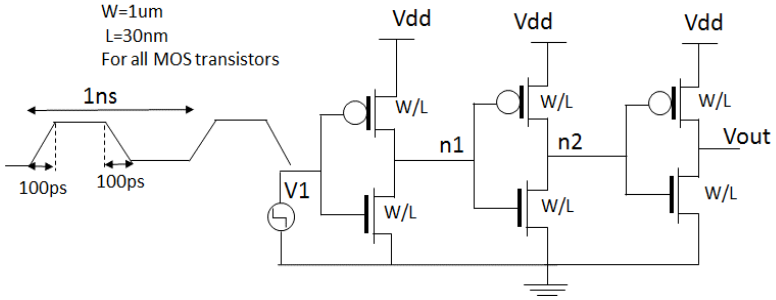
Q1. Perform transistor-level circuit simulations using LTspice of three series connected CMOS inverter using 22nm CMOS process technology to observe the following effects (use VDD = 1V). Assume the width (W) =1um and length (L) =0.03um for both NMOS and PMOS transistors. Apply a pulse train as shown in figure below.

(a) Find the rise and fall propagation delay of the middle inverter (i.e., between nodes n1 and n2).

(b) Plot propagation delay v/s width of the transistors (you can use excel to plot). Sweep the width from 1u-5u in the step of 1u. Keep L=30nm.

Hint: You can set W=S and use the following command in LT spice:

.step param S 1um 5um 1um **(10+30 points)**



Q2. Configure the circuit in the previous problem as a ring oscillator by connecting node Vout back to input and removing the voltage source V1 as shown in the diagram below. Sweep the width from 1um-5um and plot:

(a) Frequency of oscillations v/s width. **(30 Points)**

(b) Average power v/s width. **(30 Points)**