*CIS4930.002*

# VLSI Design Automation

**Summer C – 2015**

# Homework 3

**Due:** *Saturday, June 20th, 2015*
**Submit PDF to Canvas by 11:59 PM**

**All Problems are worth 20pts unless otherwise specified**

**Use Cell Sizes for the Project to Calculate Partition Width/Heights, Assume that the bounding area is that of a padframe slice, multiple slices may be needed.**

Using the table below, complete the following problems minimizing dead space across the slices.

**(1)** Floorplan your solution to Problem 1 from HW2.

**(2)** Floorplan your solution to Problem 2 from HW2.

**(3)** Floorplan your solution to Problem 3 from HW2.

**(4)** Floorplan your solution to Problem 4 from HW2.

**(5)** Floorplan your solution to Problem 5 from HW2.

**(6)** Floorplan your solution to Problem 6 from HW2. (Optional, 10pts EC)

**(7)** Floorplan your solution to Problem 7 from HW2. (Optional, 10pts EC)

| **Module** | **Width** | **Length** |
|---|---|---|
| Partition 1 (HW2) | W | L |
| Partition 2 (HW2) | W | L |
| 3 | 20 | 15 |
| 4 | 70 | 45 |
| 5 | 25 | 30 |
| 6 | 88 | 27 |