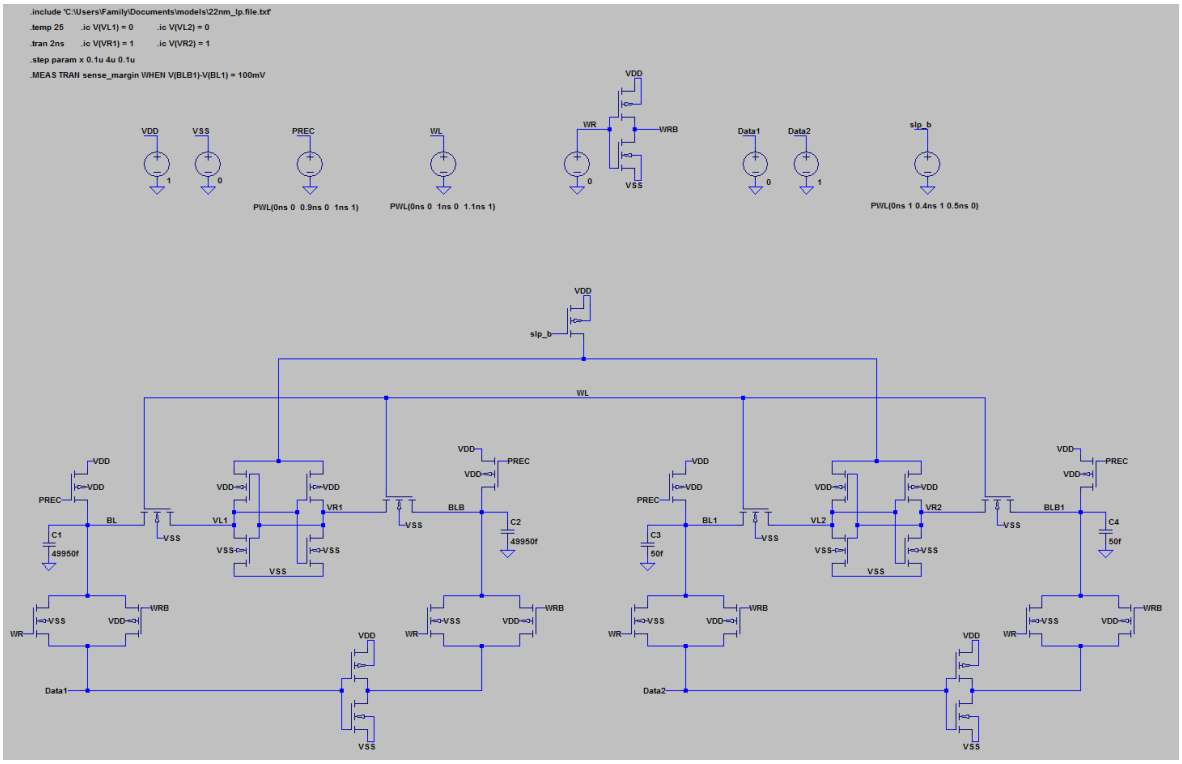
Team Low Power Rangers
John Gangemi
Christopher Frazier
Bassam Saed

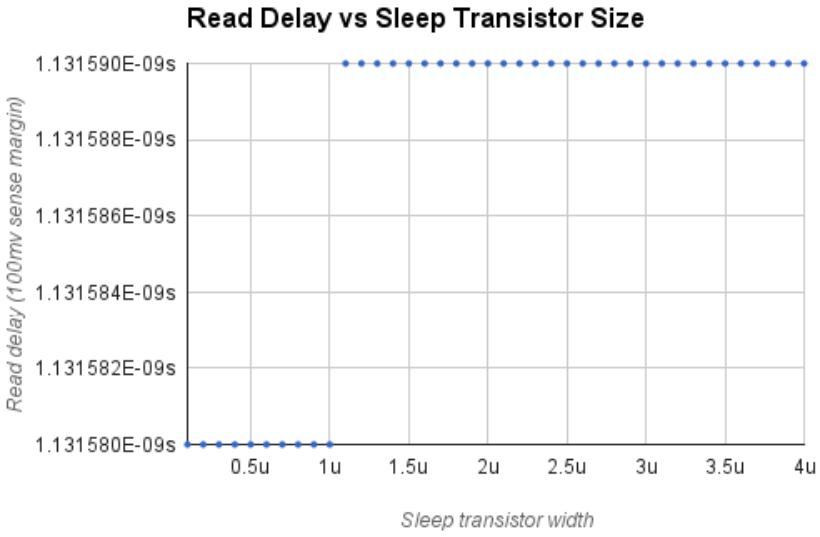
Stage 3 Report

Part A

Read Delay Schematic



Read Delay Plot



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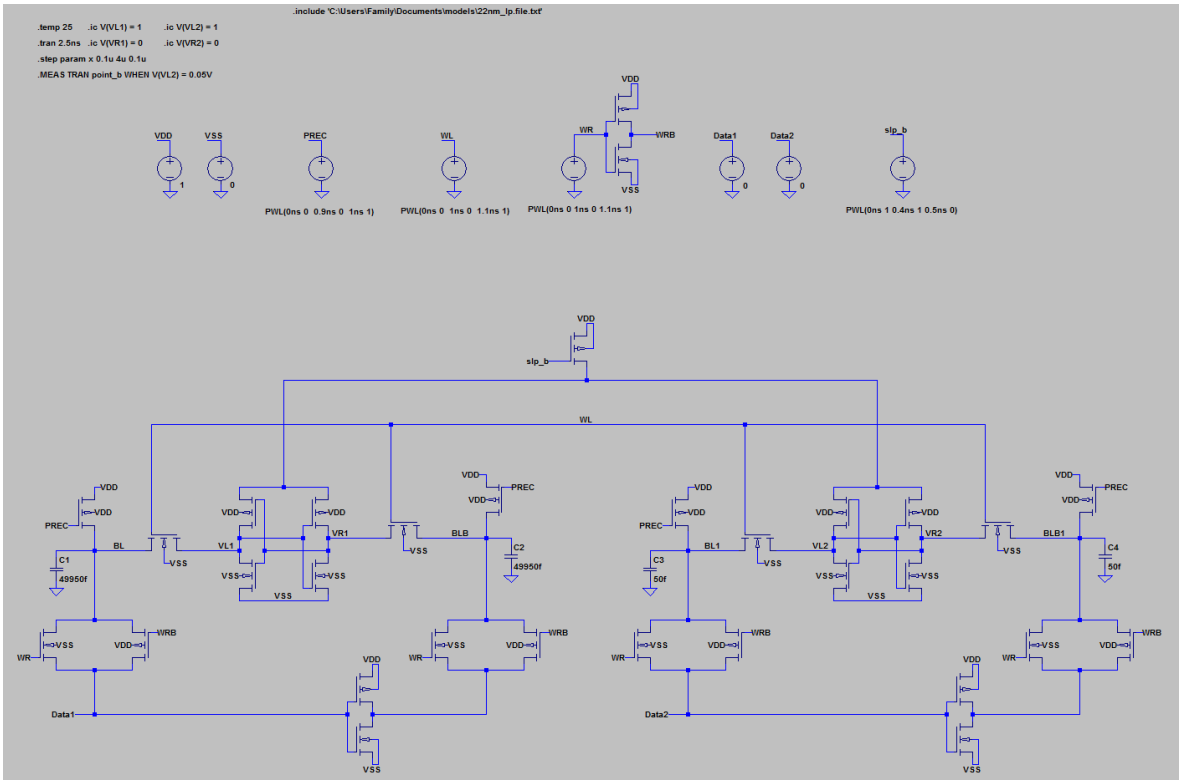
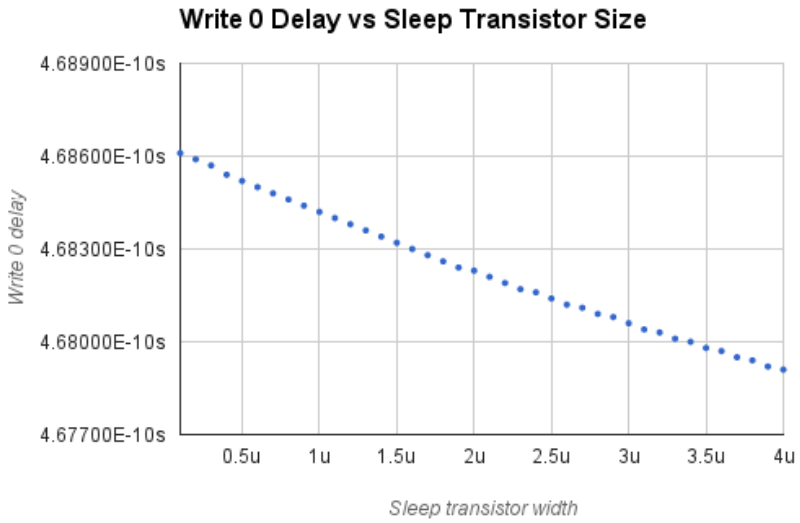
Write 0 Delay Schematic



Write 0 Delay Plot



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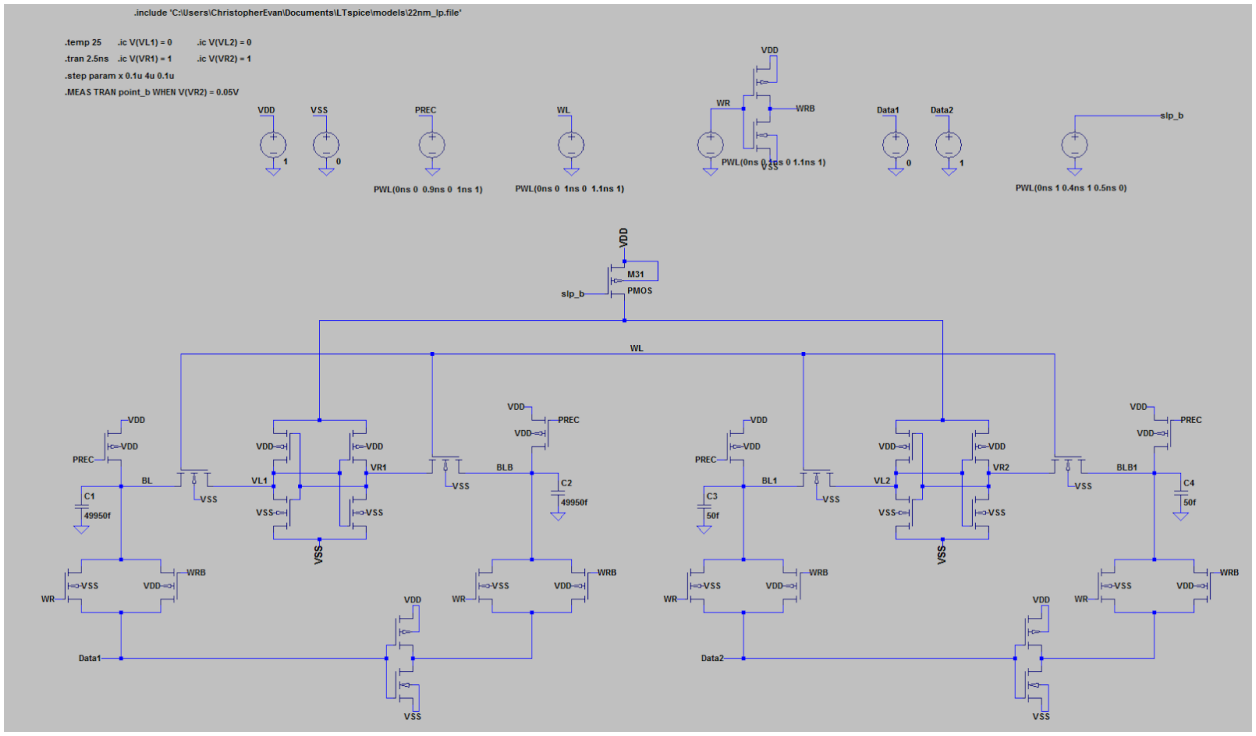
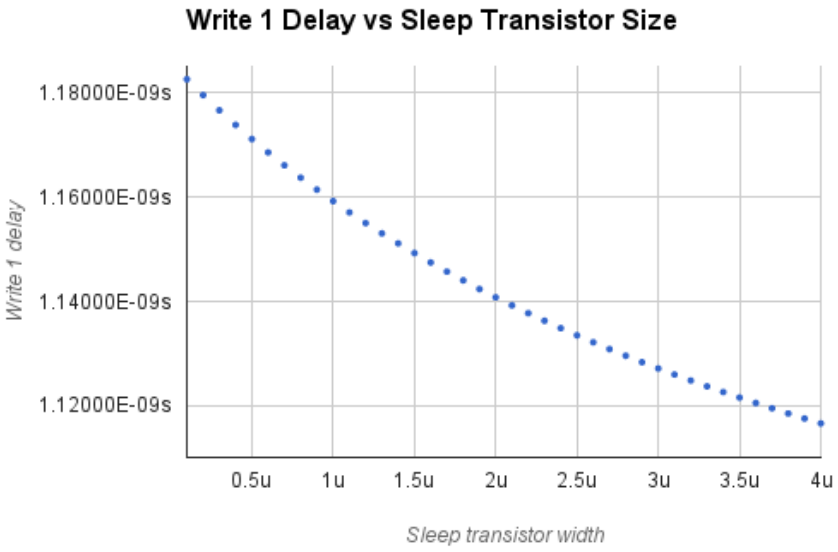
Write 1 Delay Schematic



Write 1 Delay Plot



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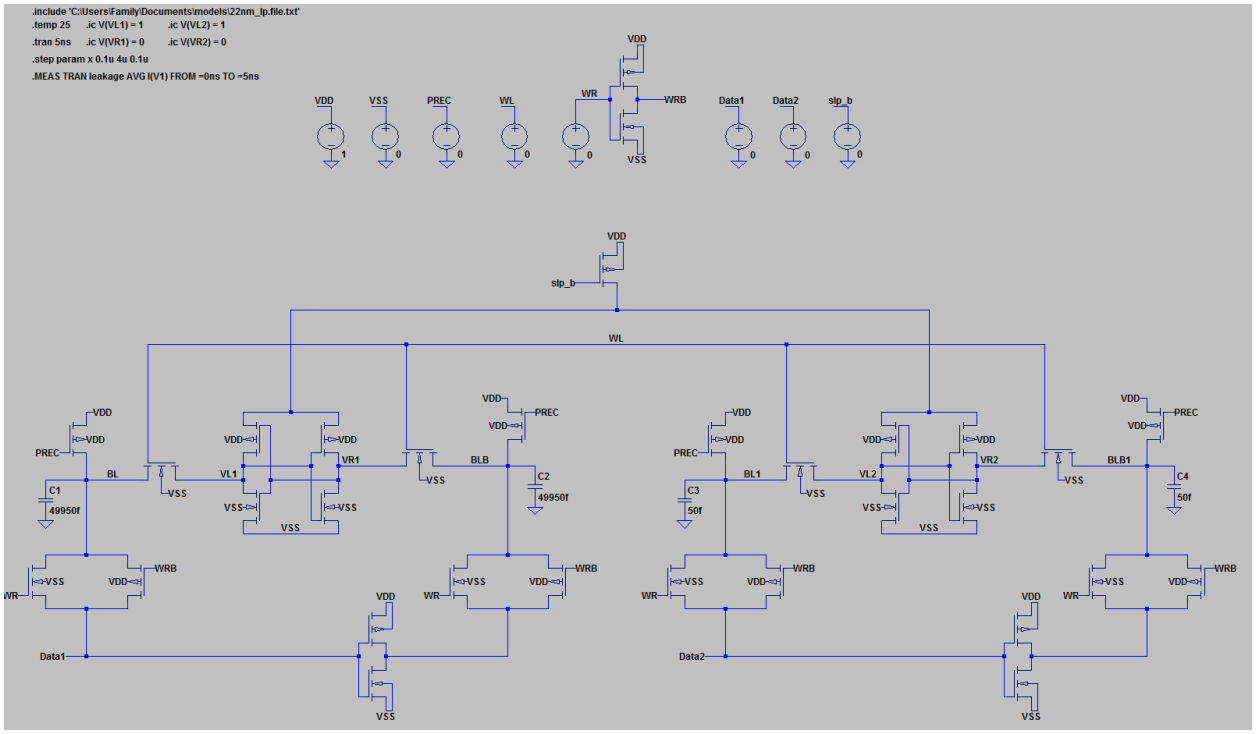
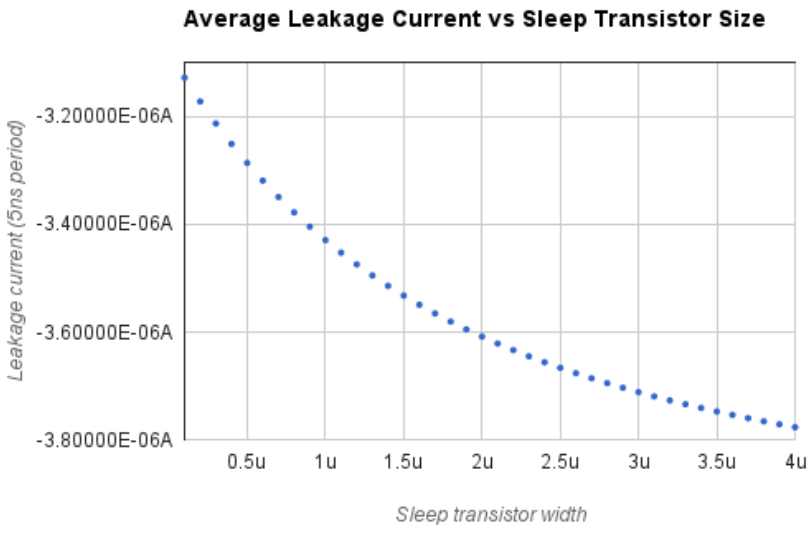
Leakage Schematic



Leakage Plots



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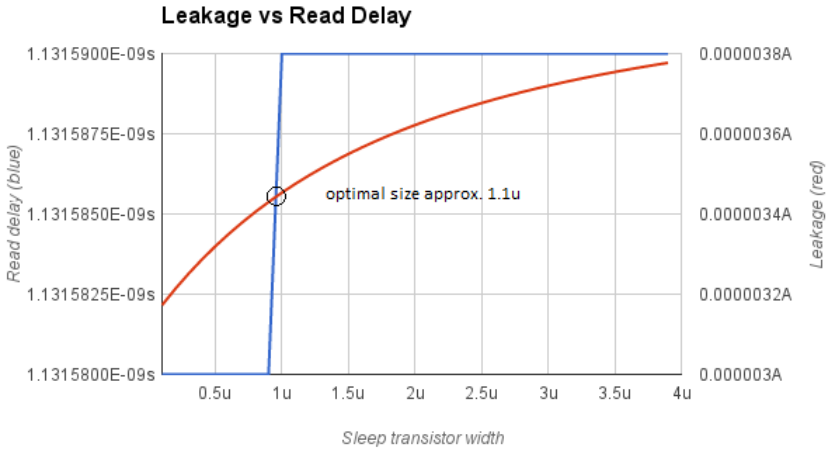

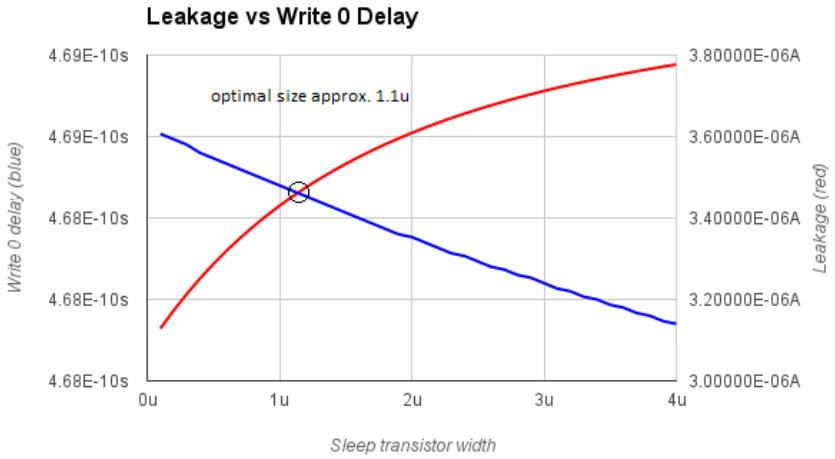

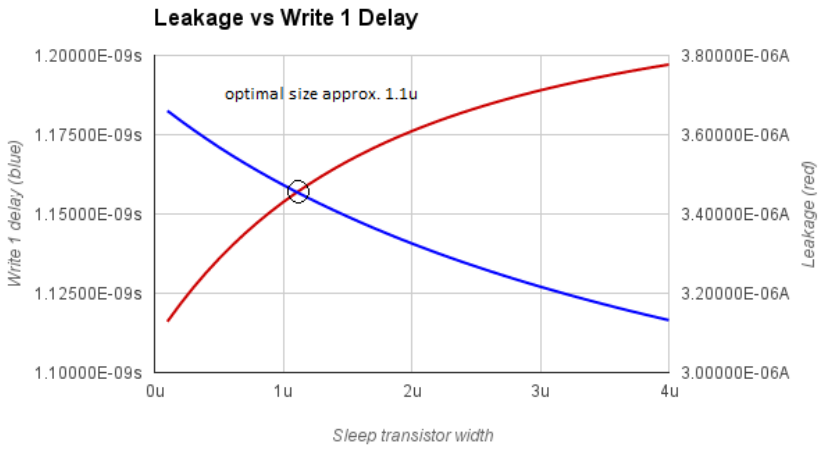

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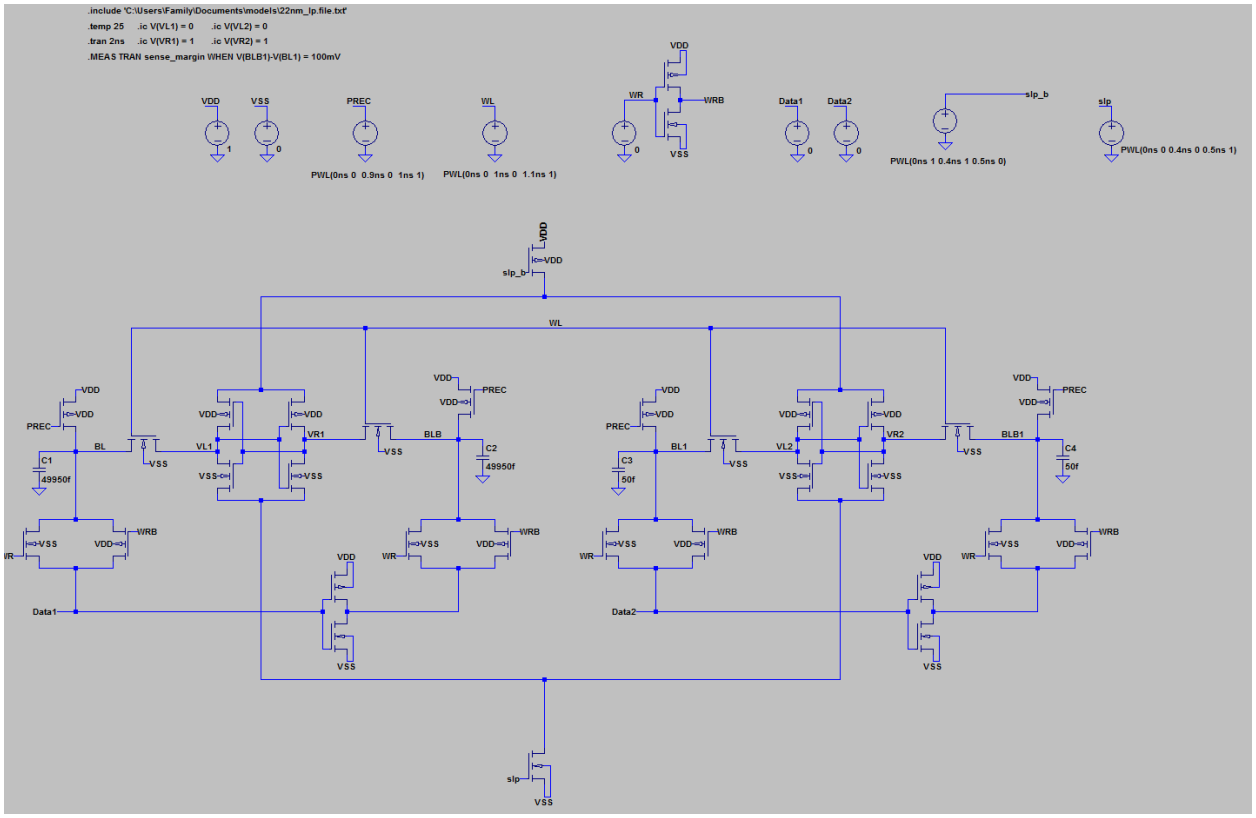
Optimum size of the sleep header transistor is approximately **1.1 microns** (width) as shown in the Leakage vs Delay plots.

Part B

Optimum size of the sleep header transistor used in testing was 1.1 microns for width and 0.03 microns for length.

Optimum size of the sleep footer transistor used in testing was 1.6 microns for width and 0.03 microns for length.

Read Delay Schematic



Read delay measurement for the circuit above was **1.13328e-009 seconds** according to the corresponding errorlog.

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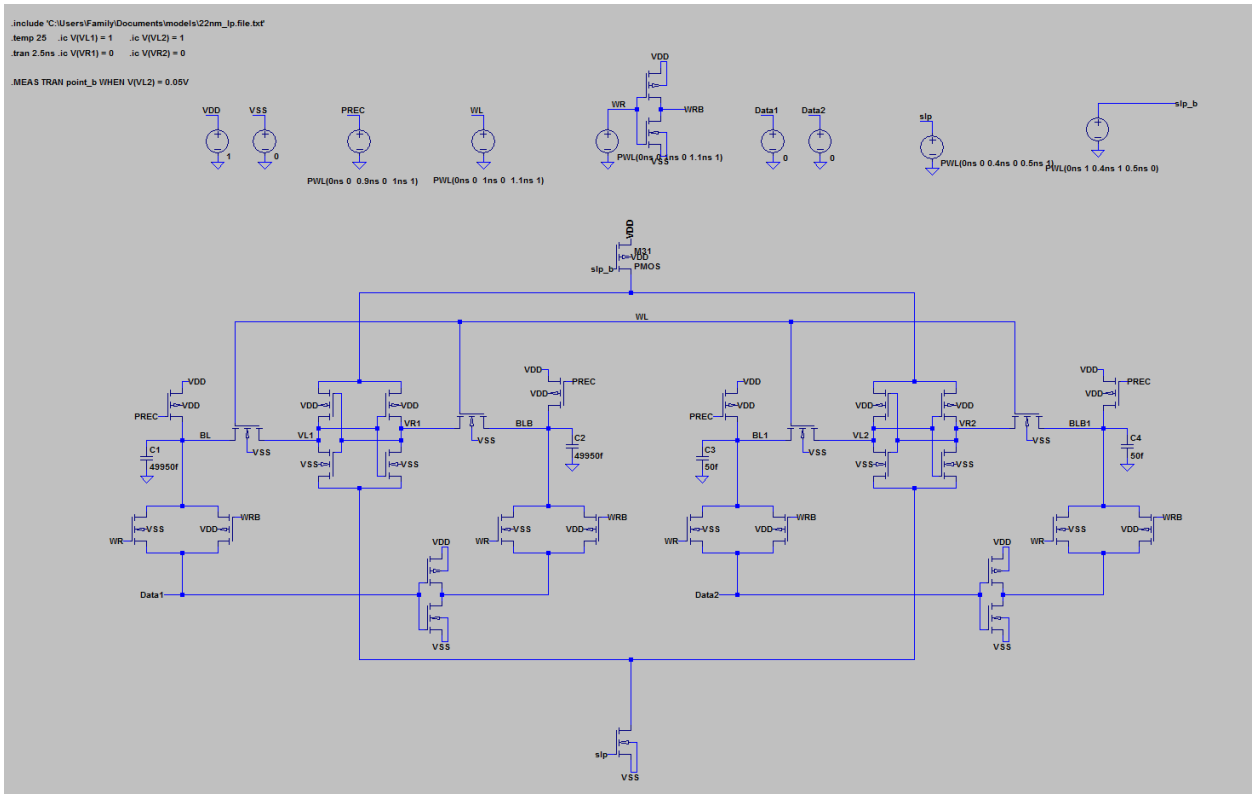
Write 0 Delay Schematic



Write 0 delay measurement for the circuit above was **1.53435e-009 seconds** according to the corresponding errorlog.

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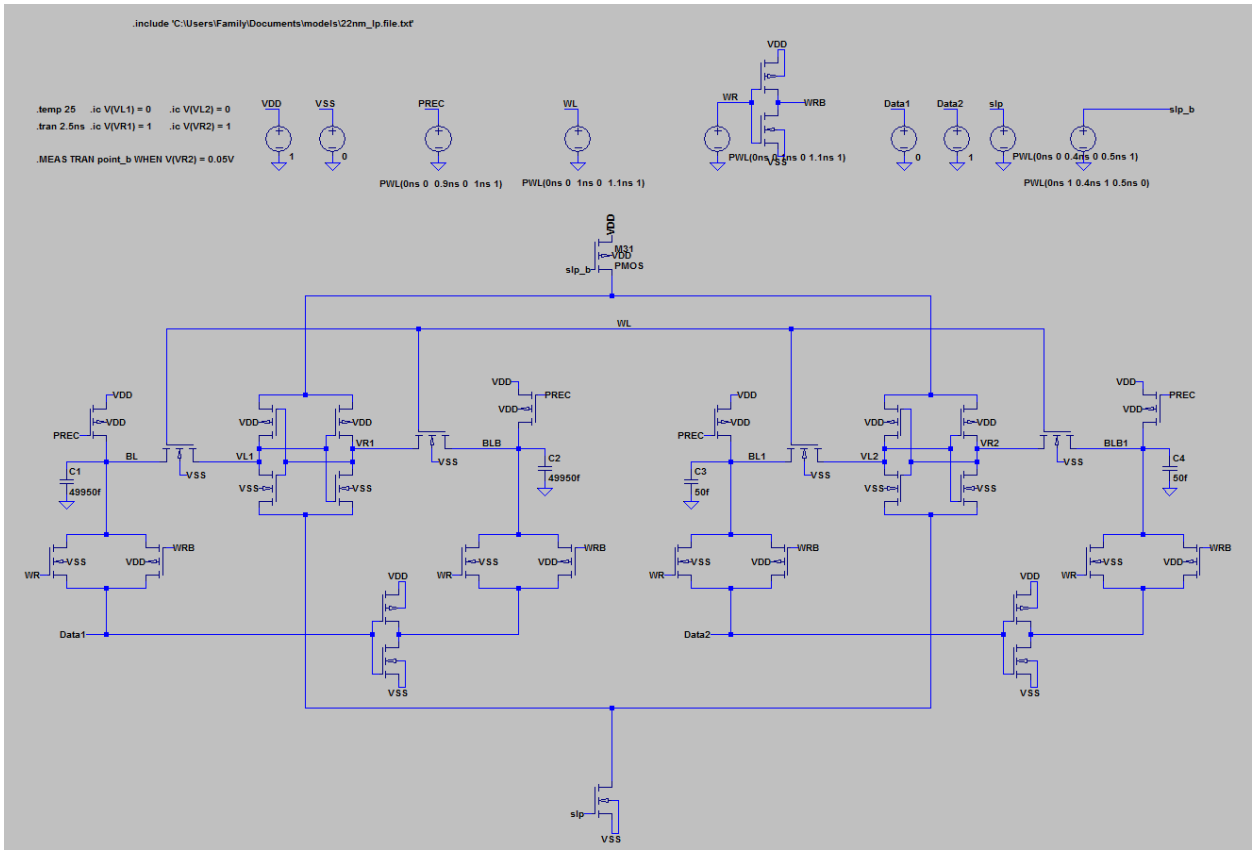
Write 1 Delay Schematic



Write 1 delay measurement for the circuit above was **2.15541e-009 seconds** according to the corresponding errorlog.

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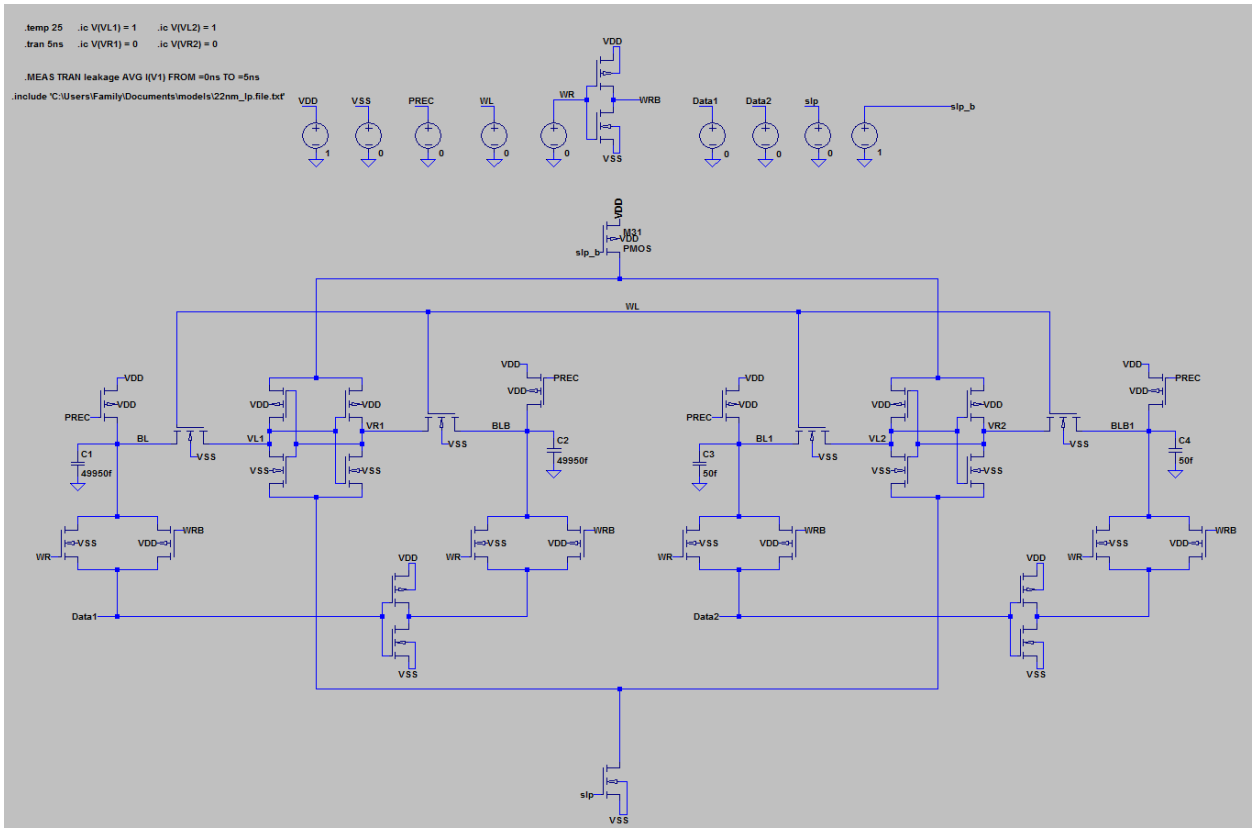
Leakage Schematic



Leakage measurement across 5 ns interval for the circuit above was **2.72289e-006 amperes** according to the corresponding errorlog.

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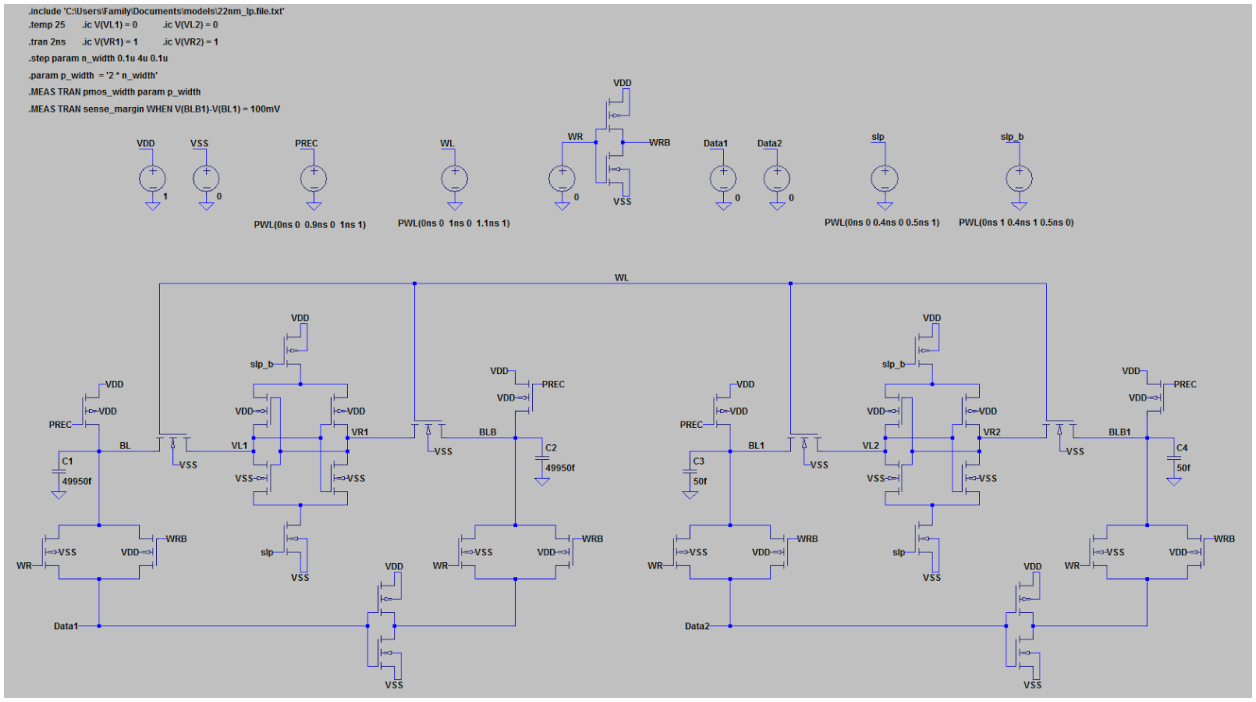
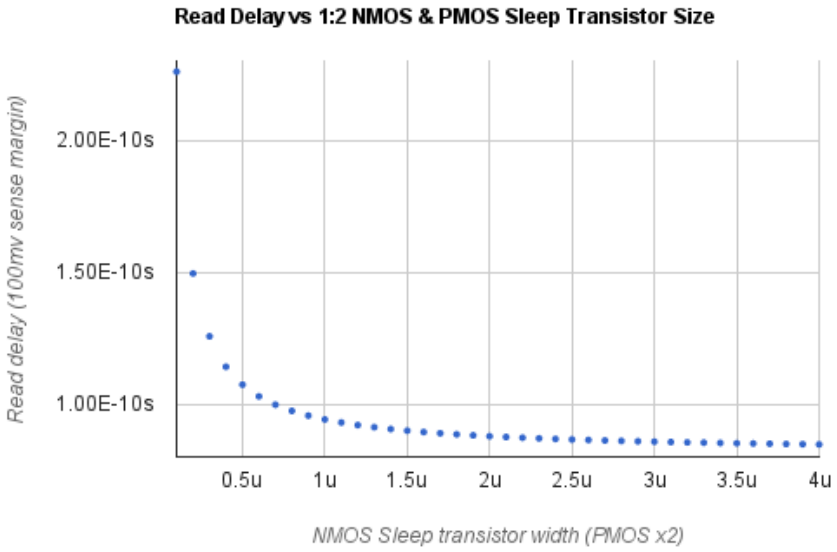
Part C

Read Delay Schematic



Read Delay Plot



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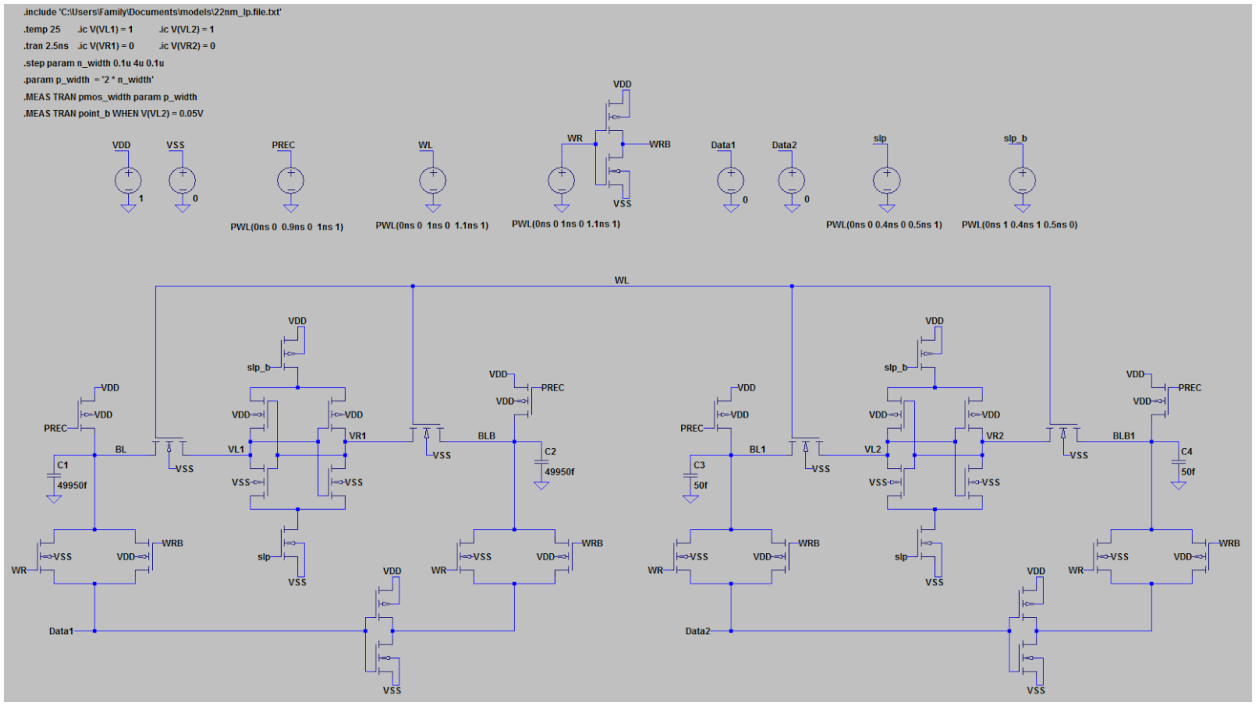
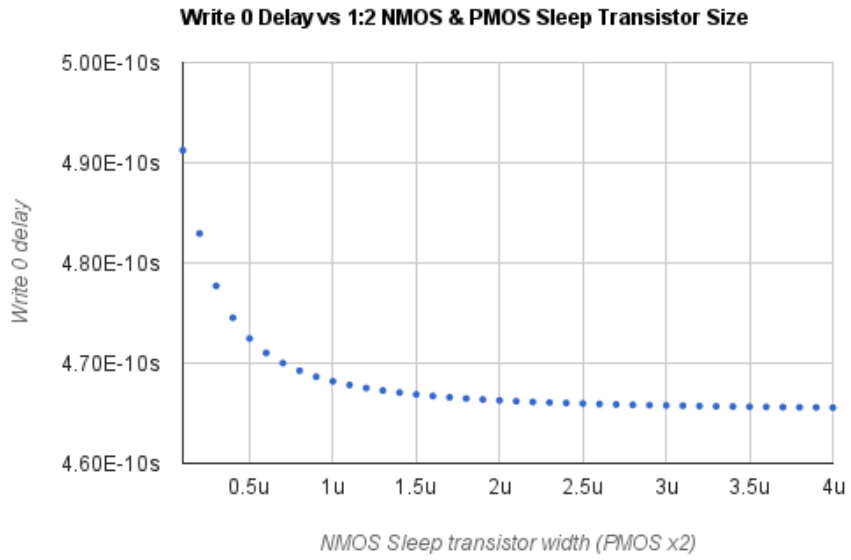
Write 0 Delay Schematic



Write 0 Delay Plot



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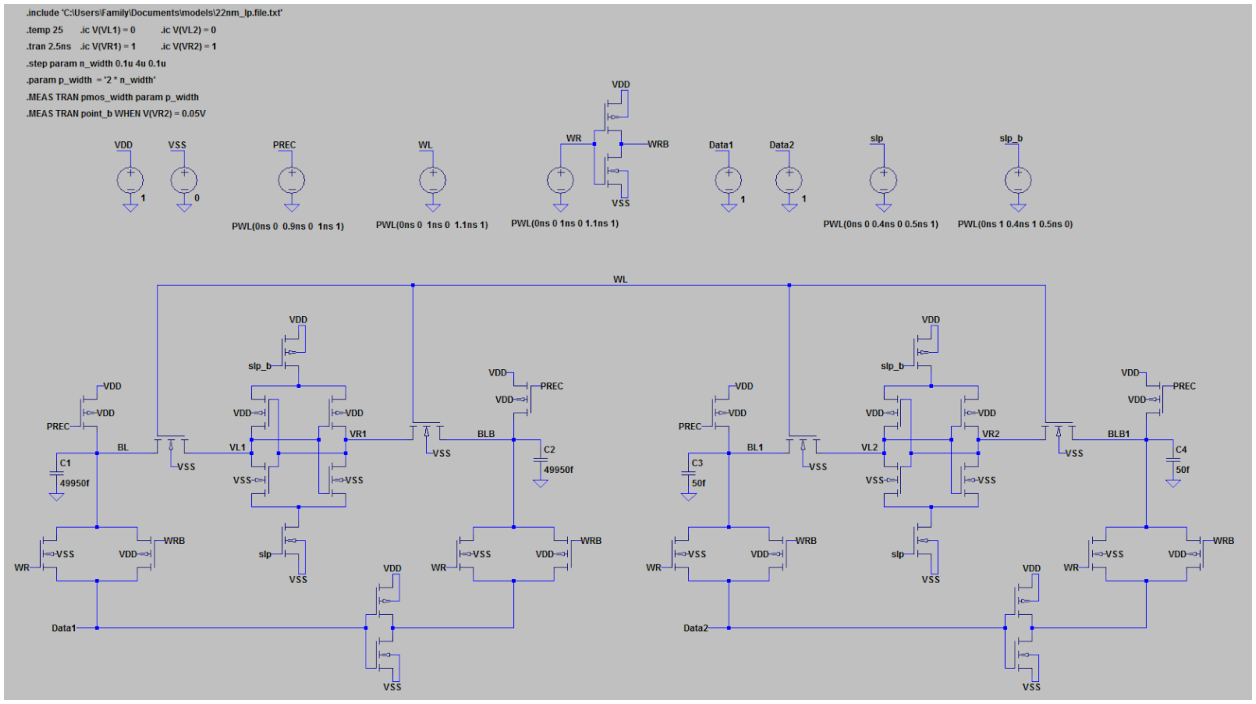
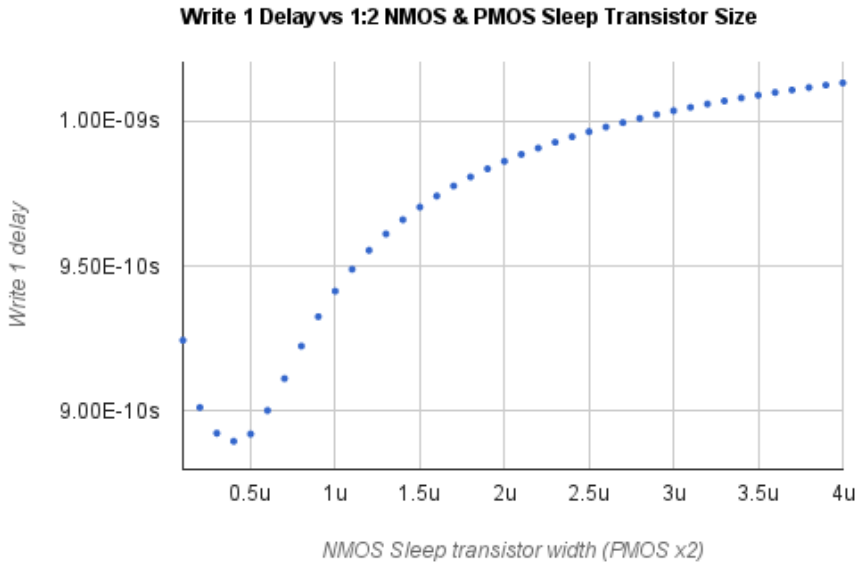
Write 1 Delay Schematic



Write 1 Delay Plot



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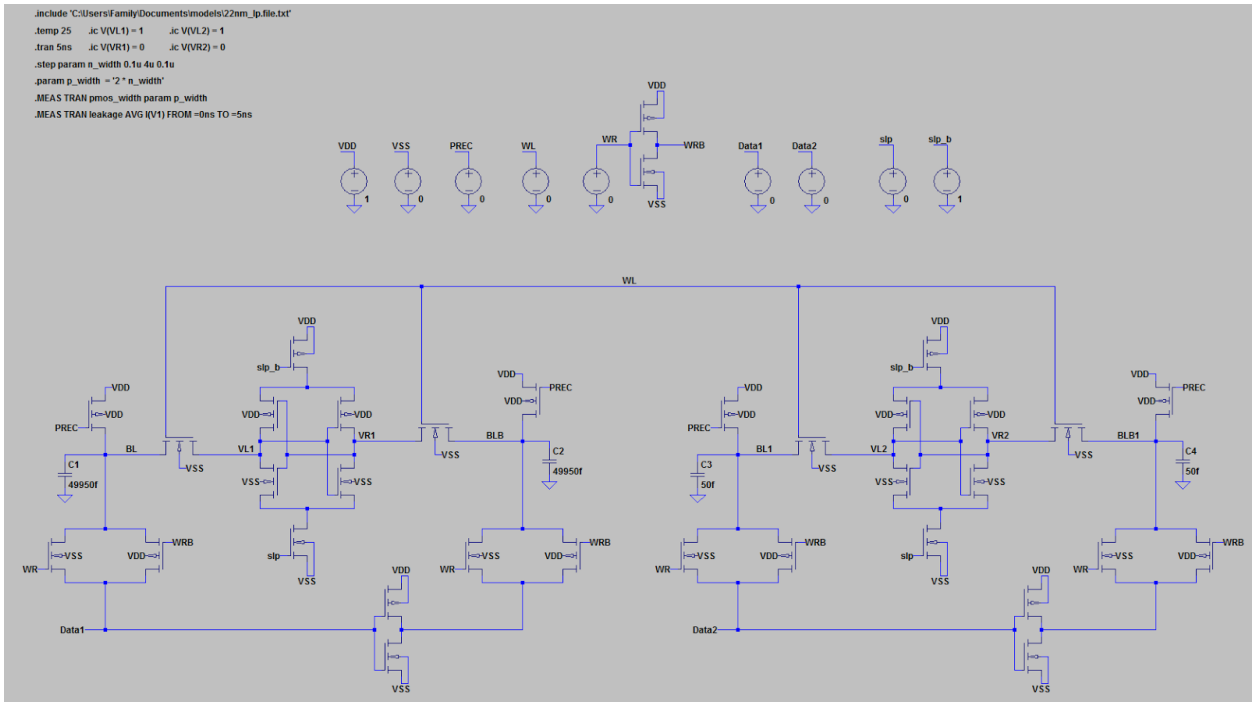
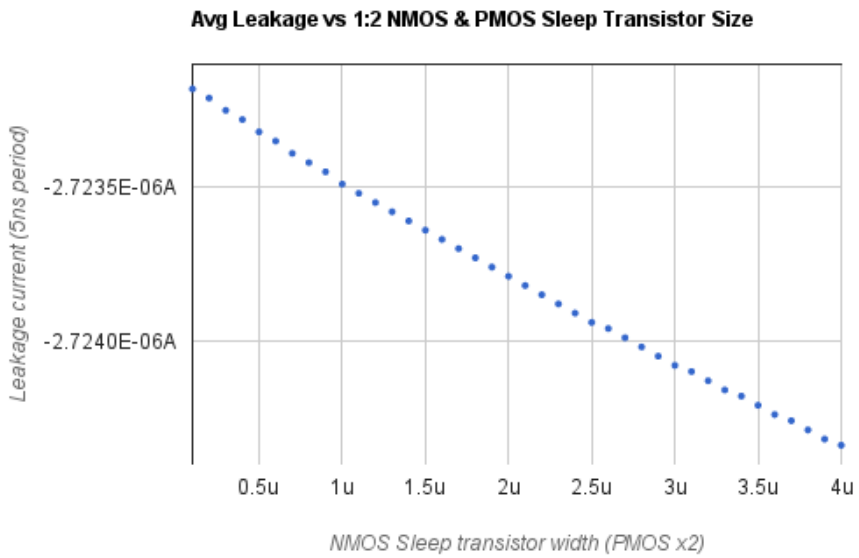
Leakage Schematic



Leakage Plots



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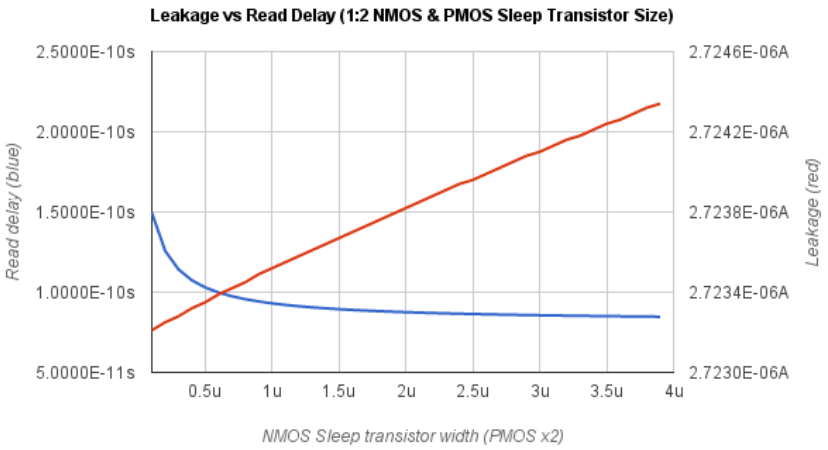

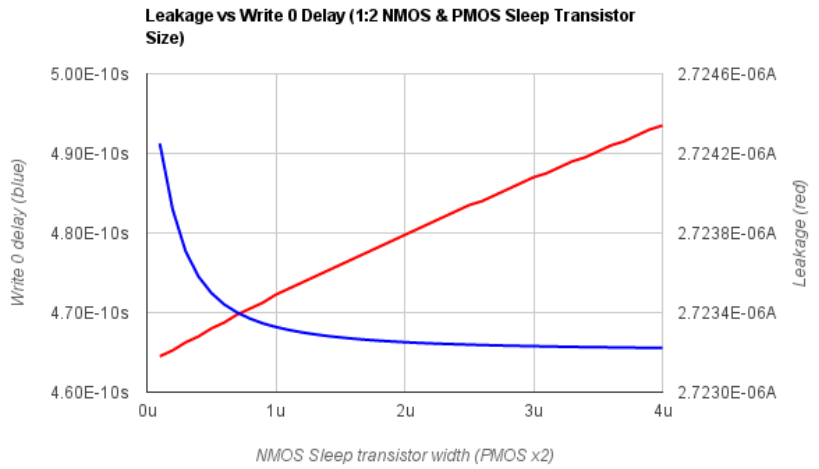

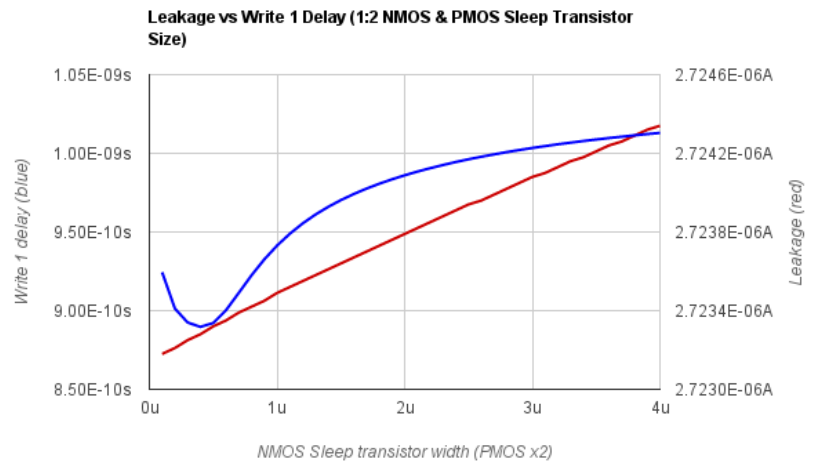

It can be observed that the “write 1” delay in the appropriate plots above exhibits abnormal characteristics. This behavior is due to the actual waveform “twisting” when it reaches 5% of VDD for the VR2 node.

However it is possible to see in the leakage versus write 1 delay plot the initial negative slope of the write 1 delay is approaching 0.6 microns in NMOS sleep transistor width before it abruptly reverses direction (twisting of waveform). Therefore one can conclude the write 1 delay in a best case scenario would exhibit the same trend as the other leakage versus delay plots.

Optimum size of the sleep header transistor is approximately **1.2 microns** (x2 NMOS size) in width and 0.03 microns in length.

Optimum size of the sleep footer transistor is approximately **0.6 microns** in width and 0.03 microns in length.

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Appendix

Netlist and Errorlogs

- Please see the Text Files folders for delay and leakge
  - /Part A/Delay/Text Files
  - /Part A/Leakage/Text Files

- Please see the Text Files folders for delay and leakge
  - /Part B/Delay/Text Files
  - /Part B/Leakage/Text Files

- Please see the Text Files folders for delay and leakge
  - /Part C/Delay/Text Files
  - /Part C/Leakage/Text Files