

10.9 - OVERSAMPLING CONVERTERS

INTRODUCTION

What is an oversampling converter?

An oversampling converter uses a noise-shaping modulator to reduce the in-band quantization noise to achieve a high degree of resolution.

What is the possible performance of an oversampled converter?

The performance can range from 16 to 18 bits of resolution at bandwidths up to 50kHz to 8 to 10 bits of resolution at bandwidths up to 5-10MHz.

What is the range of oversampling?

The oversampling ratio, called M , is a ratio of the clock frequency to the Nyquist frequency of the input signal. This oversampling ratio can vary from 8 to 256.

- The resolution of the oversampled converter is proportional to the oversampled ratio.
- The bandwidth of the signal to be converted is inversely proportional to the oversampled ratio.

What are the advantages of oversampling converters?

Very compatible with VLSI technology because most of the converter is digital

High resolution

Single-bit quantizers use a one-bit DAC which has no INL or DNL errors

Provide an excellent means of trading precision for speed

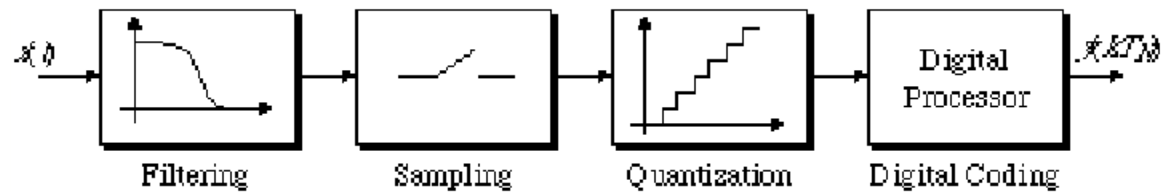
What are the disadvantages of oversampling converters?

Difficult to model and simulate

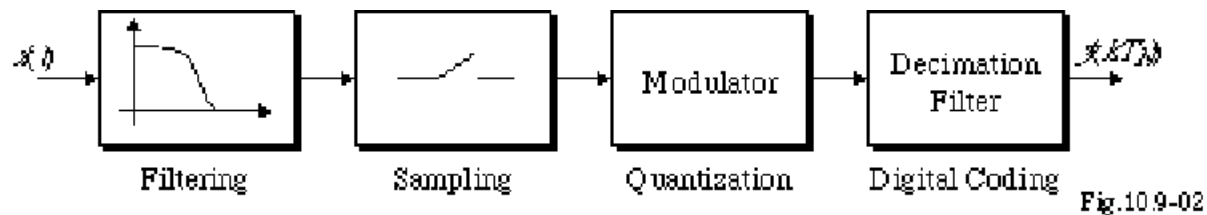
Limited in bandwidth to the clock frequency divided by the oversampling ratio

NYQUIST VERSUS OVERSAMPLED ADCs

Conventional Nyquist ADC Block Diagram:



Oversampled ADC Block Diagram:



Components:

- Filter - Prevents possible aliasing of the following sampling step.
- Sampling - Necessary for any analog-to-digital conversion.
- Quantization - Decides the nearest analog voltage to the sampled voltage (determines the resolution).
- Digital Coding - Converts the quantizer information into a digital signal.

FREQUENCY SPECTRUM OF NYQUIST AND OVERSAMPLED CONVERTERS

Definitions:

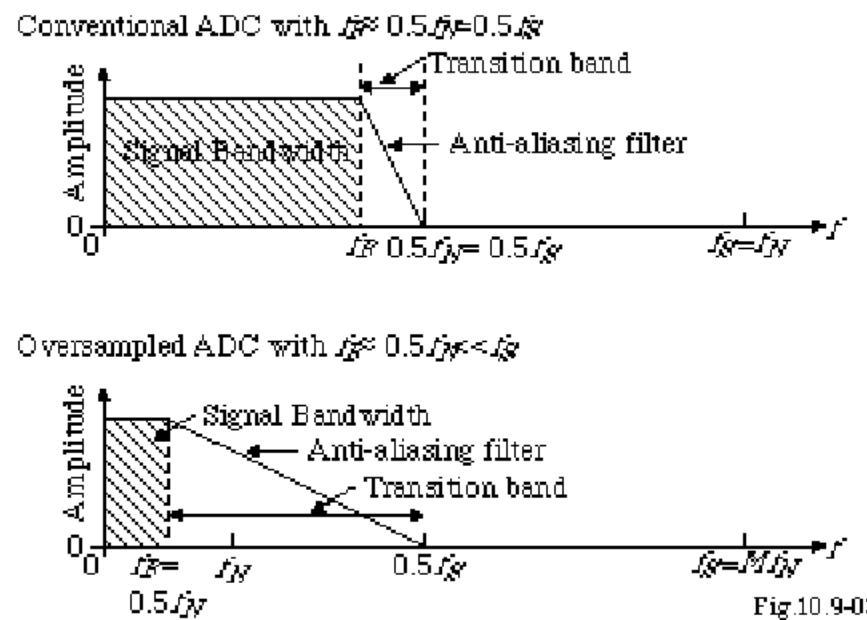
f_B = analog signal bandwidth

f_N = Nyquist frequency (two times f_B)

f_S = sampling or clock frequency

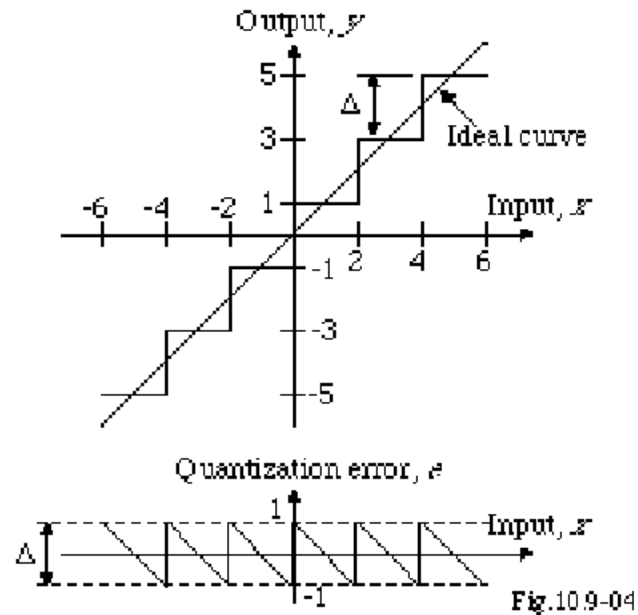
$M = \frac{f_S}{f_N} = \frac{f_S}{2f_B}$ = oversampling ratio

Frequency spectrums:



QUANTIZATION NOISE OF A CONVENTIONAL (NYQUIST) ADC

Multilevel Quantizer:



The quantized signal y can be represented as,

$$y = Gx + e$$

where

G = gain of the ADC, normally 1

e = quantization error

The mean square value of the quantization error is

$$e_{rms}^2 = S_Q = \frac{1}{D} \int_{-D/2}^{D/2} e(x)^2 dx = \frac{D^2}{12}$$

QUANTIZATION NOISE OF A CONVENTIONAL (NYQUIST) ADC - CONTINUED

Spectral density of the sampled noise:

When a quantized signal is sampled at $f_S (= 1/t)$, then all of its noise power folds into the frequency band from 0 to $0.5f_S$. Assuming that the noise power is white, the spectral density of the sampled noise is,

$$E(f) = e_{rms} \sqrt{\frac{2}{f_S}} = e_{rms} \sqrt{2t}$$

where

$$t = 1/f_S \quad \text{and} \quad f_S = \text{sampling frequency}$$

The inband noise energy n_o is

$$n_o^2 = \int_0^{f_B} E^2(f) df = e_{rms}^2 (2f_B t) = e_{rms}^2 \left(\frac{2f_B}{f_S} \right) = \frac{e_{rms}^2}{M}$$

$$n_o = \frac{e_{rms}}{\sqrt{M}}$$

What does all this mean?

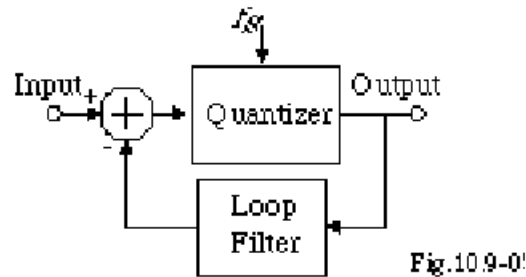
- One way to increase the resolution of an ADC is to make the bandwidth of the signal, f_B , less than the clock frequency, f_S . In otherwords, give up bandwidth for precision.
- However, it is seen from the above that a doubling of the oversampling ratio M , only gives a decrease of the inband noise, n_o , of $1/\sqrt{2}$ which corresponds to -3dB decrease or an increase of resolution of 0.5 bits

The conclusion is that reduction of the oversampling ratio is not a very good method of increasing the resolution of a Nyquist analog-digital converter.

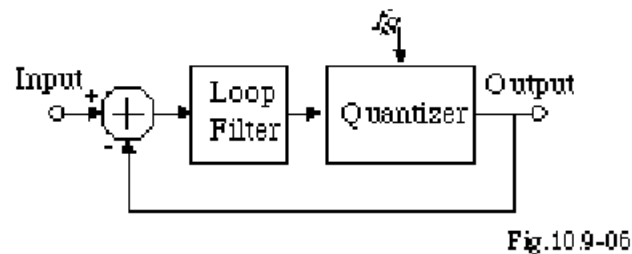
OVERSAMPLED ANALOG-DIGITAL CONVERTERS

Classification of oversampled ADCs:

- 1.) Straight-oversampling - The quantization noise is assumed to be equally distributed over the entire frequency range of dc to $0.5f_S$. This type of converter is represented by the Nyquist ADC.
- 2.) Predictive oversampling - Uses noise shaping plus oversampling to reduce the inband noise to a much greater extent than the straight-oversampling ADC. Both the signal and noise quantization spectrums are shaped.



- 3.) Noise-shaping oversampling - Similar to the predictive oversampling except that only the noise quantization spectrum is shaped while the signal spectrum is preserved.



The noise-shaping oversampling ADCs are also known as *delta-sigma* ADCs. We will only consider the delta-sigma type oversampling ADCs.

OVERSAMPLING ANALOG-DIGITAL CONVERTERS - CONTINUED

General block diagram of an oversampled ADC:

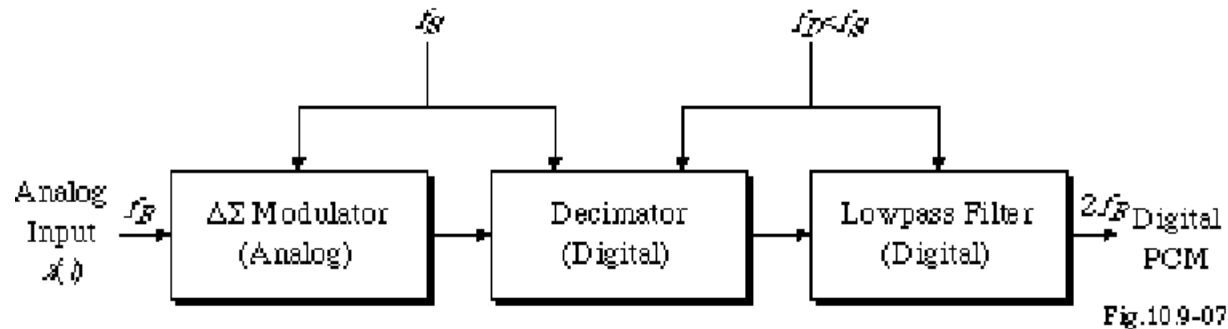


Fig.10.9-07

Components of the Oversampled ADC:

- 1.) $\Delta\Sigma$ Modulator - Also called the noise shaper because it can shape the quantization noise and push the majority of the inband noise to higher frequencies. It modulates the analog input signal to a simple digital code, normally a one-bit serial stream using a sampling rate much higher than the Nyquist rate.
- 2.) Decimator - Also called the down-sampler because it down samples the high frequency modulator output into a low frequency output and does some pre-filtering on the quantization noise.
- 3.) Digital Lowpass Filter - Used to remove the high frequency quantization noise and to preserve the input signal.

Note: Only the modulator is analog, the rest of the circuitry is digital.

FIRST-ORDER, DELTA-SIGMA MODULATOR

Block diagram of a first-order, delta-sigma modulator:

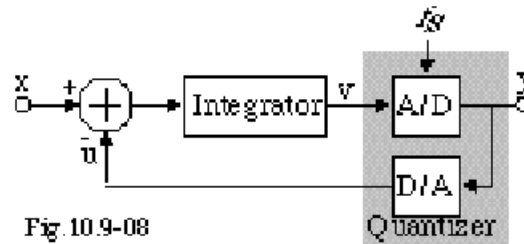


Fig.10.9-08

Components:

- Integrator (continuous or discrete time)
- Coarse quantizer (typically two levels)
 - A/D which is a comparator for two levels
 - D/A which is a switch for two levels

First-order modulator output for a sinusoidal input:

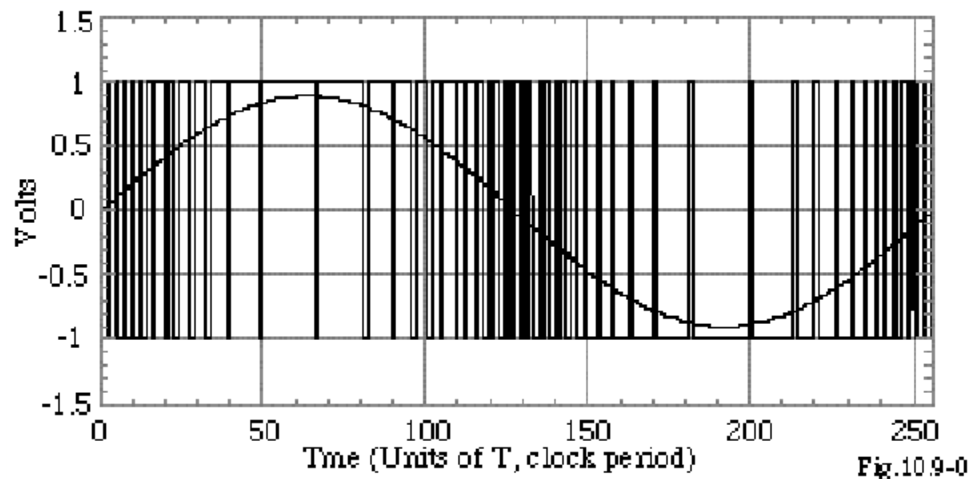


Fig.10.9-0

SAMPLED-DATA MODEL OF A FIRST-ORDER DS MODULATOR

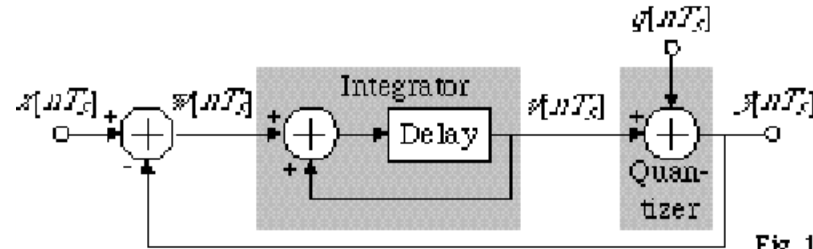


Fig. 10.9-10

Writing the following relationships,

$$y[nT_s] = q[nT_s] + v[nT_s]$$

$$v[nT_s] = w[(n-1)T_s] + v[(n-1)T_s]$$

$$\therefore y[nT_s] = q[nT_s] + w[(n-1)T_s] + v[(n-1)T_s] = q[nT_s] + \{x[(n-1)T_s] - y[(n-1)T_s]\} + v[(n-1)T_s]$$

But the first equation can be written as

$$y[(n-1)T_s] = q[(n-1)T_s] + v[(n-1)T_s] \quad \rightarrow \quad q[(n-1)T_s] = y[(n-1)T_s] - v[(n-1)T_s]$$

Substituting this relationship into the above gives,

$$y[nT_s] = x[(n-1)T_s] + q[nT_s] - q[(n-1)T_s]$$

Converting this expression to the z -domain gives,

$$Y(z) = z^{-1}X(z) + (1-z^{-1})Q(z)$$

Definitions:

$$\text{Signal Transfer Function} = STF = \frac{Y(z)}{X(z)} = z^{-1} \quad \text{and} \quad \text{Noise Transfer Function} = NTF = \frac{Y(z)}{Q(z)} = 1-z^{-1}$$

HIGHER-ORDER DS MODULATORS

A second-order, $\Delta\Sigma$ modulator:

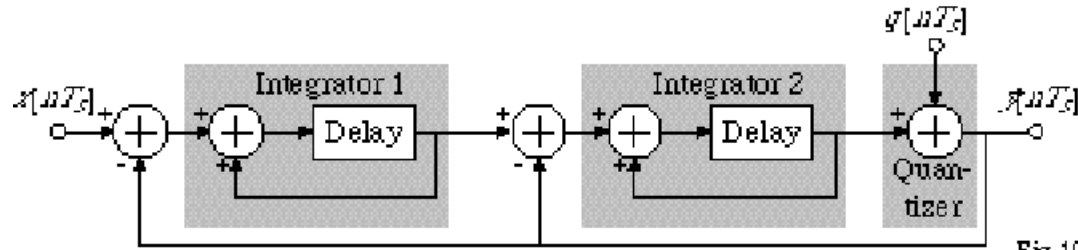


Fig.10.9-11

It can be shown that the z -domain output is,

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2Q(z)$$

The general, L -th order $\Delta\Sigma$ modulator has the following form,

$$Y(z) = z^{-L}X(z) + (1-z^{-1})^LQ(z)$$

Note that noise transfer function, NTF , has L -zeros at the origin resulting in a high-pass transfer function.

This high-pass characteristic reduces the noise at low frequencies.

NOISE TRANSFER FUNCTION

The noise transfer function can be written as,

$$NTF_Q(z) = (1 - z^{-1})^L$$

Evaluate $(1 - z^{-1})$ by replacing z by $e^{j\omega T_s}$ to get

$$(1 - z^{-1}) = (1 - e^{-j\omega T_s}) \times \frac{2j}{2j} \times \frac{e^{j\omega T_s/2}}{e^{j\omega T_s/2}} = \left(\frac{e^{j\omega T_s/2} - e^{-j\omega T_s/2}}{2j} \right) 2j e^{-j\omega T_s/2} = \sin(\omega T_s/2) 2j e^{-j\omega T_s/2}$$

$$(1 - z^{-1}) = (2 \sin \omega T_s/2) \rightarrow |NTF_Q(f)| = (2 \sin \omega T_s/2)^L$$

Magnitude of the noise transfer function,

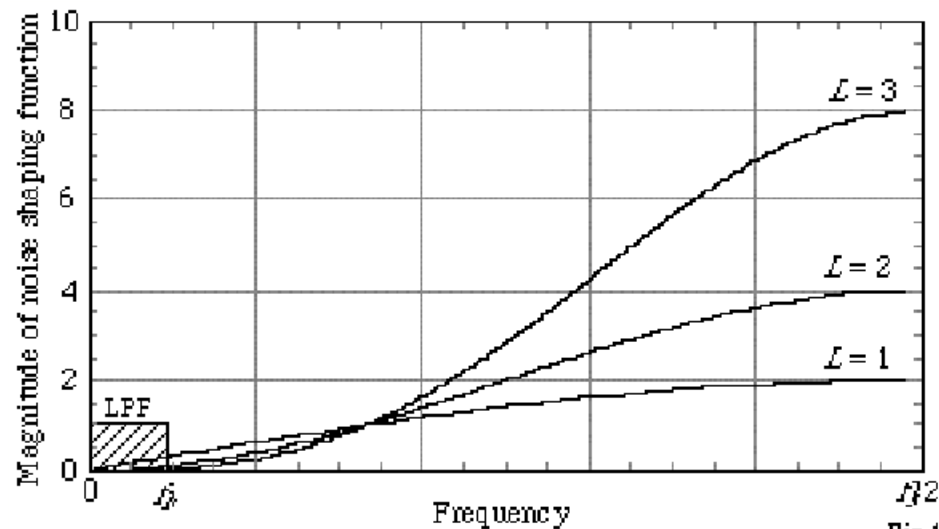


Fig.10.9-12

Note: Single-loop modulators having noise shaping characteristics of the form $(1 - z^{-1})^L$ are unstable for $L > 2$ unless an L -bit quantizer is used.

IN-BAND RMS NOISE OF SINGLE-LOOP DS MODULATOR

The power spectral density of the $\Delta\Sigma$ modulator, $S_E(f)$, is given as

$$S_E(f) = |NTF_Q(f)|^2 \frac{|S_Q(f)|}{f_s}$$

where we have assumed that noise power is white.

Next, integrate $S_E(f)$ over the signal band to get the inband noise power recalling that $S_Q = \frac{D^2}{12}$

$$\therefore S_B = \frac{1}{f_s} \int_{-f_b}^{f_b} (2\sin \mathbf{p}fT_s)^{2L} \frac{D^2}{12} df \approx \left(\frac{\mathbf{p}^{2L}}{2^{L+1}} \right) \left(\frac{1}{M^{2L+1}} \right) \left(\frac{D^2}{12} \right)$$

where $\sin \mathbf{p}fT_s$ has been approximated as $\mathbf{p}fT_s$ for $M \gg 1$.

Therefore, the in-band, rms noise is given as

$$n_0 = \sqrt{S_B} = \left(\frac{\mathbf{p}^L}{\sqrt{2^{L+1}}} \right) \left(\frac{1}{M^{L+0.5}} \right) \left(\frac{D}{\sqrt{12}} \right) = \left(\frac{\mathbf{p}^L}{\sqrt{2^{L+1}}} \right) \left(\frac{1}{M^{L+0.5}} \right) e_{rms}$$

Comment:

Note that as the $\Delta\Sigma$ is a much more efficient way of achieving resolution by increasing M .

$$n_0 \propto \frac{e_{rms}}{M^{L+0.5}} \quad \Rightarrow \quad \text{Doubling of } M \text{ leads to a } 2^{L+0.5} \text{ decrease in in-band noise}$$

which leads to an extra $L+0.5$ bits of resolution!

*\therefore The reduction of the oversampling ratio is an excellent method of increasing the resolution of a **DS** oversampling analog-digital converter.*

ILLUSTRATION OF RMS NOISE VERSUS OVERSAMPLING RATIO FOR SINGLE LOOP DS MODULATORS

Plotting n_0/e_{rms} gives,

$$\frac{n_0}{e_{rms}} = \left(\frac{p^L}{\sqrt{2L+1}} \right) \left(\frac{1}{M^{L+0.5}} \right)$$

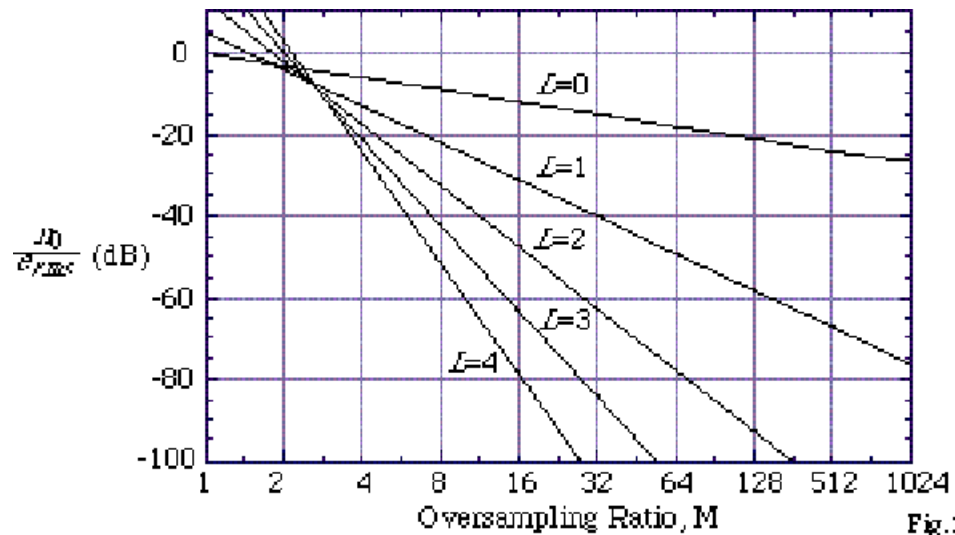


Fig.10.9-1

DYNAMIC RANGE OF $\Delta\Sigma$ ANALOG-DIGITAL CONVERTERS

Oversampled **DS** Converter:

The dynamic range, DR , for a single bit-quantizer with level spacing $D = V_{REF}$, can be found as

$$DR^2 = \frac{\text{Maximum signal power}}{S_B(f)} = \frac{\left(\frac{D}{2\sqrt{2}}\right)^2}{\left(\frac{p^{2L}}{2L+1}\right)\left(\frac{1}{M^{2L+1}}\right)\left(\frac{D^2}{12}\right)} = \frac{3}{2} \frac{2L+1}{p^{2L}} M^{2L+1}$$

Nyquist Converter:

The dynamic range of a N -bit Nyquist rate ADC is given as (now D becomes $\approx V_{REF}$ for large N),

$$DR^2 = \frac{\text{Maximum signal power}}{S_Q} = \frac{(V_{REF}/2\sqrt{2})^2}{D^2/12} = \frac{3}{2} 2^{2N} \quad \rightarrow \quad DR = \sqrt{1.5} 2^N$$

Expressing DR in terms of dB (DR_{dB}) and solving for N , gives

$$N = \frac{DR_{dB} - 1.7609}{6.0206} \quad \text{or} \quad DR_{dB} = (6.0206N + 1.7609) \text{ dB}$$

For Example:

A 16-bit $\Delta\Sigma$ ADC requires about 98dB of dynamic range.

For a second-order modulator, this implies that M is 153 or 256 since we must use powers of 2.

If the bandwidth is 20kHz, then the clock frequency must be 10.24MHz.

MULTIBIT QUANTIZERS

A single-bit quantizer:

$$D = V_{REF}$$

Advantage is that the DAC is linear.

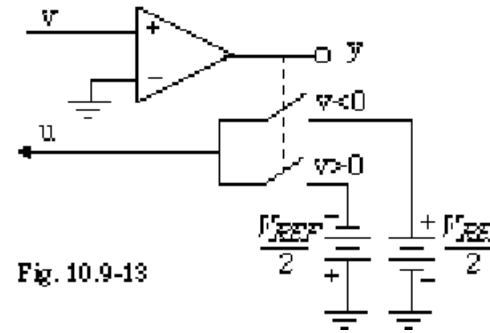


Fig. 10.9-13

Multi-bit quantizer:

Consists of an ADC and DAC of B-bits.

$$D = \frac{V_{REF}}{2^B - 1}$$

Disadvantage is that the DAC is no longer perfectly linear.

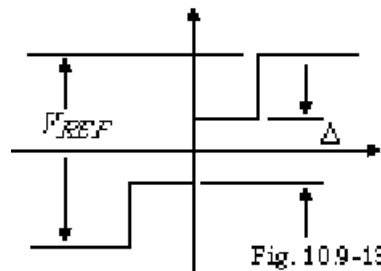


Fig. 10.9-13b

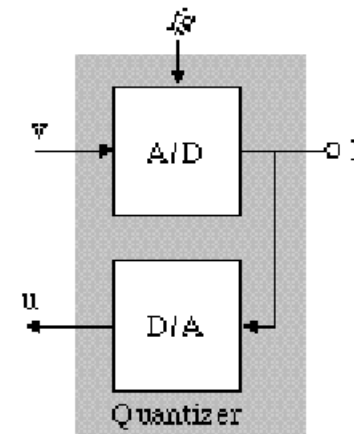


Fig. 10.9-14

Dynamic range of a multibit $\Delta\Sigma$ ADC:

$$DR^2 = \frac{3}{2} \frac{2L+1}{p^{2L}} M^{2L+1} (2^{B-1})^2$$

EXAMPLE 1 - TRADEOFF BETWEEN SIGNAL BANDWIDTH AND ACCURACY OF DS ADCs

Find the minimum oversampling ratio, M , for a 16-bit oversampled ADC which uses (a.) a 1-bit quantizer and third-order loop, (b.) a 2-bit quantizer and third-order loop, and (c.) a 3-bit quantizer and second-order loop. For each case, find the bandwidth of the ADC if the clock frequency is 10MHz.

Solution

We see that 16-bit ADC corresponds to a dynamic range of approximately 98dB.

(a.) Solving for M gives

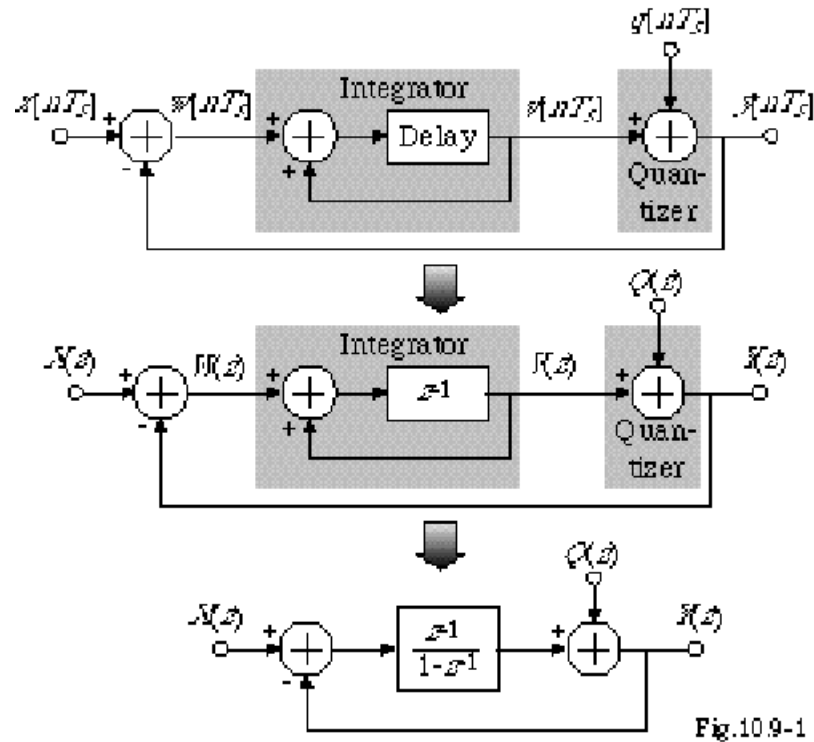
$$M = \left(\frac{2}{3} \frac{DR^2}{2L+1} \frac{p^{2L}}{(2^{B-1})^2} \right)^{1/(2L+1)}$$

Converting the dynamic range to 79,433 and substituting into the above equation gives a minimum oversampling ratio of $M = 48.03$ which would correspond to an oversampling rate of 64. Using the definition of M as $f_c/2f_B$ gives f_B as $10\text{MHz}/2 \cdot 64 = 78\text{kHz}$.

(b.) and (c.) For part (b.) and (c.) we obtain a minimum oversampling rates of $M = 32.53$ and 96.48, respectively. These values correspond to oversampling rates of 32 and 128, respectively. The bandwidth of the converters is 312kHz for (b.) and 78kHz for (c.).

Z-DOMAIN EQUIVALENT CIRCUITS

The modulator structures are much easier to analyze and interpret in the z-domain.



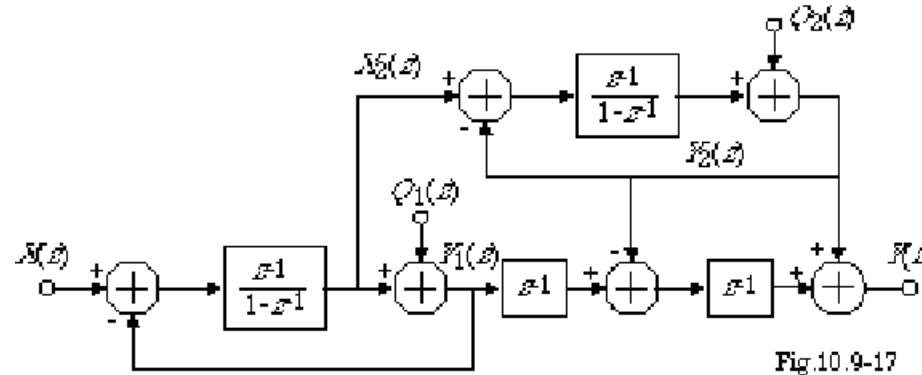
$$Y(z) = Q(z) + \left(\frac{z^{-1}}{1-z^{-1}} \right) [X(z) - Y(z)] \quad \rightarrow \quad Y(z) \left(\frac{1}{1-z^{-1}} \right) = Q(z) + \left(\frac{z^{-1}}{1-z^{-1}} \right) X(z)$$

$$\therefore Y(z) = (1-z^{-1})Q(z) + z^{-1}X(z) \quad \rightarrow \quad NTF_Q(z) = (1-z^{-1}) \quad \text{for } L = 1$$

ALTERNATIVE MODULATOR ARCHITECTURES

Since the single-loop architecture with order higher than 2 are unstable, it is necessary to find alternative architectures that allow stable higher order modulators.

Cascaded $\Delta\Sigma$ Modulator - Second-Order



$$Y_1(z) = (1-z^{-1})Q_1(z) + z^{-1}X(z)$$

$$X_2(z) = \left(\frac{z^{-1}}{1-z^{-1}} \right) (X(z) - Y_1(z)) = \left(\frac{z^{-1}}{1-z^{-1}} \right) X(z) - \left(\frac{z^{-1}}{1-z^{-1}} \right) [(1-z^{-1})Q_1(z) + z^{-1}X(z)]$$

$$\begin{aligned} Y_2(z) &= (1-z^{-1})Q_2(z) + z^{-1}X_2(z) = (1-z^{-1})Q_2(z) + \left(\frac{z^{-2}}{1-z^{-1}} \right) X(z) - z^{-2}Q_1(z) - \left(\frac{z^{-2}}{1-z^{-1}} \right) X(z) \\ &= (1-z^{-1})Q_2(z) - z^{-2}Q_1(z) \end{aligned}$$

$$Y(z) = Y_2(z) - z^{-1}Y_2(z) + z^{-2}Y_1(z) = (1-z^{-1})Y_2(z) + z^{-2}Y_1(z)$$

$$= (1-z^{-1})^2 Q_2(z) - (1-z^{-1})z^{-2}Q_1(z) + (1-z^{-1})z^{-2}Q_1(z) + z^{-3}X(z) = (1-z^{-1})^2 Q_2(z) + z^{-3}X(z)$$

$$\therefore Y(z) = (1-z^{-1})^2 Q_2(z) + z^{-3}X(z)$$

ALTERNATIVE MODULATOR ARCHITECTURES - CONTINUED

MASH Architecture - Third Order

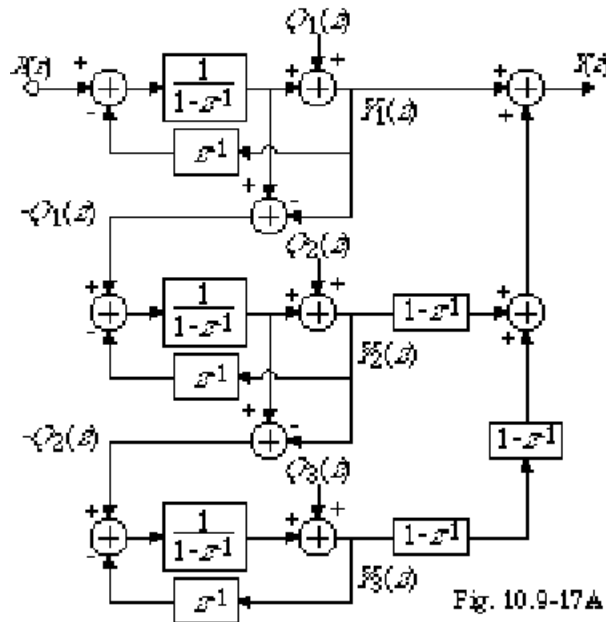


Fig. 10.9-17A

It can be shown that

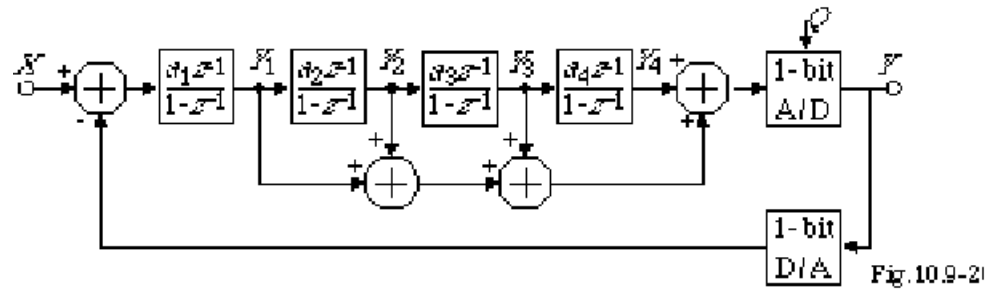
$$Y(z) = X(z) + (1-z^{-1})^3 Q_3(z)$$

Comments:

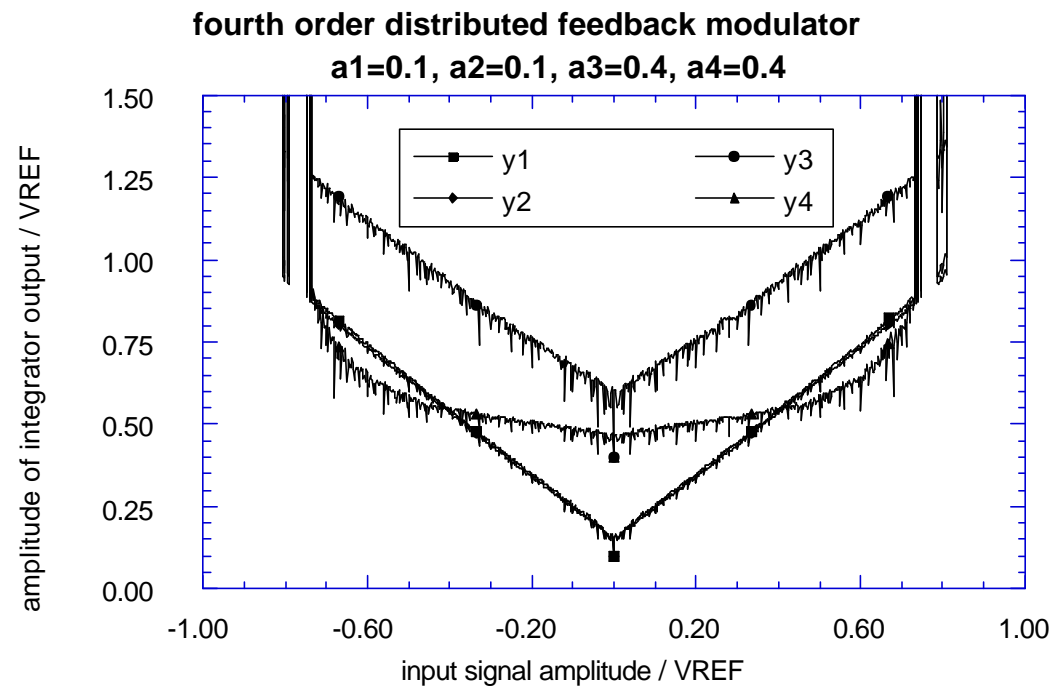
- The above structures that eliminate the noise of all quantizers except the last are called *MASH* or multistage architectures.
- Digital error cancellation logic is used to remove the quantization noise of all stages, except that of the last one.

ALTERNATIVE MODULATOR ARCHITECTURES - CONTINUED

Distributed Feedback $\Delta\Sigma$ Modulator - Fourth-Order

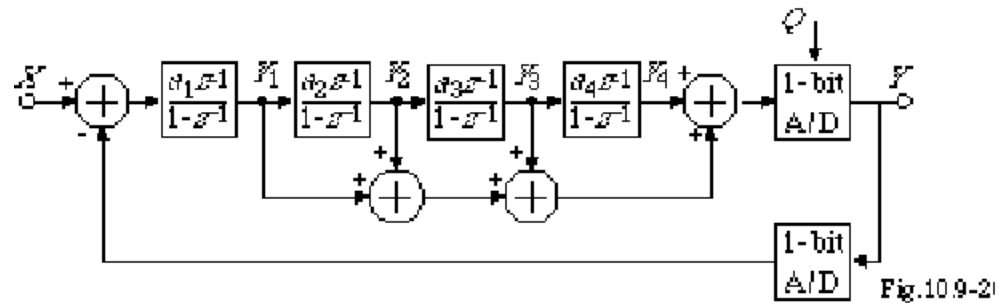


Amplitude of integrator outputs:

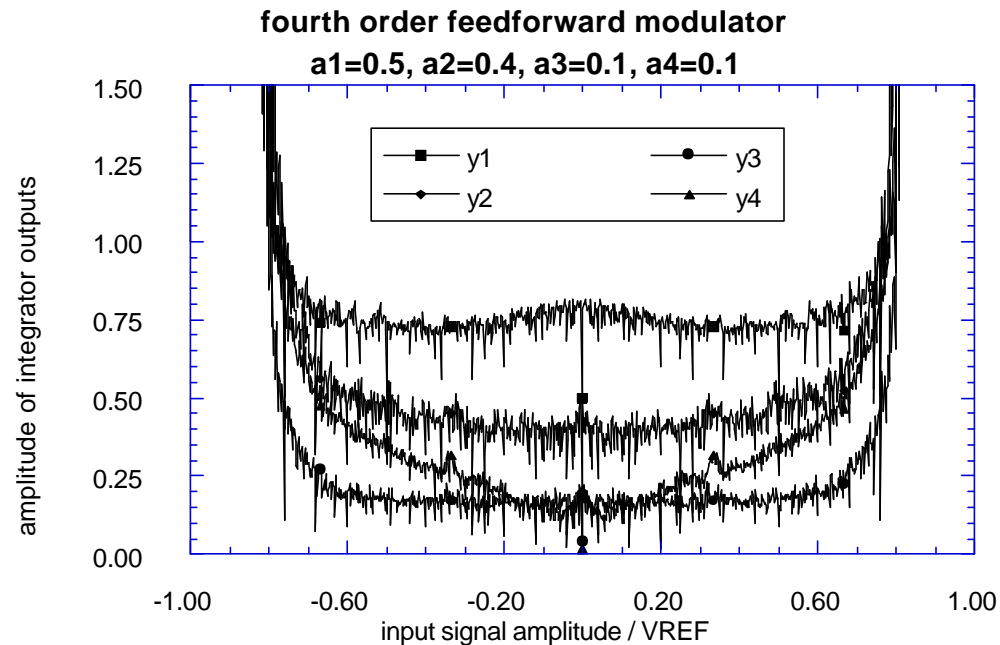


ALTERNATIVE MODULATOR ARCHITECTURES - CONTINUED

Distributed Feedback $\Delta\Sigma$ Modulator - Fourth-Order



Amplitude of integrator outputs:



ALTERNATIVE MODULATOR ARCHITECTURES - CONTINUED

Cascaded of a Second-Order Modulator with a First-Order Modulator

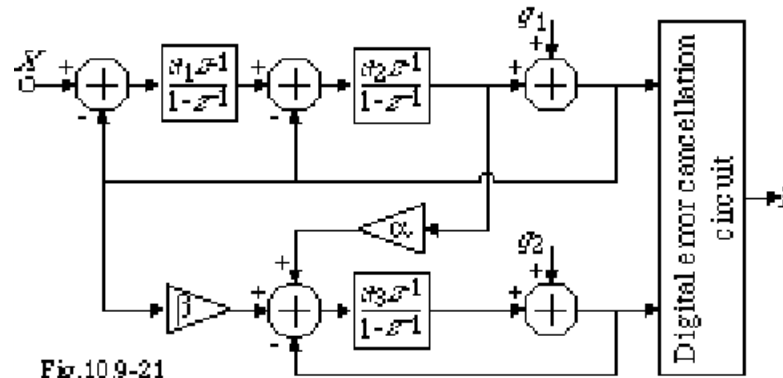
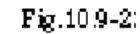


Fig.10.9-21

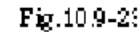
Comments:

- The stability is guaranteed for cascaded structures
- The maximum input range is almost equal to the reference voltage level for the cascaded structures
- All structures are sensitive to the circuit imperfection of the first stages
- The output of cascaded structures is multibit requiring a more complex digital decimator

Fundamental block of the $\Delta\Sigma$ modulator:



Fully-Differential, Switched Capacitor Implementation:



It can be shown (Chapter 9) that,

$$\frac{V_{out}(z)}{V_{in}(z)} = \left(\frac{C_s}{C_i} \right) \left(\frac{z^{-1}}{1-z^{-1}} \right) \Rightarrow \frac{V_{out}^o(e^{j\omega T})}{V_{in}^o(e^{j\omega T})} = \left(\frac{C_1}{C_2} \right) \frac{e^{-j\omega T/2}}{j2 \sin(\omega T/2)} \left(\frac{\omega T}{\omega T} \right) = \left(\frac{C_1}{j\omega T C_2} \right) \left(\frac{\omega T/2}{\sin(\omega T/2)} \right) (e^{-j\omega T/2})$$

$$\frac{V_{out}^o(e^{j\omega T})}{V_{in}^o(e^{j\omega T})} = (\text{Ideal}) \times (\text{Magnitude error}) \times (\text{Phase error}) \text{ where } \omega T = \frac{C_1}{T C_2} \Rightarrow \text{Ideal} = \frac{\omega T}{j\omega T}$$

POWER DISSIPATION VS. SUPPLY VOLTAGE AND OVERSAMPLING RATIO

The following is based on the above switched-capacitor integrator:

1.) Dynamic range:

The noise in the band $[-f_s, f_s]$ is kT/C while the noise in the band $[-f_s/2M, f_s/2M]$ is kT/MC . We must multiply this noise by 4; x2 for the sampling and integrating phases and x2 for differential operation.

$$\therefore DR = \frac{\frac{V_{DD}^2}{2}}{\frac{4kT}{MC_s}} = \frac{V_{DD}^2 MC_s}{8kT}$$

2.) Lower bound on the sampling capacitor, C_s :

$$C_s = \frac{8kT \cdot DR}{V_{DD}^2 M}$$

3.) Static power dissipation of the integrator:

$$P_{int} = I_b V_{DD}$$

4.) Settling time for a step input of $V_{o,max}$:

$$I_b = C \frac{V_{o,max}}{T_{settle}} = \left(\frac{C_i}{T_{settle}} \right) \left(\frac{C_s}{C_i} V_{DD} \right) = \frac{C_s V_{DD}}{T_{settle}} = C_s V_{DD} (2f_s) = 2Mf_N C_s V_{DD}$$

$$\therefore P_{int} = 2Mf_N C_s V_{DD}^2 = 16kT \cdot DR \cdot f_N$$

Because of additional feedback signal to the first integrator, the maximum voltage can be as large as $2V_{DD}$.

$$P_{1st-int} = 32kT \cdot DR \cdot f_N$$

Note that the power dissipation is a strong function of the dynamic range or number of bits.

IMPLEMENTATION OF DS MODULATORS

Most of today's delta-sigma modulators use fully differential switched capacitor implementations.

Advantages are:

- Doubles the signal swing and increases the dynamic range by 6dB
- Common-mode signals that may couple to the signal through the supply lines and substrate are canceled
- Charge injected by the switches are canceled to a first-order

Example:

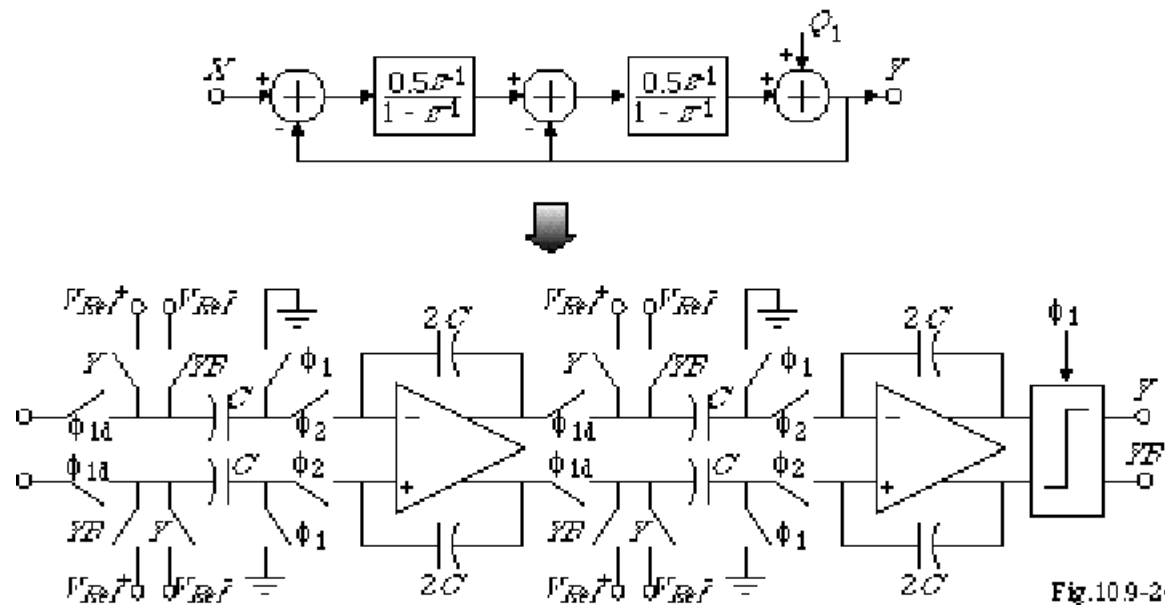
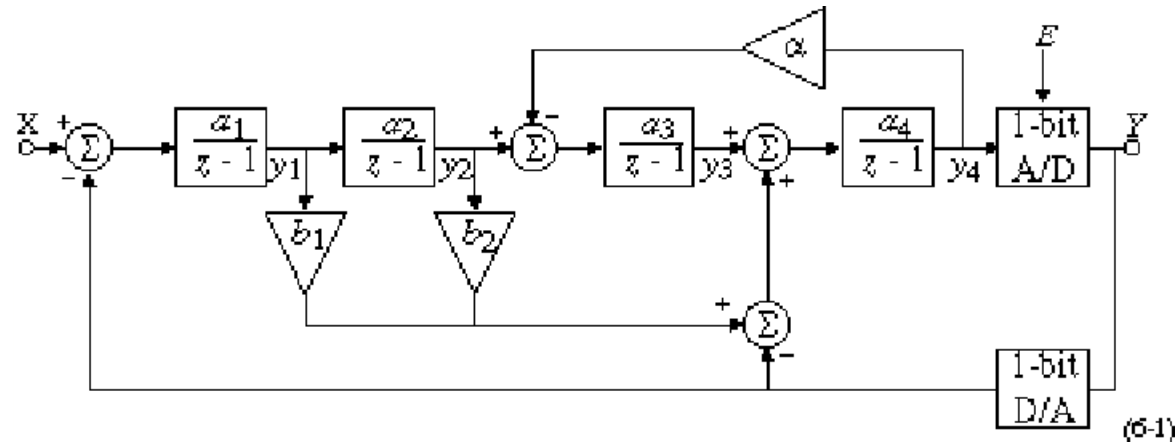


Fig.10.9-2:

First integrator dissipates the most power and requires the most accuracy.

EXAMPLE - 1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER[†]

where $a_1 = 1/3$, $a_2 = 3/25$, $a_3 = 1/10$, $a_4 = 1/10$, $b_1 = 6/5$, $b_2 = 1$ and $a = 1/6$

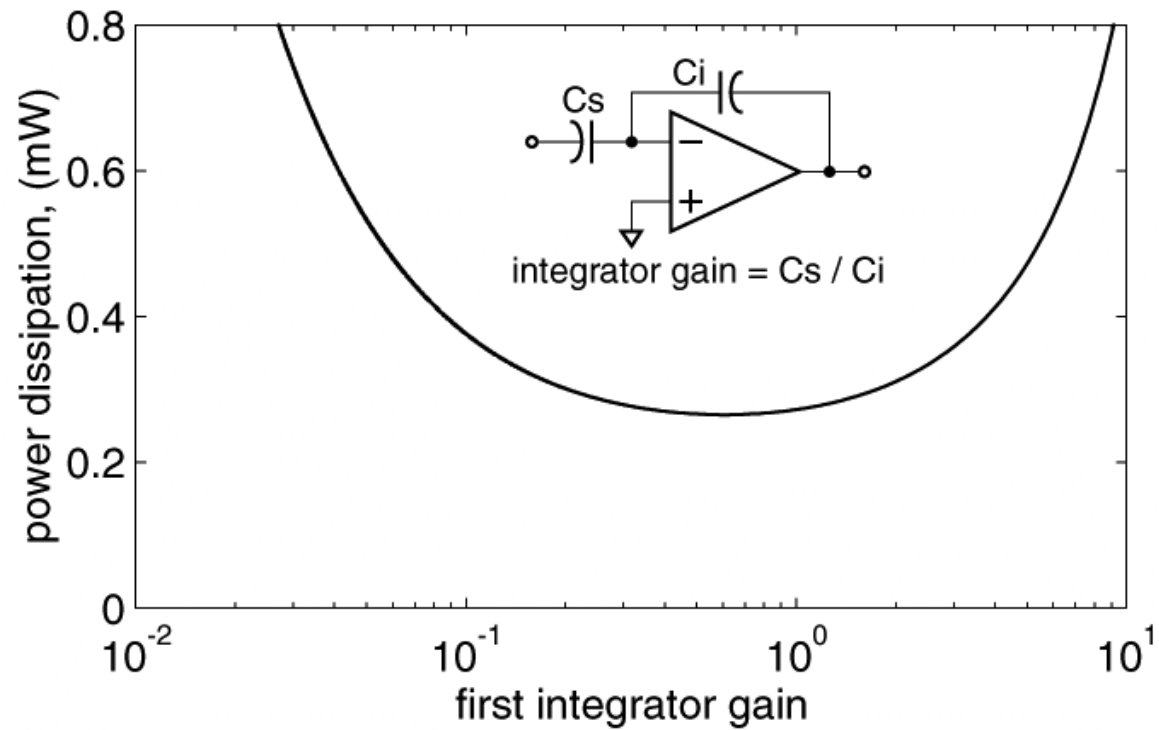
Advantages:

- The modulator combines the advantages of both DFB and DFF type modulators:
Only four op amps are required.
The first integrator's output swing is confined between $\pm V_{REF}$ for large input signal amplitudes ($0.6V_{REF}$), even if the integrator gain is large (0.5).
- A local resonator is formed by the feedback around the last two integrators to further suppress the quantization noise.
- The modulator is fully pipelined for fast settling.

[†] A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio $\Delta\Sigma$ Modulator with 98dB Dynamic Range," *Proc. of 1999 Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 50-51.

1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUED

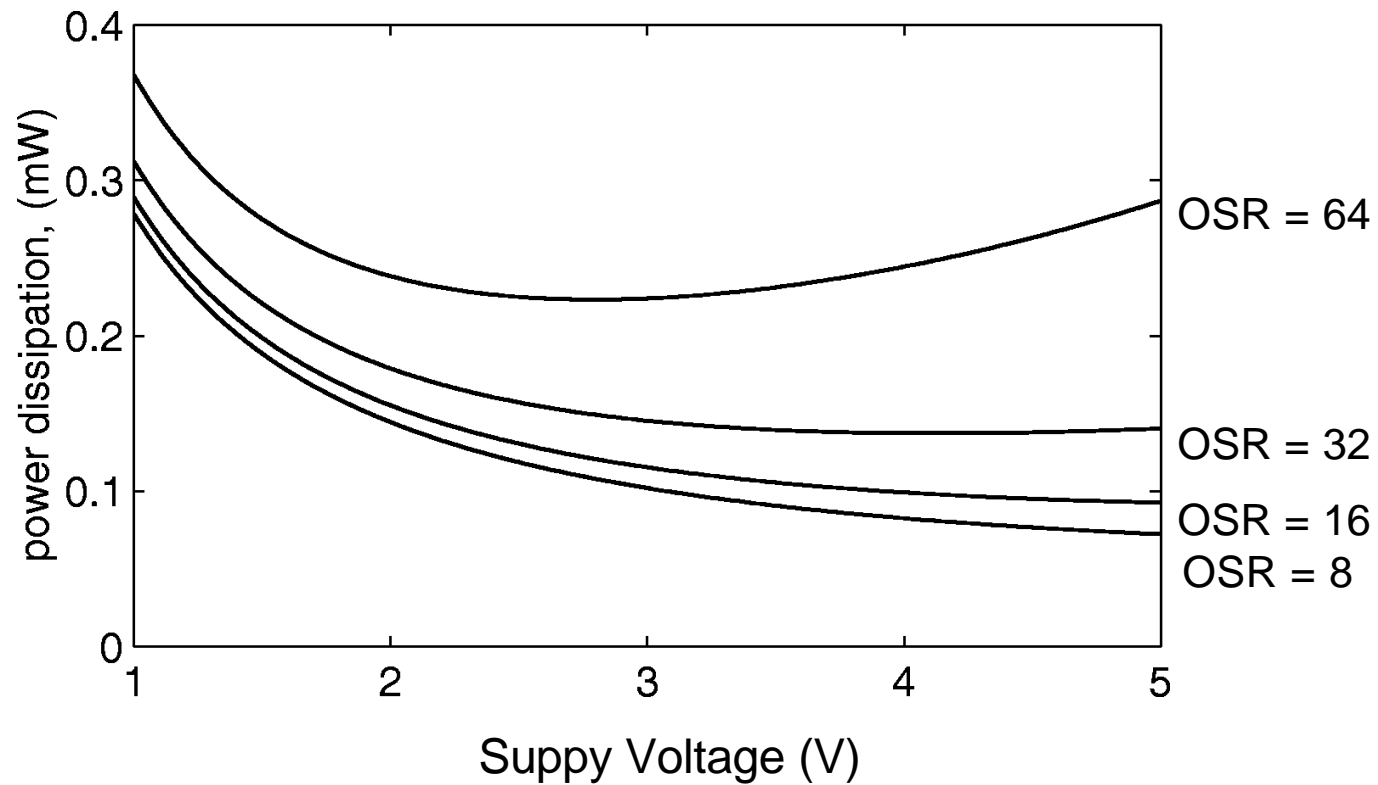
Integrator power dissipation vs. integrator gain



$DR = 98 \text{ dB}$
 $BW = 20 \text{ kHz}$
 $C_s = 5 \text{ pF}$
 $0.5 \mu\text{m CMOS}$

1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUED

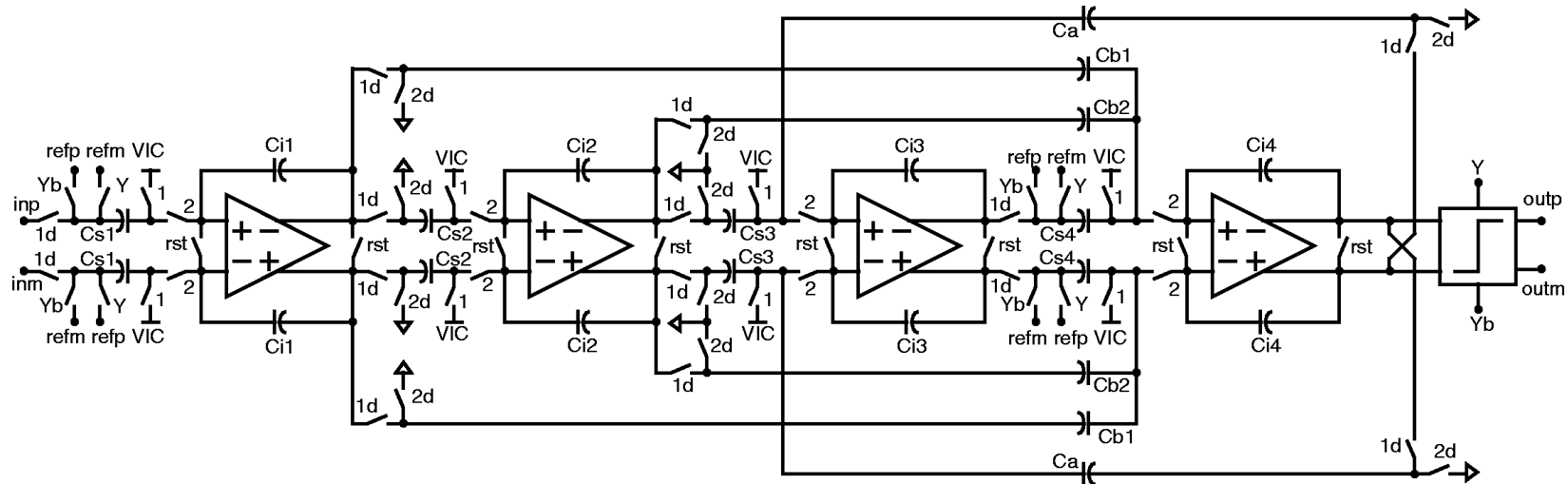
Modulator power dissipation vs. oversampling ratio

 $DR = 98 \text{ dB}$ $BW = 20 \text{ kHz}$ Integrator gain = $1/3$

0.5 μ m CMOS

1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUED

Circuit Implementation



Capacitor Values

Capacitor	Integrator 1	Integrator 2	Integrator 3	Integrator 4
C_s	5.00pF	0.15pF	0.30pF	0.10pF
C_i	15.00pF	1.25pF	3.00pF	1.00pF
C_a	-	-	0.05pF	-
C_{b1}	-	-	-	0.12pF
C_{b2}	-	-	-	0.10pF

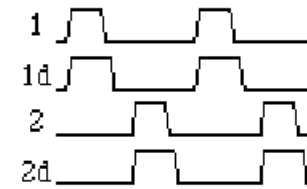
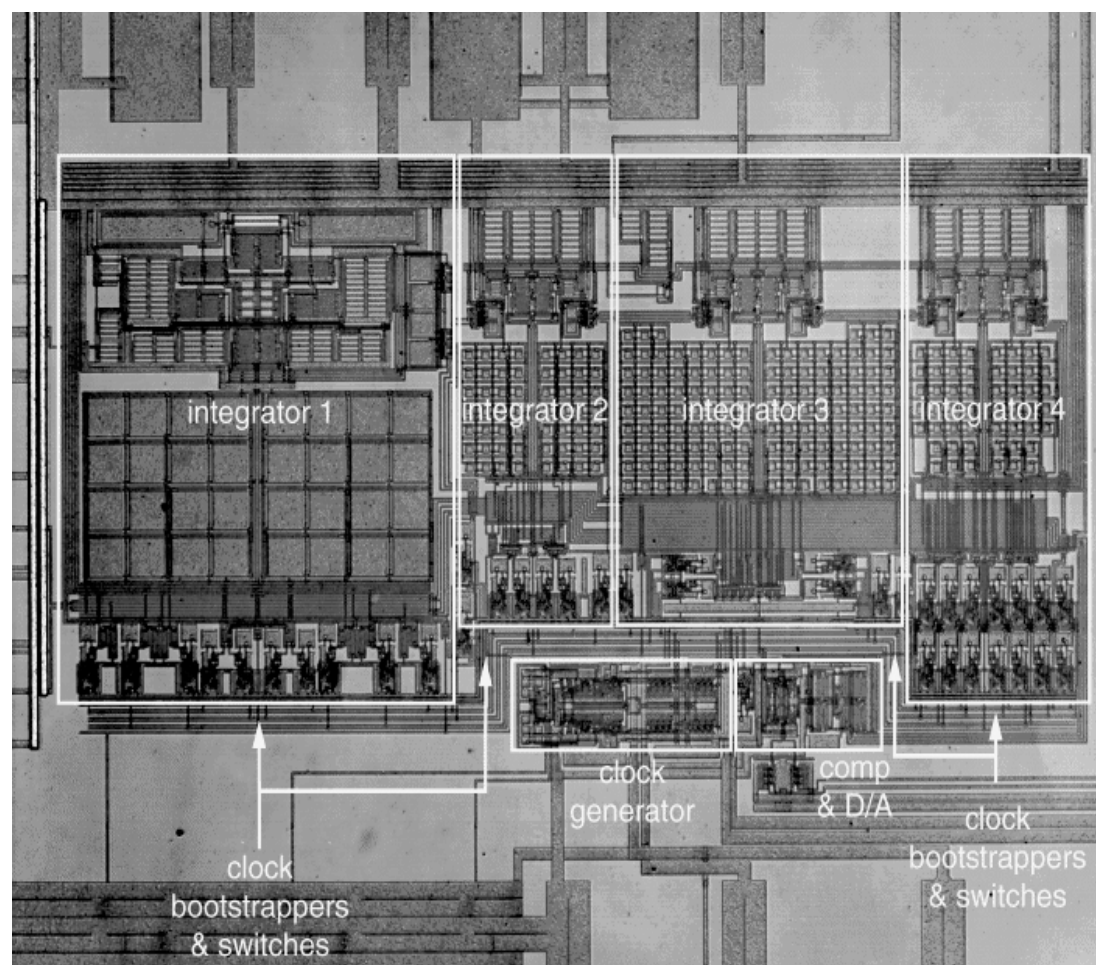


Fig.10.9-25

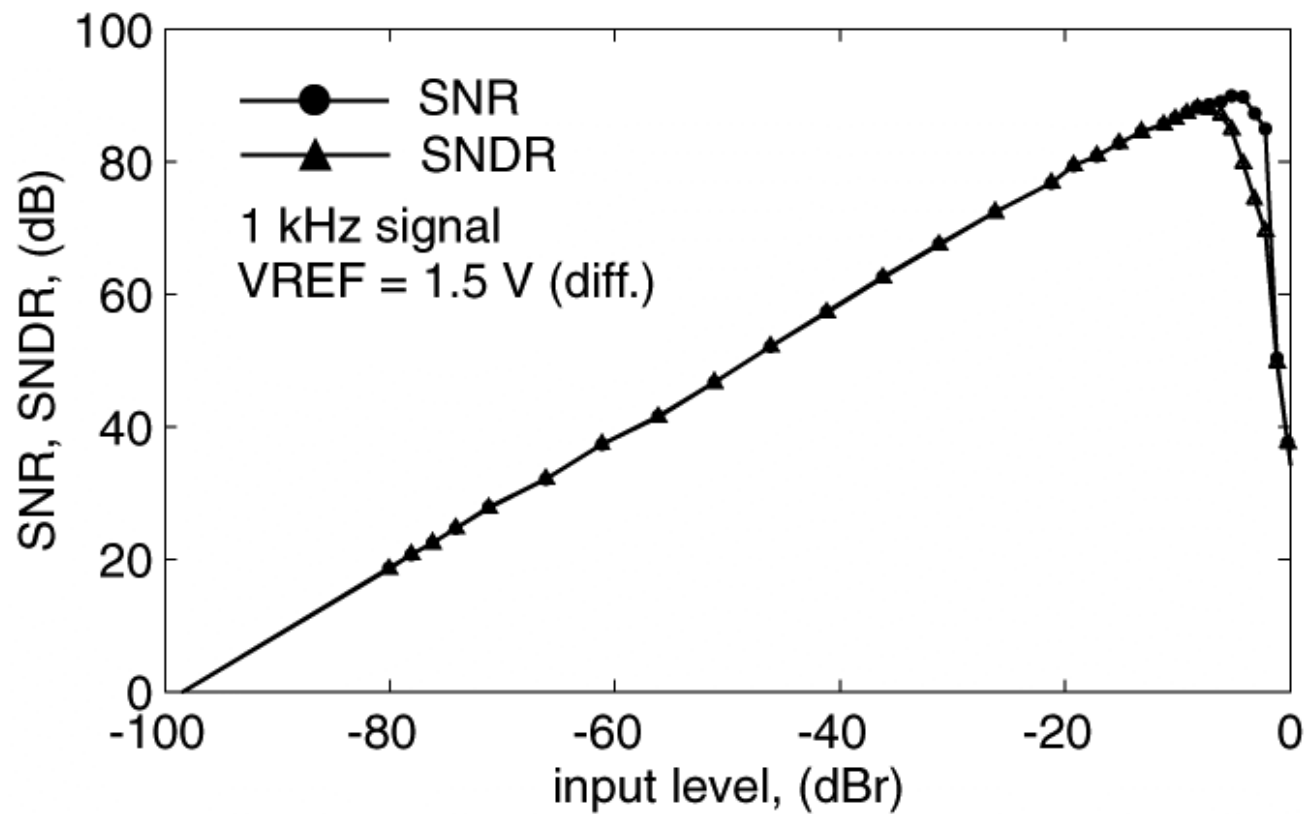
1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUED

Microphotograph of the experimental $\Delta\Sigma$ modulator.



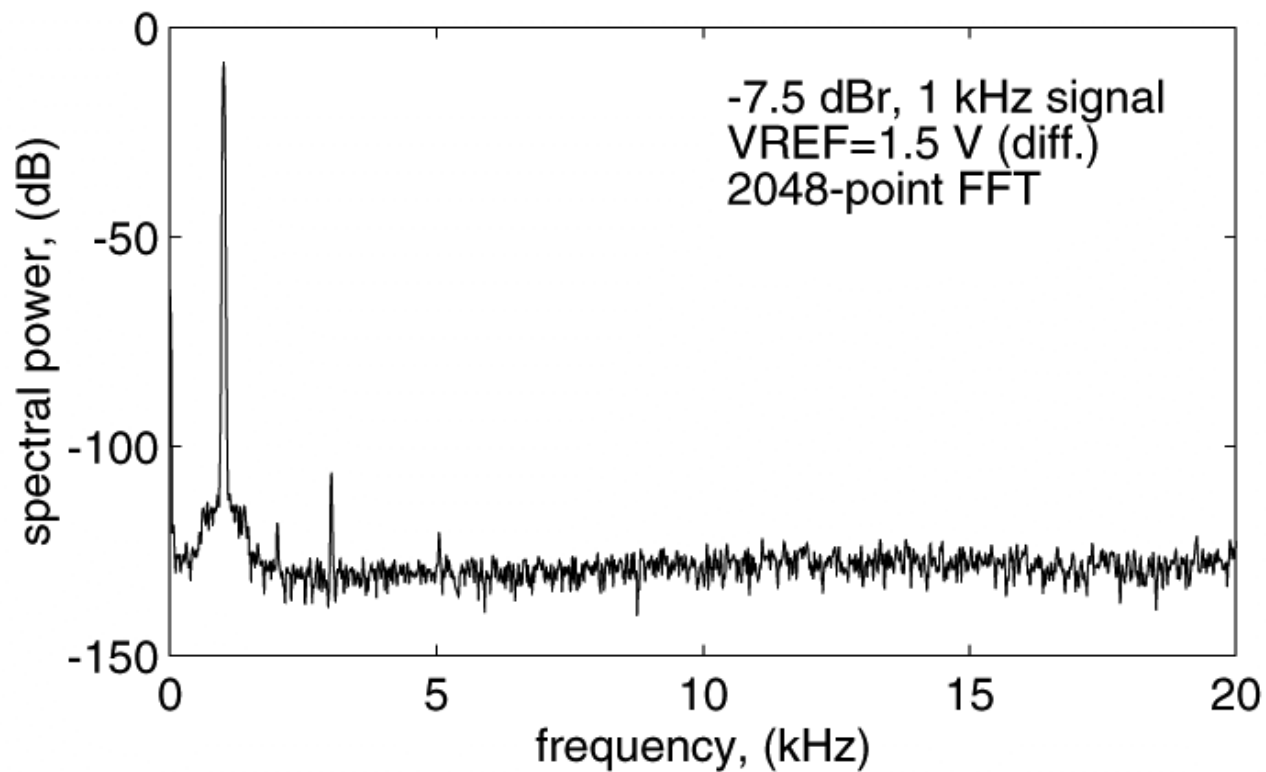
1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUED

Measured SNR and SNDR versus input level of the modulator.



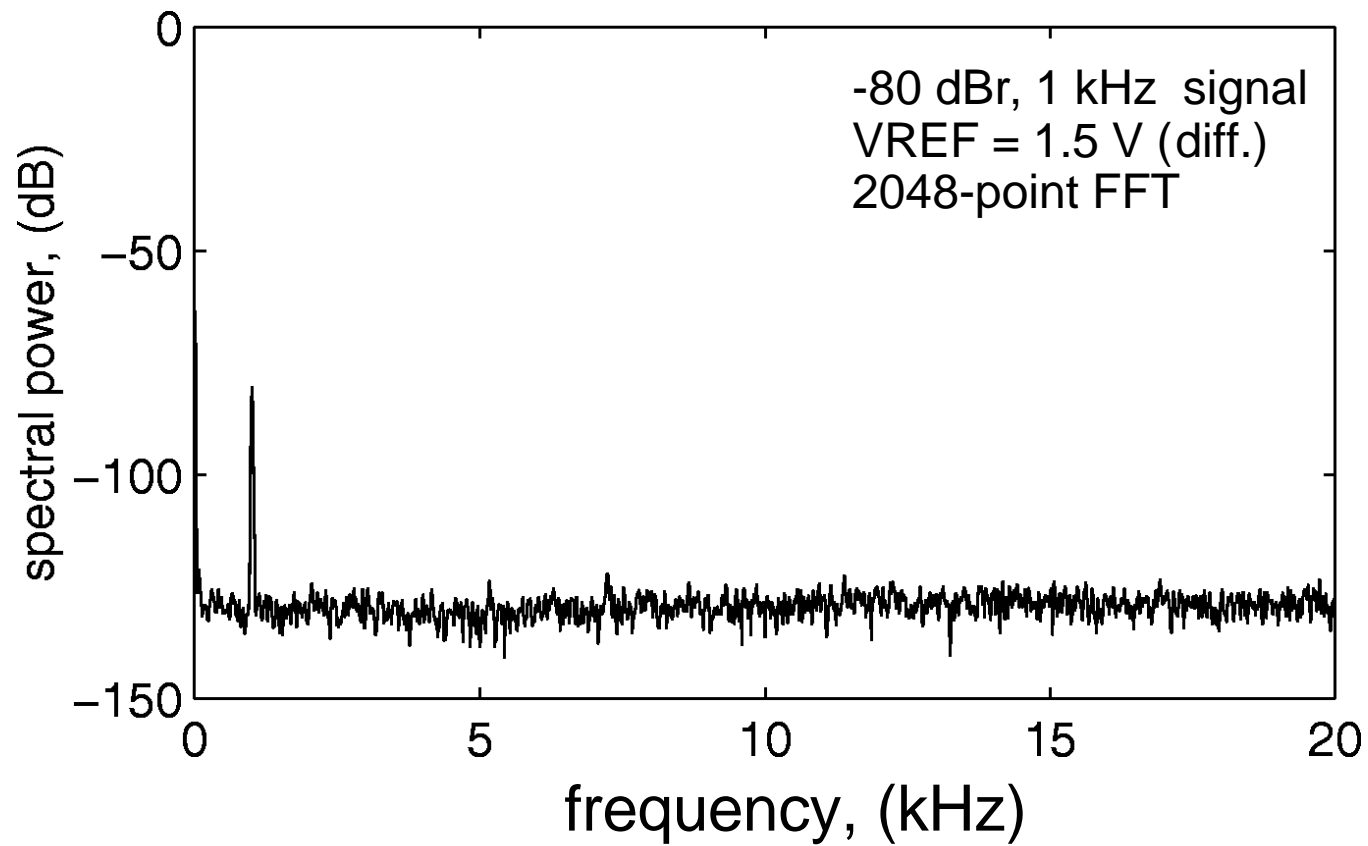
1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUED

Measured baseband spectrum for a -7.5dBr 1kHz input.



1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUED

Measured baseband spectrum for a -80dB_r 1kHz input.



1.5V, 1mW, 98dB DS ANALOG-DIGITAL CONVERTER - CONTINUEDMeasured 4th-Order $\Delta\Sigma$ Modulator Characteristics:

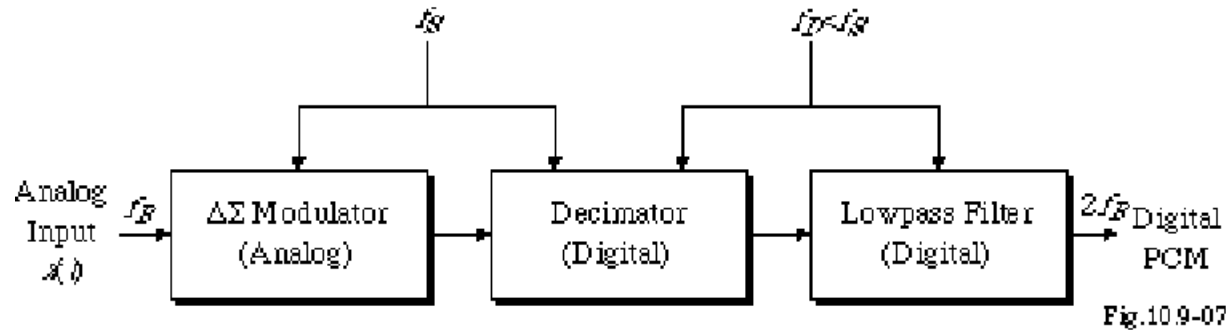
Table 5.4

Measured fourth-order delta-sigma modulator characteristics

Technology : 0.5 μm triple-metal single-poly n-well CMOS process

Supply voltage	1.5 V
Die area	1.02 mm x 0.52 mm
Supply current	660 μA
analog part	630 μA
digital part	30 μA
Reference voltage	0.75V
Clock frequency	2.8224MHz
Oversampling ratio	64
Signal bandwidth	20kHz
Peak SNR	89 dB
Peak SNDR	87 dB
Peak S/D	101dB
HD ₃ @ -5dBv 2kHz input	-105dBv
DR	98 dB

DECIMATION AND FILTERING



The decimator and filter are implemented digitally and occupy most of the area and consume most of the power.

Function of the decimator and filter are;

- 1.) To attenuate the quantization noise above the baseband
- 2.) Bandlimit the input signal
- 3.) Suppress out-of-band spurious signals and circuit noise

Most of the $\Delta\Sigma$ ADC applications demand decimation filters with linear phase characteristics which leads to the use of finite impulse response (FIR) filters.

FIR filters:

For a specified ripple and attenuation,

$$\text{Number of filter coefficients} \propto \frac{f_s}{f_t}$$

where f_s is the input rate to the filter (clock frequency of the quantizer) and f_t is the transition bandwidth.

To reduce the number of stages, the decimation filters are implemented in several stages.

A MULTI-STAGE DECIMATION FILTER

Typical multi-stage decimation filter:

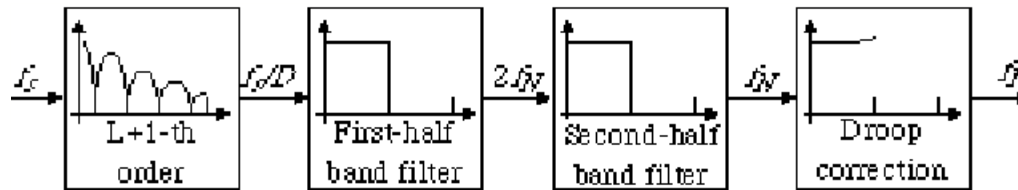


Fig. 10.9-26

- 1.) For $\Delta\Sigma$ modulators with $(1-z^{-1})^L$ noise shaping comb filters are very efficient.
 - Comb filters are suitable for reducing the sampling rate to four times the Nyquist rate.
 - Designed to suppress the quantization noise that would otherwise alias into the signal band upon sampling at an intermediate rate of f_{s1} .
- 2.) The remaining filtering is performed by in stages by FIR or IIR filters.
 - Suppresses out-of-band components of the signal
- 3.) Droop correction - may be required depending upon the ADC specifications

COMB FILTERS

A comb filter that computes a running average of the last D input samples is given as

$$y[n] = \frac{1}{D} \sum_{i=0}^{D-1} x[n-i]$$

where D is the decimation factor given as

$$D = \frac{f_s}{f_{s1}}$$

The corresponding z -domain expression is,

$$H_D(z) = \sum_{i=1}^D z^{-i} = \frac{1}{D} \frac{1 - z^{-D}}{1 - z^{-1}}$$

The frequency response is obtained by evaluating $H_D(z)$ for $z = e^{j2\pi f T_s}$,

$$H_D(f) = \frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} e^{-j2\pi f T_s / D}$$

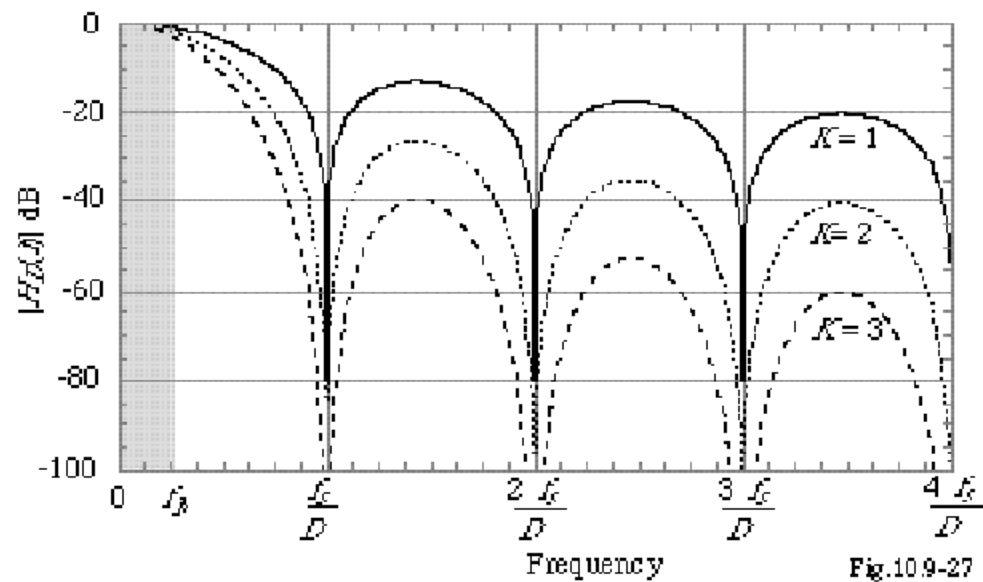
where T_s is the input sampling period ($=1/f_s$). Note that the phase response is linear.

For an L -th order modulator with a noise shaping function of $(1-z^{-1})^L$, the required number of comb filter stages is $L+1$. The magnitude of such a filter is,

$$|H_D(f)| = \left(\frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} \right)^K$$

MAGNITUDE RESPONSE OF A CASCADED COMB FILTER

$K = 1, 2$ and 3



IMPLEMENTATION OF A CASCADED COMB FILTER

Implementation:

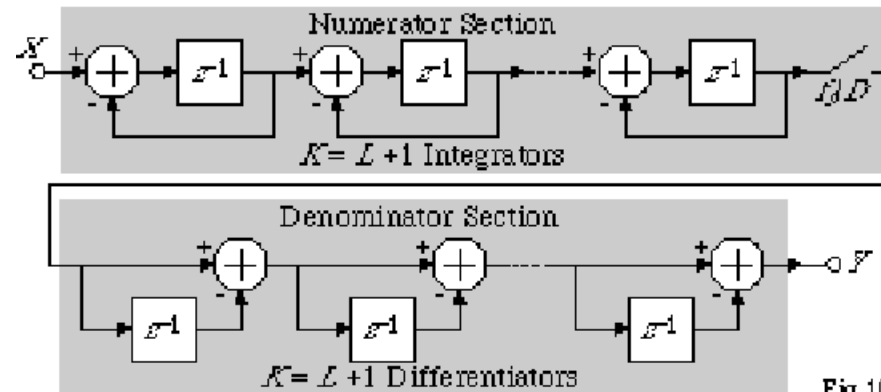


Fig.10.9-2

Comments:

- 1.) The $L+1$ integrators operating at the sampling frequency, f_s , realize the denominator of $H_D(z)$.
- 2.) The $L+1$ differentiators operating at the output rate of $f_{s1} (= f_s/D)$ realize the numerator of $H_D(z)$.
- 3.) Placing the integrator delays in the feedforward path reduces the critical path from $L+1$ adder delays to a single adder delay.

IMPLEMENTATION OF DIGITAL FILTERS[†]

Digital filter structures:

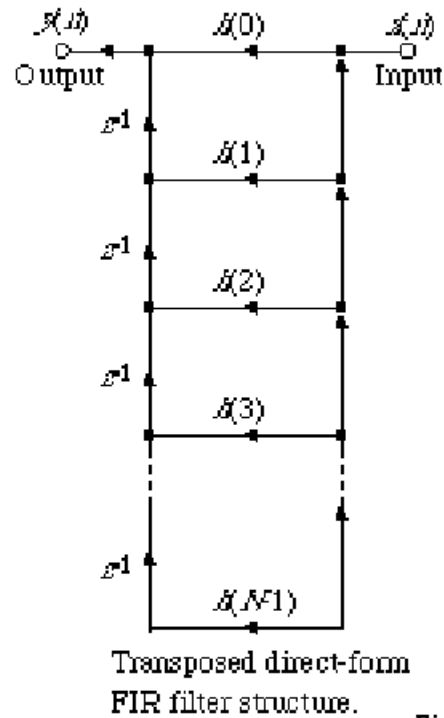
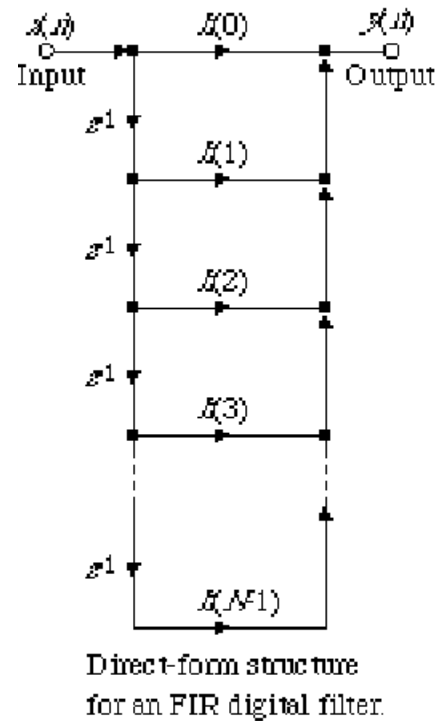


Fig.10.9-2

[†] S.R. Norsworthy, R. Schreier, and G.C. Temes, *Delta-Sigma Data Converters-Theory, Design, and Simulation*, IEEE Press, NY, Chapter 13, 1997.

DIGITAL LOWPASS FILTER

Example of a typical digital filter used in removal of the quantization noise at higher frequencies

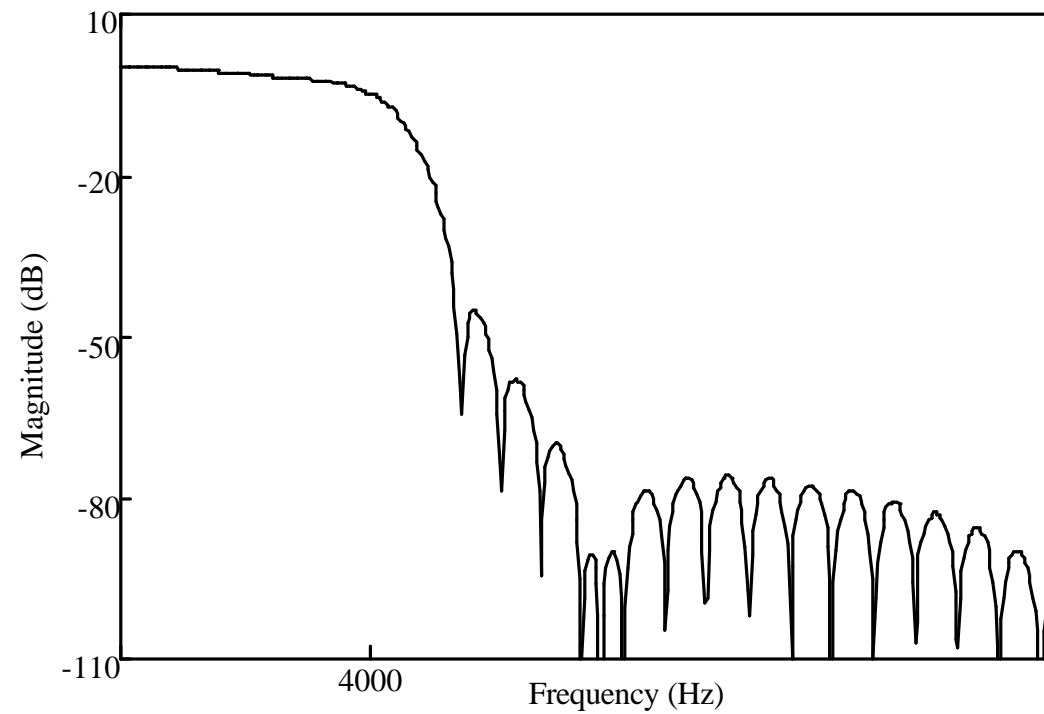
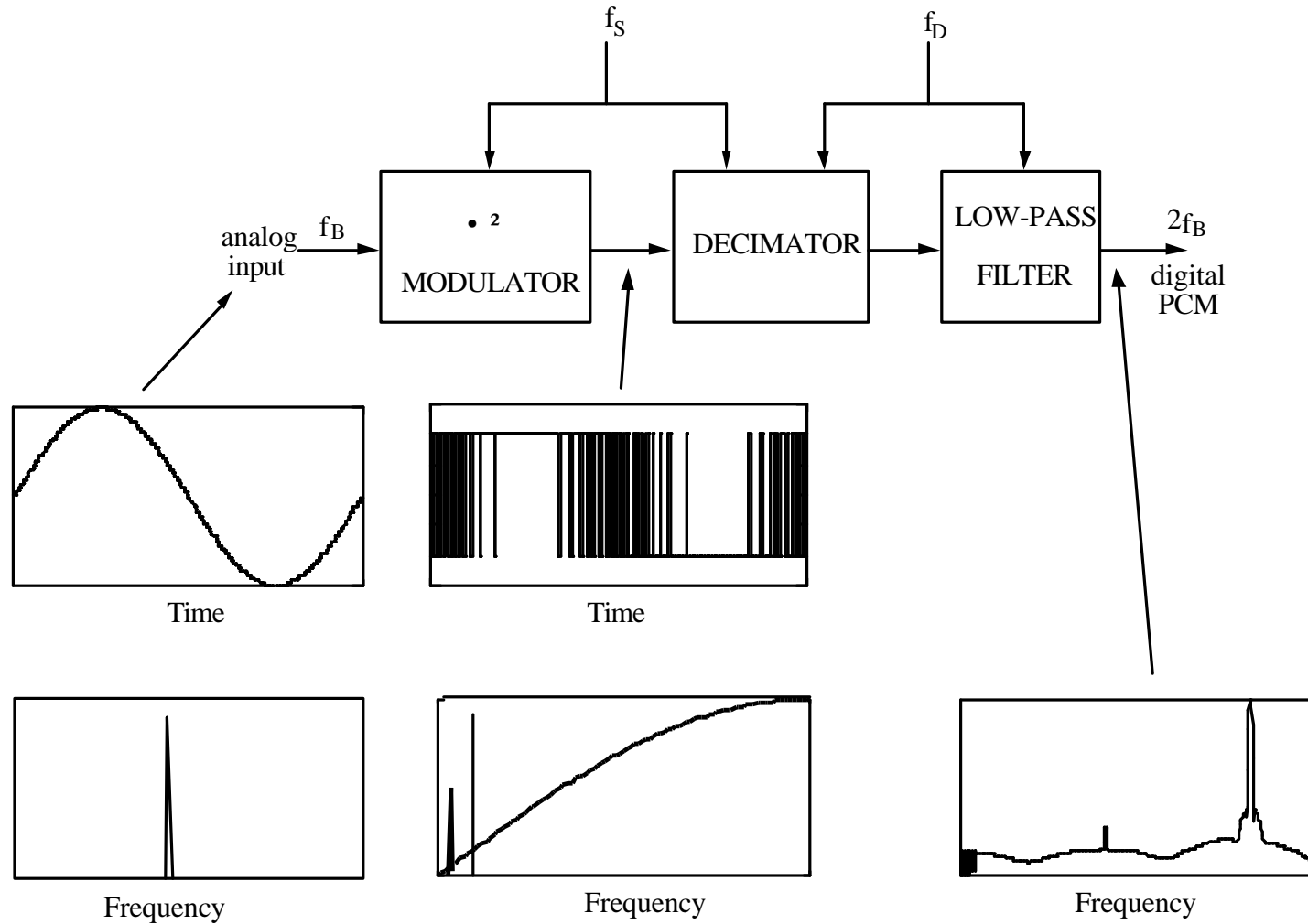


ILLUSTRATION OF THE DELTA-SIGMA ADC IN TIME AND FREQUENCY DOMAIN

BANDPASS DS MODULATORS

Block diagram of a bandpass modulator:

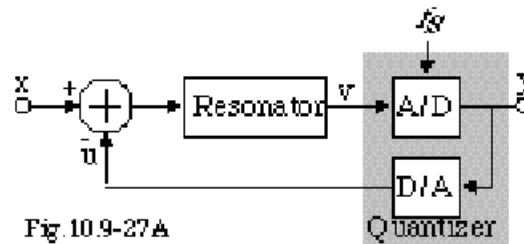


Fig. 10.9-27A

Components:

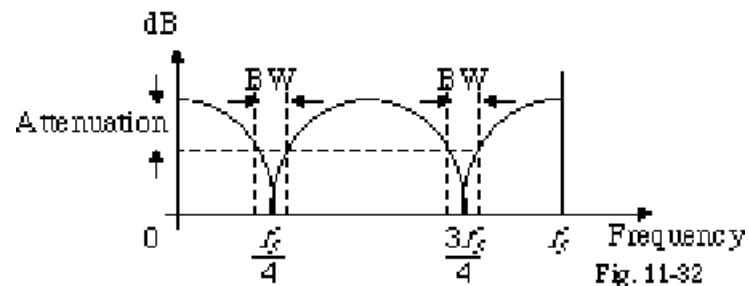
- Resonator - a bandpass filter of order $2N$, $N = 1, 2, \dots$
- Coarse quantizer (1 bit or multi-bit)

The noise-shaping of the bandpass oversampled ADC has the following interesting characteristics:

$$\text{Center frequency} = f_s \cdot (2N-1)/4$$

$$\text{Bandwidth} = BW = f_s / M$$

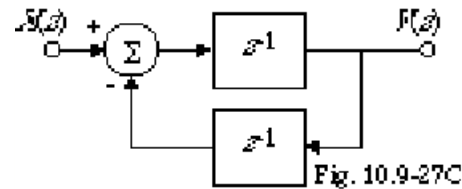
Illustration of the Frequency Spectrum ($N=1$):



Application of the bandpass $\Delta\Sigma$ ADC is for systems with narrowband signals (IF frequencies)

A FIRST-ORDER DS BANDPASS MODULATOR

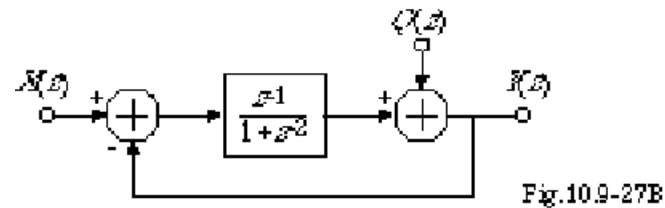
Bandpass Resonator:



$$V(z) = z^{-1} [X(z) - z^{-1}V(z)] = z^{-1}X(z) - z^{-2}V(z)$$

$$V(z) (1+z^{-2}) = z^{-1}X(z) \quad \rightarrow \quad \frac{V(z)}{X(z)} = \frac{z^{-1}}{1+z^{-2}}$$

Modulator:



$$Y(z) = Q(z) + [X(z) - Y(z)] \left(\frac{z^{-1}}{1+z^{-2}} \right) \quad \rightarrow \quad Y(z) = \left(\frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right) Q(z) + \left(\frac{z^{-1}}{1+z^{-1}-z^{-2}} \right) X(z)$$

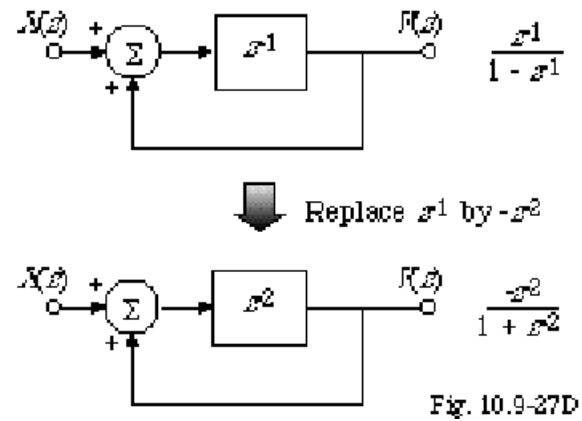
$X(z)$

$$NTF_Q(z) = \left(\frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right)$$

The $NTF_Q(z)$ has two zeros on the $j\omega$ axis.

RESONATOR DESIGN

Resonators can be designed by applying a lowpass to bandpass transform as follows:



Result:

- Simple way to design the resonator
- Inherits the stability of a lowpass modulator
- Center frequency located at $f_s/4$

FOUTH-ORDER BANDPASS DS MODULATOR

Block diagram:

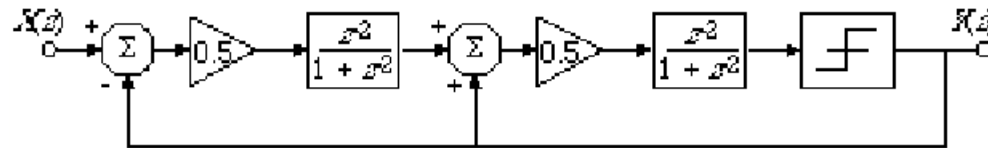


Fig. 10.9-27E

Comments:

- Designed by applying a lowpass to bandpass transform to a second-order lowpass $\Delta\Sigma$ modulator
- The stability and SNR characteristics are the same as those of a second-order lowpass modulator
- The z -domain output is given as,

$$Y(z) = z^{-4}X(z) + (1+z^{-2})^2Q(z)$$

- The zeros are located at $z = \pm j$ which corresponds to notches at $f_s/4$.

RESONATOR CIRCUIT IMPLEMENTATION

Block diagram of $z^{-2}/(1+z^{-2})$:

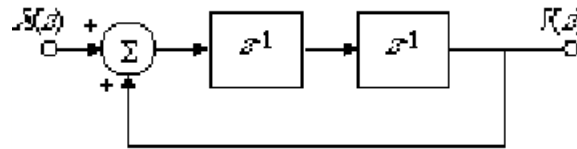


Fig. 10.9-27F

Fully differential switch-capacitor implementation:

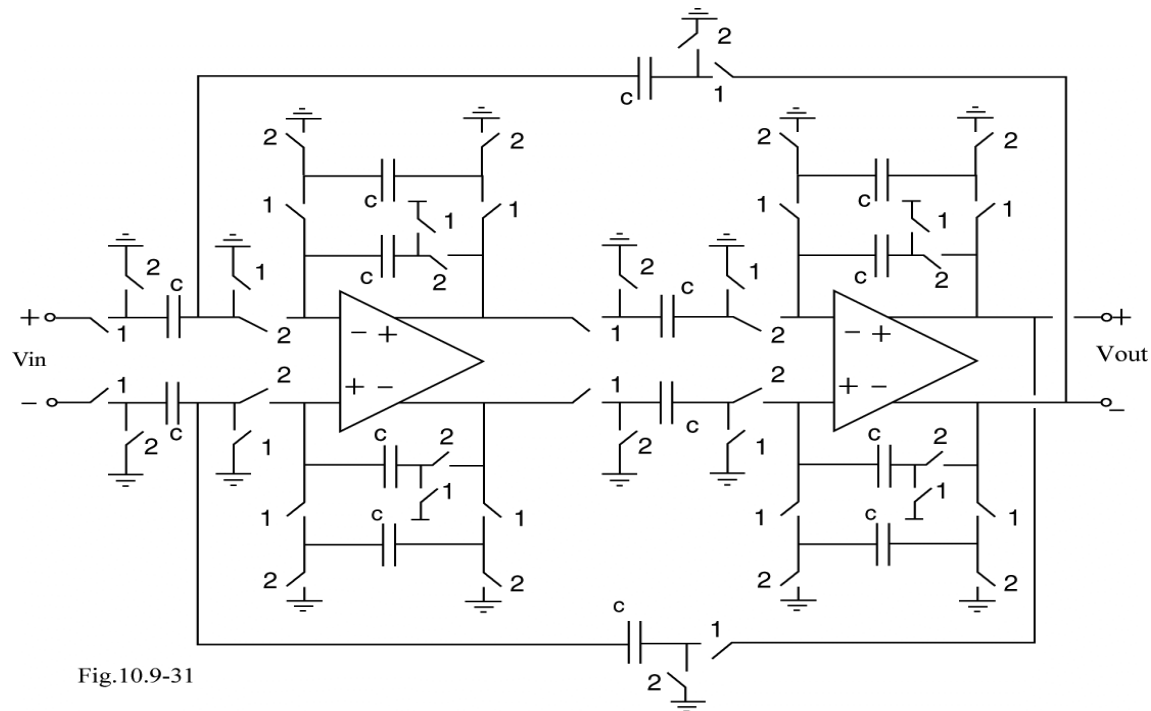
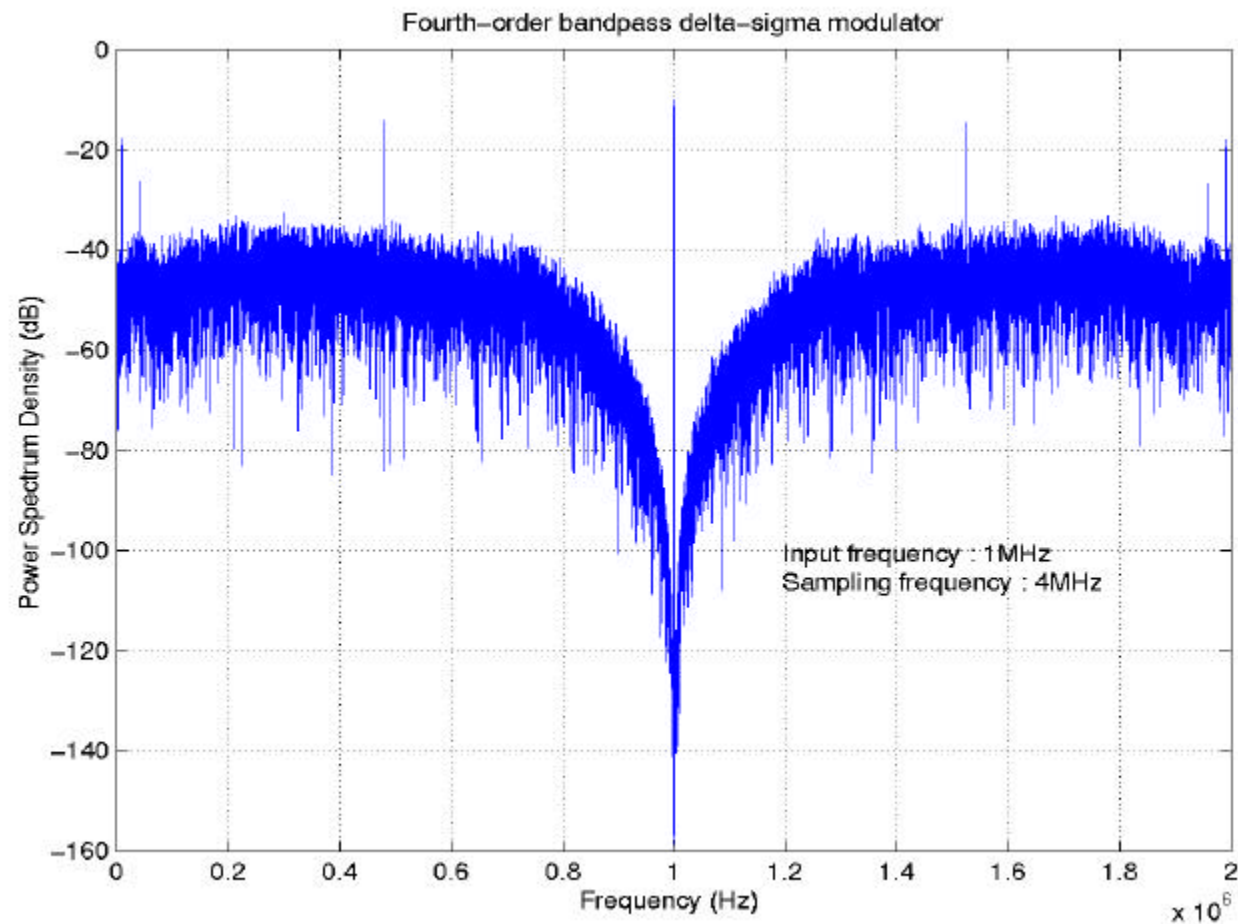


Fig.10.9-31

POWER SPECTRAL DENSITY OF THE PREVIOUS 4-TH ORDER BANDPASS DS MODULATOR

Simulated result:



APPLICATION OF THE BANDPASS DS ADC IN WIRELESS APPLICATIONS

Comparison of the classical versus the bandpass $\Delta\Sigma$ ADC approaches in wireless baseband:

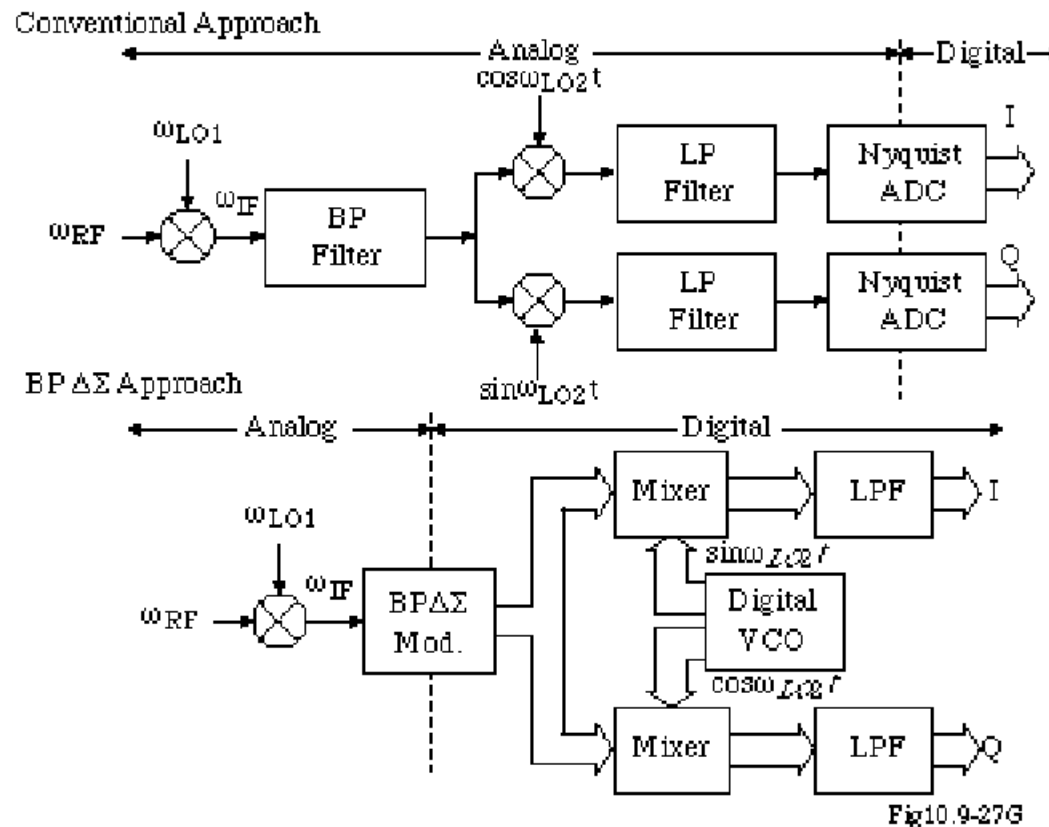


Fig10.9-27G

Assume an IF center frequency of 10MHz and BW of 200kHz:

Sampling frequency would be 40MHz and the OSR would be $40/0.2 = 200$ which is easily within capability.

Typical results (0.5 μ m CMOS):

$$f_s = 20\text{MHz}, f_{IF} = 15\text{MHz}, BW = 200\text{kHz}, DR = 80\text{dB}, \text{Supply current} = 5\text{mA}, \text{Supply voltage} = 2.7\text{V}$$

DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTERS

PRINCIPLES

The principles of oversampling and noise shaping are also widely used in the implementation of $\Delta\Sigma$ DACs.

Simplified block diagram of a delta-sigma DAC:

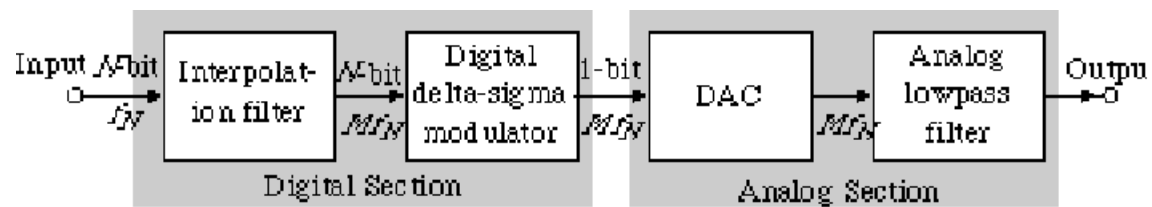
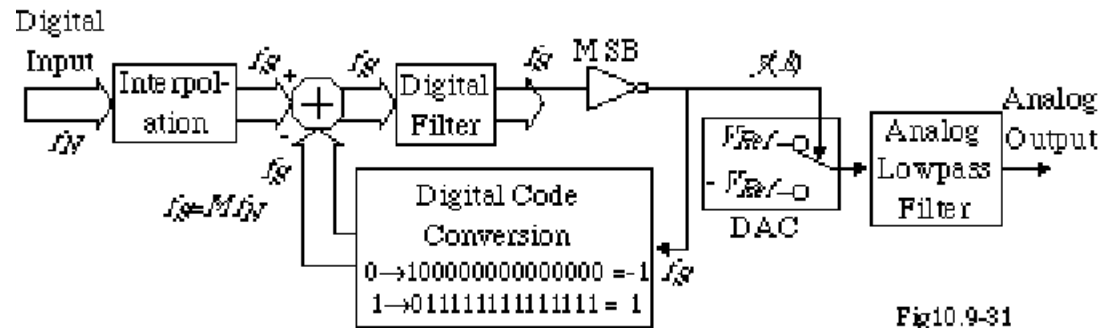


Fig10.9-29

Operation:

- 1.) A digital signal with N -bits with a data rate of f_N is sampled at a higher rate of Mf_N by means of an interpolator.
- 2.) Interpolation is achieved by inserting “0”s between each input word with a rate of Mf_N and then filtering with a lowpass filter.
- 3.) The MSB of the digital filter is applied to a DAC which is applied to an analog lowpass filter to achieve the analog output.

BLOCK DIAGRAM OF A DS DAC



Operation:

- 1.) Interpolate a digital word at the conversion rate of the converter (f_N) up to the sample frequency, f_s .
- 2.) The word length is then reduced to one bit with a digital sigma-delta modulator.
- 3.) The one bit PDM signal is converted to an analog signal by switching between two reference voltages.
- 4.) The high-frequency quantization noise is removed with an analog lowpass filter yielding the required analog output signal.

Sources of error:

- Device mismatch (causes harmonic distortion rather than DNL or INL)
- Component noise
- Device nonlinearities
- Clock jitter sensitivity
- Inband quantization error from the Δ - Σ modulator

1-BIT DAC FOR THE DS DIGITAL-TO-ANALOG CONVERTER - THE ANALOG PART

The MSB output from the digital filter is used to drive a 1-bit DAC.

Possible architectures:

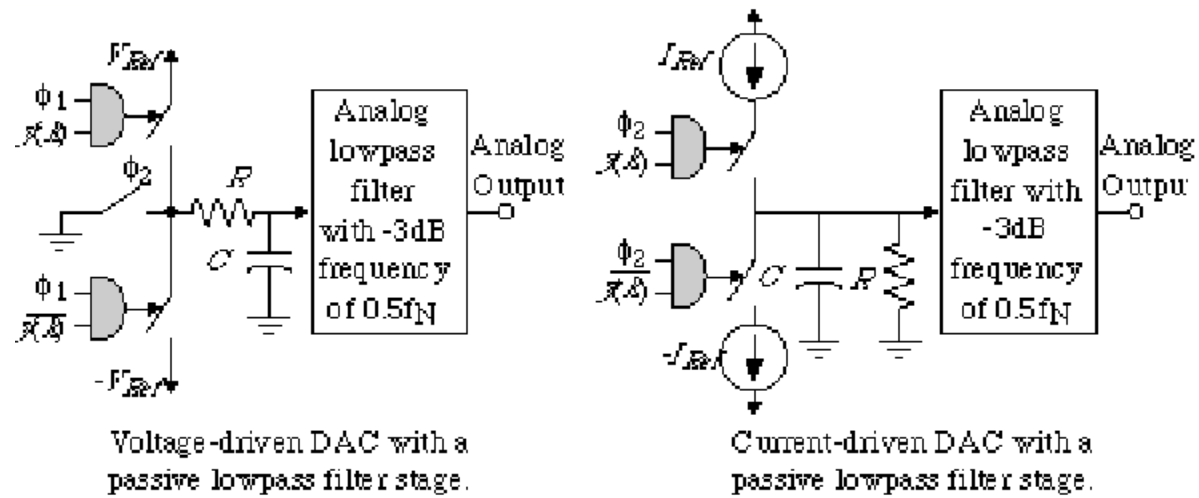


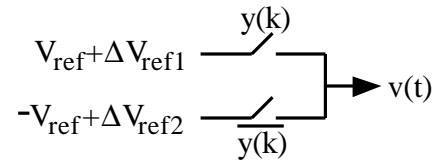
Fig10.9-32

ERRORS IN THE 1-BIT DAC

Offset Error:

$$V_{ref} \neq |-V_{ref}| \text{ or } I_{ref} \neq |-I_{ref}| \Rightarrow \text{Offset error}$$

Influence of offsets in the voltage reference:



The resulting transfer function is:

$$v(t) = V_{ref} + \mathbf{DV}_{ref1}, \quad y(k) = 1$$

or

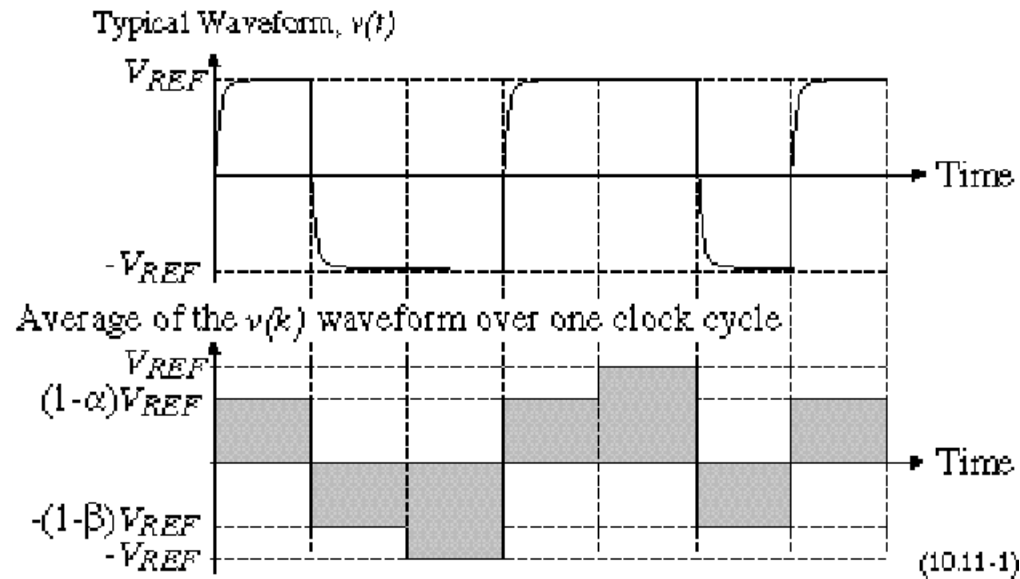
$$v(t) = -V_{ref} + \mathbf{DV}_{ref2}, \quad y(k) = -1$$

$$\therefore v(t) = \left(V_{ref} + \frac{\mathbf{DV}_{ref1} - \mathbf{DV}_{ref2}}{2} \right) y(k) + \frac{\mathbf{DV}_{ref1} + \mathbf{DV}_{ref2}}{2}$$

This results in a gain or an offset error, but the output is still linear.

ERRORS IN THE 1-BIT DAC - CONTINUED

Switching Time Error:



Let, $v(k) = V_{REF}$, $y(k) = 1$ and $y(k-1) = 1$

$v(k) = (1-\alpha)V_{REF}$, $y(k) = 1$ and $y(k-1) = -1$

$v(k) = -V_{REF}$, $y(k) = -1$ and $y(k-1) = -1$

$v(k) = -(1-\beta)V_{REF}$, $y(k) = -1$ and $y(k-1) = 1$

Therefore, the transfer function becomes,

$$v(k) = [(\beta - \alpha) + (\alpha + \beta)y(k-1) + (4 - \alpha - \beta)y(k) + (\alpha - \beta)y(k) \cdot y(k-1)] \frac{V_{REF}}{4}$$

(Note: The f_2 switch in the voltage DAC removes this error by resetting the voltage at every clock.)

SWITCHED-CAPACITOR DAC AND FILTER

Typically, the DAC and the first stage of the lowpass filter are implemented using switched-capacitor techniques.

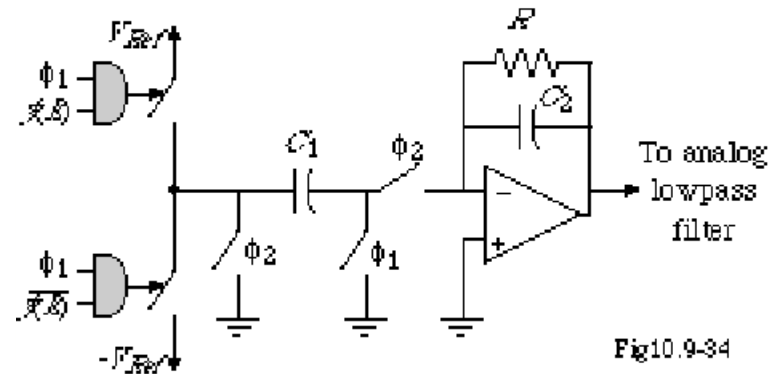
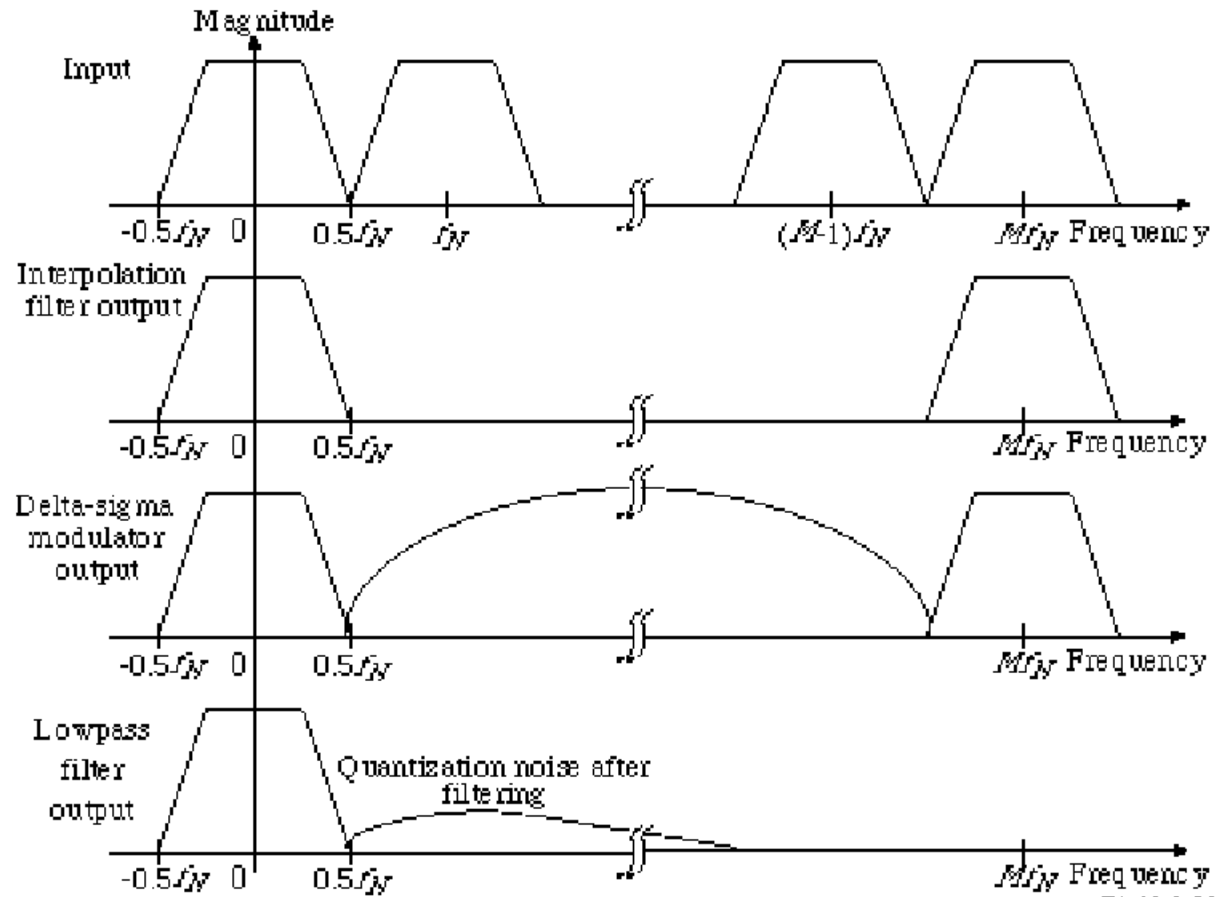


Fig10.9-34

It is necessary to follow the switched-capacitor filter by a continuous time lowpass filter to provide the necessary attenuation of the quantization noise.

FREQUENCY VIEWPOINT OF THE DS DAC

Frequency spectra at different points of the delta-sigma ADC:



COMPARISION OF THE DS ADC AND DS DAC

Both the $\Delta\Sigma$ ADC and $\Delta\Sigma$ DAC have many of the same properties

- Loops with identical topologies have the same stability conditions
- Loops with identical topologies have the same amount of quantization noise for a given oversampling ratio
- Higher order loops give better noise shaping and more dynamic range
- Multiple bit DACs are also used in $\Delta\Sigma$ DACs as well as $\Delta\Sigma$ ADCs