Improving Synchronization Stability of VSC via Novel Anti-windup Augmented Phase-Locked Loop

Zhenke Zhang, Yuanlong Li, Fei Gao.

***Abstract*—It is challenging to guarantee the synchronization stability of grid-following VSC during severe ac-grid faults, due to the vulnerability of the commonly used synchronous reference frame phase-locked loop (SRF-PLL) to grid voltage variation. Previous researches usually sacrifice the computation cost and latency for stability gains, as seen in methods like DDSRF-PLL. Attempts have also been made to introduce artificial limiter and anti-windup mechanism to the SRF-PLL, but their effectiveness in improving stability has not yet been confirmed. In this paper, we propose a performance-activated anti-windup augmented PLL in order to enlarge the long-term grid fault tolerance of grid-following VSC, hence improving the system synchronization stability. The phase difference between PCC and grid is taken as the performance indicator, and is injected to the input of the artificial limiter to control the activation time of the anti-windup compensator. An iterative optimization algorithm is developed to determine the parameters of the anti-windup compensator. Simulation results proved the effectiveness of the proposed PLL configuration.**

***Index Terms*—Synchronization stability, long-term large disturbance, voltage-source converter (VSC), phase-locked loop (PLL), anti-windup, performance activation**

I. Introduction

DURING the past few decades, an energy revolution has been gradually emerging all around the world. Renewable energy sources (RES) including photovoltaic power, wind power, hydropower, etc., have experienced a rapid development, prompting the advancement of power electronic grid interfaces like voltage-source converter (VSC) [1], [2].

Depending on the adopted control strategy, VSC can be divided into two categories: grid-following and grid-forming, with the former being the current mainstream [3]. Typically, grid-following VSC depends on phase-locked loop (PLL) to keep synchronization with grid. When grid short-circuit faults occurs, the point of common coupling voltage would drop to a lower value [4], causing the short circuit ratio at PCC to decrease, thereby weakening the connection between the RES and grid [5], [6]. As a consequence, the synchronization stability issue would arise when grid faults occur [7], [8].

Most of the previous researches focus on transient stability, as grid faults are assumed to be removed within a short time by the relay protection devices. However, the fault clearance takes time, typically ranging from several hundred ms to several seconds, not to mention the possibility of relay protection failure. Thereby, the long-term fault voltage dip tolerance (FVDT) should be a critical stability index of the VSC. Notice that the PCC voltage is the input of PLL, while the PLL dynamics determines the currents injected to the grid from the grid-following VSC, which will affect the PCC voltage in turn [9]. Therefore, adjusting the current injected to ac-grid and modifying the PLL configuration are two feasible approaches to enhance the synchronization stability of VSC.

The first approach, known as current injection strategy, can provide enough line current to maintain the PCC voltage, hence diminishing the affect of fault voltage dip. An adaptive switching current injection strategy relying on grid impedance angle is introdeced in [7]. However, it is nearly impossible for the local control terminal to know the grid impedance angle, making the strategy impractical. Another strategy proposed in [10] uses the disparity between the PLL-detected frequency and the grid's nominal frequency to compensate the active current output of VSC, yet compromising the reactive current capability and requiring an additional STATCOM to supply extra reactive current, thereby reducing the system reliability and increasing the cost.

In terms of PLL configuration modifying, there are numerous possibilities. In [11], an adaptive PLL switching between SRF-PLL and first-order PLL is proposed, yet the switching threshold highly depends on the severity of the fault, and the steady-state error problem also arises when the first-order PLL is activated. In [12], an artificial limiter is inserted at the output of the PI controller in SRF-PLL, forming a constrained PLL (CPLL), while the "windup" problem caused by the limiter is not discussed, which would definitely degrade the system stability [13]–[15]. Another research force incorporated the artificial limiter and some obsolete anti-windup compensators into the SRF-PLL [16], finding that the limiter would damage the system transient stability, while the VSC with a back-calculation anti-windup augmented PLL, which is equivalent to a static anti-windup augmented PLL (SAWAPLL), shows the largest FVDT among all the other anti-windup augmented PLLs and the original SRF-PLL. Nevertheless, neither [16] nor [12] has considered the long-term FVDT.

In this paper, we apply the performance-activation mechanism for anti-windup compensators proposed in [17] to the SAWAPLL, to improve the long-term FVDT of the grid-following VSC. The rest of the paper is organized as follows. In section II, the model of SRF-PLL is established, the impact of grid voltage fault on the synchronization stability of the grid-following VSC is analyzed, and the long-term FVDT of CPLL and SAWAPLL is tested via simulation. In section III, the model of performance-activated anti-windup augmented PLL (PAAWAPLL) is established, and an anti-windup syn-

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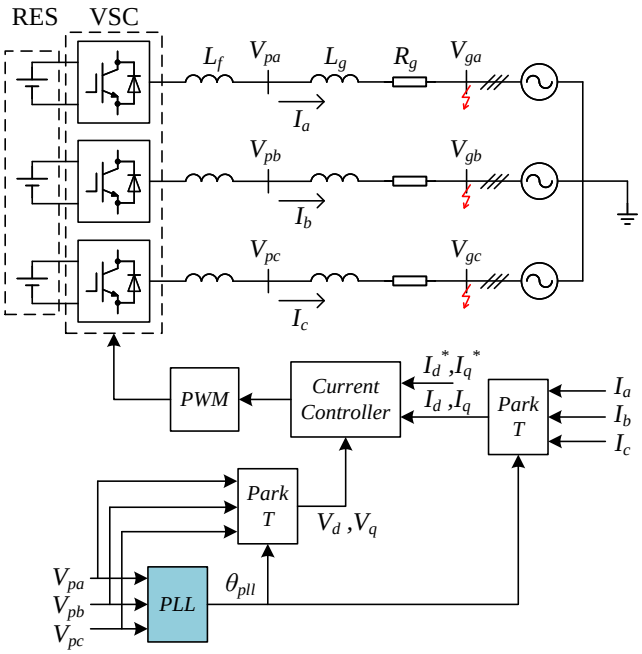

Fig. 1: Configuration of a simplified grid-following VSC system

thesis algorithm is developed. In section IV, the effectiveness of the proposed PLL in improving synchronization stability of grid-following VSC is evaluated by simulation in two different scenarios. Finally, conclusions are drawn in section V.

Notation. For a square matrix A, $\mathrm{He}(A) = A + A^T$. For any two integers $j_1 < j_2$, $I[j_1, j_2] := \{j_1, j_1 + 1, \ldots, j_2\}$.

II. Impact of Grid Faults on Synchronization Stability

A. System Configuration

Fig. 1 presents the configuration of a simplified grid-connected RES-VSC system, in which the transformers are omitted. The circuit parameters are presumed to be balanced in three phases. The PCC voltages V_p can be modelled by the grid voltage V_{gx}, line current I_x, and impedance $R_g + \omega_p L_g$ in the following phasor form,

$$\boldsymbol{V}_{px} = \boldsymbol{V}_{gx} + R_g \boldsymbol{I}_x + j\omega_p L_g \boldsymbol{I}_x, \tag{1}$$

where $x \in \{A, B, C\}$ denotes the phase, and ω_p denotes the grid angular frequency. Applying Park's transformation to (1), we get the synchronous reference frame form,

$$\begin{cases} V_{pd} = V_g \cos\left(\theta_g - \theta_p\right) + R_g I_d - \omega_p L_g I_q \\ V_{pq} = V_g \sin\left(\theta_g - \theta_p\right) + R_g I_q + \omega_p L_g I_d \end{cases} \tag{2}$$

Usually, the bandwidth of the current controller is much greater than that of the PLL, with the former being greater than $100Hz$ [18] while the latter being about $10Hz$ [19]. This allows us to disregrad the transient behavior of currents when studying the synchronization stability of the system. Besides, θ_p, ω_p should be replaced by the output of PLL $\theta_{pll}, \omega_{pll}$, and since θ_g is not accessible, we substitute it with $\theta_{gn} = \int_t \omega_{gn} \mathrm{d}t$ without loss of generality. Define $\delta = \theta_{gn} - \theta_{pll}$ as the phase difference. Then we have the following circuit model in synchronous reference frame,

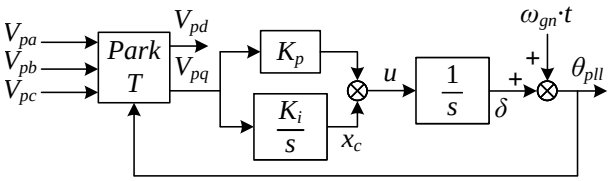

Fig. 2: Diagram of SRF-PLL

$$\begin{cases} V_{pd} = V_g \cos\delta + R_g I_d^* - \omega_{pll} L_g I_q^*, \\ V_{pq} = -V_g \sin\delta + R_g I_q^* + \omega_{pll} L_g I_d^*, \end{cases} \tag{3}$$

where I_d^* and I_q^* are current references.

Fig. 2 shows the configuration of the original SRF-PLL. Denote δ_{ss} as the steady-state value of δ. From (3), we have

$$\delta_{ss} = \mathrm{asin}\left(\frac{R_g I_q^* + \omega_{gn} L_g I_d^*}{V_g}\right). \tag{4}$$

Denote u as the PI controller output in PLL. Let $x_p = \delta - \delta_{ss}$ and $x_c = \int_t K_i V_{pq}$. Then the model of SRF-PLL is shown as follows

$$\begin{cases} \dot{x}_p = u, \\ \dot{x}_c = K_i \left(-V_g \sin\left(x_p + \delta_{ss}\right) + R_g I_q^* + \omega_{pll} L_g I_d^*\right), \\ u = x_c + K_p \left(-V_g \sin\left(x_p + \delta_{ss}\right) + R_g I_q^* + \omega_{pll} L_g I_d^*\right), \\ \omega_{pll} = u + \omega_{gn}. \end{cases} \tag{5}$$

Since the PLL model is nonlinear, we design the PI parameters of PLL based on the linearized model. In [20], the small signal model of SRF-PLL is discussed, with damping ratio ζ and settling time t_s being

$$\zeta = \frac{K_p}{2}\sqrt{\frac{V_g}{2K_i}}, \tag{6}$$

$$t_s = \frac{18.4}{K_p V_s}. \tag{7}$$

The PI parameters of PLL can be determined by specifying the performance indices ζ and t_s. Both simulation and experiments in [21] demonstrated the effectiveness of the design method.

B. Impact of Grid Fault

The equilibium points of SRF-PLL exist if and only if δ_{ss} exists. Moreover, from (4) we know that δ_{ss} exists if and only if the following condition holds,

$$V_g \geqslant R_g I_q^* + \omega_{gn} L_g I_d^*. \tag{8}$$

To guarantee the stability of SRF-PLL, its linearized model should be considered. The linearized model of SRF-PLL is given as follows,

$$\bar{\Sigma}_0 \begin{cases} \dot{\bar{x}} = A_0 \bar{x} + B_{0q} q, \\ u = C_0 \bar{x} + D_{0q} q, \end{cases} \tag{9}$$

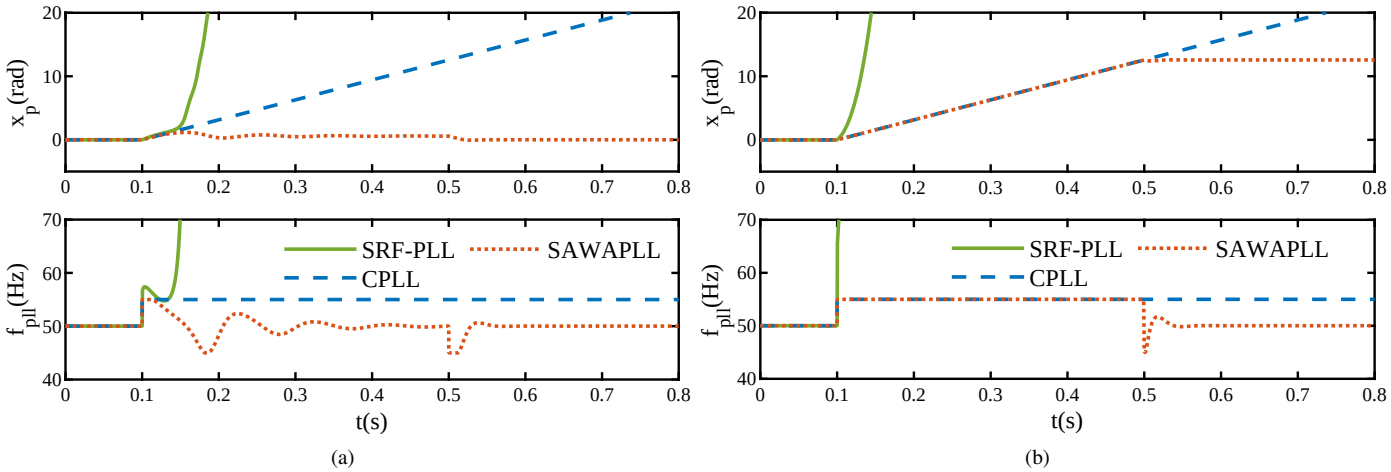

Fig. 3: Simulation result of VSCs with SRF-PLL, CPLL, and SAWAPLL, in the HV scenario. The fault voltage dip magnitude is $-66\sqrt{2}kV$ in (a) and $-70\sqrt{2}kV$ in (b).

where $\bar{x} = [\bar{x}_p, \bar{x}_c]^T$ is the state of the linearized model, and

$$A_0 = \begin{bmatrix} -\dfrac{K_p V_g \cos\delta_{ss}}{C_1} & \dfrac{1}{C_1} \\ -\dfrac{K_i V_g \cos\delta_{ss}}{C_1} & \dfrac{K_i L_g I_d^*}{C_1} \end{bmatrix}, \quad B_{0q} = \begin{bmatrix} -\dfrac{1}{C_1} \\ -\dfrac{K_i L_g I_d^*}{C_1} \end{bmatrix},$$
$$C_0 = \begin{bmatrix} -\dfrac{K_p V_g \cos\delta_{ss}}{C_1} & \dfrac{1}{C_1} \end{bmatrix}, \quad D_{0q} = -\dfrac{1 - C_1}{C_1}.$$

By analyzing the eigenvalues of A_0, we obtain the following stablility conditions for SRF-PLL

$$V_g^2 > \left(R_s I_q^* + \omega_{gn} L_g I_d^*\right)^2 + \left(\frac{42.32 L_g I_d^*}{18.4\zeta^2 t_s}\right)^2, \tag{10}$$
$$V_g > \frac{18.4 L_g}{t_s}. \tag{11}$$

From (8), (10) and (11), it can be inferred that, with all other conditions being equal, higher V_g means stronger system stability. The grid fault voltage dip directly reduces V_g, thereby harming the system stability.

C. The limitation of the existing anti-windup augmented PLL

The conclusion that a VSC with a CPLL has stronger stability than one with an SRF-PLL stated in [12] is not well-supported, as the authors only provided some numerical results to support it. According to existing solid researches on actuator saturation, the artificial limiter added in CPLL would definitely cause the "windup" phenomenon, therefore degrading the stability of the VSC. Moreover, [12] and [16] only takes short-time grid faults into consideration, with the fault duration being tens to several hundreds of milliseconds. However, most grid faults cannot be resolved within such a short period, sometimes it even takes several hours to repair the affected area of the grid. Therefore, the system stability under long-term grid faults should be studied. For grid faults which cause voltage dips, the long-term FVDT, which is the maximum tolerable voltage dip of the specific power system, should be used as the stability index of the VSC.

We obtain the long-term FVDT of VSCs with SRF-PLL, CPLL, and SAWAPLL, respectively, via simulation in two scenarios given in Table II. By increasing the fault voltage dip magnitude ΔV_g from $0V$ to the value when the fault-time PLL

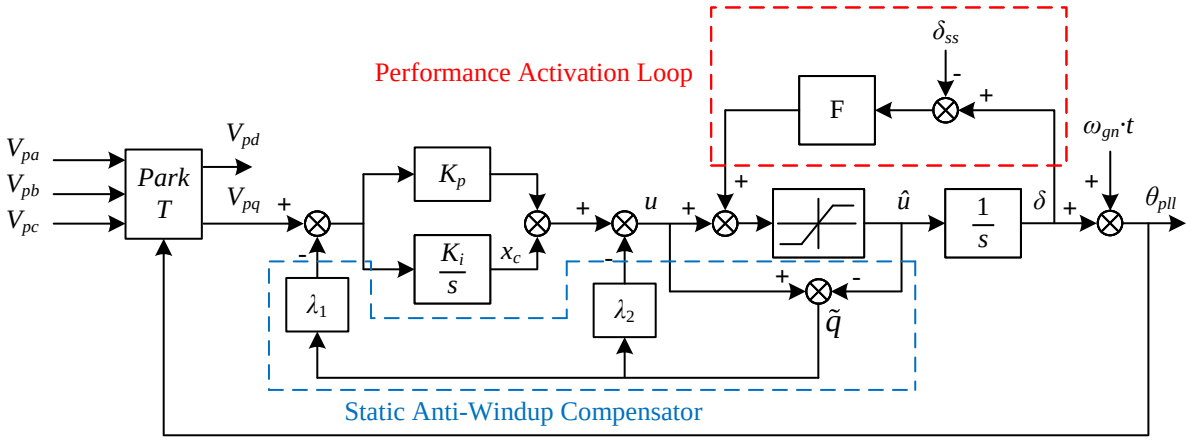

Fig. 4: Diagram of the performance-activated anti-windup augmented PLL

response diverges, we can obtain the FVDT of the VSCs with different PLLs in a specific scenario. The simulation result is shown in Table I. Fig. 3 presents an example in the HV scenario. The symbol f_{pll} denotes the grid frequency estimated by the PLL, which is defined as follows

$$f_{pll} = \begin{cases} \dfrac{(u+\omega_{gn})}{(2\pi)}, & \text{no artificial limiter,} \\ \dfrac{(\hat{u}+\omega_{gn})}{(2\pi)}, & \text{otherwise.} \end{cases}$$

TABLE I: Long-term FVDT of VSCs with SRF-PLL, CPLL, and SAWAPLL

Scenario	SRF-PLL	CPLL	SAWAPLL
HV	$-63.8\sqrt{2}kV$	$-62.5\sqrt{2}kV$	$-66.4\sqrt{2}kV$
LV	$-38.9\sqrt{2}V$	$-37.6\sqrt{2}V$	$-41.5\sqrt{2}V$

It can be inferred from Table I that, the artificial limiter added in CPLL actually hurts the synchronization stability of the VSC, which is attributed to the "windup" phenomenon caused by the limiter. The SAWAPLL performs slightly better than the SRF-PLL in long-term FVDT, with a gain of only around 6 percents. Besides, according to (8), (10) and (11), the supremum of the long-term FVDT of a VSC with a SRF-PLL is $71.762\sqrt{2}kV$ and $44.446\sqrt{2}V$ in the HV and LV scenarios, respectively. These data indicate that the stability improvement achieved by the static anti-windup compensator is quite limited and falls short of expectations, especially considering the additional computational cost it incurs.

III. Performance-Activated Anti-Windup Augmented PLL

A. Modeling

Inspired by [12], [16], based on the work in [17], we propose a novel performance-activated anti-windup augmented PLL (PAAWAPLL) which is illustrated in Fig. 4. Compared with the SAWAPLL, our PAAWAPLL incorporates the error between δ_{ss} and δ to the input of the limiter. Since δ is a signal that can characterize the performance of the PLL, the imported feedback loop allows the system performance to control the activation timing of the anti-windup compensator. Therefore, by designing an appropriate feedback gain matrix F, both transient performance and stability can be enhanced

Denote by $\Lambda = [\lambda_1, \lambda_2]^T$ the anti-windup parameters and F the performance-activation gain matrix. Let

$$\hat{u} = \text{sat}(u) = \text{sgn}(u)\min\{|u|, \beta\},$$
$$q = \text{dz}(u) = u - \text{sat}(u),$$

where β is the saturation limit. The performance-activated anti-windup augmented PLL is expressed as follows

$$\begin{cases} \dot{x} = \left(\left(A_p\Lambda + A_c\right)FI_1 + A_cI_2\right)x - \left(A_p\Lambda + A_c\right)q + d, \\ u = \left(\left(C_p\Lambda + C_c - 1\right)FI_1 + C_cI_2\right)x \\ \quad - \left(C_p\Lambda + C_c - 1\right)q + I_1 d, \end{cases} \tag{12}$$

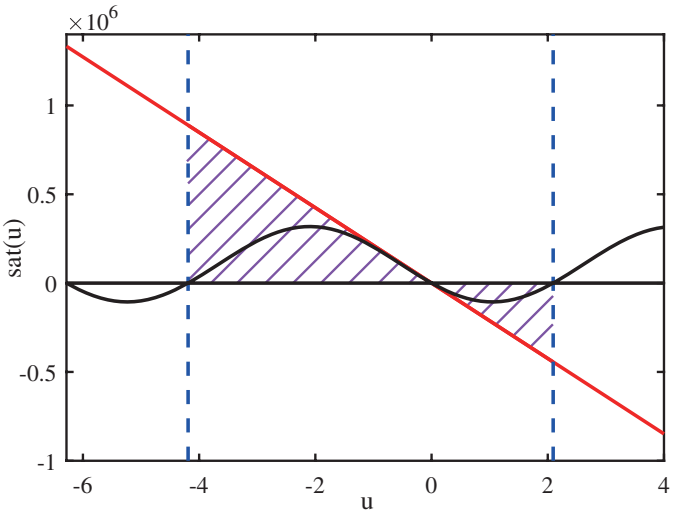

Fig. 5: Diagram of regional convex hull

where

$$A_p = \begin{bmatrix} \dfrac{K_p}{C_1} & \dfrac{1}{C_1} \\ \dfrac{K_i}{C_1} & \dfrac{K_iL_gI_d^*}{C_1} \end{bmatrix},\ A_c = \begin{bmatrix} \dfrac{1}{C_1} \\ \dfrac{K_iL_gI_d^*}{C_1} \end{bmatrix},$$
$$C_p = I_1A_p,\ C_c = I_1A_c,\ I_1 = \begin{bmatrix} 1 & 0 \end{bmatrix},\ I_2 = \begin{bmatrix} 0 & 1 \end{bmatrix},$$
$$d = \begin{bmatrix} \dfrac{K_p}{C_1} \\ \dfrac{K_i}{C_1} \end{bmatrix}\left(R_gI_q^* + L_gI_d^*\omega_{gn} - V_g\sin\left(x_p + \delta_{ss}\right)\right).$$

Since the sine terms are bounded, d can be viewed as an origin-passing perturbation.

Because of the existence of the algebraic loop

$$u + \left(C_{p1} - 1\right)\left(u - sat(u)\right) = \left(\left(C_{p1} - 1\right)FI_1 + C_cI_2\right)x \tag{13}$$

in (12), the well-posedness, i.e., the existence and uniqueness of the solution u, must be guaranteed. One sufficient well-posedness condition of the algebraic loop (13) is that there exists a diagonal matrix $W > 0$ satisfying

$$-\text{He}\left(C_{p1}^TW\right) - 2W < 0. \tag{14}$$

B. Anti-Windup Synthesis

The aim of anti-windup synthesis is to develop a compensator that reduces the impact of saturation on performance and stability. This requires formulating an optimization problem that maximizes the system R_A while ensuring that the stability criteria are met.

Anti-windup synthesis for general nonlinear systems with saturation remains a challenging and unresolved issue, with only a few methods available for some specific nonlinear systems [22]–[24]. Since the stability of a nonlinear system's equilibrium point can be determined by the stability of its linearized counterpart [25], we apply the anti-windup synthesis result of the linearized system to the original nonlinear system (12).

Given a system $\dot{x} = f(x), x \in \mathbb{R}^n$ and an initial condition $x(0) = x_0$, we define the state trajectory as $\phi(t, x_0)$. Suppose the origin is an equilibrium point of the system, and then its R_A can be defined as

$$R_A := \{x_0 \in \mathbb{R}^n : \lim_{t \to +\infty} \phi(t, x_0) = 0\}.$$

In general, it is not feasible to determine the exact R_A of a linear system with saturation feedback. Nevertheless, for a planar system with a single input, its boundary of R_A corresponds to its unique convex limit cycle [26]–[28]. This characteristic allows us to approximate R_A using certain tractable sets.

The invariant set is a logical choice for approximating R_A. It is defined as a set that all state trajectories originating within it stay within it. Moreover, if these trajectories tend to converge towards an equilibrium point within the set, it is considered a contractively invariant set, which makes it a valid estimate of R_A.

Ellipsoidal invariant sets has been widely used as the level sets of Lyapunov functions in estimating R_A for high-order systems and nonlinear systems, due to its simplicity [27], [29], [30]. Define a quadratic Lyapunov function as $V(x) = x^T P x$, where $P \in \mathbb{R}^{n \times n}$ is positive-definite. For a given positive number ρ, the ellipsoidal level set is defined as $\mathcal{E}(P, \rho) = \{x \in \mathbb{R}^n : x^T P x \leqslant \rho\}$. Then, Definition 1 provides the criteria under which $\mathcal{E}(P, \rho)$ qualifies as a contractively invariant set of the system.

Definition 1: $\mathcal{E}(P, \rho)$ is a contractively invariant set of the system $\dot{x} = f(x)$, if

$$\dot{V}(x) = 2x^T P f(x) < 0,$$

holds for any $x \in \mathcal{E}(P, \rho) \setminus \{0\}$.

Let $A_{p1} = A_p \Lambda + A_c$, then the following contractive invariance condition for $\mathcal{E}(P, \rho)$ can be obtained from Definition 1.

$$\dot{V} = 2x^T P \left(A_{p1} F I_1 + A_c I_2\right) x + 2x^T P \left(-A_{p1} q + d\right) < 0. \quad (15)$$

Besides, the following condition needs to be satisfied to ensure that there exists ρ for $\mathcal{E}(P, \rho)$ to be contractively invariant.

$$\mathrm{He}\left(P A_{p1} F I_1 + P A_c I_2\right) < 0. \quad (16)$$

Because of the existence of nonlinearities q and d, (15) cannot be solved directly. These nonlinearities must be eliminated from the inequalities to make them feasible. First, we deal with d. Note that d is periodic and origin-crossing. Thus we can use the following regional convex hull to handle it,

$$d \in \mathrm{co}\{0, Lx\}, \ \forall x \in D_x, \quad (17)$$

where

$$L = \begin{bmatrix} -\dfrac{K_p V_g}{C_1} & 0 \\ -\dfrac{K_i V_g}{C_1} & 0 \end{bmatrix},$$

$$D_x = \{x : I_1 x \in [-\pi - 2\delta_{ss}, \pi - 2\delta_{ss}]\}.$$

The geometric imterpretation of the regional convex hull is depicted in Fig. 5.

Then we obtain the following differential inclusion

$$\begin{aligned} \dot{x} &\in \mathcal{F}(x, q, \eta) \\ &= \mathrm{co}\left\{ \begin{matrix} \left(A_{p1} F I_1 + A_c I_2\right) x - A_{p1} q, \\ \left(A_{p1} F I_1 + A_c I_2 + L\right) x - A_{p1} q \end{matrix} \right\}. \end{aligned} \quad (18)$$

Thus, for any $x \in \mathcal{E}(P, \rho) \subseteq D_x$, there exists a scalar $\eta \in [0, 1]$, such that

$$\dot{x} = \left(A_{p1} F I_1 + A_c I_2 + \eta L\right) x - A_{p1} q, \quad (19)$$

and (15) can be reevaluated as

$$\dot{V} = 2x^T P \left(A_{p1} F I_1 + A_c I_2 + \eta L\right) x - 2x^T P A_{p1} q < 0. \quad (20)$$

An obvious sufficient condition for (20) to hold is shown below

$$\dot{V}_1 = 2x^T P \left(A_{p1} F I_1 + A_c I_2\right) x - 2x^T P A_{p1} q < 0, \quad (21)$$

$$\dot{V}_2 = 2x^T P \left(A_{p1} F I_1 + A_c I_2 + L\right) x - 2x^T P A_{p1} q < 0. \quad (22)$$

Now that the disturbance d has been handled, the next step is to addresss the deadzone q.

Regional sector condition is the traditional way of dealing with saturation or deadzone nonlinearities [15], [28]. Suppose that the input of saturation is $u \in \mathbb{R}^m$, given a matrix $H \in \mathbb{R}^{m \times n}$, define

$$\mathcal{L}(H) = \{x \in \mathbb{R}^n : |Hx|_\infty \leqslant \beta\}.$$

$\mathcal{L}(H)$ is the linear zone of $\mathrm{sat}(Hx)$. Then, lemma 1 gives a definition of the regional sector condition.

Lemma 1: For any $x \in \mathcal{L}(H)$ and diagonal matrix $W \in \mathbb{R}^{n \times n}$ which is positive-definite, the following two equivalent inequalities hold

$$\begin{aligned} (u - \mathrm{sat}(u))^T W (\mathrm{sat}(u) + Hx) &\geqslant 0, \\ q^T W (u - q + Hx) &\geqslant 0. \end{aligned}$$

By adding the regional sector condion to the contractive invariance condition of $\mathcal{E}(P, \rho)$, an linear quadratic inequality can be formed, where x and q are the free variables, therefore the deadzone q is eliminated in the solving procedure.

The regional sector condition of the corresponding system of (21) is

$$q^T W \left(\left(C_{p1} F I_1 + C_c I_2 + H\right) x - C_{p1} q\right) \geqslant 0, \forall x \in \mathcal{L}(H). \quad (23)$$

Then, add (23) to (21) so that we get the following sufficient condition for (21) to hold

$$\dot{V}_1 \leqslant \dot{V}_1 + 2q^T W \left(C_{p1} F I_1 + C_c I_2 + H\right) x - 2q^T W C_{p1} q < 0, \quad (24)$$

which is equivalent to

$$\mathrm{He}\begin{bmatrix} P A_{cl} & -P(A_p \Lambda + A_c) \\ W\left(I_1 A_{cl} + H\right) & -W\left(C_p \Lambda + C_c\right) \end{bmatrix} < 0, \quad (25)$$

where $A_{cl} = A_{p1} F I_1 + A_c I_2$. The deadzone q becomes a free variable and thus is eliminated in the matrix inequality (25).

In the same way, the sufficient condition for (22) to hold can obtained as follows

$$\mathrm{He}\begin{bmatrix} P\left(A_{cl} + L\right) & -P(A_p \Lambda + A_c) \\ W\left(I_1 A_{cl} + I_1 L + H\right) & -W\left(C_p \Lambda + C_c\right) \end{bmatrix} < 0. \quad (26)$$

TABLE II: Circuit and controller parameters in simulation

Symbol	Description	HV Scenario	LV Scenario
V_g	Magnitude of the grid voltage	$150\sqrt{2}kV$	$100\sqrt{2}V$
ω_{gn}	Nominal grid angular frequency	100π	100π
I_d^*	Magnitude of d-axis current reference of VSC	$1kA$	$20A$
I_q^*	Magnitude of q-axis current reference of VSC	$0A$	$0A$
R_f	Resistance of the VSC output low-pass filter	0Ω	0Ω
L_f	Inductance of the VSC output low-pass filter	$15mH$	$1.5mH$
R_g	Grid resistance	106Ω	3.75Ω
L_g	Grid inductance	$338mH$	$12mH$
ζ	Damping ratio in PLL parameter design	0.5	0.5
t_s	Settling time in PLL parameter design	$0.1s$	$0.1s$
β	Saturation limit	10π	10π
Λ	Anti-windup parameters	$\left[517.14, -1.3917\right]^T$	$\left[5.9289, -7.7758\right]^T$
F	Performance-activation gain	-348.11	-208.55

Additionally, to ensure that the regional sector condition holds for any $x \in \mathcal{E}(P,\rho)$, the following condition should hold, which is,

$$\mathcal{E}(P,\rho) \subseteq \mathcal{L}(H) \Longleftrightarrow \begin{bmatrix} P & H^T \\ H & \beta^2/\rho \end{bmatrix} \geqslant 0. \tag{27}$$

The combination of (25), (26) and (27) yields a sufficient condition for $\mathcal{E}(P,\rho)$ to be a contractively invariant set of the system (12).

Both (16) and (14) are already incorporated in (25) and (26).

For optimization objective, we simply choose $-\rho$ as the objective function, since ρ directly represents the size of $\mathcal{E}(P,\rho)$.

Finally, an optimization problem maximizing the size of the contractively invariant set $\mathcal{E}(P,\rho)$ is formulated below

$$\begin{aligned} \min_{\rho>0,P>0,W>0,F,\Lambda,H} \quad & -\rho \\ \text{s.t.} \quad & \text{inequalities (25), (26), (27).} \end{aligned} \tag{28}$$

However, the optimization problem (28) is not convex, as non-convex terms like ΛF appears in the constraints. To eliminate the non-convex terms in (28), some nonlinear transformation needs to be performed [15]. Let $Q = P^{-1}, U = W^{-1}, Y = HQ$, then the following optimization problem can be obtained

$$\begin{aligned} \min_{\rho>0,Q>0,F,U>0,\Lambda,Y} \quad & -\rho \\ \text{s.t.} \quad & \text{He}\begin{bmatrix} A_{cl}Q & -(A_p\Lambda + A_c)U \\ (I_1A_{cl}+H)\,Q & -\left(C_p\Lambda + C_c\right)U \end{bmatrix} < 0, \\ & \text{He}\begin{bmatrix} (A_{cl}+L)\,Q & -(A_p\Lambda + A_c)U \\ (I_1A_{cl}+I_1L+H)\,Q & -\left(C_p\Lambda + C_c\right)U \end{bmatrix} < 0, \\ & \begin{bmatrix} Q & Y^T \\ Y & \beta^2/\rho \end{bmatrix} \geqslant 0. \end{aligned} \tag{29}$$

Then the following iterative algorithm can be developed.

Algorithm 1

Step 1: Fix $F = 0$, let $Z = \Lambda U$, solve the optimization prpblem (28) to obtain $\Lambda = ZU^{-1}$

Step 2: Choose an initial value F_1 for F, threshold α and the maximum iteration number k_m. Let $k = 1$.

Step 3: Fix Λ, F_k, solve the optimization problem (28). Denote by $\left(\tilde{\rho}, \tilde{Q}, \tilde{U}, \tilde{Y}\right)$ the solution. Let $\rho_k = \tilde{\rho}$, update Q with $\tilde{Q}$.

Step 4: If $k \geq 2$ and $|\rho_k - \rho_{k-1}| < \alpha$, then stop, and take Λ, F_k as outputs; else, if $k = k_m$, then stop, and select the minimum ρ_t among all ρ_k, and take Λ, F_t as outputs; else, let $k = k + 1$, go to step 5.

Step 5: Fix Λ, Q, solve the optimizatioon problem (28). Denote by $\left(\tilde{\rho}, \tilde{F}, \tilde{U}, \tilde{Y}\right)$ the solution. Let $F_k = \tilde{F}$. Go back to step 3.

IV. Validation

To illustrate the effectiveness of the PAAWAPLL in improving the synchronization stability of RES-VSC, we carry out simulations in two different scenarios, one is the low-voltage (LV) scenario, and the other is the high-voltage (HV) scenario. The circuit and controller parameters of the two scenarios are listed in Table II. In each scenario, we test the responses of VSCs with SRF-PLL, CPLL, SAWAPLL, and PAAWAPLL, respectively, under several fault conditions, for obtaining the long-term FVDT of them. The system is said to be able to tolerate a specific fault voltage dip if the fault-time x_p always falls in the range $(-\pi - 2\delta_{ss}, \pi - 2\delta_{ss})$ and converges to 0 once the fault is resolved.

TABLE III: long-term FVDT of VSCs with SRF-PLL, CPLL, SAWAPLL and PAAWAPLL

Scenario	SRF-PLL	CPLL	SAWAPLL	PAAWAPLL
HV	$-63.8\sqrt{2}kV$	$-62.5\sqrt{2}kV$	$-66.4\sqrt{2}kV$	$-149.9\sqrt{2}kV$
LV	$-38.9\sqrt{2}V$	$-37.6\sqrt{2}V$	$-41.5\sqrt{2}V$	$-99.9\sqrt{2}V$

The long-term FVDT of VSCs with the four PLLs is shown in Table III, from which it can be infered that the PAAWAPLL dramatically improves the long-term FVDT of the grid-following VSC. Figs. 6 and 7 present some simulation results in the HV and LV scenarios, respectively.

The simulation outcome is a sufficient and compelling evidence to demonstrate the efffectiveness of the proposed PLL configuration.

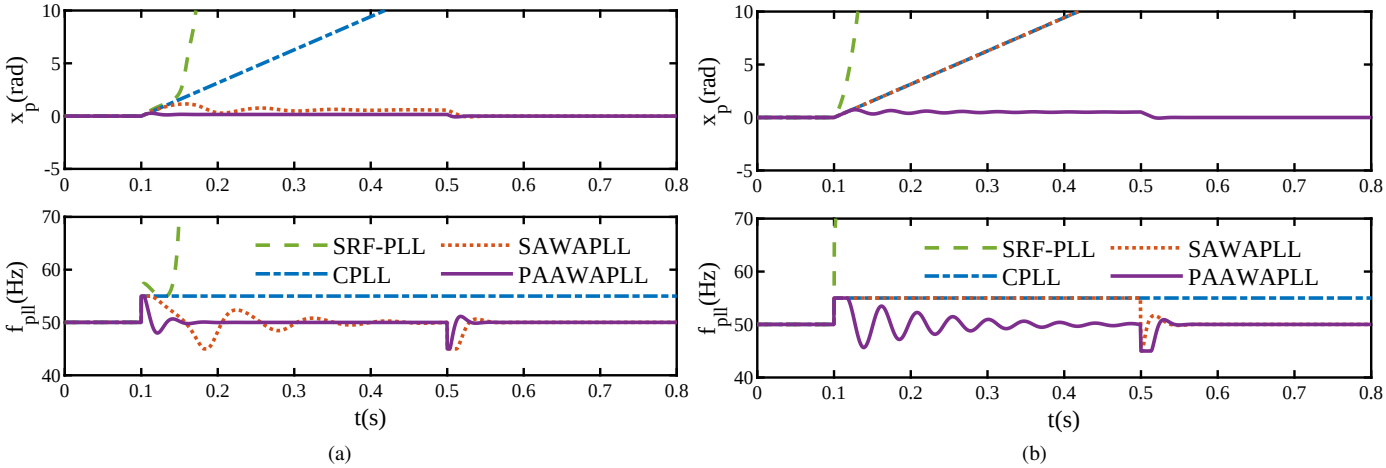

Fig. 6: Simulation result of VSCs with SRF-PLL, CPLL, SAWAPLL, and PAAWAPLL, in the HV scenario. The fault voltage dip magnitude is $-66\sqrt{2}kV$ in (a) and $-149\sqrt{2}kV$ in (b).

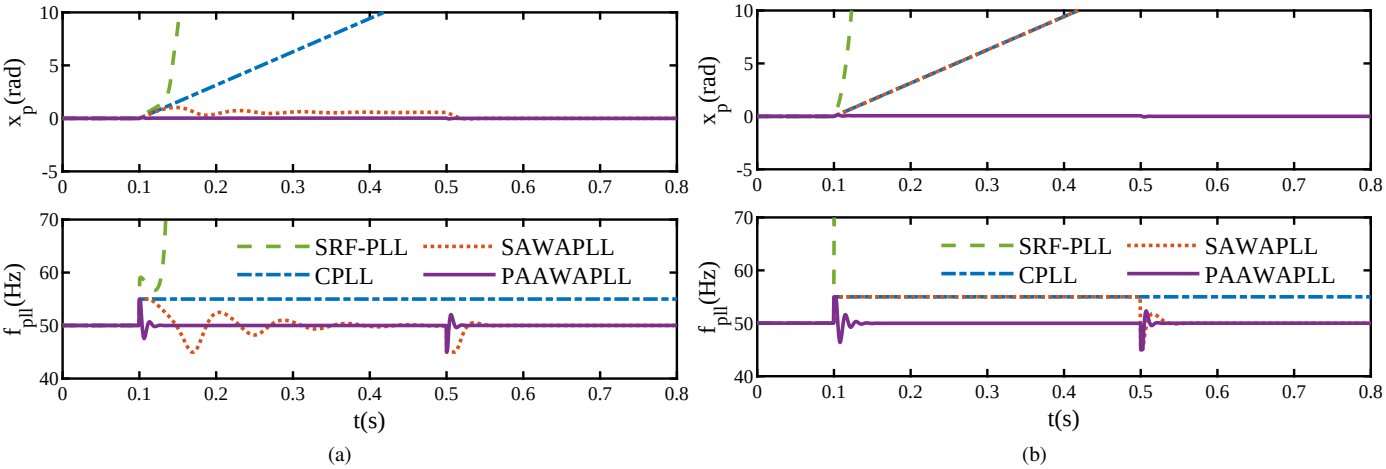

Fig. 7: Simulation result of VSCs with SRF-PLL, CPLL, SAWAPLL, and PAAWAPLL, in the LV scenario. The fault voltage dip magnitude is $-41\sqrt{2}V$ in (a) and $-99\sqrt{2}V$ in (b).

V. Conclusion

In this paper, a novel PLL configuration with performance-activated anti-windup compensation is proposed for improving the synchronization stability of grid-following VSC under severe grid faults. Detailed PLL parameter determination and anti-windup synthesis methodology is elaborated. Simulation results show the significant synchronization stability enhancement achieved by the proposed PLL configuration in comparison with the original SRF-PLL and some other existing PLL configurations.

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