Chip Design Rubric	A	B	C	D/E/F
README.md (5%)	• Writing style is clear, effective, and succinct. There are no errors. • Well-structured with headers • The level of detail is tailored to the target audience • Well structured with headers • Figures are used appropriately, and are of high quality. They are labeled, captioned and referenced in-text. • Comprehensive coverage of the design	• Writing style is mostly clear, but not always succinct, with some minor errors • Good structure but some inconsistencies • The level of detail is mostly tailored to the target audience • Figures are mostly used appropriately, though not referenced in-text or lacking captions. • Covers most aspects of the design	• Writing is unclear or contains errors • Some structure but many inconsistencies • Misses key elements of the design • The level of detail is not tailored to the target audience • Figures do not support the details provided in-text	• Writing is unclear or contains errors • Lacks coherent structure • Inadequate coverage of design • Figures are irrelevant or non-existent
Chip Design & Technical Detail (5%)	• Chip design successfully completed with all actions passing at time of submission • Design is executed creatively and features optimized design choices • Technical choices are described with clear intuition behind the detail is provided • Deep insight into design • Justification for design choices	• Chip design successfully completed with all actions passing at time of submission • Technical choices are described but some depth missing • Some justification for design decisions, e.g., an attempt has been made, but may not be wholly accurate	• Chip design unsuccessful with one or more actions passing, though a reasonable attempt has been made based on design intent in report • Tests are incorrectly scoped • Covers basics without diving deep into design • Some overlooked aspects of the design • Few justifications for choices	• Chip design unsuccessful with one or more actions passing, and a reasonable attempt has not been made • Technical choices are not described • Design decisions are unmotivated • Many components not considered
Simulations and Tests (5%)	• Tests and simulations are appropriate at the time of report submission • Timing diagrams are present and clearly explained, supporting the design itself • Appropriate metrics are proposed to assess the project	• Tests are inappropriate for the intended use-case but an attempt has been made • Timing diagrams are present but not clearly explained • Appropriate metrics are proposed, but described vaguely	• Tests are incorrectly scoped, simulations do not characterize the chip • Timing diagrams do not support the report • Inappropriate metrics are proposed	• Tests and simulations are missing or do not work • Metrics are not proposed to assess the project.