

Data: S-parameters @ 2,4 GHz (followed  
 +5V @ 545 mA 25°C RF design  
 chris bowick)  
 $\text{dB/Ang}$   $20 \log(|S_{11}|) = S_m, \text{dB}$   
 $|S_m| = 10^{\frac{S_m, \text{dB}}{20}}$  p. 141

$S_{11}$	$S_{21}$	$S_{12}$	$S_{22}$
-1,909435 dB	19,91734 dB	-59,34703 dB	-1,790494 dB
$\angle 162,7281^\circ$	$\angle 79,60395^\circ$	$\angle 96,81291^\circ$	$\angle -178,5883^\circ$

$\sigma, 802659$	$\sigma, 90529$	$\sigma, 6019171$	$\sigma, 810418$
$\angle 162,7281^\circ$	$\angle 79,60395^\circ$	$\angle 96,81291^\circ$	$\angle -178,5883^\circ$

i) Calculate stability

$$DS = S_{11}S_{22} - S_{12}S_{21} = 0,675474 \angle -15,5177^\circ$$

$$|DS| = 0,675474$$

$$K = \frac{1 + |DS|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}| |S_{12}|}$$

$$= 3,74425 > 1 \Rightarrow \text{unconditional stability}$$

2) Calculate maximum achievable gain possible (MAG):

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |D_{sl}|^2 = 0, \text{ } 51818$$

$$\text{MAG} = 10 \log \left( \frac{|S_{21}|}{|D_{12}|} \right) + 10 \log \left( k - \sqrt{k^2 - 1} \right)$$

$B_1 > 0$

$$= 28,4678 \text{ dB}$$



Find load and source reflection coefficients that will provide a conjugate match:

1) load reflection:

$$C_2 = S_{22} - (D_s S_{11}^*) = 0,276275 \angle -79,26^\circ$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |D_{sl}|^2 = 0,56929$$

$$|\Gamma_L| = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2|C_2|} = 0,782286$$

$$\angle \Gamma_L = 179,26^\circ$$

optimal load impedance:

$$Z_L = 50 \frac{1 + \Gamma_L}{1 - \Gamma_L} = 6,11625 \angle 2,9792^\circ$$
$$\underbrace{6,10738 + 0,31788 j}_j$$

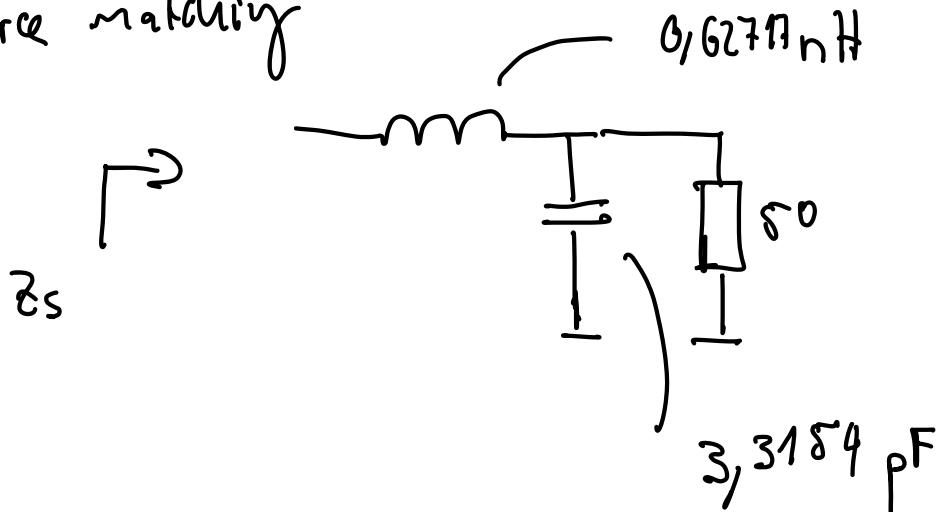
2) optimal source impedance

$$\Gamma_S = \left[ S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 + \Gamma_L S_{22}} \right]^*$$
$$= 0,762699 \angle -161,9703151^\circ$$

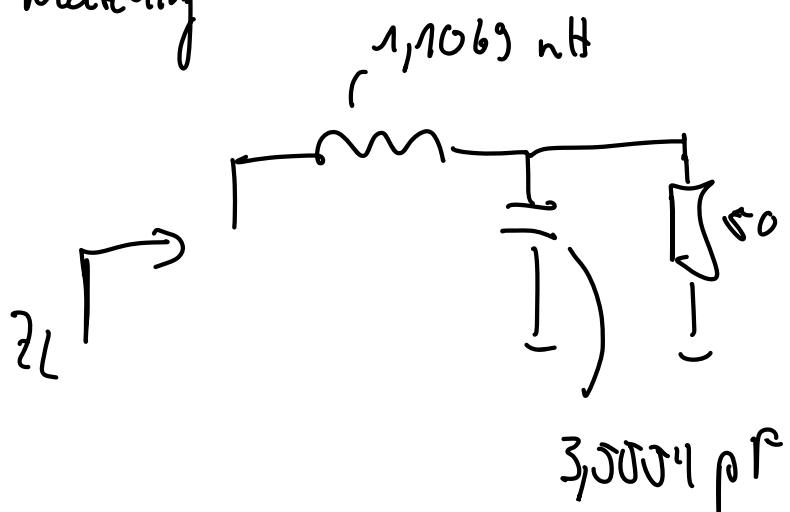
$$Z_S = 6,89762 - 3,78518 j$$
$$\sim$$

# Calculating impedance matching circuits

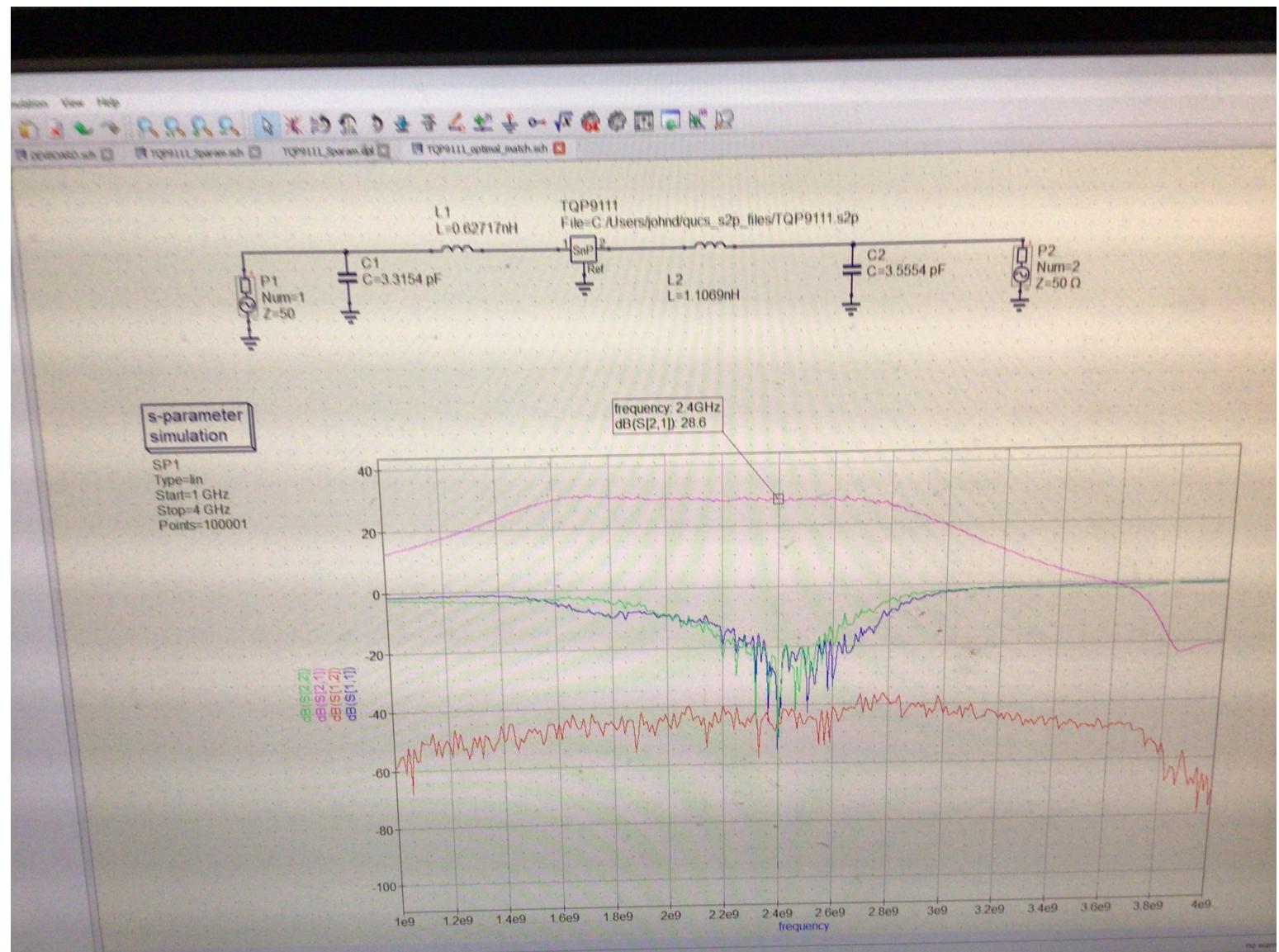
source matching



load matching



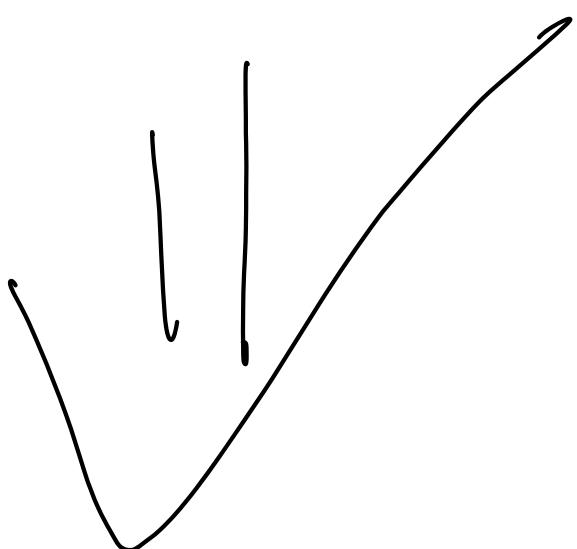
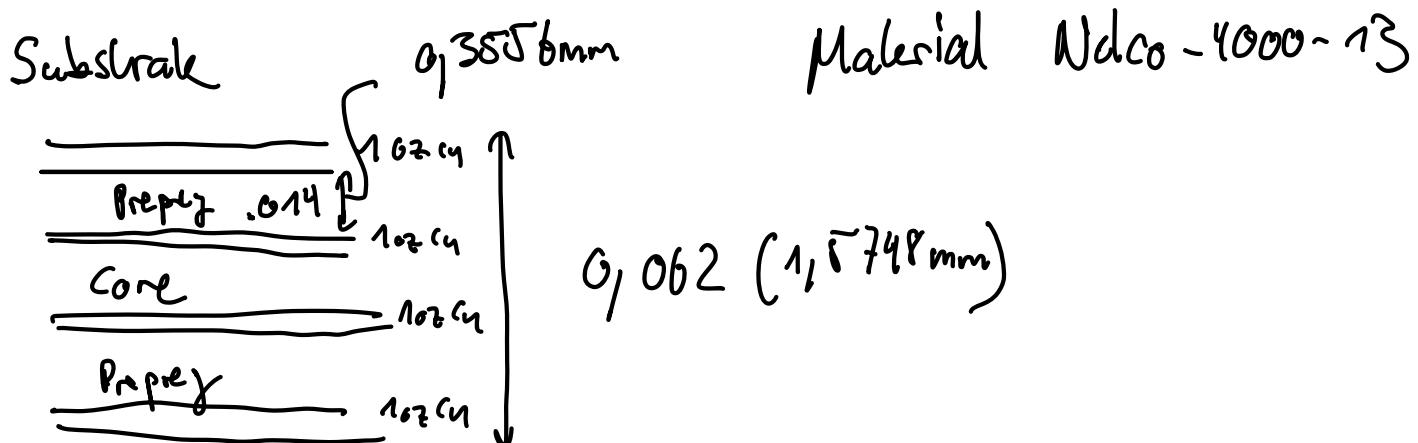
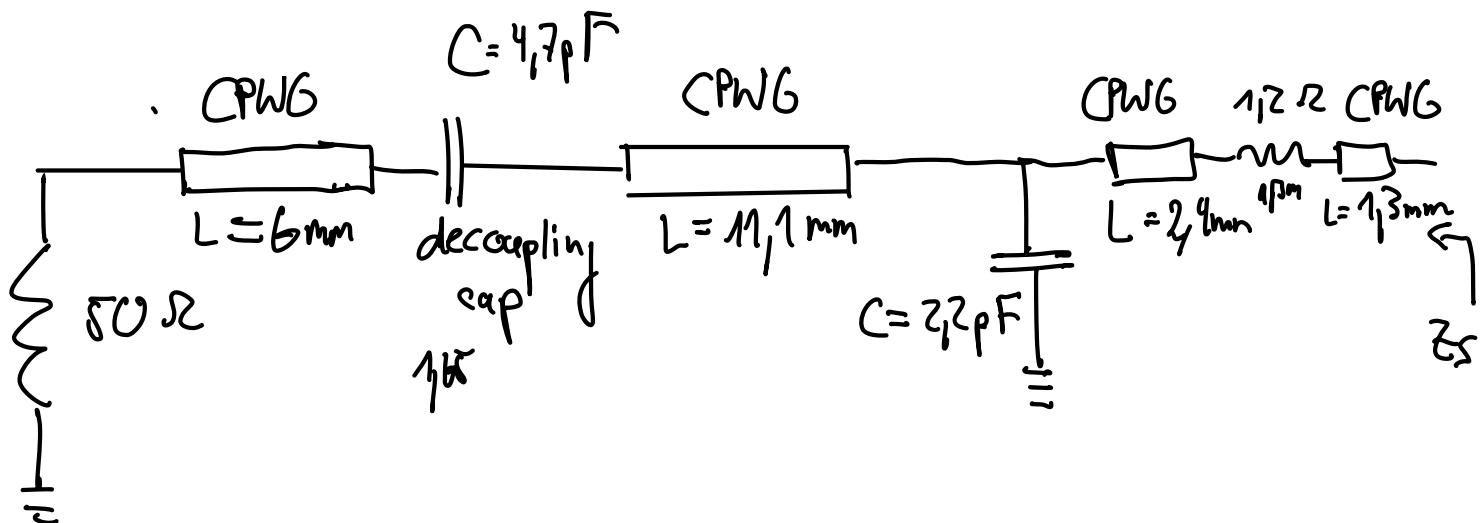
Qucs Simulation:

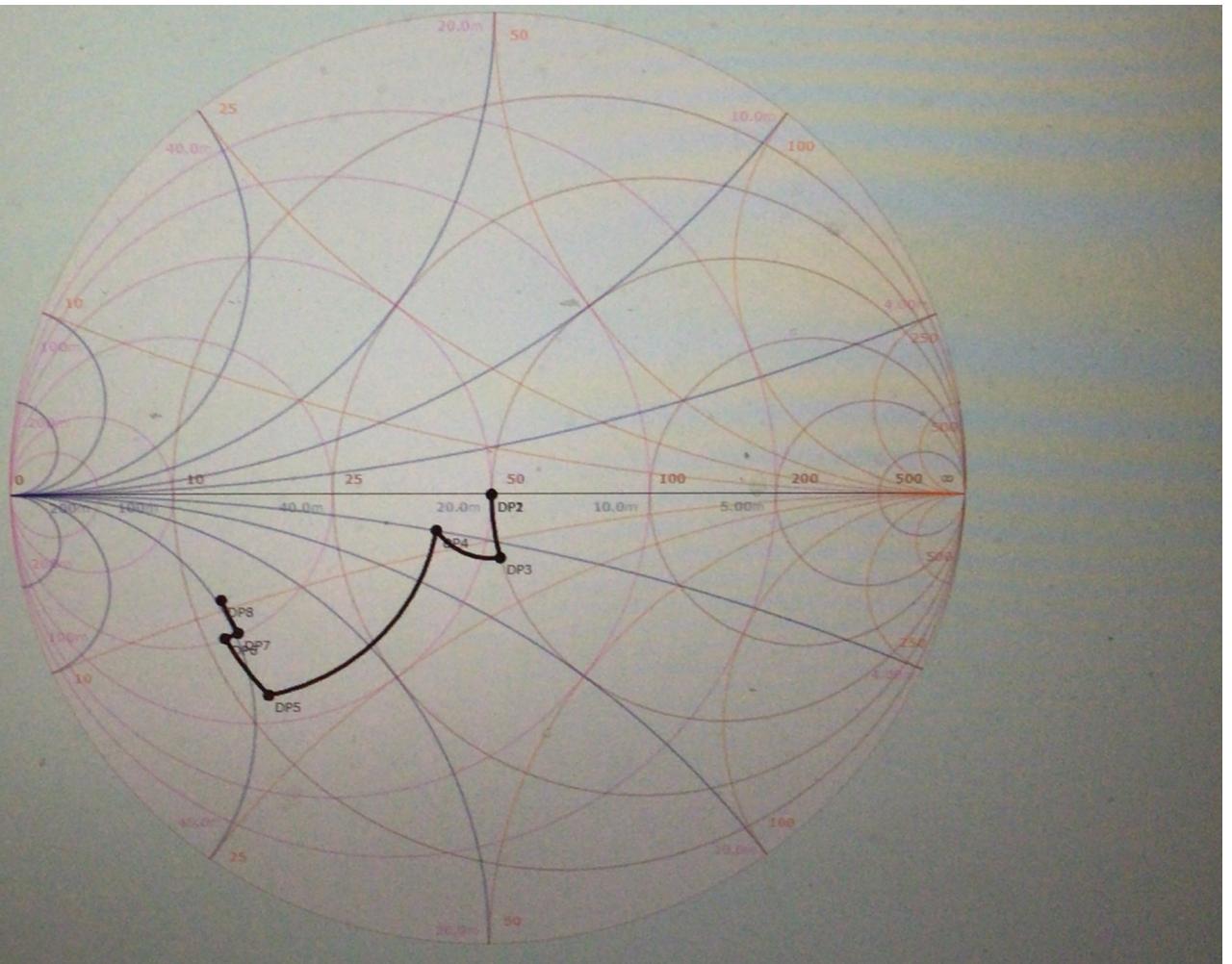


# Reverse engineering of Devboard matching from data sheet:

## Source matching

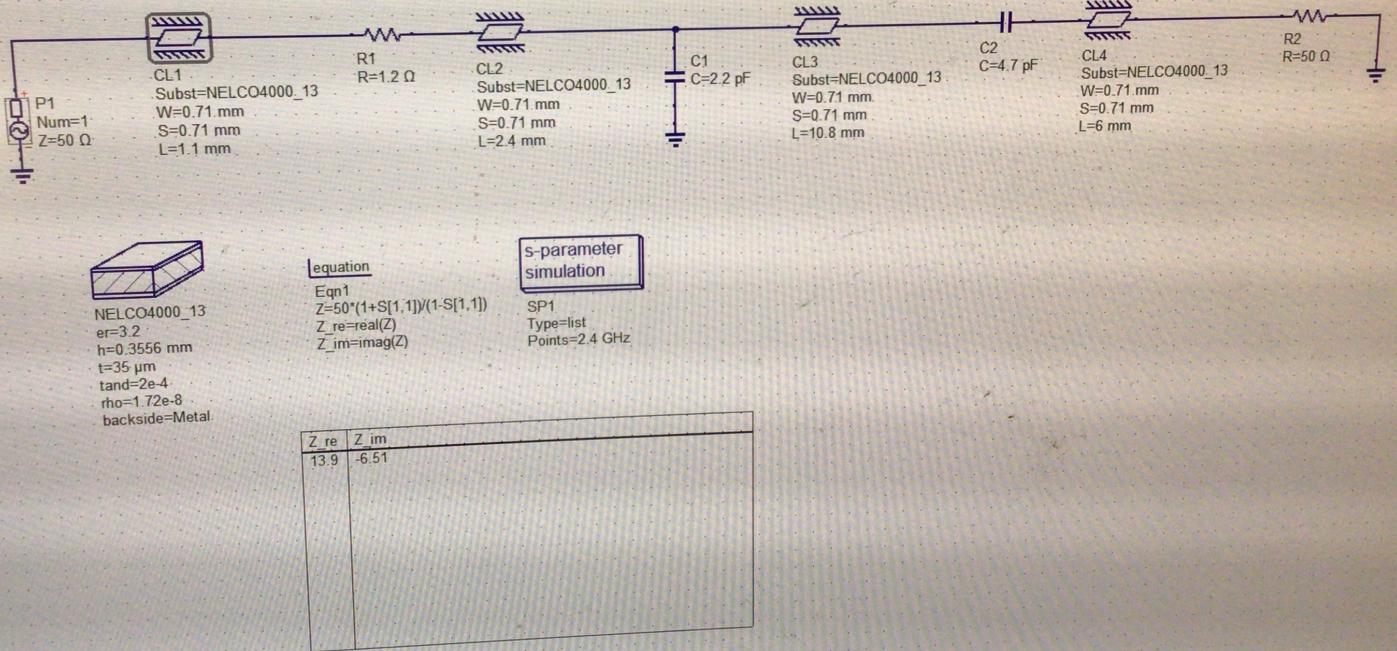
23, 8





$$Z_{S\text{-ideal}} = 6,9 - 7,78j$$

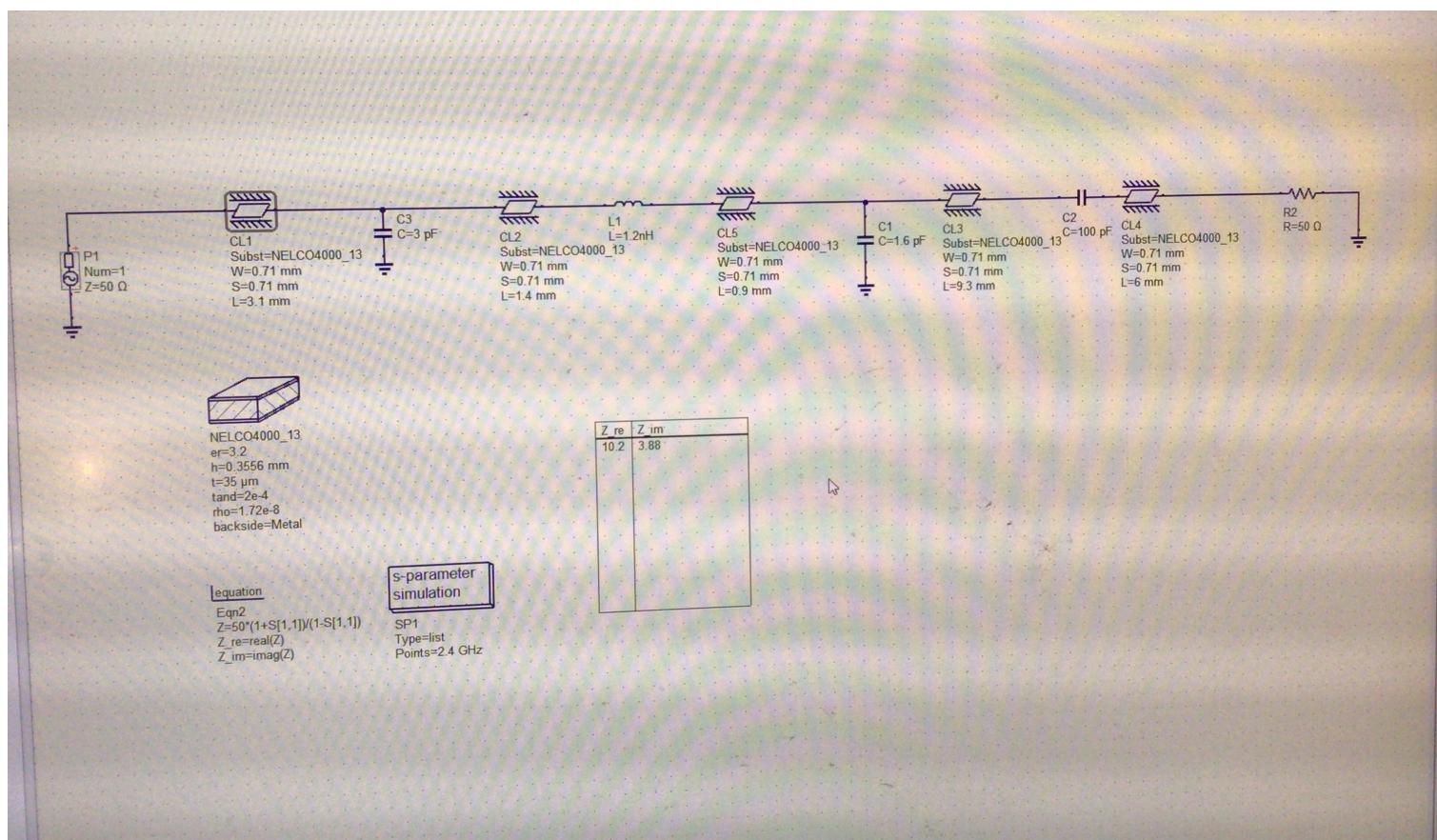
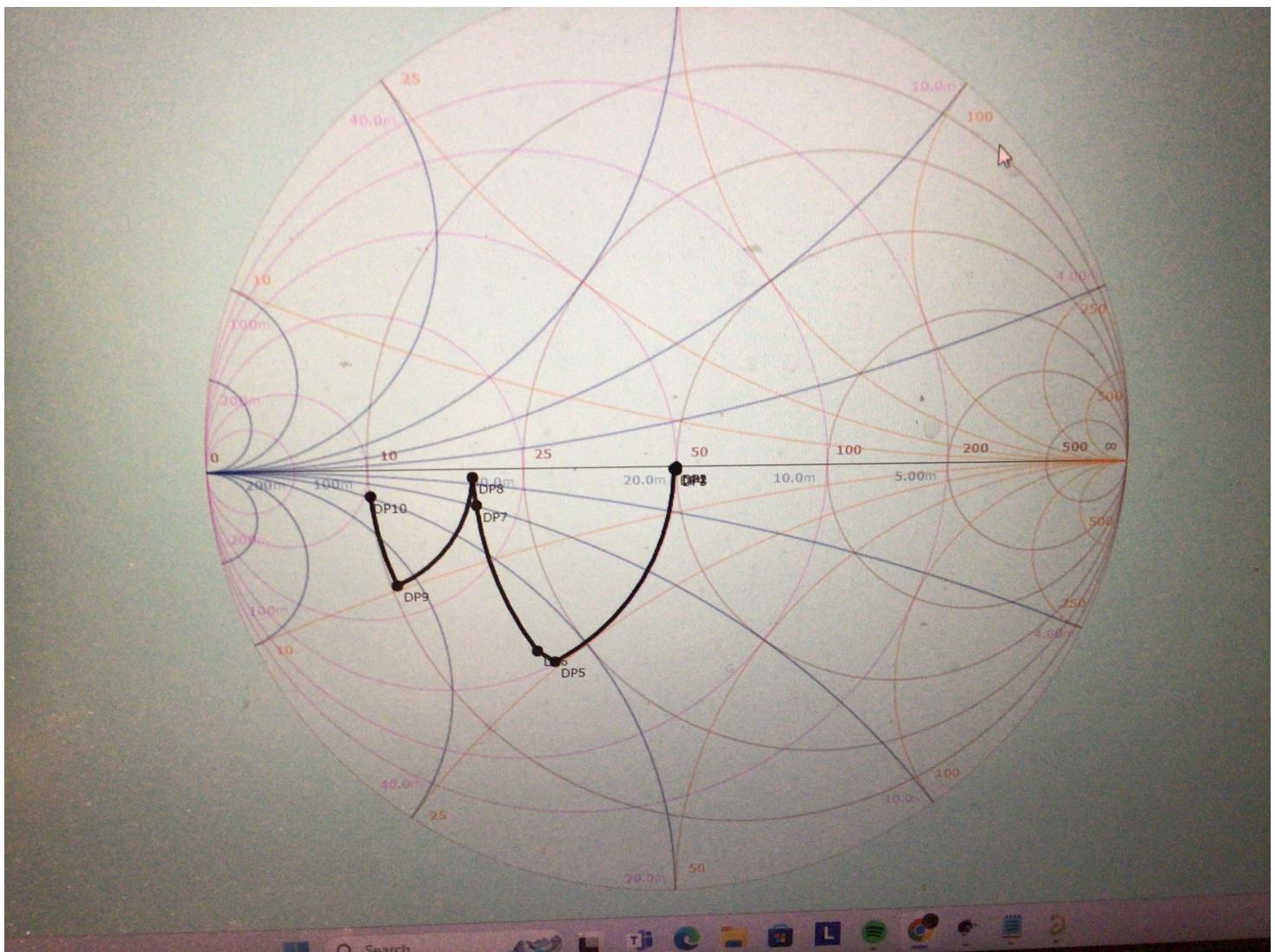
$$Z_{S\text{-sim}} = 13,9 - 6,81j$$



Load matching :

$$Z_{L, \text{ideal}} = 6,11 + 0,32 j$$

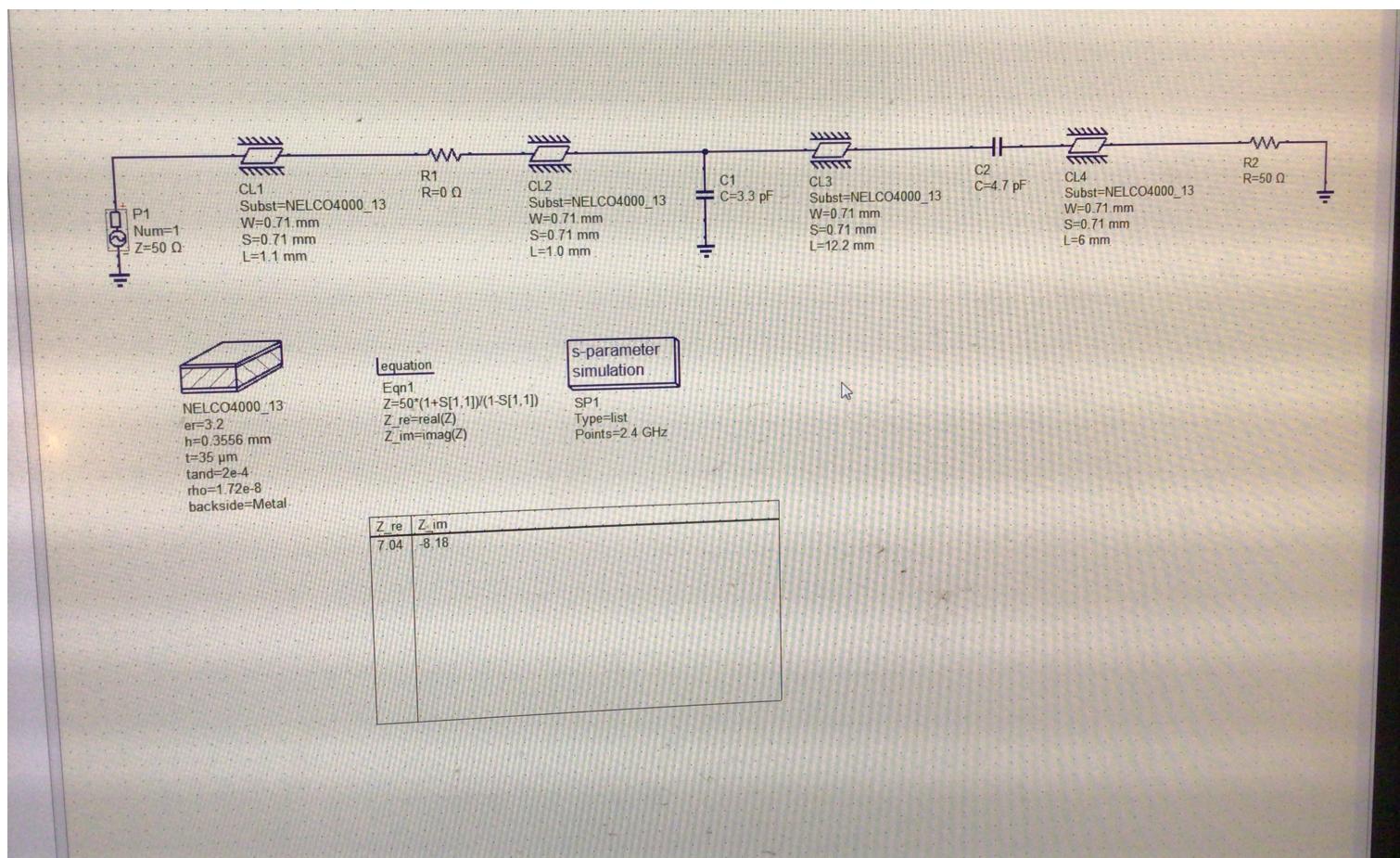
$$Z_{L, \text{sim}} = 10,2 + 3,88 j$$



# Optimising datasheet circuit

I looked at Smith chart and looked what components influence what.

For input matching I moved  $C_1$  closer to  $R_1$  and increased capacitance

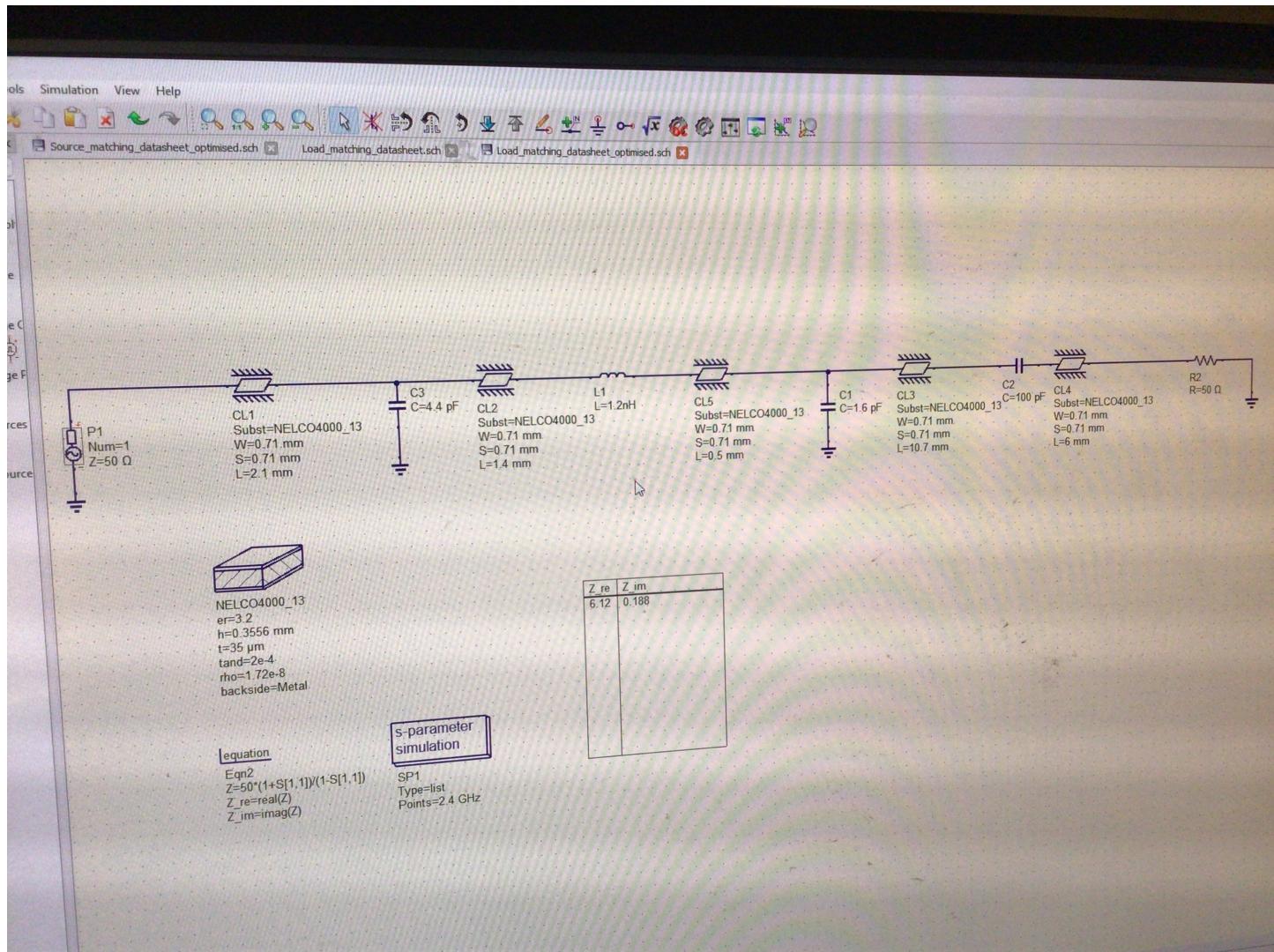


$$Z_{sim} = 7,04 - j8,18$$

$$Z_{ideal} = 6,9 - j7,78$$

for output matching :

Move  $C_1$ ,  $L_1$  and  $C_3$  together 1mm closer to the chip and increase  $C_3$  to  $4.4\text{ pF}$



# Simulation:

