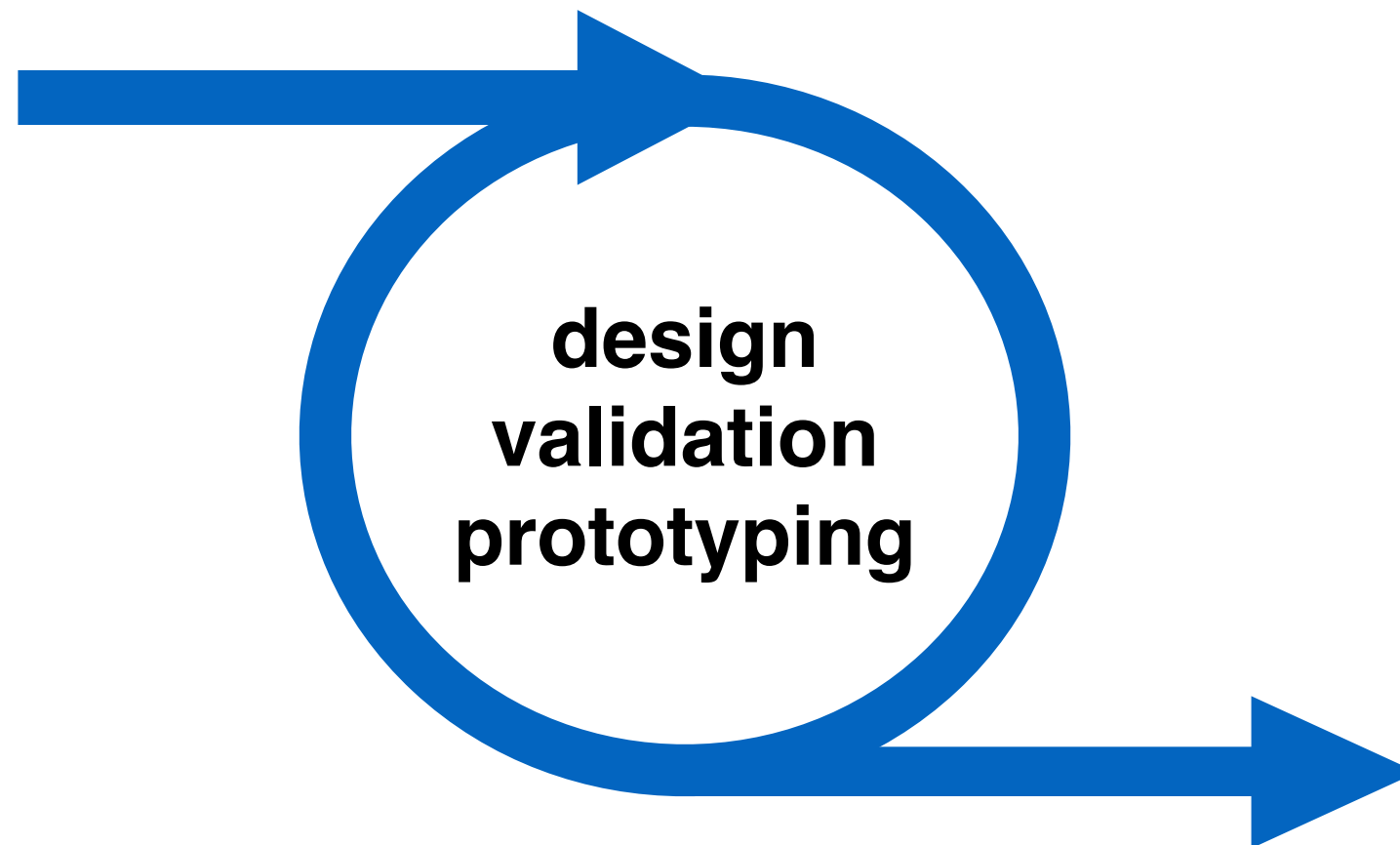


# ICL SDK4FPGA

framework

algorithm



FPGA based  
system

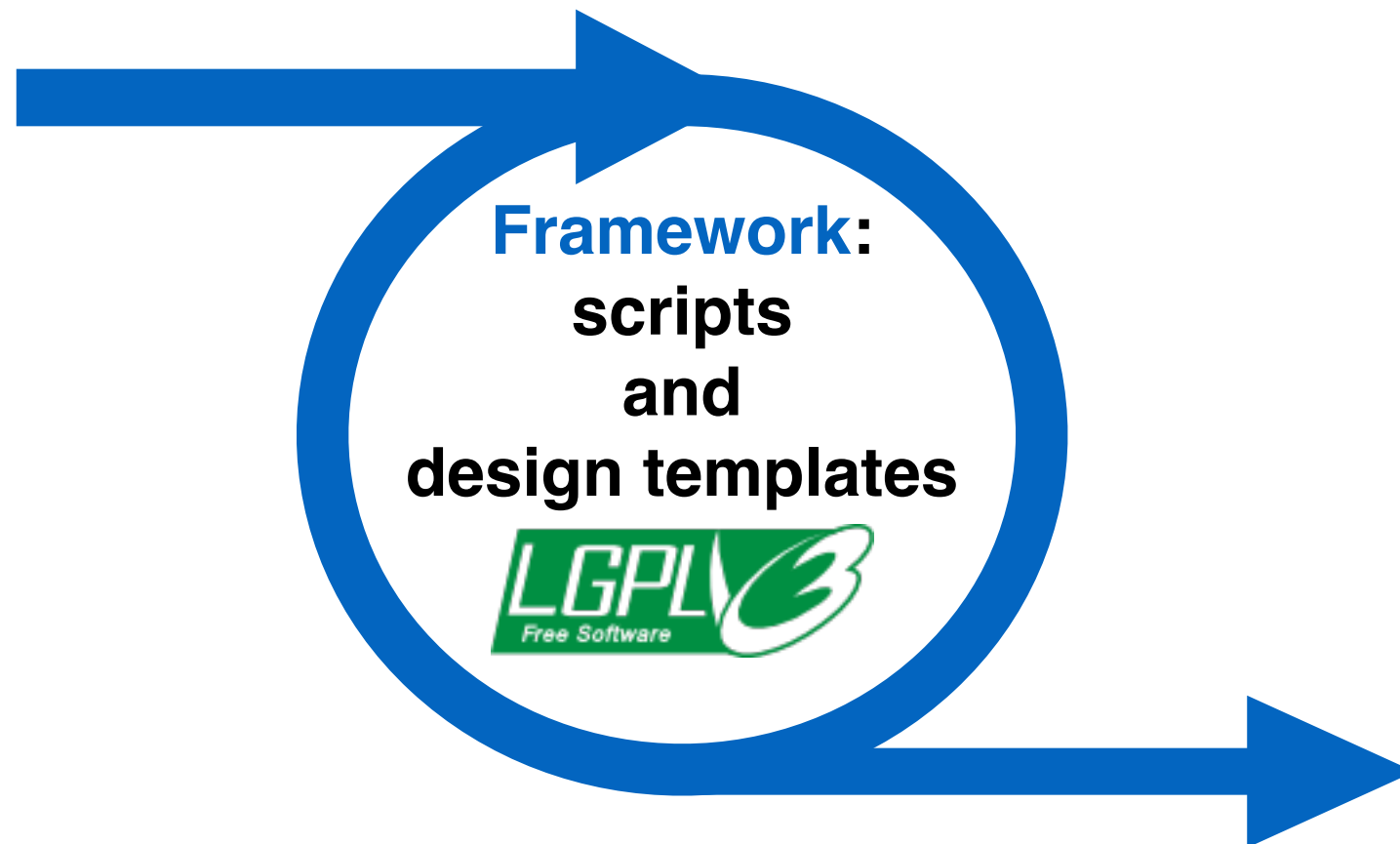


<https://github.com/asuardi/SDK4FPGA.git>  
Andrea Suardi [[a.suardi@imperial.ac.uk](mailto:a.suardi@imperial.ac.uk)]

# Why it ?

- **Enables** researchers and engineers (**with or without FPGA knowhow**) to build their own mathematical algorithms into an FPGA device.
- User needs **only** to **code** his **algorithm**
- **Abstracts low level** FPGA **details** from the user
- Gives **full control (NOT a black box)** of all FPGA project phases (test, build, prototype)

# Ecosystem



## Example designs:

- controller LQR
- controller FGM
- ...



## Plugins:

- design exploration 
- ...



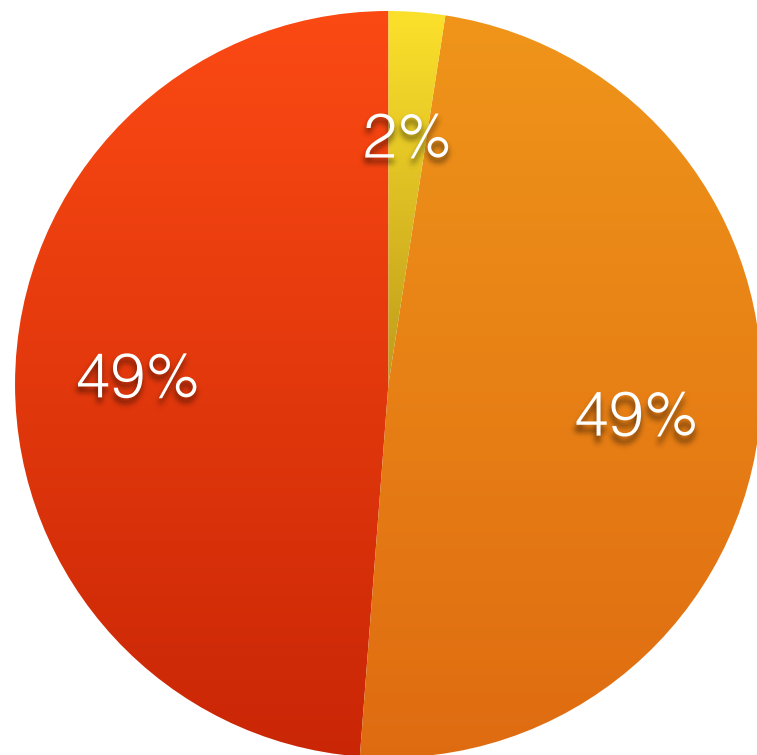
or



# What do I need

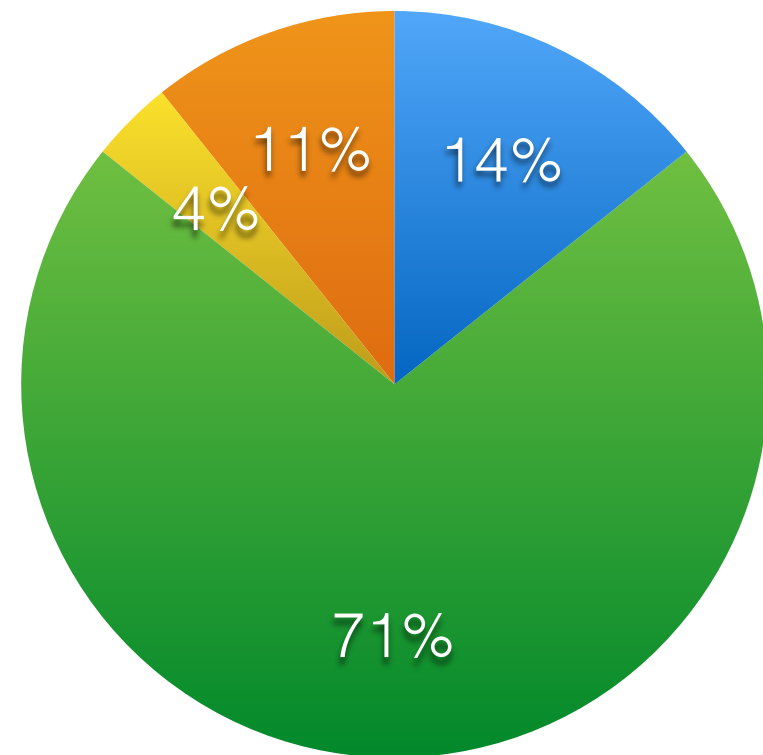
to set up an algorithm running in FPGA ?

● Matlab ● C/C++ ● TCL  
● FPGA ● HDL



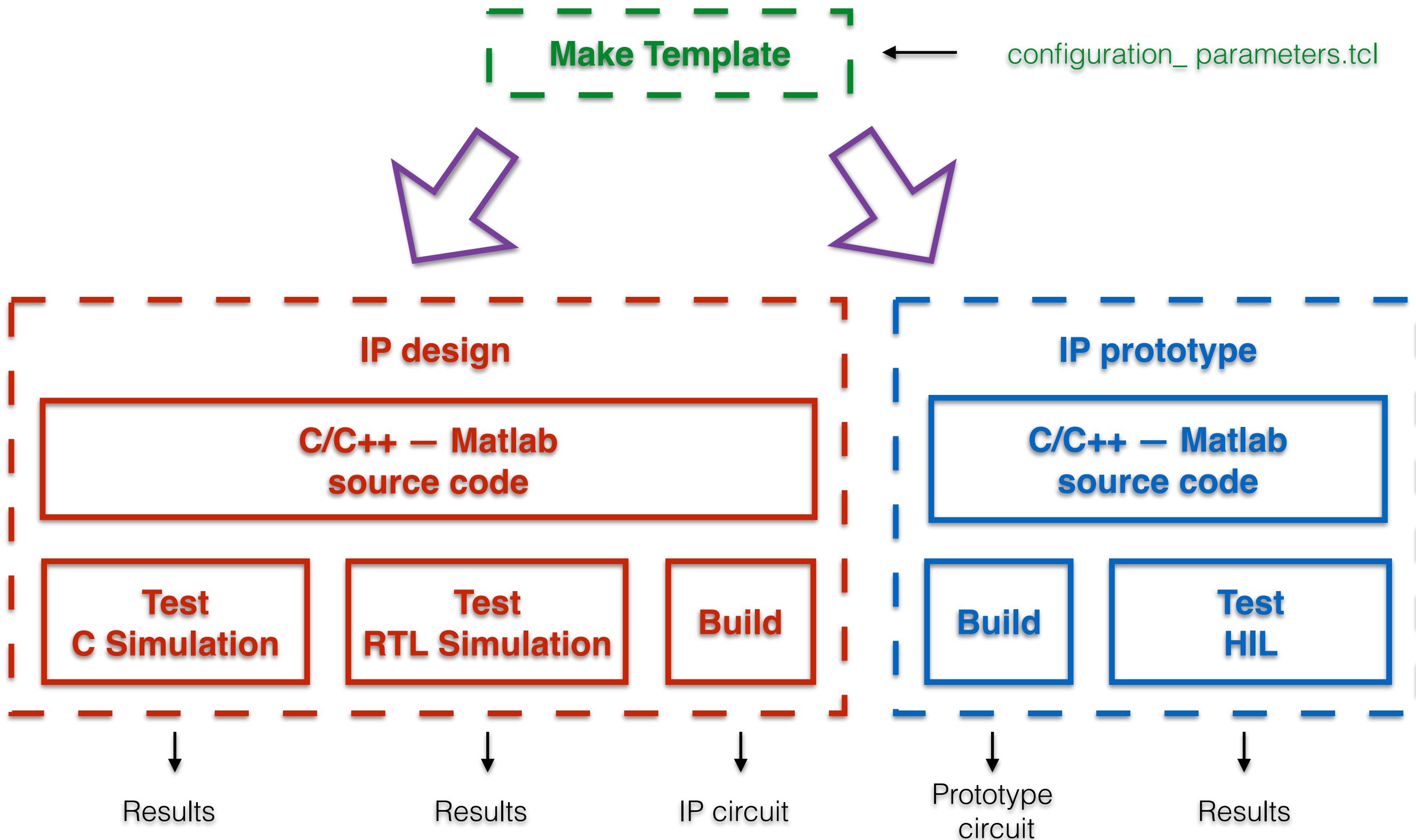
**Standard approach**

● Matlab ● C/C++ ● TCL  
● FPGA ● HDL

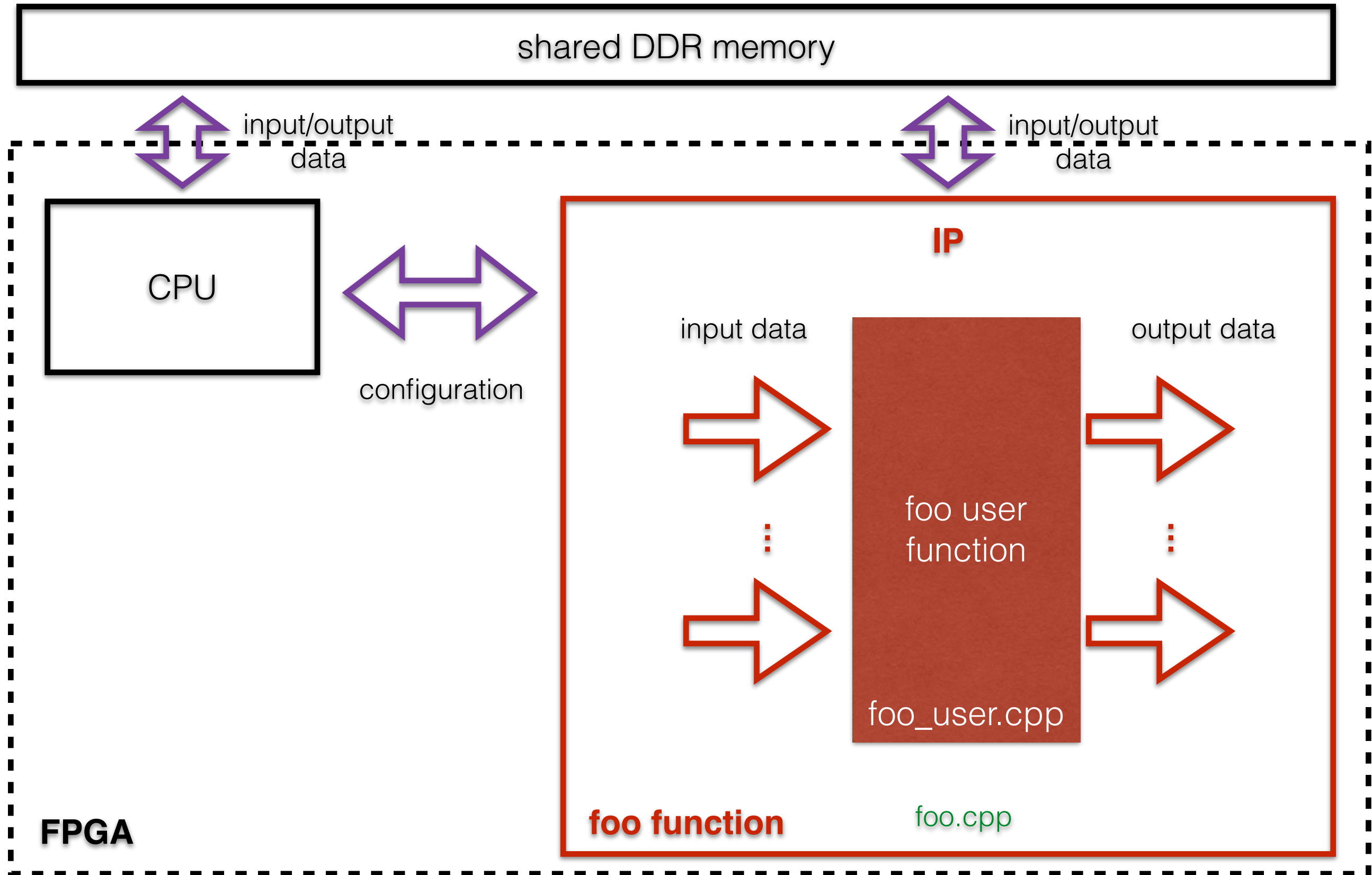


**SDK4FPGA**

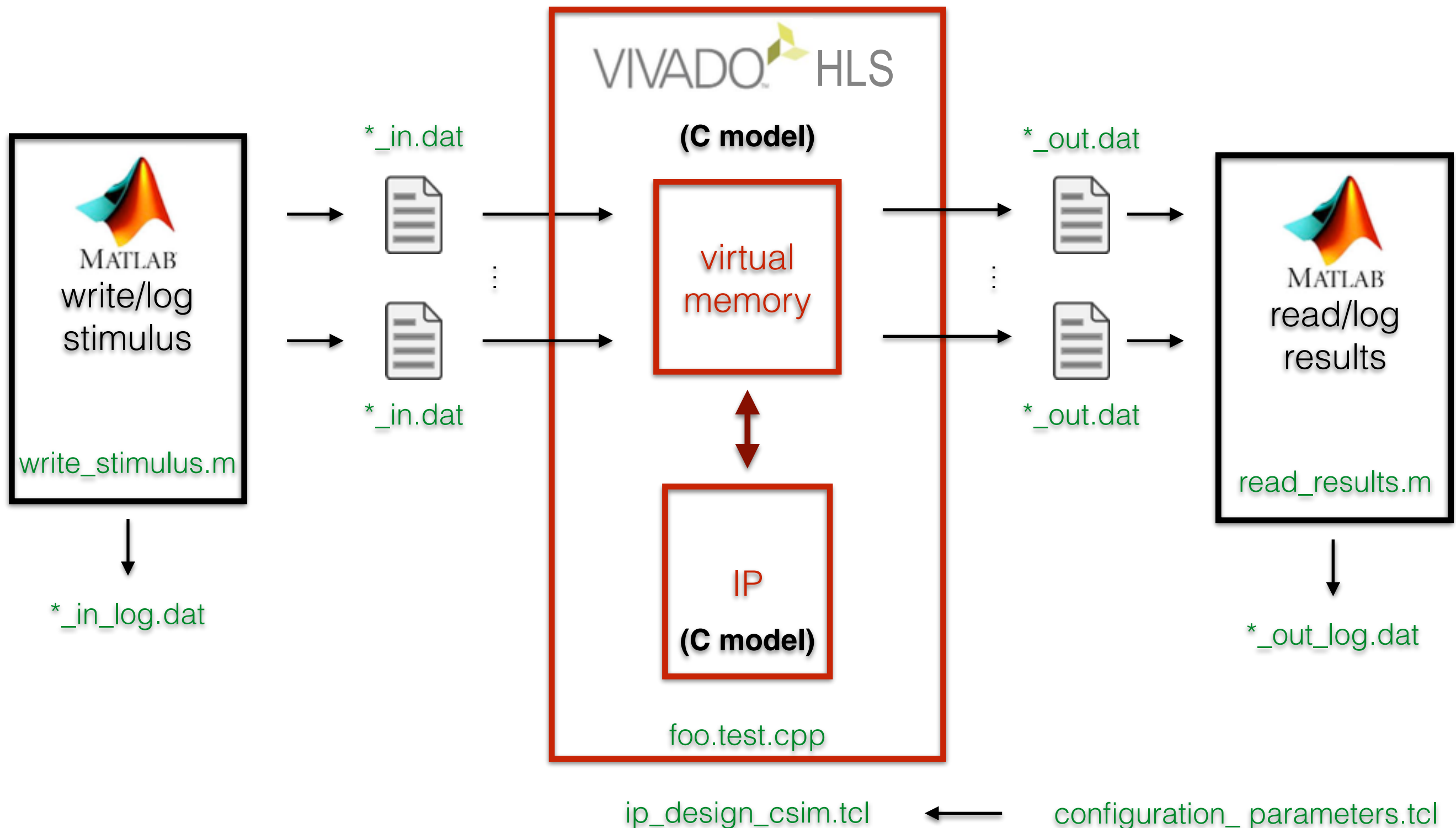
# How does it work?



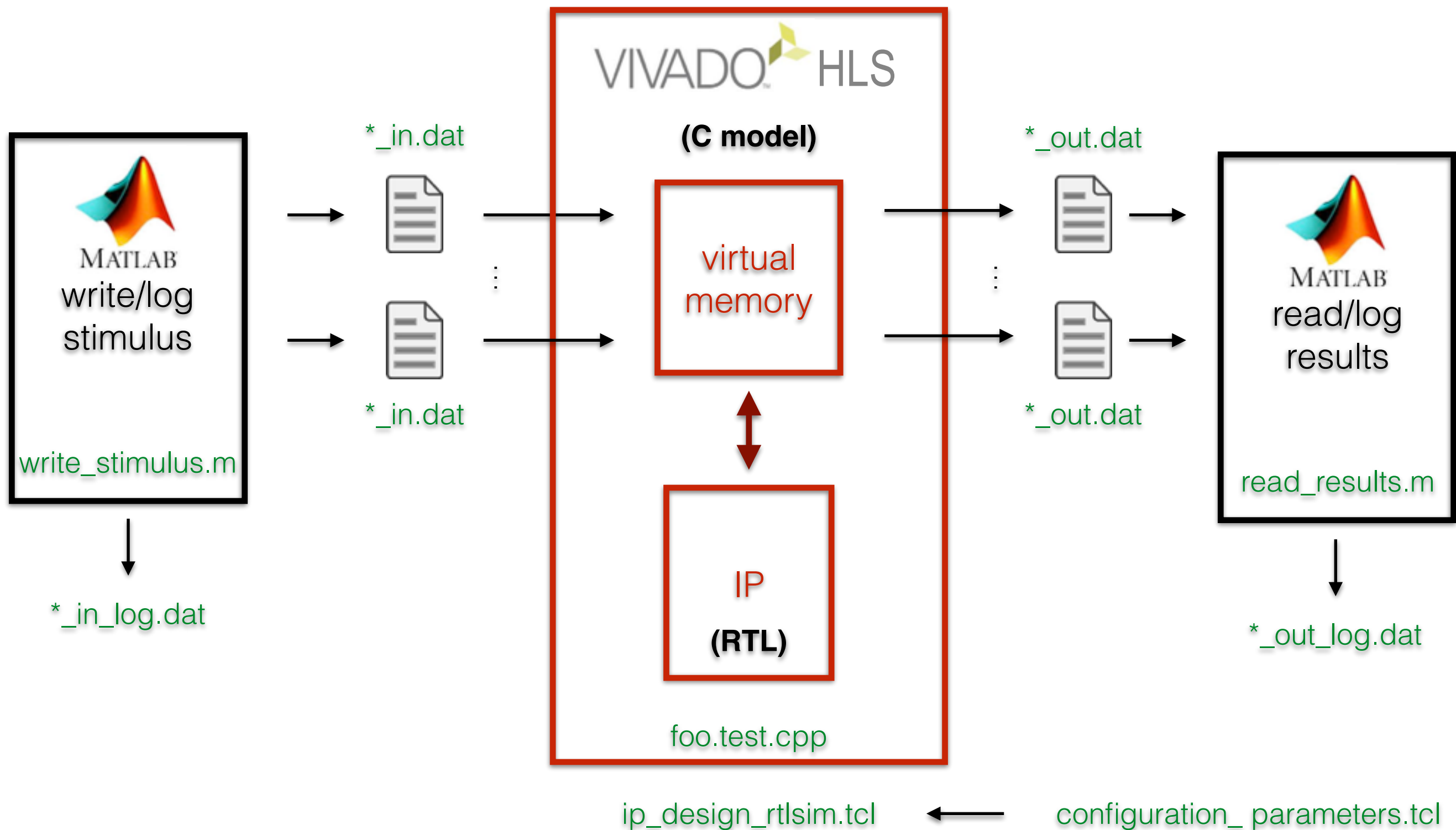
# Hardware architecture



# IP design: c-simulation

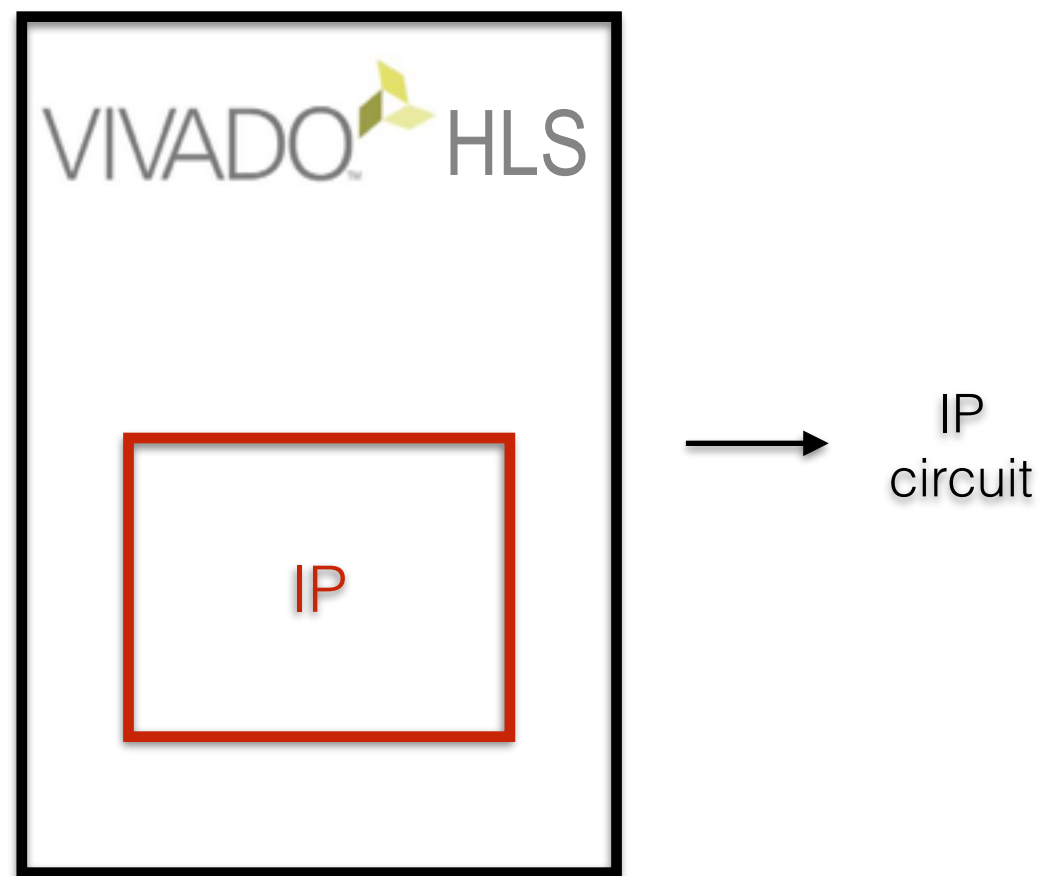


# IP design: RTL-simulation





# IP design: build

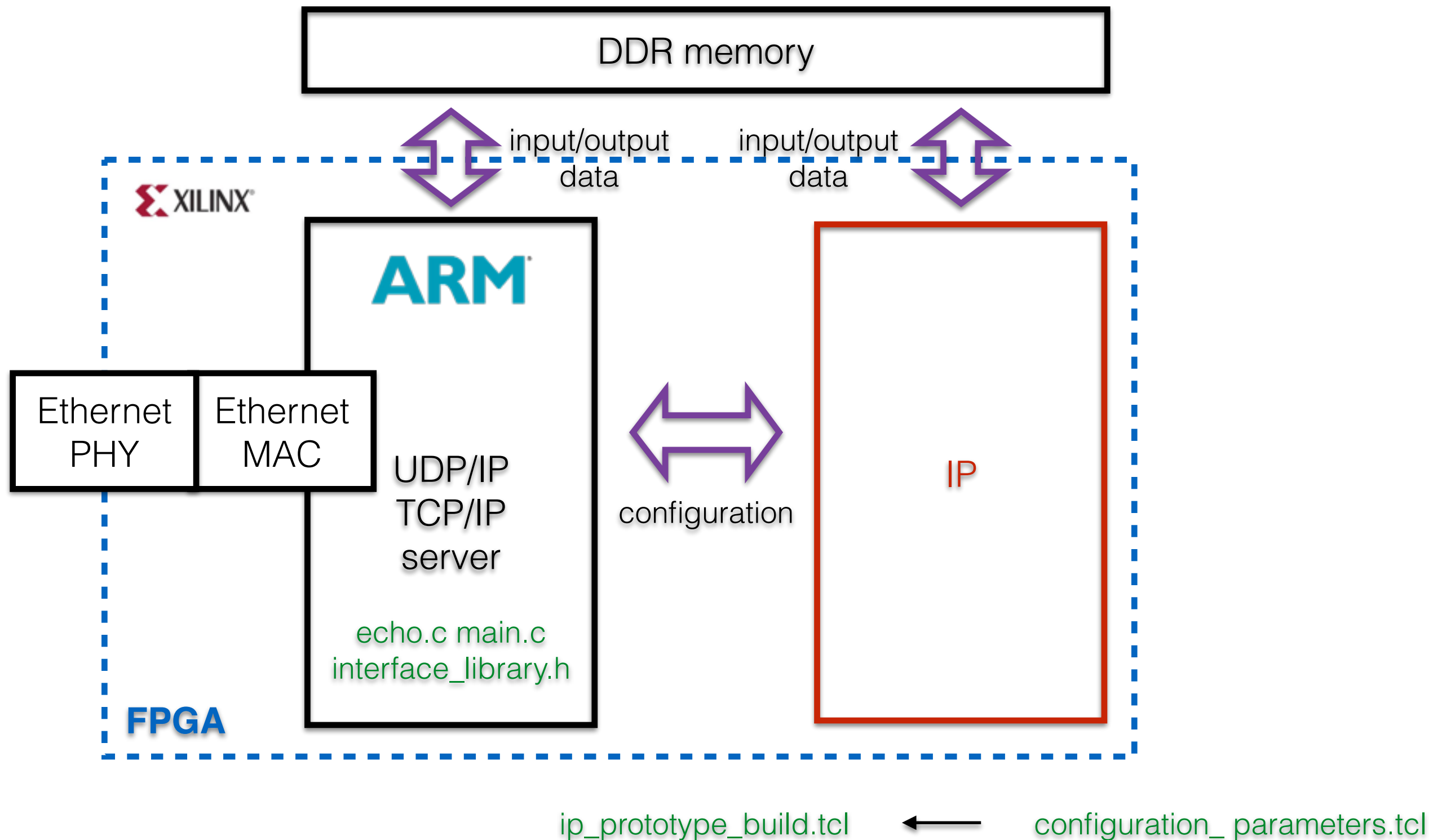


ip\_design\_build.tcl

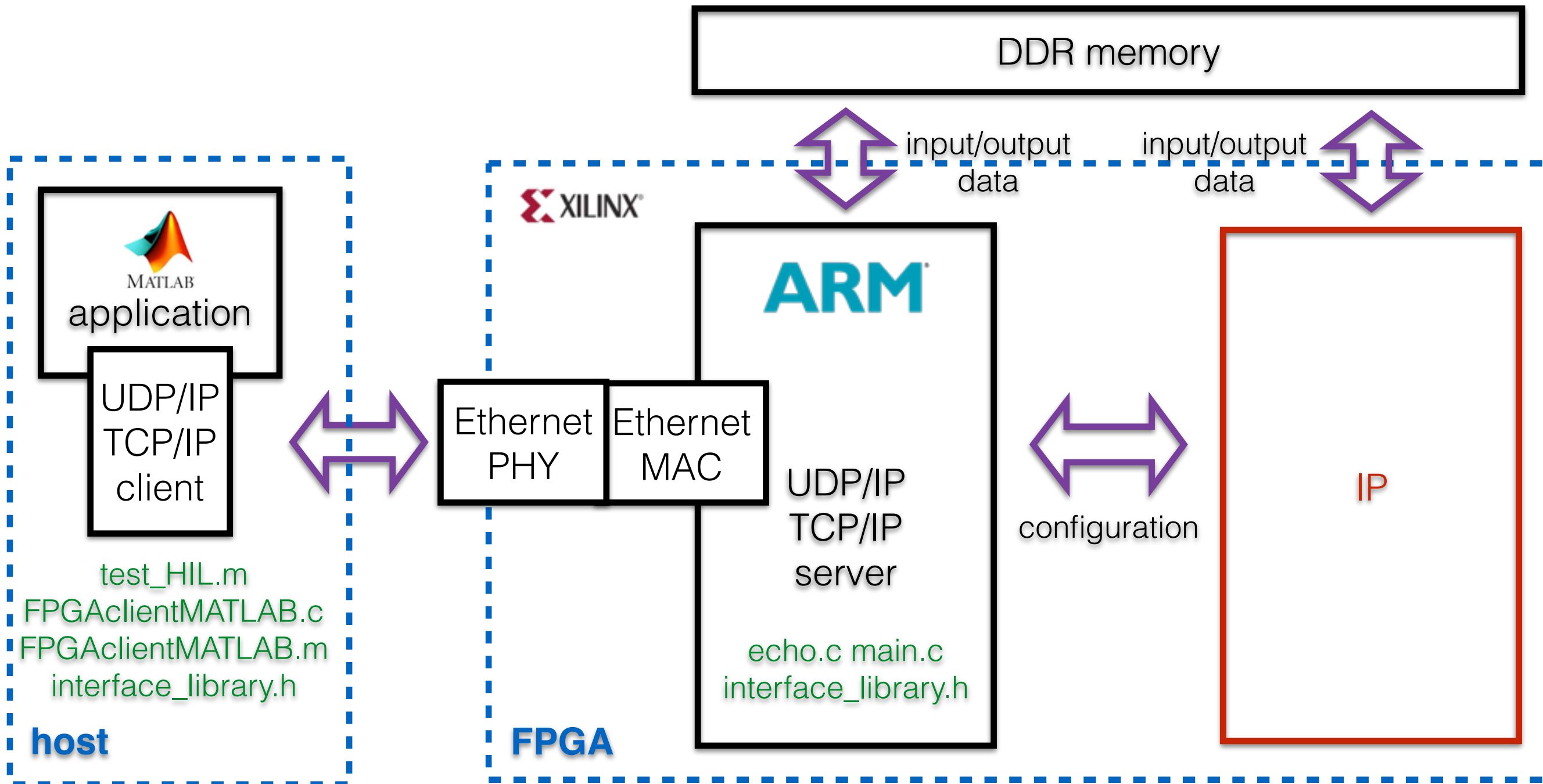


configuration\_parameters.tcl

# IP prototype: build



# IP prototype: test\_HIL





**WE WANT YOU!**



<https://github.com/asuardi/SDK4FPGA.git>  
Andrea Suardi [[a.suardi@imperial.ac.uk](mailto:a.suardi@imperial.ac.uk)]