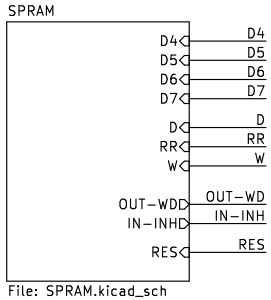
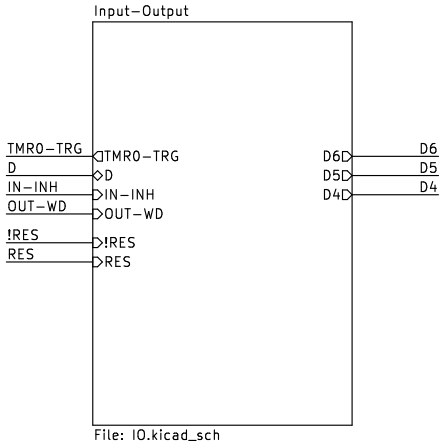
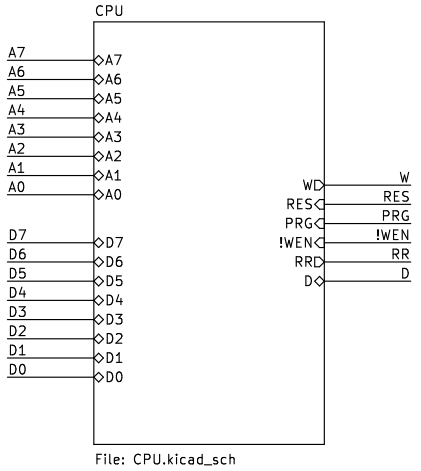
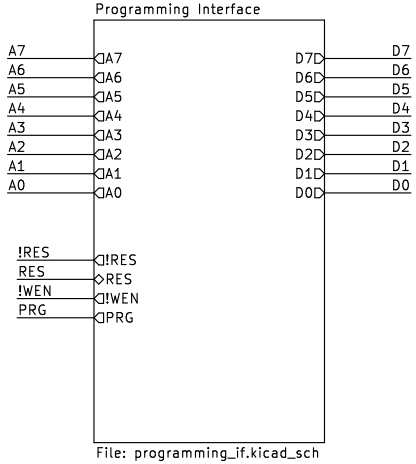








REV.D

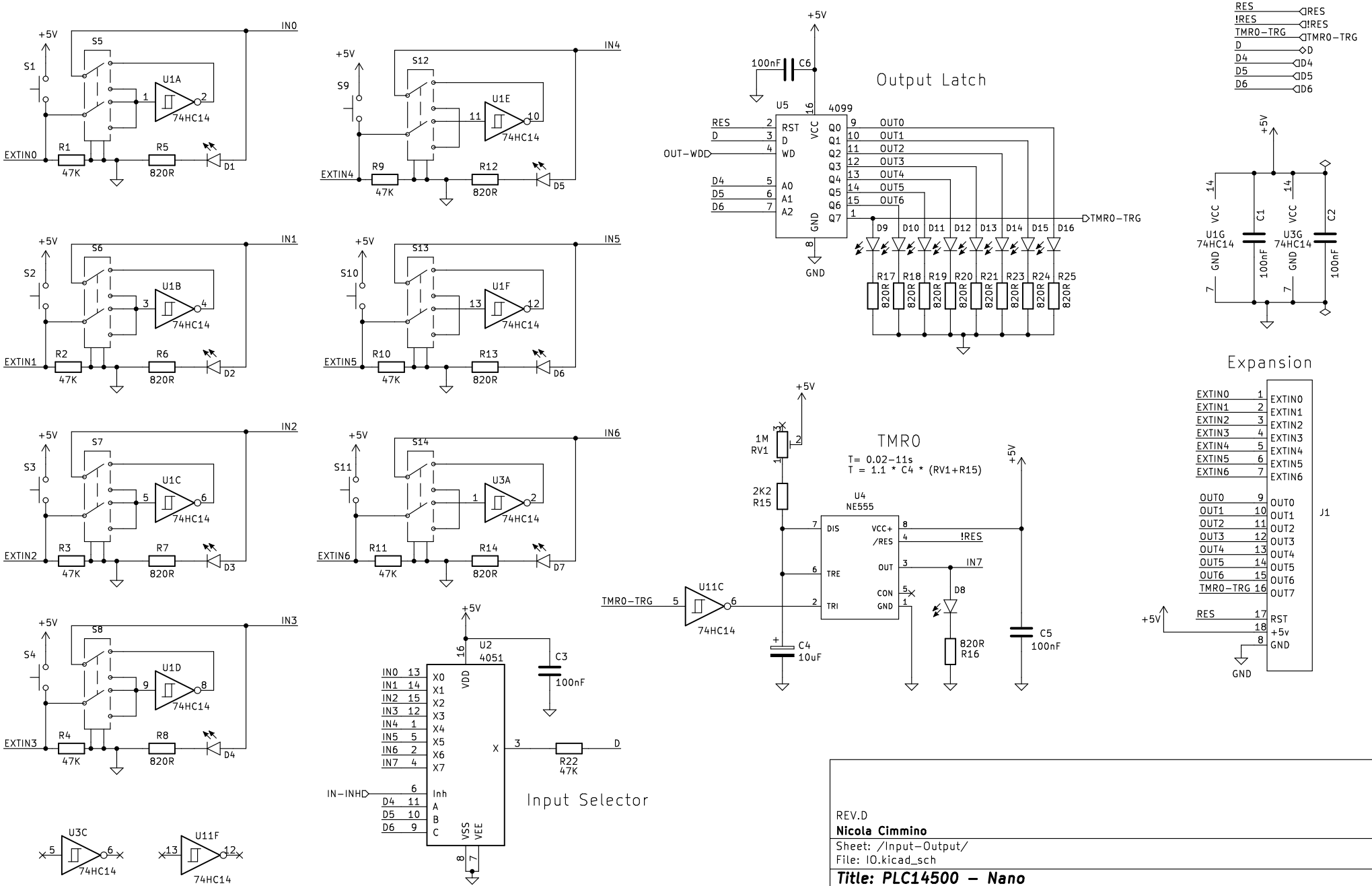
Nicola Cimmino

Sheet: /

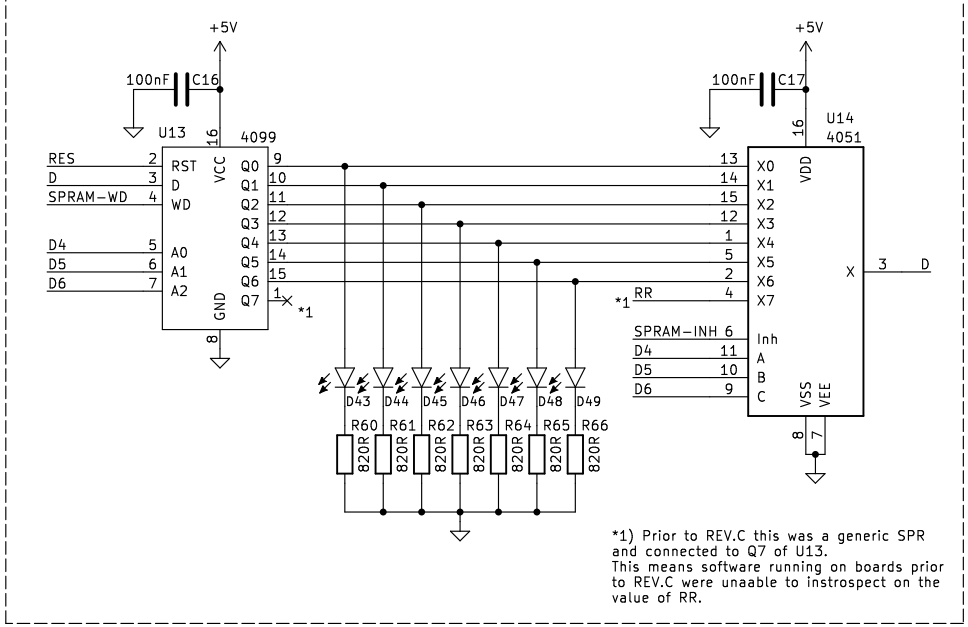
File: plc14500.kicad_sch

Title: PLC14500 – Nano

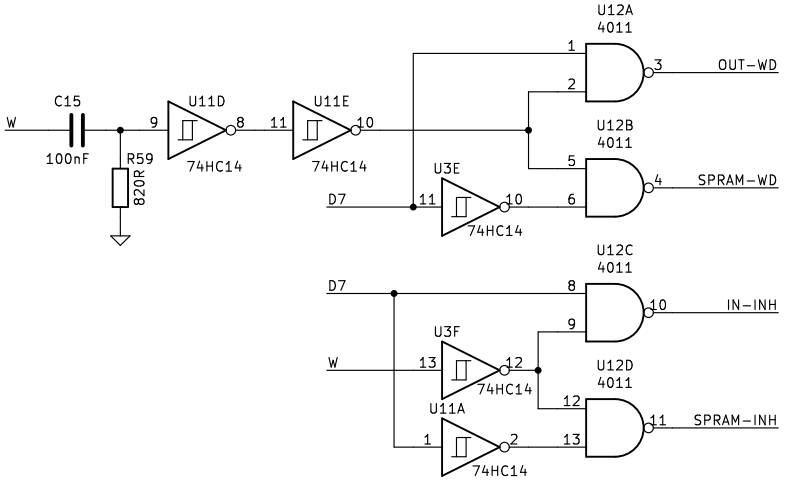
Size: A4	Date: 2024-01-22	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.7		Id: 1/5


IN0
IN1
IN2
IN3
IN4
IN5
IN6
+5V
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
U1A
U1B
U1C
U1D
U1E
U1F
U3A
74HC14
EXTIN0
EXTIN1
EXTIN2
EXTIN3
EXTIN4
EXTIN5
EXTIN6
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
47K
820R
D1
D2
D3
D4
D5
D6
D7
U3C
U11F
U2
4051
C3
100nF
IN-INH
R22
D
Input Selector
100nF
C6
U5
4099
RES
D
OUT-WD
D4
D5
D6
RST
WD
A0
A1
A2
VCC
GND
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
TMR0-TRG
D9
D10
D11
D12
D13
D14
D15
D16
R17
R18
R19
R20
R21
R23
R24
R25
Output Latch
!RES
U1G
U3G
C1
C2
Expansion
J1
+5v
1M
RV1
2K2
R15
TMR0
T= 0.02-11s
T = 1.1 * C4 * (RV1+R15)
U4
NE555
DIS
TRE
TRI
VCC+
/RES
OUT
CON
IN7
D8
R16
C4
10uF
C5
U11C
REV.D
Nicola Cimmino
Sheet: /Input-Output/
File: IO.kicad_sch
Title: PLC14500 - Nano
Size: A4
Date: 2024-01-22
Rev: 0.6
KiCad E.D.A. kicad 7.0.7
Id: 2/5

Scratchpad RAM



Write Line Glue Logic



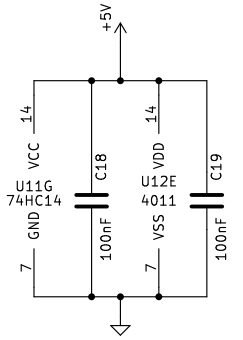
W	D7	OUT-WD	SPRAM-WD	IN-INH	SPRAM-INH	
0	0	1	1	1	0	Read Scratchpad RAM
0	1	1	1	0	1	Read Inputs
1	0	1	0	1	1	Write Scratchpad RAM
1	1	0	1	1	1	Write Outputs

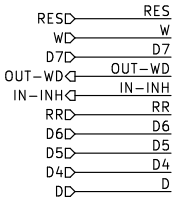
W – Is the Write line from the MC14500. When asserted the processor wants to write out D. The 4 lines from the Write Line Glue logic address what is being written to or read from.

D7 is the msb of the program byte currently executed and addresses the I/O if set or the SPRAM is clear.

IN-INH and SPRAM-INH control the INH line of the input sekector and SPRAM selector respectively. When asserted the outputs will be in HiZ thus releasing the D line.

OUT-WD and SPRAM-WD control the WD of the input latch and output latch respectively. When asserted the latc will ignore changes on the D line.

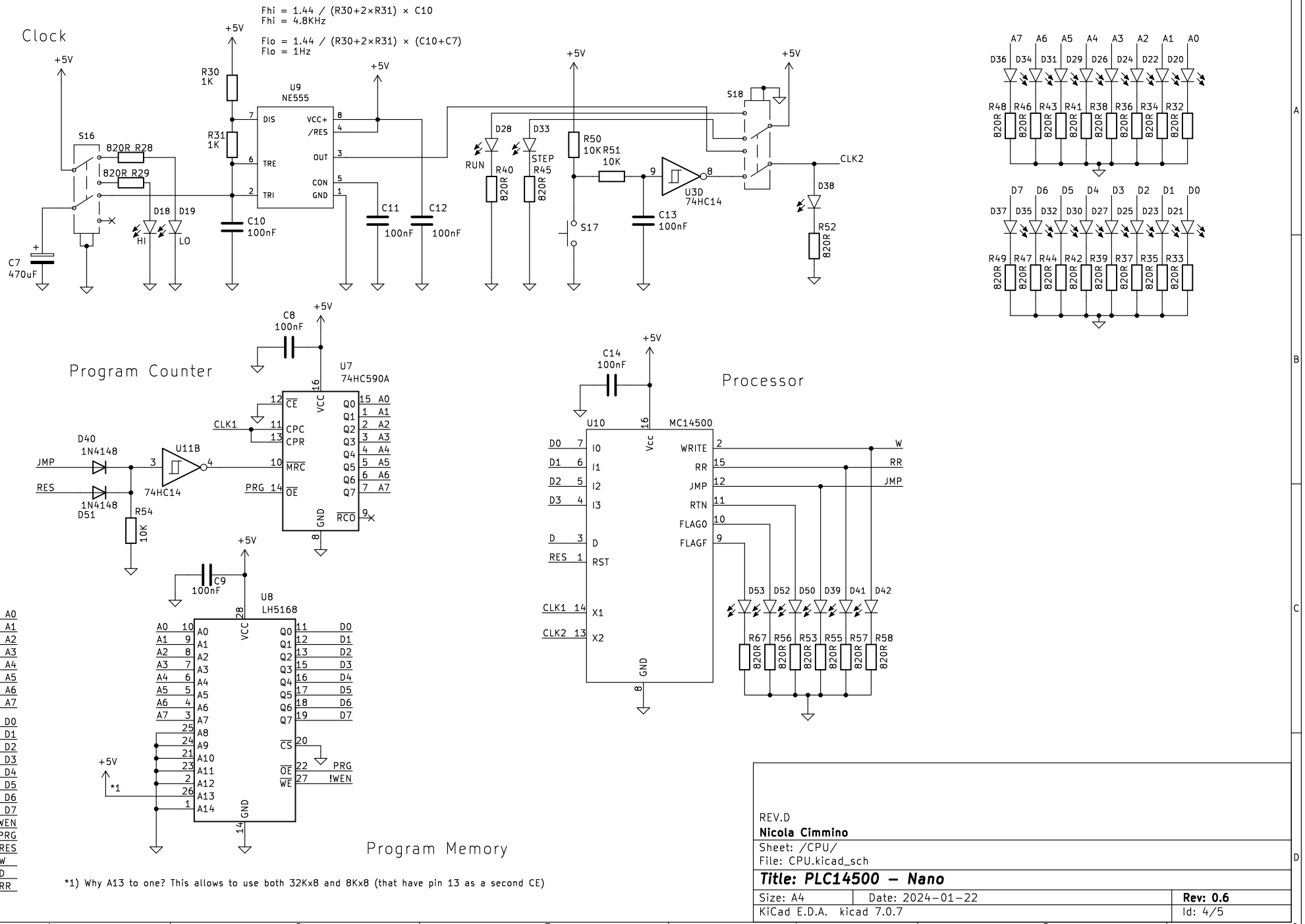




REV.D
Nicola Cimmino
Sheet: /SPRAM/
File: SPRAM.kicad_sch

Title: PLC14500 – Nano

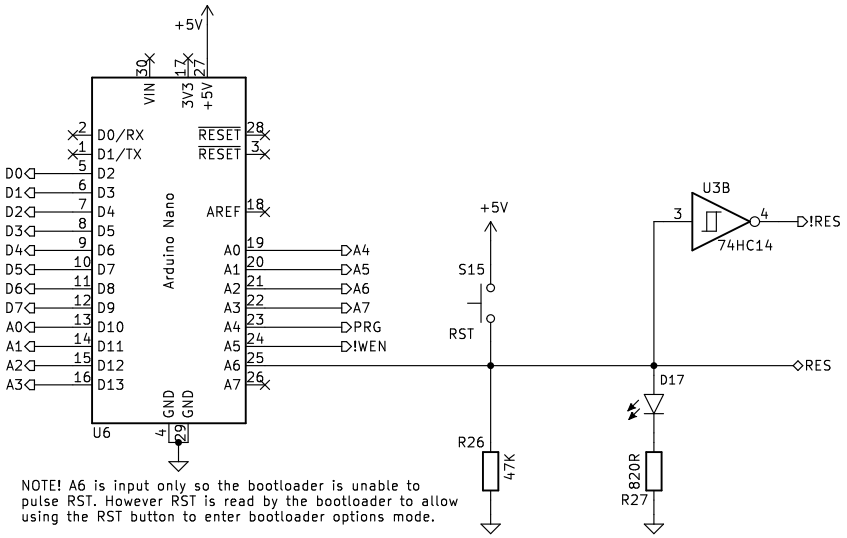
Size: A4	Date: 2024-01-22	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.7		Id: 3/5


Clock
Fhi = 1.44 / (R30+2×R31) × C10
Fhi = 4.8KHz
Flo = 1.44 / (R30+2×R31) × (C10+C7)
Flo = 1Hz
+5V
R30 1K
R31 1K
U9 NE555
DIS
VCC+
/RES
TRE
OUT
CON
TRI
GND
S16
820R R28
820R R29
D18
D19
HI
LO
C7 470uF
C10 100nF
C11 100nF
C12 100nF
D28
D33
RUN
STEP
R40 820R
R45 820R
R50 10K
R51 10K
S17
U3D 74HC14
C13 100nF
S18
CLK2
D38
R52 820R
A7 A6 A5 A4 A3 A2 A1 A0
D36 D34 D31 D29 D26 D24 D22 D20
R48 R46 R43 R41 R38 R36 R34 R32
D7 D6 D5 D4 D3 D2 D1 D0
D37 D35 D32 D30 D27 D25 D23 D21
R49 R47 R44 R42 R39 R37 R35 R33
Program Counter
C8 100nF
U7 74HC590A
CE
VCC
CPC
CPR
MRC
OE
RCO
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
CLK1
PRG
D40 1N4148
D51 1N4148
JMP
RES
U11B 74HC14
R54 10K
Processor
C14 100nF
U10 MC14500
I0 I1 I2 I3 D RST X1 X2
Vcc
GND
WRITE
RR
JMP
RTN
FLAG0
FLAGF
D0 D1 D2 D3 D RES CLK1 CLK2
W
RR
JMP
D53 D52 D50 D39 D41 D42
R67 R56 R53 R55 R57 R58
C9 100nF
U8 LH5168
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
D0 D1 D2 D3 D4 D5 D6 D7
CS
OE
WE
!WEN
PRG
*1
Program Memory
A0 A1 A2 A3 A4 A5 A6 A7
D0 D1 D2 D3 D4 D5 D6 D7
!WEN PRG RES W D RR
*1) Why A13 to one? This allows to use both 32Kx8 and 8Kx8 (that have pin 13 as a second CE)
REV.D
Nicola Cimmino
Sheet: /CPU/
File: CPU.kicad_sch
Title: PLC14500 – Nano
Size: A4
Date: 2024-01-22
Rev: 0.6
KiCad E.D.A. kicad 7.0.7
Id: 4/5

The programmer asserts the PRG line to take control of the bus. This causes the PC address lines to go to HiZ.

!WEN is cleared by the programmer once each program byte value and address is stable. This triggers a write in RAM.

The programmer, or the user, can assert the RES line to cause a reset of the PC and of the latches.



NOTE! A6 is input only so the bootloader is unable to pulse RST. However RST is read by the bootloader to allow using the RST button to enter bootloader options mode.

REV.D

Nicola Cimmino

Sheet: /Programming Interface/
File: programming_if.kicad_sch

Title: PLC14500 – Nano

Size: A4	Date: 2024-01-22	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.7		Id: 5/5