

REV.D

Nicola Cimmino

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File: plc14500.kicad_sch

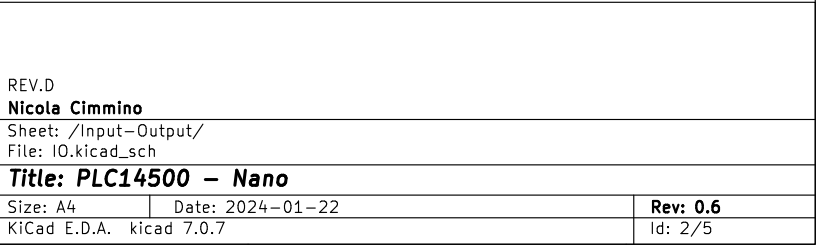
Title: PLC14500 – Nano

Size: A4 Date: 2024-01-22

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Id: 1/5



The circuit diagram illustrates the Write Line Glue Logic for the MC14500. It features several 74HC14 inverters (U11D, U11E, U3E, U3F, U11A) and 4011 NAND gates (U12A, U12B, U12C, U12D). The inputs include the Write signal (W), D7, and various control signals. The outputs are OUT-WD, SPRAM-WD, IN-INH, and SPRAM-INH. A timing diagram for W is shown at the top left.

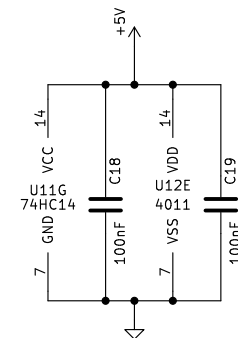
W	D7	OUT-WD	SPRAM-WD	IN-INH	SPRAM-INH	
0	1	1	1	0	1	Read Scratchpad RAM
0	1	1	0	1	1	Read Inputs
1	0	1	0	1	1	Write Scratchpad RAM
1	1	0	1	1	1	Write Outputs

W – Is the Write line from the MC14500. When asserted the processor wants to write out D. The 4 lines from the Write Line Glue logic address what is being written to or read from.

D7 is the msb of the program byte currently executed and addresses the I/O if set or the SPRAM is clear.

IN-INH and SPRAM-INH control the INH line of the input selector and SPRAM selector respectively. When asserted the outputs will be in HIZ thus releasing the D line.

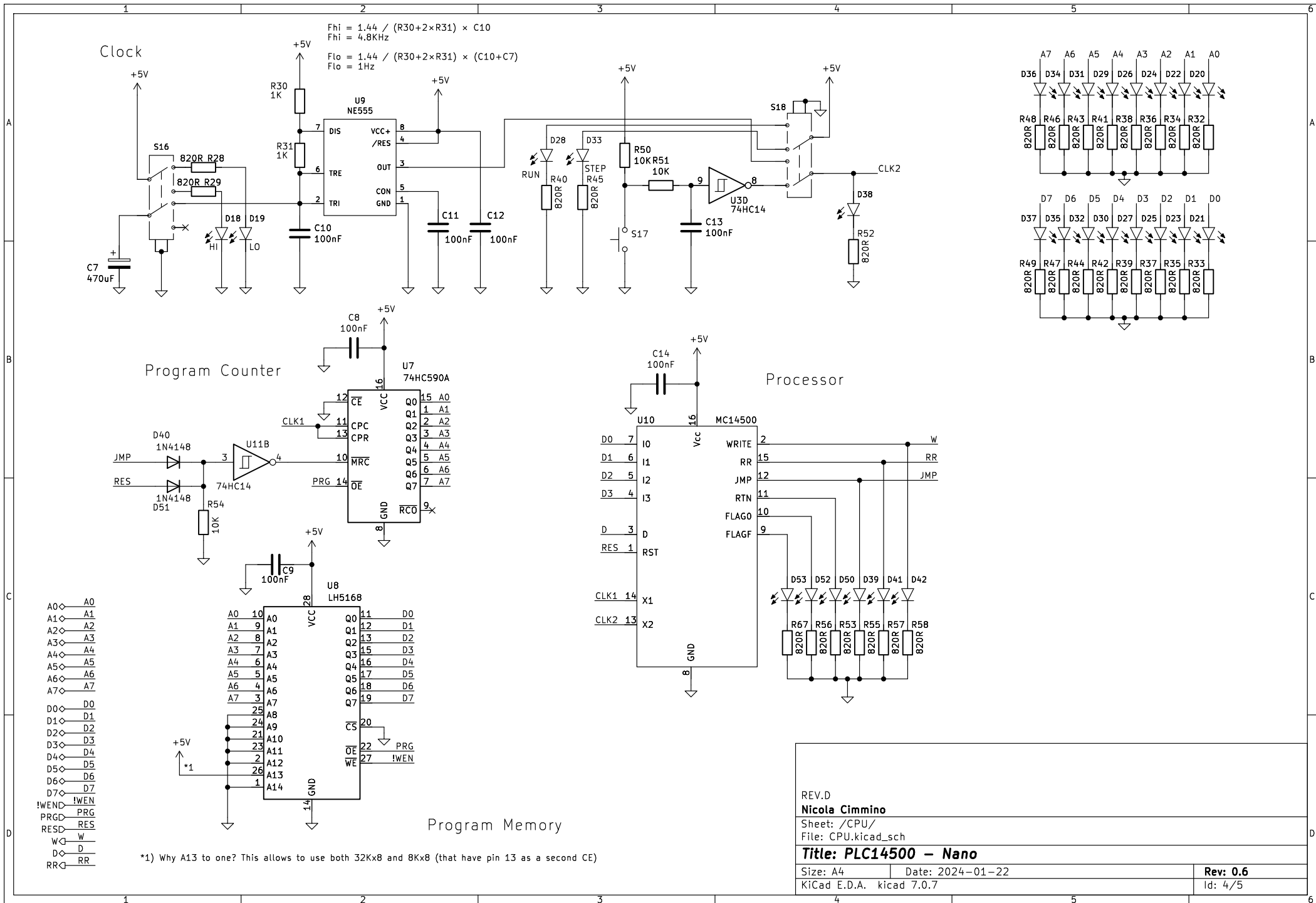
OUT-WD and SPRAM-WD control the WD of the input latch and output latch respectively. When asserted the latch will ignore changes on the D line.

[illegible]

*1) Prior to REV.C this was a generic SPR and connected to Q7 of U13. This means software running on boards prior to REV.C were unable to introspect on the value of RR.

RES	RES
WD	W
D7	D7
OUT-WD	OUT-WD
IN-INH	IN-INH
RR	RR
D6	D6
D5	D5
D4	D4
D	D

Id: 3/5



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