Practical 5: Digital Building Blocks – Arithmetic Logic Unit

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Part 1: ALU Design

In order to design the ALU a full operations table needs to be constructed. This will make the design process simpler and will allow for a step by step approach to be used. The operations table is as follows:

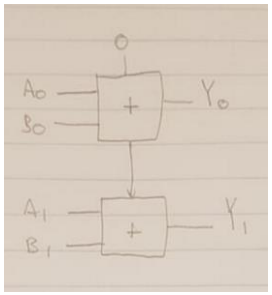
F2	F1	F0	Function	Logic unit required
0	0	0	A+B	Adder
0	0	1	A+!B+1	Adder
0	1	0	A+1	Adder
0	1	1	A+!1+1	Adder
1	0	0	A<<1	Mux
1	0	1	A>>1	Mux
1	1	0	A&B	And
1	1	1	A|B	Or

Each logical unit will be broken down and designed and hand drawn using block diagrams.

Adders:

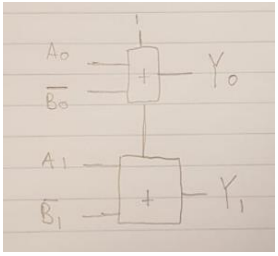
It is clear that an adder will be needed. Since A and B are 2 bit inputs this ALU requires at least two 1 bit adders. Adders for addition and subtraction will be required.

Addition Adder:



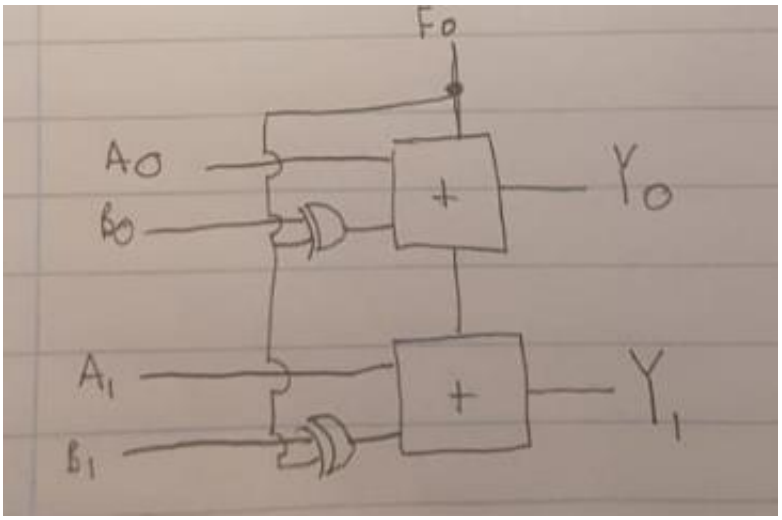
This simple 2 stage ripple adder uses the carry out pin of the first full bit adder to iterate the carry in pin of the second full bit adder, allowing for 2 bit addition.

Subtraction Adder:



By making use of twos-compliment to do subtraction (A-B = A +!B +1) a 2 bit subtraction adder can be created.

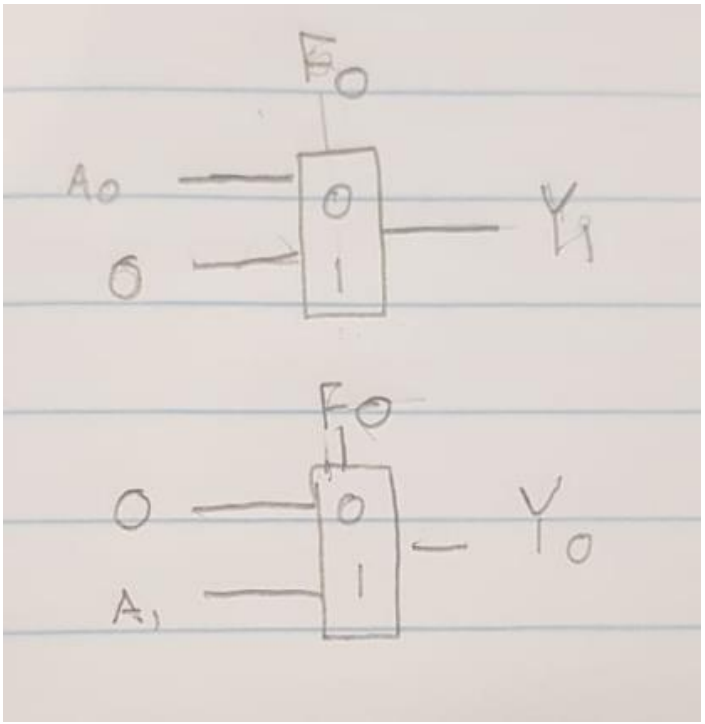
Joined Addition and Subtraction adder:



Since it is clear from the design table that F0 determines if subtraction or addition happens we can use it as a control signal as well as 2 exclusive or (XOR) gates to make a combined subtraction and addition adder. This same unit can be used to add/subtract 1 from A, the inputs can be controlled by a MUX. Therefor the adder section is complete.

Mux for shifting:

Multiplexors can be used to shift inputs and therefore perform multiplication and division by 2. This will be perfect for the multiplication and division functions. Since we are only shifting bits of A and from the design table it is clear that the shift direction is determined by F0, a simple combination of 2 multiplexors can be used:

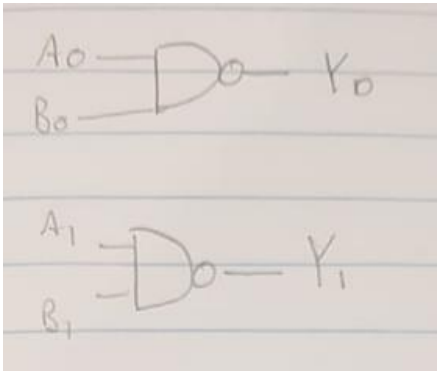


It is clear here that a 0 on F0 will implement a LEFT (multiplication) shift of A and a 1 on F0 will implement a RIGHT (devision) shift of A.

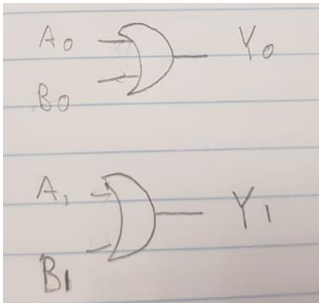
2 bit Bitwise AND and OR operations:

These operations can be made simply with a combination of AND and OR gates.

2 bit Bitwise AND:



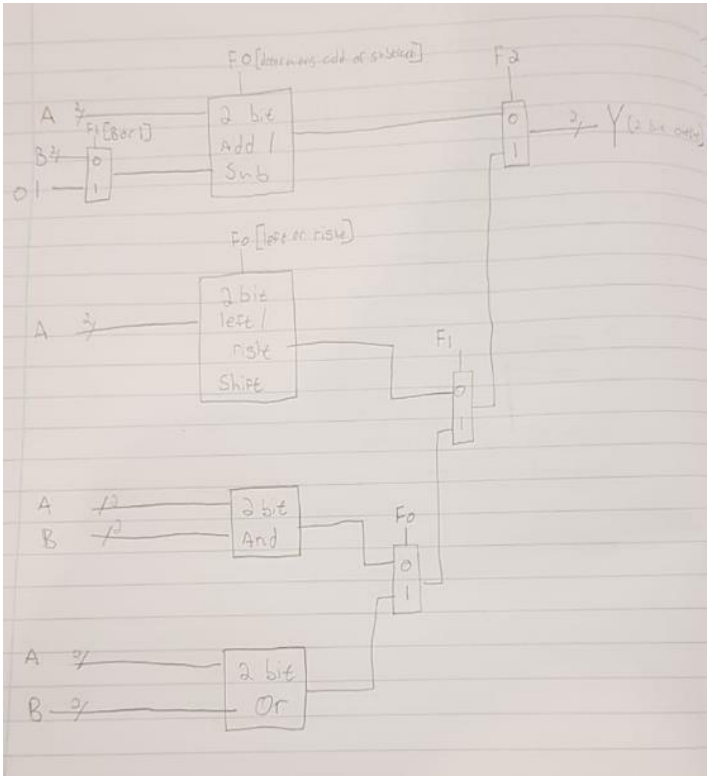
2 bit Bitwise OR:



Both of these are simple to create and their inputs will be determined by multiplexors.

Mux Control:

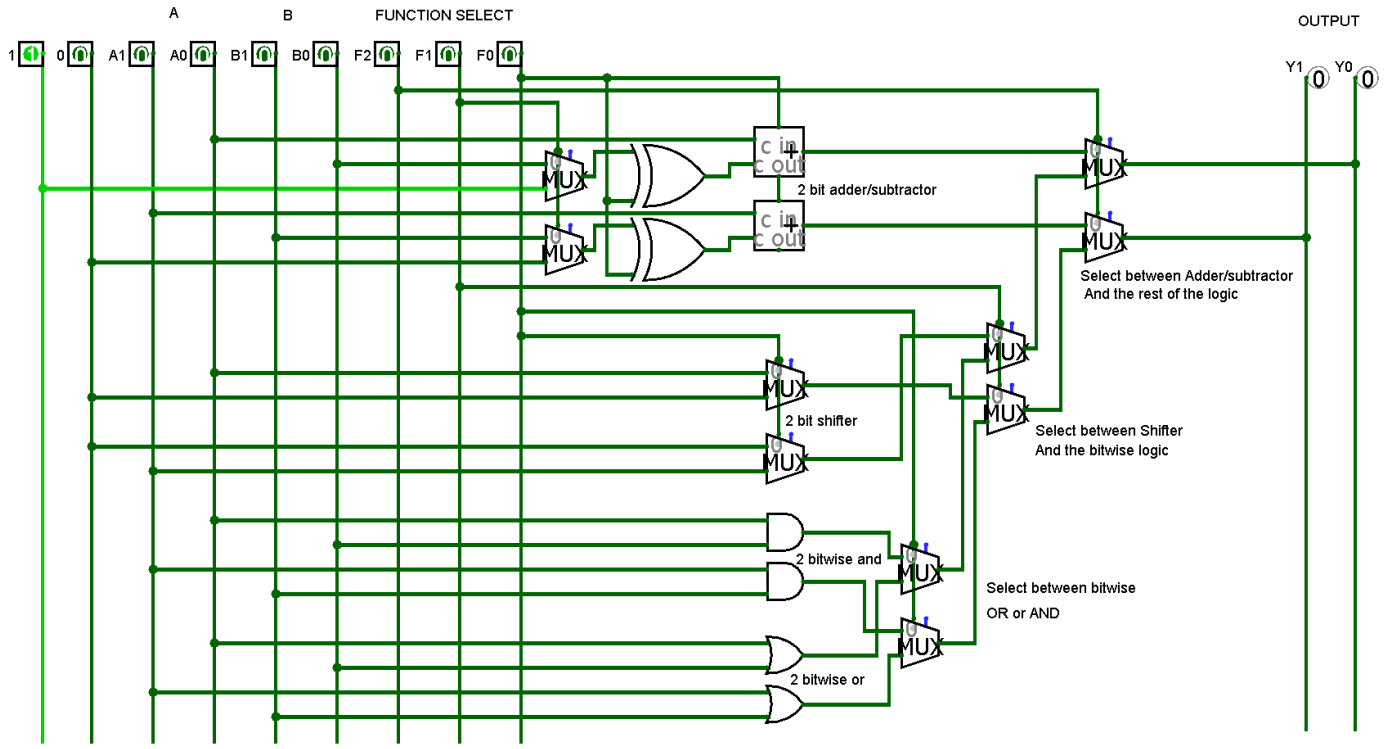
Now that the individual logic circuitry requirements are met, the control circuitry (Using Multiplexors) can be designed. This is once again designed using hand drawn block diagrams:



The circuit design is now complete and can be simulated in Logisim. Since only 1 bit circuitry is available, each block will have to be split into is individual design as shown earlier.

Logisim Simulation:

The circuit was built using the base mux control diagram and replacing the 2 bit blocks with their appropriate 1 bit logic devices as allowed by the prac outline.



Function select is done by changing F2, F1 and F0 and inputs are editable by changing A1, A0, B1 and B0. Outputs are Y1 and Y0. The ALU works as intended.