VREFBUF peripheral applications and trimming technique

Introduction

The applicable STM32xx devices (see Table 1) embed a very precise buffered reference voltage VREFBUF which can be used either as a voltage reference for internal peripherals like ADC, DAC or externally through the VREF+ pin.

The purpose of the VREFBUF peripheral is to provide an accurate reference voltage with limited changes over temperature, supply variations or product lifetime.

VREFBUF peripheral has several features like the output voltage reference scale selection, output voltage reference tuning/ trimming or output mode control in order to use an internal or external reference.

VREFBUF structure is based on low drop output regulator design with a compensation circuitry to optimize its accuracy within the application environment including the current load on VREF+.

Table 1. Applicable products

Type	Product Series/Lines(1)
Microcontrollers	STM32L4 Series
	STM32L4+ Series
	STM32L5 Series
	STM32WL Series
	STM32H7 Series
	STM32G0 Series
	STM32G4 Series
	STM32WBx5 Line
	STM32U5 Series
Microprocessors	STM32MP1 Series

1. *This application note applies only to products with:*
   - *presence of a VREFBUF peripheral*
   - *VREF+ ball/pin not internally connected to VDD nor VDDA.*

   Refer to product datasheet.

1 General information

This document applies to STM32 Arm®-based microprocessors and microcontrollers.

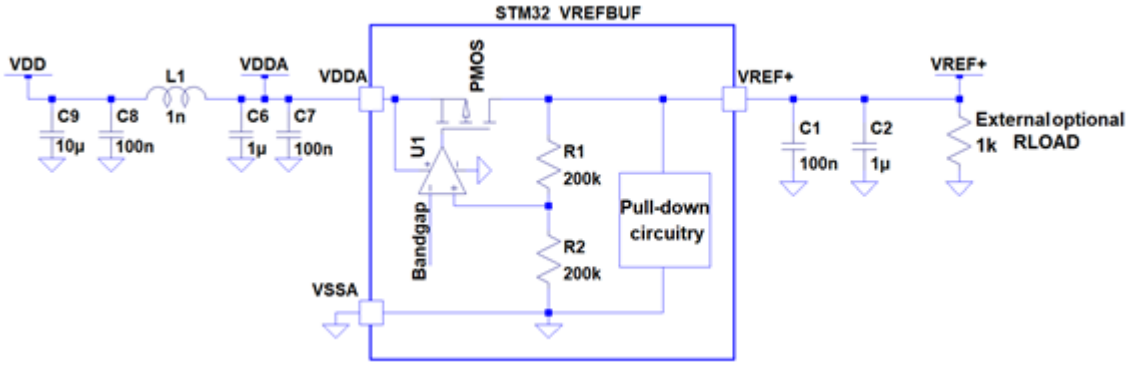
Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 VREFBUF peripheral principle

VREFBUF peripheral is a low drop output regulator powered by the analog supply VDDA. VREFBUF output is always connected to VREF+ pin and the associated external capacitors C1 and C2. VREFBUF output and VREF+ are always connected internally to DAC and ADC reference inputs. There are several output voltages scales available (depending on STM32 series) which can be fine adjusted by the application with the peripheral bit registers (some scales are calibrated/trimmed during factory test).

Note: The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 1. STM32 VREBUF peripheral simplified schematic



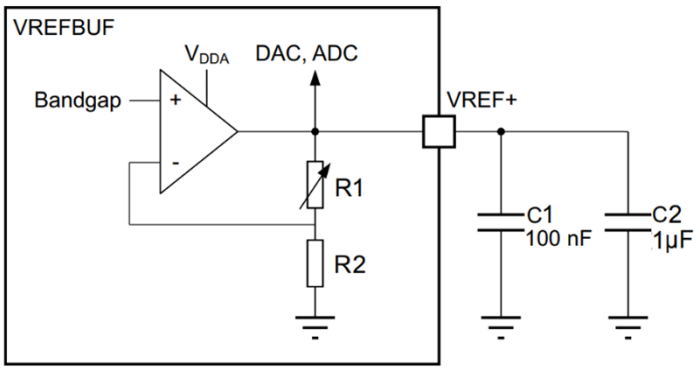
2.1 Principle and circuitry

The VREFBUF voltage regulator architecture is based on a regulation loop with an amplifier. The following figure introduces its simplified circuitry using a PMOS transistor. The output voltage regulation depends on the Bandgap voltage and R1/ R2 resistors through the following formula:

$$\text{VREFBUF output} = \text{Bandgap} \times \left(1 + \frac{R1}{R2}\right)$$

R1 resistor is variable to provide the following features: output scale selection and trimming.

Figure 2. VREFBUF peripheral simplified principle



For example: the VREFBUF STM32G4 product family supports three voltage scales: 2.048 V , 2.500 V and 2.900 V. The output voltage selection is performed changing the R1 resistor value. The selection of R1 value is performed with the VREFBUF register configuration. Considering VREFBUF bandgap voltage equal to 1.25 V, the following table shows the relationship between VREFBUF output voltage, Bandgap and R1/R2 resistors for the STM32G4 series.

Table 2. STM32G4 series VREFBUF output with R1 and R2 resistors example

VREFBUF output voltage on VREF+ pin	Bandgap	R1/R2 ratio	R1(kΩ) / R2(kΩ)
2.048 V	1.25 V	0.6384	127.68 / 200
2.500 V	1.25 V	1	200 / 200
2.900 V	1.25 V	1.32	264 / 200

2.2 Peripheral functional modes and status

The VREFBUF peripheral has several control bits registers available: ENVR, HIZ, VRS, and VRR and TRIM. The following paragraph describes the behavior change on the peripheral.

2.2.1 ENVR and HIZ bits

- ENVR bit: simply enable or disable the VREFBUF peripheral.
- HIZ bit: enable or disable the VREFBUF output high impedance.

The following table describes the VREFBUF peripheral behavior with ENVR/HIZ bits.

Table 3. VREFBUF peripheral behavior with ENVR/HIZ bits

ENVR	HIZ	Mode	Description
0	0	Pull-down	VREFBUF is disable, VREF+ pin is pulled down to VSSA.
	1	External voltage reference	VREFBUF is disable, VREF+ is input floating pin. An external reference voltage can be connected for analog peripherals usage.
1	0	VREFBUF voltage reference	VREFBUF is enable and buffering VREF+ pin with VREFBUF_OUT voltage.
	1	VREFBUF hold	VREFBUF is enable without output buffer. Voltage on VREF+ pin is hold with the external capacitor

2.2.2 VRS bits

- VRS bits: select the VREFBUF_OUT voltage reference scale.

The following table list the available VREFBUF output voltage scales per STM32 series. The VRS size depends on STM32 series.

Table 4. Example of VREFBUF output voltage per STM32 series

STM32 Series	VRS size (bits)	Available VREFBUF output voltage scale(1)					
		1.5 V	1.8 V	2.040 V / 2.048 V(2)	2.5 V	2.9 V	-
STM32L4	1	-	-	o	o	-	-
STM32L4+	1	-	-	o	o	-	-
STM32L5	1	-	-	o	o	-	-
STM32WB	1	-	-	o	o	-	-
STM32WL	1	-	-	o	o	-	-
STM32G0	1	-	-	o	o	-	-
STM32G4	2	-	-	o	o	o	-
STM32H7	3	o	o	o	o	-	-
STM32MP1	3	o	o	o	o	-	-
STM32U5	3	o	o	o	o	-	-

1. *O = available VREFBUF output voltage.*
2. *VREFBUF voltage selection is between 2.040V and 2.048V depends on STM32 series (refer to datasheet).*

Table 5. **STM32G4 series VREFBUF output voltage with VRS value**

STM32 series	VRS[1:0]	VREFBUF output voltage on VREF+ pin
STM32G4	00	2.048V
	01	2.500V
	10	2.900V

2.2.3 VRR

- VRR bit (voltage reference ready) is set when the VREFBUF output voltage accuracy is 1% from the selected voltage range. When HIZ bit is set, VRR is maintained at 1 and by consequence, application must ensure that VREFBUF_OUT voltage is always in its scale voltage limits.

2.2.4 TRIM

- TRIM bits control the VREFBUF adjustable trimming code.

3 VREFBUF constraints in application

The following sections describe application constraints when VREFBUF is used.

3.1 VREFBUF trimming circuitry

STM32 peripherals like ADC or OPAMP may embed a self-calibration circuitry but some others like internal oscillators or VREFBUF require a measured trimming performed during factory.

A specific parameter (output voltage for VREFBUF case) is adjusted by trimming, based on a register word value. VREFBUF output voltage is trimmed at factory level with different conditions depending on the STM32 series. The product datasheet provides trimming temperature and voltage range details.

In most cases the parameter variation is linear with the register word and the default value for centered parameter is the median code. Each trimming register step changes the trimmed parameter with a given resolution step. For example, the VREFBUF typical trimming step is ± 0.05% equivalent to 1.25 mV when VREFBUF output is 2.5 V (VRS = 1). If calibration operation is correctly performed the adjusted parameter fits in the half of the trimming step.

The VREFBUF trimming operation needs the following steps to be completed:

1. Set median code value in the TRIM register and measure the VREFBUF output.
2. Calculate the difference voltage with the target voltage and the trimming code steps to apply.
   a. Trim code to apply = median code – round nearest (ΔV / typical trim step voltage)
3. Apply the adjusted trimming code and measure again the VREFBUF output voltage to verify its accuracy after trimming.

The following table provides trimming operation steps examples.

Table 6. Trimming operation example for STM32G4 2.5 V VREFBUF output voltage

Example	Trimming step 1			Trimming step 2		Trimming step 3		Trimming results
	Initial trimming code	Initial Voltage (mV)	ΔV vs 2.5 V (mV)	Trimming step correction	Adjusted trimming code	Trimmed Voltage (mV)	Voltage Accuracy (mV)	Trimming code Accuracy
#1	32	2503.83	3.83	-3	29	2500.08	0.08	0.06
#2	32	2498.28	-1.72	1	33	2499.53	-0.47	-0.38
#3	32	2503.88	3.88	-3	29	2500.13	0.13	0.10
#4	32	2497.53	-2.47	2	34	2500.03	0.03	0.03
#5	32	2491.42	-8.58	7	39	2500.17	0.17	0.14
#6	32	2498.85	-1.15	1	33	2500.10	0.10	0.08

3.2 VREFBUF trimming with an external voltage and ADC

VREFBUF output can be trimmed with the ADC peripheral and an external accurate voltage source. When the VREFBUF is used as ADC reference, there is a proportional/linear factor between the ADC input voltage and the ADC digital output:

$$\text{Digital output} = \text{int}\left(\frac{\text{Vin} \times 2^N}{\text{VREF+}}\right) = \text{int}\left(\frac{\text{Vin} \times 2^{12}}{\text{VREF+}}\right) \text{ with VREF+ = VREFBUF and 12 bits ADC}$$

For example, applying 1.800 V at ADC input and getting 2961 LSB ADC digital output, we can obtains VREFBUF voltage calculation:

$$\text{VREFBUF} = \text{Vin} \times \frac{2^N}{\text{digital output}} = 1.800 \times \frac{4096}{2953} = 2.4967 \text{ V}$$

There is no trimming correction to apply, because the VREFBUF output is 3.3 mV below 2.5 V.

It is important to apply a high voltage input signal to minimize the ADC offset error, but ADC gain error should be also considered. The offset error can be cancelled and the VREFBUF estimation improved by performing the acquisition of 2 input voltages. The following table presents accuracy performances of this method using various input voltage configuration.

Table 5 STM32 ADC digital output code /VREFBUF estimation

Table 7. STM32 ADC digital output code /VREFBUF estimation

Method	Input voltage (V)	ADC condition	ADC digital output (LSB)	VREFBUF voltage estimation (V)	Estimation error (mV) (real VREFBUF = 2.051 V)
Single point	0.1	Theorical	200	2.048	3
	1.8		3595	2.0508	0.15
Two points	1.8 - 0.1 = 1.7		3595-200 = 3395	2.051	0.016
single point	0.1	ADC offset error=2 LSB ADC gain error 2.5 LSB	202	2.0277	23.3
	1.8		3599	2.0486	2.43
Two points	1.8 - 0.1 = 1.7		3599-202 = 3397	2.04981	1.2

In order to get the most accurate estimation of VREFBUF voltage via STM32 ADC digital output, one can use 2 input voltage points to minimize the ADC offset error and achieve a good VREFBUF voltage calculation result.

3.3 VREFBUF trimming with the internal VREFINT voltage and ADC

Another interesting method to improve the VREFBUF trimming is to use the VREFINT calibration (VREFINT_CAL) and the ADC peripheral. During the production process, VREFINT value is store in the product memory for a given reference (VREF+ = 3.0 V ± 10m V for STM32G4 series) and a given temperature (30 °C ± 5°C for STM32G4 series).

We can calculate the VREFBUF voltage value directly from the following procedure:

1. Retrieve the VREFINT conversion value result at VREFINT_CAL address:
   a. Conversion value is 0x067B or 1659 in decimal
   b. Equivalent voltage is 1659 × (3 V/2^{12}) = 1.2151 V with factory conditions (3 V and 30 °C)
2. Configure the 12-bit ADC peripheral and acquire the VREFINT voltage while VREFBUF is ADC reference.
3. Retrieve the VREFINT average conversion value:
   a. Average conversion value is 1989.2 (10 samples acquisition) 0x067B or 1659 in decimal
   b. Calculating VREFBUF voltage from the equation: 1989.2 × (VREFBUF/2^{12}) = 1.2151 V
   c. VREFBUF = (1.2151/1989.2) × 2^{12} = 2.5020 V

With this simple firmware operation, VREFBUF voltage could be simply retrieved using the ADC peripheral and the VREFINT calibrated input.

3.4 Minimum VDDA supply voltage

VREFBUF peripheral circuitry is based on low drop voltage regulator and requires margin voltage of few hundred of millivoltage with its supply (VDDA) and its output to operates normally. When the supply margin voltage is reduced, VREFBUF operates in degraded mode and its output follows VDDA supply with a voltage drop. The minimum voltage margin (indicated in the product datasheet) and depends on the temperature, silicon process and the output current load. The following table presents the degraded mode parameter for STM32G4 series when VREFBUF output is 2.5V and VDDA supply variation for maximum current load.

Table 8. VREFBUF degraded mode example

VREFBUF supply	VREFBUF OUTPUT (VRS = 1)	Operation mode
$1.65V \le V_{DDA} \le 2.8$ V	$\min(V_{DDA} - 250$ mV, 2.5 V)	Degraded
$V_{DDA} \ge 2.8$ V	2.5 V	Normal

3.5 VREFBUF output decreases when VRS changes

VREFBUF circuitry is designed to drive/source current only. If in application VREFBUF output voltage decrease with VRS change, it is important to proceed with the following operation order to obtain the correct and accurate output voltage:

- Disable VREFBUF with HIZ = 0 to discharge output voltage on VREF+ with VREFBUF VSSA pulldown.
- Configure the VRS register value.
- Enable the VREFBUF with HIZ = 1 and monitor VRR bit status when output reached the requested level.

4 VREFBUF application examples

The following chapter describes analog oriented application using the VREFBUF reference peripheral with analog-to-digital converter (ADC), digital-to-analog converter (DAC) or a resistor voltage divider.

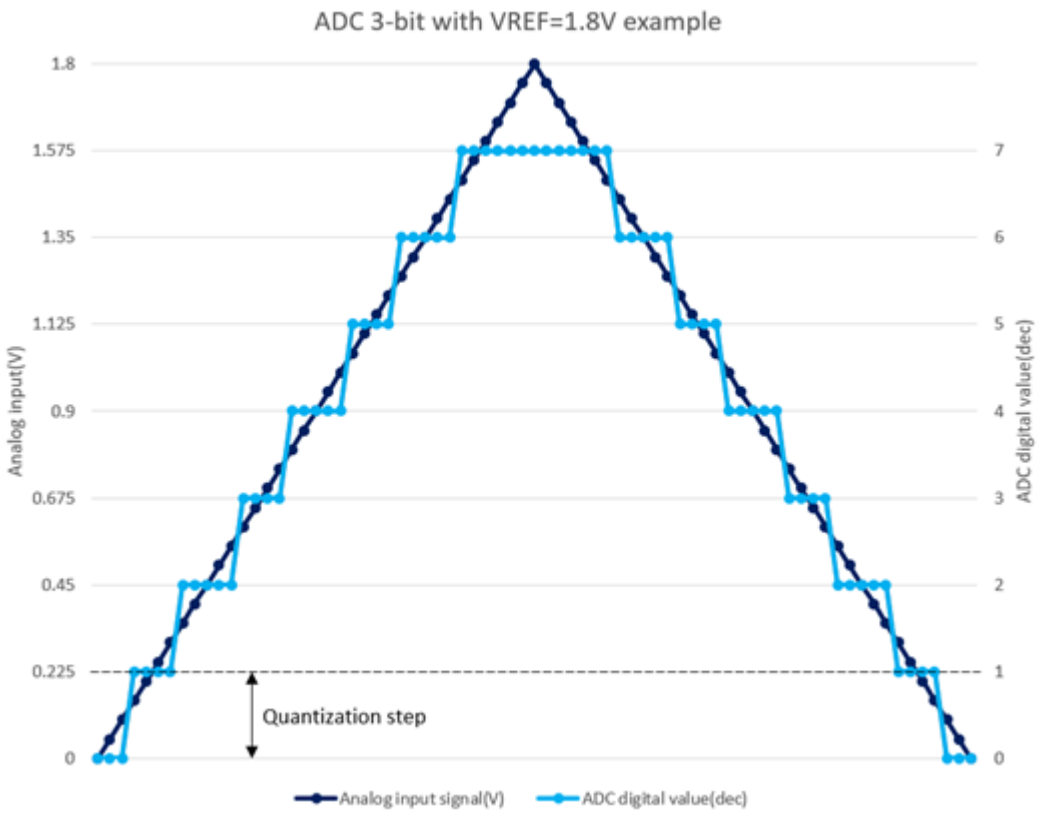
4.1 VREFBUF used as ADC reference for analog signal acquisition

Converting an analog signal to digital values with ADC requires an accurate analog reference voltage to define the quantization step amplitude: it is a key parameter of ADC. When the input signal voltage variation is above a multiple quantization step amplitude, the less significant bit of the digital value will be incremented.

Quantization step formula is $VREF/2^n$ where n is the number of bits of the ADC. For example, an ADC with 1.8V reference voltage and 16-bit resolution: quantization step = $1.8\ V/2^{16}$ = 27.466 µV.

The following figure shows this behavior for a 3-bit ADC, VREF=1.8 V and quantization step = 225 mV. Once the input voltage is greater than a multiple of quantization step, the digital value is increased and when input voltage is lower than a multiple of quantization step, the digital value is decreased.

Figure 3. ADC 3-bit quantization step example

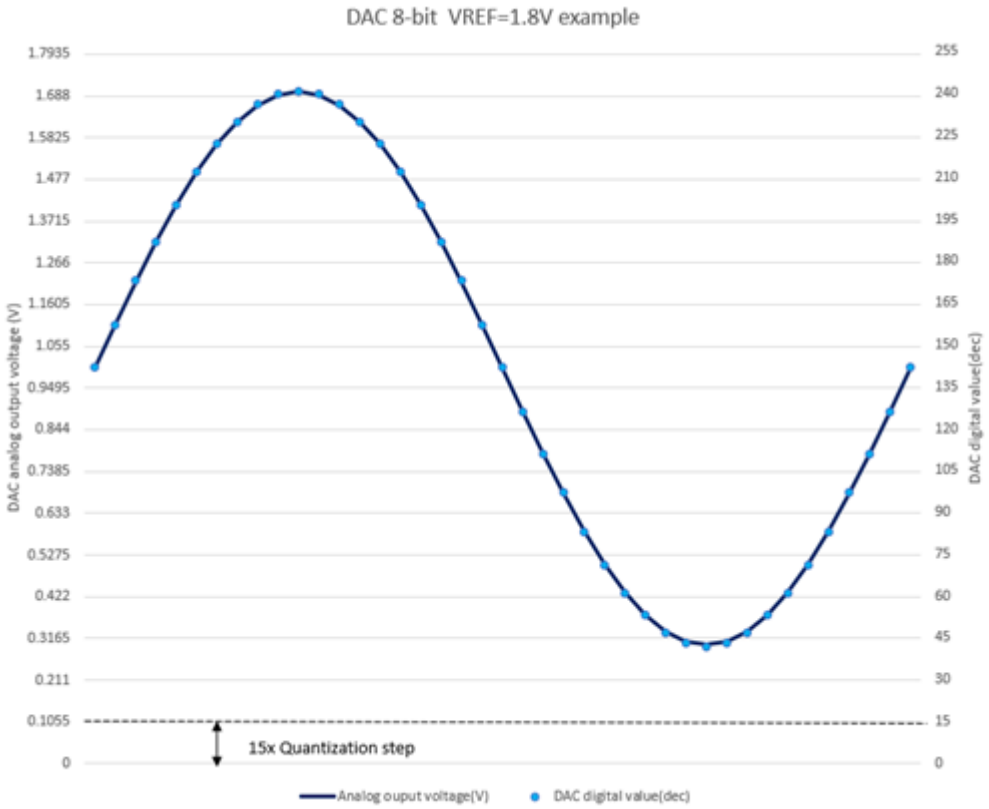


For this application case the ADC reference (VREF+ pin) is internally connected to the VREFBUF output and no external connection between pins is required. Only external capacitors on VREF+ pin are required.

4.2 VREFBUF used as DAC reference for signal generation application

The DAC peripheral enables to generate analog signal from digital values. As the ADC principle, a quantization step amplitude voltage ($VREF/2^n$ = 1.8 V/ 2^8 = 7.03 mV for 8-bit DAC) is required to convert a digital value to an output signal in the analog domain. The quantization step amplitude computed from the DAC reference voltage and the DAC bit resolution.

Figure 4. **DAC 8-bit quantization step example**



For this application case the DAC reference (VREF+ pin) is internally connected to the VREFBUF output and no external connection between pins is required.

4.3 VREFBUF used as voltage reference with a voltage divider

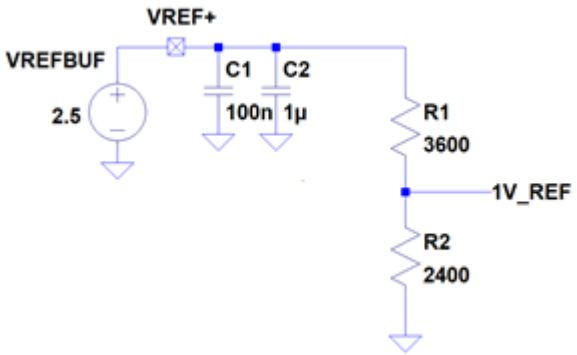
There are many other applications where the VREFBUF could be used thanks to its driving current capability (few mA). Other reference voltage values could be obtained using a voltage bridge divider connected to VREF+ pin.

The following schematic shows how to build 1 V reference voltage from VREFBUF/VREF+ pin.

A simple voltage divider circuitry with two resistors allows to obtain the desired 1 V reference voltage.

$$1\ V_{VREF} = 2.5 V_{VREFBUF} \times \frac{R2}{R1 + R2} = 2.5 \times \frac{2400}{3600 + 2400} = 2.5 \times \frac{2400}{6000} = 1\ V$$

Figure 5. **1 V reference voltage from VREFBUF divided**



The resistor bridge divider is loading the VREFBUF output and the maximum VREFBUF load capability should be respected. With this example, the static current load is 0.415 mA = 2.5 V / (3600 + 2400). In STM32G4 series datasheet, the maximum static load is 6 mA which is higher than the application load : circuitry choice is correct.

4.4 VREFBUF used as voltage reference with thermal sensor

Another VREFBUF application usage is relative to thermal sensor which could be found in batteries, computer main boards, heating/cooling system, etc. This temperature sensor circuit could simply be composed by voltage divider between a resistor and a negative–temperature–coefficient (NTC) thermistor. When the temperature is increasing, the NTC thermistor impedance is decreasing.

Figure 6. Example of a generic NTC thermistor impedance versus temperature

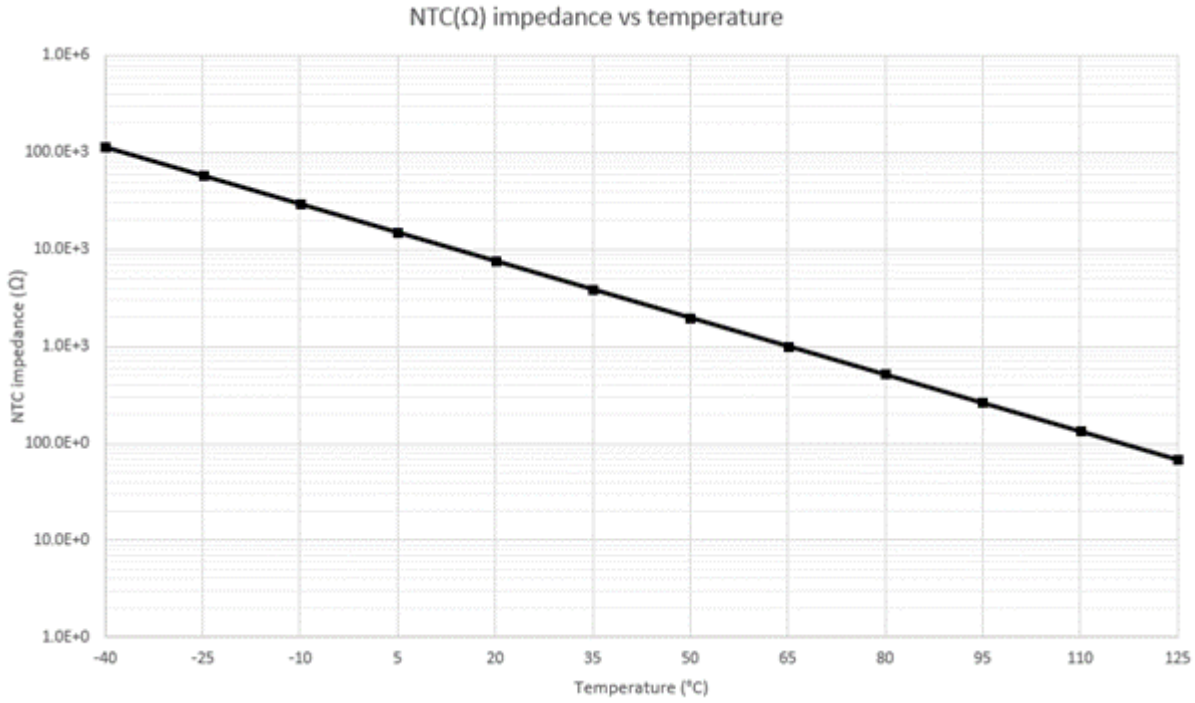
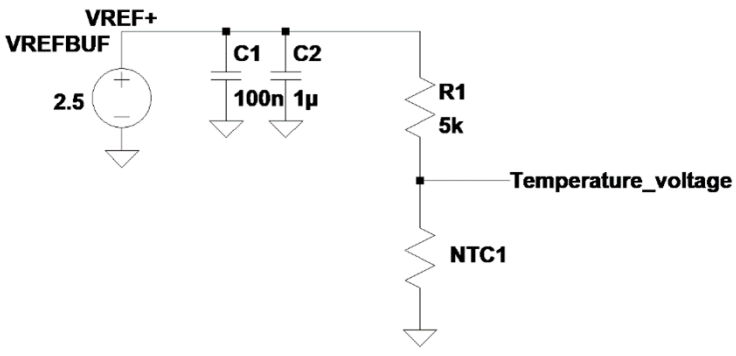


Figure 7. NTC thermistor voltage divider with VREFBUF peripheral



If we connect the Temperature_voltage signal to a STM32 12-bit ADC input, the following table represents the digitalized temperature characteristic values (ADC VREF is VREFBUF = 2.5 V).

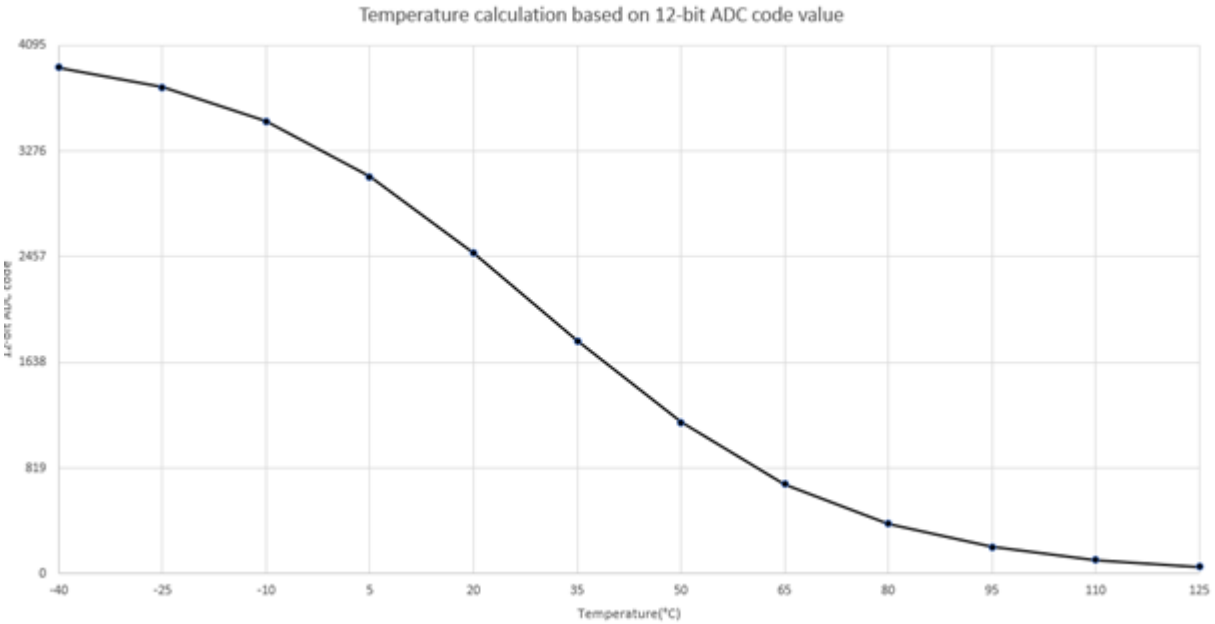
Table 9. Temperature / STM32 12-bit ADC code summary

T°C	NTC1(Ω)	R1(Ω)	Temperature voltage (mV)	STM32 12-bit ADC code
-40	114943.3	5000	2395.784	3925
-25	58524.1	5000	2303.224	3773
-10	29797.9	5000	2140.783	3507
5	15171.8	5000	1880.323	3080
20	7724.8	5000	1517.666	2486
35	3933.1	5000	1100.71	1803
50	2002.6	5000	714.9487	1171
65	1019.6	5000	423.4501	693
80	519.2	5000	235.179	385
95	264.3	5000	125.5153	205
110	134.6	5000	65.53578	107
125	68.5	5000	33.78712	55

We can estimate the actual temperature value from the ADC code with the help of a polynomial calculation.

$$T°C = C0 + C1 \times \mathrm{ADC}_{\mathrm{code}} + C2 \times \mathrm{ADC}_{\mathrm{code}}^{2} + C3 \times \mathrm{ADC}_{\mathrm{code}}^{3} + \ldots$$

Figure 8. Table results and estimation curve from ADC code with a polynomial interpolation



The previous interpolation curve is obtained with the following coefficients:

Table 10. Polynomial coefficients of the interpolation function

C0	C1	C2	C3	C4	C5
3277.1	-32.104	-0.3492	0.0024	4e-5	-2e-7

With those coefficients, the estimation function accuracy is ± 4 °C compared to the real temperature.

This temperature sensor application accuracy is relative to the VREFBUF peripheral stability over supply voltage, temperature and silicon process variation. To answer those constraints the peripheral has a specific regulator voltage architecture with a trimming feature.

Revision history

Table 11. **Document revision history**

Date	Version	Changes
24-Sep-2021	1	Initial release.
09-Dec-2021	2	Updated Table 1. Applicable products. Updated Table 4. Example of VREFBUF output voltage per STM32 series.

Contents

List of tables

List of figures