BeagleBone Al System Reference Manual

(BB AI Image)

BeagleBone Al

System Reference Manual (SRM)

THIS DOCUMENT



This work is licensed under a Creative Commons Attribution-ShareAlike

4.0 International License

All derivative works are to be attributed to Jason Kridner of BeagleBoard.org.

Supply comments and errors via https://github.com/beagleboard/beaglebone-ai/issues.

All information in this document is subject to change without notice.

For an up to date version of this document refer to:

https://github.com/beagleboard/beaglebone-ai/wiki/System-Reference-Manual

BeagleBone Al Design

REGULATORY AND COMPLIANCE INFORMATION

WARNINGS, RESTRICTIONS, AND DISCLAIMERS

WARRANTY

Table of Contents (insert here)

1.0 Introduction

Built on the proven BeagleBoard.org® open source Linux approach, BeagleBone® Al fills the gap between small SBCs and more powerful industrial computers. Based on the Texas Instruments AM5729, developers have access to the powerful SoC with the ease of BeagleBone® Black header and mechanical compatibility. BeagleBone® Al makes it easy to explore how artificial intelligence (Al) can be used in everyday life via TI C66x digital-signal-processor (DSP) cores and embedded-vision-engine (EVE) cores supported through an optimized TIDL machine learning OpenCL API with pre-installed tools. Focused on everyday automation in industrial, commercial and home applications.

2.0 Change History

2.1 Document Change History

2.2 Board changes

2.2.1 Rev A0

Initial prototype revision. Not taken to production.

2.2.2 Rev A1

Second round prototype.

- · Fixed size of mounting holes.
- · Added LED for WiFi status.
- · Added microHDMI.
- Changed eMMC voltage from 3.3V to 1.8V to support HS200.
- Changed eMMC from 4GB to 16GB.
- Changed serial debug header from 6-pin 100mil pitch to 3-pin 1.5mm pitch.

 Switched expansion header from UART4 to UART5. The UART4 pins were used for the microHDMI.

2.2.3 Rev A1a

Pilot run.

· Added pull-down resistor on serial debug header RX line.

2.2.4 Rev A2

Proposed changes.

- · Moved microSD card cage closer to microHDMI to fit cases better.
- Connected AM5729 ball AB10 to to P9.13 to provide a GPIO.
- · HDMI hot-plug detection fixes planned (TBD).

3.0 Connecting Up Your BeagleBone Al

- 3.1 What's In the Box
- 3.2 Main Connection Scenarios
- 3.3 Tethered to a PC
- 3.4 Standalone w/Display and Keyboard/Mouse

4.0 BeagleBone Al Overview

- 4.1 BeagleBone Compatibility (Do we want this?)
- 4.2 BeagleBone Al Features

Main Processor Features

- Dual 1.5GHz ARM® Cortex®-A15 with out-of-order speculative issue 3-way superscalar execution pipeline for the fastest execution of existing 32-bit code
- · 2 466x Floating-Point VLIW DSP supported by OpenCL
- 4 Embedded Vision Engines (EVEs) supported by TIDL machine learning library
- 2x Dual-Core Programmable Real-Time Unit (PRU) subsystems (4 PRUs total) for ultra low-latency control and software generated peripherals
- 2x Dual ARM® Cortex®-M4 co-processors for real-time control
- IVA-HD subsystem with support for 4K @ 15fps H.264 encode/decode and other codecs @ 1080p60

- Vivante® GC320 2D graphics accelerator
- Dual-Core PowerVR® SGX544™ 3D GPU

Communications

- BeagleBone Black header and mechanical compatibility
- 16-bit LCD interfaces
- 4+ UARTs
- 2 I2C ports
- · 2 SPI ports
- · Lots of PRU I/O pins

Memory

- 1GB RAM
- 16GB on-board eMMC flash

Connectors

- USB Type-C connector for power and SuperSpeed dual-role controller
- · Gigabit Ethernet
- 802.11ac 2.4/5GHz WiFi

Out of Box Software

· Zero-download out of box software environment

4.3 Board Component Locations

5.0 BeagleBone Al High Level Specification

Block Diagram
Processor
OSP
EVEs
PRUs
Graphics Accelerator
Memory
Power
Connectivity

6.0 Detailed Hardware Design

7.0 Connectors

7.1 Expansion Connectors

The expansion interface on the board is comprised of two 46 pin connectors. All signals on the expansion headers are **3.3V unless otherwise indicated.

**NOTE: Do not connect 5V logic level signals to these pins or the board will be damaged.

NOTE: DO NOT APPLY VOLTAGE TO ANY I/O PIN WHEN POWER IS NOT SUPPLIED TO THE BOARD. IT WILL DAMAGE THE PROCESSOR AND VOID THE WARRANTY.

NO PINS ARE TO BE DRIVEN UNTIL AFTER THE SYS_RESET LINE GOES HIGH.

Figure ? shows the location of the expansion connectors.

Insert Figure Here

The location and spacing of the expansion headers are the same as on the BeagleBone Black.

7.1.1 Connector P8

Table ? shows the pinout of the **P8** expansion header. Other signals can be connected to this connector based on setting the pin mux on the processor, but this is the default settings on power up. The SW is responsible for setting the default function of each pin. There are some signals that have not been listed here. Refer to the processor documentation for more information on these pins and detailed descriptions of all of the pins listed. In some cases there may not be enough signals to complete a group of signals that may be required to implement a total interface.

The **PROC** column is the pin number on the processor.

The PIN column is the pin number on the expansion header.

The **MODE** columns are the mode setting for each pin. Setting each mode to align with the mode column will give that function on that pin.

NOTE: DO NOT APPLY VOLTAGE TO ANY I/O PIN WHEN POWER IS NOT SUPPLIED TO THE BOARD. IT WILL DAMAGE THE PROCESSOR AND VOID THE WARRANTY.

NO PINS ARE TO BE DRIVEN UNTIL AFTER THE SYS_RESET LINE GOES HIGH.

Table ?. Expansion Header P8 Pinout

1 **GND** 2 **GND** 3 AB8 AB8 M/M/C3spia/T64/Cart10 ctsn vin2b de1 vin5a_ethanyoweofpu32tmpiator@expiritmpia2gpi1d0pigpo24 4 AB5 AB5 M/11/1/C3spi/att7/Assort10 rtsn vin2b clk1 vin5a exSAARCSpin2 PANANABXadaQqQ2gpinLaQpiqqbo215 5 AC9 AC9 M/M/C3s/Dia/T2As20rt5 ctsn vin2b d3 vin5a ed3EP3piadexiprarprode2gpia0piq7o6 6 AC3 AC3 M/M/C3s/Dia/TBAsart5 rtsn vin2b d2 vin5a ed2EP3ps2rorbiedr2xplxq0/2gpi7q0biq7bo2 7 G14 G14 TriMates Portricas printicas vin6a d9 timer11pr2_mip0r2rxplruptr2gpirl@pigpo56 F14 F14_Tith/blaspottecassportectesp7_fsr vin6a_d8 8 9 E17 E17_TxlkelE_Rclledtaspraca vin6a_clk0 timer14pr2_mipr2crsrupr2gpi6gpig6po68 A13 A13 TriMotes Station as pt/3 axr1 10 vin6a_d10 timer10or2 milon2rorrodk2gpit650ig6o45 AH4 AH4_QaiPhtQa3d71 vout3_vob0ut3_d16 eQEP2B_in pr1_pru001gpi400piq6o41 11 12 AG6 AG6 QiPMQ3d60 vout3 vootut3 d17 eQEP2A_in pr1_prup0r1gpi3g0pigq8o30 D3 D3_EH; FR12; W 16/11/20/B mdio_www.lk2_d13 kbd cel7rpwnp2B majoo1 npodaplk1 gpi7gpigso71 13 14 D5 D5 GP11024a 13812 rgmii1vbut2_d11 mii1_rkbltk_cel8AP2pin1_PNVVVIExpbruutr1gpi9qpjigepo93 uart10klooddroen06AP1pin1_Petrolof0 eerdintop1daetalioninidiatiaeno uto7 15 D1 GPIO4/in32a d2 vout2 edf21u12 АЗ vin2a d19 vin2b roll4nii1voxut2 d4 vin3a d11 mii1 txer ehrpwnp81 trippiatornexploppiutgpirt@pigeo26 B4 GP16024a 25921 vin2b rob2nii1voxxdd2 vdla23a vfld0a d13 16 B4 mii1 col pr1 mijor1rxbinkor1gpinkopiogo29 17 Α7 A7 GPb0081 18818 emu4 vin4a vdi23a od2s11 obs27 pr2 edipr2dætalipiia22antan0c2ontair160piop8o18 18 F5 F5 GP/16024a 9d8 vout2 edfn5i18 mii1_rkbl6_celQEP2pstrorbiidr1txpl6.prt1gpi5gpigeo9 19 F6 E6 EH/R128/VM2A vout2_edf14119 mii1_rkdd_cellerpwnp21A_miidr1txpl2upr1gpi6gpige060 20 AC4 AC4_M/M/C3s/D/M/D3clk vin2b d6 vin5a_ed6AP2pin2_PNVM22xptfq02gpi3q0pig6o30 AD4 AD4 MIMIC3 CILK vin2b d7 vin5a ed7rpwnp22trippiadratexplianp022tgpi200big6029 21 AD6 AD6 MMMC3sDAT54Jart10 txd vin2b d0 22 AC8 AC8 M/1/1/C3s/D/A/TAGEL/rt10 rxd vin2b d1 vin5a_ethrpwnp82A_miphr2rxpl8p02gpi80pbigpbo82 23 AC6 AC6 MHVHC3s Diantal art5 txd vin2b d4 vin5a edQEP3pr2nmipr2xpl0p02gpi50pigpo5

27	PIN	PRO	CNAMEMODE MOD					E190DE100DE1140DE120DE130DE14
26	25	AC7	AC7_M/M/c3spia00	Aucart5_rxd	vin2b_d5		vin5a	 <u>et3EP3ør2in</u> miør <u>2ix</u> prlu0/2gpi4@pig6o341
A8	26	ВЗ	B3_GP16224a_23820	vin2b_moonii1	<u>∨</u> oxdl2_vdl63a	_vde3a_d12	mii1_rxer	eCAP3pir1_PW/M/18xenutr1gpirt@pigoto28
28	27	E11					spi3_sclk	pr2_pr u r2g pit@<u>bi</u>g@o23
28		A8	vout1_d19	emu15/in4a	vol63a_od2s12	2obs28	•	pr2_edjor <u>2dætaljori23</u> æta <u>m02@</u> 61160pigopo19
29	28	D11					spi3_cs0	gpio4_19
A9		C9	vout1_d20	emu16/in4a	_vdi43a_ods4s13	3obs29		pr2_edjor <u>2dædajori2d</u> apta <u>n020p</u> 4rt@pig&o20
30 B10 CD_De_De_De_De_De_De_De_De_De_De_De_De_De	29	C11	LCD_l\subseteq 6\text{VtNiQhsyn}	c vin4a	√nisβa<u>c</u>0 isyn	c0	spi3_d0	gpio4_22
B9		A 9	vout1_d21	emu17vin4a	v d5 3a_ od5 s14	lobs30		pr2_edjor <u>2dædajori25</u> apta <u>n020p5i1660piog6o2</u> 18
C3	30	B10	LCD_ D &ut1_de	vin4a	_de8 a_de0		spi3_d1	gpio4_20
G16 mcasp4_axr8pi3_dtlart8_utlartM_rxd vout2_d18_vin4a_vin48a_d13 32 C7 LCD_DATA15i15 emu14vin4a_vin48a_utls1o_bs26 pr2_ecap0_ecap2_gamum2gapidspiigh00p00 D17 mcasp4_axrspi3_oss9rt8_utlartM_txd vout2_d19_vin4a_vin49a_d12 pr2_prupt2gpi011_gp00 33 C6 LCD_DATA15i13 emu12vin4a_vin3a_utls86 obs24 pr2_uart0_rxdpr2_prupt2gpi011_gp00 AF9 vin1a_vind0b_vsync1 vout3_uslkt7_txd timer15pi3_ddbd_rcavQEP1B_in gpi03_ 34 D8 LCD_DATA15i11 emu10vin4a_vin3a_utls66 obs22obs_dmarq2 pr2_uart0_cts.pm2_prupt2gpi3gpi0gb00 AF9 vin2a_vsync0 vin02_wsayta2etssys9c uart9_spi4_dbdd_rcavQEP1B_in gpi03_ AF9 vin1a_vide0b_hsyncxtout3_wtls1a_utls20 obs23 pr2_uart0_rts.pm2_prupt2gpi3gpi0gb00 AF9 vin1a_vide0b_hsyncxtout3_wtls1a_utls56 obs23 pr2_uart0_rts.pm2_prupt2gpi3gpi0gb00 AF9 vin1a_vide0b_hsyncxtout3_wtls1a_utls56 obs21obs_irq2 pr2_edio_sof_pr2_prupt2gpi3gpi0gb00 AF9 vin1a_vide0b_hsyncxtout3_wtls1a_utls56 obs21obs_irq2 pr2_edio_sof_pr2_prupt2gpi3gpi0gb00 AF9 vin1a_vide0b_hsyncxtout3_wtls1a_utls56 obs21obs_irq2 pr2_edio_sof_pr2_prupt2gpi3gpi0gb00 AF9 vin2a_d0 vout2_dtl8810 uart9_spish_d0bd_rcavApvmptB_uart01_rectipr1datatagpi0fdsta AF1 mcasp4c2sspspi8srdtlart8_i2xd4_scl vout2_d17 vin4a_wtls2a_d14 AF1 mcasp4c2sspspi8srdtlart8_i2xd4_scl vout2_d17 vin4a_wtls2a_d14 AF1 mcasp4c2sspspi8srdtlart8_i2xd4_scl vout2_d16 vin4a_wtln6a_d15 AF8 F8_LOQ_uDA_DAF7 emu9 vin4a_wtls2a_dtls2a_obs20 pr2_edc_latchpr2nprupt2gpi3gpi0gb00 AF9 LOD_DATABAH emu6 vin4a_wtls2a_dtls2a_obs20 obs16 AF9 F9_LOQ_uDA_DAF8 emu9 vin4a_vtls2a_dtls2a_obs20 obs16 AF0 F10_LOQ_uDA_DAF8 emu9 vin4a_vtls2a_dtls2a_obs20 obs16 AF1 LCD_DATABAH emu6 vin4a_vtls2a_dtls2a_obs10 obs17obs_dmarq1 pr1_uart0_txdpr2_prupt2gpi3gpi0gb00 AF1 LCD_DATABAH emu6 vin4a_vtls2a_dtls3a_dtls30 obs17obs_dmarq1 pr1_uart0_txdpr2_prupt2gpi3gpi0gb00 AF2 LCD_DATABAH emu6 vin4a_vtls2a_dtls3a_dtls30 obs17obs_dmarq1 pr1		В9	vout1_d22	emu18/in4a	vd163a_odb6s15	obs31		pr2_edjor <u>2dædajori266</u> pta <u>r002.og</u> 6i1 <u>69pi.og8o2</u> 2
2	31	C8	LCD_ DATA 14d14	emu13/in4a	<u>v</u> dn183a_odds19	obs25		pr2_uart0_txdpr2_pru0 <u>2g</u> prlu0 <u>pigo</u> 014
D17		G16	mcasp4_ax	r 9 pi3_d0art8_	www.rxd	vout2_d18	vin4a_ vdr18 a	_d13
See C.D. DATA Still Semula Still	32	C7	LCD_ DAJTA 1 <u>5</u> d15	emu14vin4a	vdn136a_odds510	obs26		pr2_ecap0_ec ap2_qaqqi0 n2 qapi1460piqqbo112
AF9		D17	mcasp4_ax	r s pi3_ as:0 rt8_	_wtamt4_txd	vout2_d19	vin4a_ vdn9 a	_d12 pr2_pr upt 2g pi@ 1_gpo0
D8 LCD_DATA11d11 emu10/in4a_vin18a_vist6 obs22obs_dmarq2 pr2_uart0_ctspr2_prup02gpi8qpigh0ip8o G6 vin2a_vsync0 vin2b_vssyn8c0stssyst9c uart9_spit4_ddod_resh8pvmptA_uapt0_resdjer1dataigpird4ta 35 A5 LCD_DATA11d112 emu11vin4a_vin18a_vist97 obs23 pr2_uart0_rtspr12_prup02gpi8qpigh0ip8o AD9 vin1a_vine0b_hsyncotout3_vist17a_vist97 rxd timer18pi3_sdtbid_resh0tEP1A_in gpio3_c F2 vin2a_d0 vout2_ext8010 uart9_spis4_ddod_resh4pvmptB_uapt0_resdjer1dataigpis64ta 37 E8 LCD_DATA18d8 uart6_vixd4a_vid63a_d8 pr2_edio_sof pr2_prup02gpi8qpigh0ip8ot A21 mcaspr4c_tsspr3pi8crtdart8_i2xd4_scl vout2_d17 vin4a_vin18a_d14 38 D9 LCD_DATA19d9 uart6_vixd4a_vid63a_d9 pr2_edio_latchpr2n_prup02gpi8qpigh0ip8ot C18 mcaspr4c_asplati_8clbutkt8_i2xd4_sda vout2_d16 vin4a_vin16a_d15 39 F8 F8_LCAD_DATA66 emu8 vin4a_vid63a_d23 obs20 pr2_edc_latchpr2n_prup02gpi8qpigh0ip8ot 40 E7 E7_LCAD_DATA66 emu8 vin4a_vid63a_d23 pr2_edc_syncpr2ouprup02gpi8qpigh0ip8ot 41 E9 E9_LCAD_DATA66 emu8 vin4a_vid63a_d23 obs20 pr2_edc_latchpr2n_prup02gpi8qpigh0ip8ot 42 F9 F9_LCAD_DATA66 emu6 vin4a_vid63a_d23 obs19 pr2_edc_latchpr2n_prup02gpi8qpigh0ip8ot 43 F10 F10_LCAD_IDAT665 emu7 vin4a_vid63a_d123 obs19 pr2_edc_latchpr2n_prup02gpi8qpigh0ip8ot 44 G11 G11_LCAD_IDAT642 emu2 vin4a_vid63a_d16 spi3_cs2 pr1_uart0_rxdpr2_prup02gpi8qpigh0ip8ot 45 F11 LCD_DATA600 uart5_vixd4a_vid63a_d0 46 G10 LCD_DATA611_d1 uart5_vixd4a_vid63a_d0 47 pr1_uart0_rts_pr2_prup02gpi8qpigh0ip8ot 48 G10 LCD_DATA611_d1 uart5_vixd4a_vid63a_d0 49 pr2_edio_sord2a_ts_ts_ts_ts_ts_ts_ts_ts_ts_ts_ts_ts_ts_	33	C6	LCD_ DATA 13d13	emu12/in4a	<u>v</u> dn13a_odds38	obs24		pr2_uart0_rxdpr2_pru0 0 2g pi1@pig&o13
G6		AF9	vin1a_ vfld0 b	_vsync1	vout3_ucalkt7	_txd time	1 5 pi3_d x bd_i	roeAQEP1B_in gpio3_1
A5 LCD_DATA12d12 emu11vin4a_vin12a_cits27 obs23 pr2_uart0_rts_pr2_prvp02gpi3vpjigsp0: AD9 vin1a_viae0b_hsyncxiout3_votr73_udert7_rxd timer16pi3_skdtld_rcev00EP1A_in gpi03_cits2 B7 LCD_DATA10d10 emu3 vin4a_vin10a_cits5 obs21obs_irq2 pr2_edio_sof pr2_prvp02gpi3vpjigsp0: B7 vin2a_d0 vout2_edia810 uart9_spi4a_d0bd_rcev04ypvrp01B_uart01_rccdjor1dataidgpi3d4ta B8 LCD_DATA8888 uart6_vird4a_vid63a_d8 pr2_edc_synctpr2vp02gpi3vpjigsp0: B8 LCD_DATA9989 uart6_vird4a_vid63a_d8 pr2_edc_synctpr2vp02gpi3vpjigsp0: B9 LCD_DATA9999 uart6_vird4a_vid83a_d9 pr2_edio_latchpr2vprvp02gpi3vpjigsp0: B8 B8 LCD_DATA9999 uart6_vird4a_vid83a_d9 pr2_edio_latchpr2vprvp02gpi3vpjigsp0: B9 B8 B8_LCDD_DATA986 emu8 vin4a_vid83a_d23 pr2_edc_latchpr2vprvp02gpi3vpjigsp0: B9 B9_LCDD_DATA986 emu8 vin4a_vid83a_d23 pr2_edc_latchpr2vprvp02gpi3vpjigsp0: B9 B9_LCDD_DATA985 emu7 vin4a_vid83a_d23 pr2_edc_latchpr2vprvp02gpi3vpjigsp0: B9 B9_LCDD_DATA985 emu7 vin4a_vid83a_d233 obs19 pr2_edc_latchpr2vprvp02gpi3vpjigsp0: B9 B9_LCDD_DATA985 emu7 vin4a_vid83a_dds0 obs16obs_irq1 pr1_uart0_rxdpr2_prvp02gpi3vpjigsp0: B1 LCD_DATA900 uart5_vird4a_vid18a_dds0 obs17obs_dmarq1 pr1_uart0_rxdpr2_prvp12gpi3vpjigsp0: B7 vout1_d16 uart7_vird4a_vid13a_d16 spi3_cs2 pr1_uart0_ctspr2_prvp12gpi3vpjigsp0: B7 vout1_d16 uart7_vird4a_vid13a_d17 pr1_uart0_rts_pr2_prvp12gpi3vpjigsp0:	34	D8	LCD_ DATA 1 <u>1</u> d11	emu10/in4a	_v dr13 a_ odds1 6	obs22obs_	dmarq2	pr2_uart0_cts_pm2_prundr <u>2g</u> pi& <u>npig</u> po81
AD9 vin1a_vde0b_hsynotout3_vdxt73_udert7_rxd timer16pi3_sddtd_rae00EP1A_in gpio3_0 D7 LCD_DATA10d10 emu3 vin4a_vdx055 obs21obs_irq2 pr2_edio_sof pr2_pru02gpi7g0_ig8o F2 vin2a_d0 vout2_ed20810 uart9_spis4_d0bd_rae0x4pwnpx1B_uapt01_raedig=1data4gijid5data BE LCD_DATA8_d8 uart6_vixd4a_vd63a_d8 pr2_edc_syncpr2_upru02gpi5g0_ig8o A21 mcaspr4cfaspcspi8srd4art8_if2cd4_scl vout2_d17 vin4a_vdx1a_d14 BD LCD_DATA9_d9 uart6_vixd4a_vd63a_d9 pr2_edio_latchpr2n_pru02gpi6g0_ig8o C18 mcaspr4casplaspi3eStadatrt8_if2cd4_sda vout2_d16 vin4a_vdx16a_d15 BF F8_LCIA0_uDATA966 emu8 vin4a_vd62a_od2s2 obs20 pr2_edc_latchpr2n_pru02gpi6g0_ig8o 40 E7 E7_LCIA0_uDATA966 emu8 vin4a_vd62a_od2s2 obs20 pr2_edc_latchpr2n_pru02gpi6g0_ig8o 41 E9 E9_LCIA0_uDATA944 emu6 vin4a_vd62a_od2s3 obs19 pr1_ecap0_ecap2_cappi4g0_ig8o 42 F9 F9_LCIA0_uDATA945 emu7 vin4a_vd62a_od2s3 obs19 pr2_edc_latchpr2n_pru02gpi6g0_ig8o 43 F10 F10_L6d0t_DATA94 emu6 vin4a_vd63a_od2s3 obs19 pr2_edc_latchpr2n_pru02gpi6g0_ig8o 44 G11 G11_L6d0t_DATA94 emu2 vin4a_vdr8a_ods80 obs16obs_irq1 pr1_uart0_rxdpr2_pru02gpi6g0_ig8o 45 F11 LCD_DATA90 uart5_vixd4a_vdr8a_ods91 obs17obs_dmarq1 pr1_uart0_txdpr2_pru02gpi6g0_ig8o 46 G10 LCD_DATA91_d1 uart5_vixd4a_vdr8a_d16a_d16 spi3_es2 pr1_uart0_ctspr2_pru02gpi6g0_ig8o 47 pr1_uart0_rtspr2_pru02gpi6g0_ig8o 48 pr2_edig=2data6igi6data6ig0_ig8o		G6	vin2a_vsyn	c0 vin2b	wasyt2celvssyu9	t uarts)_ sxpci 4_dk1od_ı	ræми8рwn p1fA_ ua pt01_resd<u>i</u>por1dæntakgpinie4et a0_out4
D7 LCD_DATA1010 emu3 vin4a_vin9a_ots65 obs21 obs_irq2 pr2_edio_sof pr2_prvt02gpi7gtpig9o F2 vin2a_d0 vout2_edf2810 uart9_spish_d0bd_rosh4pwnpt1B_uapt01_redipr1d_edipr1d_edipri04data F8 LCD_DATA8 d8 uart6_vind4a_vin83a_d8 pr2_edc_syncpr2ouprvt02gpi7gtpig9od A21 mcaspr4c_fesspr4pi8rdtart8_i2xct4_scl vout2_d17 vin4a_vin175a_d14 B9 LCD_DATA9 d9 uart6_vind4a_vin83a_d9 pr2_edio_latchpr2o_prvt02gpi7gtpig9od C18 mcaspr4c_astspi3c_featt8_i2xct4_sda vout2_d16 vin4a_vin16a_d15 F8 LCD_DATA9 d9 uart6_vind4a_vin83a_d29 pr2_edc_latchpr2o_prvt02gpi7gtpig9od E7 E7_LCD_DATA9 emu8 vin4a_vin83a_d23 pr2_edc_syncpr2o_uprvt02gpi7gtpig9od E7 E7_LCD_DATA9 emu9 vin4a_vin83a_d23 pr2_edc_syncpr2o_uprvt02gpi7gtpig9od E8 E9 LCD_DATA9 emu6 vin4a_vin83a_d23 obs19 pr2_edc_latchpr2o_prvt02gpi7gtpig9od E9 F9_LCD_DLATA9 emu2 vin4a_vin83a_ots23 obs19 pr2_edc_latchpr2o_prvt02gpi7gtpig9od E7 F10_LCD_DATA9 emu2 vin4a_vin8a_ots30 obs16obs_irq1 pr1_uart0_rxdpr2_prvt02gpi7gtpig9od E7 E10_LCD_DATA9 emu5 vin4a_vin8a_ots30 obs17 obs_dmarq1 pr1_uart0_rxdpr2_prvt02gpi7gtpig9od E7 vout1_d16 uart5_vind4a_vin8a_d16 spi3_cs2 pr1_uart0_ctspm2_prvt02gpi7gtpig9od E7 vout1_d16 uart5_vind4a_vin8a_d16 pr2_edipr2dedipri02dpirg9od E7 vout1_d16 uart5_vind4a_vin8a_d163a_d0 E7 vout1_d16 uart5_vind4a_vin8a_d163a_d0 E7 vout1_d16 uart5_vind4a_vin8a_d160a_d0 E7 vind4a_vin8	35	A5	LCD_ DAJTA 1 <u>2</u> d12	emu11vin4a	_vdn12a_odds27	obs23		pr2_uart0_rts_ pr 2_pr u0 2g pi9 0pi g6 092
F2 vin2a_d0 vout2_ed2810 uart9_spish_d0bd_reshMpwnpt1B_uapt01_resdipr1dætatgpiid4ta 37 E8 LCD_DATIN8_d8 uart6_vind4a_vid83a_d8 pr2_edc_syncpr2ouprvp02gpi6gpig60b A21 mcaspr4c2espspi8crd1art8_i2xc4_scl vout2_d17 vin4a_vid18a_d14 38 D9 LCD_DATIN9_d9 uart6_vind4a_vid83a_d9 pr2_edio_latchpr2o_prvp02gpi6gpig60b C18 mcaspr4caststepi3c4batkt8_i2xc4_sda vout2_d16 vin4a_vid16a_d15 39 F8 F8_LCVD_uD1AT066 emu8 vin4a_vid23a_vd234 obs20 pr2_edc_latchpr2o_prvp02gpi6gpig60b 40 E7 E7_LCVD_uD1AT067 emu9 vin4a_vid23a_vd23 41 E9 E9_LCVD_uD1AT067 emu9 vin4a_vid23a_vd23 42 F9 F9_LCVD_uD1AT065 emu7 vin4a_vid23a_vd23 obs18 pr1_ecap0_ecap2_cap2_vapvi02gpi6gpig60b 44 G11 G11_LCVD_tDATCA2 emu2 vin4a_vid23a_vd230 obs16 obs_irq1 pr1_uart0_rxdpr2_prvp12gpi6gpig60b 45 F11 LCD_DATCA3 emu5 vin4a_vid18a_vd180a_d16 spi3_cs2 pr1_uart0_ctspr2_prvp12gpi1gpig60b 46 G10 LCD_DATCA1_d1 uart5_vind4a_vid13a_d17 pr1_uart0_rtspr2_prvp12gpi1gpig60b		AD9	vin1a_ \de0 b	_hsyncvlout3	_v ob1.7 t3_u dee rt7_	_rxd time	1 6 pi3_s ktlkd _u	roe-QOEP1A_in gpio3_0
BE LCD_DATABAB uart6_virot4a_vid3a_d8 pr2_edc_syncpr2oupru02gpi60pig8od A21 mcaspr4cfaspspi8srdJart8_i2vd4_scl vout2_d17 vin4a_vid15a_d14 BD LCD_DATABAB uart6_virot4a_vid3a_d9 pr2_edio_latchpr2o_pru02gpi60pig8od C18 mcaspr4casptabiactat4t8_i2vd4_sda vout2_d16 vin4a_vid16a_d15 BF F8_LCV2outDAT666 emu8 vin4a_vid2a_dt234 obs20 pr2_edc_latchpr2o_pru02gpi60pig8od C1 E7 E7_LCV2outDAT647 emu9 vin4a_vid23a_dt23 pr2_edc_syncpr2oupru02gpi60pig8od C2 E9_LCV2outDAT644 emu6 vin4a_vid23a_dt23 pr1_ecap0_ecap2_garpi02gpi40pig8od C4 E9 F9_LCV2outDAT645 emu7 vin4a_vid23a_dt23 obs19 pr2_edc_latchpr2o_pru02gpi60pig8od C4 E7 E7_LCV2outDAT645 emu7 vin4a_vid23a_dt23 obs19 pr2_edc_latchpr2o_pru02gpi60pig8od C4 E7 E7_LCV2outDAT645 emu7 vin4a_vid23a_dt23 obs19 pr2_edc_latchpr2o_pru02gpi60pig8od C4 E7 E7_LCV2outDAT645 emu7 vin4a_vid23a_dt235 obs19 pr2_edc_latchpr2o_pru02gpi60pig8od C4 E7 E7_LCV2outDAT645 emu2 vin4a_vid23a_dt235 obs19 pr2_edc_latchpr2o_pru02gpi60pig8od C4 E7 E7_LCV2outDAT6455 emu7 vin4a_vid23a_dt255 obs18 pr1_uart0_rxdpr2_pru02gpi60pig8od C4 E7 E7_LCV2outDAT6455 emu8 vin4a_vid23a_dt255 obs18 pr1_uart0_rxdpr2_pru02gpi60pi60pi60pi60pi60pi60pi60pi60pi60pi60	36		LCD_ DA JTA11_0d10	emu3 vin4a	<u>v</u> dn103a_odds05	obs21obs_	irq2	pr2_edio_sof pr2_pru0 <u>12g</u> pi7 <u>00pig\$o</u> 70
A21 mcasprictaspspitsculart8_itacti_scl vout2_d17 vin4a_vint3a_d14 38 D9 LCD_DATM9_d9 uart6_viva4a_vint3a_d9 pr2_edio_latchpri2n_pru02gpitqpigpot C18 mcaspricaspspiacstuckt8_itacti_sda vout2_d16 vin4a_vint6a_d15 39 F8 F8_LCuto_DA_TM66 emu8 vin4a_vint3a_d23 vout2_d16 vin4a_vint6a_d15 40 E7 E7_LCvto_UDA_TM66 emu8 vin4a_vint3a_d23 vot224 obs20 pr2_edc_latchpr2n_pru02gpitqpigpot 41 E9 E9_LCvto_UDA_TM44 emu6 vin4a_vint3a_d23 42 F9 F9_LCvto_UDA_TM45 emu7 vin4a_vint3a_vint3a_vint3a_vint3a_vint3a_vint4a_vint3a_vint3a_vint4a_vint3a_vint3a_vint4a_vint3a_vint4a_vint3a_vint4a_vint3a_vint4a_vint3a_vint4a_vint3a_vint4a_vint3a_vint4a_vi		F2	vin2a_d0		vout2_edf281	0 uarts)_saptsi4h_dk0bd_i	roeMn4pwnpo11B_uapt01_roedpor1d.extalogomo54ta1_out5
D9 LCD_DATA9 d9 uart6_vivida_vil63a_d9 pr2_edio_latchpri2_pru02_gpi6gpig96d C18 mcasp4casp4spi3c3busht8_i2c4_sda vout2_d16 vin4a_vil6a_d15 39 F8 F8_LCV2_DAT666 emu8 vin4a_vil63a_d232 obs20 pr2_edc_latchpri2_pru02_gpi3gpig96d E7 E7_LCV2_DAT667 emu9 vin4a_vil63a_d23 pr2_edc_sync0r2_ubru02_gpi3gpig96d E8 E9_LCV2_DAT6644 emu6 vin4a_vil63a_d232 obs18 pr1_ecap0_ecap2_cappi02_gpi3gpig96d E9 F9_LCV2_DAT665 emu7 vin4a_vil63a_obs30 obs19 pr2_edc_latchpri2_pru02_gpi3gpig96d E7 F10_LCV2_DAT6A3 emu5 vin4a_vil63a_obs30 obs19 pr2_edc_latchpri2_pru02_gpi3gpig96d E7 E7_LCV2_DAT6A3 emu5 vin4a_vil63a_obs30 obs16obs_irq1 pr1_uart0_rxdpr2_pru02_gpi3gpig96d E7 Vout1_d16 uart5_vivida_vil63a_d16 spi3_cs2 pr1_uart0_tspr2_pru02_gpi3gpig96d E7 Vout1_d16 uart5_vivida_vil63a_d0 E7 LCD_DAT641_d1 uart5_vivida_vil63a_d17 pr1_uart0_rts_pr2_pru02_gpi3gpi3g96d	37	E8						pr2_edc_sync.pr2ouprun2gpi50pigpo5
C18 mcaspatcastadict8 i2cd4 sda vout2_d16 vin4a_vin6a_d15 39 F8 F8_LCV20_D1A_066 emu8 vin4a_vin2a_cut224 obs20 pr2_edc_latchpr2n_pru02gpi3gpig8od 40 E7 E7_LCV20_D1A_0677 emu9 vin4a_vin2a_cut222 obs18 pr1_ecap0_ecap2_carpin02gpi3gpig8od 41 E9 E9_LCV20_D1A_0644 emu6 vin4a_vin2a_cut223 obs18 pr1_ecap0_ecap2_carpin02gpi3gpig8od 42 F9 F9_LCV20_D1A_0655 emu7 vin4a_vin2a_cut233 obs19 pr2_edc_latchpr2n_pru02gpi3gpig8od 43 F10 F10_LCV20_tDA_0622 emu2 vin4a_vin1a_cut230 obs16obs_irq1 pr1_uart0_rxdpr2_pru02gpi3gpig8od 44 G11 G11_LCV20_tDA_0633 emu5 vin4a_vin19a_cut231 obs17obs_dmarq1 pr1_uart0_txdpr2_pru02gpi3gpig8od 45 F11 LCD_DA_063040 uart5_virc4a_vin16a_d16 spi3_cs2 pr1_uart0_ctspr2_pru02gpi3gpig8od 46 G10 LCD_DA_06411d1 uart5_virc4a_vin13a_d17 pr1_uart0_rts_pr2_pru012gpi3gpi3god 47 pr1_uart0_rts_pr2_pru012gpi3gpi3god 48 G10 LCD_DA_06411d1 uart5_virc4a_vin13a_d17			mcasp r 4 <u>c</u> tas			vout2_d17	vin4a_ vdn 3a	—
F8 F8_LCLQueDLA_T0466 emu8 vin4a_vil23a_otd234 obs20 pr2_edc_latchpr2n_pru022gpi3gpig804 E7 F7_LCLQueDLA_T0477 emu9 vin4a_vil23a_otd232 obs18 pr1_ecap0_ecap2_cappi3gpi3gpi3gp04 E9 F9_LCLQueDLA_T0455 emu6 vin4a_vil23a_otd232 obs18 pr1_ecap0_ecap2_cappi3gpi3gp04 E9 F9_LCLQueDLA_T0455 emu7 vin4a_vil23a_otd233 obs19 pr2_edc_latchpr2n_pru022gpi3gpi3gp04 E9 F9_LCLQueDLA_T0455 emu7 vin4a_vil23a_otd233 obs19 pr2_edc_latchpr2n_pru022gpi3gpi3gp04 E7 F10_LCQD_TD_AT0242 emu2 vin4a_vil18a_otd330 obs16obs_irq1 pr1_uart0_rxdpr2_pru022gpi3gpi3gp04 E7 F11_LCCD_DA_T0400 uart5_virxd4a_vil19a_otd391 obs17obs_dmarq1 pr1_uart0_txdpr2_pru022gpi3gpi3gp04 E7 F11_LCD_DA_T0400 uart5_virxd4a_vil18a_d16 spi3_cs2 pr1_uart0_ctspm2_pru022gpi3gpi3gp04 E7 F11_uart0_txdpr2_pru022gpi3gp0400 E7 F11_uart0_txdpr2_pru022gpi3gpi3gp0400 E7 F11_uart0_ttspm2_pru022gpi3gp040000 E7 F11_uart0_ttspm2_pru022gpi3gp0400000000000000000000000000000000000	38		LCD_ DATA 9_d9	uart6_wtxxx4a	_vdi9 3a_d9			pr2_edio_latch <u>pr2h_</u> pru <u>n02gpi@pig\$o</u> \$
F7 E7_LG/DutDAT647 emu9 vin4a_vila3a_d23 pr2_edc_syncpr2ouptru02gpi4gpigpoc4 E9 E9_LG/DutDAT644 emu6 vin4a_vila3a_vila32 obs18 pr1_ecap0_ecap2_gamin02api4gpigpoc4 E9 F9_LG/DutDAT645 emu7 vin4a_vila3a_vila33 obs19 pr2_edc_latchpr2npru02gpi2gpigpoc4 E7 F10_LQ/DutDAT645 emu7 vin4a_vila3a_vila30 obs19 pr2_edc_latchpr2npru02gpi2gpigpoc4 E7 F11 LCD_DAT640 uart5_viru4a_vila9a_vila91 obs17 obs_dmarq1 pr1_uart0_rxdpr2_pru02gpi0gpi0gpi0gpoc4 E7 F11 LCD_DAT640 uart5_viru4a_vila9a_vila91 obs17 obs_dmarq1 pr1_uart0_txdpr2_pru02gpi0gpi0gpoc4 E7 Vout1_d16 uart7_viru4a_vila3a_d0 E7 Vout1_d16 uart7_viru4a_vila3a_d0 E7 LCD_DAT6411d1 uart5_viru4a_vila3a_d17 pr1_uart0_rts_pr2_pru012gpi1gpi0gpoc4 E7 F11 LCD_DAT6411d1 uart5_viru4a_vila3a_d17		C18	mcas p4i<u>c</u>as			_	vin4a_ vdn6 a	_d15
F9 F9_LQQQ_DQATA4 emu6 vin4a_vid23a_vd233 obs19 pr1_ecap0_ecap2_qarpinQapridqbiqqbc4 F9 F9_LQQQ_DATA5 emu7 vin4a_vid23a_vd233 obs19 pr2_edc_latchpr2npru02gpi2qbiqqbc4 F10 F10_LQQQ_DATA2 emu2 vin4a_vid18a_vd230 obs16obs_irq1 pr1_uart0_rxdpr2_pru02gpi2qbiqqbc4 G11 G11_LQQQ_DATA3 emu5 vin4a_vid19a_vd231 obs17obs_dmarq1 pr1_uart0_txdpr2_pru02gpi0qbiqqbc4 F11 LCD_DATA0_d0 uart5_vixd4a_vid16a_d16 spi3_cs2 pr1_uart0_cts_pr2_pru02gpi1qbiqqbc4 F12 vout1_d16 uart7_vixd4a_vid13a_d0 F13 LCD_DATA1_d1 uart5_vixd4a_vid13a_d17 pr1_uart0_rts_pr2_pru012gpi1qbiqqbc4 F14 G15 LCD_DATA1_d1 uart5_vixd4a_vid13a_d17	39	F8		emu8 vin4a	_v d232 a_od2324	obs20		pr2_edc_latchø <u>r2n</u> pru@2g p i@ <u>pi@</u> 6
F9 F9_LCADutDAT0855 emu7 vin4a_vid3a_cot283 obs19 pr2_edc_latch@r2n_prw02gpi2wpicg8cd F10 F10_LCaDutDAT0822 emu2 vin4a_vid18a_cot280 obs16obs_irq1 pr1_uart0_rxdpr2_prw02gpi2wpicg8cd F11 G11_LCaDutD_et083 emu5 vin4a_vid19a_cot291 obs17obs_dmarq1 pr1_uart0_txdpr2_prw02gpi2wpicg8cd F11 LCD_DAT08000 uart5_vixc4a_vid18a_d16 spi3_cs2 pr1_uart0_ctspm2_prw02gpi1wpicg8cd F11 vout1_d16 uart7_vixc4a_vid13a_d0 F12 edipr2dexidioi3dexid	40	E7	E7_LGAD <u>u</u> tJATAY7	emu9 vin4a	_v d23 a_d23			pr2_edc_sync pr2 ouprum2gpi4 <u>mpig</u> po7
43 F10 F10_L@Dit_DATEA2 emu2 vin4a_vin18a_orbis0 obs16obs_irq1 pr1_uart0_rxdpr2_prupt2gpi@pigsoc 44 G11 G11_L@Dit_DATEA3 emu5 vin4a_vin19a_orbis91 obs17obs_dmarq1 pr1_uart0_txdpr2_prupt2gpi@pigsoc 45 F11 LCD_DATEA0_d0 uart5_vixd4a_vin16a_d16 spi3_cs2 pr1_uart0_ctspm2_prupt2gpinl@pigsoc 46 G10 LCD_DATEA1_d1 uart5_vixd4a_vin13a_d17 pr1_uart0_rts_pm2_prupt2gpinl@pigsoc 47 pr1_uart0_rxdpr2_prupt2gpinl@pigsoc 48 pr2_edipr2dataipinl@diplataipinl@pigsoc 49 pr1_uart0_rts_pm2_prupt2gpinl@pigsoc 40 pr1_uart0_rts_pm2_prupt2gpinl@pigsoc 40 pr1_uart0_rts_pm2_prupt2gpinl@pigsoc		E9	E9_LG/10 <u>u</u> t/1 <u>A</u> 70/44	emu6 vin4a	_vd12832a_od12832	obs18		pr1_ecap0_ec ap2_qaqqii0<u>2</u>apid_qqbigqbo 4
44 G11 G11_L020Lt1DATBA3 emu5 vin4a_vdi19a_otds91 obs17obs_dmarq1 pr1_uart0_txdpr2_pru02gpi00pi09otd 45 F11 LCD_DATB40_d0 uart5_vind4a_vdi18a_d16 spi3_cs2 pr1_uart0_cts_pm2_pru012gpi10pi09otd 46 G10 LCD_DATB41_d1 uart5_vind4a_vdi13a_d17 pr1_uart0_rts_pm2_pru012gpi10pi09otd 47 pr1_uart0_rts_pm2_pru012gpi10pi09otd 48 pr1_uart0_rts_pm2_pru012gpi10pi09otd 49 pr1_uart0_rts_pm2_pru012gpi10pi09otd	42	F9	F9_LO.10 <u>u</u> 101A_10455	emu7 vin4a	_v d23 a_ od23 3	obs19		pr2_edc_latch p r <u>2n</u> pr u0 2g pi 2g0pi 2g0
45 F11 LCD_DATA10d0 uart5_vint4a_vdn8a_d16 spi3_cs2 pr1_uart0_cts_pm2_prupt2gpi146pig6pct B7 vout1_d16 uart7_vint4a_vdn3a_d0 pr2_edjpr2dæddjpi146pig6pct 46 G10 LCD_DATA1_d1 uart5_vint4a_vdn3a_d17 pr1_uart0_rts_pm2_prupt2gpi146pig6pct	43	F10		-		_	•	pr1_uart0_rxdpr2_prupr <u>2g</u> pi2 <u>ofpig</u> po20
B7 vout1_d16 uart7_vird4a_vil03a_d0 pr2_edipr2datdipi120tptaqu02d001400pig0s0 46 G10 LCD_DATA1_d1 uart5_vird4a_vil13a_d17 pr1_uart0_rts_pr12_prupt2gpi149pig0s0				-		obs17obs_	•	pr1_uart0_txdpr2_pr ო <u>2gpi0ტი</u> ტიტ
46 G10 LCD_DATA1_d1 uart5_txit4a_vdn3a_d17 pr1_uart0_rts_pr2_prupt2gpit6pig6po	45						spi3_cs2	pr1_uart0_cts_pn2_prupr <u>2g</u> pru@pigo_08
			-					pr2_edjor <u>2dætaljoi20</u> pta <u>n020</u> p10 <u>00jojo</u> 0
A10 vout1_d23 emu19/in4a_vdii/3a_d7 spi3_cs3 pr2_edjor2dætaljori2dfætaljori2d	46							pr1_uart0_rts_pr2_prupr2gpi1@pig8o19
		A10	vout1_d23	emu19/in4a	_v d i7/3a_d7		spi3_cs3	pr2_edj <u>or2dædajoil2d</u> æda <u>n020</u> djoil2d0bilgopo23

Notes regarding the resistors on muxed pins.

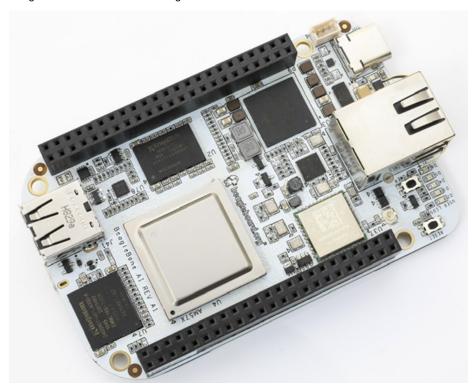
7.1.2 Connector P9

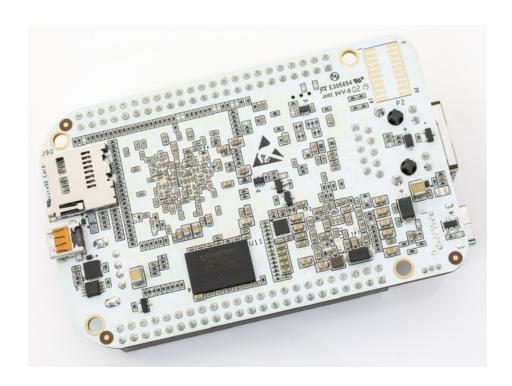
8.0 Cape Board Support

9.0 BeagleBone Al Mechanical

10.0 Pictures

BeagleBone Al Back of Board Image





11.0 Support Information