

## Planning

Use DAC  
DAC Output  
→ RA2 } DAC1  
→ RE7 }

don't use because we don't want to use the programming/debugging lines

• outputs unbuffered and it's simply the series combination of the resistors in ladder.

•  $R = 20k$  each

$$256 \times 20k > 5M\Omega$$

$i = 0$  ; any load  $[i_{load}]$  will impact significantly DAC output.

↓  
pull out LED that's connected to RA2 and plug a scope probe in to RA2 to monitor the output signal

↓  
Do not use a speaker connected onto breadboard (BULB 313 hands on)

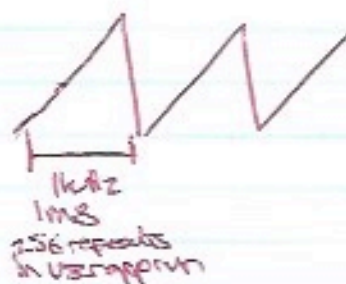
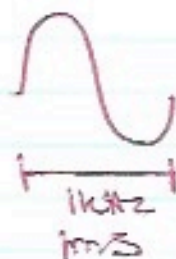
### Characteristics

DAC enabled, RA2 output, VDD positive reference, VSS as negative reference

DAC<sub>1</sub> CON = 0b10100000000000000000000000000000  
↓     ↓     ↓     ↓     ↓     ↓     ↓     ↓     ↓     ↓     ↓     ↓     ↓     ↓  
DAC    Data    VDD    Data    VSS    Data    VDD    Data    VSS    Data    VDD    Data    VSS    Data    VSS  
enabled    bits    DAC output is    bits    VSS    bits    VSS    bits    VSS    bits    VSS    bits    VSS    bits    VSS  
enabled on pin RA2 only

DAC<sub>4</sub> CON = 0x40;

### System Test Time



$$\frac{1 \times 10^{-3} \text{ s}}{256} = 3.90625 \mu\text{s} = 4 \mu\text{s}$$

actual frequency = 976.5628 kHz