Shift-and-Add Multiplication ASM

- Note the concatenation notation
- From the ASM we can write out the RT description of the system in terms of:
  - System state
  - Input signals
- The table on the following slide allows us to deduce the design of each register:

Control and Sequencing

- Two distinct aspects in control unit design
  - Control of micro-operations
  - Sequencing
- We separate the two aspects by providing:
  - A state table
    - Defines signals in terms of states and inputs
  - A simplified ASM chart
    - Represents only state transitions

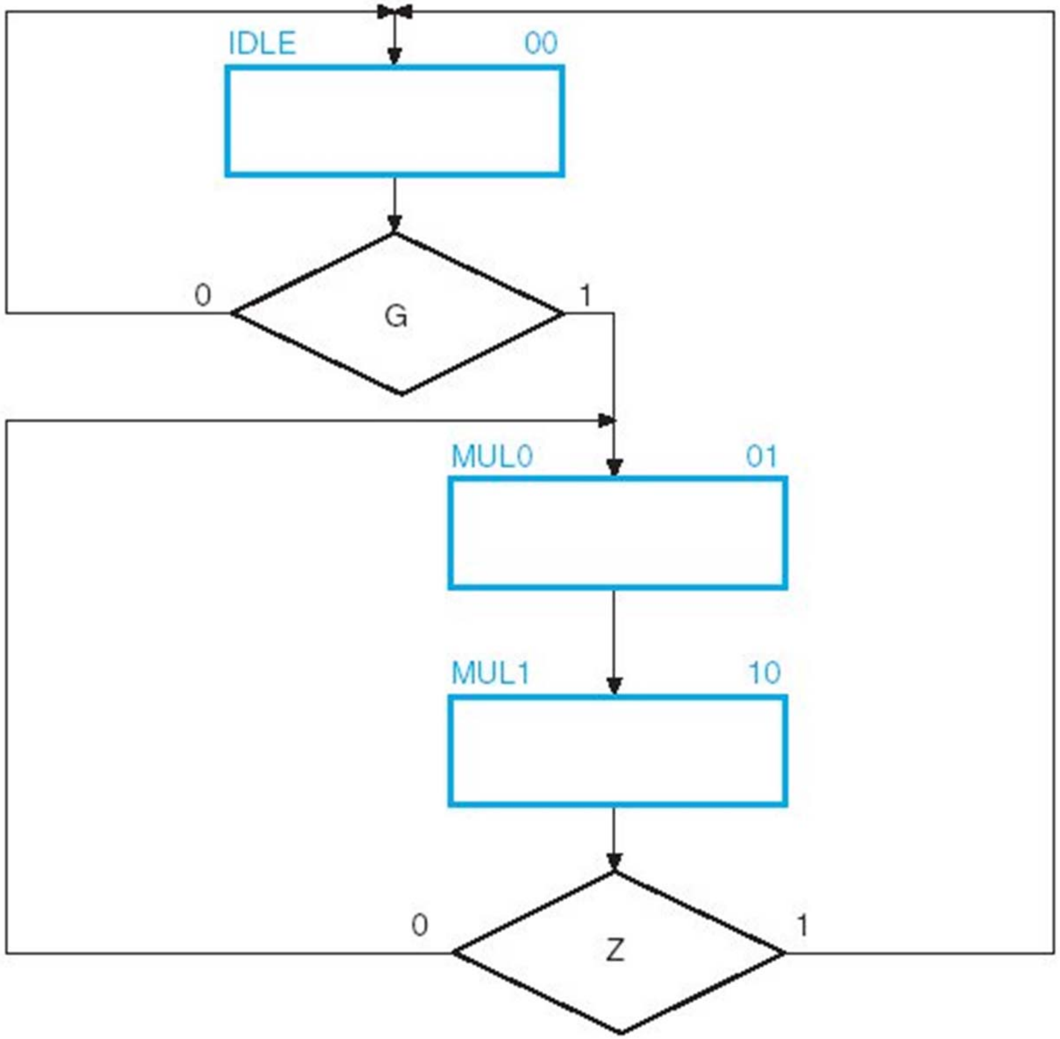
Register Transfers

- From the ASM we can write out the RT description of the system in terms of:
  - System state
  - Input signals
- By gathering together the RTs loading each register we may easily deduce the design of each register.

Control Signals for Binary Multiplier

Block Diagram Module	Microoperation	Control Signal Name	Control Expression
Register A:	$A \leftarrow 0$	Initialize	$\mathrm{IDLE} \cdot G$
	$A \leftarrow A + B$	Load	$\mathrm{MUL0} \cdot Q_0$
	$C \| A \| Q \leftarrow \text{sr } C \| A \| Q$	Shift_dec	MUL1
Register B:	$B \leftarrow IN$	Load_B	LOADB
Flip-Flop C:	$C \leftarrow 0$	Clear_C	$\mathrm{IDLE} \cdot G + \mathrm{MUL1}$
	$C \leftarrow C_{out}$	Load	—
Register Q:	$Q \leftarrow IN$	Load_Q	LOADQ
	$C \| A \| Q \leftarrow \text{sr } C \| A \| Q$	Shift_dec	—
Counter P:	$P \leftarrow n - 1$	Initialize	—
	$P \leftarrow P - 1$	Shift_dec	—

Sequencing Part of ASM Chart



Sequence Register and Decoder

- This method uses:
  - Sequence Register:
    - That holds control states
    - Register with n flop-flops has 2^n states
  - Decoder
    - Provides output signal for each state.
    - An n-to-2^n decoder has 2^n outputs

State Table

- Derived from the Sequencing Part of ASM Chart
  - $D_{M0} = IDLE \cdot G + MUL1 \cdot \overline{Z}$
  - $D_{M1} = MUL0$

Present state			Inputs		Next state		Decoder Outputs		
Name	M_1	M_0	G	Z	M_1	M_0	IDLE	MUL0	MUL1
IDLE	0	0	0	×	0	0	1	0	0
	0	0	1	×	0	1	1	0	0
MUL0	0	1	×	×	1	0	0	1	0
MUL1	1	0	×	0	0	1	0	0	1
	1	0	×	1	0	0	0	0	1
—	1	1	×	×	×	×	×	×	×

Control Unit for Binary Multiplier