



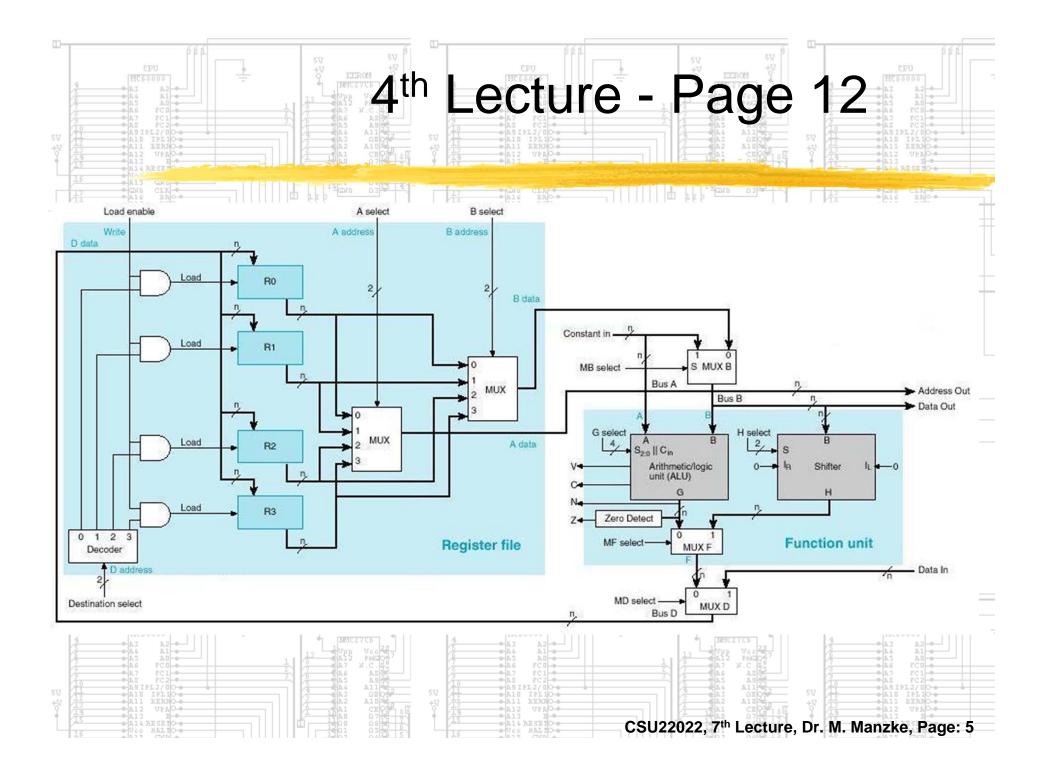
If multiple shifts are required we wire them into multiplexers that have an input for every bit on the bus to obtain a Barrel shifter (Previous slide).

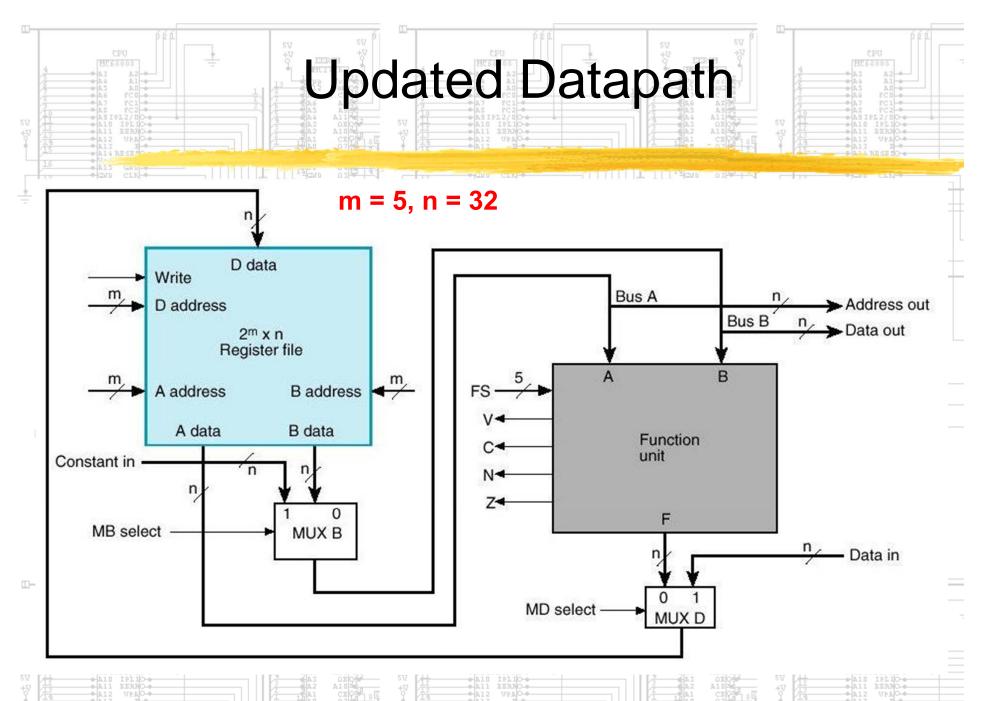
$S_1 S_2$	$Y_3 Y_2 Y_1 Y_0$	Micro-ops	
0 0	$D_3 D_2 D_1 D_0$	No Rotate	
0 1 counter 5'	D_2 D_1 D_0 D_3	Rotate One	
1 0 1 1 1 1 1 1 1 1 1	D_1 D_0 D_3 D_2	Rotate Two	
1 1	D_0 D_3 D_2 D_1	Rotate Three	

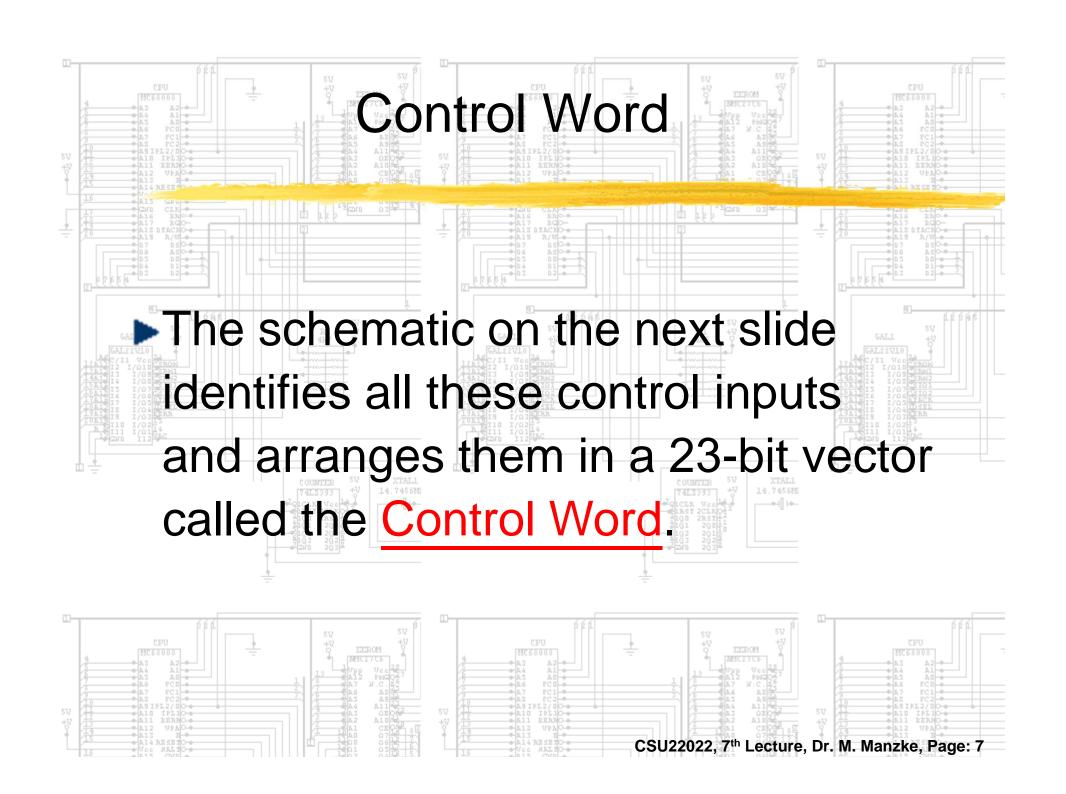
Controlling a Datapath

The Control Word

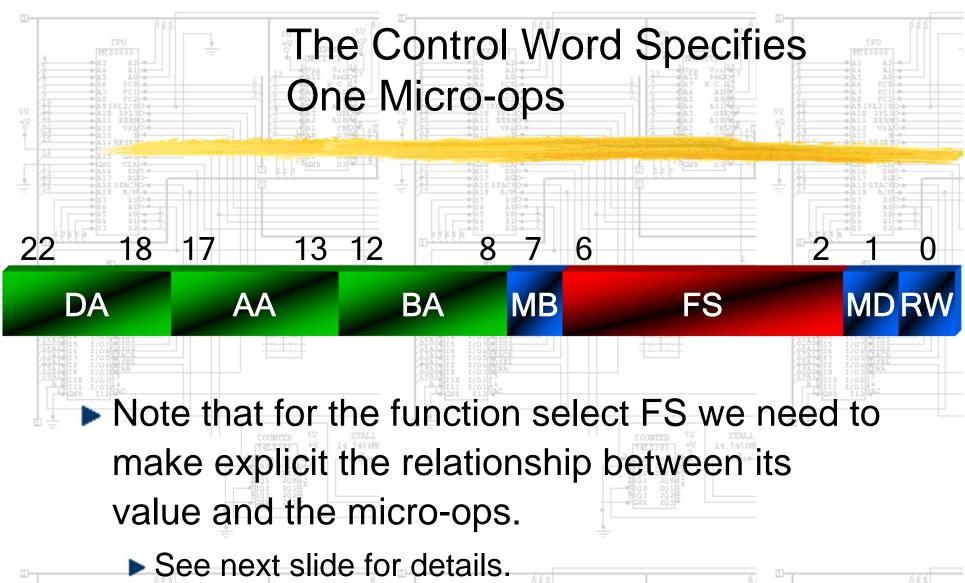
- The figure on the next slide is an updated version of our introductory datapath (4th Lecture, Page 12) where the register file has been expanded to a more realistic eight n-bit registers.
- Consequently the destination decoder and A and B bus MUX require three-bit select input.
- ► The Function Unit still requires five bits to select ALU/Shift micro-ops.
- ▶ Three more bits are required to control:
 - Writing to the registers (RW)
 - ► MUX B (MB)
 - ► MUX D (MD)







Datapath and the **Control Word** We have 5 bits for DA, AA, and BA. Also n = 32 bits D data RW 0 Write Address out DA D address 15-8 x n Register file Data out Bus A Bus B 13 AA A address B address 12-11 B data V A data Function C FS unit Bus A Bus B N + Z Constant in MB 7 MUX B Data in MD 1 MUX D Bus D 16 15 14 13 12 11 10 9 M R D W FS DA AA BA



G Select, H Select and MF Select determine the FS code

A SAIT EGO-			1817 BGO-	The first of the f	718 - 1417 EGO-
**************************************		G ‡ ∄	A18 DIACKO+	Output	7 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
05 00 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Sele	ect Select	Select		05 00 00 00 00 00 00 00 00 00 00 00 00 0
00	000 0	0000	XX	G = A	TRANSFER
50 OO	001 0	9 0001	XX	G = A + 1 R 50	INCREMENT
ASCALERYIO OC	010 0	0010	XX	G = A + B	ADD 12 AFC (11 VCC PARK)
1/0 200 00	011 0	0011	XX	G = A + B + 1	ADD WITH C
This i/O DEAR OC	100 0	0100	XX	G = A + B	A plus 1's C.B
OC	101 0	0101	XX	G = A + B + 1	SUBTRACT
00	110 0	0110	XX	G = A - 1	DECREMENT
00	111 0	¹ 0111	XX	G = A	TRANSFER
01	000 0	1000	XX	$G = A \wedge B$	AND
01	010 0	1010	XX	$G = A \vee B$	OR
01	100 0	1100	XX	$G = A \oplus B$	XOR
<u>01</u>	110 0	1110	XX	G = A	NOT
EPU 10	000 1	XXXX	OO CPU	G = B 50 mm	TRANSFER
A A A A A A A A A A A A A A A A A A A	100 1	XXXX	0 4 A1 A1	G = sr B	SHIFT RIGTH
8	000 1	XXXX	10	G = sl B	SHIFT LEFT

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