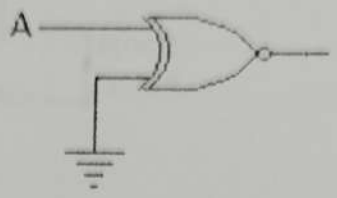
Part I: Multiple Choice

B 1. Decimal number 46 in excess 3 code = _____.

A. 1000 1001
B. 0111 1001
C. 0111 1111
D. 1000 1111

D 2. For the gate in the given figure the output will be



A. 0
B. 1
C. A
D. $\bar{A}$

C 3. An AND gate with schematic "bubbles" on its inputs performs the same function as a(n)_____ gate.

A. NOT B. OR C. NOR D. NAND

A 4. Full adder circuit can be implemented by

A. Multiplexers
B. Half adders
C. AND or OR gates
D. Decoders

B 5. A device which converts BCD to seven segments is called _____

A. Encoder B. Decoder C. Multiplexer D. Multiplexer

C 6. Which one of the following can be used as parallel to series converter?

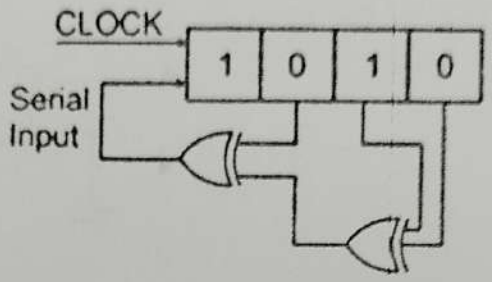
A. Decoder
B. Digital counter
C. Multiplexer
D. DeMultiplexer

A 7. As the number of flip flops are increased, the total propagation delay of

A. Ripple counter increases but that of synchronous counter remains the same
B. Both ripple and synchronous counters increase
C. Both ripple and synchronous counters remain the same
D. Ripple counter remains the same but that of synchronous counter increases

B 8. The shift register shown in the figure below is initially loaded with the bit patten **1010**. Subsequently, the shift register is clocked and with each clock pulse the pattern gets shifted by a one-bit position to the right. With each shift, the bit at the serial input is pushed to the leftmost position (MSB). After how many clock pulses will the content of the shift register become **1010** again?

A. 3
B. 7
C. 15
D. 11



D 9. Types of ROM memories are_____.

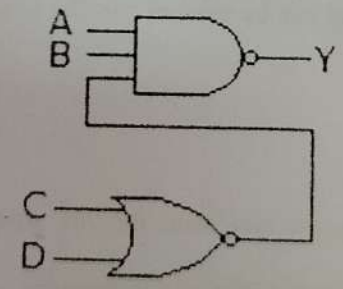
A
. EPROM B. PROM C. EEPROM D. All of these

A 10. The _____ is programmable logic device with a fixed OR array and a programmable AND array.

A. PAL B. PROM C. PLA D. None of the above

Part II: **Fill in the blanks space**

1. The decimal equivalent of the binary 0.1011 is $(0.6875)_{10} = (11/16)_{10}$
2. In the given figure, A = B = 1 and C = D = 0. Then Y = 0.



3. The number of product terms in the minimized sum of product expression obtained through the following K-map, where d, don't care is 2 output F= $\bar{B}\bar{D} + A\bar{C}\bar{D}$.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	0	1
$\bar{A}B$	0	d	0	0
AB	0	0	d	1
$A\bar{B}$	1	0	0	1

$\bar{B}\bar{D}$

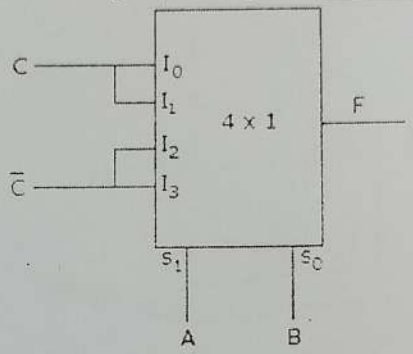
$\rightarrow AC\bar{D}$

$= \sum m(1,3,+6)$

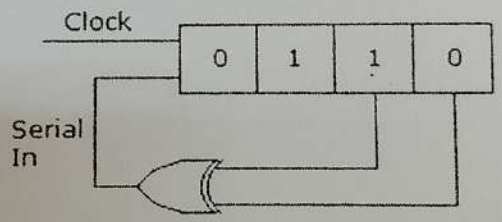
$= A'B'C + A'BC + AB'C' + ABC'$

?? $= A\bar{B}\bar{C} = AB' + A'C$

4. The logic realized by the circuit shown in figure, the output F= $A\bar{B}\bar{C} = AB' + A'C$



5. In the given figure shows a 4-bit serial in parallel out right shift register. The initial contents as shown are 0110. After 3 clock pulses the contents will be 1010.



Q1. BCD to Gray code Convertor Truth table

Decimal	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1

2

K-map for G_3

B_3B_2 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	X	X	X	X
10	1	1	X	X

1

$\therefore G_3 = B_3$

for G_2

B_3B_2 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

1

$G_2 = B_2 + B_3$

for G_1

B_3B_2 \ B_1B_0	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	X	X	X	X
10	0	0	X	X

1

$G_1 = B_2\bar{B}_1 + \bar{B}_2 B_1$

$= B_1 \oplus B_2$

K-map for G_0

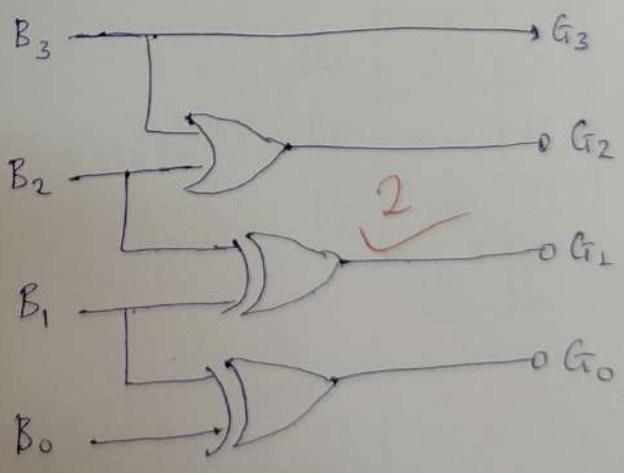
B_3B_2 \ B_1B_0	00	01	11	10
00		1		1
01		1		1
11	X	X	X	X
10		1	X	X

1

$G_0 = \bar{B}_1 B_0 + B_1 \bar{B}_0$

$= B_0 \oplus B_1$

Circuit Implementation



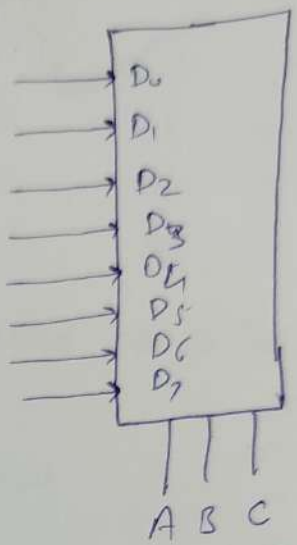
Solution : 2

(1)

Decimal No	Select Lines A	B	C	D	Output Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1

(1)

(2) Assume a, b, c as Select line and D as data line

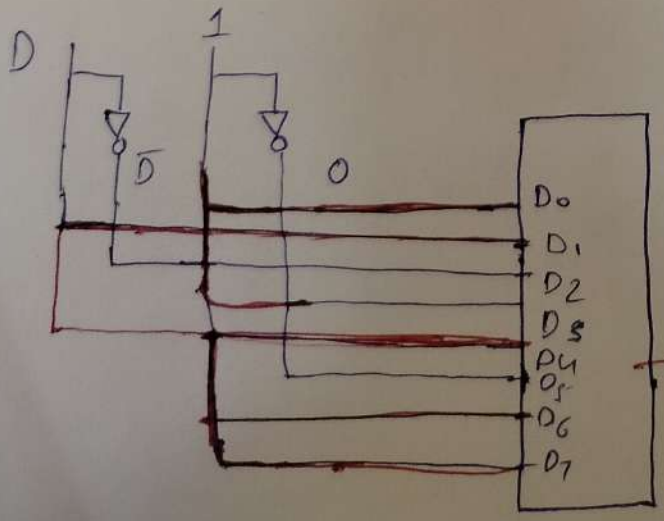


(1.5)

(3) Implement in Table

	$\bar{D}$	D
D_0	(0)	(1) — 1
D_1	2	(3) — D
D_2	(4)	5 — $\bar{D}$
D_3	6	7 — 0
D_4	(8)	(9) — 1
D_5	10	11 — 0
D_6	12	(13) — D
D_7	14	(15) — D

4 Implementation of Circuit using 8:1 MUX



$D_0 = A_4 = 1$

$D_1 = D_6 = D_7 = D$

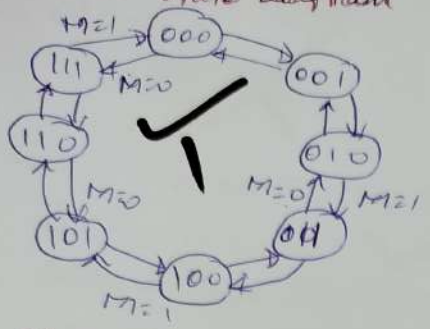
$D_2 = \bar{D}$

$D_3 = D_5 = 0$

(1.5)

Design the 3-bit up/down counter using JK FF
M=0, Count down, M=1 Count up

Step-1 State diagram



Step 2 Excitation Table

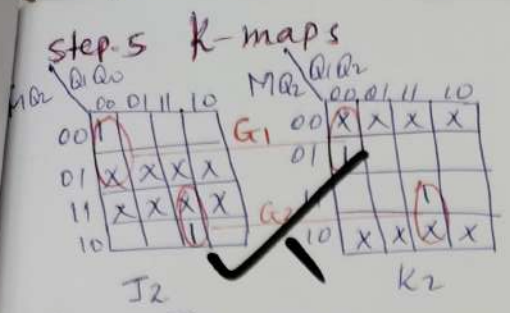
Output		FF Input	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

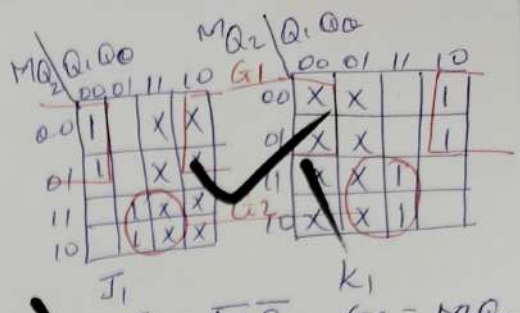
Step 3 & 4 - State diagram and next state Table.

M Control	Present state			next state			FF Input					
	Q_2	Q_1	Q_0	Q_{2+1}	Q_{1+1}	Q_{0+1}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	1	1	1	1	X	1	X	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
0	0	1	0	0	0	1	0	X	X	0	1	X
0	0	1	1	0	1	0	0	X	X	1	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	1	0	1	0	0	0	X	0	0	X	X	1
0	1	1	0	0	0	1	X	0	X	0	1	X
0	1	1	1	1	0	0	X	0	X	1	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	0	1	0	X	0	0	X	1	X
1	1	0	1	1	0	1	X	0	1	X	X	1
1	1	1	0	1	1	0	X	0	X	1	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

Q_4 From ...

Step-5 K-maps





$G_1 = \overline{M}\,\overline{Q_1}\,\overline{Q_0}$ + $G_2 = MQ_1Q_0$

$G_1 = \overline{M}\,\overline{Q_0}$, $G_2 = MQ_0$

$J_0 = K_0 = HIGH$ (1)

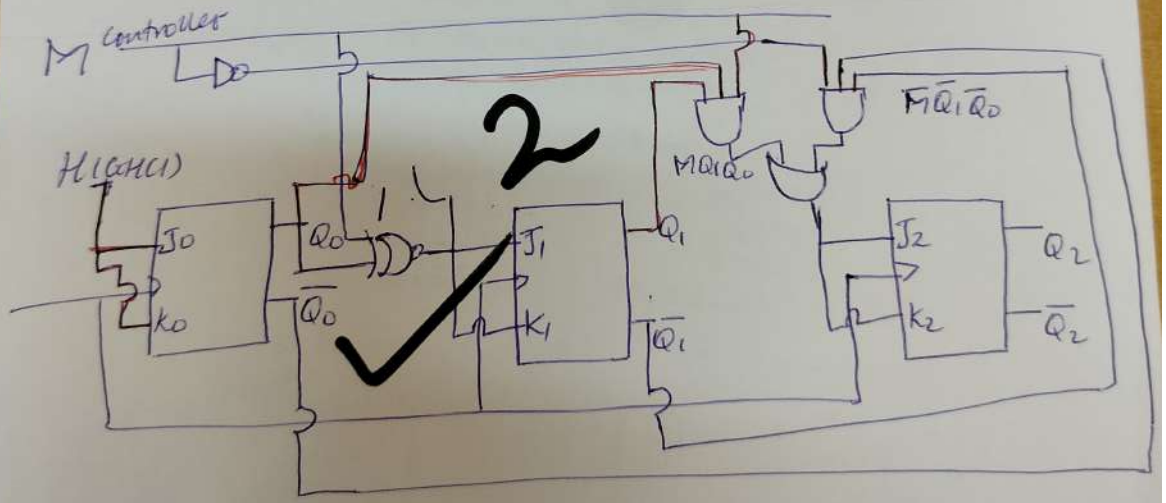
Step-6 Logic Expression

$J_2 = K_2 = \overline{M}\,\overline{Q_1}\,\overline{Q_0} + MQ_1Q_0$

$J_1 = K_1 = \overline{M}\,\overline{Q_0} + M\overline{Q_0} = \overline{M \oplus Q_0}$

$J_0 = K_0 = 1$ (H)

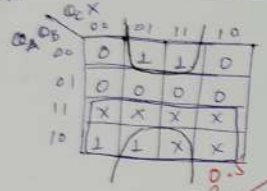
Step-7 Counter Implementation.



Present State			Input	Next State			o/p	T-FF			S-R FF					
Q_A	Q_B	Q_C	X	Q_A'	Q_B'	Q_C'	Y	T_A	T_B	T_C	S_A	R_A	S_B	R_B	S_C	R_C
0	0	0	0	0	1	1	0	0	1	1	0	x	1	0	1	0
0	0	0	1	1	0	0	1	1	0	0	1	0	0	x	0	x
0	0	1	0	0	0	1	0	0	0	0	0	x	0	x	x	0
0	0	1	1	1	0	0	1	1	0	1	1	0	0	x	0	1
0	1	0	0	0	1	0	0	0	0	0	0	x	x	0	0	x
0	1	0	1	0	0	0	1	0	1	0	0	x	0	1	0	x
0	1	1	0	0	0	1	0	0	1	0	0	x	0	1	x	0
0	1	1	1	0	1	0	1	0	0	1	0	x	x	0	0	1
1	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0	x
1	0	0	1	0	1	1	0	1	1	1	0	1	1	0	1	0

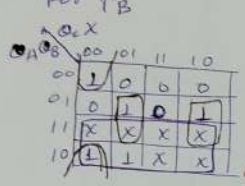
K-map for T

For T_A



$T_A = Q_A + \bar{Q}_B X$ 0.5

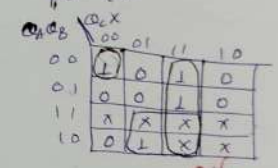
For T_B



$T_B = Q_A + \bar{Q}_B \bar{Q}_C \bar{X} + Q_B \bar{Q}_C X + Q_B Q_C \bar{X}$

$= Q_A + \bar{Q}_B \bar{Q}_C \bar{X} + Q_B (Q_C \oplus X)$ 0.5

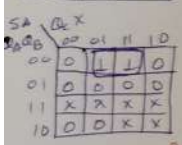
For T_C



$T_C = Q_A \bar{X} + Q_C X + \bar{Q}_A \bar{Q}_B \bar{Q}_C \bar{X}$

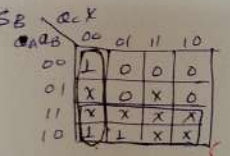
$= X(Q_A + Q_C) + \bar{Q}_A \bar{Q}_B \bar{Q}_C \bar{X}$ 0.5

K-map for S



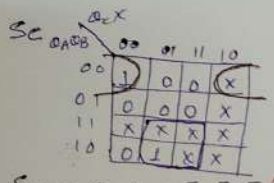
$S_A = \bar{Q}_A \bar{Q}_B X$ 0.5

S_B



$S_B = Q_A + \bar{Q}_C \bar{X}$ 0.5

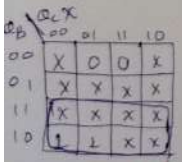
S_C



$S_C = Q_A X + \bar{Q}_A \bar{Q}_B \bar{X}$ 0.5

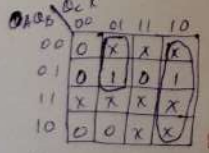
K-map for R

For R_A



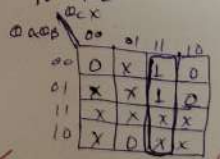
$R_A = Q_A$ 0.5

For R_B



$R_B = \bar{Q}_A \bar{Q}_C X + Q_C \bar{X}$ 0.5

For R_C



$R_C = Q_C X$ 0.5

K-map for o/p Y

$Y = \bar{Q}_A X$ 0.5

Q5 → Realized 4-bit Johnson Counter using D-FF

	Q_A	Q_B	Q_C	Q_D	Q_A'	Q_B'	Q_C'	Q_D'	D_A	D_B	D_C	D_D
initial	0	0	0	0	1	0	0	0	1	0	0	0
1	1	0	0	0	1	1	0	0	1	1	0	0
2	1	1	0	0	1	1	1	0	1	1	1	0
3	1	1	1	0	1	1	1	1	1	1	1	1
4	1	1	1	1	0	1	1	1	0	1	1	1
5	0	1	1	1	0	0	1	1	0	0	1	1
6	0	0	1	1	0	0	0	1	0	0	0	1
7	0	0	0	1	0	0	0	0	0	0	0	0
8												

K-map D_A

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	1	0	0	x
01	x	x	0	x
11	1	x	0	1
10	1	x	x	x

$D_A = \bar{Q}_D$

D_B

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	0	0	0	x
01	x	x	0	x
11	1	x	1	1
10	1	x	x	x

$D_B = Q_A$

D_C

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	0	0	0	x
01	x	x	1	x
11	1	x	1	1
10	0	x	x	x

$D_C = Q_B$

D_D

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	0	0	1	x
01	x	x	1	x
11	0	x	1	1
10	0	x	x	x

$D_D = Q_C$