√ TC74HC593AP/AF PRELIMINARY

8 BINARY COUNTER WITH INPUT REGISTER(3-State I/O)

The TC74HC593A is a high speed CMOS 8-BIT BINARY COUNTER/REGISTER fabricated with C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation

The TC74HC593A has all the features of the "HC592A with the addition of a 3-state I/O which provides parallel counter outputs. The 3-state outputs are active when enable input \overline{G} is low and G is high.

Inputs A through H are loaded into registers on the rising edge of Register Clock (RCK) only when Register Clock Enable (RCKEN) is low. The register outputs are loaded into the counter when Counter Load (CLOAD) is low.

The internal counter counts on the rising edge of Counter Clock (CCK) when Counter Clock Enable (CCKEN) is low and or Counter Clock Enable (CCKEN) is high.

If Counter Clear (CCLR) is set low, the internal counter is cleared asynchronously to the clock.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

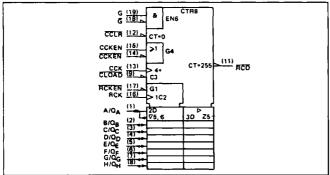
FEATURES.

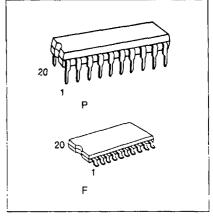
real cres:
• High Speed ······ f_{MAX} =80MHz(typ.)at V_{CC} =5V
• Low Power Dissipation ······ I _{CC} =4 µ A(Max.)at Ta=25°C
• High Noise Immunity ······· $V_{NIII} = V_{NIL} = 28\% \ V_{CC}(Min.)$
• Output Drive Capability 15 LSTTL Loads For QA~QH
10 LSTTL Loads For $\overline{ ext{RCO}}$
• Symmetrical Output Impedance ···
$ I_{OL} = I_{OL} = 6mA(Min.)$ For $QA \sim QH$
$ I_{OL} = I_{OL} = 4 \text{mA(Min.) For } \overline{\text{RCO}}$
• Balanced Propagation Delays to 14 = truly

• Wide Operating Voltage Range ··· V(C)(opr)=2V~6V

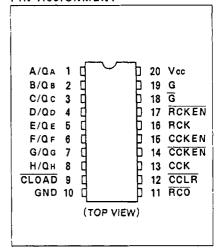
Pin and Function Compatible with 74LS593

IEC LOGIC SYMBOL



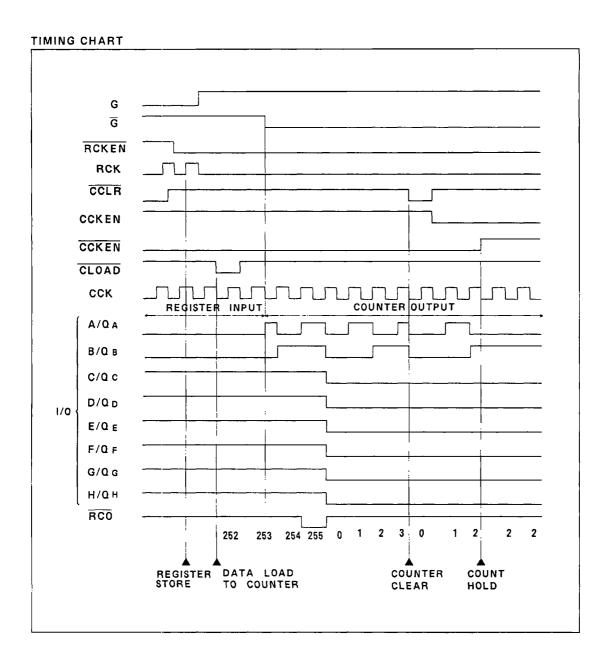


PIN ASSIGNMENT



APPLICATION NOTES

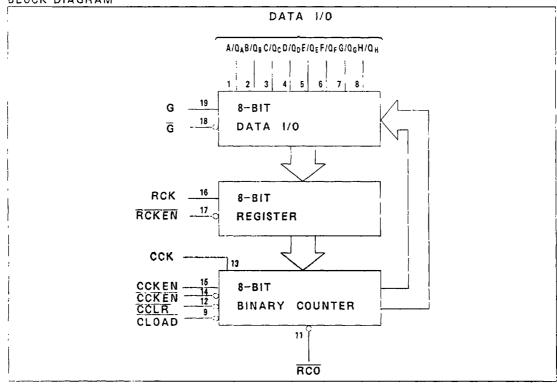
- 1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.



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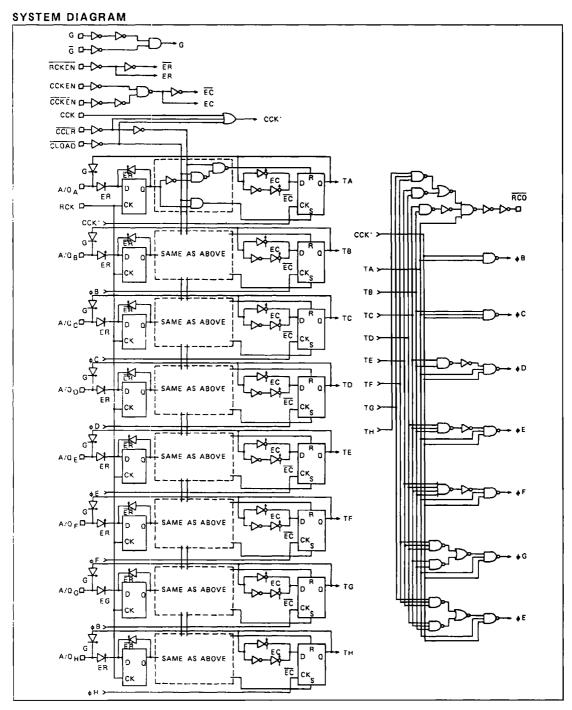
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H L X X X X X X X X THE I/O TERMINALS OUTPUT COUNTER DATA X X L X X X X X THE DATA OF A THRU H INPUTS IS STORED INTO REGISTER X X L X X X X X X X REGISTER STATE IS NOT CHANGED. X X X X X L H X X X X REGISTER DATA IS LOADED INTO COUNTER. X X X X X H L X X X COUNTER CLEAR. X X X X H H H X L	L	Х	; ×	_ X	X	X	: X	Х	X	THE 1/0 TERMINALS ARE IN THE HIGH			
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X X X X H L X X X COUNTER CLEAR. X X X X H H X L X X X X H H X L X X X X H H X L NO COUNTER ADVANCES THE COUNT.	X	X	Н	5	X	X	Х	X	X	REGISTER STATE IS NOT CHANGED.			
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X	X	X	X	X	Н	Н	Н	X	5	COUNTER ABYANGES THE COUNT			
X X X X H H X L L NO COUNT	X	X	X	X	Н	Н	X	L	4	COUNTER ADVANCES THE COUNT.			
	X	X	X	X	Н	Н	Н	Х	Ť.				
XXXXHHLHL	X	X	X	, X	Н	Н	Х	L	ŧ	NO COUNT			
	X	X	X	X	Н	Н	L	H	4				

BLOCK DIAGRAM



TC74HC593AP/AF-3 645





TC74HC593AP/AF-4 646

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{∞}	$-0.5 \sim 7$	V
DC Input Voltage	V_{lN}	$-0.5 \sim V_{\infty} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{\rm CC} + 0.5$	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current (RCO)	IOLT	±25 ±35	mA
DC V _C /Ground Current	I_{∞}	±75	mA
Power Dissipation	P_{D}	500(DIP)*/180(SOIC)	mW
Storage Temperature	Tstg	−65 ~ 150	ొ
Lead Temperature 10sec	T_{L}	300	°C

*500mW in the range of Ta=
-40°C~ 65°C. From Ta=65°C
to 85°C a derating factor of
-10mW/°C shall be applied
until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	v_{∞}	2 ~ 6	V
Input Voltage	V _{IN}	0 ~ Vcc	V
Onput Voltage	VOLT	$0 \sim V_{CC}$	V
Operating Temperature	Topr	-40 ~ 85	°C
		$0 \sim 1000(V_{\infty}=2.0V)$	
Input Rise and Fall Time	tr, tf	$0 \sim 500(V_{\infty}=4.5V)$	ns
		$0 \sim 400(V_{\rm CC}=6.0V)$	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃		Ta=-40		UNIT
1 MICAMESTER	DIMBOL	TEST CONSTITUTE	V_{∞}	MIN.	TYP.	MAX.	MIN.	MAX.	01111
High-Level			2.0	1.5		-	1.5	-	
Input Voltage	V_{iH}		4.5	3, 15	-		3, 15	_	V
Input Citage			6, 0	4. 2		_	4.2	-	
Low-Level			2.0	-	-	0.5	_	0, 5	i . I
Input Voltage	V_{IL}		4.5	-	-	1.35	-	1, 35	V
Impat ventage	<u></u>		6.0		-	1.8		1.8_	
	1	V _N = 1 20 " A	2, 0	1. 9	2, 0	-	1.9	-	
	1	$V_{\text{IH}} = -20 \mu \text{ A}$		4.4	4.5	-	4. 4	-	}
High-Level	İ		6.0	5.9	6, 0		5, 9		
Output Voltage	V_{OH}	$\frac{1}{RCO}$ $I_{OH} = -4$ mA		4.18	4, 31	-	4.13	_] V
Output Voltage		$I_{OH} = -5.2 \text{m}A$	6.0	5.68	5, 80	<u> </u>	5, 63	_	<u> </u>
i I		$I_{OH} = -6 \text{ mA}$	4.5	4. 18	4. 31	-	4.31	1	1 1
		$Q_{A} \sim Q_{H} I_{QH} = -6 \text{ mA}$ $I_{QH} = -7.8 \text{mA}$	6,0	5, 68	5, 80	<u>-</u>	5, 63	L	ļ
	ì	X7 _	2, 0	_	0.0	0.1		0.1	
		$\begin{vmatrix} V_{IN} = \\ V_{IH} \text{ or } V_{IL} \end{vmatrix} I_{OL} = 20 \mu \text{ A}$	4.5	ļ -	0.0	0.1	-	0.1	
Low-Level		VIHOLV II,	6.0	-	0.0	0.1	-	0.1	
1	V_{OL}	\overline{RCO} $I_{OL}=4$ mA	4. 5	-	0.17	0, 26	-	0.33	\ V
Output Voltage)	$I_{OL} = 5.2 \text{mA}$	6.0	L	0.18	0. 26	-	0. 33	
1		$I_{\alpha} = 6 \text{ mA}$	4.5		0.17	0. 26	-	0. 33	1
	L	$Q_{A} \sim Q_{H} \begin{vmatrix} I_{CL} = 6 & \text{mA} \\ I_{CL} = 7.8 \text{mA} \end{vmatrix}$	6.0		0, 18	0, 26		0, 33_	
3-State Output	T	$V_{\rm IN} = V_{\rm IH} \text{ or } V_{\rm IL}$	6.0	_		±0.5		±5.0	
Off-State Current	Icz	$V_{OUT} = V_{CC}$ or GND		<u> </u>				3. 0	μΑ
Input Leakage Current	I_{IN}	$V_{\rm IN} = V_{\rm CC}$ or GND	6.0			±0.1		±1.0	$\int_{-\mu}^{\mu} \Lambda$
Quiescent Supply Current	l_{∞}	$V_{\rm IN} = V_{\rm CC}$ or GND	6,0	-	-	4.0		40.0	

TC74HC593AP/AF-5

TIMING REQUIREMENTS(Input tr=tf=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=		Ta=-40 ~85℃	UNIT
THEMMETER	UODIM I	THE COMPTION	V_{CC}	TYP.	LIMIT	LIMIT	0.111
Minimum Pulse Width	twa.		2.0	-	75	Į 9 5	İ
(CCK, RCK)	1 . 11 /1.		4.5	_	15	19	
(CCR, RCR)	t _{W(H)}		6.0	_	13	16]
Menimum Pulse Width			2.0	_	100	125	
(CCLR)	$t_{W(L)}$		4.5	_	20	, 25	l
(CC17K)	i i		6.0		17	<u>. 21</u>	1
Minimum Pulse Width			2.0		100	125	
(CLOAD)	tw(L)		4.5	-	20	25	
(CLOAD)	!		6.0		17	21	
Minimum Set-up Time			2. 0	_	100	125	1
(RCKEN- RCK)	ts		4.5	-	20	25	
(RCKEN RCK)			6.0		17	21	j
Minimum Set-up Time			2.0	-	75	95	Ì
(CCKEN, CCKEN-CCK)	ts		4.5	-	15	19	
(CCKEN, CCKEN-CCK)			6.0	-	13	16	
Minimum Set-up Time	[2.0		150	190	
	t _s :		¹ 4.5 [']	-	30	ļ 38	ns
(RCK-CLOAD)			6.0	-	25	32	
Minimum Set- up Time			2.0		75	95	
-	t _s		4.5	- 1	15	! 19	i
(A~H-RCK)			6.0		13	16	ļ
	:		2.0		0	0	ì
Minimum Hold Time	th		4.5	-	0	0	
			6.0	-	0	0	
Minimum Hold Time	ii		2.0	-	5	5]
	t _h		4.5	-	5	, 5	
(CCKEN, CCKEN-CCK)	. "		6.0	-	5	5	
Minimum Damaual Ti			2.0	_	50	: 60	
Minimum Removal Time	t _{rem}		4.5	-	10	12	
(CCLR)	,		6.0	_	9	11	1
Minimum Dannum I TT	<u> </u>		2.0	_	75	95	1
Minimum Removal Time	trem		4.5	-	15	19	
(CLOAD)			6.0	_	13	16	
	;		2.0	_	4. 4	3.6	
Clock Frequency	f		4.5	-	22	18	MHz
	i		6.0	_	26	21	

AC ELECTRICAL CHARACTERISTICS($C_L = 15pF, V_{CC} = 5V, Ta = 25^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (RCO)	talli tall		-	4	8	
Propagation Delay Time (CCK-RCO)	t _{pl.II}		_	25	40	
Propagation Delay Time (RDK-RCO)	t _{plli}		_	35	53	ns
Propagation Delay Time (CCLR-RCO)	t _{pLH}		_	27	43	
Propagation Delay Time (CLOAD-RCO)	t _{pLH} t _{pHL}		_	29	43	
Maximum Clock Frequency	f _{MAX}		24	80		MHz

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6 \text{ns}$)

Output Transition Time (RCO) t t t t t t t t t	AX. 60 12 10 75 15 13 225 45 38 265 53 45 225 45 38 265 53 45 225 45 45	Ta=-4(MIN	75 15 13 95 19 16 280 56 48 330 66 56 280 56 48 330	UNIT
Output Transition Time (RCO) t TLH t THL 50 4.5 - 7 Output Transition Time (QA~QH) t TLH t THL 2.0 - 30 Propagation Delay Time (CCK-QA~QH) t pLH t pHL 2.0 - 93 2 Propagation Delay Time (CCLR-QA~QH) t pLH t pHL 2.0 - 106 2 Propagation Delay Time (CLOAD-QA~QH) t pLH t pHL 150 4.5 - 33 Propagation Delay Time (CLOAD-QA~QH) t pHL 150 4.5 - 30 Propagation Delay Time (CCK-RCO) t pLH t pHL 50 4.5 - 35 Propagation Delay Time (CCK-RCO) t pLH t pHL 50 4.5 - 35 Propagation Delay Time (CCK-RCO) t pLH t pHL 50 4.5 - 29 Propagation Delay Time (CCK-RCO) t pLH t pHL 50 4.5 - 29 Propagation Delay Time (CCK-RCO) t pHL 50 4.5 - 29 Propagation Delay Time (CCK-RCO) t pHL 50	12 10 75 15 13 225 45 38 265 53 45 225 45 38 265 53 45 225 45 38 265 53 45 225 45 38 225 45 38 225 45 45 45 45 45 45 45 45 45 45 46 46 46 46 46 46 46 46 46 46 46 46 46		15 13 95 19 16 280 56 48 330 66 56 280 56 48 330	
(RCO) t _{THL} 50 4.5 - 7 0utput Transition Time (QA~QH) t _{TLH} t _{THL} 50 4.5 - 8 Fropagation Delay Time (CCK-QA~QH) t _{pLH} t _{pHL} 2.0 - 93 2 Propagation Delay Time (CCLR-QA~QH) t _{pLH} t _{pHL} 2.0 - 106 2 Propagation Delay Time (CLOAD-QA~QH) t _{pLH} t _{pHL} 2.0 - 104 3 Propagation Delay Time (CLOAD-QA~QH) t _{pHL} t _{pHL} 2.0 - 100 2 Propagation Delay Time (CCK-RCO) t _{pHL} t _{pLH} t _{pHL} 2.0 - 113 3 Propagation Delay Time (CCK-RCO) t _{pHL} t _{pHL} 2.0 - 113 3 Propagation Delay Time (CCK-RCO) t _{pHL} 2.0 - 23 Propagation Delay Time (CCK-RCO) t _{pHL} 2.0 - 23 Propagation Delay Time (CCK-RCO) t _{pHL} 2.0 - 150 4.5 - 23 2.0 - 150 4.5 - 29 6.0 - 28 - 20 - 29 6.0 - 23 - 20 - 20	10 75 15 13 225 45 38 265 53 45 225 45 38 265 53 45 225 45 225 45 45 225 45 45 225 45 45 45 45 45 45 45 45 45 45 45 45 45		13 95 19 16 280 56 48 330 66 56 280 56 48 330	
Output Transition Time (QA~QH)	75 15 13 225 45 38 265 53 45 2225 445 38 265 53 45 225 45 225 45 38		95 19 16 280 56 48 330 66 56 280 56 48 330	
Output Transition Time (QA~QH) t _{TLH} t _{THL} 50 4.5	15 13 225 45 38 265 53 45 2225 45 38 265 53 45 225 45 225 45		19 16 280 56 48 330 66 56 280 56 48	
Propagation Delay Time (CCK-QA~QH) tpHL	13 2225 45 38 265 53 45 2225 45 38 265 53 45 225 45	- - - - - - - -	16 280 56 48 330 66 56 280 56 48	
Propagation Delay Time (CCK-QA~QH) Propagation Delay Time (CCLR-QA~QH) Propagation Delay Time (CCLR-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CCK-RCO)	2225 45 38 265 53 45 225 45 38 265 53 45 225 45 225 45 45 45 45 45 45 45 45 45 4	- - - - - - - - -	280 56 48 330 66 56 280 56 48 330	
Propagation Delay Time (CCK−QA~QH) Propagation Delay Time (CCK−QA~QH) tpHL tpHL tpHL	45 38 265 53 45 225 45 38 265 53 45 225 45 45 45 225 45 45 45 45 45 45 45 45 45 4	- - - - - - - -	56 48 330 66 56 280 56 48 330	
Propagation Delay Time (CCK−QA~QH) Propagation Delay Time (CCLR−QA~QH) tpHL tpHL	38 2265 53 45 2225 45 38 2265 53 45 2225 45	- - - - - - -	48 330 66 56 280 56 48 330	
CCK-QA~QH tpHL	265 53 45 2225 45 38 265 53 45 2225 45	- - - - -	330 66 56 280 56 48 330	
Propagation Delay Time (CCLR-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CCK-RCO) Propagation Delay Time (LUL) Pro	53 45 225 45 38 265 53 45 225 45		66 56 280 56 48 330	
Propagation Delay Time (CCLR-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CCK-RCO) Propagation Delay Time (LUL) Pro	45 225 45 38 265 53 45 225 45		56 280 56 48 330	
Propagation Delay Time (CCLR-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CCK-RCO)	225 45 38 265 53 45 225 45	- - - -	280 56 48 330	
Propagation Delay Time (CCLR−QA~QH) Propagation Delay Time (CLOAD−QA~QH) Propagation Delay Time (CLOAD−QA~QH) Propagation Delay Time (CCK−RCO) Propagation Delay Time (Location De	45 38 265 53 45 225 45	-	56 48 330	
Propagation Delay Time (CCLR−QA~QH) t _{pl.H} t _{pHL} 6.0 - 22 150 4.5 - 33 - 26 2.0 - 104 5 - 33 6.0 - 26 - 26 2.0 - 100 5 - 30 50 4.5 - 30 - 24 2.0 - 113 5 - 24 150 4.5 - 35 - 35 6.0 - 28 - 28 Propagation Delay Time (CCK−RCO) t _{pHL} t _{pHL} 50 4.5 - 29 Fropagation Delay Time (CCK − RCO) t _{pHL} t _{pHL} 50 4.5 - 29 2.0 - 23 - 23	38 265 53 45 225 45	-	48 330	
CCLR-QA~QH tpHL 150 4.5 - 33 6.0 - 26 2.0 - 100 50 4.5 - 30 6.0 - 24 2.0 - 113 50 4.5 - 35 6.0 - 24 2.0 - 113 50 4.5 - 35 6.0 - 28 2.0 - 113 50 50 4.5 - 35 6.0 - 28 2.0 - 28 2.0 - 28 2.0 - 23 2.0 - 23 2.0 - 23 2.0 - 25 2.0 - 2.0 - 2.0 2.0 - 2.0 2.0 - 2.0 2.0 - 2.0 2.0 - 2.0 2.0 - 2.0 2.0 - 2.0 2.0 - 2.0	265 53 45 225 45	-	330	
Propagation Delay Time (CCK-RCO) Propagation Delay Time (CCK-RCO) Propagation Delay Time (CCK-RCO) Propagation Delay Time tplH tpHL 150 4.5 - 35 6.0 - 28 2.0 - 113 2 2.0 - 113 2 2.0 - 28 2.0 - 95 2 2.0 - 95 2 2.0 - 23	53 45 225 45	-		
Propagation Delay Time (CCK−RCO) Propagation Delay Time (CCK−RCO) Propagation Delay Time tplH tpHL CCK − RCO 45 225 45				
Propagation Delay Time (CLOAD-QA~QH) Propagation Delay Time (CCK-RCO) Propagation Delay Time (CCK-RCO) Propagation Delay Time (CCK-RCO) Propagation Delay Time tplH tpHL Propagation Delay Time tpLH tpHL 2.0 - 100 2 2.0 - 24 2.0 - 113 2 2.0 - 95 2 6.0 - 28 Propagation Delay Time tpLH tpHL 2.0 - 150 3	225 45		66	
Propagation Delay Time (CCK-RCO) to the total control of the phil. Time (CCK-RCO) to the phil. Time (CCK-RCO) to the phil. Time to the phil to the phi	45		56	
Propagation Delay Time (CLOAD-QA~QH) tpHL tpHL		_	280	ĺ
CLOAD-QA~QH tpHL		_	56	ĺ
150 4.5 - 35 6.0 - 28	38		48	Į
Propagation Delay Time (CCK-RCO)	265	_	330	ns
Propagation Delay Time (CCK-RCO) to the print to the propagation Delay Time to the print to the	53	_	66	
CCK-RCO	45 225		56 280	1
(CCK-RCO) t _{pHL} 30 4.3 - 23 Propagation Delay Time 1 2.0 - 150 3	45	_	56	
Propagation Delay Time to 2.0 - 150 3	38	_	48	
Propagation Ligian Little 1 f - 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	300	_	375	i
'Borr = 36'	60	_	75	
$\begin{array}{c cccc} (RCK-RCO) & t_{pHL} & 30 & 4.3 & - & 40 \\ \hline & 6.0 & - & 31 & - & 31 \\ \hline \end{array}$	51	_	64	
	250		315	
1 Topagation <u>Detay</u> 1 time +	50	-	63	
$\begin{array}{c cccc} (CCLR-RCO) & \begin{array}{c ccccc} cpLH & & 30 & 4.3 \\ \hline 6.0 & - & 24 \end{array}$	43	_	54	ļ
	250	-	315	
(CTOAD_BCO) 50 4.5 30	50	_	63	l
0.0 - 26	43	-	54	1
	150	_	190	
50 4.5 - 18	30	_	38	l
Output Enable time $R_1 = 1 k\Omega$	26	 -	32	1
t _{pZH} 2.0 /1	190	_	240	ļ
100 4.5 25	38 32	_	48 41	1
	150	-	190	1
Output Disable time $t_{pl.Z}$ $R_L = 1 k\Omega$ 50 4.5 - 21	30	_	38	
t _{pHZ} 6.0 - 18	26	_	32	}
2.0 4.4 17		3, 6	-	1 —
Maximum Clock Frequency f _{MAX} 50 4.5 22 64	-	18	_	MHz
6.0 26 84		21_		l
Input Capacitance C _N - 5			10]
Output Capacitance Cout - 13	10		_] pF
Power Dissipation Capacitance C _{PD} (1) - 59	10		T-	

Note (1) CpD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

IC co = CpD • Vcc • f_N + I_C

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