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Review on Clock Gating Techniques

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Abstract— this is an era of hand held devices like cellular mobile phones, personal digital assistants and many more. This is possible because of microprocessors embedded in these devices. These devices must operate at high speeds but at the same time must survive long standby time. So low power high speed processors are the need of the hour, one such method for reducing dynamic power consumption is clock gating. This paper reviews various clock gating techniques available in literature.

Keywords— Clock gating, dynamic power consumption, FPGA

I. INTRODUCTION

Portable devices with wireless network connections such as Personal Digital Assistants (PDA), cellular phones and Global Positioning System (GPS) navigators have become increasing popular and widely-used over the past few years. One reason for the widespread adoption is their usability such as a transformation to a graphical interface. The ability for such a transformation has much to do with the high performance microprocessors embedded in them. Not only are the microprocessors expected to execute complicated functions, but they also should sustain reasonably long usage times giving rise to a need for low power consumption. This explains why a lot of research effort and technological developments centre on building microprocessors that can deliver high performance and yet consume minimal power. In this paper some techniques that have been developed to reduce power consumption in microprocessors are discussed.

Low Power processor Design is based on application of clock gate to turn off the sub-module of processor that is not in use by current executing instruction as decided by instruction decoder unit. According to [1]-[3], Clock Power consumes 50-70 percent of total chip power and will increase in the next coming generation of hardware designs at 32nm and below. Hence, reducing clock power is very important. Clock gating is a key power reduction technique used by hardware designers and is typically implemented by RTL-level HDL Simulator or gate level power analyzer tools.

Power = C_L × (Voltage × frequency) ------- (1)

In equation (1) power is directly proportional to the square of voltage and the frequency of the clock. Clock gating is used in VLSI circuit design to reduce dynamic power by gating off the functional unit that is not in use by current executing instructions as decided by instruction decoder unit.

The various clock gating techniques are listed below:

- Latch Free AND Clock Gating
- Clock Gating using NOR Gate
- Latch based AND Gate Clock Gating
- Latch based NOR Gate clock Gating
- MUX based Clock Gating
- Optimized Latch Based Clock Gating

Following sections will discuss above mentioned clock gating techniques.

II. Latch Free AND Clock Gating

Initially many authors suggested using AND gate for Clock gating because of its simple logic [4][5][6]. In sequential circuit one two-input AND gate is inserted in logic for clock gating. One input to AND gate is clock and while the second input is a signal used to control the output (means it will control the sequential circuit's clock). For experimental purpose we are taking a simple counter shown in Figure 1 as a sequential circuit application. Figure 2 shows the waveform of the output of regular counter, initially at reset = '0', counter initialized to "0" and after that when reset='1' counter increments at each negative edge of the clock. Figure 3 shows the clock gating technique for the counter by inserting one AND Gate. Figure 4 shows the output of counter when counter is negative edge triggered and enable ('en') changes from clock cycle starting from negative edge to the next negative edge, in this case output of the counter changes after one clock cycle of being en='1'. From Figure 5 we have observed that when counter is positive edge triggered and enable is changing starting from positive edge to the next positive edge, counter increments one extra time, due to tiny "Glitch", when it goes down due to more falling time of the enable, and the output in this case is wrong. In Figure 6 shows that for positive edge triggered system when enable turns ON at negative edge of the clock to the
next negative edge, the counter increments only one time at positive edge of the clock because when enable goes down there is the negative edge of the clock not positive. In Figure 7 we have shown a major problem of Hazards when any hazard at the enable could be pass on to the Gclk when clk='1' this situation is particularly very dangerous and could jeopardize the correct functioning of the entire system [7].

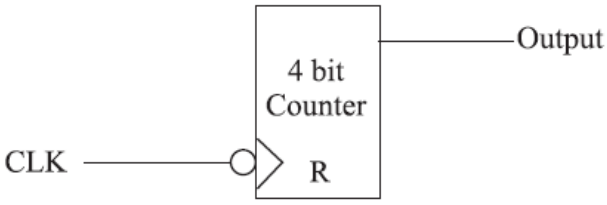

Figure 1: 4 bit counter

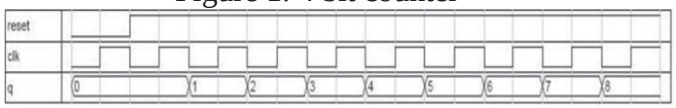

Figure 2: Normal output of counter without clock gating

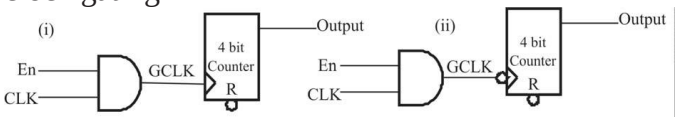

Figure 3: Clock gating using AND gate

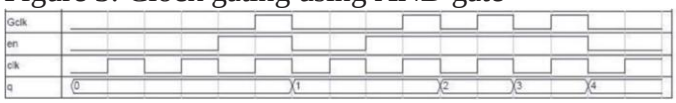

Figure 4: Output of counter when counter is negative edge triggered

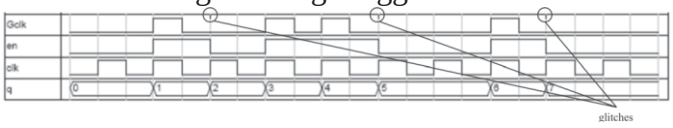

Figure 5: Wrong output of counter when it is positive edge triggered

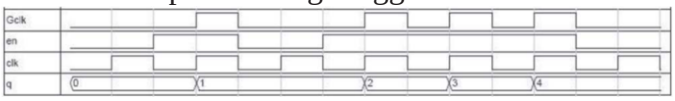

Figure 6: Correct output when counter is positive edge triggered

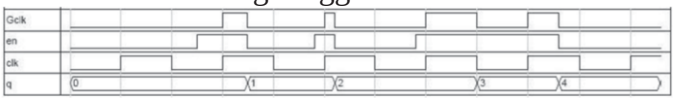

Figure 7: Hazard Problem when using AND gate clock gating technique

III. Clock Gating Using NOR gate

NOR gate is a very suitable technique for clock gating where we need actions to be performed on Positive Edge of the Global clock [7][6]. For analysis using NOR gate, the circuit connection is shown in Figure 8; in this figure we can observe that Counter will work when enable turn "ON". Figure 9 shows the waveform for incorrect output of the Counter when enable changes to '1' at negative edge of

the clock. Incorrect output is due to the small glitch when enable turns low at negative edge of the clock, counter increments one more clock. Figure 10 shows output of Counter when enable changes from positive edge to next positive edge but counter is negative edge triggered. Figure 11 shows correct output of the counter with positive edge triggered because enable is changing from positive edge of the clock to the next positive edge of the clock. In the figure 12 we have shown a major problem of Hazards. When any hazard at the enable could be pass on to the Gclk when clk='0' this situation is particularly very dangerous and could jeopardize the correct functioning of the entire system [7].

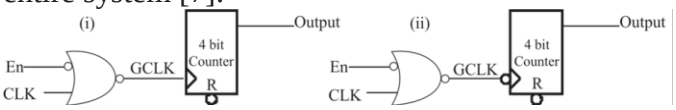

Figure 8: Clock gating using NOR gate

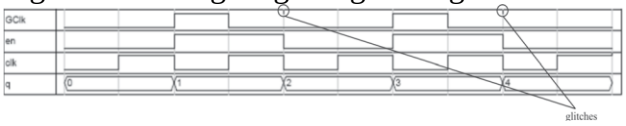

Figure 9: Incorrect Output of counter when counter is positive edge triggered

Figure 10: Output of Counter when enable changes from positive edge to next positive edge but counter is Negative edge Triggered.

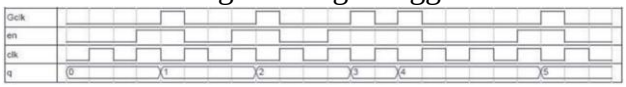

Figure 11: Correct output of Counter when Counter is positive edge triggered

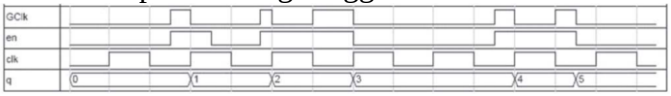

Figure 12: Hazards Problem when NOR Gate is used for clock gating

IV. Latch Based AND Clock Gating

Latch Based AND Gated Clock circuit is shown in Figure 13. The enable signal 'En' is applied through a latch to overcome the previous problems of incorrect output in place of directly connected to AND gate. The Latch is needed for correct behavior, because En might have Hazards that must not propagate through AND gate when Global clock is '1' [9][12][8]. However, the delay of the logic for the computation of En may on the critical path of the circuit will increase and its effect must be taken into account during time verification [12][10][8][11].

It is clear from Figure 14 that counter will take one extra clock cycle delay to change its state and after that it will work normally until, En is de-asserted and this time also it will take one clock cycle extra to stop changing its state. Figure 15 verifies that unwanted outputs due to Hazards at the En are avoided. Figure 17 waveform show that when controlling latch is positive and counter is also positive edge triggered then output of the counter is incorrect because it increments once even when enable is turned down due to a tiny glitch.

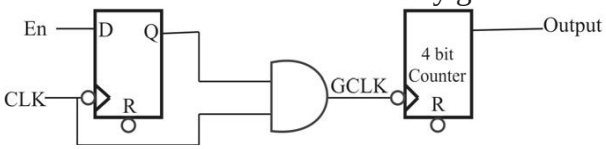

Figure 13: Flip Flop based clock gating technique

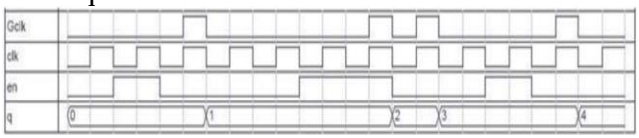

Figure 14: Normal output of negative edge counter when negative latch AND gated clock is used

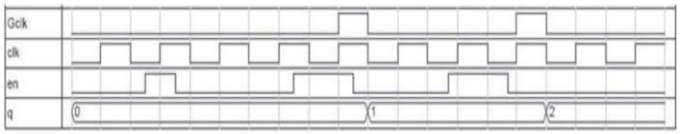

Figure 15: Output of negative edge counter when there is some random hazards at En

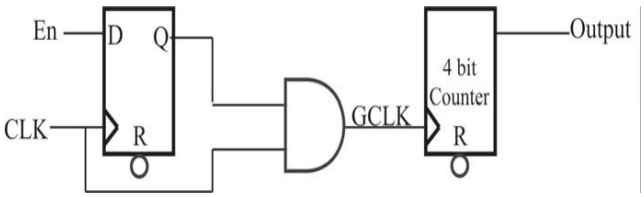

Figure 16: Clock gating of positive edge counter using positive latch Based and gate circuit

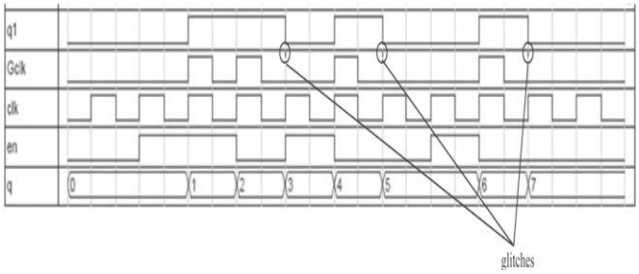

Figure 17: Output of counter when latch is positive and counter also positive edge triggered

V. LATCH BASED NOR GATE CLOCK GATING

Latch based NOR Gated Clock scheme is shown in Figure 18. Here enable signal is a applied through latch in place of direct connection to NOR gate. We can observe from Figure 19 that counter will take one extra clock cycle delay to change its state and after that it will work normally until En is de-asserted and this time also it will take one clock cycle extra to stop changing its state. In Figure 20 we have verified that unwanted outputs due to Glitches at the En are avoided. In Figure 22 waveform the case when controlling Latch is negative and Counter is also negative edge triggered is shown. The output of the counter is incorrect because it increments once even when enable is turned down due to a tiny glitch due to the fall time delay of enable.

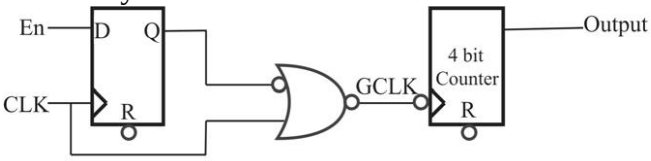

Figure 18: Clock gating of negative edge counter using positive latch based NOR gate circuit

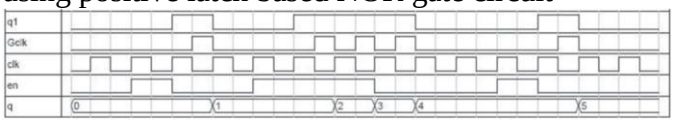

Figure 19: Normal output of negative edge counter when positive latch based OR Gated Clock is used

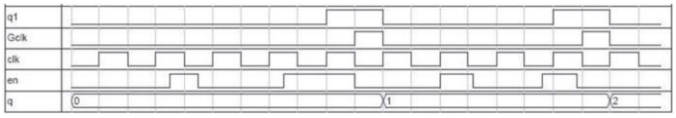

Figure 20: Output of negative edge counter when there are some random hazards at En

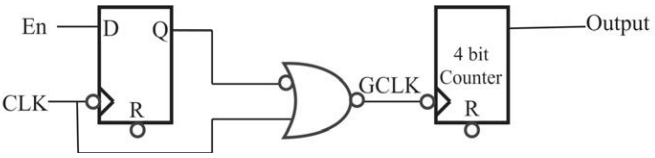

Figure 21: Clock gating of negative edge counter using negative latch based NOR gate circuit

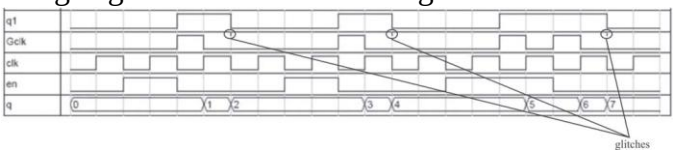

Figure 22: Output of counter when latch is negative and counter also negative edge triggered

VI. MUX BASED CLOCK GATING

In mux based clock gating we use multiplexer to close and open a feedback loop around a basic D-type flip-flop under control of the enable signal as shown in Figure 23. As the resulting circuit is simple, robust, and compliant with the rules of synchronous design this is a safe and often also a reasonable choice. On the negative side, this approach takes one fairly expensive multiplexer per bit and consumes more power. This is because any toggling of the clock input of a disabled flip-flop amounts to wasting of energy in discharging and recharging the associated node capacitances for nothing. The capacitance of the CLK input is not the only contribution as any clock edge causes further nodes to toggle within the flip - flop itself [7]. In Figure 24 waveform of Negative Edge triggered Counter is shown and in 25 Positive edge triggered. We can observe from these waveforms that when En turns ON then at each Negative and Positive Edge of the clock respectively counter increments and when En goes Low counter holds its state.

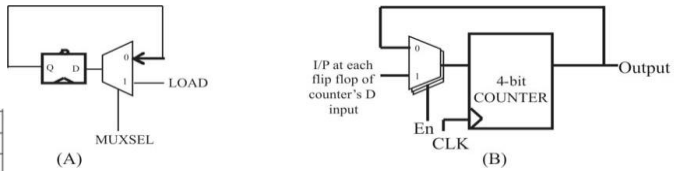

Figure 23: (A) Logic of MUX based Gated Clock (B) Counter using MUX based Clock Gating

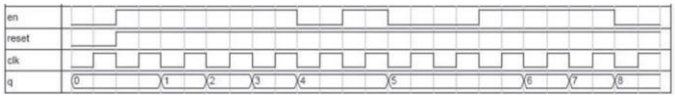

Figure 24: Output of negative edge triggered counter with MUX based clock Gating

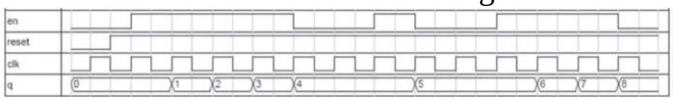

Figure 25: Output of positive edge triggered counter with MUX based clock Gating

VII. Optimized Latch Based Clock Gating

An input signal named 'En' is provided to the latch. When En turns to '1' at that time GEN is '0', XNOR will produce x='0' which goes to the first clock generation logic that generates clock for controlling device (LATCH). In first logic we have an OR gate which have Global Clock as an input at the other input of OR gate. This logic will generate a clock pulse that will drive the controlling latch when 'x' turns to '0'.

In the next clock pulse, when GEN turns to '1' our second clock generation logic which is an AND gate which has GEN and Global clk at its input and when Gen goes '1' it generates clock pulse that goes to the target device. Since GEN is '1' the XNOR will produce x='1' thus OR will produce at CClk constant HIGH until En turns to '0'. This way GClk will be running and CClk will be at Constant '1' state that means latch will hold its state without any switching.

The circuit shown in figure 27 performs similar sequence of operations as explained for the circuit shown in figure 26. When En turns to '1' at that time GEN is '0' so XOR will produce x='1' which goes to the first clock generation logic that generates clock for controlling device (LATCH). In first logic we have an AND gate, which have Global Clock as an input at the other input of AND gate. This logic will generate a clock pulse that will drive the controlling latch when 'x' turns to '1'. In the next clock pulse, when GEN turns to '1' our second clock generation logic which is an OR gate which has Q and Global clock at its input and when Q goes '0' it generates clock pulse that goes to the target device. Since GEN is '1' the XOR will produce x='0' thus OR will produce at CClk constant LOW until En turns to '0'. This way GClk will be running and CClk will be at Constant '0' state that means latch will hold its state without any switching.

The output of Counter for circuit as in Figure 26 is shown in Figure 28, 29. In Figures 28 and 29 enable changes from negative edge to next negative edge and positive edge to next positive edge respectively and also target is negative edge triggered and positive edge triggered respectively. However, in both cases counter's state changing delay is different but output is correct which gives us solution of the problem that persists in first four types of clock gating.

The output of Counter for circuit as in Figure 27 is shown in Figure 30 & 31. In figure 30 & 31 enable changes from negative edge to next negative edge and positive edge to next positive edge respectively and also target is negative edge triggered and positive edge triggered respectively. However, in both cases counter's state changing delay is different but output is correct which gives us solution of the problem that persists in first four types of clock gating. Thus one can avoid more switching and can save power.

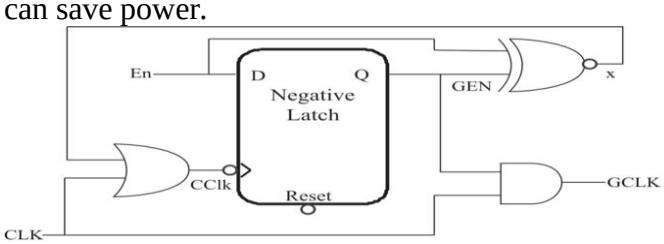

Figure 26: Generation of gated clock when negative latch is used

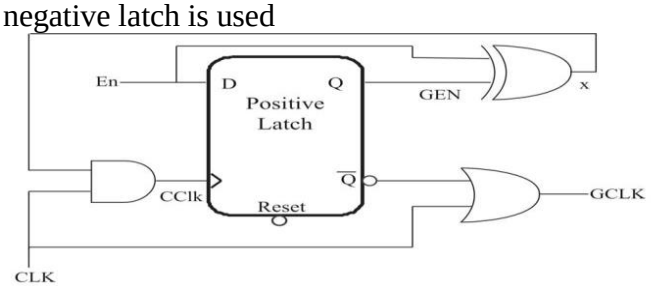

Figure 27: Generation of gated clock when positive Latch is used

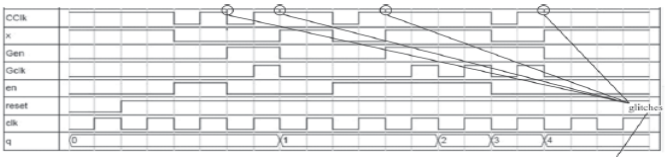

Figure 28: Output of negative edge counter with gated clock for circuit 26

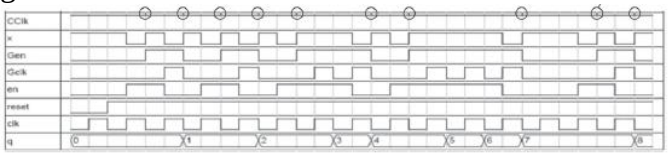

Figure 29: Output of positive edge counter with gated clock for circuit 26

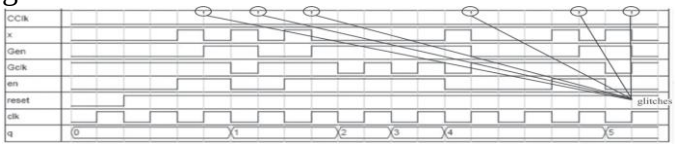

Figure 30: Output of negative edge counter with gated clock for circuit 27

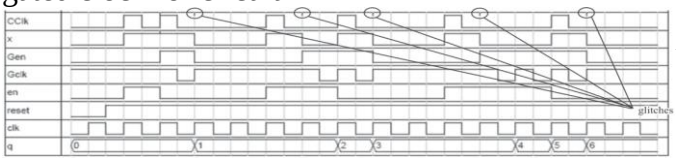

Figure 31: Output of positive edge counter with gated clock for circuit 27

VIII. CONCLUSION

In this paper we have reviewed different clock gating techniques. Hazard is the basic problem associated with all the clock gating techniques discussed in section II to V. in section VI mux based clock gating technique is discussed which didn't have this problem. In the end a optimized clock gating scheme is discussed, this technique is hazard free and also reduces the power consumption more effectively compared to other methods discussed.

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