MIT International Journal of Electronics and Communication Engineering *Vol. 1 No. 2 Aug 2011 pp 106-114*
ISSN 2230-7672 © MIT Publications

A Review of Clock Gating Techniques

Jagrit Kathuria
Centre for Development of Advanced Computing, NOIDA, India

M. Ayoubkhan
Centre for Development of Advanced Computing, NOIDA, India

Arti Noor
Centre for Development of Advanced Computing, NOIDA, India

Abstract: **The synchronous design operates at highest frequency that drives a large load because it has to reach many sequential elements throughout the chip. Thus, clock signals have been a great source of power dissipation because of high frequency and load. Clock signals do not perform any computation and mainly used for synchronization. Hence these signals are not carrying any information. So, by using clock gating one can save power by reducing unnecessary clock activities inside the gated module. In this paper, we present a review of some existing techniques available for clock gating. Also a new technique that provides more immunity to the existing problems in available techniques is discussed.**

Keywords: **Chirp signals, digital watermarking, perceptual transparency, and robustness.**

I. Introduction

Today's consumer demands more functionality, energy efficient device and optimized power devices as time goes, so in order to optimize power of a device the simplest control technique is to shut off the clock of the sequential block of the device when there is no function required from that section for some duration.

Clock Gating is a technique that can be used to control power dissipated by Clock net. In synchronous digital circuits the clock net is responsible for significant part of power dissipation (up to 40%) [2]. Clock gating reduces the unwanted switching on the parts of clock net by disabling the clock.

RTL clock gating is the most common technique used for optimization and improving efficiency but still it leaves one question that how efficiently design is clock gated [7]. Gated Clock is easily accepted technique in order to optimize power and can be applied at system level, gate level and RTL.Clock Gating can save more power by not clocking the register if there is no change in its state. Clock continuously consumes power because it toggles the registers and their associated logic. So, to reduce power consumption clock gating shuts off the clock while system maintaining its current state.

In this paper, we will discuss five existing techniques available for clock gating and observations made during their simulations. A new technique is also suggested in this paper which saves more power as compared to existing one.

II. Review of Available Techniques

There are five different techniques for Clock Gating as discussed below:

A. AND GATES

Initially many authors suggested using AND gate for Clock gating because of its simple logic [6][9][13]. In sequential circuit one two-input AND gate is inserted in logic for clock gating. One input to AND gate is clock and while the second input is a signal used to control the output(means it will control the sequential circuit's clock). For experimental purpose we are taking a simple counter shown in Fig 1(A) as a sequential circuit application.

Figure 1(B) shows the waveform of the output of regular counter, initially at reset = '0', counter initialized to "0" and after that when reset='1' counter increments at each negative edge of the clock.

Figure 2(A) shows the clock gating technique for the counter by inserting one AND Gate. Figure 2(B) shows the output of counter when counter is negative edge triggered and enable ('en') changes from clock cycle starting from negative edge to the next negative edge, in this case output of the counter changes after one clock cycle of being en='1'. From Figure 2(C) we have observed that when counter is positive edge triggered and enable is changing starting from positive edge to the next positive edge, counter increments one extra time, due to tiny "Glitch", when it goes down due to more falling time of the enable, and the output in this case is wrong.

In Figure 2(D) shows that for positive edge triggered system when enable turns ON at negative edge of the clock to the next negative edge, the counter increments only one time at positive edge of the clock because when enable goes down there is the negative edge of the clock not positive. In Figure 2(E) we have shown a major problem of Hazards when any hazard at the enable could be pass on to the Gclk when clk='1' this situation is particularly very dangerous and could jeopardize the correct functioning of the entire system [11].

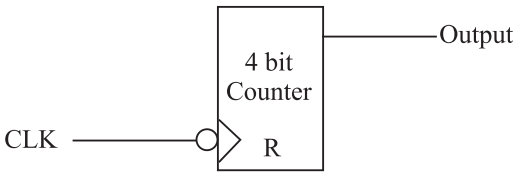

Figure 1(A): Basic Counter (negative edge triggered).

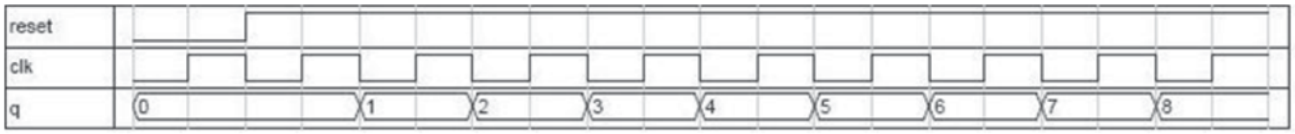

Figure 1(B): Normal output of the counter without Clock Gating.

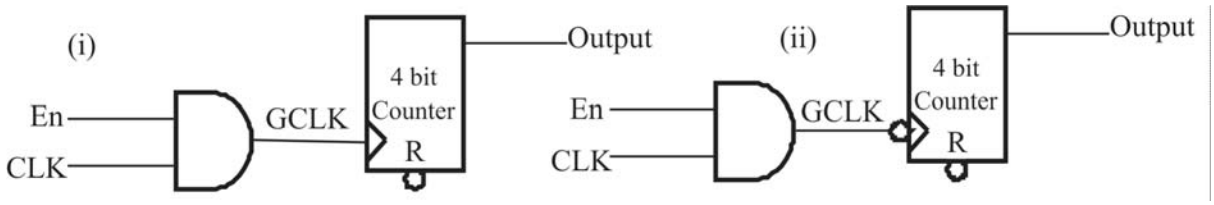

Figure 2(A): Clock gating using AND gate Circuit.

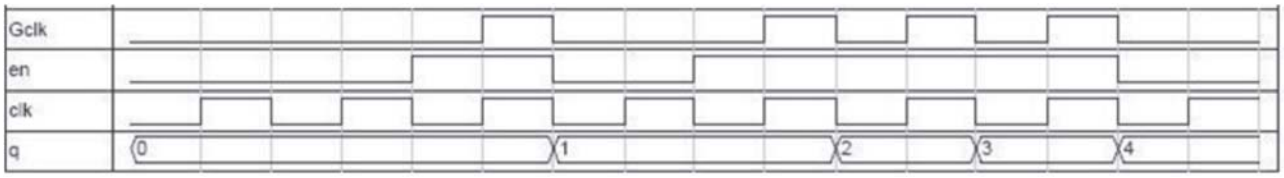

Figure 2(B): Output of Counter when Counter is Negative edge triggered.

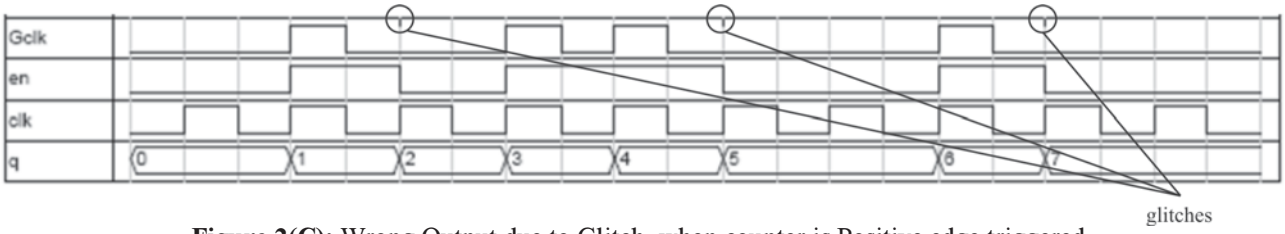

Figure 2(C): Wrong Output due to Glitch, when counter is Positive edge triggered.

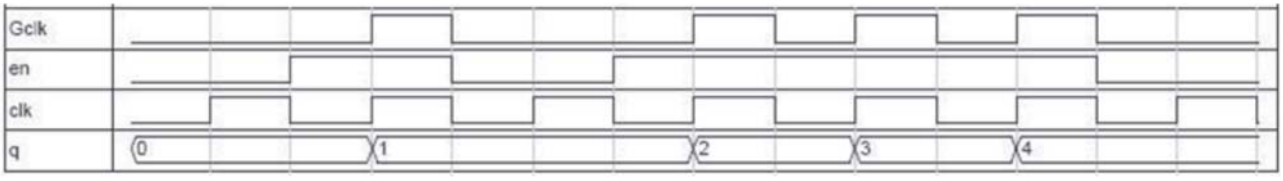

Figure 2(D): Right Output when counter is positive edge triggered.

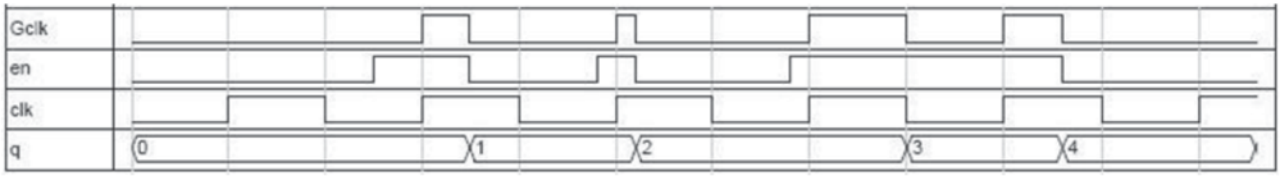

Figure 2(E): Hazards Problem when AND clock gating Circuitry used.

B. NOR GATES

NOR gate is a very suitable technique for clock gating where we need actions to be performed on Positive Edge of the Global clock [11][13].

For analysis using NOR gate, the circuit connection is shown in Figure 3(A); in this figure we can observe that Counter will work when enable turn "ON".

Figure 3(B) shows the waveform for incorrect output of the Counter when enable changes to '1' at negative edge of the clock. Incorrect output is due to the small glitch when enable turns low at negative edge of the clock, counter increments one more clock. Figure 3(C) shows output of Counter when enable changes from positive edge to next positive edge but counter is negative edge triggered. Figure 3(D) shows correct output of the counter with positive edge triggered because enable is changing from positive edge of the clock to the next positive edge of the clock. In the figure 3(E) we have shown a major problem of Hazards. When any hazard at the enable could be pass on to the Gclk when clk='0' this situation is particularly very dangerous and could jeopardize the correct functioning of the entire system [11].

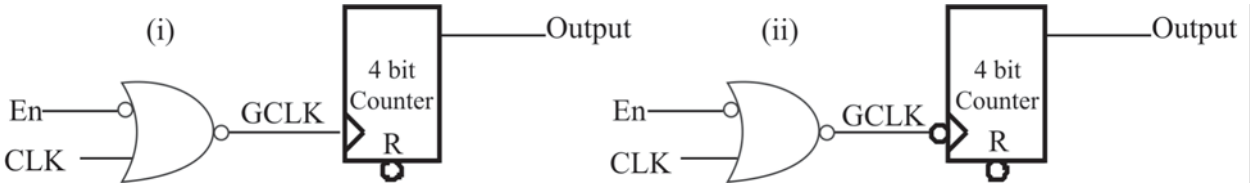

Figure 3(A): Clock gating using NOR gate Circuit.

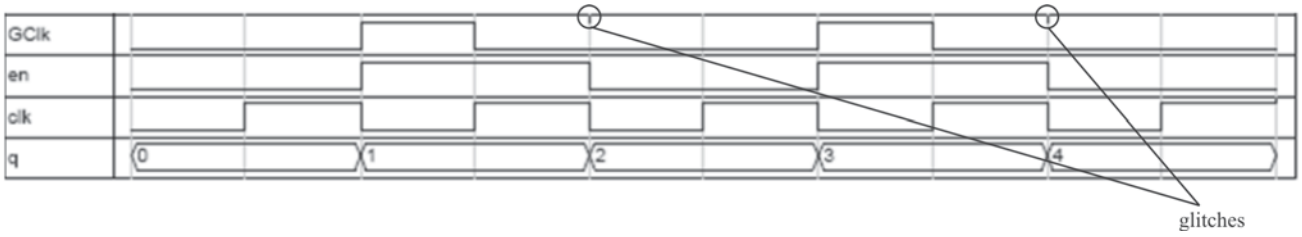

Figure 3(B): Incorrect Output of Counter when Counter is positive edge triggered.

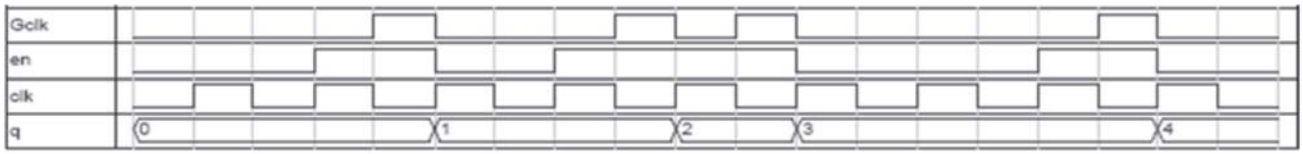

Figure 3(C): Output of Counter when enable changes from positive edge to next positive edge but counter is Negative edge Triggered.

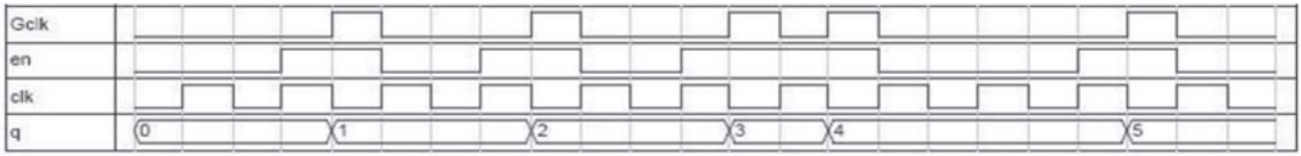

Figure 3(D): Correct Output of Counter when counter is Positive edge triggered.

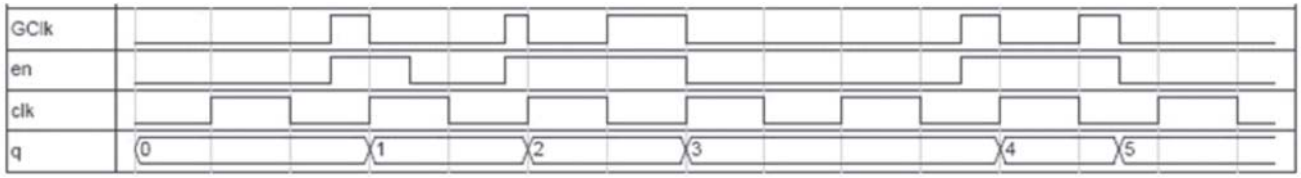

Figure 3(E): Hazards Problem when NOR Gate is used for clock gating.

C. LATCH BASED AND GATE CLOCK GATING

Latch Based AND Gated Clock circuit is shown in Figure 4(A). The enable signal 'En' is applied through a latch to overcome the previous problems of incorrect output in place of directly connected to AND gate. The Latch is needed for correct behavior, because En might have Hazards that must not propagate through AND gate when Global clock is '1' [1][3][5]. However, the delay of the logic for the computation of En may on the critical path of the circuit will increase and its effect must be taken into account during time verification [1][4][5][12].

It is clear from Figure 4(B) that counter will take one extra clock cycle delay to change its state and after that it will work normally until, En is de-asserted and this time also it will take one clock cycle extra to stop changing its state.

Figure 4(C) verifies that unwanted outputs due to Hazards at the En are avoided. Figure 4(E) waveform show that when controlling latch is positive and counter is also positive edge triggered then output of the counter is incorrect because it increments once even when enable is turned down due to a tiny glitch.

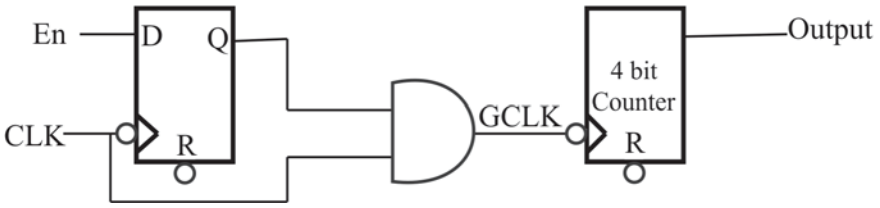

Figure 4(A): Clock gating of negative edge counter using negative Latch Based AND gate Circuit.

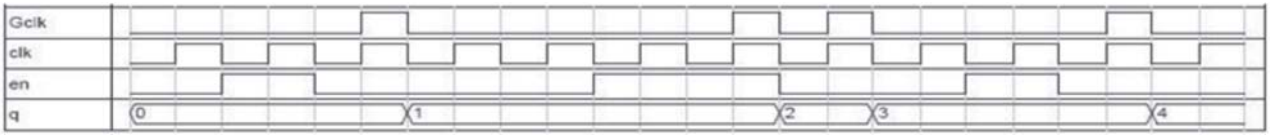

Figure 4(B): Normal output of Negative edge Counter when negative Latch based AND Gated Clock is used.

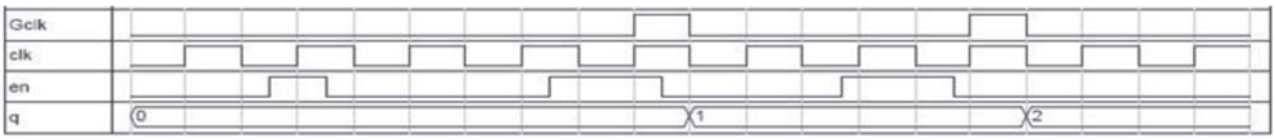

Figure 4(C): Output of negative edge counter when there are some random Hazards at En.

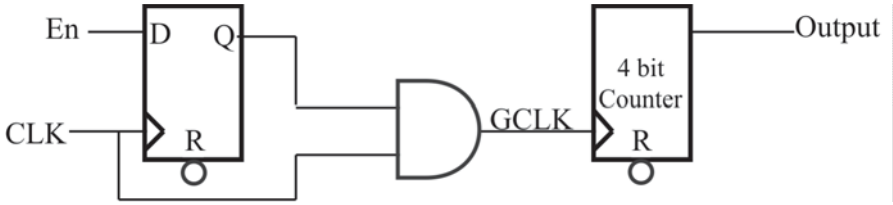

Figure 4(D): Clock gating of positive edge counter using positive Latch Based AND gate Circuit.

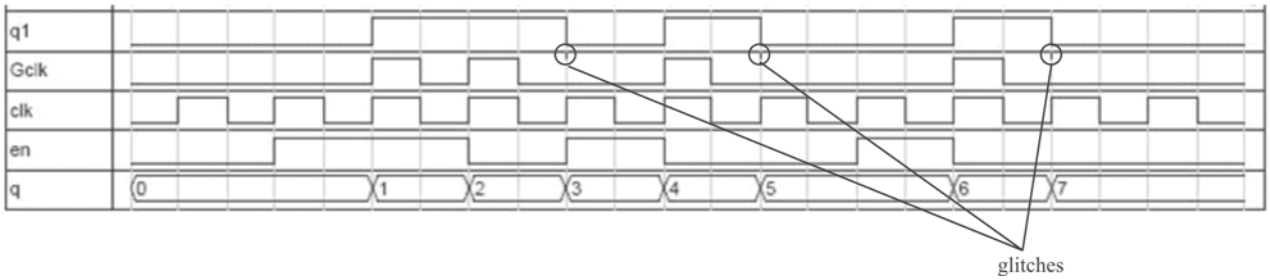

Figure 4(E): Output of counter when latch is positive and Counter also positive edge triggered.

D. LATCH BASED NOR GATE CLOCK GATING

Latch based NOR Gated Clock scheme is shown in Figure 5(A). Here enable signal is applied through latch in place of direct connection to NOR gate.

We can observe from Figure 5(B) that counter will take one extra clock cycle delay to change its state and after that it will work normally until En is de-asserted and this time also it will take one clock cycle extra to stop changing its state.

In Figure 5(C) we have verified that unwanted outputs due to Glitches at the En are avoided.

In Figure 5(E) waveform the case when controlling Latch is negative and Counter is also negative edge triggered is shown. The output of the counter is incorrect because it increments once even when enable is turned down due to a tiny glitch due to the fall time delay of enable.

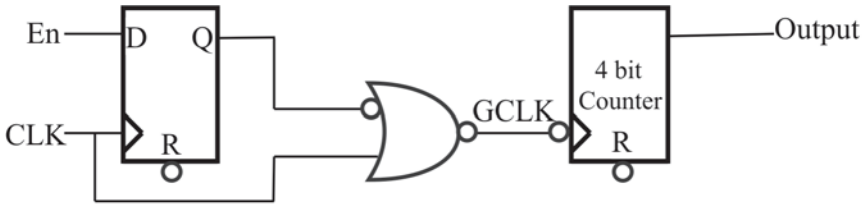

Figure 5(A): Clock gating of negative edge counter using positive Latch Based NOR gate Circuit.

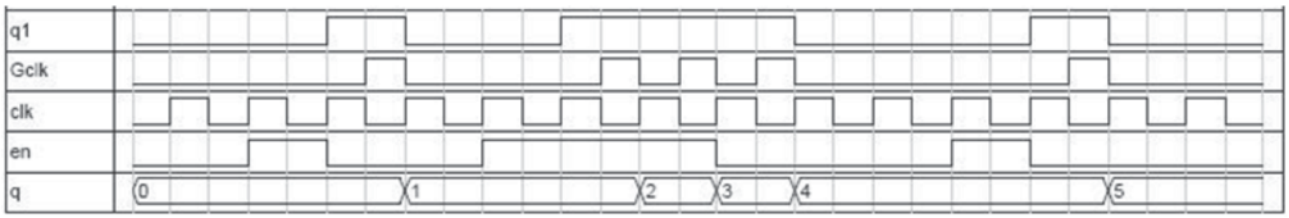

Figure 5(B): Normal output of negative edge Counter when positive Latch based OR Gated Clock is used.

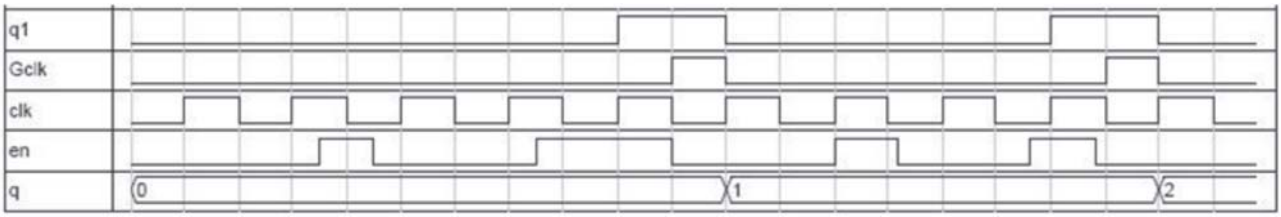

Figure 5(C): Output of negative edge counter when there are some random Hazards at En.

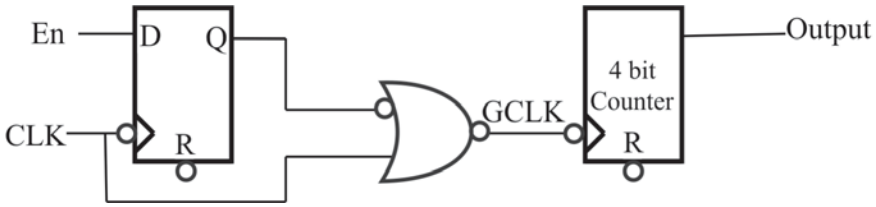

Figure 5(D): Clock gating of negative edge counter using negative Latch Based NOR gate Circuit.

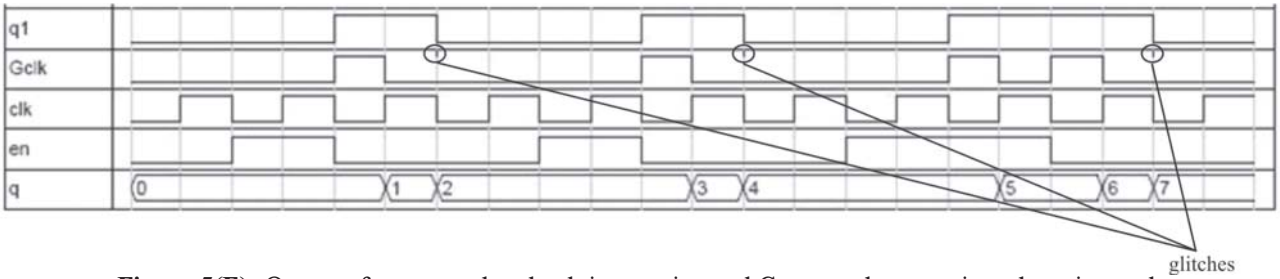

Figure 5(E): Output of counter when latch is negative and Counter also negative edge triggered.

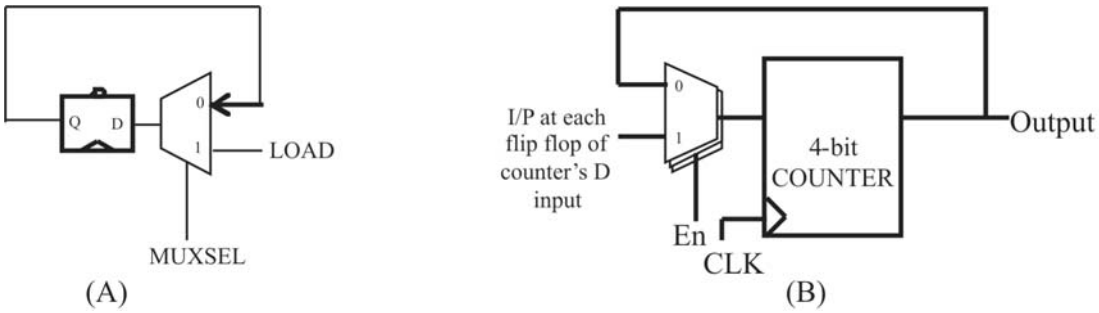

Figure 6(A): Logic of Mux Based Gated Clock. (B) Counter using Mux Based Clock Gating [4][8][12].

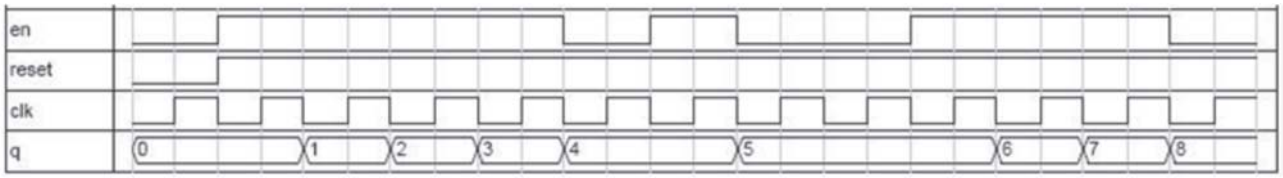

Figure 7(A): Output of Negative edge triggered Counter with Mux Based Clock Gating.

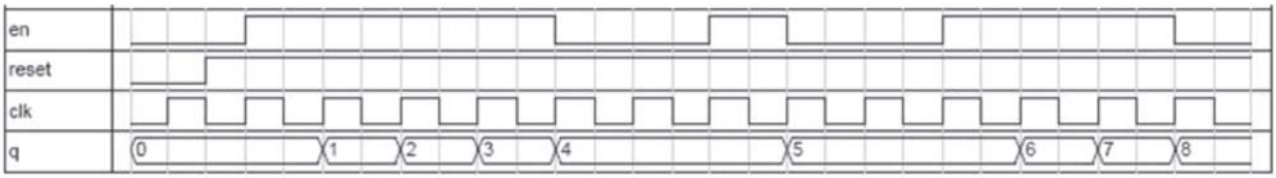

Figure 7(B): Output of Positive edge triggered Counter with Mux Based Clock Gating.

E. MUX BASED CLOCK GATING

In mux based clock gating we use multiplexer to close and open a feedback loop around a basic D-type flip-flop under control of the enable signal as shown in Figure 6(A). As the resulting circuit is simple, robust, and compliant with the rules of synchronous design this is a safe and often also a reasonable choice. On the negative side, this approach takes one fairly expensive multiplexer per bit and consumes more power. This is because any toggling of the clock input of a disabled flip-flop amounts to wasting of energy in discharging and recharging the associated node capacitances for nothing. The capacitance of the CLK input is not the only contribution as any clock edge causes further nodes to toggle within the flip-flop itself [11]. In Figure 7(A) waveform of Negative Edge triggered Counter is shown and in 7(B) Positive edge triggered. We can observe from these waveforms that when En turns ON then at each Negative and Positive Edge of the clock respectively counter increments and when En goes Low counter holds its state.

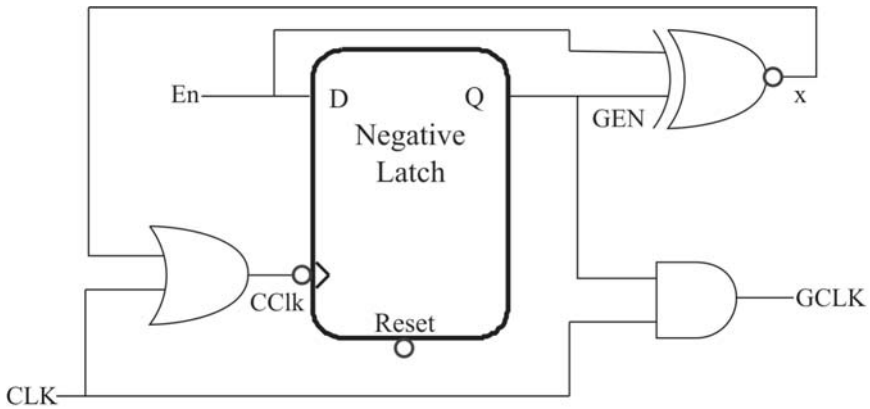

Figure 8(A): Generation of Gated Clock When Negative Latch is used [14].

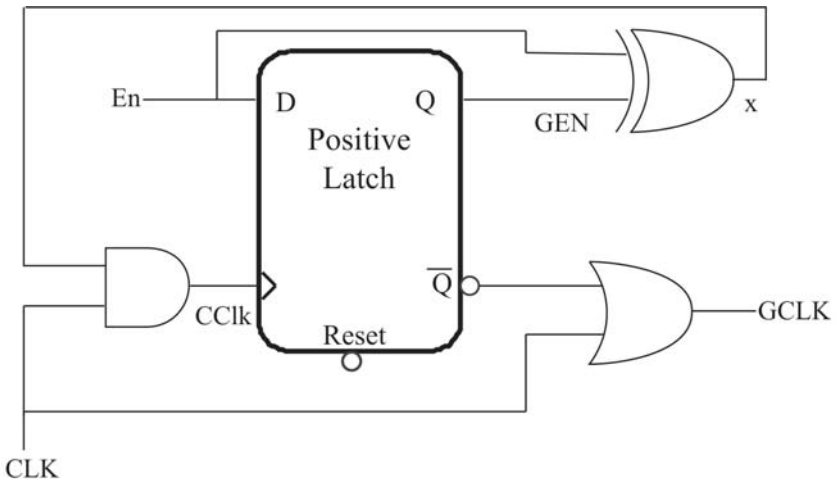

Figure 8(B): Generation of Gated Clock When Positive Latch is used [14].

F. NEW APPROACH FOR CLOCK GATING

In this section, we will discuss a new design that will save more power.

The new Gated Clock Generation Circuit is shown in Figure 8(A) and 8(B) using negative latch and positive latch respectively. This circuit saves power in such a way that even when Target device's clock is ON, the controlling device's clock is OFF and also when the target device's clock is OFF then also Controlling device's clock is OFF. This way we can save more power by avoiding unnecessary switching at clock net [14].

To understand the working of circuit consider Figure 8(A), an input signal named 'En' is provided to the latch. When En turns to '1' at that time GEN is '0' , XNOR will produce x='0' which goes to the first clock generation logic that generates clock for controlling device (LATCH). In first logic we have an OR gate which have Global Clock as an input at the other input of OR gate. This logic will generate a clock pulse that will drive the controlling latch when 'x' turns to '0'.

In the next clock pulse, when GEN turns to '1' our second clock generation logic which is an AND gate which has GEN and Global clk at its input and when Gen goes '1' it generates clock pulse that goes to the target device. Since GEN is '1' the XNOR will produce x='1' thus OR will produce at CClk constant HIGH until En turns to '0'. This way GClk will be running and CClk will be at Constant '1' state that means latch will hold its state without any switching.

The circuit shown in figure 8(B) performs similar sequence of operations as explained for the circuit shown in figure 8(A). When En turns to '1' at that time GEN is '0' so XOR will produce x='1' which goes to the first clock generation logic that generates clock for controlling device (LATCH). In first logic we have an AND gate, which have Global Clock as an input at the other input of AND gate. This logic will generate a clock pulse that will drive the controlling latch when 'x' turns to '1'. In the next clock pulse, when GEN turns to '1' our second clock generation logic which is an OR gate which has Q and Global clock at its input and when Q goes '0' it generates clock pulse that goes to the target device. Since GEN is '1' the XOR will produce x='0' thus OR will produce at CClk constant LOW until En turns to '0'. This way GClk will be running and CClk will be at Constant '0' state that means latch will hold its state without any switching.

The output of Counter for circuit as in Figure 8(A) is shown in Figure 9(A & B). In Figures 9(A) and 9(B) enable changes from negative edge to next negative edge and positive edge to next positive edge respectively and also target is negative edge triggered and positive edge triggered respectively. However, in both cases counter's state changing delay is different but output is correct which gives us solution of the problem that persists in first four types of clock gating.

The output of Counter for circuit as in Figure 8(B) is shown in Figure 10(A & B). In figure 10(A) and 10(B) enable changes from negative edge to next negative edge and positive edge to next positive edge respectively and also target is negative edge triggered and positive edge triggered respectively. However, in both cases counter's state changing delay is different but output is correct which gives us solution of the problem that persists in first four types of clock gating.

Thus one can avoid more switching and can save power.

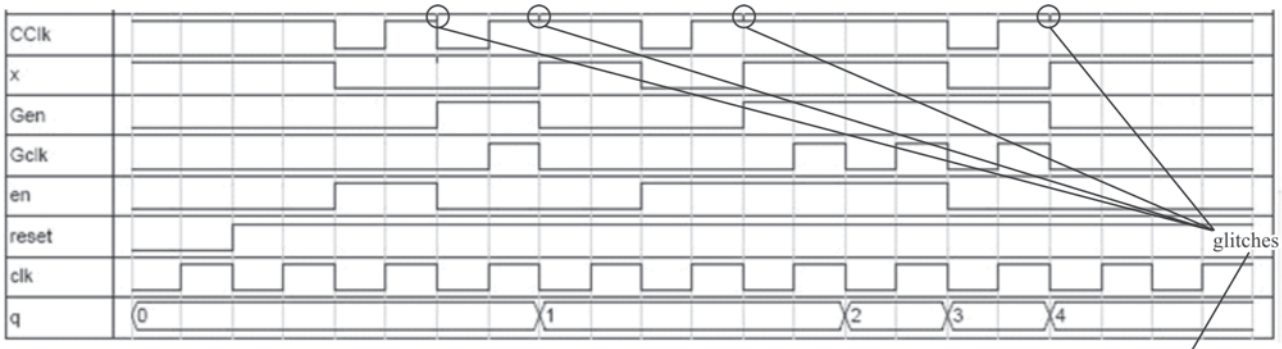

Figure 9(A): Output of negative edge Counter with gated clock for circuit shown in Fig. 8(A).

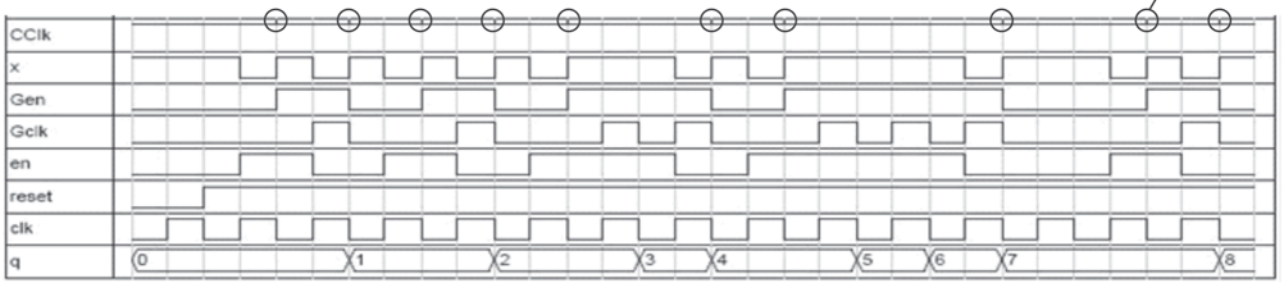

Figure 9(B): Output of positive edge Counter with gated clock for circuit shown in Fig. 8(A).

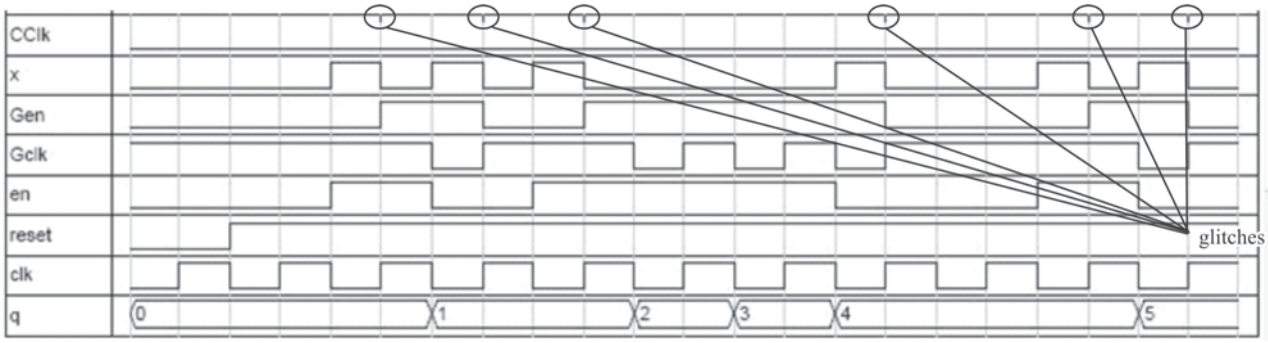

Figure 10(A): Output of negative edge Counter with gated clock for circuit shown in Fig. 8(B).

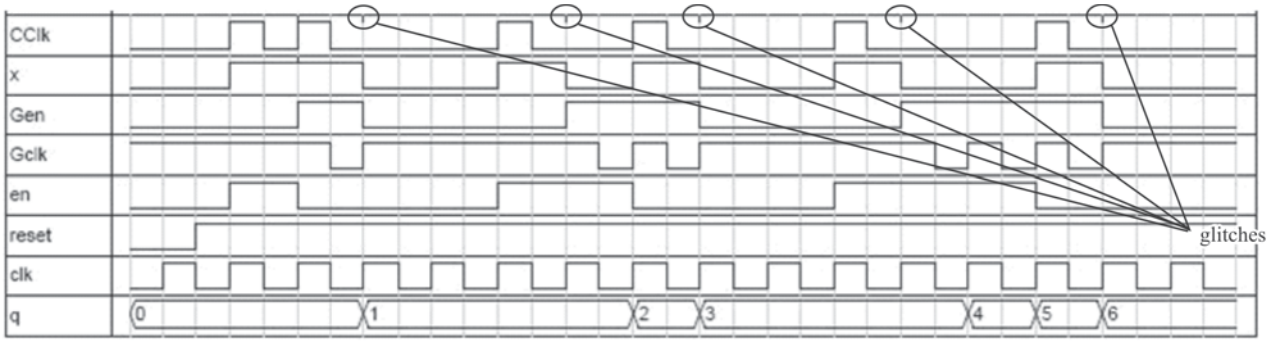

Figure 10(B): Output of positive edge Counter with gated clock for circuit shown in Fig. 8(B).

III. Conclusion

This paper has described five available techniques of clock gating. In first two techniques, AND and NOR based clock gating, we have output correctness problem due to Glitches and Hazards. Where in Latch based AND and NOR techniques Hazards problem is removed, however Glitches problem still exists in them. In fifth technique we does not have these problem but still we cannot consider it very good power saving technique. In new technique Glitches and Hazards problem

is resolved due to the clock gating applied at controllers side and also at target side and this techniques saves more power than any other technique.

References

[1] L. Benini, G. De Micheli, E. Macii, M. Poncino, and R. Scarsi, "Symbolic Synthesis of Clock-Gating Logic for Power Optimization of Synchronous Controllers," ACM Trans. Des. Autom. Electron, Oct. 1999.

[2] D. Dobberpuhl, R. Witek, "A 200MHz 64b Dual-Issue CMOS Microprocessor," IEEE International Solid-State Circuits Conference, pp. 106-107, 1992.

[3] Vishwanadh Tirumalashetty, Hamid Mahmoodi, "Clock Gating and Negative Edge Triggering for Energy Recovery Clock," ISCAS 2007, New Orleans, LA, pp. 1141-1144, 2007.

[4] Safeen Huda, Muntasir Mallick, Jason H. Anderson, "Clock Gating Architectures For FPGA Power Reduction", FPL 2009.

[5] P.J. Shoenmakers, J.F.M. Theeuwen, "Clock Gating on RT-Level VHDL", Proc. of the int. Workshop on logic synthesis, Tahoe City, CA, pp. 387-391, June 7-10,1998.

[6] Frank Emnett, Mark Biegel, "Power Reduction Through RTL Clock Gating," SNUG San Jose, 2000.

[7] Mitch Dale, "Utilizing Clock-Gating Efficiency To Reduce Power", EE Times India, January 2008.

[8] Takeshi Kitahara, Fumihiro Minami, Toshiaki Ueda, Kimiyoshi Usami, Seiichi Nishio, Masami Murakata, Takashi MitsuhashiA, "Clock-Gating Method for Low-Power LSI Design", TOSHIBA Corporation.

[9] Gary K. Yeap, "Practical Low-Power Digital VLSI Design", Kluwer Publishing, 1998.

[10] Frederic Rivoallon, "Reducing Switching Power With Intelligent Clock Gating", Xillix WP370 (V1.2), October 5, 2010.

[11] Hubert Kaeslin, ETH Zurich, "Digital Integrated Circuit Design from VLSI Architectures to CMOS Fabrication," Cambridge University Press, 2008.

[12] Vojin G. Oklobdzjja, Vladlmlr M. Stojanovic, Dejan M. Markovic, Nikola M. Nedovic, "DIGITAL SYSTEM CLOCKING High-Performance and Low-Power Aspects," Wiley Interscience, U.S., 2003.

[13] John F. Wakerly, "Digital Design Principles and Practices", Prentice Hall, 2005.

[14] Patent, US20100109707, http://www.freepatentsonline.com/y2010/0109707.html, accessed on 26 February 2011.