C²MOS™ LOGIC IC
Product Guide
HC Series

Description

This document describes the product outline of the C²MOS™ LOGIC IC (HC series).

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1. General

1.1. General

This document describes the HC series of C²MOS™ Logic ICs.

The HC series is indicated by the red frame in Figure 1.1.

This series realizes high-speed switching by CMOS fine processing technology and is widely used under the 5 V condition.

In the case of analog multiplexer ICs (HC4051, HC4052, HC4053), the amplitude of control signal is between V_{CC} and GND, and the amplitude of analog signal is between V_{CC} and V_{EE}.

The package lineup is wide, from DIP package to TSSOP package.

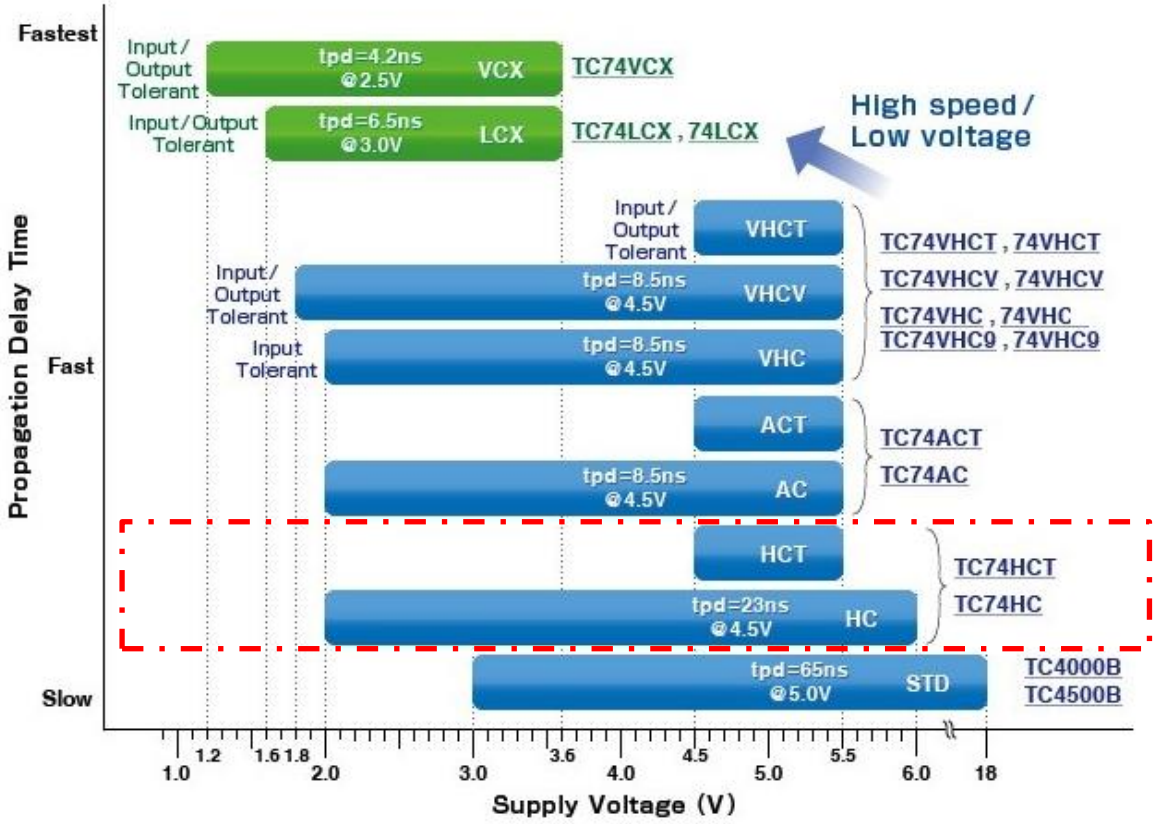


Figure 1.1 Supply Voltage Range and Propagation Delay Time of Each Series

1.2. Features

1.2.1. Interface Capability

The HC series adopts an input protection circuit with diode from input terminal to power supply side. Therefore, please use this series within the supply voltage.

The diode is eliminated in the case of the HC4049 and HC4050, and thus they can convert voltage level from high-level voltages (up to 15 V) to V_{CC}.

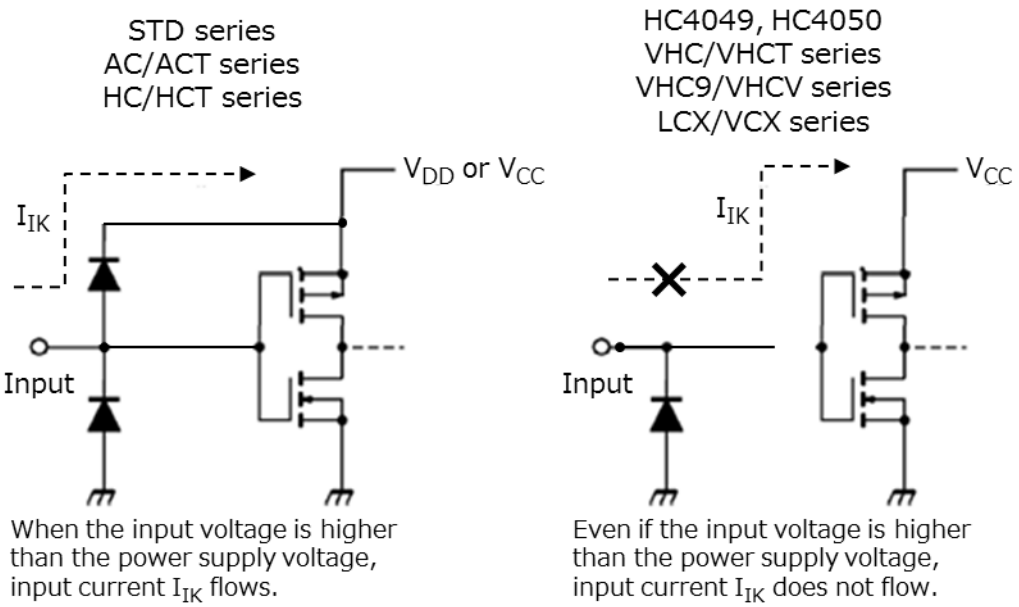


Figure 1.2 Input Equivalent Circuit for Each Series

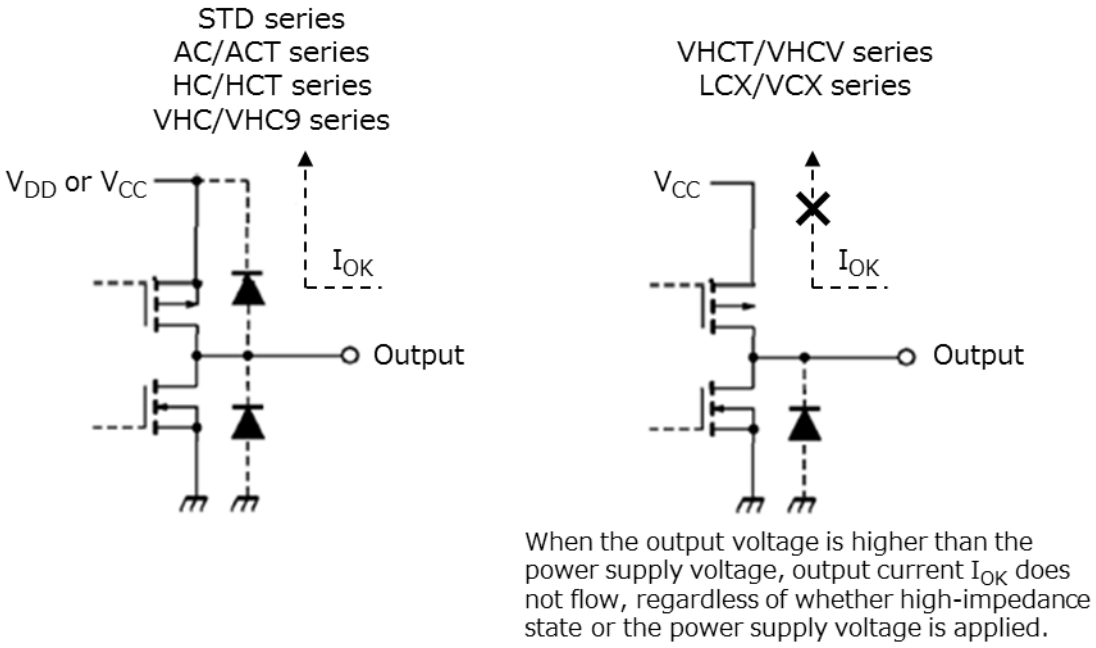


Figure 1.3 Output Equivalent Circuit for Each Series

Table 1.1 Voltage Applicable to I/O Terminals

	HC / HCT
Input Voltage Range	
(Operation)	0 to V_{CC}
(Power Down)	0 (Note 1)
Output Voltage Range	
(Output Enable)	0 to V_{CC}
(Output Disable)	0 to V_{CC}
(Power Down)	0 (Note 1)

Note 1: Voltage cannot be applied.

1.2.2. Standard Output Current

Standard-type: ±4 mA @V_{CC} = 4.5 V

Buffer-type: ±6 mA @V_{CC} = 4.5 V

2. Method of Designating CMOS Logic ICs

2.1. Part Naming Conventions

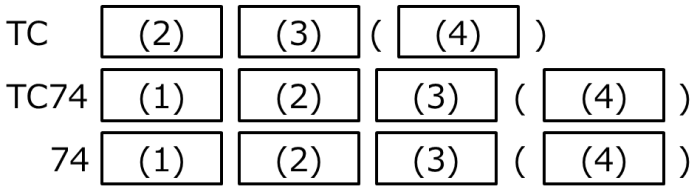


Figure 2.1 Part Naming Conventions

(1) Series, (2) Function, (3) Package, (4) Packing Method

(Example) TC74VCX08FT(EL)

(1) VCX Series, (2) 08 Function, (3) Plastic TSSOP Package, (4) Embossed tape and reel

(1) Series Definition

Table 2.1 shows each series and the input level.

Table 2.1 Series Definition

Series	Definition
Blank	STD series
HC	CMOS level input of HC series
HCT	TTL level input of HC series
AC	CMOS level input of AC series
ACT	TTL level input of AC series
VHC	CMOS level input of VHC series
VHCT	TTL level input of VHC series
VHC9	Schmitt circuit-type input of VHC series
VHCV	Schmitt circuit-type input of VHC series Capable of handling twice as much output current as other products in VHC series.
LCX	TTL level input of LCX series
VCX	TTL level input of VCX series

(2) Function

The function number is represented by 2 to 8 alphanumeric characters.

Function numbers are common for all series.

(3) Package Type

Package classification is common for all series.

P・・・	Dual in-line package (DIP)	14/16/20 pin
F・・・	200-mil small-outline package (SOP)	14/16/20 pin
D・・・	150-mil small-outline package (SOIC)	14/16/20 pin
FT・・・	Thin shrink small-outline package (TSSOP)	14/16/20/48 pin
FK・・・	300-mil small-outline package (US)	14/16/20 pin

(4) Packing Method

Please refer to the Toshiba web page. (URL: https://toshiba.semicon-storage.com/ap-en/top.html)

3. Explanation of Ratings and Standards

The tables below show common ratings and electrical characteristics for the HC/HCT series. When the ratings and electrical characteristics are different from those of individual data sheets, the latter take precedence.

For the meanings of the parameters, please refer to the glossary at the end of this document.

3.1. Absolute Maximum Ratings

In general, absolute maximum rating values should not be exceeded, in order to guarantee the life and reliability of integrated circuit products.

Absolute maximum ratings should not be exceeded, even for a moment.

When a device is used in excess of any absolute maximum rating, it may not recover, and in many cases, permanent damage will occur.

Table 3.1 shows the common absolute maximum ratings for the HC/HCT series.

Table 3.1 Absolute Maximum Rating

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to V_{CC}+0.5	V
DC output voltage	V_{OUT}	-0.5 to V_{CC}+0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25 (Standard-type) ±35 (Buffer-type)	mA
DC V_{CC}/ground current	I_{CC}	±50 (Standard-type) ±75 (Buffer-type)	mA
Power dissipation	P_D	500 (DIP) (Note 1) 180 (Other)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

3.2. Operating Ranges

These are the conditions under which the operation of HC/HCT series devices is guaranteed. When any of these values is exceeded, operation is not guaranteed, even if the value is still within the absolute maximum rating in Table 3.1.

Unused input terminals must be connected to either V_{CC} or GND.

Tables 3.2 and 3.3 show the common operating ranges for the HC/HCT series.

3.2.1. HC Series

Table 3.2 Operating Ranges (HC Series)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85 (Note 1) -40 to 125 (Note 1)	°C
Input rise and fall time	t_r, t_f	0 to 1000 (Note 2) 0 to 500 (Note 3) 0 to 400 (Note 4)	ns

Note 1: Different by products

Note 2: V_{CC} = 2.0 V

Note 3: V_{CC} = 4.5 V

Note 4: V_{CC} = 6.0 V

3.2.2. HCT Series

Table 3.3 Operating Ranges (HCT Series)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85 (Note 1) -40 to 125 (Note 1)	°C
Input rise and fall time	t_r, t_f	0 to 500 (Note 2)	ns

Note 1: Different by products

Note 2: V_{CC} = 4.5 V

3.3. DC Characteristics

Tables 3.4 and 3.5 show DC characteristics for the HC/HCT series.

3.3.1. HC Series

Table 3.4 Characteristics (HC Series)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	-	2.0 4.5 6.0	1.5 3.15 4.2	- - -	- - -	1.5 3.15 4.2	- - -	V
Low-level input voltage (Note 2)	V_{IL}	-	2.0 4.5 6.0	- - -	- - -	0.5 1.35 1.8	- - -	0.5 1.35 1.8	
High-level output voltage (Note 2)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	- - -	1.9 4.4 5.9	- - -	V
			I_{OH} = -4 mA (Note 1) I_{OH} = -5.2 mA (Note 1)	4.5 6.0	4.18 5.68	4.31 5.80	- -	4.13 5.63	- -	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0 4.5 6.0	- - -	0.0 0.0 0.0	0.1 0.1 0.1	- - -	0.1 0.1 0.1	
			I_{OL} = 4 mA (Note 1) I_{OL} = 5.2 mA (Note 1)	4.5 6.0	- -	0.17 0.18	0.26 0.26	- -	0.33 0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent supply current (Note 2)	I_{CC}	V_{IN} = V_{CC} or GND		6.0	-	-	4.0	-	40.0	μA

Note 1: For buffer-type products, multiply this value by 1.5. (|IOH|=IOL=6 mA, 7.8 mA)

Note 2: Items guaranteed to meet JEDEC Standard 7A

3.3.2. JEDEC Standard

Table 3.5 JEDEC Standard (JEDEC Standard No.7A)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = -40 to 85°C Min	Ta = -40 to 85°C Max	Unit
High-level input voltage	V_{IH}	-		2.0 4.5 6.0	1.5 3.15 4.2	- - -	- - -	1.5 3.15 4.2	- - -	V
Low-level input voltage	V_{IL}	-		2.0 4.5 6.0	- - -	- - -	0.3 0.9 1.2	- - -	0.3 0.9 1.2	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0 4.5 6.0	1.9 4.4 5.9	- - -	- - -	1.9 4.4 5.9	- - -	V
			I_{OH} = -4 mA (Note 1) I_{OH} = -5.2 mA (Note 1)	4.5 6.0	3.98 5.48	- -	- -	3.84 5.34	- -	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0 4.5 6.0	- - -	- - -	0.1 0.1 0.1	- - -	0.1 0.1 0.1	
			I_{OL} = 4 mA (Note 1) I_{OL} = 5.2 mA (Note 1)	4.5 6.0	- -	- -	0.26 0.26	- -	0.33 0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	-	-	8.0	-	80.0	μA

Note 1: For buffer-type products, multiply this value by 1.5. (|IOH|=IOL=6 mA, 7.8 mA)

4. Explanation of Symbols Used in Data sheets

4.1. How to Read a Truth Table

Table 4.1 Definition of Symbols Used in Truth Tables

SYMBOL	DEFINITION
H	High level (indicates stationary input or output)
L	Low level (indicates stationary input or output)
⎍	Indicates leading edge changing from L to H.
⎎	Indicates leading edge changing from H to L.
X	Don't care (either H or L)
Z	High-impedance state
a···h	The level of the parallel inputs A to H (either H or L).
Q0	Level of Q just before input condition indicated in truth table
Qn	Level of Q just before input active edge (⎍ or ⎎)
⎍⎍	One H-level pulse
⎎⎎	One L-level pulse

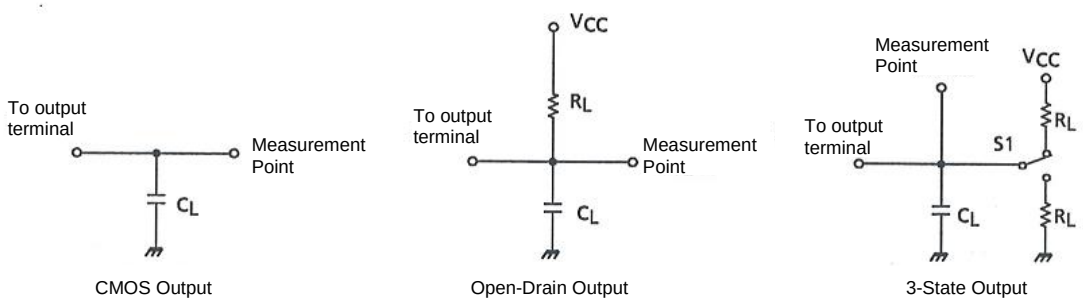
4.2. AC Characteristics

The AC characteristics of datasheets specify the transient characteristics.

Figure 4.1 shows measuring circuit. Figures 4.2 and 4.3 show I/O switching waveforms.

(Condition of input waveform: An amplitude range is between V_{CC} and GND, and rise and fall times are 6 ns.)

To ensure normal functioning of the device, the following timings must be adhered to.

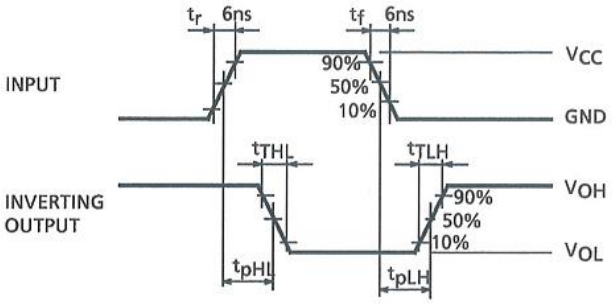


Note: C_L includes the probe capacitance.

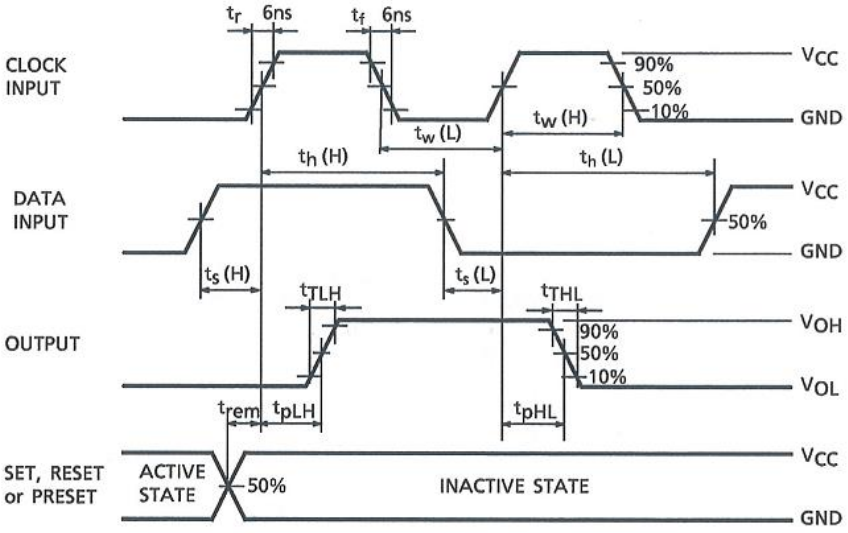
Figure 4.1 Measuring Circuit of Output

4.2.1. I/O Switching Waveforms of HC Series

1) t_{pLH},t_{pHL}



2) t_w, t_s, t_h, t_{rem}



3) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

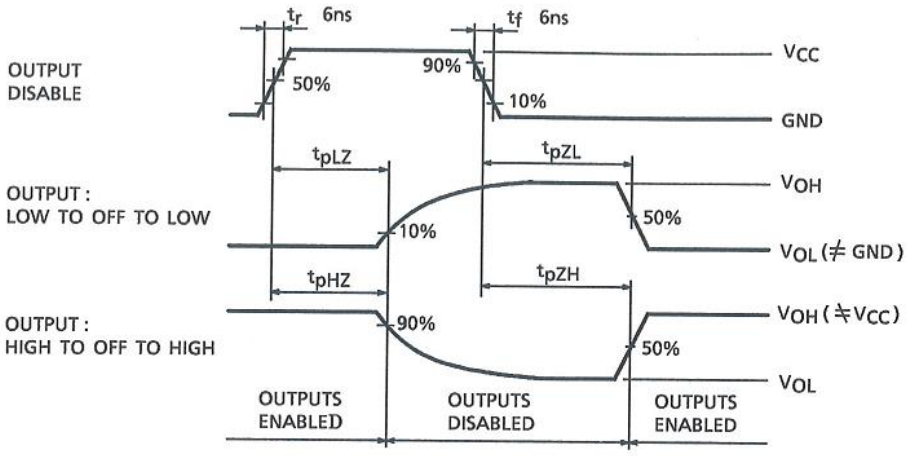
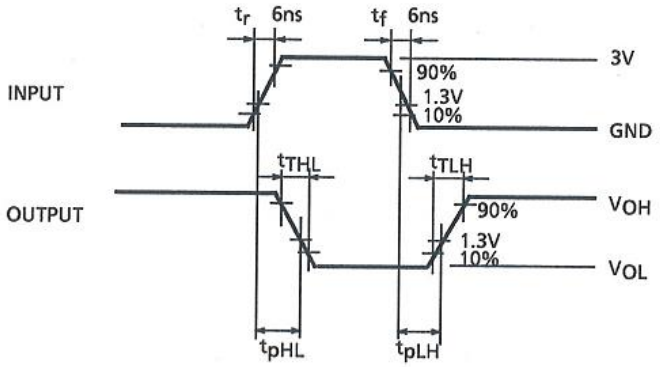


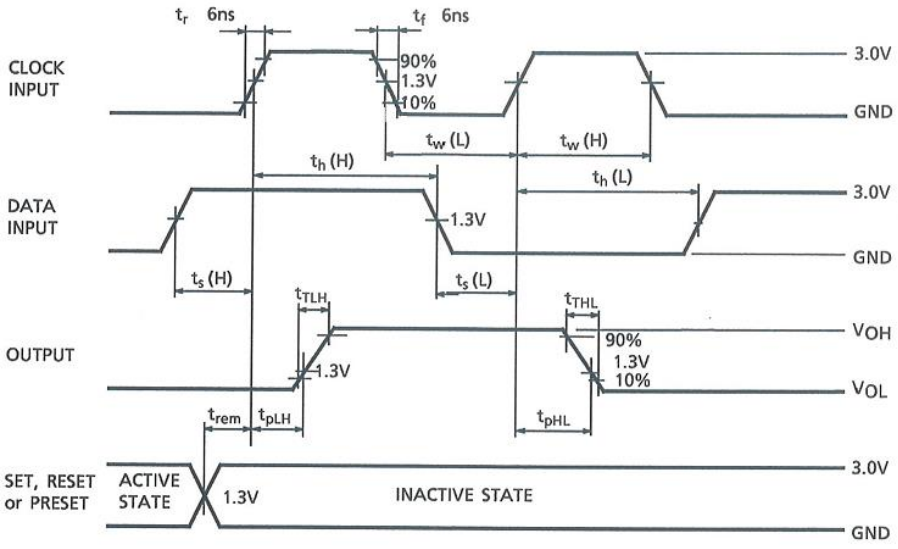
Figure 4.2 I/O Switching Waveforms of HC Series

4.2.2. I/O Switching Waveforms of HCT Series

1) t_{pLH},t_{pHL}



2) t_w, t_s, t_h, t_{rem}



3) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

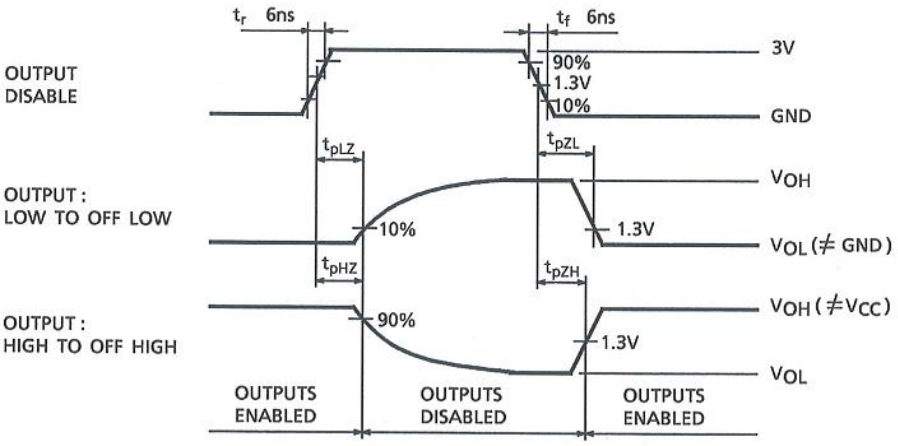


Figure 4.3 I/O Switching Waveforms of HCT Series

4.3. Standardized Test Procedure for Power Dissipation Capacitance

Measurements for all devices are under the conditions of "V_{CC} = 5 V" and "Ta = 25 deg C". And a relatively high frequency, about 1 MHz, is used for measurement of power consumption, because if a device is tested at a high enough frequency, the contribution of the DC supply current to the overall power consumption will be negligible and can be ignored. Devices with 3-state outputs are measured in the enabled state.

In the case of devices that have several circuits in the same package (e.g., HC04: Hex inverter, HC74: Dual D-F/F etc.), only one circuit is measured and the result is shown on the data sheet as the C_{pd} per circuit.

In the case of devices that contain several circuits in the same package operating simultaneously from the same clock signal (e.g., HC174A: HEX D-F/F etc.), the C_{pd} can be obtained by measuring either the C_{pd} of the device with only one output active, or the C_{pd} with all device outputs active.

The pin states for each IC are listed in the table.

C_{PD} Measuring Condition

Table 4.2 C_{PD} Measuring condition

Type No.		Pin No. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
00		P	H	O	X	X	O	G	O	X	X	O	X	X	V										
02		O	P	L	O	X	X	G	X	X	O	X	X	O	V										
03		P	H	R	X	X	O	G	O	X	X	O	X	X	V										
04		P	O	X	O	X	O	G	O	X	O	X	O	X	V										
05		P	R	X	O	X	O	G	O	X	O	X	O	X	V										
07		P	R	X	O	X	O	G	O	X	O	X	O	X	V										
08		P	H	O	X	X	O	G	O	X	X	O	X	X	V										
14		P	O	X	O	X	O	G	O	X	O	X	O	X	V										
20		P	H	O	H	H	O	G	O	X	X	O	X	X	V										
21		P	H	O	H	H	O	G	O	X	X	O	X	X	V										
32		P	L	O	X	X	O	G	O	X	X	O	X	X	V										
42		O	O	O	O	O	O	O	G	O	O	O	L	L	L	P	V								
74		H	Q	P	H	O	O	G	O	O	X	X	X	X	V										
86		P	L	O	X	X	O	G	O	X	X	O	X	X	V										
123		L	H	P	O	O	O	O	G	X	X	X	O	O	O	R	V								
125		H	P	O	X	X	O	G	O	X	X	O	X	X	V										
126		H	P	O	X	X	O	G	O	X	X	O	X	X	V										
132		P	H	O	X	X	O	G	O	X	X	O	X	X	V										
138		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V								
139		L	P	L	O	O	O	O	G	O	O	O	O	X	X	X	V								
151		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V								
153		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V								
157	1*	P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V								
157	4*	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V								
164		Q	H	O	O	O	O	G	P	H	O	O	O	O	V										
165		H	P	X	X	X	X	O	G	O	Q	X	X	X	X	L	V								
166		Q	X	X	X	X	L	P	G	H	X	X	X	O	X	H	V								
174	1*	H	O	Q	X	O	X	O	G	P	O	X	O	X	X	O	V								
174	6*	H	O	Q	Q	O	Q	O	G	P	O	Q	O	Q	Q	O	V								
175	1*	H	O	O	Q	X	O	O	G	P	O	O	X	X	O	O	V								
237		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V								
238		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V								
240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V				
241		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V				
244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V				
245		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
251		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V								
253		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V								
259		L	L	L	O	O	O	O	G	O	O	O	O	Q	P	H	V								
273	1*	H	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V				
273	8*	H	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V				
365		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V								
366		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V								
373	1*	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V				
373	8*	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V				
374	1*	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V				
374	8*	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V				
393		P	L	O	O	O	O	G	O	O	O	O	X	X	V										

*: Number of active outputs

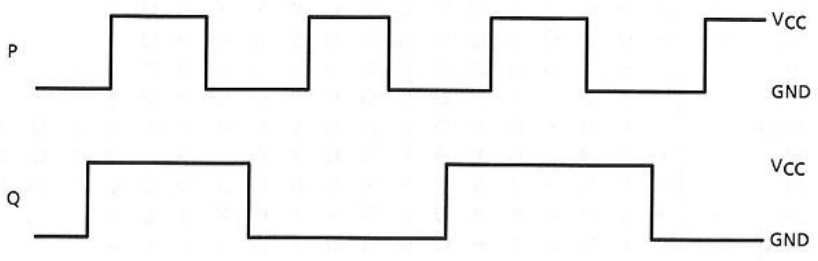
Table 4.3 C_{PD} Measuring Condition (Continued)

Type No.		Pin No. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
423		L	P	H	O	O	O	O	G	X	X	X	O	O	O	R	V								
540	1*	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
540	8*	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V				
541	1*	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
541	8*	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V				
573	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V				
573	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V				
574	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V				
574	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V				
594		O	O	O	O	O	O	O	O	O	H	P	P	H	Q	O	V								
595		O	O	O	O	O	O	O	G	O	H	P	P	L	Q	O	V								
640		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V				
4020		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V								
4040		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V								
4049		V	O	P	O	X	O	X	G	X	O	X	O	O	X	O	O								
4050		V	O	P	O	X	O	X	G	X	O	X	O	O	X	O	O								
4051		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V								
4052		O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V								
4053		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V								
4060		O	O	O	O	O	O	O	G	O	O	P	L	O	O	O	V								
4066		O	O	O	O	X	X	G	O	O	O	O	X	P	V										
4538		G	R	H	P	H	O	O	G	O	O	X	X	L	O	G	V								
7007		P	O	X	O	X	O	G	O	X	O	X	O	X	V										
7240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V				
7244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V				
7292		H	L	O	P	L	O	O	G	O	L	H	O	O	L	L	V								

*: Number of active outputs

-Explanation of symbols-

V = V_{CC} (+5.0 V)
G = GND (0 V)
H = Logic 1 (V_{CC})
L = Logic 0 (GND)
X = Don't care. V_{CC} or GND (but not switching)
R = 1.0 kΩ pull-up resistor connected between the IC and a 5-V power supply other than V_{CC}.
O = Open
P = 50% duty cycle input pulse (shown below)
Q = 50% duty cycle half-frequency out-of-phase input pulse (shown below)



Input Pulse Waveforms

5. Other Electrical Characteristics

5.1. Power Dissipation

The power dissipation is given by the sum of the quiescent supply current and the dynamic operating current. Therefore, it can be obtained from the following equation:

$$P_D = C_{PD} \cdot f_{IN} \cdot V_{CC}^2 + C_L \cdot f_{OUT} \cdot V_{CC}^2 + I_{CC} \cdot V_{CC}$$

C_{PD} : Power Dissipation Capacitance

C_L : Load Capacitance

f_{IN} : Input Frequency

f_{OUT} : Output Frequency

In the case of CMOS ICs, if inputs are held at V_{CC} or GND, either the N-ch MOS or the P-ch MOS turns off. As a result, the quiescent supply current from V_{CC} to GND is just a few nA at room temperature.

Therefore, the quiescent supply current increases in direct proportion to the power supply voltage and increases exponentially with the temperature.

The dynamic power dissipation of CMOSs IC is calculated by summing the switching currents and the through currents. The switching currents are due to the charging and discharging of each gate capacitance, when the gate in the circuit that includes the output buffer inverts, and the through currents flow from V_{CC} to GND when the P-ch MOS and the N-ch MOS that constitute the gate turn on briefly at the same time during inversion time.

When the rise and fall times of the input signal are small (a few ns), the through current in the gate is negligible compared with the switching current. Thus, the dynamic supply current is determined by the internal capacitance of the IC and the charging and discharging currents of the load capacitance (C_L).

However, in specific applications such as crystal oscillators, supply current characteristics depend on the through current, and the result calculated using C_{PD} cannot be used.

5.2. Output Current Characteristics

The output current characteristics of the HC series can be divided into standard and buffer-types. An IC of the standard-type is capable of directly driving 10 LSTTL, and it is guaranteed that V_{CC}-V_{OH} ≦ 0.37 V, V_{OL} ≦ 0.33 V within the entire operating temperature range. The buffer-type is capable of directly driving 15 LSTTL under the same conditions.

Figures 5.1 and 5.2 show the standard output current characteristics for each type when used at 4.5 V.

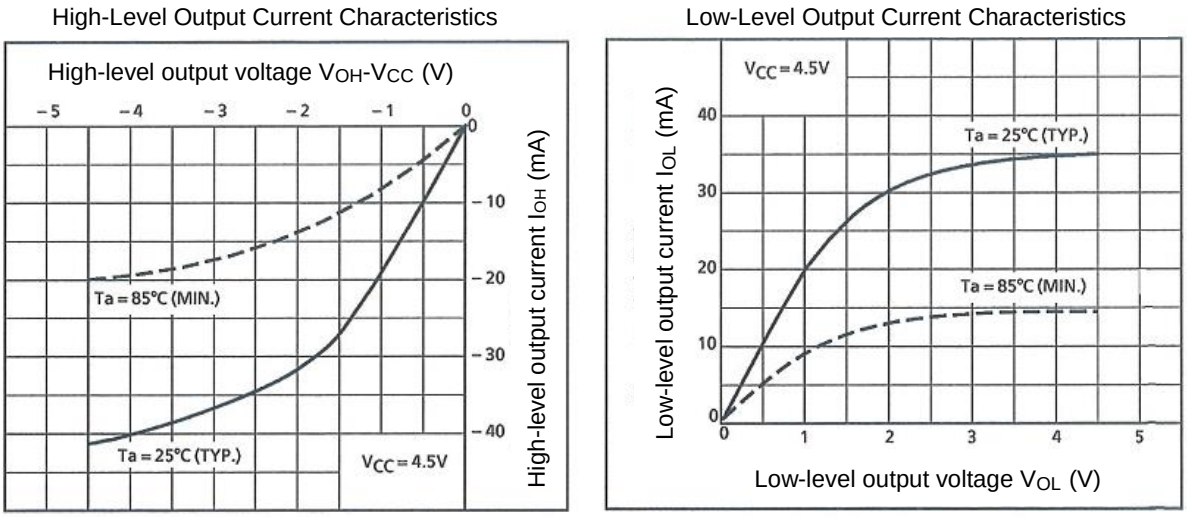


Figure 5.1 Standard Output Current (Standard-type)

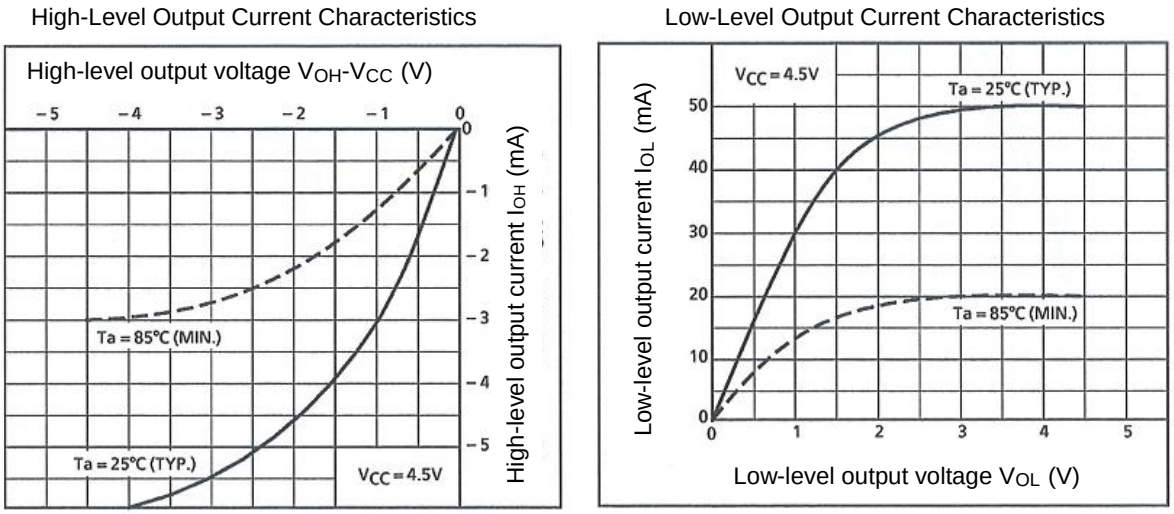


Figure 5.2 Standard Output Current (Buffer-type)

Note: When designing circuits, refer to the dotted-line characteristic and the individual product datasheet, so as to take account of variations within product samples.

The current flowing in a MOSFET is determined by the gate voltage V_{GS} and the voltage V_{DS} between the source and drain. In the actual IC, the gate voltage of the output stage MOSFET becomes almost V_{CC} or almost GND. Therefore, if $|V_{GS}| = V_{CC}$, the following equation is valid for the non-saturation zone:

$$I_{DS} = K\left[2V_{DS}(V_{GS} - V_T) - {V_{DS}}^2\right]$$

If V_{DS} is kept constant, I_{DS} is proportional to V_{CC}-V_T.

For the saturation zone:

$$I_{DS} = K(V_{GS} - V_T)^2$$

Thus, I_{DS} is proportional to $(V_{CC}\text{-}V_T)^2$, not to V_{DS}. Here V_T is the threshold voltage for MOSFETs and is set to a value of about 0.7 V for the HC series.

Figure 5.3 shows supply voltage-output current characteristics for standard-type outputs. This figure shows standard values.

Note: The variation in output current at low supply voltages is large compared with that at 4.5 V.

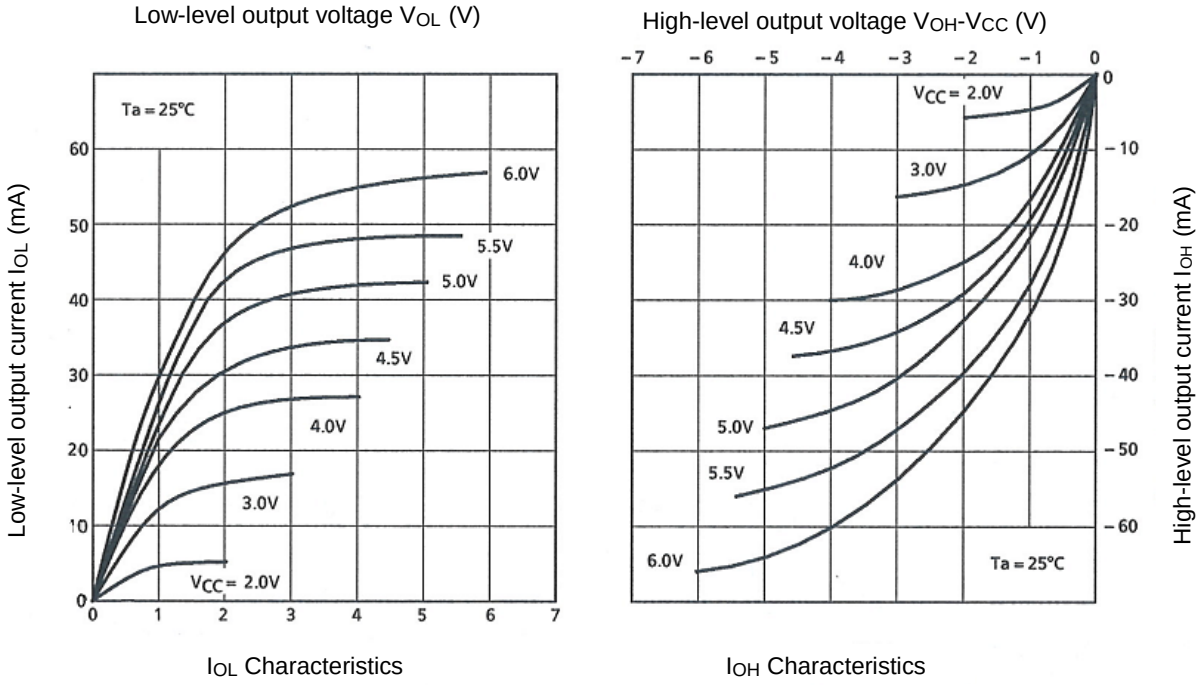


Figure 5.3 Standard Output Current Characteristics

5.3. AC Electrical Characteristics

5.3.1. Capacitive Loading Effects

For the HC series, output current has been greatly improved compared to the conventional 4000B/4500B series, and a capacitive load can be driven at high speed. However, when the output impedance is determined by selection of the supply voltage, the output waveform rise and fall times and the propagation delay time depend only on the load capacitance. Thus, these will increase in proportion to any increase in the load capacitance.

Figure 5.4 indicates the dependence of the load capacitance on the output rise and fall times at a supply voltage of 4.5 V.

Figure 5.5 shows the dependence of the load capacitance on the propagation delay time.

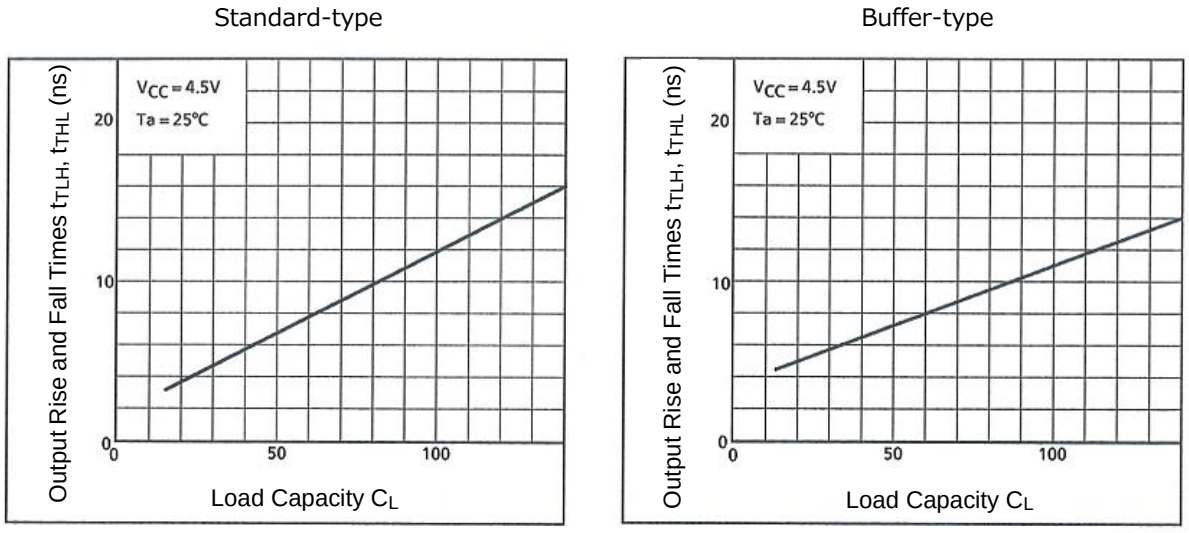


Figure 5.4 Dependence of Load Capacitance on t_{TLH}, t_{THL}

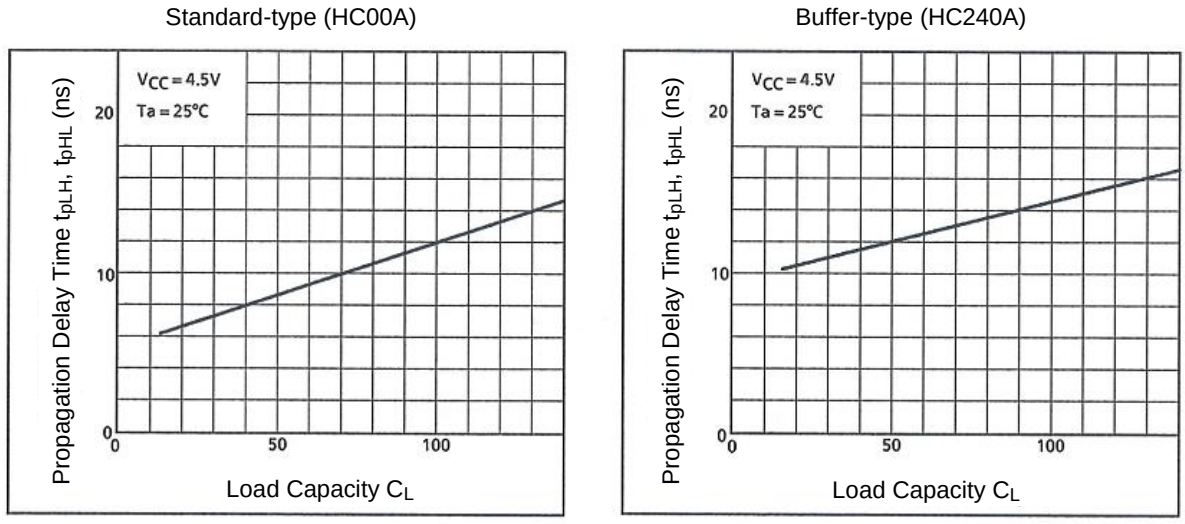


Figure 5.5 Dependence of Load Capacitance on t_{pLH}, t_{pHL}

6. Glossary of CMOS Logic IC Terms

6.1. Absolute Maximum Ratings

Parameter	Symbol	Definition
Supply voltage	V_{DD} - V_{SS} V_{CC}	The rated voltage of the power supply terminal at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Supply voltage	V_{DD} - V_{EE} V_{CC} - V_{EE}	The rated voltage across the V_{CC}, V_{DD} and V_{EE} terminals at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Input voltage	V_{IN}	The rated voltage of the input terminal at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Output voltage	V_{OUT}	The rated voltage of the output terminal at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Switch I/O voltage	$V_{I/O}$	The rated voltage across the input and output terminals at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
Input diode current	I_{IK}	The rated current of the input terminal at which an IC will not suffer breakdown due to latch-up.
Output diode current	I_{OK}	The rated current of the output terminal at which an IC will not suffer breakdown due to latch-up.
Output current	I_{OUT}	The rated current that can flow through one output terminal.
Switch through current	I_T	The rated current between the input and output terminals of a switch at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability.
V_{CC}/ground current	I_{CC} I_{CC} / I_{GND}	The rated current between the power supply and ground terminals at which an IC will not suffer breakdown, deterioration of characteristics, or reduced reliability. As V_{CC} / ground current includes output current, substantial V_{CC} / ground current can flow in an IC having multiple output terminals.
Power dissipation	P_D	Power consumption that does not cause IC breakdown over the entire operating temperature range.
Storage temperature	T_{stg}	The ambient temperature range over which no deterioration of characteristics or reliability occurs when an IC is stored for a long period of time or is transported with no supply voltage present.

6.2. Operating Ranges

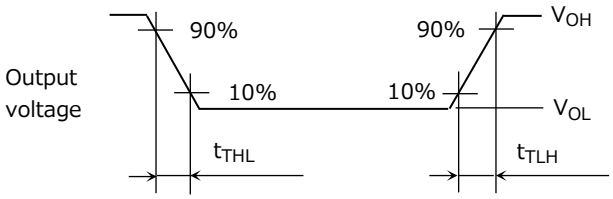
Parameter	Symbol	Definition
Supply voltage	V_{DD} V_{CC} V_{EE} $V_{DD} - V_{EE}$ $V_{CC} - V_{EE}$	The supply voltage range over which the normal operation of an IC is guaranteed.
Input voltage	V_{IN}	The input voltage range over which the normal operation and electrical characteristics of an IC are guaranteed.
Output voltage	V_{OUT}	The output voltage range over which the normal operation and electrical characteristics of an IC are guaranteed.
Switch I/O voltage	V_S $V_{I/O}$	The switch I/O voltage range over which the normal operation and electrical characteristics of an IC are guaranteed.
Output current	I_{OUT} I_{OH} , I_{OL} I_{OL}	The maximum output current at which the normal operation and electrical characteristics of an IC are guaranteed.
Input rise and fall times	t_r,t_f dt/dv	The ranges of rise and fall times of an input signal that will not cause malfunction due to oscillation of the output.
External capacitor	C_X	The external capacitance range over which the normal operation and electrical characteristics of a multivibrator IC are guaranteed.
External resistor	R_X	The external resistance range over which the normal operation and electrical characteristics of a multivibrator IC are guaranteed.
Operating temperature	T_{opr}	The operating temperature range over which the normal operation and electrical characteristics of an IC are guaranteed.

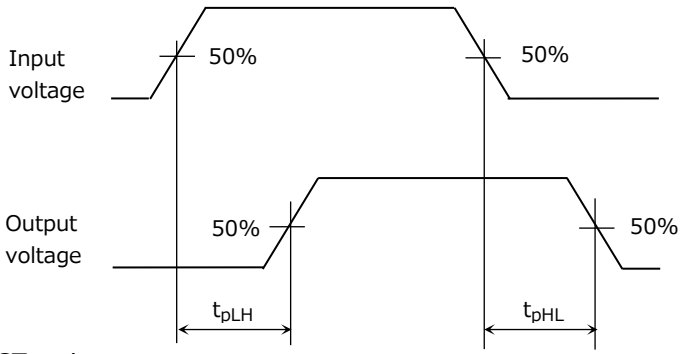
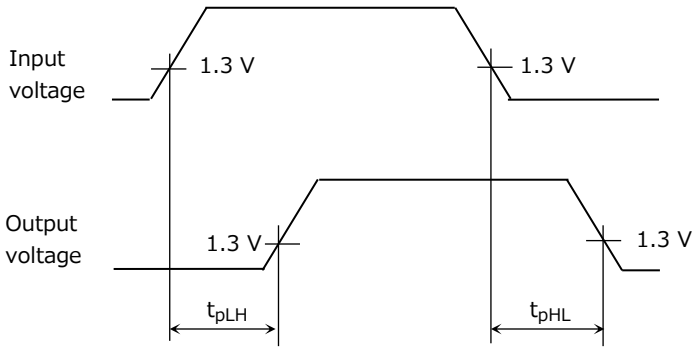
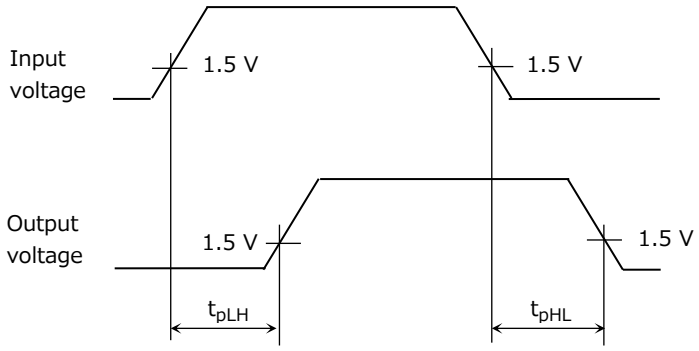
6.3. Electrical Characteristics

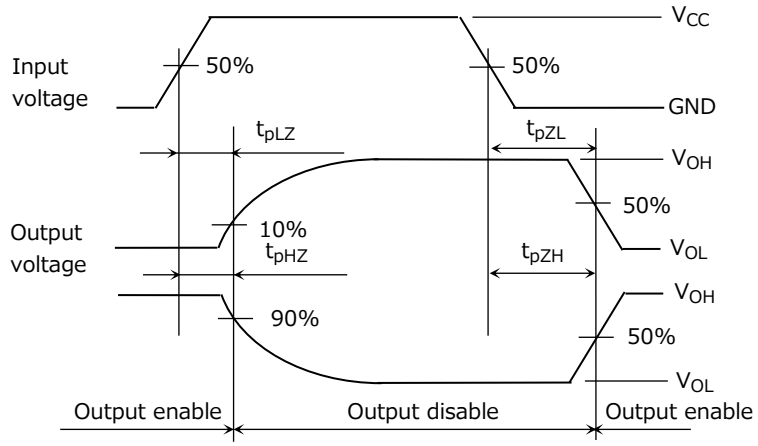
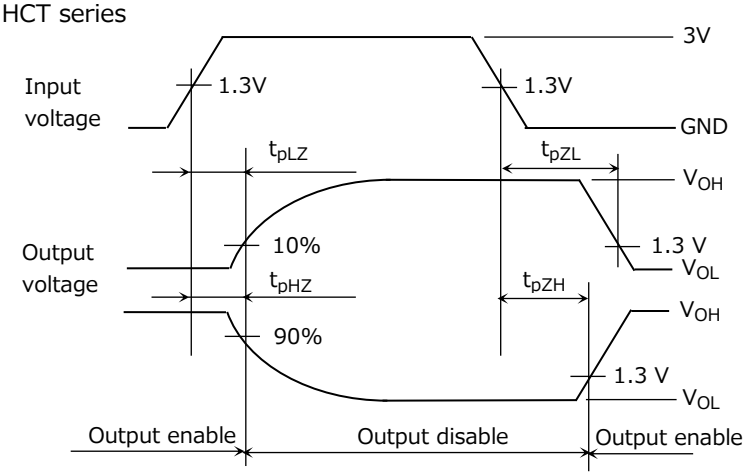
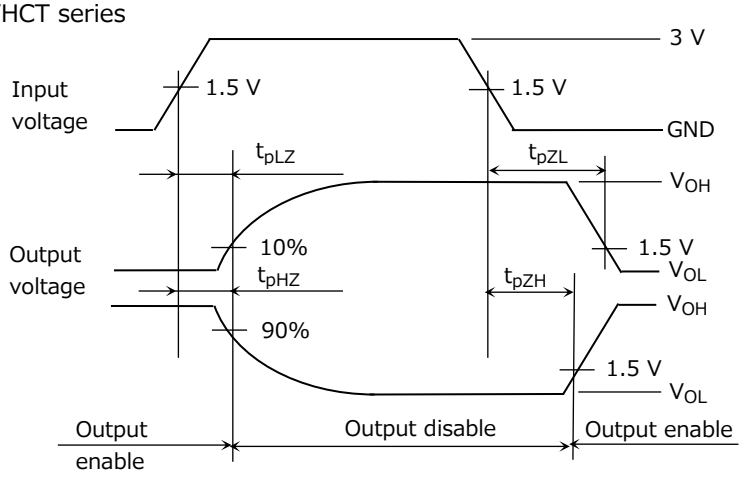
＊電気的特性は測定条件下において規定されます。

Parameter	Symbol	Definition
High-level input voltage	V_{IH}	The input voltage at which input of an IC is driven to the High level.
Low-level input voltage	V_{IL}	The input voltage at which the input of an IC is driven to the Low level.
Positive threshold voltage	V_P	The input threshold voltage at which a Schmitt-trigger input is driven to the High level.
Negative threshold voltage	V_N	The input threshold voltage at which a Schmitt-trigger input is driven to the Low level.
Hysteresis voltage	V_H	The difference between the positive and negative threshold voltages of a Schmitt-trigger input.
High-level output voltage	V_{OH}	The voltage that appears at the output when either VIH or VIL is applied to each input terminal such that the output is set to the High level.
Low-level output voltage	V_{OL}	The voltage that appears at the output when either VIH or VIL is applied to each input terminal such that the output is set to the Low level.
Power-off leakage current	I_{OFF}	The leakage current that flows into an IC via input and output terminals when the power supply is off.
Input leakage current	I_{IN}	The leakage current that flows through the input terminal when a voltage is present at the input terminal of an IC.
Output off-state leakage current	I_{OZ}	The leakage current of an IC with an open-drain output that flows through the output terminal when it is in the high-impedance state.
Output leakage current (Power-off)	I_{OPD}	The leakage current that flows into an IC via the output terminals when V_{CC} is in the off state (V_{CC} = 0 V)
3-state output off-state leakage current	I_{OZ}	The leakage current of an IC with an open-drain or three-state output that flows through the output terminal when it is in the high-impedance state.

Parameter	Symbol	Definition
Input/output leakage current (Switch off)	I_{OFF}	The leakage current that flows through an IC from the input terminals to the output terminal when the power supply is off.
Input/output leakage current (Switch on)	$I_{I/O}$	The leakage current that flows from the input terminal to the output terminal in the switch-on and open-output states.
Control input leakage current	I_{IN}	The leakage current that flows through the control input terminal of an IC when a voltage is applied to the terminal.
RX/CX terminal off-state current	I_{IN}	The current that flows through the RX/CX terminal of a multivibrator IC when a voltage is applied to the terminal.
T2 terminal input leakage current	I_{IN}	The current that flows through the T2 terminal of a multivibrator IC when a voltage is applied to the terminal.
Quiescent supply current	I_{CC}	The current that flows into an IC via the V_{CC} terminal when the V_{CC} or ground level is held constant without changing the input voltage.
	ΔI_{CC}	The current that flows into an IC via the V_{CC} terminal when V_{CC} - 0.6 V is applied to one input terminal.
	I_{CCT}	The current that flows into an IC with TTL-level input via the V_{CC} terminal when a TTL-level voltage is applied to one input terminal.
Active-state supply current (per circuit)	$I_{CC(opr)}$	The average current that flows in the no-load condition between the power supply and ground terminals due to an internal circuit operation.
On-resistance	R_{ON}	The resistance between the input and the output of an analog switch, multiplexer or demultiplexer IC in the switch-on state.
Difference of on-resistance between switches	ΔR_{ON}	The difference in on-resistance between different input-output pairs of an analog switch, multiplexer or demultiplexer IC.

Parameter	Symbol	Definition
Minimum pulse width	$t_{w(H)}$ $t_{w(L)}$	The minimum pulse width that is accepted at a clock input, etc. as a normal pulse.
Minimum setup time	t_S	The time interval during which data must be stable before the associated input (e.g., clock) changes. For example, when data is latched on the rising edge of a clock pulse, it is necessary to apply data at least t_S before the rising edge of the clock.
Minimum hold time	t_h	The time interval during which data must be stable after the active transition of the associated input (e.g., clock).
Minimum removal time	t_{rem}	The minimum time between the release of an asynchronous input (e.g., Clear, Preset) and the application of the next input (e.g., clock).
Minimum retrigger time	t_{rr}	The minimum time necessary for a multivibrator IC to accept the next trigger signal after having received one.
Output transition time	t_{TLH} t_{THL}	The rise and fall times of the output voltage. t_{TLH} is the time from 10% to 90% when the output transitions from Low to High, and t_{THL} is the time from 90% to 10% when the output transitions from High to Low. 

Parameter	Symbol	Definition
Propagation delay time	t_{pLH} t_{pHL}	The delay time between the application of an input signal and an output response. t_{pLH} is defined as the time required for an output to transition from Low to High, and t_{pHL} is defined as the time required for an output to transition from High to Low. HC/VHC series  HCT series  VHCT series 

Parameter	Symbol	Definition
Output enable time Output disable time	t_{pLZ} t_{pHZ} t_{pZL} t_{pZH}	The output enable time is defined as the delay time required for a three-state terminal to be driven High or Low after the output control terminal is set to an inactive level. The output disable time is defined as the delay time required for an output terminal to assume the high-impedance state after the output control signal is set to an active level. HC/VHC series  HCT series  VHCT series 

Parameter	Symbol	Definition
Propagation delay time	Δt_{PD}	For counter ICs, the delay time defined for an IC from when the Qn output is inverted to when the next output (Qn+1) is inverted.
Output pulse width	t_{wOUT}	For multivibrator ICs, the width of the output pulse generated when a prescribed external component is connected and a prescribed voltage is applied.
Output pulse width error between circuits (in the same package)	Δt_{wOUT}	For multivibrator ICs, a difference in output pulse width between two circuits in the same package.
Output skew	t_{osLH} t_{osHL} t_{osZL}	Differences in propagation delay time among output terminals when some outputs in the same package change from the Low level to the High level, from the High level to the Low level, or from the high-impedance state to the Low level.
Phase difference between input and output	$\varphi_{I/O}$	For analog switch, multiplexer and demultiplexer ICs, the delay time from the input to the output when a signal is applied to the input in the switch-on state.
Clock frequency	f	The clock frequency at which an IC operates.
Maximum clock frequency	f_{MAX}	The maximum clock frequency at which the IC operates normally.
Maximum frequency response Phase difference between input and output	$f_{MAX(I/O)}$ f_{MAX}	For analog switch, multiplexer and demultiplexer ICs, the maximum input frequency that the signal can transmit to the output in the switch-on state.
Input capacitance	C_{IN}	The capacitance between the input and ground terminals.
Control input capacitance	C_{IN}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the control input and ground terminals.
Common terminal capacitance	C_{IS}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the common and ground terminals in the off state.
Switch terminal capacitance	C_{OS}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the switch and ground terminals in the off state.

Parameter	Symbol	Definition
Feedthrough capacitance	C_{IOS}	For analog switch, multiplexer and demultiplexer ICs, the capacitance between the switch and common terminals in the off state.
Bus I/O capacitance	$C_{I/O}$	The capacitance between the bus and ground terminals.
Power dissipation capacitance	C_{PD}	The equivalent internal capacitance of a device calculated by measuring the operating current in the no-load condition.
Output capacitance	C_{OUT}	The capacitance between the output and ground terminals for a three-state or open-drain output in the high-impedance state.
Sine Wave Distortion	THD	For analog switch, multiplexer and demultiplexer ICs, the distortion rate of the sine wave that is output when a sine wave is input in the on state.
Feed-through attenuation (switch off)	FTH	For analog switch, multiplexer and demultiplexer ICs, the ratio of the leakage voltage that appears at the output to the input voltage applied in the off state
Crosstalk (control input to signal output)	X_{talk}	For analog switch, multiplexer and demultiplexer ICs, the leakage voltage of a signal to the input and output that occurs when the control input changes.
Crosstalk (between any switches)	X_{talk}	For analog switch, multiplexer and demultiplexer ICs, the ratio of the voltage applied to a switch (port) in the on state to the voltage that appears at a switch (port) in the off state
Quiet output maximum dynamic V_{OL}	V_{OLP}	The maximum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.
Quiet output minimum dynamic V_{OL}	V_{OLV} $\lvert V_{OLV} \rvert$	The minimum peak voltage induced into an output that is fixed at the Low level when the other outputs are switching simultaneously.
Quiet output minimum dynamic V_{OH}	V_{OHV}	The minimum peak voltage induced into an output that is fixed at the High level when the other outputs are switching simultaneously.
Minimum high-level dynamic input voltage	V_{IHD}	High-level dynamic threshold voltage when all inputs are switching simultaneously
Maximum low-level dynamic input voltage	V_{ILD}	Low-level dynamic threshold voltage when all inputs are switching simultaneously.

6.4. Built-in Function

Parameter	Definition
Input tolerant function	A function designed to prevent a current from flowing from an input to the power supply when the input voltage is higher than the power supply voltage or when V_{CC} = 0 V.
Output tolerant function	A function designed to prevent a current from flowing from an output to the power supply when the output is in the high-impedance state or when V_{CC} = 0 V.
Power-down protection	A function designed to prevent a current from flowing to the power supply terminal even if a voltage is applied to the input and output terminals when V_{CC} = 0 V.
Bus-hold function	A function designed to hold the input logic level using a latch circuit even when the input terminal becomes open.

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