TC74HC593AP/AF
PRELIMINARY

8 BINARY COUNTER WITH INPUT REGISTER(3-State I/O)

The TC74HC593A is a high speed CMOS 8-BIT BINARY COUNTER/REGISTER fabricated with C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC593A has all the features of the "HC592A with the addition of a 3-state I/O which provides parallel counter outputs. The 3-state outputs are active when enable input $\overline{G}$ is low and G is high.

Inputs A through H are loaded into registers on the rising edge of Register Clock (RCK) only when Register Clock Enable ($\overline{RCKEN}$) is low. The register outputs are loaded into the counter when Counter Load ($\overline{CLOAD}$) is low.

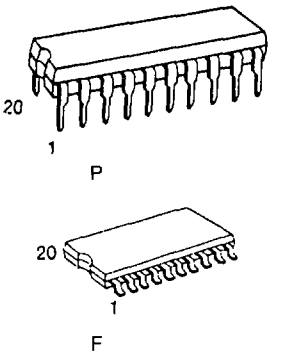
The internal counter counts on the rising edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is low and or Counter Clock Enable ($\overline{CCKEN}$) is high.

If Counter Clear ($\overline{CCLR}$) is set low, the internal counter is cleared asynchronously to the clock.

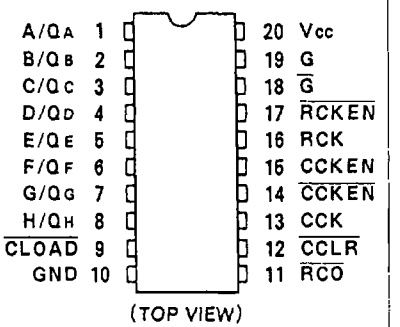
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

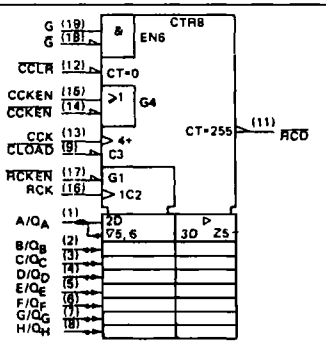
- High Speed ····· f_{MAX}=80MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QH
  10 LSTTL Loads For $\overline{RCO}$
- Symmetrical Output Impedance ···
  $|I_{OH}|=I_{OL}$=6mA(Min.) For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For $\overline{RCO}$
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS593



PIN ASSIGNMENT



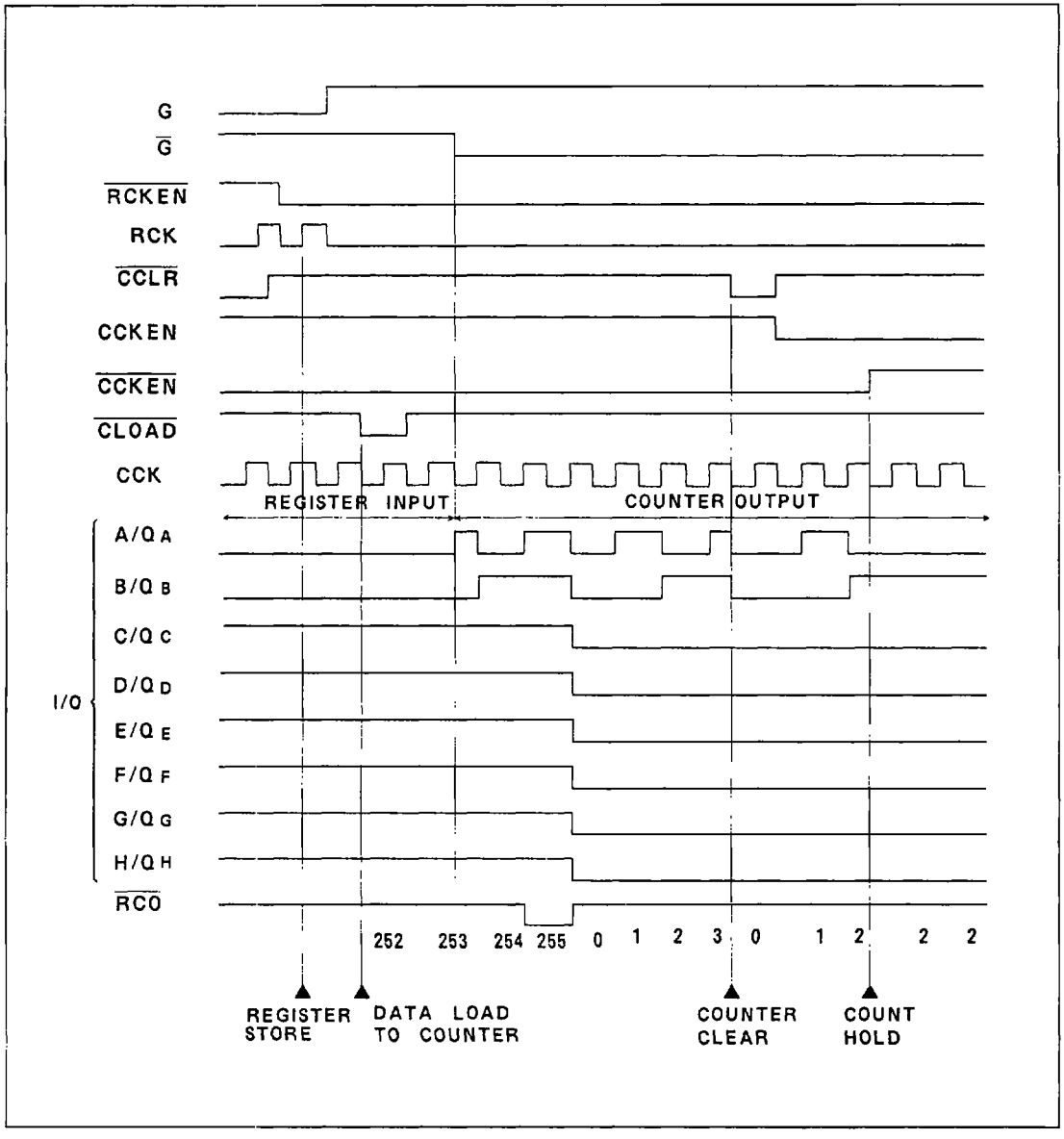
IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TIMING CHART



TRUTH TABLE

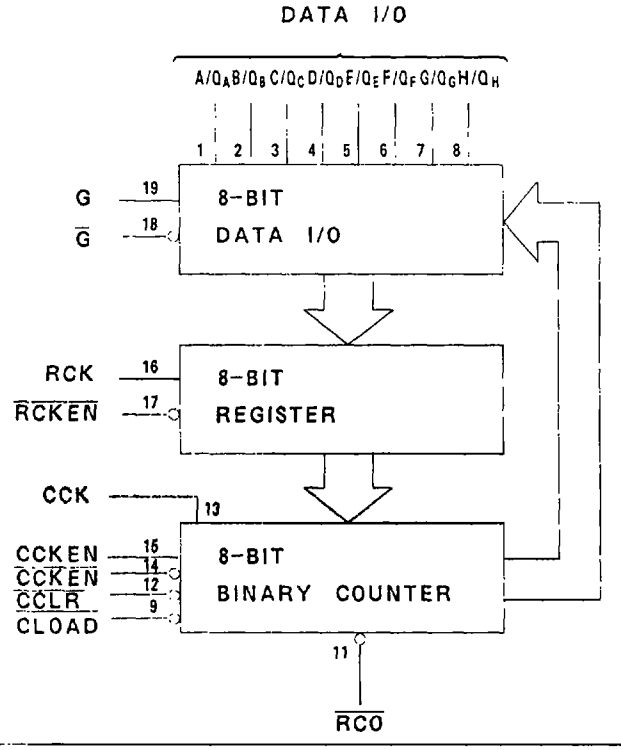
INPUT									FUNCTION
G	$\overline{G}$	$\overline{RCKEN}$	RCK	$\overline{CLOAD}$	$\overline{CCLR}$	CCKEN	$\overline{CCKEN}$	CCK	
L	X	X	X	X	X	X	X	X	THE I/O TERMINALS ARE IN THE HIGH INPEDANCE. THE DATA INPUTS ARE ENABLE.
X	H	X	X	X	X	X	X	X	
H	L	X	X	X	X	X	X	X	THE I/O TERMINALS OUTPUT COUNTER DATA.
X	X	L	↑	X	X	X	X	X	THE DATA OF A THRU H INPUTS IS STORED INTO REGISTER
X	X	L	↓	X	X	X	X	X	REGISTER STATE IS NOT CHANGED.
X	X	H	↑	X	X	X	X	X	
X	X	X	X	L	H	X	X	X	REGISTER DATA IS LOADED INTO COUNTER.
X	X	X	X	H	L	X	X	X	COUNTER CLEAR.
X	X	X	X	H	H	H	X	↑	COUNTER ADVANCES THE COUNT.
X	X	X	X	H	H	X	L	↑	
X	X	X	X	H	H	H	X	↓	NO COUNT
X	X	X	X	H	H	X	L	↓	
X	X	X	X	H	H	L	H	↑	

X:Don't care

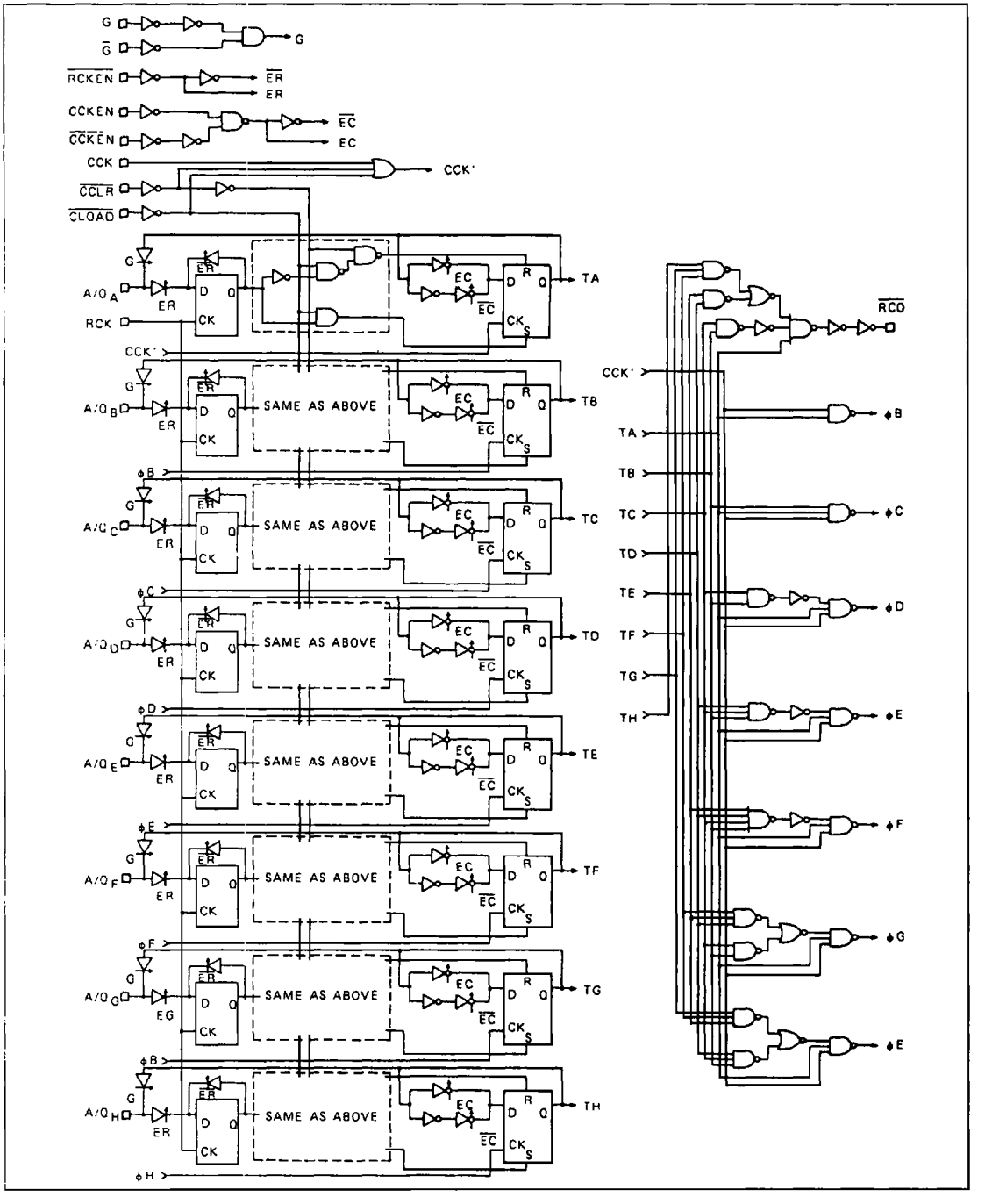
$\overline{RCO}=\overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

(QA'-QH':Internal outputs of the counter)

BLOCK DIAGRAM



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current ($\overline{RCO}$) / (Q_A~Q_H)	I_{OUT}	±25 / ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Onput Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}				2.0	1.5	−	−	1.5	−	V
					4.5	3.15	−	−	3.15	−	
					6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}				2.0	−	−	0.5	−	0.5	V
					4.5	−	−	1.35	−	1.35	
					6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}		I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
					4.5	4.4	4.5	−	4.4	−	
					6.0	5.9	6.0	−	5.9	−	
			$\overline{RCO}$	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
				I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
			Q_A~Q_H	I_{OH} =−6 mA	4.5	4.18	4.31	−	4.31	−	
				I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}		I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
					4.5	−	0.0	0.1	−	0.1	
					6.0	−	0.0	0.1	−	0.1	
			$\overline{RCO}$	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
				I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
			Q_A~Q_H	I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
				I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND			6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND			6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND			6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CCK, RCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{W(L)}$		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Pulse Width ($\overline{CLOAD}$)	$t_{W(L)}$		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time ($\overline{RCKEN}$−RCK)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time ($\overline{CCKEN}$, $\overline{CCKEN}$−CCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (RCK−$\overline{CLOAD}$)	t_s		2.0	−	150	190	
			4.5	−	30	38	
			6.0	−	25	32	
Minimum Set−up Time (A~H−RCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time ($\overline{CCKEN}$, CCKEN−CCK)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	−	50	60	
			4.5	−	10	12	
			6.0	−	9	11	
Minimum Removal Time ($\overline{CLOAD}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	4.4	3.6	MHz
			4.5	−	22	18	
			6.0	−	26	21	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	25	40	
Propagation Delay Time (RDK−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	35	53	
Propagation Delay Time ($\overline{CCLR}$−$\overline{RCO}$)	t_{pLH}		−	27	43	
Propagation Delay Time ($\overline{CLOAD}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	29	43	
Maximum Clock Frequency	f_{MAX}		24	80	−	MHz

AC ELECTRICAL CHARACTERISTICS(Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time (Q_A~Q_H)	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (CCK−Q_A~Q_H)	t_{pLH} t_{pHL}		50	2.0	−	93	225	−	280	
				4.5	−	30	45	−	56	
				6.0	−	23	38	−	48	
			150	2.0	−	106	265	−	330	
				4.5	−	35	53	−	66	
				6.0	−	27	45	−	56	
Propagation Delay Time ($\overline{CCLR}$−Q_A~Q_H)	t_{pLH} t_{pHL}		50	2.0	−	89	225	−	280	
				4.5	−	28	45	−	56	
				6.0	−	22	38	−	48	
			150	2.0	−	104	265	−	330	
				4.5	−	33	53	−	66	
				6.0	−	26	45	−	56	
Propagation Delay Time ($\overline{CLOAD}$−Q_A~Q_H)	t_{pHL}		50	2.0	−	100	225	−	280	
				4.5	−	30	45	−	56	
				6.0	−	24	38	−	48	
			150	2.0	−	113	265	−	330	
				4.5	−	35	53	−	66	
				6.0	−	28	45	−	56	
Propagation Delay Time (CCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		50	2.0	−	95	225	−	280	
				4.5	−	29	45	−	56	
				6.0	−	23	38	−	48	
Propagation Delay Time (RCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		50	2.0	−	150	300	−	375	
				4.5	−	40	60	−	75	
				6.0	−	31	51	−	64	
Propagation Delay Time ($\overline{CCLR}$−$\overline{RCO}$)	t_{pLH}		50	2.0	−	110	250	−	315	
				4.5	−	32	50	−	63	
				6.0	−	24	43	−	54	
Propagation Delay Time ($\overline{CLOAD}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		50	2.0	−	120	250	−	315	
				4.5	−	36	50	−	63	
				6.0	−	26	43	−	54	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1\,k\Omega$	50	2.0	−	58	150	−	190	
				4.5	−	18	30	−	38	
				6.0	−	14	26	−	32	
			150	2.0	−	71	190	−	240	
				4.5	−	23	38	−	48	
				6.0	−	18	32	−	41	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1\,k\Omega$	50	2.0	−	51	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	18	26	−	32	
Maximum Clock Frequency	f_{MAX}		50	2.0	4.4	17	−	3.6	−	MHz
				4.5	22	64	−	18	−	
				6.0	26	84	−	21	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	59	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$