California State University, Sacramento
CpE 151
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October 16, 2022

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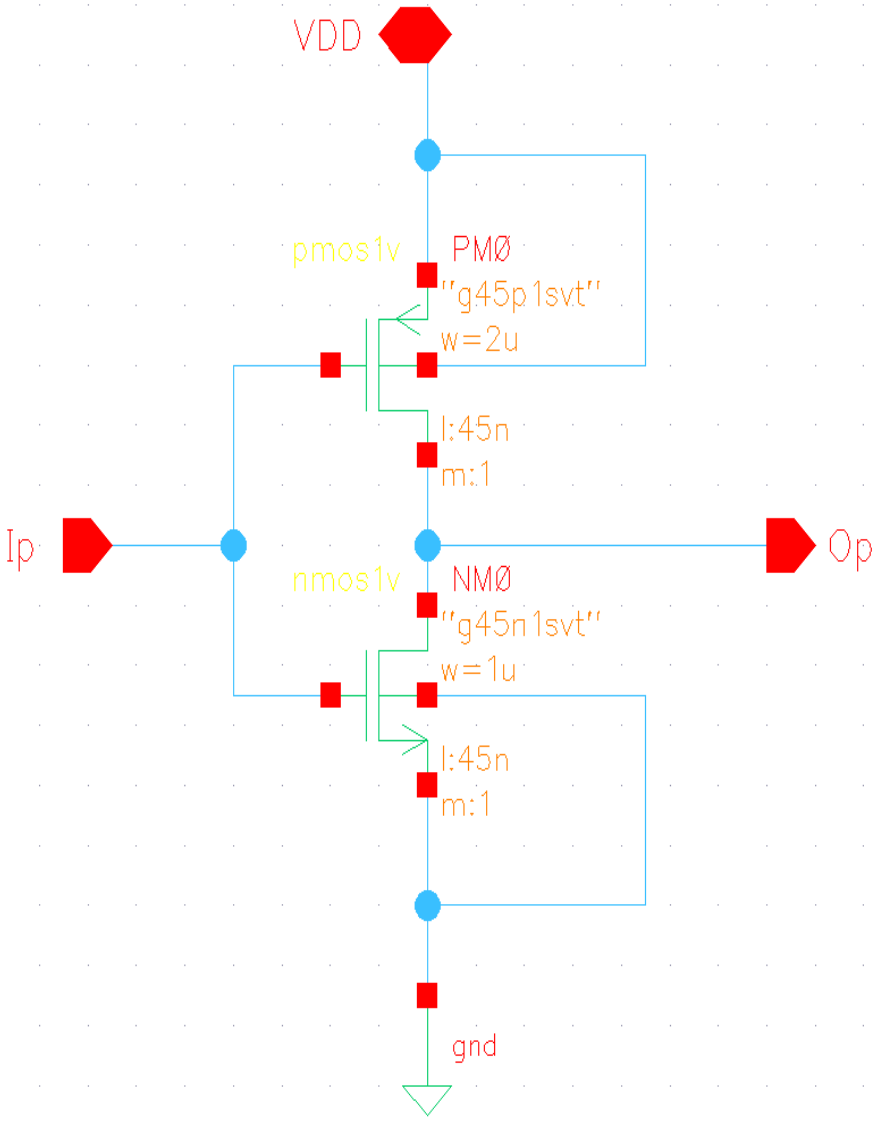
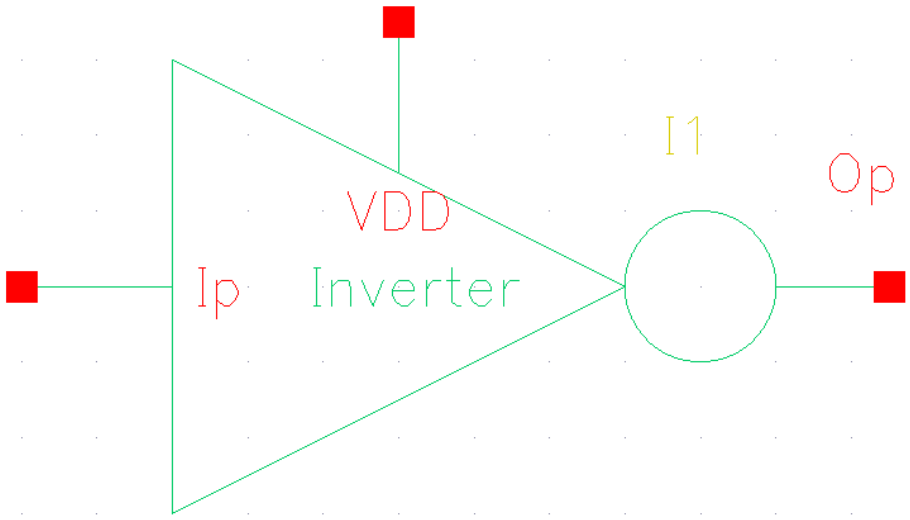
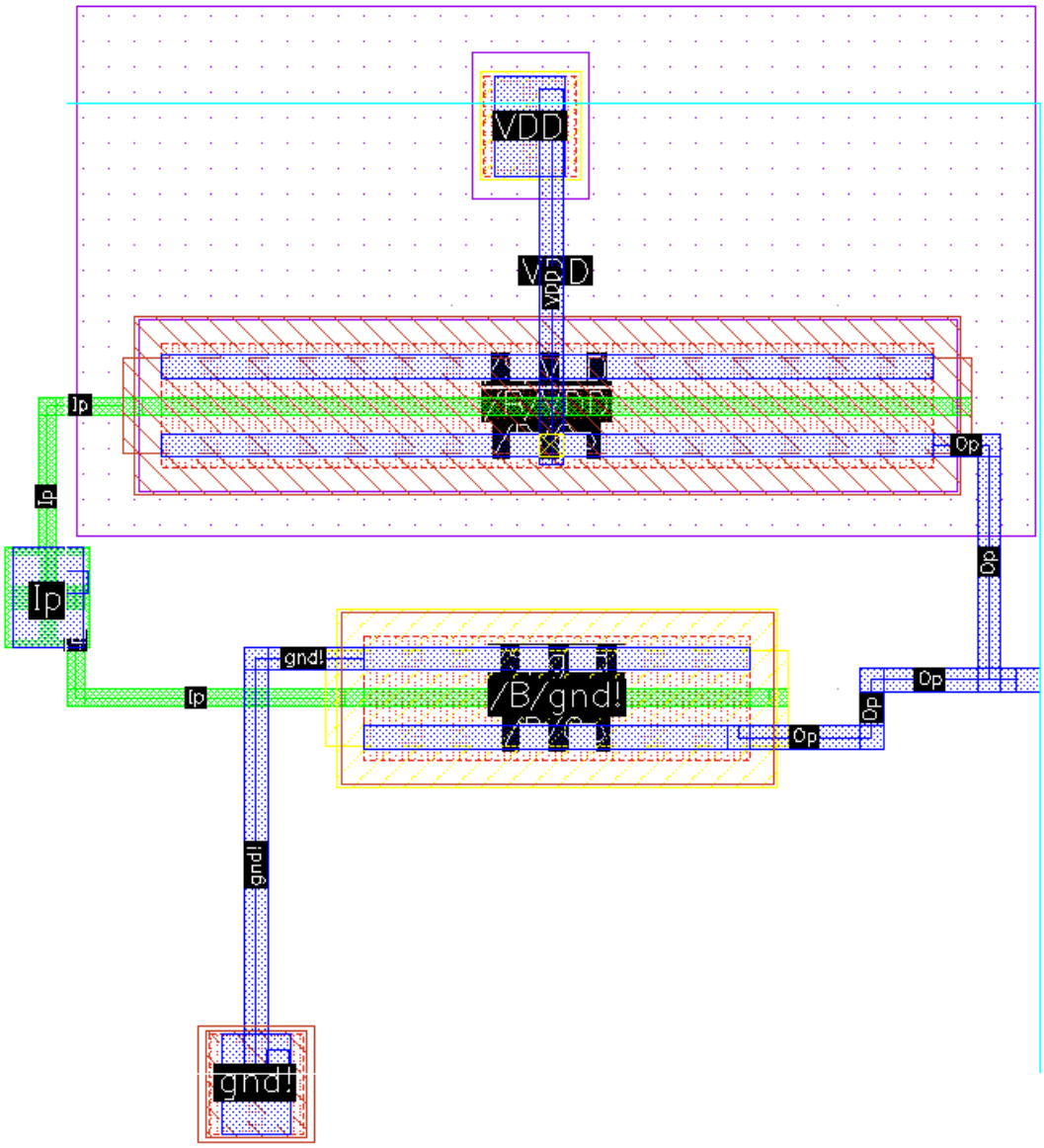
INVERTER Circuit Schematic (A + B)
Use: (W/L)n = 1.0/0.045 and (W/L)p = 2.0/0.045



INVERTER Symbol



INVERTER Layout



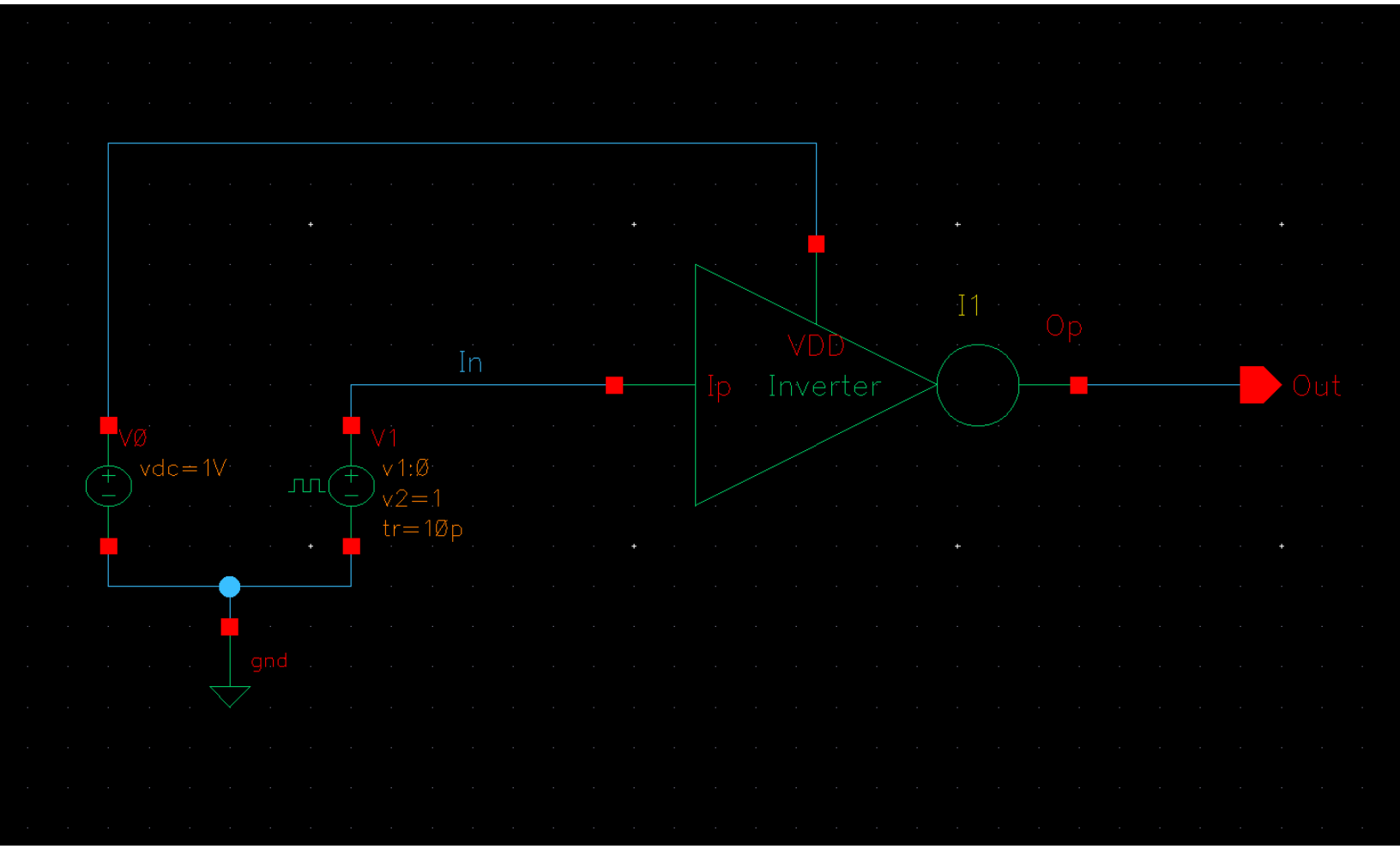
INVERTER DRC / LVS

Host is
cmd is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/johnmatthewjimenez/cpe151/Inverter.rsf -cdslib /home/student/johnmatthewjimenez/cpe151/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:14: pid 25294.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
WARNING No DRC errors found.

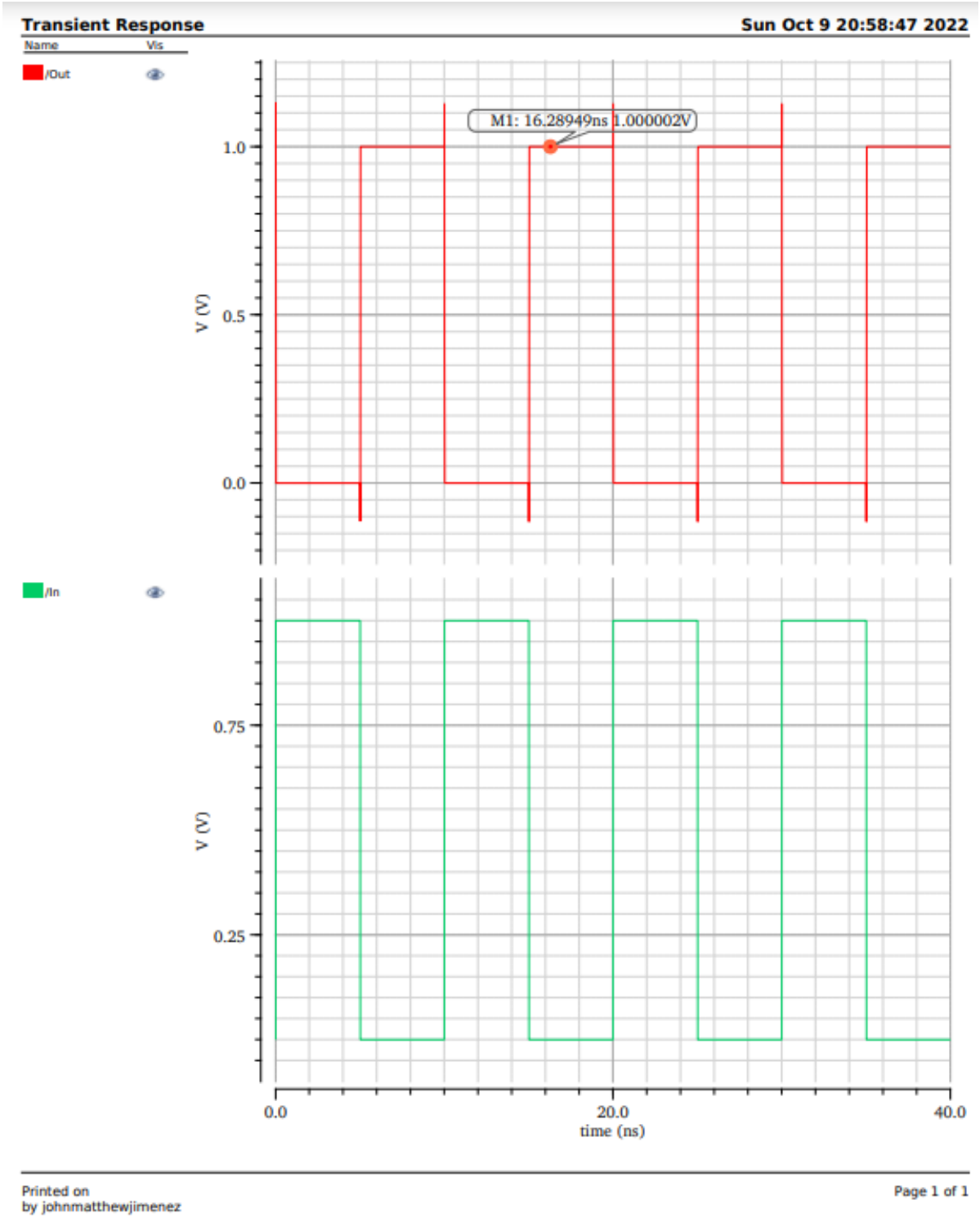
```
================================================================================
====File: Inverter.cfr
================================================================================
The LVS run "Inverter" has completed successfully.

Compare problems were detected in 1 cells.
   1 cells had nets mismatches.
   1 cells had pins mismatches.
   0 cells matched

Extraction Problems were detected in 1 cell(s).
  2 Label Short(s) detected.

You currently have an open run (project).
Press "OK" to close this run and enter the LVS Debug Environment.
Press "Cancel" to leave this run open and close this Dialog box.

LVS Run "Inverter"
is located in /home/student/johnmatthewjimenez/cpe151/
```


```
WARNING      Multiple label discarded: "VDD" at (1.2600, 2.5300) and "Op" on net C3.
WARNING      1 net(s) with multi-label warning found in cell 'Inverter layout Project-1'.
WARNING      Multiple label discarded: "VDD" at (1.2600, 2.5300) and "Op" on net C3.
WARNING      1 net(s) with multi-label warning found in cell 'Inverter layout Project-1'.
WARNING      deleteCellPin - Unable to find cell 'g45inds'
```

INVERTER Testbench Circuit



INVERTER Testbench Results



INVERTER (Quantus Extraction)

Summary for testProjectProject-1/Inverter_rcx/av_extracted

instance count totals:

lib	cell	view	total
analogLib	pcapacitor	symbol	14
analogLib	presistor	symbol	10
gpdk045	nmos1v	ivpcell	1
gpdk045	pmos1v	ivpcell	1

Summary for Project-1/Inverter/av_extracted

instance count totals:

lib	cell	view	total
testProjectProject-1	Inverter_rcx	av_extracted	1

extracted view creation completed
cpu: 0.10 elap: 0 pf: 4 in: 176 out: 192 virt: 433M phys: 833M
INFO (LBRCXU-114): Finished /opt/cadence/ASSURA41/tools.lnx86/assura/bin/rcxToDfII

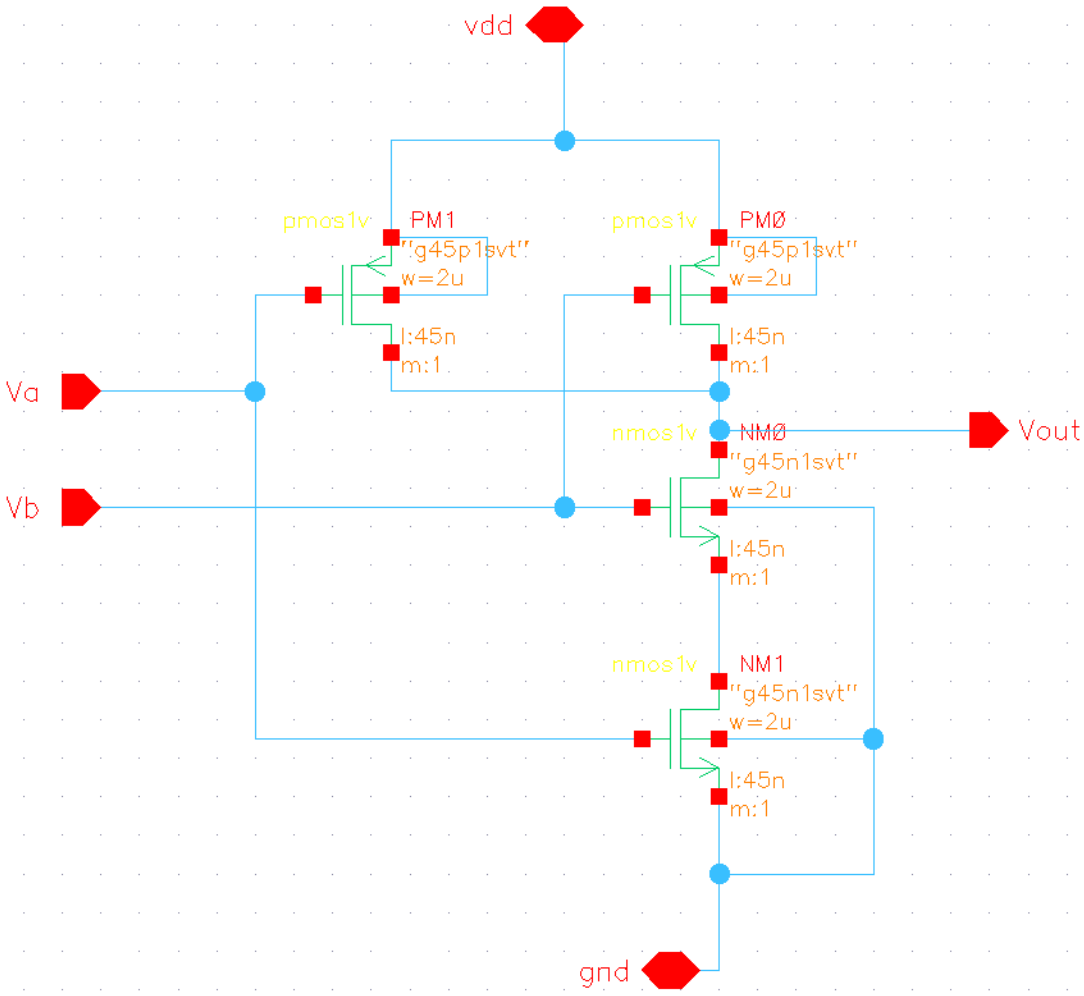
INFO (LBRCXM-582): Checking in license of QTS300 21.10

INFO (LBRCXM-702): Run ended: Mon Oct 10 13:14:51 2022

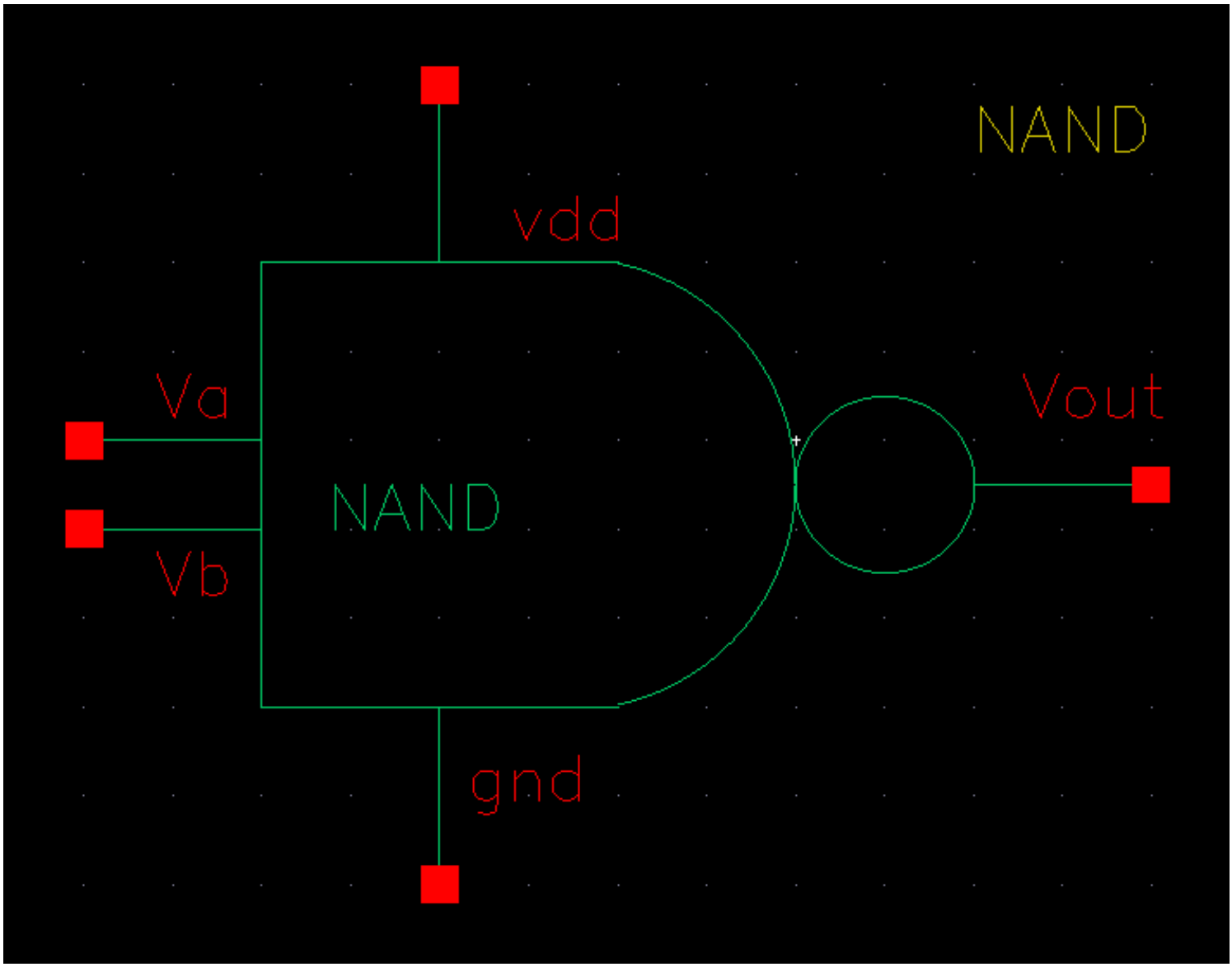
INFO (LBRCXM-805): Run took: 15s elapsed

INFO (LBRCXM-708): ***** Quantus terminated normally *****

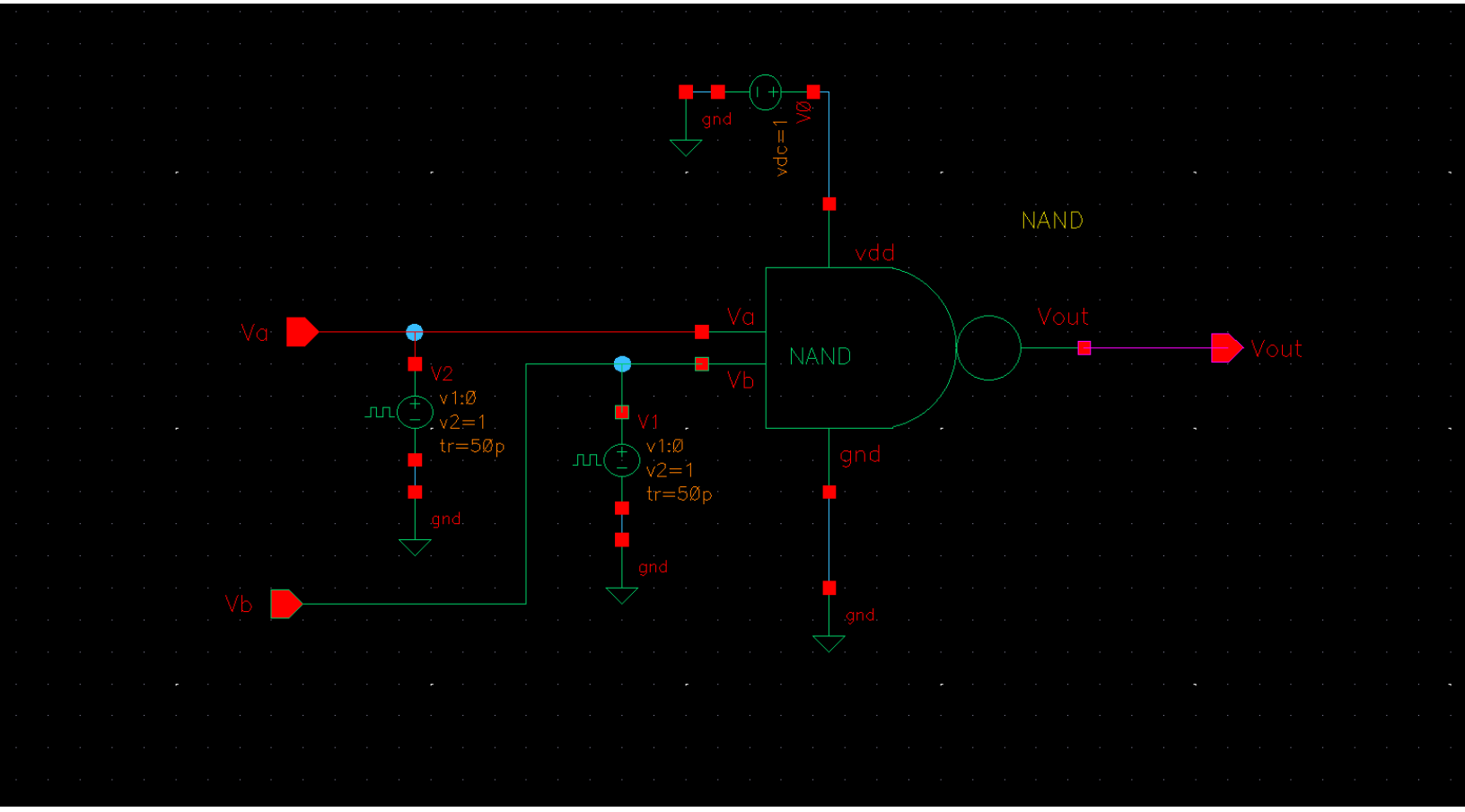
NAND Gate Circuit Schematic ~(A*B)
A 2-input Use: (W/L)n = 2.0/0.045 and (W/L)p = 2.0/0.045



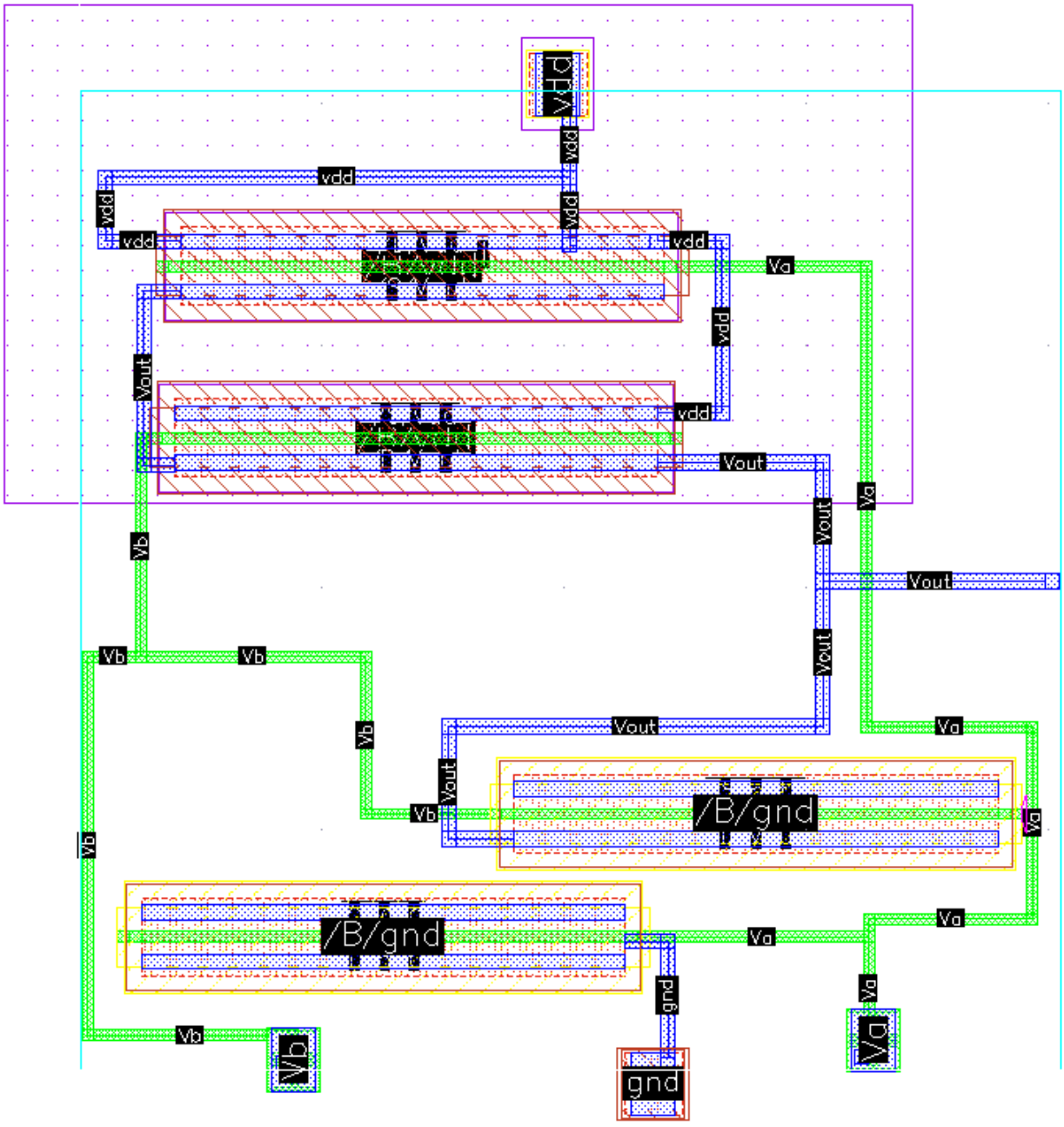
NAND Symbol



NAND Testbench Circuit



NAND Layout


vdd
vdd
vdd
vdd
vdd
vdd
vdd
vdd
Va
Vout
Vout
Vout
Vout
Vout
Vout
Vb
Vb
Vb
Vb
Vb
Vb
Vb
Vb
Va
Va
Va
Va
Va
/B/gnd
/B/gnd
gnd
gnd
Vb
Vb
Va

NAND DRC

done!
Loaded gpdk045/libInit.il successfully!
Loading drdEdit.cxt
Loading soi.cxt
Loading schematic.cxt
Loading ddui.cxt
Loading vb.cxt
Loading cfde.cxt
Loading nt.cxt
Loading oi.cxt
Loading see.cxt
Loading treeAssistant.cxt
Loading asst.cxt
Loading simui.cxt
Loading hsm.cxt
Loading ap.cxt
INFO (BND-1003): Binder initialized for layout cellview 'Project-1.2/NAND/layout' and source cellview 'Project-1.2/NAND/schematic':

	bound
terminals	5
nets	6
instances	4

Host is
cmd is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/johnmatthewjimenez/cpe151/NAND.rsf -cdslib /home/student/johnmatthewjimenez/cpe151/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:10: pid 5935.
Loading layers.cxt
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
WARNING No DRC errors found.

NAND LVS Check

Host is
cmd is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura
/home/student/johnmatthewjimenez/cpe151/NAND.rsf -cdslib
/home/student/johnmatthewjimenez/cpe151/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:11: pid 9969.
STATUS: Schematic and Layout Match

Checking in license for "Phys_Ver_Sys_Results_Mgr"
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
Schematic cell - NAND schematic Project-1.2
Schematic cell - NAND schematic Project-1.2
INFO (LX-1947): Editing 'Project-1.2/NAND/layout' in Layout XL without a connectivity reference can introduce Layout XL compliance issues.
Specify the source schematic using the 'Connectivity - Update - Connectivity Reference' menu command.
INFO (BND-1003): Binder initialized for layout cellview 'Project-1.2/NAND/layout' and source cellview 'Project-1.2/NAND/schematic':

	bound
terminals	5
nets	6
instances	4

INFO (BND-1004): Layout instances and terminals match source.

(NAND testbench results)

DC simulation time: CPU = 517 us, elapsed = 517.845 us.

Opening the PSFXL file ../psf/tran.tran.tran ...
Important parameter values:
start = 0 s
outputstart = 0 s
stop = 100 ns
step = 100 ps
maxstep = 2 ns
ic = all
useprevic = no
skipdc = no
reltol = 1e-03
abstol(V) = 1 uV
abstol(I) = 1 pA
temp = 27 C
tnom = 27 C
tempeffects = all
errpreset = moderate
method = traponly
lteratio = 3.5
relref = sigglobal
cmin = 0 F
gmin = 1 pS
rabsshort = 1 mOhm

Notice from spectre during transient analysis `tran'.
Multithreading is disabled due to the size of the design being too small.

Output and IC/nodeset summary:
save 3 (current)
save 9 (voltage)

Notice from spectre at time = 336.036 ps during transient analysis `tran'.
Found trapezoidal ringing on node V0:p.

```
Notice from spectre at time = 564.566 ps during transient analysis `tran'.
    Found trapezoidal ringing on node V0:p.
Notice from spectre at time = 1.02163 ns during transient analysis `tran'.
    Found trapezoidal ringing on node V0:p.
Notice from spectre at time = 1.92965 ns during transient analysis `tran'.
    Found trapezoidal ringing on node V0:p.
Notice from spectre at time = 3.36923 ns during transient analysis `tran'.
    Found trapezoidal ringing on node V0:p.
        Further occurrences of this notice will be suppressed.

    tran: time = 3.369 ns    (3.37 %), step = 1.44 ns      (1.44 %)
    tran: time = 8.71 ns     (8.71 %), step = 1.34 ns      (1.34 %)
    tran: time = 13.28 ns    (13.3 %), step = 1.576 ns     (1.58 %)
    tran: time = 18.64 ns    (18.6 %), step = 1.361 ns     (1.36 %)
    tran: time = 22.53 ns    (22.5 %), step = 1.215 ns     (1.21 %)
    tran: time = 28.53 ns    (28.5 %), step = 2 ns         (2 %)
    tran: time = 33.28 ns    (33.3 %), step = 1.576 ns     (1.58 %)
    tran: time = 38.64 ns    (38.6 %), step = 1.361 ns     (1.36 %)
    tran: time = 42.53 ns    (42.5 %), step = 1.215 ns     (1.21 %)
    tran: time = 48.53 ns    (48.5 %), step = 2 ns         (2 %)
    tran: time = 53.28 ns    (53.3 %), step = 1.576 ns     (1.58 %)
    tran: time = 58.64 ns    (58.6 %), step = 1.361 ns     (1.36 %)
    tran: time = 62.53 ns    (62.5 %), step = 1.215 ns     (1.21 %)
    tran: time = 68.53 ns    (68.5 %), step = 2 ns         (2 %)
    tran: time = 73.28 ns    (73.3 %), step = 1.576 ns     (1.58 %)
    tran: time = 78.64 ns    (78.6 %), step = 1.361 ns     (1.36 %)
    tran: time = 82.53 ns    (82.5 %), step = 1.215 ns     (1.21 %)
    tran: time = 88.53 ns    (88.5 %), step = 2 ns         (2 %)
    tran: time = 93.28 ns    (93.3 %), step = 1.576 ns     (1.58 %)
    tran: time = 98.64 ns    (98.6 %), step = 1.361 ns     (1.36 %)
Number of accepted tran steps =           451

Notice from spectre during transient analysis `tran'.
    Trapezoidal ringing is detected during tran analysis.
        Please use method=trap for better results and performance.


Maximum value achieved for any signal of each quantity:
V: V(Vout) = 1.092 V
I: I(V0:p) = 12.38 uA
```

If your circuit contains signals of the same quantity that are vastly different in size (such as high voltage circuitry combined with low voltage control circuitry), you should consider specifying global option `bin_relref=yes'.

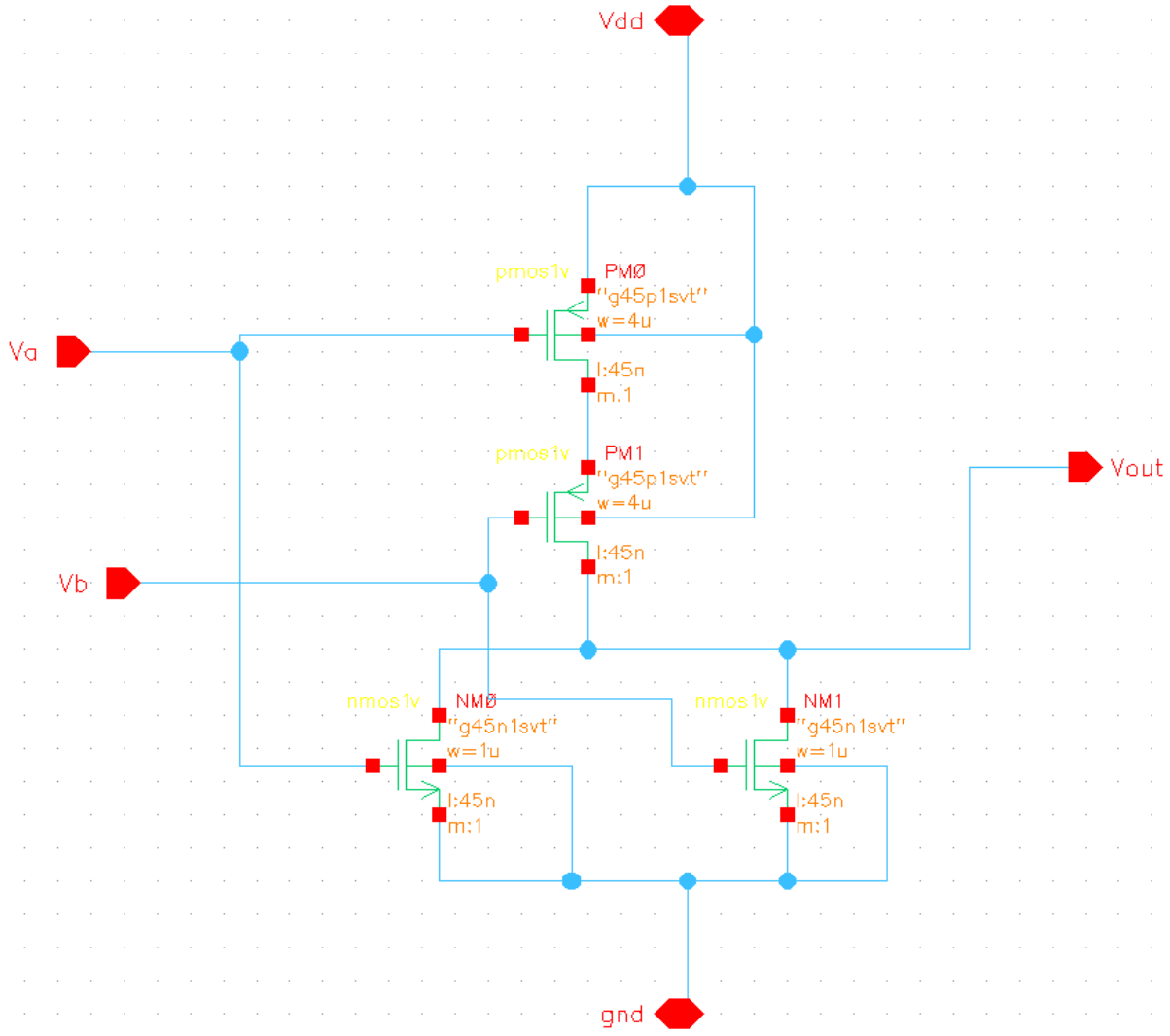
~~~~~~
Post-Transient Simulation Summary
~~~~~~
- To further speed up simulation, consider
  add ++aps on command line
~~~~~~

During simulation, the CPU load for active processors is :
2 (1.6 %) 4 (66.7 %) 5 (1.6 %) 6 (1.6 %)
7 (1.6 %)
Total: 73.1%
Initial condition solution time: CPU = 560 us, elapsed = 560.045 us.
Intrinsic tran analysis time: CPU = 20.719 ms, elapsed = 40.189 ms.
Total time required for tran analysis `tran': CPU = 22.911 ms, elapsed = 44.6892 ms.
Time accumulated: CPU = 479.172 ms, elapsed = 735.247 ms.
Peak resident memory used = 96.6 Mbytes.

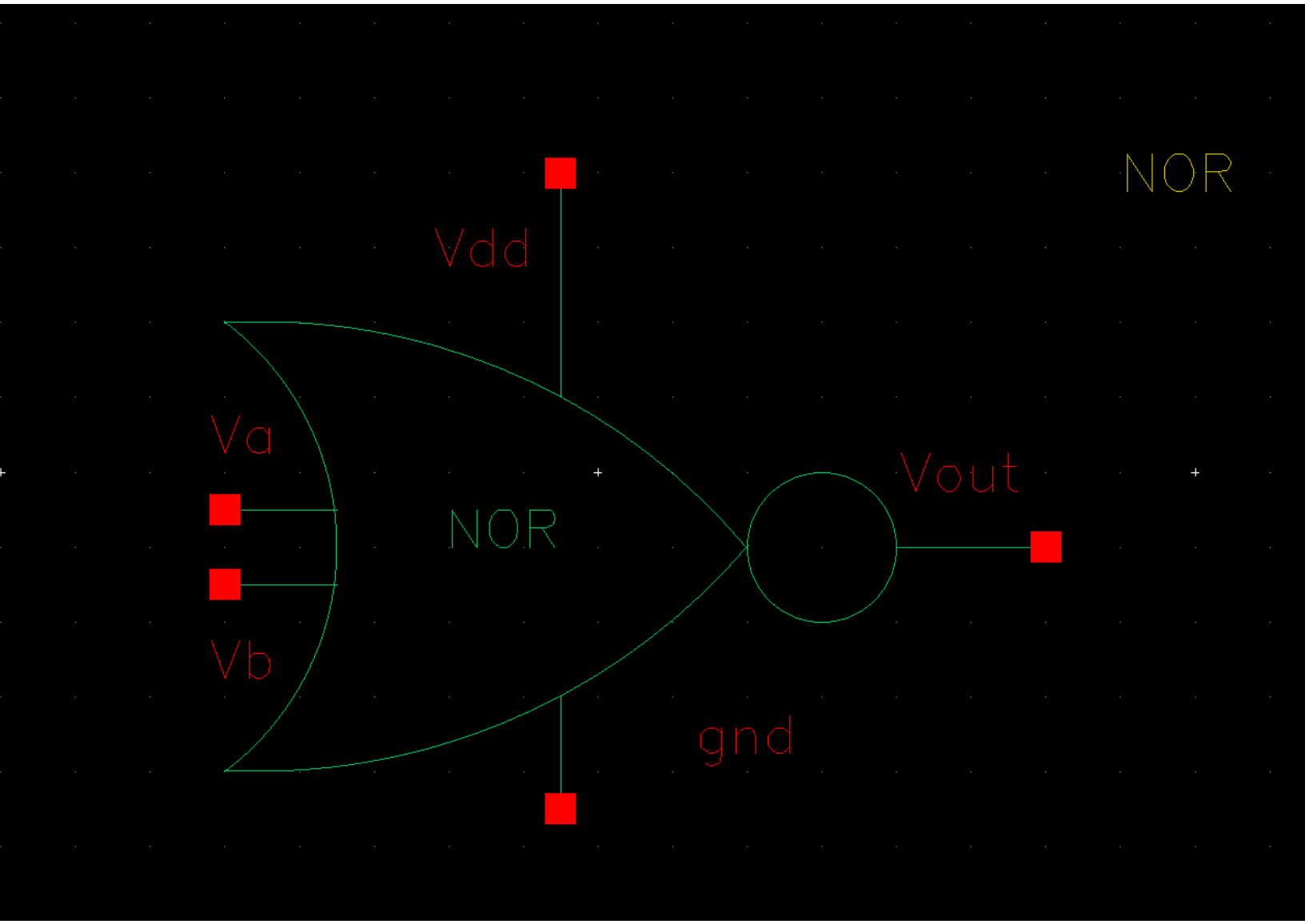
Notice from spectre.
82 notices suppressed.

Aggregate audit (10:56:28 AM, Thur Oct 13, 2022):
Time used: CPU = 502 ms, elapsed = 776 ms, util. = 64.7%.
Time spent in licensing: elapsed = 33.5 ms.
Peak memory used = 97.3 Mbytes.
Simulation started at: 10:56:27 AM, Thur Oct 13, 2022, ended at: 10:56:28 AM, Thur Oct 13, 2022, with elapsed time (wall clock): 776 ms.
spectre completes with 0 errors, 2 warnings, and 12 notices.
~~~~~~

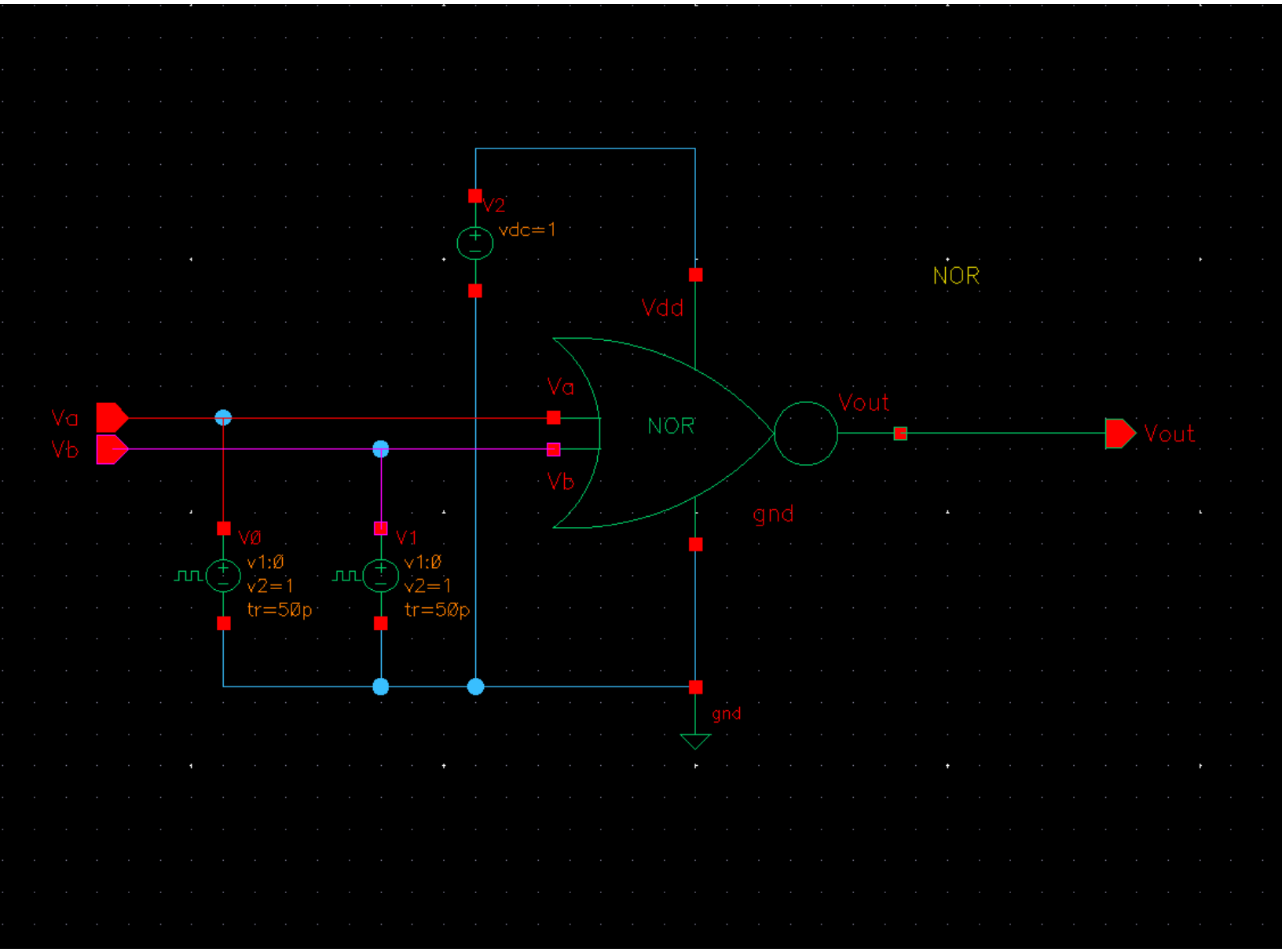
NOR GATE Circuit Schematic ~(A + B)
A 2-input Use: (W/L)n = 1.0/0.045 and (W/L)p = 4.0/0.045



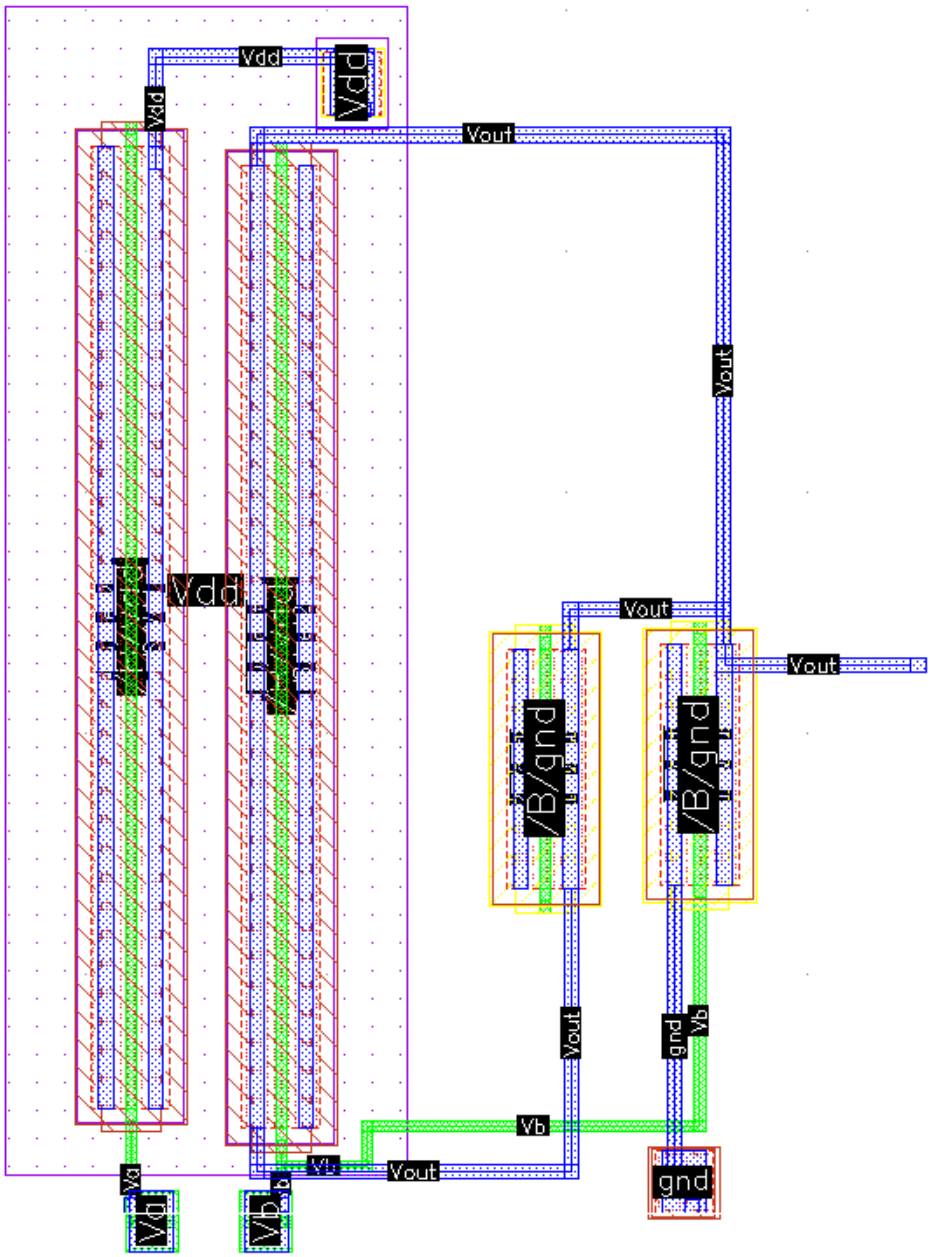
NOR Symbol



NOR Testbench Circuit Schematic



NOR Layout


Vdd
Vdd
Vdd
Vout
Vout
Vout
Vout
Vout
Vout
/B/gnd
/B/gnd
Vb
Vb
Vb
Vb
gnd
gnd
Vb
Vb

NOR DRC / LVS

INFO (BND-1003): Binder initialized for layout cellview 'Project-1.3/NOR/layout' and source cellview 'Project-1.3/NOR/schematic':

	bound	unbound	ungenerated
terminals	0	0	5
nets	0	0	9
instances	0	0	4

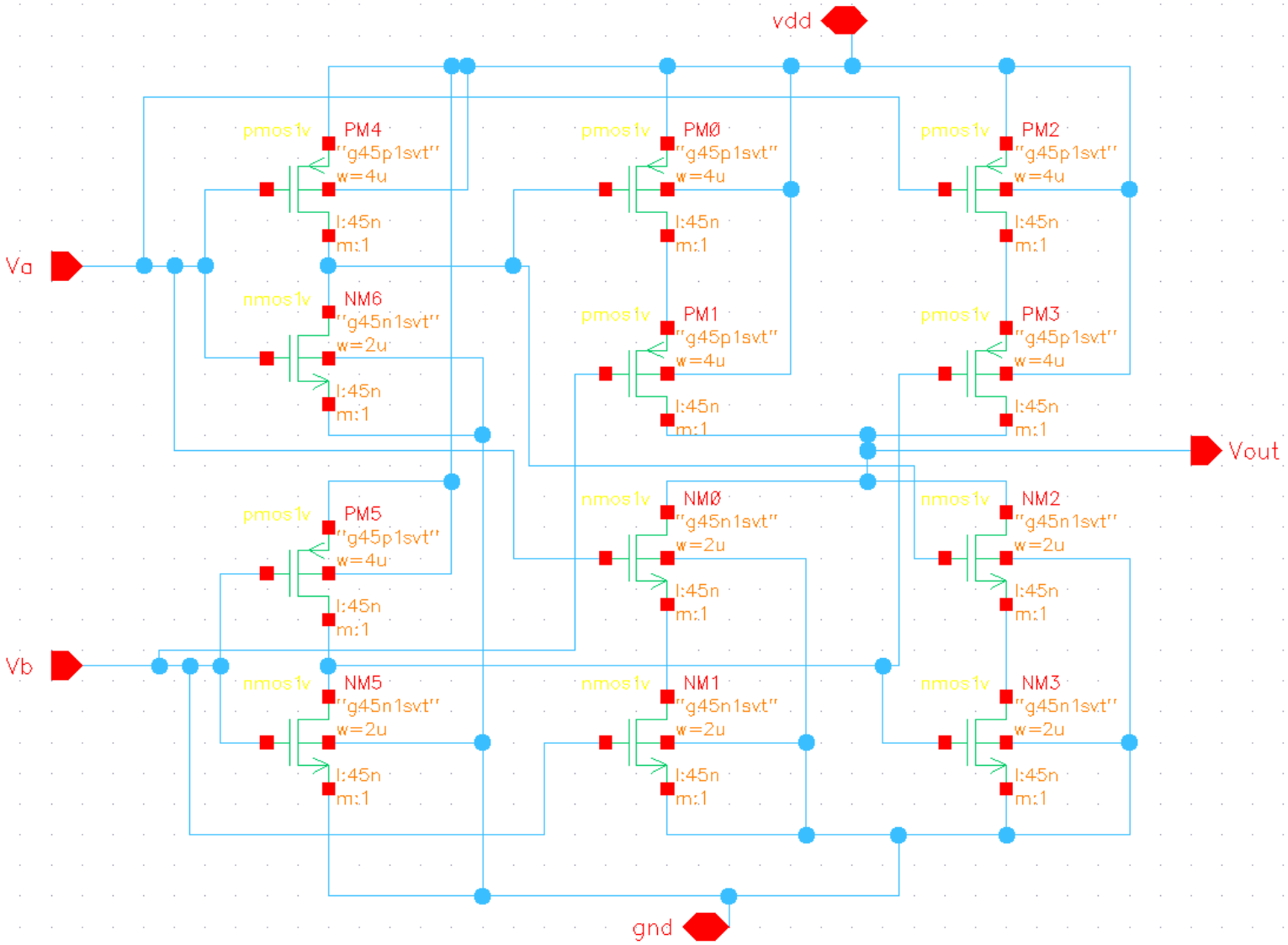
Host is
cmd is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura
/home/student/johnmatthewjimenez/cpe151/NOR.rsf -cdslib
/home/student/johnmatthewjimenez/cpe151/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:11: pid 15949.
WARNING No DRC errors found.

The LVS run "NOR" has completed successfully.

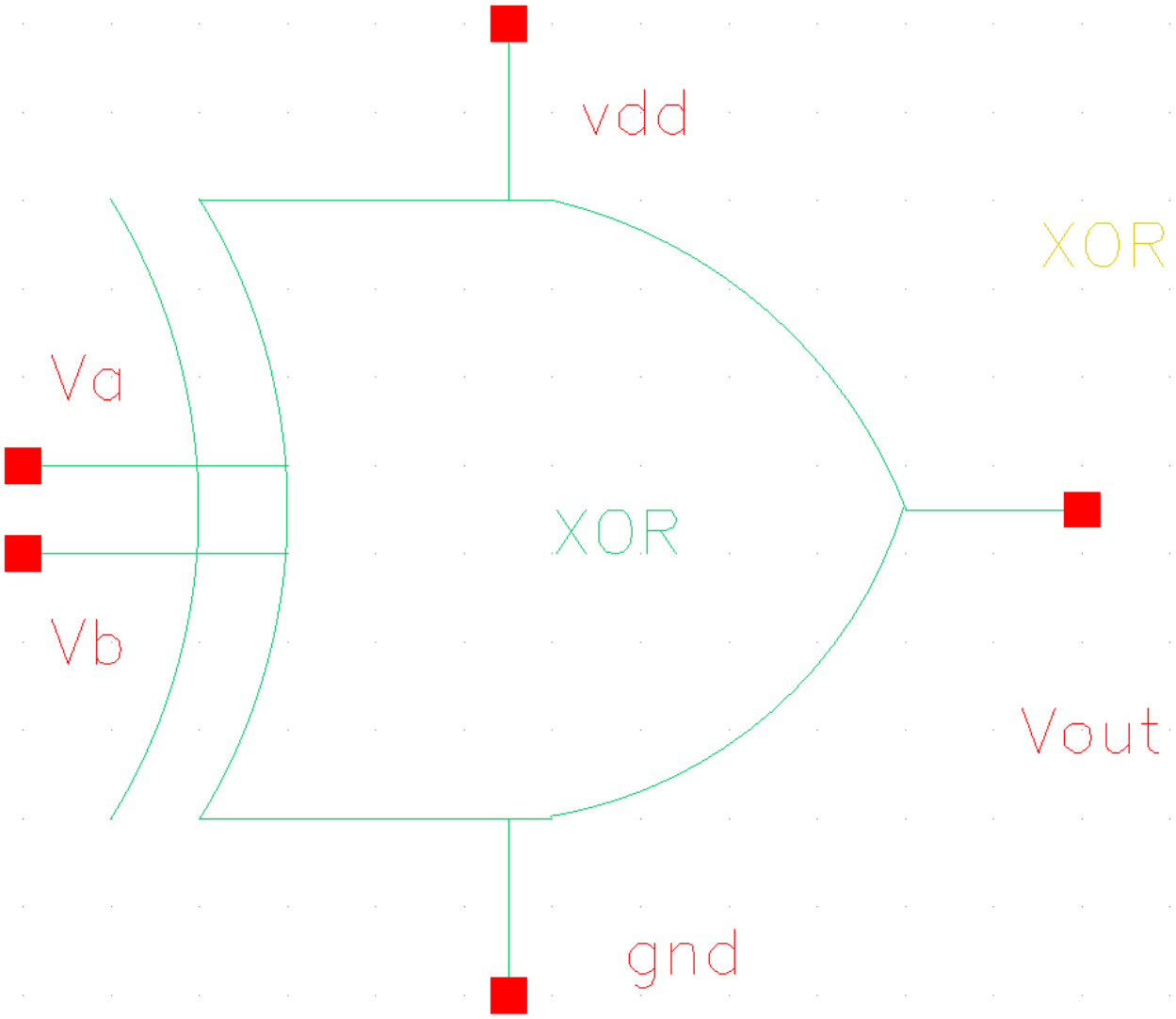
Checking in license for "Phys_Ver_Sys_Results_Mgr"
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
Schematic cell - NOR schematic Project-1.3
Schematic cell - NOR schematic Project-1.3
INFO (LX-1947): Editing 'Project-1.3/NOR/layout' in Layout XL without a connectivity reference can introduce Layout XL compliance issues.
Specify the source schematic using the 'Connectivity - Update - Connectivity Reference' menu command.
INFO (BND-1003): Binder initialized for layout cellview 'Project-1.3/NOR/layout' and source cellview 'Project-1.3/NOR/schematic':

	bound
terminals	5
nets	9
instances	4

XOR GATE Circuit Schematic (A * ~B) + (~A * B)
A 2-input Use: (W/L)n = 2.0/0.045 and (W/L)p = 4.0/0.045

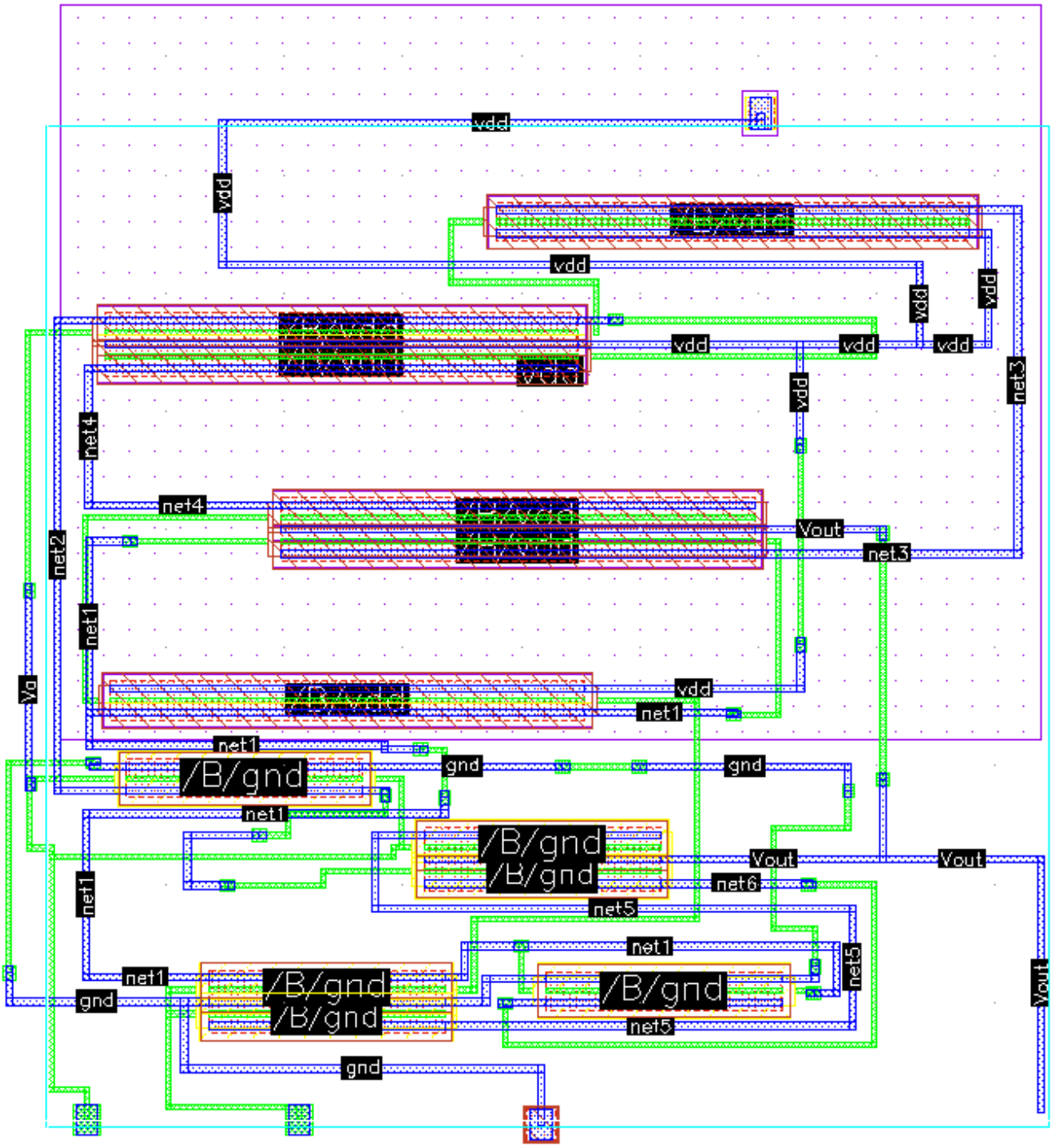


XOR Symbol

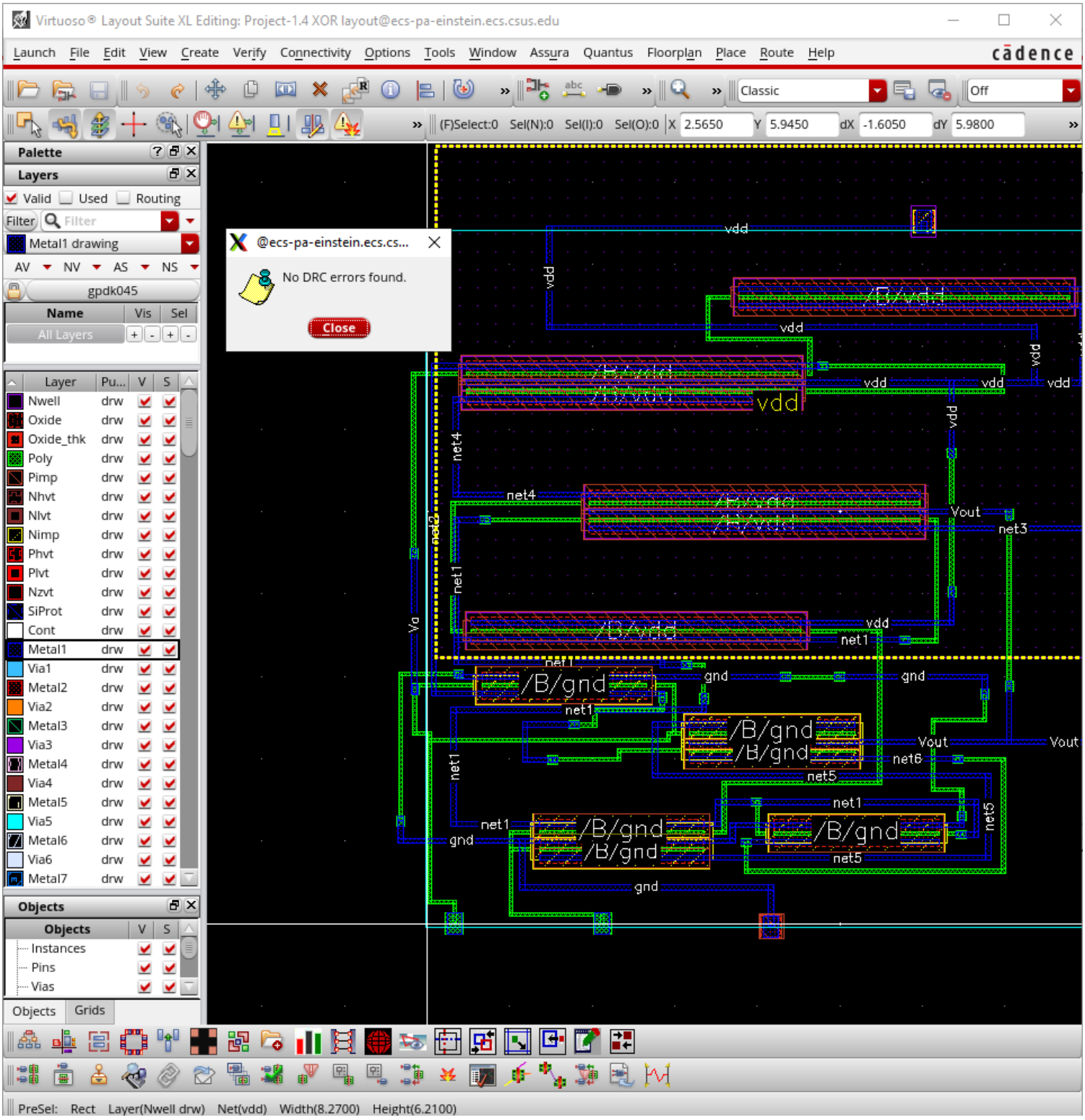


XOR Layout

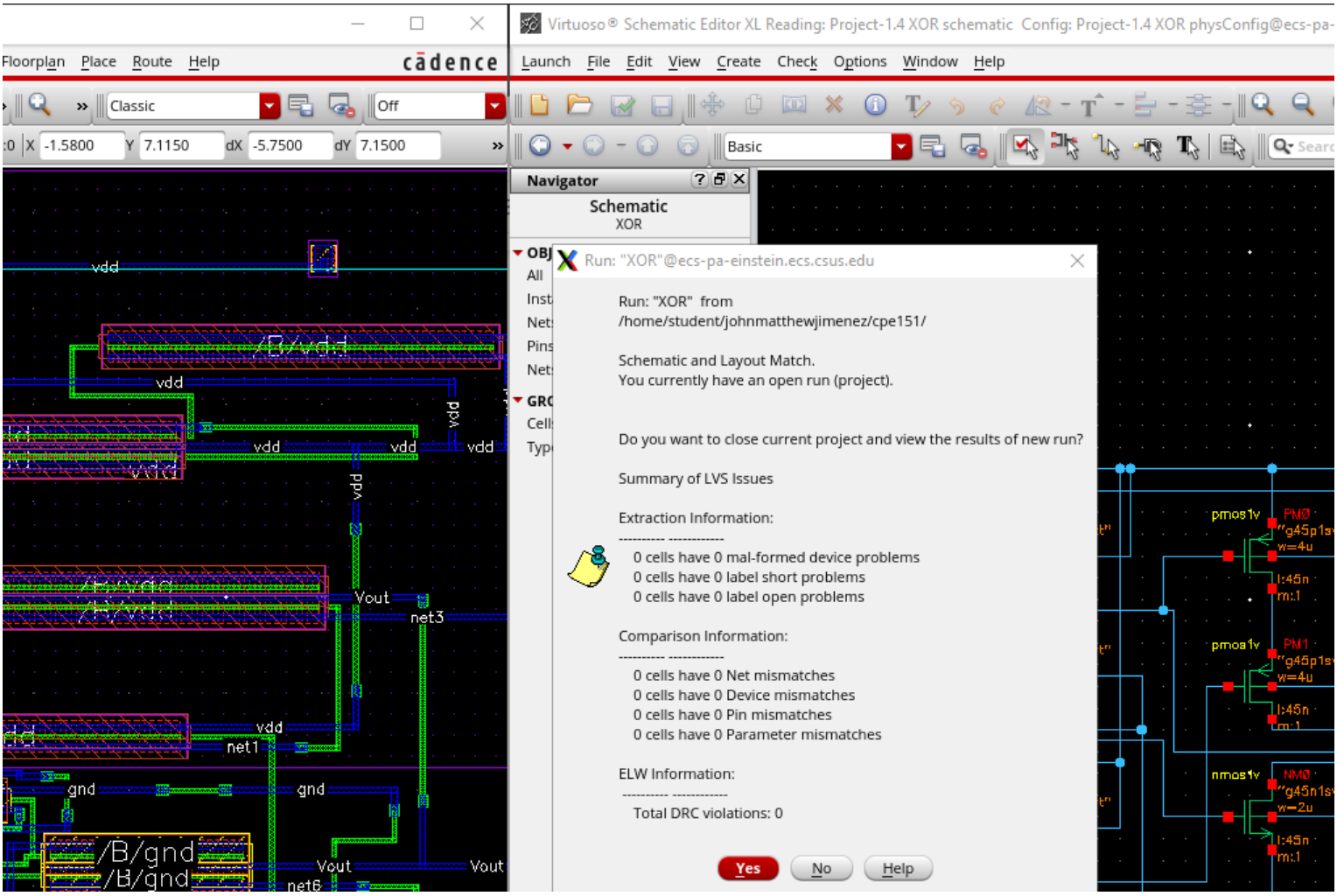
This is my 4th iteration of this layout because the LVS would fail if the nets were not connected, so I did this.



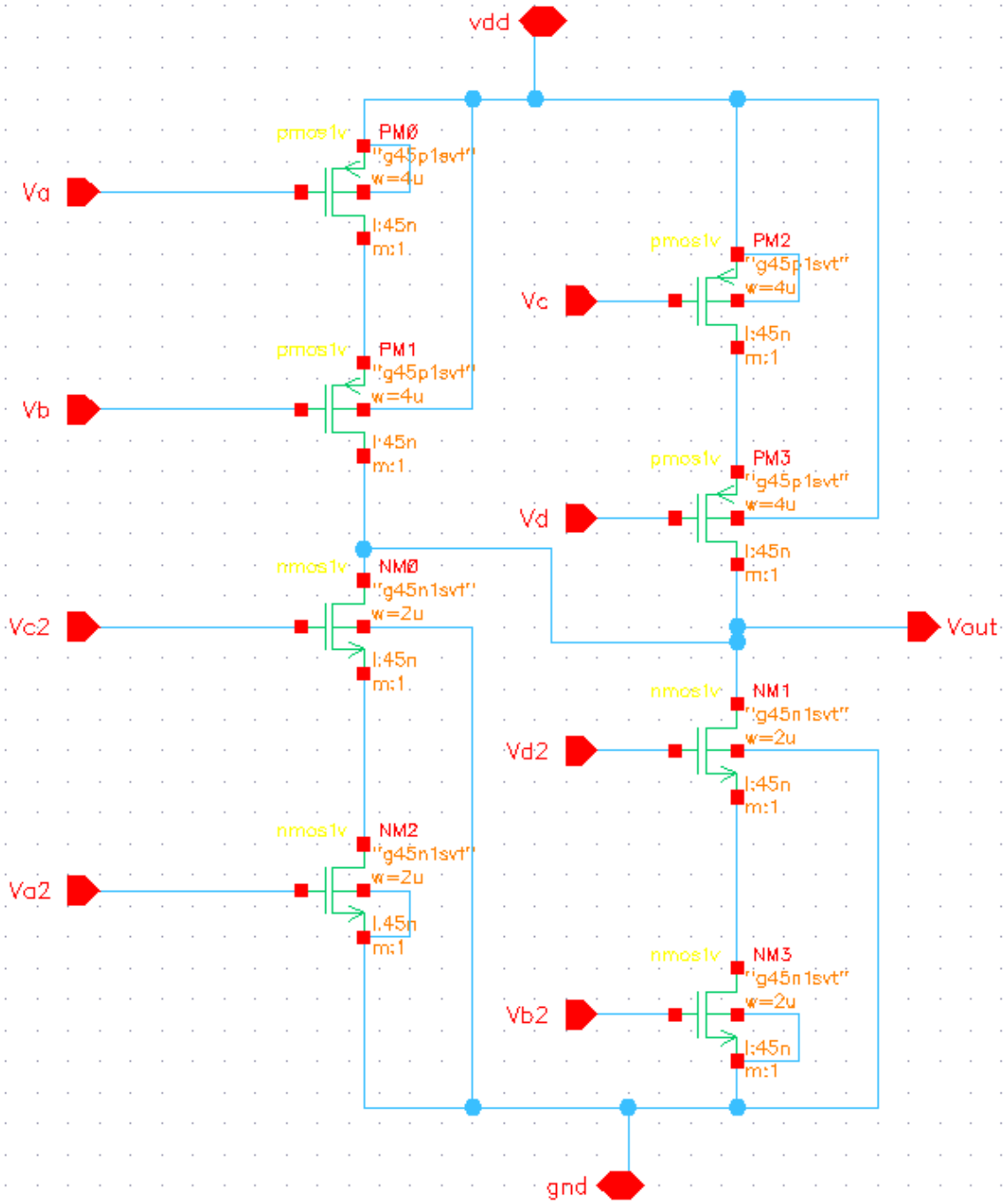
XOR DRC


Virtuoso® Layout Suite XL Editing: Project-1.4 XOR layout@ecs-pa-einstein.ecs.csus.edu
Launch File Edit View Create Verify Connectivity Options Tools Window Assura Quantus Floorplan Place Route Help
cadence
@ecs-pa-einstein.ecs.cs...
No DRC errors found.
Close
Palette
Layers
Valid Used Routing
Metal1 drawing
gpdk045
Objects
Instances
Pins
Vias
Objects Grids
vdd
gnd
net1
net4
net5
net6
Vout
/B/gnd
PreSel: Rect Layer(Nwell drw) Net(vdd) Width(8.2700) Height(6.2100)

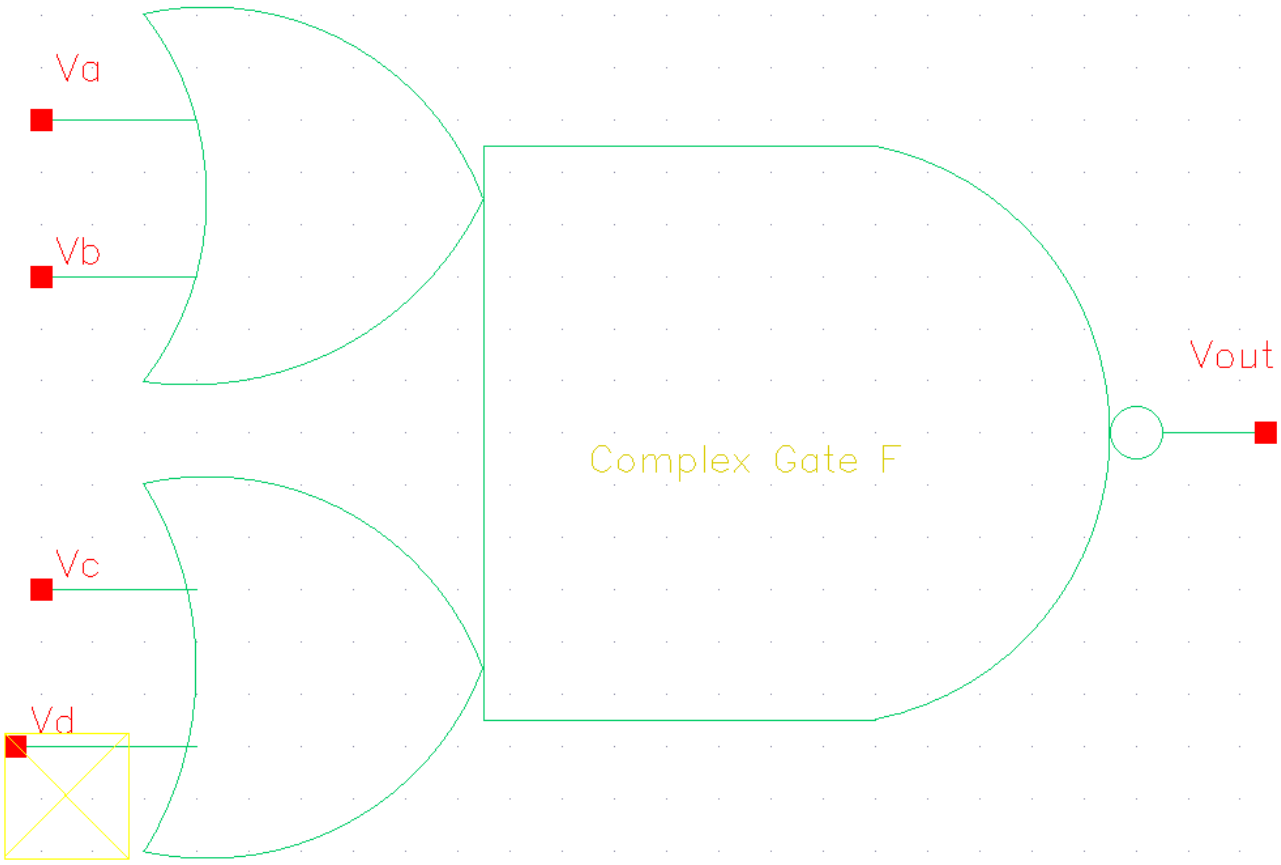
XOR LVS


Floorplan Place Route Help
cadence
Virtuoso® Schematic Editor XL Reading: Project-1.4 XOR schematic Config: Project-1.4 XOR physConfig@ecs-pa-
Launch File Edit View Create Check Options Window Help
Navigator
Schematic
XOR
Run: "XOR"@ecs-pa-einstein.ecs.csus.edu
Run: "XOR" from
/home/student/johnmatthewjimenez/cpe151/
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
Total DRC violations: 0
Yes
No
Help
vdd
gnd
Vout
net3
net1
net6
pmos1v
nmos1v

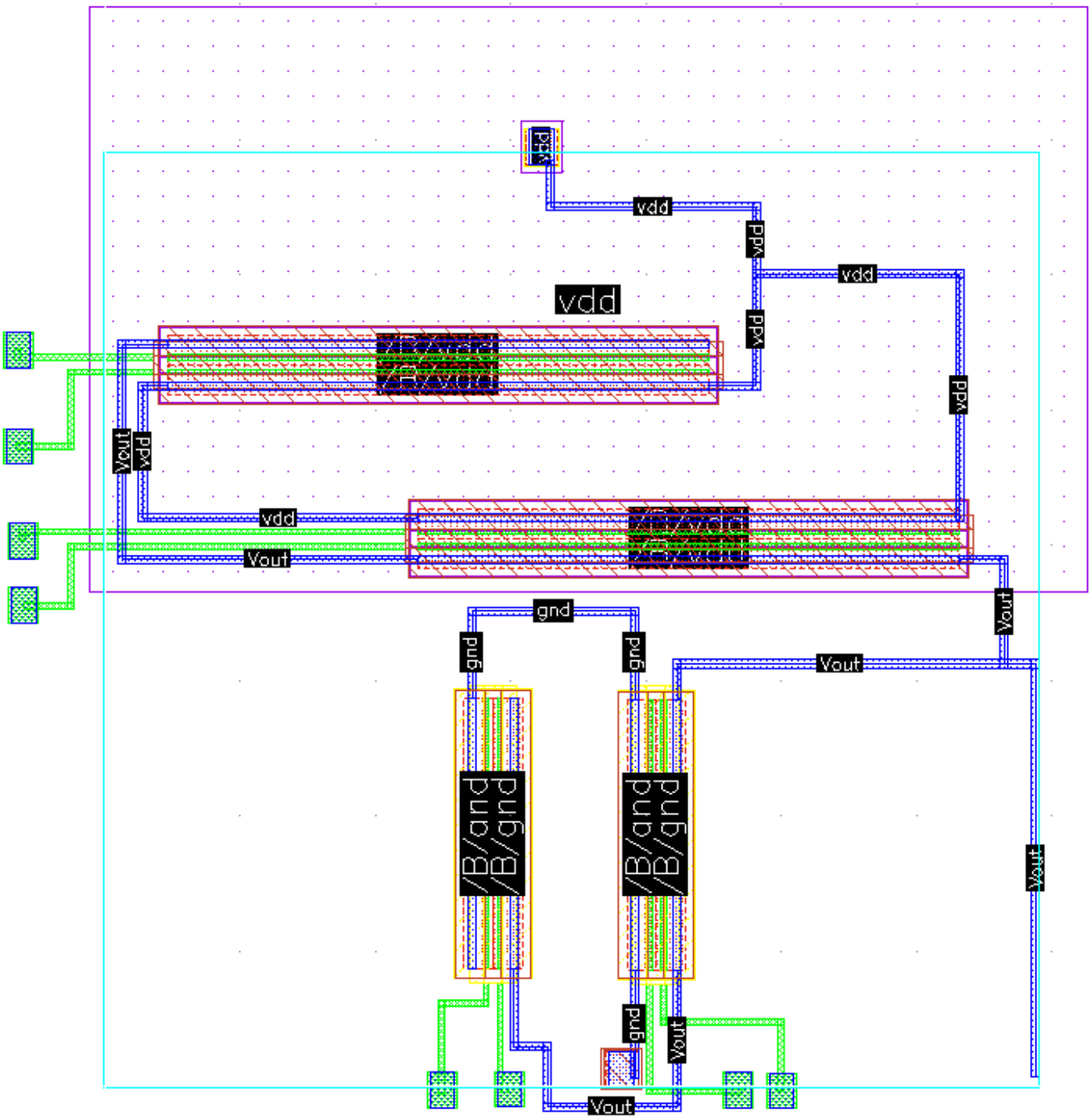
COMPLEX GATE F Circuit Schematic ~((A+B)•(C+D))
Use: (W/L)n = 2.0/0.045 and (W/L)p = 4.0/0.045



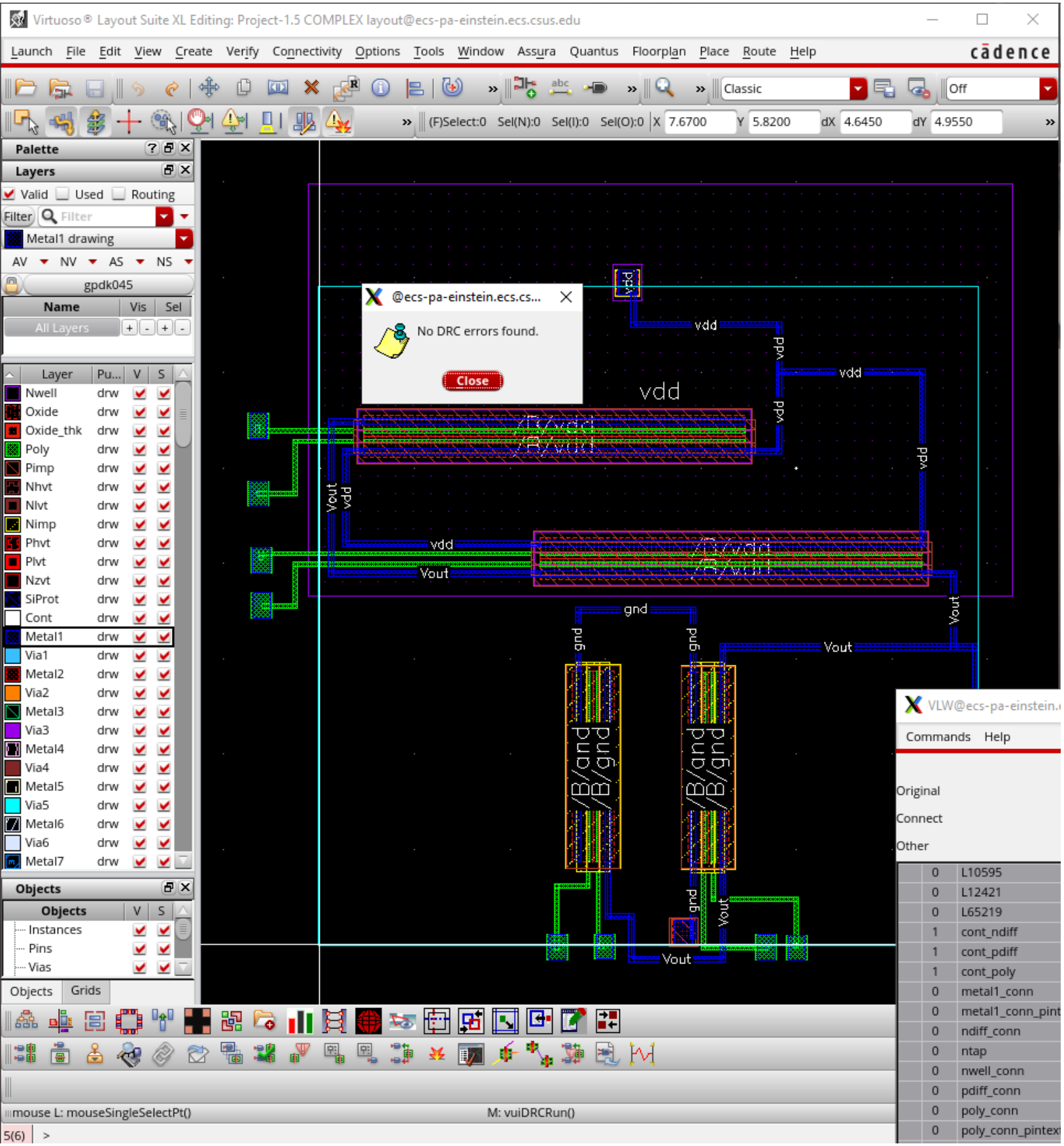
Complex Gate F Symbol



COMPLEX GATE F Layout



COMPLEX GATE F DRC Check



COMPLEX LVS Check