

California State University Sacramento
Electrical and Computer Science Department

EEE 108L Lab - Section 05
Laboratory Experiment Number 4: Lab Report

Single-Supply Operational Amplifiers

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ADDENDUM

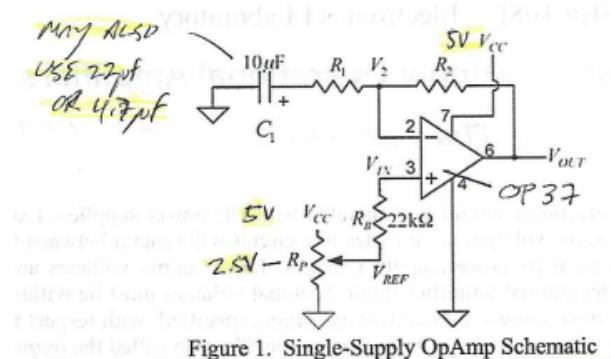
Abstract

For this laboratory experiment we are tasked to experiment on single-supply operational amplifiers in which we will run tests to get a better understanding of what these amplifiers can be used for. With the data collected in this lab report we are able to see results from a simulation stand point and compare it to physical boards of the same circuit. We will be searching for many different data points as seen in the table of contents or in the lab report below.

Part 1: Preliminary Calculations

STEP 1: Theoretical Calculations

For these calculations we must assume that the operational amplifier is ideal. We will be taking a look at figure 1 shown below as a non-inverting amplifier with a single power supply.



For this step we have also chosen the R₁ and R₂ so that the gain will be between 30 and 45.

$$V_{CC} = 5V$$

$$R_P = 5k\Omega \text{ to } 25k\Omega \text{ inclusive,}$$

$$R_1 = 2k\Omega$$

$$R_2 = 68k\Omega$$

$$\text{Gain} = 35$$

STEP 2: Finding the frequency when the reactance of the 10 uF capacitor is equal to the resistance of R1.

Step 1- setting up the equation.

$$2000 = 1 / (2 * \pi * (f) * 10\text{uf})$$

$$f = 1 / (2 * \pi * 2000 * 10\text{uf})$$

$$\text{Freq} = 7.9577$$

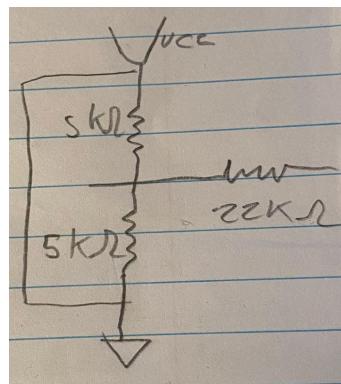
STEP 3: Finding DC Voltages for Vout and V2.

If the Vref = 5V,

With that we know that the Vout and V2 are 5V.

STEP 4: Input Resistance seen looking at the Node

Now assume that the operation amplifier's input resistance is infinite, what is the lowest and highest small-signal resistance seen to ground Vin?

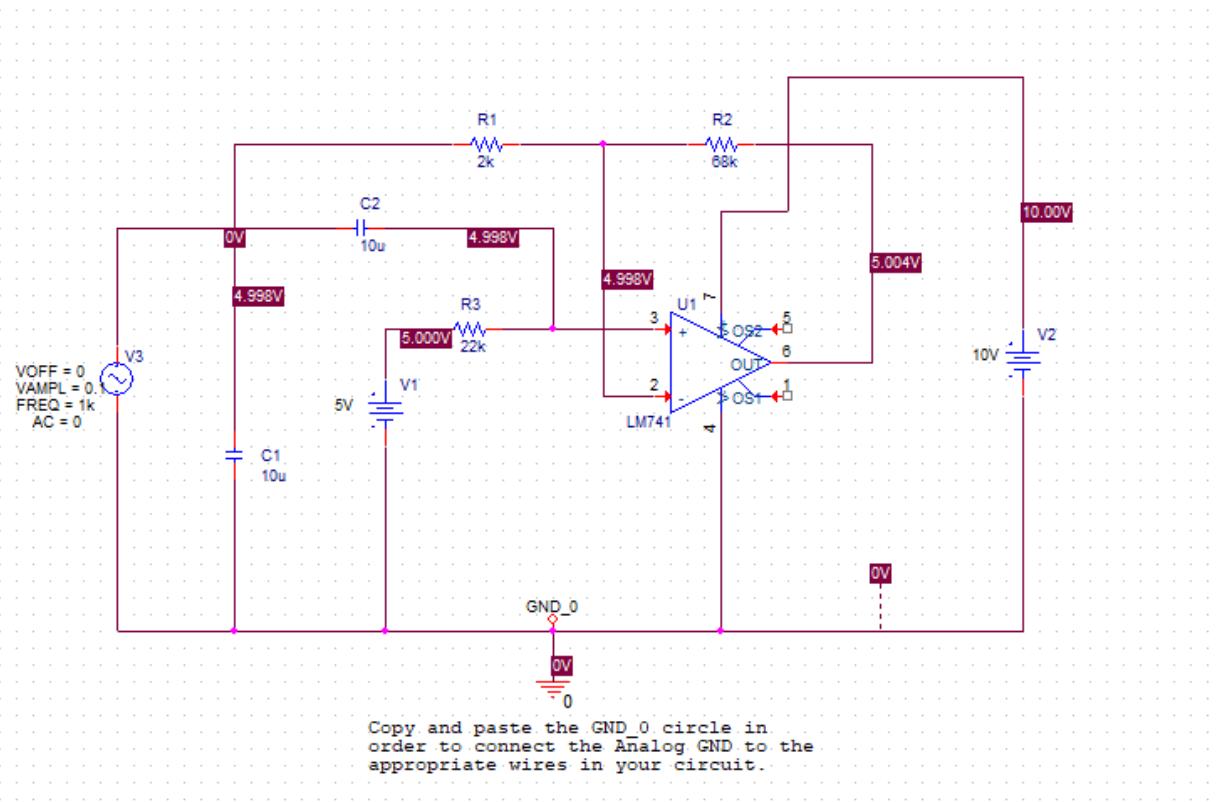


$$Z_{\min} = 22\text{k}$$

$$Z_{\max} = 22\text{k} + 2.5\text{k} = 24.5\text{k} \text{ (middle point has the maximum resistance)}$$

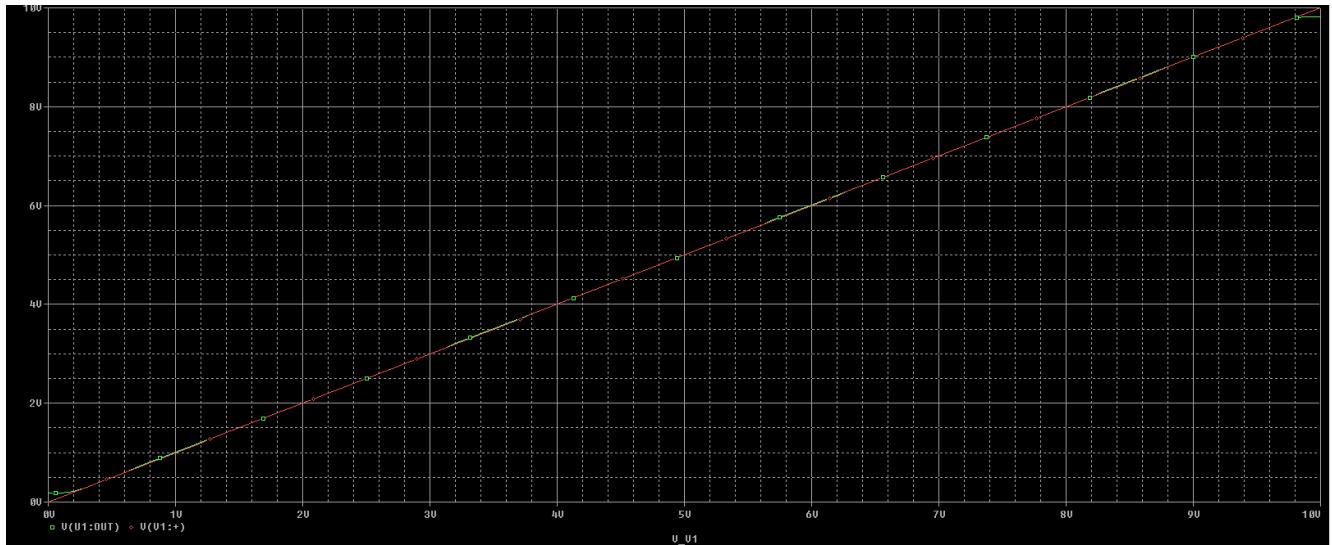
Part 2: PSpice Simulations

STEP 5: Construct circuit on PSpice

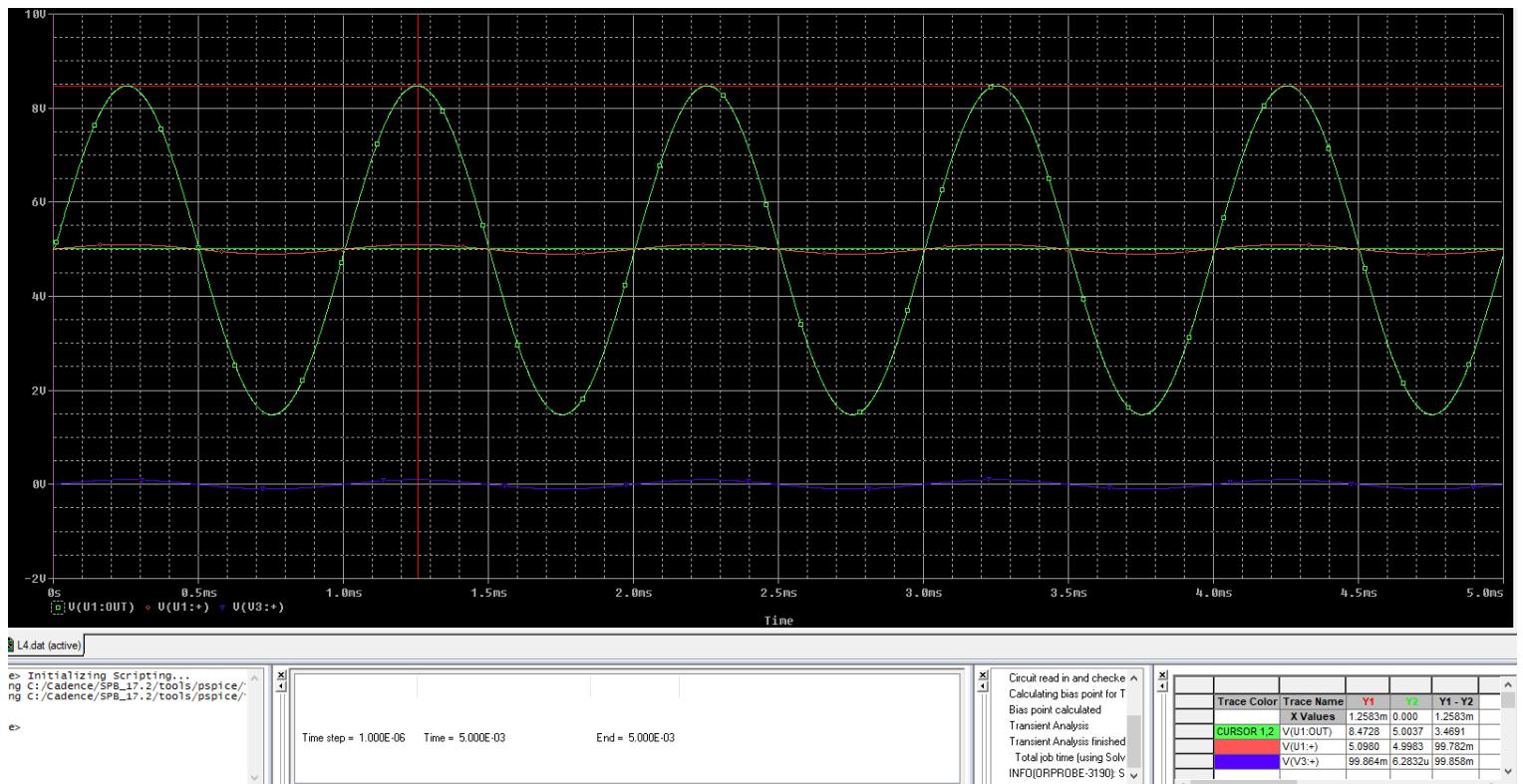


After seeing the results of the readings of the Voltage throughput I agree with the theoretical calculations.

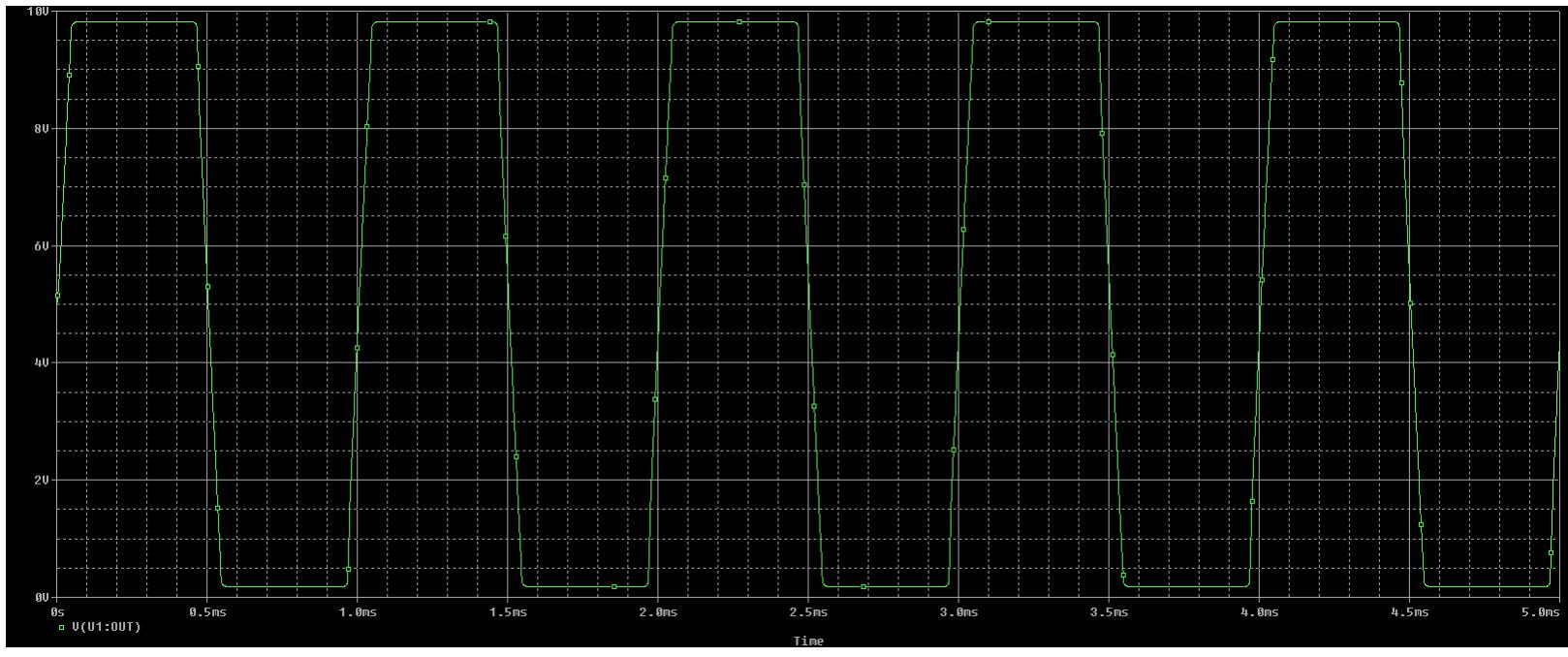
STEP 6: Clipping Levels



STEP 7: AC couple a signal to the Node

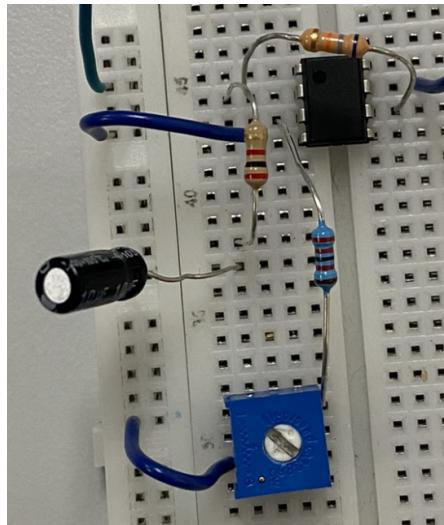


AC sweep response = 24.5V = 7.29 Hz



Part 3: Laboratory Experiment

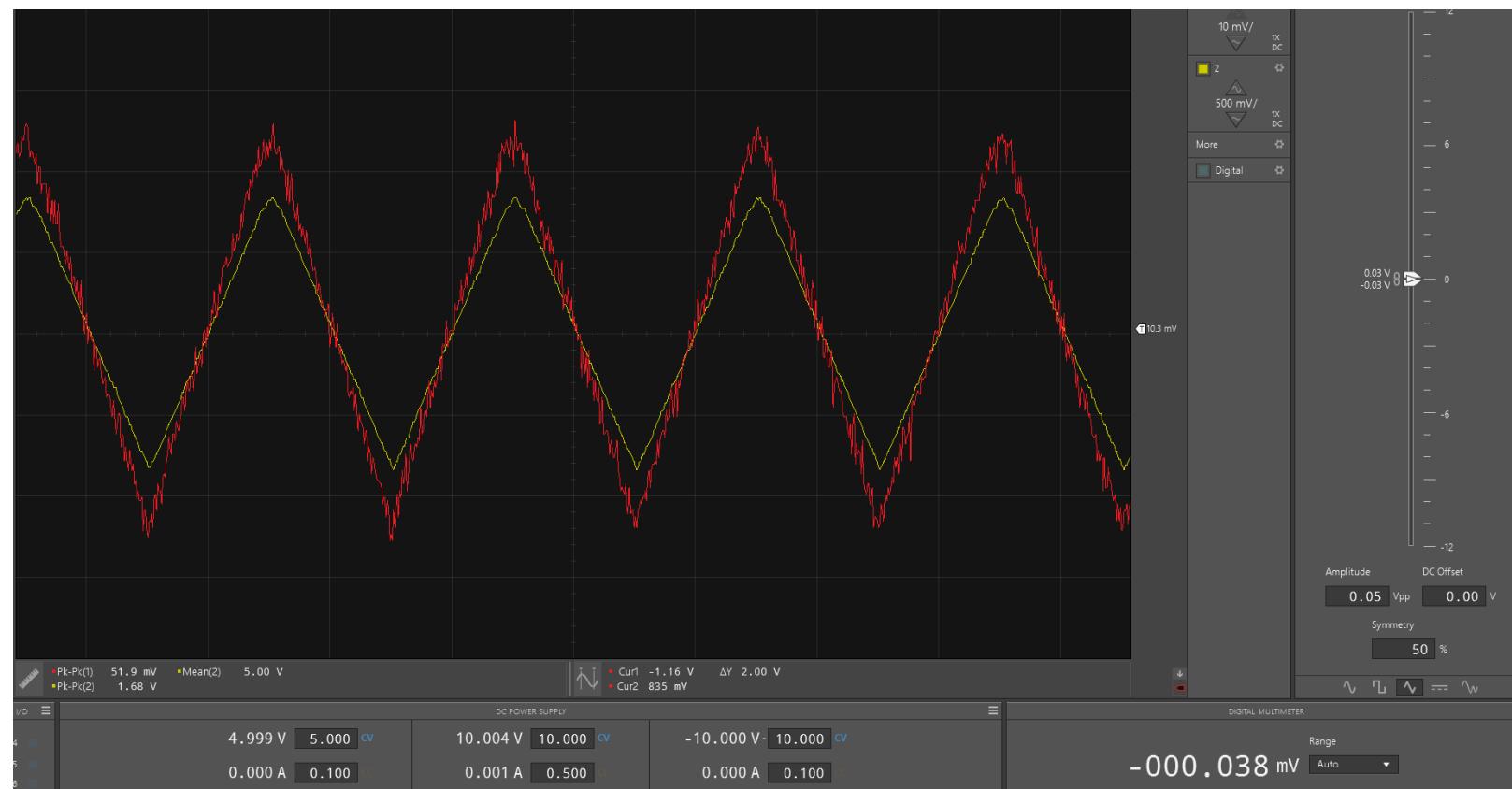
STEP 8: Construct circuit on breadboard



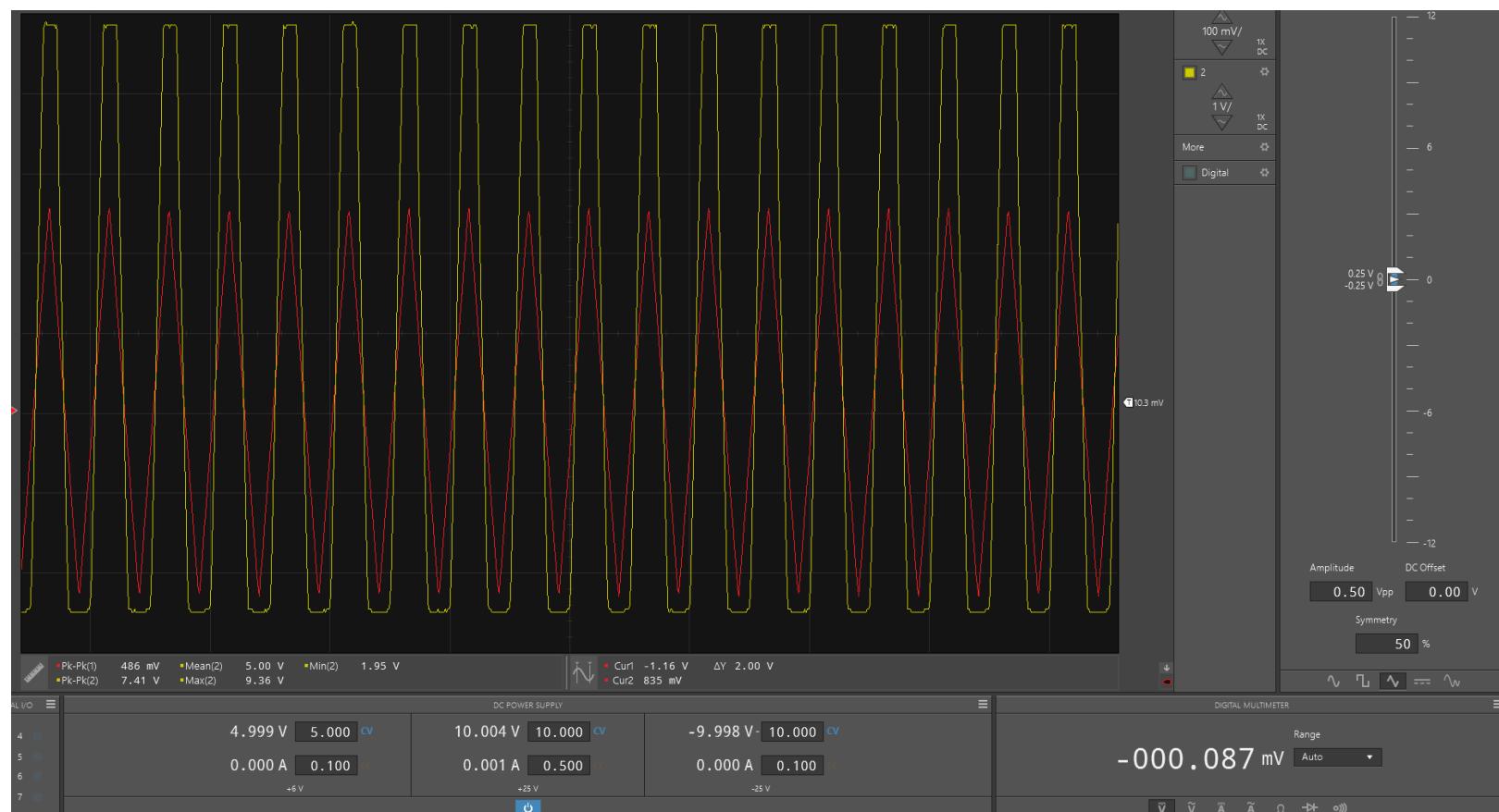
STEP 9: Data table of Vref, Vin, Vout

Vref	Vin	Vout	Gain
4.997	5.0196	5.024	=35

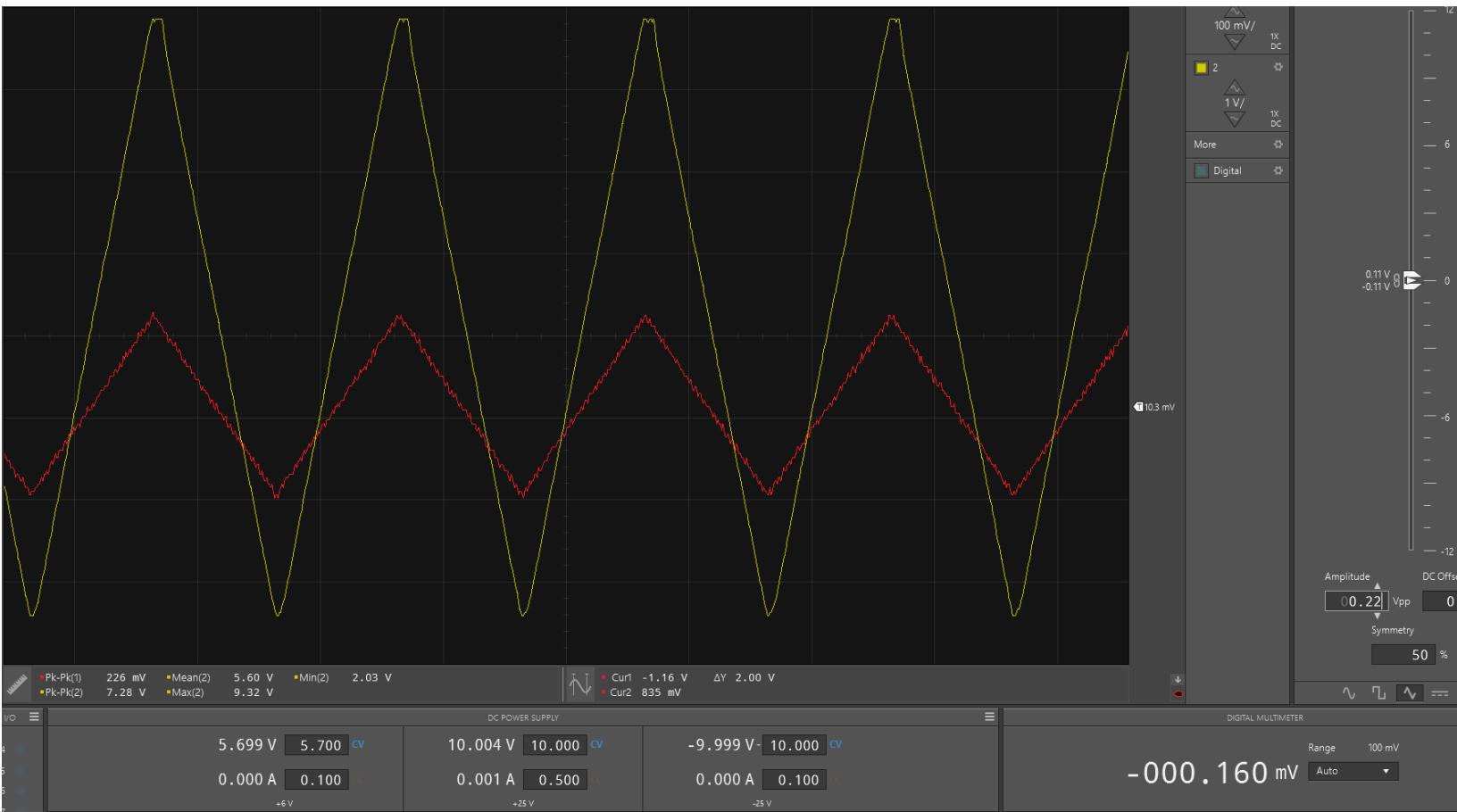
STEP 10: DC Coupling



STEP 11: Measure Maximum and Minimum Clipping Levels

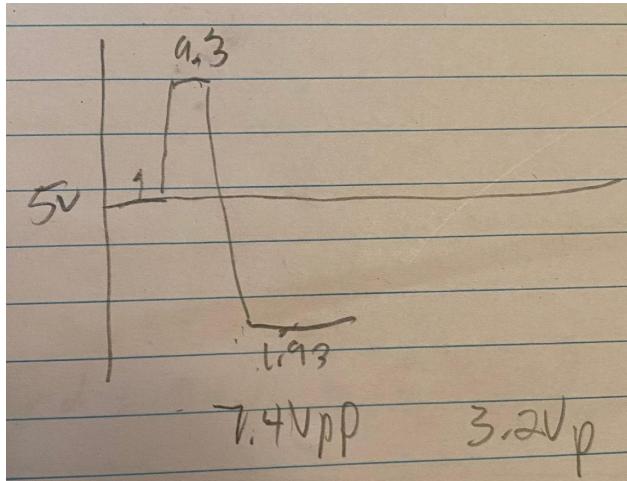


STEP 12: Ac Output Signal Amplitude



STEP 13: Finding the Value of Rref?

No, you can't. This is because the gain will make the signal go to the top and be detected by the DC coupling.



CONCLUSION:

ITEM 2: From the results seen in step 10 about the DC bias, the relationship between the input and output DC bias voltage is that the Vref has to do with the DC Offset.

ITEM 3: $Fp1 = 1/ (2\pi \cdot 10\text{uf} \cdot (22\text{k}\Omega))$, $Fp2 = 1/ (2\pi \cdot 10\text{uf} \cdot (22\text{k}\Omega))$

ITEM 4: For the bias condition found in step 12, it is called the maximum symmetrical clipping. That is the term for that condition because it is at its maximum DC offset which causes it to swing in a positive and a negative direction.

ITEM 5: the DC signal would be exposed to all the gain when removing the capacitor.