Example FPGA

Example Registers Specification

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1 ATXMEGA SPI controller

Register description of Atmel XMEGA AU's SPI controller Transcribed from original manual as an example exercise: http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-8331-8-and-16-bit-AVR-Microcontroller-XMEGA-AU_Manual.pdf

Base Address: 32'h0000_0000
Size(bytes): 0x4

Registers List

Offset	Identifier	Name
32'h0000_0000	CTRL	CTRL
32'h0000_0001	INTCTRL	INTCTRL
32'h0000_0002	STATUS	STATUS
32'h0000_0003	DATA	DATA

1.1 CTRL

Control Register

Absolute Address: 32'h0000_0000
Base Offset: 32'h0000_0000
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[7]	CLK2X	RW	1'h0	CLK2X When this bit is set, the SPI speed (SCK frequency) will be doubled in master mode
[6]	ENABLE	RW	1'h0	ENABLE Setting this bit enables the SPI module. This bit must be set to enable any SPI operations
[5]	DORD	RW	1'h0	DORD DORD decides the data order when a byte is shifted out from the DATA register. When DORD is written to one, the least-significant bit (lsb) of the data byte is transmitted first, and when DORD is written to zero, the most-significant bit (msb) of the data byte is transmitted first
[4]	MASTER	RW	1'h0	MASTER Selects master mode when written to one, and slave mode when written to zero. If SS is configured as an input and driven low while master mode is set, master mode will be cleared
[3:2]	MODE	RW	2'h0	MODE These bits select the transfer mode
[1:0]	PRESCALER	RW	2'h0	PRESCALER Controls the SPI clock rate when configured in master mode

1.2 INTCTRL

Interrupt Control

Absolute Address: 32'h0000_0001
Base Offset: 32'h0000_0001
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[1:0]	INTLVL	RW	2'h0	INTLVL These bits enable the SPI interrupt and select the interrupt level

1.3 STATUS

STATUS

Absolute Address: 32'h0000_0002
Base Offset: 32'h0000_0002
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[7]	IF	RO	1'h0	IF
[6]	WRCOL	RO	1'h0	WRCOL

1.4 DATA

DATA

The DATA register is used for sending and receiving data. Writing to the register initiates the data transmission, and the byte written to the register will be shifted out on the SPI output line. Reading the register causes the shift register receive buffer to be read, returning the last byte successfully received

Absolute Address: 32'h0000_0003
Base Offset: 32'h0000_0003
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[7:0]	RDATA	RO	8'h00	RDATA
[7:0]	WDATA	WO	8'h00	WDATA