



Example FPGA

Example Registers Specification

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1 Trigger Routing Unit

The trigger routing unit (TRU) provides simple sequence control of distributed modules without the penalties associated with core intervention

Base Address: 32'h1000_0000

Size(bytes): 0x2020

Registers List

Offset	Identifier	Name
32'h0000_1FFF	-	-
32'h0000_2000	TRU_SSRN	Slave Select Register
32'h0000_2004	TRU_MTR	Master Trigger Register
32'h0000_2008	-	-
32'h0000_200C	-	-
32'h0000_2010	TRU_ERRADDR	Error Address Register
32'h0000_2014	TRU_STAT	Status Information Register
32'h0000_2018	TRU_GCTL	Global Control Register
32'h0000_201C	TRU_RXDATA	Receive Data Register

1.1 Slave Select Register

The TRU slave select registers (TRU_SSRn) each provide slave selection and register locking.

Absolute Address: 32'h1000_2000
Base Offset: 32'h0000_2000
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31]	LOCK	RW	1'h0	SSRn Lock If the global lock is enabled (SPU_CTL_GLCK bit =1) and the TRU_SSRn.LOCK bit is enabled, the TRU_SSRn register is read only.
[30:8]	RESERVED1	RW	23'h0_0000	Reserved1 Reserved bits
[7:0]	SSR	RW	8'h00	SSRn Slave Select The TRU_SSRn register selects the trigger master ID to which the trigger slave responds. For example, when a TRU_SSRn register is set to respond to trigger master ID n, a trigger that is generated by trigger master ID n results in a trigger out to the slave.

1.2 Master Trigger Register

The TRU master trigger register (TRU_MTR) permits trigger generation through software by writing a trigger master ID value to one of the four fields in the TRU_MTR register. If the global lock is enabled (SPU_CTL_GLCK bit =1) and the TRU_GCTL.LOCK bit is set, the TRU_MTR register is read only.

Absolute Address: 32'h1000_2004
Base Offset: 32'h0000_2004
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:24]	MTR3	RW	8'h00	Master Trigger Register 3
[23:16]	MTR2	RW	8'h00	Master Trigger Register 2
[15:8]	MTR1	RW	8'h00	Master Trigger Register 1
[7:0]	MTR0	RW	8'h00	Master Trigger Register 0

1.3 Error Address Register

The TRU error address register (TRU_ERRADDR) holds the address from the memory mapped register access generating an access error of TRU registers.

Absolute Address: 32'h1000_2010

Base Offset: 32'h0000_2010

Reset: 32'h0000_0000

Access: RW

Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:12]	RESERVED1	RW	20'h0_0000	Reserved1 Reserved bits
[11:0]	ADDR	RW	12'h000	Error Address The TRU_ERRADDR.ADDR holds the address from the memory mapped register access generating an access error of TRU registers. These errors occur on access to the TRU_SSRn or TRU_MTR registers when these registers are locked or on access to an invalid address. See the TRU_SSRn and TRU_MTR register descriptions for more information about locking. The TRU_ERRADDR register holds the address of the first error to occur. In the event of multiple errors occurring, the TRU_ERRADDR register contains the address of the first error. To re-enable the TRU_ERRADDR register for update, both status bits (TRU_STAT.LWERR and TRU_STAT.ADDRERR) in the TRU_STAT register must be cleared.

1.4 Status Information Register

The TRU status register (TRU_STAT) contains the status of TRU_MTR and TRU_SSRn register writes and status of bus read/write errors.

Absolute Address: 32'h1000_2014

Base Offset: 32'h0000_2014

Reset: 32'h0000_0000

Access: RW

Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:2]	RESERVED1	RW	30'h00_0000	Reserved1 Reserved bits
[1]	ADDRERR	RW1C	1'h0	Address Error Status The TRU_STAT.ADDRERR bit is set when an invalid address is provided for an MMR access while the TRU is selected. Writing a one to this bit clears the error indication. The TRU_ERRADDR register also is updated when an address error occurs during an MMR access while the TRU is selected.
[0]	LWERR	RW1C	1'h0	Lock Write Error Status If TRU_STAT.LWERR is set, a lock write error has occurred. Writing a one to this bit clears the error indication.

1.5 Global Control Register

The TRU global control register (TRU_GCTL) provides register locking, TRU reset, and TRU enable.

Absolute Address: 32'h1000_2018

Base Offset: 32'h0000_2018

Reset: 32'h0000_0002

Access: RW

Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31]	LOCK	RW	1'h0	GCTL Lock Bit If the global lock is enabled (SPU_CTL_GLCK bit =1) and the TRU_GCTL.LOCK bit is enabled, the TRU_GCTL register is read only.
[30:3]	RESERVED1	RW	28'h00_0000	Reserved1 Reserved bits
[2]	MTRL	RW	1'h0	MTR Lock Bit If the global lock is enabled (SPU_CTL_GLCK bit =1) and the TRU_GCTL.MTRL bit is enabled, the TRU_MTR register is read only.
[1]	RESET	RW	1'h1	Soft Reset The TRU_GCTL.RESET bit is write-1-action and triggers a soft reset to all TRU registers.
[0]	EN	RW	1'h0	Non-MMR Enable The TRU_GCTL.EN bit is read/write and must be set for the TRU to propagate trigger events. All TRU register read/write operations continue to operate independent of the TRU_GCTL.EN bit.

1.6 Receive Data Register

Used for storing the received data

Absolute Address: 32'h1000_201C
Base Offset: 32'h0000_201C
Reset: 32'h0000_0000
Access: RO
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:0]	RXDATA	RO	32'h0000_0000	Receive Data The Trigger block received data is stored in this field

2 ATXMEGA SPI controller

Register description of Atmel XMEGA AU's SPI controller Transcribed from original manual as an example exercise: http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-8331-8-and-16-bit-AVR-Microcontroller-XMEGA-AU_Manual.pdf

Base Address: 32'h0000_0000

Size(bytes): 0x4

Registers List

Offset	Identifier	Name
32'h0000_0000	CTRL	Control Register
32'h0000_0001	INTCTRL	Interrupt Control
32'h0000_0002	STATUS	STATUS
32'h0000_0003	DATA	DATA

2.1 Control Register

Absolute Address: 32'h0000_0000
Base Offset: 32'h0000_0000
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[7]	CLK2X	RW	1'h0	CLK2X When this bit is set, the SPI speed (SCK frequency) will be doubled in master mode
[6]	ENABLE	RW	1'h0	ENABLE Setting this bit enables the SPI module. This bit must be set to enable any SPI operations
[5]	DORD	RW	1'h0	DORD DORD decides the data order when a byte is shifted out from the DATA register. When DORD is written to one, the least-significant bit (lsb) of the data byte is transmitted first, and when DORD is written to zero, the most-significant bit (msb) of the data byte is transmitted first
[4]	MASTER	RW	1'h0	MASTER Selects master mode when written to one, and slave mode when written to zero. If SS is configured as an input and driven low while master mode is set, master mode will be cleared
[3:2]	MODE	RW	2'h0	MODE These bits select the transfer mode
[1:0]	PRESCALER	RW	2'h0	PRESCALER Controls the SPI clock rate when configured in master mode

2.2 Interrupt Control

Absolute Address: 32'h0000_0001
Base Offset: 32'h0000_0001
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[1:0]	INTLVL	RW	2'h0	INTLVL These bits enable the SPI interrupt and select the interrupt level

2.3 STATUS

Absolute Address: 32'h0000_0002
Base Offset: 32'h0000_0002
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[7]	IF	RO	1'h0	IF
[6]	WRCOL	RO	1'h0	WRCOL

2.4 DATA

The DATA register is used for sending and receiving data. Writing to the register initiates the data transmission, and the byte written to the register will be shifted out on the SPI output line. Reading the register causes the shift register receive buffer to be read, returning the last byte successfully received

Absolute Address: 32'h0000_0003
Base Offset: 32'h0000_0003
Reset: 8'h00
Access: RW
Size(bytes): 0x1

Fields List

Bits	Identifier	Access	Reset	Name / Description
[7:0]	RDATA	RO	8'h00	RDATA
[7:0]	WDATA	WO	8'h00	WDATA