FINGERPRINTS

Product Specification

FPC1140A

ASIC

Revision PA3

Contents

1 Overview

The FPC1140 is a capacitive touch fingerprint sensor with low power consumption, specifically developed and optimized for mobile devices. The FPC1140 sensor offers smartphone, tablet and PC OEMs the opportunity to relieve consumers from the burden of using PIN codes and passwords for user verification. The FPC1140 sensor includes the following features:

- Fingerprint area sensor
- Superior 3D image quality
- 508 dpi resolution
- 56 x 196 pixels with 8-bit depth
- High-speed SPI interface
- Ultra-low power consumption
- 1.8 Volt operation
- Extended ESD range 30kV
- Wake-up functionality

Securing mobile devices, mobile payments, accessing cloud services, and assigning shortcuts to different fingers are among the use cases for the FPC1140 sensor. The FPC1140 enables OEMs to offer consumers a compelling user experience combining convenience and security with performance and design.

The robustness, low cost and size of the FPC1140 fingerprint sensor make it ideal for integration into cost-sensitive consumer electronics, such as mobile phones and tablets. In addition, the low power consumption makes it very attractive for use in battery-powered devices.

1.1 General Description

The FPC1140 sensor series is built around Fingerprint Cards (FPC) proprietary CMOS implementation with high-speed serial interface, offering high-resolution fingerprint images. The FPC1140 interface includes:

- Interrupt (finger detect) and reset
- Support for ESD protection

To integrate the FPC1140 sensor into a biometric system, only a few additional low-cost, passive components are required, including a Transient Voltage Suppressor (TVS) for Electrostatic Discharge (ESD) protection purposes, and RC filters. The sensor is easily configured using a few simple software commands sent over high-speed SPI interface and can be soldered to a PCB or flex cable.

The FPC1140 delivers superior image quality, with 256 greyscale values in each pixel. Fingerprint images are delivered in a raw and unprocessed format from the sensor.

2 Functional Description

This chapter includes a functional description of an FPC1140 sensor.

2.1 Technical Features

An overview of the technical features of an FPC1140 sensor is shown in Table 1.

Parameter	Description	Value	Unit
Weight	Sensor body	<1	gram
Sensing array	Active pixel matrix	56 x 192	pixel
Die size	Cut die, assuming 30 µm saw blade	3090 * 11090	µm
Sensing area	Size of active pixel matrix	2800 * 9600	µm
Spatial resolution	-	508	dpi
Pixel resolution	256 greyscale levels	8	bit
Interface	SPI + IRQ + CS	4+1	Pin
SPI Clock	Frequency (Recommended 8 Mhz)	<12	MHz
Supply voltage	VDD, typical during image capture (IO voltage 1.8 - 3.3)	1.8	V
Supply current*	During Image capture	5	mA
	Sleep mode	2	µA
	Deep Sleep Mode	1	µA
	Idle	0.7	mA
	Wait for finger	1.7	mA

**preliminary*

Table 1: Technical features

2.2 Block Diagram

The FPC1140 electrical interface, including the high-speed serial interface is illustrated in Figure 1.

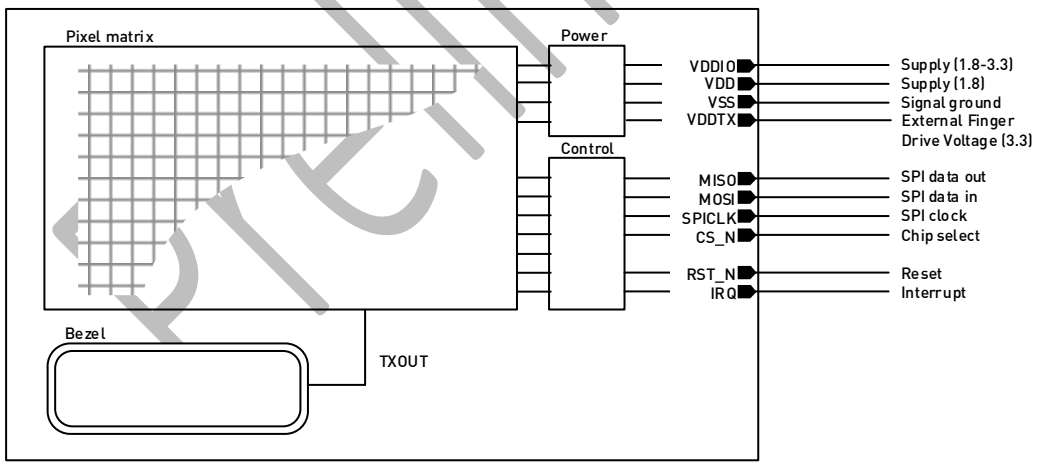

Figure 1: Block Diagram Overview

2.3 Signal List

An overview of the types of signals used for an FPC1140 sensor is shown in Table 2.

Name	Signal Type	Description
VDDIO	Supply	I/O power supply
VSSIO	Supply	I/O ground supply
SPICLK	Digital Input	SPI clock
CS_N	Digital Input	SPI chip select
MISO	Digital Output	SPI data out
MOSI	Digital Input	SPI data in
RST_N	Digital Input	System reset
VSSD	Supply	Digital ground
VDD	Supply	Core power supply
IRQ	Digital Output	Interrupt request
TEST	Input	Reserved
VDDA	Supply	Analog power supply
VSSA	Supply	Analog ground
TXOUT	Output	Drive signal
VDDTX	Supply	Power Supply TXOUT

Table 2: Signal list overview

2.4 Absolute Maximum Ratings

Absolute maximum values for the FPC1140 sensor are shown in Table 3. These values as are intended as a stress rating, where stress beyond the stated values may cause permanent damage to the device. Functional operation of the device, at these or other conditions beyond those indicated as normal operation in this specification, is not implied or supported.

Parameter	Absolute maximum value	Unit
VDD	-0.5 to +2.5	V
VDDD	-0.5 to +4.6	V
VDDA	-0.5 to +2.5	V
Operating temperature	- 40 to + 85	˚C
Storage temperature	- 40 to + 85	˚C

Table 3: Absolute maximum ratings

Exposure to absolute maximum rating conditions for extended periods, may affect device reliability. Operation of the device conditions beyond those indicated as normal operation in this specification, is not supported.

2.5 Image Quality

The FPC1140 sensor is an 56 x 192 pixel matrix with a total of 10752 pixels. Each sensor is tested to verify the image quality and establish a proper signal-to-noise ratio (SNR). If a pixel is not fully operational, it is refererred to as a pixel error (PE). A small number of PE do not degrade biometric performance.

See section 0

Pixel Errors for more details.

2.5.1 Pixel Errors

A PE is defined as a pixel value that deviates more than 20 lsb (least significant bit) - grayscale levels - from its local image median. The local image median is the median value over a sub-image consisting of 5 complete rows, where one of the rows contains the error pixel.

- The number of acceptable pixel errors is ≤ 10
- The number of PEs allowed in a finger-detect area is 0

Checkerboard and Inverted Checkerboard test patterns are generated to calculate the median and identify bad pixels.

2.6 Sensor Modes

Sensor modes for the FPC1140 sensor include:

- Idle mode (default)
- Image capture
- Sleep mode
- Deep sleep mode
- Wait for finger

See section 4.8 Sensor Modes for more information.

3 Electrical Characteristics

The following section describes the electrical characteristics of an FPC1140 sensor.

3.1 1.8 V I/O Applications

The following tables show the recommended operating conditions for 1.8V I/O applications measured at room temperature (RT) with an SPI frequency of 8 MHz.

3.1.1 Power Supply

An overview of the power supplies for 1.8V I/O applications is shown in Table 4.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD	Core Voltage supply	1.62	1.8	1.98	V
VDDA	Analog Voltage supply	1.62	1.8	1.98	V
VDDIO	IO Voltage supply	1.62	1.8	1.98	V
VDDTX	Finger Drive Voltage supply	2.97	3.3*	3.63	V

**recommended*

Table 4: Power Supply for 1.8 V I/O applications

3.1.2 Current Consumption

An overview of the curent consumption for 1.8V I/O applications is shown in Table 5.

Symbol	Parameter	Mode	Typical	Unit
IDD	Core current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA
IDDA	Analogue current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA
IDDIO	IO current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA
IDDTX	Analogue current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA

Table 5: Current Consumption 1.8 V I/O applications

3.1.3 Digital Inputs

An overview of the digital inputs for 1.8V I/O applications is shown in Table 6.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIL	Logic '0' voltage	-0.3	-	0.35*VDD	V
VIH	Logic '1' voltage	0.65*VDD	-	VDD+0.3	V
IIL	Input leakage current	-	-	±10	µA
VT+	Schmitt trigger Low to High threshold point	0.95	0.99	1.00	V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
RPU	Pull- up Resistor	94	148	261	KΩ
RST_N	Reset Signal	-	0.465	-	V

Table 6: Digital Inputs for 1.8 V I/O applications

3.1.4 Digital Outputs

An overview of the digital outputs for 1.8V I/O applications is shown in Table 7.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VOL	Logic '0' output voltage	-	-	0.45	V
VOH	Logic '1' output voltage	VDDIO-0.45	-	-	V

Table 7: Digital Outputs for 1.8 V I/O applications

3.2 3.3V I/O Applications

The following tables show the Recommended Operating Conditions for 3.3V I/O applications measured at room temperature (RT) and SPI clock frequency of 7,7 MHz.

3.2.1 Power Supply

An overview of the recommended power supply for 3.3V I/O applications is shown in Table 8.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD	Core Voltage supply	1.62	1.8	1.98	V
VDDA	Analog Voltage supply	1.62	1.8	1.98	V
VDDIO	IO Voltage supply	2.97	3.3	3.63	V
VDDTX	Finger Drive Voltage supply	2.97	3.3	3.63	V

Table 8: Power supplies for 3.3 V I/O applications

3.2.2 Current Consumption

An overview of the curent consumption for 3.3 V I/O applications is shown in Table 5.

Symbol	Parameter	Mode	Typical	Unit
IDD	Core current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA
IDDA	Analogue current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA
IDDIO	IO current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA
IDDTX	Analogue current	Image capture	TBD	mA
		Sleep	TBD	µA
		Deep sleep	TBD	µA
		Idle	TBD	mA
		Wait for finger present	TBD	mA

Table 9: Current Consumption 3.3 V I/O applications

3.2.3 Digital Inputs

An overview of digital inputs for 3.3V I/O applications is shown in Table 10.

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIL	Logic '0' voltage	-0.3	-	0.8	V
VIH	Logic '1' voltage	2.0	-	3.6	V
IIL	Input leakage current	-	-	±10	µA
VT+	Schmitt trigger Low to High threshold point	0.95	0.99	1.00	V
RPU	Pull- up Resistor	94	148	261	kΩ
RST_N	Reset Signal	-	0.465	-	V

Table 10: Digital inputs for 3.3 V I/O applications

3.2.4 Digital Outputs

An overview of the digital outputs for 3.3V I/O applications in shown in Table 11.

Symbol	Parameter	Typical	Unit
VOL	Logic '0' output voltage	0.4	V
VOH	Logic '1' output voltage	2.4	V

Table 11: Digital outputs for 3.3 V I/O applications.

4 Functionality

This chapter describes the main functionality of the FPC1140 sensor chip, including:

- Analog to Digital conversion
- Command Interpretation
- External Finger Drive Voltage
- Finger detection logic
- Host Interface
- Image properties
- Pixel Matrix Control
- Pixel Sensing Matrix
- Power Reset

4.1 Principal Block Diagram

The principal block diagram for the sensor chip is shown in Figure 2.

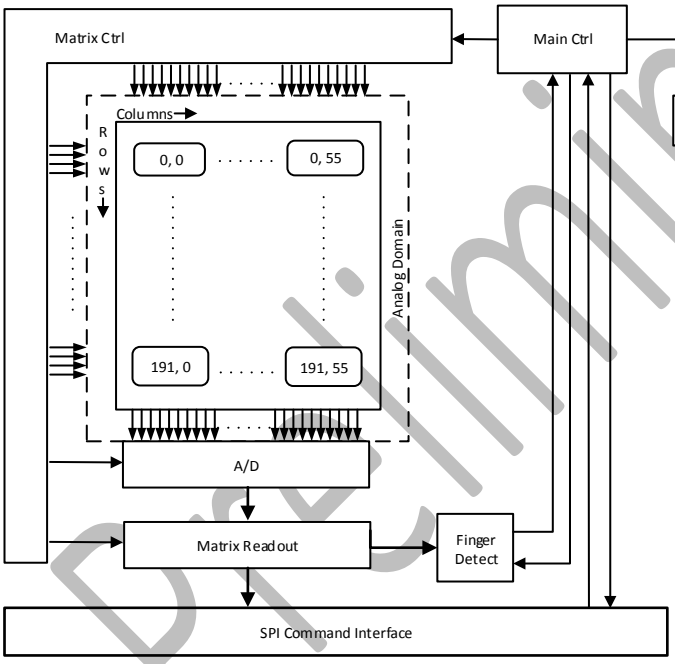

Figure 2: Sensor block diagram.

Key features of the pixel grid sensor include:

- Size: 56 columns x 192 rows
- Resolution: 508 dpi
- Pixel area: 50 µm x 50 µm
- High-speed SPI
- A/D converter

4.2 Host Communication Interface

For host control and fast image data readout, the sensor circuit includes a 4-wire Serial Peripheral Interface (SPI) and an interrupt signal.

- When the internal clocks are calibrated, the SPI interface supports speeds of up to 12 Mbit/s.
- If internal clocks are not calibrated, data speeds up to 8 Mbit/s are supported.

The SPI command interface, in relation to the sensor, can be seen in Figure 2.

For more informaton on clock calibration, see section 5.7.

4.2.1 SPI Mode

The sensor is designed to act as an SPI slave interface (SPI Mode = ‘0’) with the following values:

- Clock Phase (CPHA) = '0'
- Clock Polarity (CPOL) = '0'

4.2.2 Readout Speed

Through the communication interface, pixel data from the sensor circuit is entered into a FIFO, which in turn is read by applying read instructions. The maximum readout speed in serial mode is 1.5 Mpixel/s, which is the equivalent of 90 frames/s.

4.3 Power-on Reset

The FPC1140 sensor requires a reset signal after power-up in order to reach a defined state. This occurs when the external signal, RST_N, is connected to the host, and released by the system after the sensor power-up. Alternatively, an external capacitor, C, may be added and connected to ground, when used in conjunction with an internal pull-up resistance, R, as indicated in Figure 3.

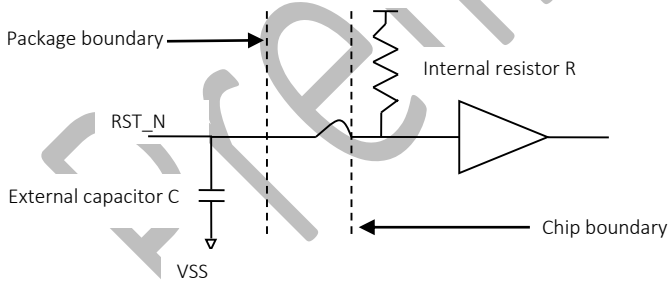

Figure 3: Power-on reset

The reset state (RST_N low) is maintained after VDD is turned on by delaying the the rise of the RST_N signal. Internal resistance depends on IO voltage and process variation.

4.4 External Finger Drive Voltage

The finger drive circuitry makes it possible to increase the internal voltage signal from 1.8V to a maximum of 3.3V. This functionality requires an external decoupling on VDDTX. It is recommended to supply this pin with and external power source of 3.3V.

For details on how to configure TXOUT and VDDTX, see section 7.3.1.

4.4.1 External Decoupling

The external finger drive supply block requires an external decoupling on VDDTX. It is also possible to supply this pin with external power (1.8V - 3.3V) instead of using the internally generated power.

It is recommended to supply this pin (VDDTX) with an external power source of either 3.3V, or 1.8V.

4.5 Finger Detection

Finger detection functionality includes the following areas:

- enhanced image capture
- optimally reduced power consumption
- response time and performance

Reduced size sub-area sets are captured to detect if and where a finger is placed on the sensor, without doing a full image capture. This decreases capture response time and improves performance. The sensor uses 12 pre-defined sub-areas of 8x8 pixels each. These sub-areas are arranged in four evenly distributed rows. Each of the four rows has three sub-areas, which are evenly distributed, horizontally.

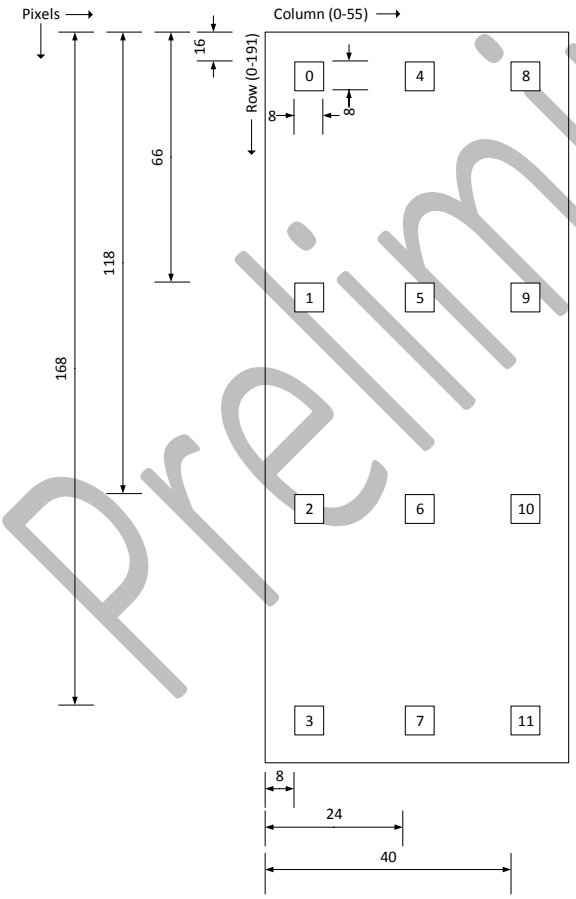

Figure 4: Finger detection sub-area distribution

The illustration in Figure 4 represents the sub-area distribution for finger detection.

4.6 System Clock

The system clock (clkSys) generates a recommended nominal frequency of 8 MHz. The frequency is configurable to approximately ± 15% of the default frequency. The clock frequency is guaranteed to be within the range of 6.25 MHz ≤ fclkSys ≤ 10 MHz without calibration.

For more information on clock calibration, see section 5.7.

4.7 Low Frequency Oscillator

The low frequency oscillator (OscLo) is always active and operates at a nominal frequency of 16 kHz in order to support Sleep Mode and Deep Sleep Mode. The frequency can be lowered to a nominal frequency of 8 kHz in order to further reduce power consumption during Sleep Mode.

Without calibration the clock frequency os guaranteed to be within the range of 8 kHz ≤ fOscLo ≤ 19 kHz.

For more information on clock calibration, see section 5.7.

4.7.1 Sleep Mode

In sleep mode, the system is not clocked. The system is awoken and clocked at regular intervals controlled by the low frequency oscillator.

4.7.2 Deep Sleep Mode

In deep sleep mode the system is not clocked at all and only the low frequency oscillator is running.

4.8 Sensor Modes

Depending on the current sensor mode, finger detection will be performed differently:

Finger Query

A single snapshot of all 12 sub-areas is taken. The status register (*fngrPresentStatus*) is updated to indicate which areas are covered by a finger at that moment.

See section 5.4 for more information on the *fngrPresentStatus* register.

Wait for Finger

The Finger Query procedure is repeated until at least one sub-area is covered in one of the snapshots and no new covered areas are registered in the next snapshot. The *fngrPresentStatus* register is updated to indicate which areas are covered by a finger at that moment, and an interrupt is set.

The idle period between repeated queries is configurable. For more information on the *fngrPresentStatus* register, see section 5.4.

Sleep

The sensor wakes up at cyclic intervals, performing reduced measurement that only checks if areas 5 and 6 are covered. If a finger is detected on the sensor, the system will wake up and an interrupt is set. The idle period between wake-ups is configurable.

For more information on sleep mode, see section 5.5.

4.9 Command / Address bytes

The FPC1140 sensor has an interpreter that processes host commands and writes to registers. Such operations typically consist of one command byte and one or more value bytes. Some basic commands only require a command byte, and some readout operations require a dummy value byte before the actual data is presented.

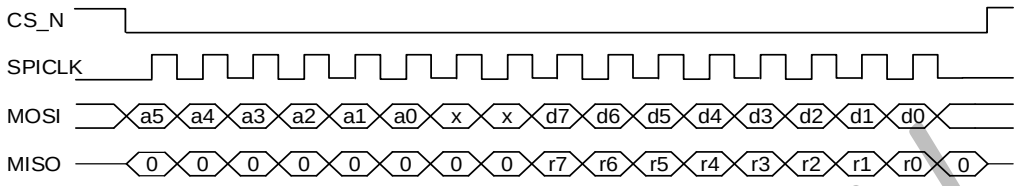

Figure 5: Principal SPI interface command/address with a command byte and one data byte.

The negative edge of CS_N indicates the start of a command or access to the register. Any command or register access must start with CS_N low and staying low throughout the command and data sequence.

For more information on supported commands, see section 6.2.

4.9.1 SPI Slave

The FPC1140 sensor is an SPI slave. The host must provide a SPICLK in order to read data. To keep the sensor active and transmitting data, the host must send dummy data on MOSI while reading data.

4.9.2 Configuration Register

A configuration register can be both read and write. Reading a configuration register alters values in the sensor and requires that suitable data be written back. Configuration register changes are not allowed while the sensor is active.

4.10 System Interrupts signals

The following interrupt signals are produced by the sensor in different scenarios:

4.10.1 Reset Interrupt

A reset interrupt signal is produced at reset release, for both soft reset and power-up.

The interrupt register is set to 0xFF.

4.10.2 Error Interrupt

When an error is detected an error interrupt signal is produced. The error status register contains information on the type of error that occurred.

4.10.3 Image Data Ready

The image data ready signal indicates that the image capture data is ready to be read in the SPI buffer.

4.10.4 Finger Down

When a finger is detected, a *finger down* signal is sent. The Finger Status register contains more data.

4.10.5 Command Done

When a command is completed or aborted, a *command done* signal is produced.

For more information on the interupt register, see section 7.2.1.

5 Use Case Scenarios

This chapter describes typical use case scenarios for a complete system, comprising a host and a sensor. All operations are available after sensor reset or power-up. The sensor can be configured to to ensure optimal performance.

For a more detailed description on how to configure the sensor, see chapter 7.

5.1 Write to Setup Register

Before initiating a sensor command, the sensor must first be configured by writing to setup registers. When accessing a multi-byte register, byte n is transmitted first and byte 0 last. Configuration changes should not be made during the execution of a command sequence.

A typical command sequence is shown in Figure 6.

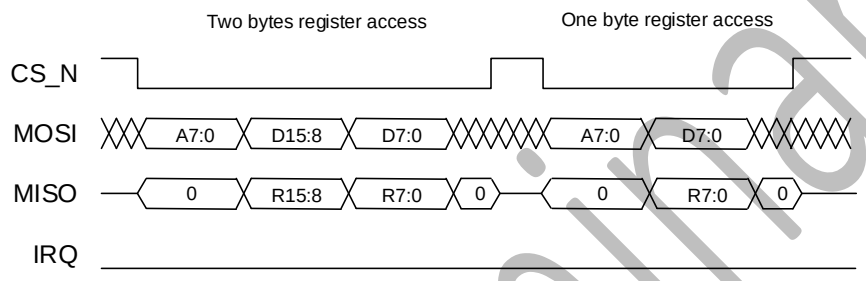

Figure 6: Principal SPI sequence for writing to a setup register

5.2 Image Capture

Image capture is the main functionality for the sensor. When captured image data is ready to be read, an interrupt is set. A typical image capture command sequence is outlined in Figure 7.

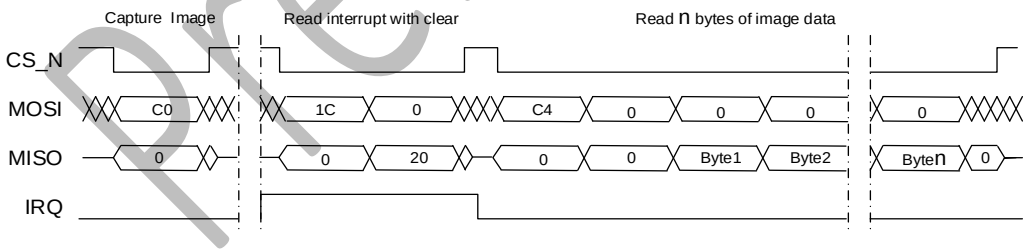

Figure 7: Principal SPI sequence for Image Capture

The *Read Image Data* command consists of the command byte, a dummy byte and the 56 * 192 = 10752 bytes of image data. The command may be interrupted at any time between data bytes. It is not a requirement that all data bytes must be read in one sequence.

Note that byte 0 is transmitted first, i.e. the opposite of a multi-byte register access. This command may be cancelled at any time by sending an ACTIVATE_IDLE_MODE command.

A number of registers affect the captured image and must be configured in advance. See chapter 7 for more information on how to configure registers.

5.3 Finger Present Query

A finger present query is used to determine if a finger is present on the sensor. Captured pixel values are divided by 8 before being compared to the adjustable threshold value that is set in the register. See chapter 7 for more information on register configuration.

When the sensor is covered by a finger, the status register indicates which of the twelve sub-areas have surpassed the threshold value. A typical finger present query command sequence is outlined in Figure 8.

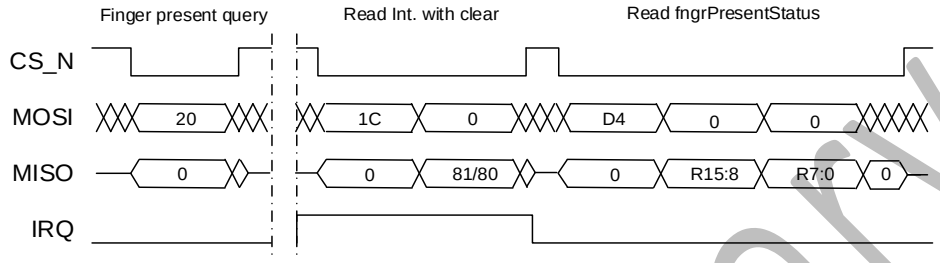

Figure 8: Principal SPI sequence for Finger Present Query

5.4 Wait for Finger

During the wait for finger command sequence, the sensor monitors changes to sensor coverage and determines the best instance to perform a full image capture. A typical wait for finger command sequence is outlined in Figure 9.

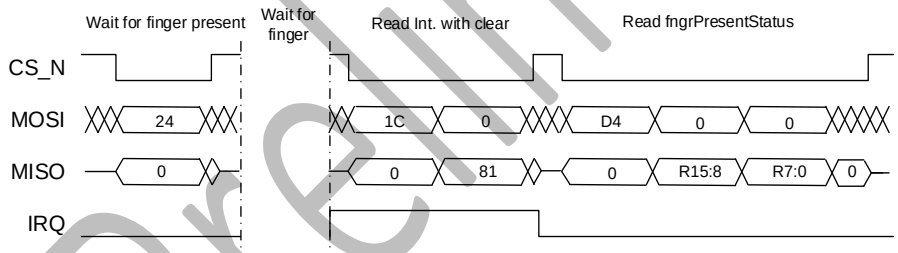

Figure 9: Principal SPI sequence for Wait for finger

The Wait for Finger command sequence may be cancelled at any time by sending an ACTIVATE_IDLE_MODE command. When returning to idle mode, an interrupt is set.

The sensor performs a finger present query at a fixed interval until a finger is placed on the sensor. See section 5.4.1 for more information on the time interval between queries.

5.4.1 Waiting Time Between Queries

The *fngrDetCntr* register determines the waiting time between repeated finger queries, as indicated in Figure 10. The adjustable range for the time is between 0 and 2 ms, approximately.

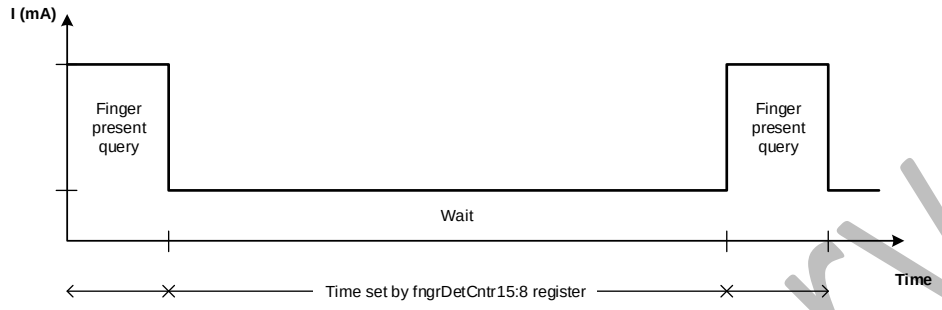

Figure 10: The fngrDetCntr register sets waiting time between finger present queries

Less current is used during the waiting (idle) time between finger present queries. See section 3.1.2 for more information on current consumption.

5.5 Sleep Mode

Sleep mode is an essential element of the FPC1140 sensor for efficient system power usage. Sleep mode keeps the sensor in a low-power mode, periodically waking up to perform reduced finger present queries. If a finger is detected on the sensor, the sensor is brought out of sleep mode and into idle mode. When returning to idle mode, an interrupt is set.

Sleep mode may be cancelled by the host at any time by sending the ACTIVATE_IDLE_MODE command. When returning to idle mode, an interrupt is set. After sending the ACTIVATE_IDLE_MODE command, the host must wait until it receives the interrupt before issuing a new command sequence. Otherwise the ACTIVATE_IDLE_MODE command may be cancelled and the sensor remains in sleep mode.

A typical sleep mode command sequence is outlined in Figure 11.

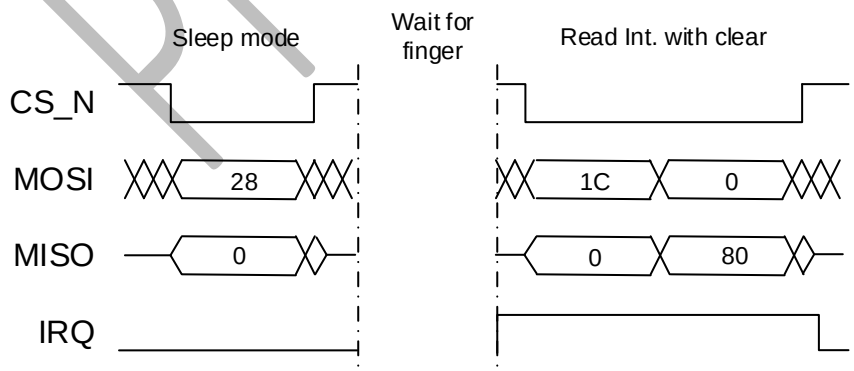

Figure 11: Principal SPI sequence for Sleep mode

5.5.1 Reduced Finger Queries

When the sensor is in sleep mode it draws less current than when performing a finger present query. Approximately 1.3 µA of current is consumed when the sensor is in sleep mode. Current drawn when performing a finger present query is approximately 6.2 mA.

The *SleepCntr* register determines the time between reduced finger queries in sleep mode, as illustrated in Figure 12.

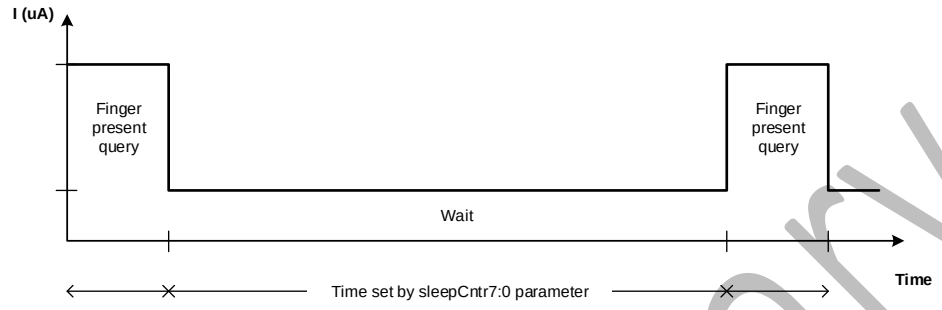

Figure 12: Time between finger present queries in sleep mode.

Values of between 0-255 for the time between iterations of the finger present query corresponds to approximately 0-2000 milliseconds. The precise value depends on the following:

- SleepCntr register settings
- Oscillator calibration
- Oscillator trimming to 8 or 16 kHz

The nominal value for 8 kHz is approximately 2s, and the corresponding value for 16 kHz is approximately 1s. These settings offer a compromise between power consumption and reaction time when a finger is placed on the sensor.

5.6 Deep Sleep Mode

Deep sleep mode is a vital aspect of efficient system power usage and can be used when a finger is not expected. Deep sleep mode is similar to sleep mode in that it keeps the sensor in a low power consumption mode, except that no finger detection is activated.

A typical deep sleep mode command sequence is outlined in Figure 13.

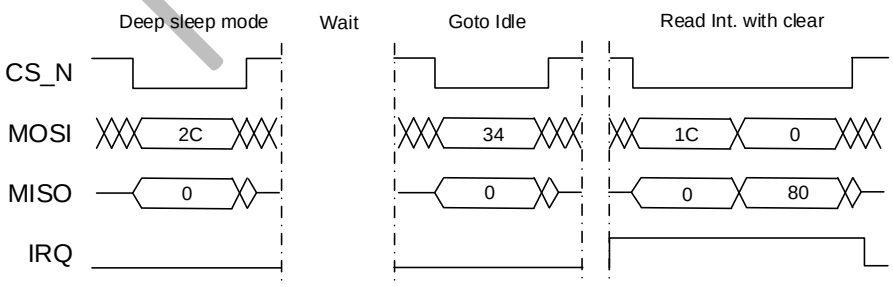

Figure 13: Principal SPI sequence for Deep sleep mode

Deep sleep mode can be exited by sending an ACTIVATE_IDLE_MODE command which brings the sensor into idle mode. When returning to idle mode, an interrupt is set. After sending the ACTIVATE_IDLE_MODE command, the host must wait for the interrupt signal before issuing a new command sequence. The ACTIVATE_IDLE_MODE command may be cancelled at any time in the sequence and the sensor will remain in deep sleep mode.

5.7 Oscillator Calibration

An internal system clock presents process variations between individual sensor chips. The oscillator should be calibrated for optimal SPI performance. Oscillator calibration can be performed if an application requires precise cycle times, such as the time between finger present queries during sleep mode.

A typical oscillator (clock) calibration mode command sequence is illustrated in Figure 14.

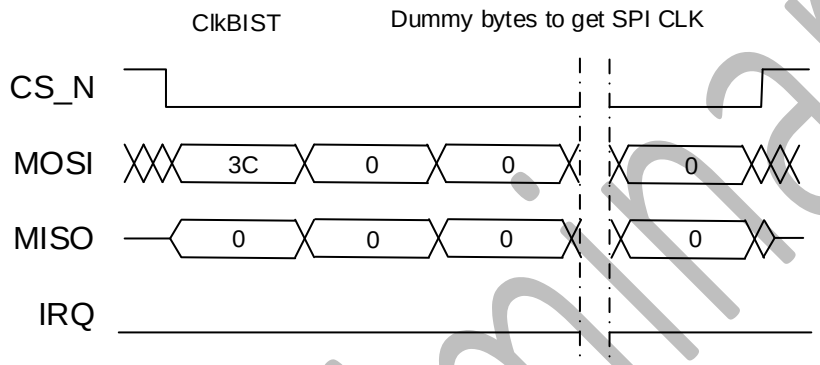

Figure 14: Principal SPI sequence for clock calibration

The lowest clock oscillation, clkOscLo, is 16kHz, and is used as reference for two other clocks. A test is performed by sending the ClkBist command, followed by a number of SPICLK cycles with a known frequency.

A counter measures the number of SPICLK cycles that appear between the two rising edges of clkOscLo. Another counter will measure the number of clkSys cycles that appear between two rising edges of clkOscLo.

The results are saved in the ClkBistResult register and can be read with an SPI sequence as outlined in Figure 15.

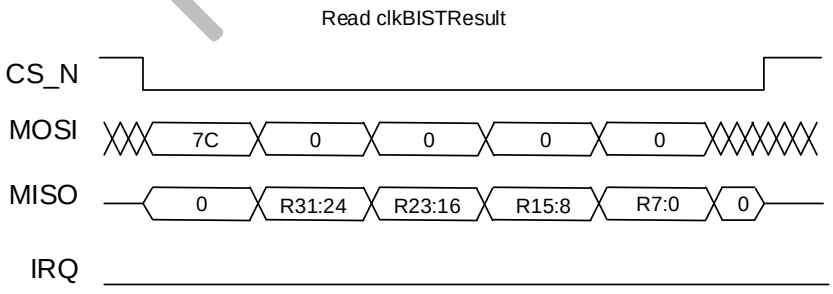

Figure 15: Principal SPI sequence for reading clock calibration result

5.7.1 Calculating Clock Frequencies

The following registers contain data which can be used to calculate clock frequencies:

- SPI register - contains SPI_{count} data
- clkSys register – contains $OscHi_{count}$ data

The clock frequencies can be calculated as follows:

Lowest oscillating frequency
$clkOscLo_{freq} = SPI_{freq} / SPI_{count}$

System clock
$clkSys_{freq} = OscLo_{freq} * OscHi_{coun}$

5.8 Soft reset

Soft reset is used to reinitialise the sensor to its default state. All writeable registers are reset to the default value (rstN Value). The soft reset SPI sequence is outlined in Figure 16.

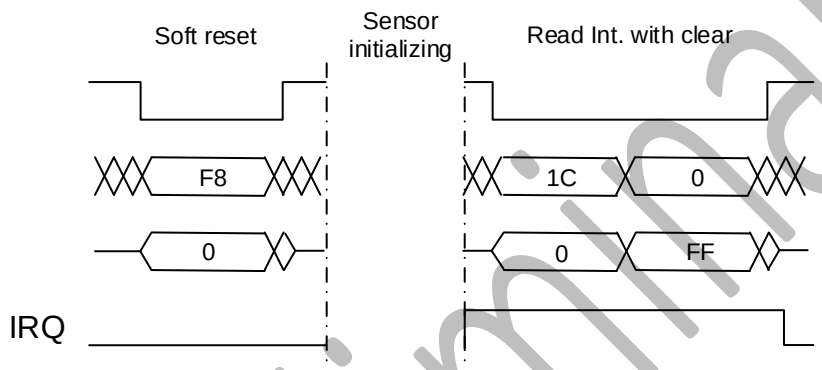

Figure 16: Principal SPI sequence for soft reset

6 Address Mapping

This chapter describes the address mapping for commands and registers which can be used to calibrate and operate the FPC1140 sensor. For more information on registers, see chapter 7.

6.1 Command and Register Overview

This section gives an overview of the corresponding address mapping for available commands and registers. See Table 12 for more information.

Command / Register	Type	Code / Address	
		Hex	Dec
-	-	14	20
Read interrupt with no clear	Command	18	24
Read interrupt with clear	Command	1C	28
Finger present query	Command	20	32
Wait for finger present	Command	24	36
Activate sleep mode	Command	28	40
Activate deep sleep mode	Command	2C	44
Activate idle mode	Command	34	52
fpcError	Register	38	56
ClkBIST	Command	3C	60
-	-	40	64
-	-	44	68
-	-	4C	76
-	-	50	80
imgCapSize	Register	54	84
-	-	5C	92
-	-	60	96
-	-	68	104
-	-	6C	108
tstColPattern	Register	78	120
clkBISTResult	Register	7C	124
-	-	84	132
-	-	88	136
FingerDriveConf	Register	8C	140
-	-	90	144
oscTrim	Register	94	148
-	-	98	152
-	-	9C	156
ADCShiftGain	Register	A0	160
-	-	A4	164

Command / Register Address	Type	Code / Address	
		Hex	Dec
-	-	A8	168
Capture image	Command	C0	192
Read image data	Command	C4	196
-	-	D0	208
fngrPresentStatus	Register	D4	212
fngrDetThresh	Register	D8	216
fngrDetCntr	Register	DC	220
Soft reset	Command	F8	248
hwID	Register	FC	252

Table 12: Command and register address mapping

6.2 Commands

Available commands and corresponding address mapping are described in Table 13.

Command	Code / Address			Description
	Hex	Dec	Bin	
Capture image	C0	192	11000000	Capture new image. One byte access. Only the command is transmitted.
Read image data	C4	196	11000100	Valid data is first received following a command with a dummy byte. The read continues until csN is set to low. It is possible to split the reading of an image into several requests. In this case, new commands (all but the first) should be issued without the dummy byte.
Read interrupt with no clear	18	24	00011000	Read interrupt register. The register is not cleared. Two byte access, command and interrupt data.
Read interrupt with clear	1C	28	00011100	Read the interrupt register and clear it. The IRQ signal is set to low. Two byte access, command and interrupt data.
Finger present query	20	32	00100000	Checks if a finger is present. One byte access, only the command is transmitted.
Wait for finger present	24	36	00100100	Continue to check for a finger until a finger is present. One byte access, only the command is transmitted.
Activate sleep mode	28	40	00101000	Go to Sleep Mode. One byte access, only the command is transmitted.
Activate deep sleep mode	2C	44	00101100	Go to Deep Sleep Mode. One byte access, only the command is transmitted.
Activate idle mode	34	52	00110100	Go to Idle Mode. One byte access, only the command is transmitted.
Soft reset	F8	248	11111000	Performs a software controlled reset of the chip. One byte access, only the command is transmitted.
ClkBIST	3C	60	11000000	Measures the frequency of the two internal oscillators in relation to a known SPICLK frequency. The command is done with one byte access plus a number of SPICLK cycles which is decided by the frequency of the OscLo oscillator. The measurement needs to run between two rising edges of the OscLo oscillator. Sending more SPICLK pulses will not affect the measurement. The result is read in the clkBistResult register. For more information on calculating clock frequencies, see section 5.7.

Table 13: Commands

7 Registers

This chapter gives an overview of the registers used to configure the FPC1140 and their main properties.

7.1 Finger Detection

This section describes the register properties for finger detection.

7.1.1 Finger Detection Threshold

The name of the finger detection threshold register is *fngrDetThresh*. The *fngrDetThresh* register has access to two bytes: one address byte and one read byte. Current register content is read when data is written to the register. Properties for this register are shown in Table 14.

fngrDetThresh		**Register Address:** 0xD8 (216d) **Access:** Read/Write **rstN Value:** 0x50
Data Bit(s)	**Name**	**Function/Coding**
7:0	fngrDetThrshld(7:0)	Threshold value for finger detects. The threshold value is compared to the pixel sum, calculated as: $$Pixelsum = \left\lfloor \frac{1}{2} \sum_x \sum_y \left\lfloor \frac{Pixel(x,y)}{8} \right\rfloor \right\rfloor$$

Table 14: Properties for the finger detection threshold register

7.1.2 Finger Detection Queries

The name of the finger detection query control register is *fngrDetCntr*. The *fngrDetCntr* register has access to three bytes: one address byte and two read bytes. Current register content is read when data is written to the register. Properties for this register are shown in Table 15.

fngrDetCntr		**Register Address:** 0xDC (220d) **Access:** Read/Write **rstN Value:** 0x00FF
Data Bit(s)	**Name**	**Function/Coding**
Byte 1:		
15:8	WaitFngrDetCntr(7:0)	The time between finger detect queries in wait for finger query mode. The wait time is calculated as: $$time = \frac{255 \cdot WaitFngrDetCntr}{f_{clkSys}}$$ Where f_{clkSys} is 10 MHz.
Byte 0:		
7:0	SleepFngrDetCntr(7:0)	The time between finger detect queries in sleep mode. The sleep time is calculated as: $$time = \frac{64 \cdot SleepFngrDetCntr}{f_{oscLo}}$$ Where f_{oscLo} is specified by the oscTrim register.

Table 15: Properties for the finger detection query register

7.2 Setup and Status Registers

This section describes the properties for registers used for setup and status.

7.2.1 Interrupts

The name of the interrupt register is *fpcInterrupts*. The *fpcInterrupts* register has access to two bytes: one address byte and one read byte. Properties for this register are shown in Table 16.

fpcInterrupts		Register Address: 0x18 (24d) or 0x1C (28d) Access: Read/Read with clear rstN Value: 0xFF
Data Bit(s)	**Name**	**Function/Coding**
7	-	Command done.
6	-	-
5	-	New image data available in FIFO.
4	-	-
3	-	-
2	-	Error. See fpcError register in section 7.2.2.
1	-	-
0	-	Finger down.

Table 16: Properties for the interrupt register

Read with Clear

Reading *fpcInterrupts* with the address 0x1C clears the interrupt register in mainCtrl and the IRQ signal is set to low.

A read with the address 0x18 will not clear the interrupt register.

Reset Value

A reset value (rstN) of *FFh* in the interrupt register indicates that a reset has occurred.

7.2.2 Errors

The name of the error register is *fpcError*. The *fpcError* register has access to two bytes: one address byte and one read byte. Properties for this register are shown in Table 17.

fpcError		Register Address: 0x38 (56d) Access: Read with clear rstN Value: 0x00
Data Bit(s)	**Name**	**Function/Coding**
7:1	Not used	Reset value.
0	-	Fifo Underflow. Attempted to read data when image FIFO was empty.

Table 17: Properties for the error register

Read with Clear

Reading the *fpcError* register clears it to the reset value.

7.2.3 Finger Present Status

The name of the register for finger present status is *fngrPresentStatus*. The *fngrPresentStatus* register has access to three bytes: one address byte, and two data bytes. Current register content is read when data is written to the register.

Properties for this register are shown in Table 18.

fngrPresentStatus		**Register Address:** 0xD4 (212d) **Access:** Read **rstN Value:** 0x0000
Data Bit(s)	**Name**	**Function/Coding**
Byte 1-0:	-	-
15:12	Not used	Reset value
11:0	fngrPresentStatus	Each bit indicates finger presence on one sub-area, where bit 0 is sub area 0. See Figure 4 for details on sub-areas.

Table 18: Properties for the finger present status register

The register value is valid after an interrupt is issued from either the *Wait for finger present* command, the *Finger present query* command, or on waking up from Sleep mode.

7.2.4 Oscillator Frequency Calculation

The name of the register used to calculate oscillator frequency is *clkBISTResult*. The *clkBISTResult* register has access to five bytes: one address byte, and four data bytes. Current register content is read when data is written to the register.

Properties for this register are shown in Table 19.

clkBISTResult		**Register Address:** 0x7C (124d) **Access:** Read **rstN Value:** 0x00 00 00 00
Data Bit(s)	**Name**	**Function/Coding**
Byte 3:2:	-	-
31	Not used	Reset value.
30	doneSPI	A zero indicates test failed.
29:16	resultSPI (13:0)	Oscillator low test result. All ‘1’ or all ‘0’ indicates overflow or fail.
Byte 1:0	-	-
15	Not used	Reset value.
	doneOscHi/doneclkSys	A zero indicates test failed.
13:0	resultOscHi/resultclkSys (13:0)	clkSys Test result. All ‘1’ or all ‘0’ indicates overflow or fail.

Table 19: Properties for the oscillator frequency calculation register

Refer to the command *clkBist* for a description how to calculate the frequency of the oscillators from the *clkBISTResult* register.

7.2.5 Oscillator Calibration

The name of the register for oscillator calibration is *oscTrim*. The *oscTrim* register has access to three bytes: one address byte, and two data bytes. Current register content is read when data is written to the register.

Properties for this register are shown in Table 20.

oscTrim		**Register Address:** 0x94 (148d) **Access:** Read/Write **rstN Value:** 0x0D07
Data Bit(s)	**Name**	**Function/Coding**
Byte 1:	-	-
15:12	Not used	Reset or the last value written to these bits is read.
11:8	ClockSysTrim(3:0)	Oscillator high frequencies (clkSys and OscHi) trim value.
Byte 0:	-	-
7:6	Not used	Reset or the last value written to these bits is read.
5:0	OscLoTrim(5:0)	Oscillator low frequencies trim value. Bit 5 = 0 -> nominal frequency 16 KHz. Bit 5 = 1 -> nominal frequency 8 kHz.

Table 20: Properties for the oscillator calibration register

7.2.6 Shift Gain

The name of the register for shift is *ADCShiftGain*. The *ADCShiftGain* register has access to three bytes: one address byte, and two data bytes. Current register content is read when data is written to the register.

Properties for this register are shown in Table 21.

ADCShiftGain		**Register Address:** 0xA0 (160d) **Access:** Read/Write **rstN Value:** 0x0000
Data Bit(s)	**Name**	**Function/Coding**
Byte 1:	-	-
15:13	Not used	Reset or the last value written to these bits is read.
12:8	ADCShift(4:0)/ ImageShift	ADC/*Image* shift value.
Byte 0:	-	-
7:4	Not used	Reset or the last value written to these bits is read.
3:0	ADCGain(3:0)/ImageGain	ADC/*Image* Gain trim value.

Table 21: Properties for the shift gain register

7.2.7 Image Capture Size

The name of the register for image capture size is *imgCaptSize*. The *imgCaptSize* register has access to five bytes: one address byte, and four data bytes. The current register content is read when data is written to the register.

Properties for this register are shown in Table 22.

imgCaptSize		**Register Address:** 0x54 (84d) **Access:** Read/Write **rstN Value:** 0x00C000C0
Data Bit(s)	**Name**	**Function/Coding**
Byte 3:	-	-
31:24	StartRow(7:0)	Image start row position. Valid range 0 to 192
Byte 2:	-	-
23:16	RowLength(7:0)	Image row length. Valid range 0 to 56
Byte 1:	-	-
15:8	StartCol (7:0)	Image start group position. Valid value is multiple of 8 in the range 0 to 48.
Byte 0:	-	-
7:0	ColLength(7:0)	Image group length. Valid value is a multiple of 8 in the range 8 to 192.

Table 22: Properties for the imgCaptSize register

If the total requested amount of data is less than 8 pixels, there will not be a data present interrupt when data is ready to be read. In the case of very small amount of data, it is recommended to wait for the sensor to scan the requested pixels.

7.2.8 Hardware ID

The name of the register for hardware ID is *hwID.* The *hwID* register has access to three bytes: one address byte, and two read bytes.

Properties for this register are shown in Table 23.

hwID		**Register Address:** 0xFC (252d) **Access:** Read **rstN Value:** 0x140A
Data Bit(s)	**Name**	**Function | Coding**
15:4	hwIDChip(11:0)	Chip version | 140 = Chip 1140
3:0	hwIDRev(3:0)	Revision number | A = Revision A

Table 23: Properties for the HardwareID register

7.3 Configuration

This section describes the properties for registers used to configure the sensor.

7.3.1 Finger Drive

The name of the register for configuring the finger drive is *fngrDriveConf*. The *fngrDriveConf* register has access to two bytes: one address byte and one data byte. Current register content is read when data is written to the register.

Properties for this register are shown in Table 24.

fngrDriveConf		**Register Address:**	**0x8C (140d)**
		Access:	**Read/Write**
		rstN Value:	**0x02**
Data Bit(s)	**Name**	**Function/Coding**	
7:6	Not used	Reset or the last value written to these is read.	
5	FngrDrvVdBstEn	Enable voltage increase for TXOUT supply. This signal must be configured together with *FngrDrvVdIntEn*. '0' – VDDA supply TXOUT. Also decreases the voltage level. '1' – Voltage level increase enabled and supply TXOUT.	
4	FngrDrvVdIntEn	Enable internal voltage supply to TXOUT. '0' – VDDTX supplies TXOUT. '1' – Internal resource controlled by the *FngrDrvVdBstEn* signal supply TXOUT.	
3	FngrDrvExtInv	Inverting TXOUT	
2	FngrDrvTst	Finger drive test control. '0' – Finger drive disconnected from pixel test capacitor. '1' – Finger drive connected to pixel test capacitor according to the *tstColPatternEn* register.	
1	FngrDrvExt	Finger drive external control. '0' – Finger drive disconnected from TXOUT pin. '1' – Finger drive connected to TXOUT pin.	
0	Not used	Reset or the last value written to these bits is read	

Table 24: Properties for the finger drive configuration register

7.3.2 Test Pattern

The *tstColPatternEn* register is used to configure test patterns by enabling capacitors. The *tstColPatternEn* register has access to three bytes: one address byte and two data bytes. Current register content is read when data is written to the register.

Properties for this register are shown in Table 25.

tstColPatternEn		**Register Address:**	**0x8C (140d)**
		Access:	**Read/Write**
		rstN Value:	**0x02**
Data Bit(s)	**Name**	**Function/Coding**	
Byte 1:	-	-	
15:8	TstColPaEn1(7:0)	Test pattern 1 enables the register. Each bit enables one test capacitor. The pattern controls pixels on row 0, column 8-15, 24-31 and so on.	
Byte 0:	-	-	
7:0	TstColPaEn0 (7:0)	Test pattern 0 enables the register. Each bit enables one test capacitor. The pattern controls pixels on row 0, column 0-7, 16-23 and so on.	

Table 25: Properties for the test pattern register

8 Timing

This chapter offers an overview of some aspects of timing for the FPC1140 sensor.

8.1 Power-up Timing

The power-up timing sequence for the sensor is shown in Figure 17.

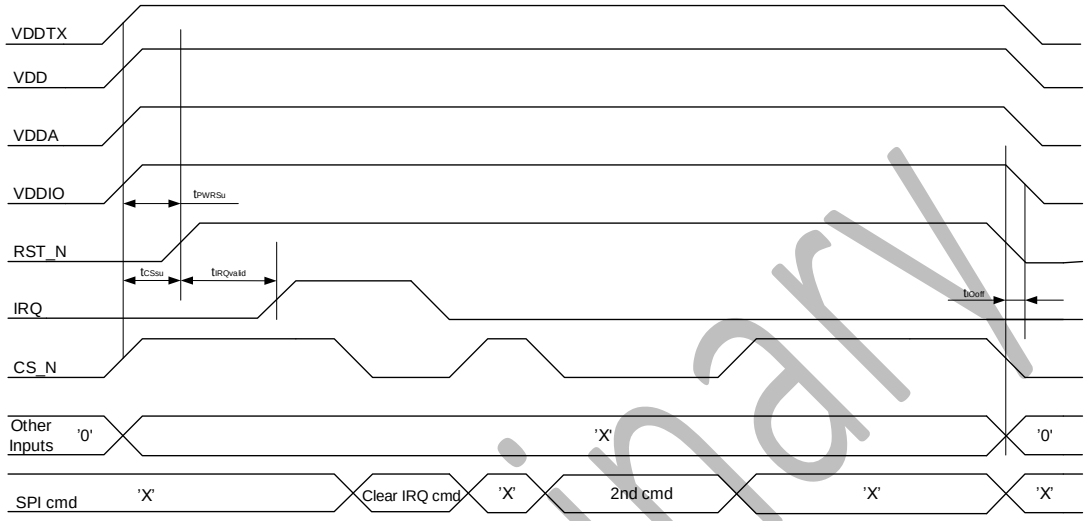

Figure 17: Power-up timing sequence

8.1.1 Voltage Difference

The maximum allowed voltage difference between VDD and VDDA is 200 mV. VDDIO may be supplied with a larger voltage than VDD and VDDA.

- |VDD – VDDA| < 200 mV
- VDDIO + 200 mV > VDD
- VDDIO + 200 mV > VDDA
- VDDTX + 200 mV > VDD
- VDDTX + 200 mV > VDDA

8.1.2 RST_N

RST_N is an input signal controlled by the host. The host may release the signal (set RST_N to high) no earlier than 100 µs after the power supplies have stabilised.

- tPWRsu = 0.1 ms

8.1.3 CS_N

CS_N should be set high before releasing RST_N.

- tCSsu > 0 ms.

8.1.4 IRQ

The sensor sets the IRQ signal to high to indicate that SPI communication can begin. The maximum time for IRQ after reset is deactivated is as follows:

- tIRQvalid = 1.3 ms

The IRQ signal is asynchronous to the SPICLK clock.

8.2 SPI Timing

An overview of SPI timing for the sensor interface is shown in Figure 18.

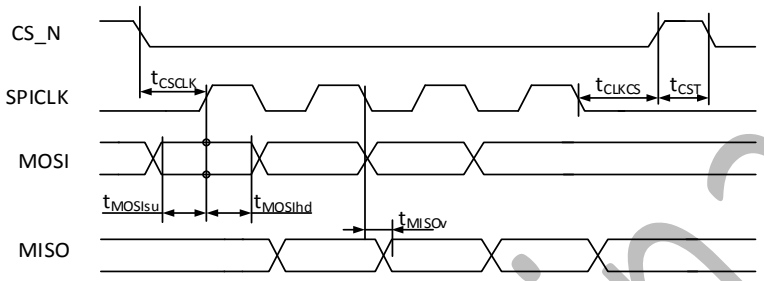

Figure 18: SPI timing

Minimum and maximum values for the parameters in the SPI timing sequence in are shown in Table 26.

Symbol	Parameter	Minimum	Maximum	Units
t_{MISOv}	MISO valid time	-	29	ns
t_{MOSIsu}	MOSI setup time	13	-	ns
t_{MOSIhd}	MOSI hold time	0	-	ns
	SPICLK Frequency	1	12	MHz
t_{CSCLK}	Time for CS_N low to SPICLK high	31.25	-	ns
t_{CLKSPI}	Time for SPICLK low to CS_N high	0	-	ns
t_{CST}	Minimum CS_N high time before setting CS_N low.	31.25	-	ns

Table 26: SPI timing for sensor interface

9 Reference Schematic

An overview of the FPC1140 sensor interfaces is shown in the reference schematic in Figure 19.

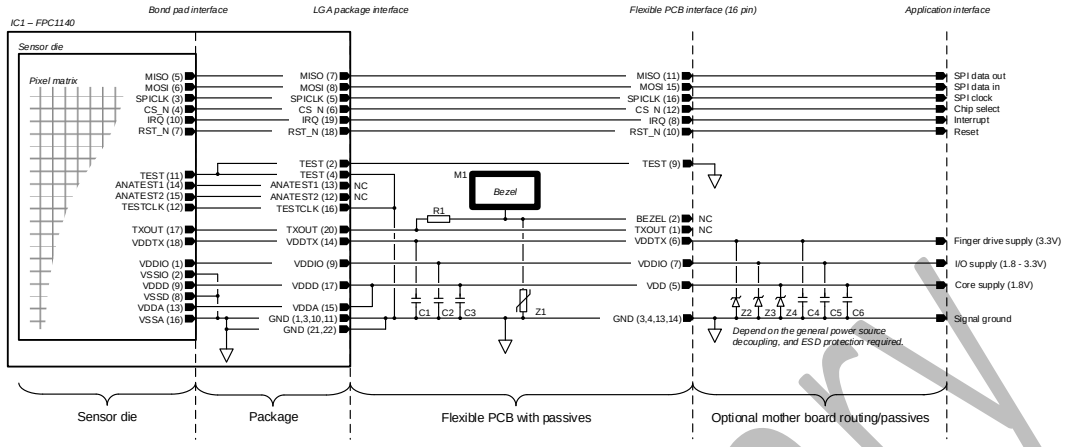

Figure 19: Reference Schematic

The reference schematic shown in Figure 19, including the external components and SMD are to be considered as examples, and as such are not guaranteed to be the best implementation for all applications.

9.1.1 Bill of Materials – Module Assembly

On-board surface-mounted device (SMD) components as shown in the reference schematic in Figure 19 are listed in Table 27.

Part	Value	Description	Comment
C1, C2, C3	100 nF	Decoupling	-
R1	100 Ω	Current Limiter	Internal ESD protection
Z1	ESD206-B1-02ELS	Voltage Clamp	Internal ESD drain
M1	-	Bezel (Drive Element)	Galvanic Fingertip Connection required
IC1	FPCV1140	LGA Touch Sensor	See separate LGA specification

Table 27: BoM – Module assembly

9.1.2 Bill of Materials – Application Interface

Optional external (SMD) motherboard components for a PCB interface are shown in the reference schematic in Figure 19. These SMD are described in Table 28.

Part	Value	Description	Comment
C4, C5, C6	100 nF	Decoupling	Optional
Z2, Z3, Z4	3.3 V	-	Optional ESD Protection

Table 28: BoM – Application interface

10 ESD Protection

To generate an image, capacitive fingerprint sensors require a finger to be in contact with the sensor surface. This will expose all capacitive sensors to severe electro-static discharges (ESDs), as they usually are the "first point of contact". ESD discharge voltages are often under-estimated and the actual voltage levels may be surprisingly high. Discharges in the 1 to 2 kV range will typically not even be noticed – they wil not be felt in the finger of the user.

All sensors from Fingerprint Cards incorporate extensive internal ESD protection for all accessible front surfaces. The protection level is well in excess of 30 kV using a standard Human Body Model discharge in a production environment.

10.1 Human Body Model

The Human Body Model, as shown in Figure 20, consists of a 100 pF capacitor, which simulates the capacitance between body and ground. This capacitor is charged to a test voltage. The resistance of the finger and skin is approximated by a 1500 Ω series resistor. The discharge will have a time constant of, 100 pF x 1500 Ω = 150 nS. For a 15 kV discharge the peak current would be 15 kV/1500 = 10 A.

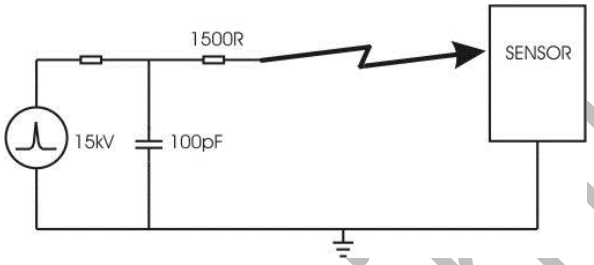

Figure 20: Human Body Model

Although the ESD-specification is given as a voltage level it is important to realize that an ESD test is effectively a current discharge test.

10.2 Internal Sensor Protection

Sensors from Fingerprint Cards have a robust sensor surface coating, which will deflect discharges to the surounding bezel. From the bezel, the discharge current will be conducted via the Transient Voltage Suppressor (TVS) to the local ESD drain node. The voltage at the bezel is thereby limited. The 100 Ω resistor will limit the current towards the sensor chip to very safe levels.

10.3 Voltages Induced by ESD current

In a simplified model, two currents occur during an ESD event - the main ESD current flowing through the TVS to the sensor ESD drain, and the much smaller current flowing through the 100 Ω resistor back into sensor chip input protection throught the TXOUT signal.

The current flow through the 100 Ω resistor will depend on the clamping voltage over the TVS. A 15 kV discharge will generate a 200 mA current pulse into the chip protection diodes, well within the chip ESD rating. The duration of the pulse will be in the order of 600 ns. After this time the current will decay exponentially. The charge through the protection diode can be estimated to 0.15 nC.

10.3.1 Sensor Cable Extensions

When the FPC1140 sensor is connnected using longer sensor cable lengths of over 0.2 m, the electromagnetic coupling between the current in the ESD drain connection and other signal and supply connections need to be considered. This coupling is rather complicated and will depend on the cable geometry.

With a standard, short connection between the sensor and the receiving electronics, these effects are not significant and can be ignored.

Longer cable lengths between sensor and the receiving electronics can in some cases be acceptable. Exact guidelines are not possible since the ESD effects will depend on the actual installation, but lengths of up to 0.2 m should, in general not cause any problems.

Extending the standard cable length will also affect signal integrity. The digital waveforms should be checked for adverse reflections. Problems with unwanted oscillation (ringing) become more evident as the length increases. At 1 m the ringing will cause waveforms that are questionable.

10.3.2 Minimizing Effects on Downstream Electronics

The ESD pulse will continue past the sensor drain path and spread into the receiving electronics ground plane and most likely further on to a "protective earth" ground via a connecting cable. This connection will often have considerable length and may potential lead to ESD problems.

To help alleviate the risk of electromagnetic coupling a separate ESD return to divert the ESD current to a more suitable point is recommended.

A way to prevent problems with stray currents due to dual ground paths, is to front the separate ESD return with a TVS in order to break this current path at low voltages while allowing the ESD pulse to pass freely.

Higher ESD diversion can be achieved by also increasing the inductance of the signal cable connection from the receiving electronics. The common mode of inductance can to help steer the ESD current over to the separate ESD return. One of the simplest methods is to mount an EMI ferrite core on the cable near the electronics.

10.4 ESD Discharge Path

It is recommended that the separate ESD discharge path is connected directly to the signal ground plane, as illustrated in Figure 21.

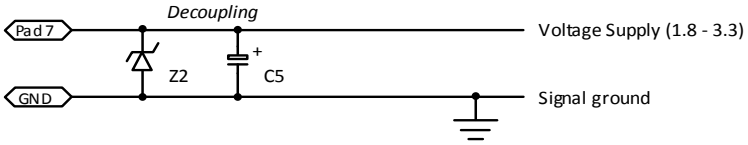

Figure 21: ESD discharge - signal ground

This solution requires the ground plane and the receiving electronics to consume the entire discharge induced by the end user. The ground plane connection should preferably be done close to a large decoupling capacitor.

11 Power Supply & Filtering

Depending on the overall quality of the connected power supply, i.e. noise, filter, or decoupling circuitries may be necessary. In normal cases a standard buffer capacitor in the range of 5-10 µF is enough. In case of a noisy environment, other types of filtering may be required to obtain optimal performance.

Although the sensor is specified for a voltage supply range between 1.8 - 3.3 V, different protection and decoupling circuitries may be necessary to reach full communication speed over the entire voltage range.

11.1 Ground Reference

A sensor in a fingerprint based authentication system will, by definition, always come in physical contact with the end user. In order to mitigate the common-mode disturbances, such as those induced by the end user, the sensor or the receiving electronics should be connected to a protective ground reference. For example, common mode disturbance may occur with isolated low cost switch-mode power supplies that do not have a direct connection or an EMI capacitor from the AC line input to the DC output.

12 Product Updates

An historical overview of the updates to the FPC1140 sensor can be found in this section.

12.1 Product History

An overview of the previous versions of the FPC1140 sensor product is shown in Table 29.

Article numbers	Description
FPC1140-0B-CW01	ES1 release of FPC1140W sensor. The FPC1140A ASIC is used in these products.

Table 29: Product History