



Analyzing the Applications of Transistors: Design, Simulation, and Implementation

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Abstract

Transistors are the fundamental components of any modern electronic device. Composed of a semiconductor material that controls the current flow within the circuit, the transistor revolutionized electronics by allowing for a much smaller-scale implementation of circuits. The two main types of transistors are Bipolar Junction Transistors (BJTs) and Field-Effect Transistors (FETs). The main function of both transistors is to either act as a switch that can turn a circuit ON or OFF, or amplify a weak electrical signal. Operational amplifiers, or op-amps, are integrated circuits made up of transistors and designed to amplify voltage signals. This report uncovers a direct design approach to designing a bipolar transistor audio amplifier, generating a square and triangle signal using op-amps, and implementing logic gates using the CMOS transistor, a combination of PMOS and NMOS transistors. The design process includes theoretical analysis, circuit modeling, and simulation using MULTISIM software attempting to mimic practical implementation. We compare and contrast the theoretical designs with the practical simulation outcomes, examining signal fidelity, noise levels, and efficiency. Lastly, we conclude the report by highlighting the importance of simulation in predicting real-world performance and guiding effective circuit design.

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Introduction

In the realm of digital electronics, the utilization of Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) is pivotal for constructing logic gates that form the backbone of modern computing. This paper dives deep into the fundamental design principles of MOSFET-based logic gates to specifically design the AND and OR gates. We explore the intricate construction of the gates using a combination of n-type and p-type MOSFETs, examining their behavior practically using MULTISIM simulation. We also justify that they correctly work by connecting measuring the output voltage of each design. The study provides insights into the practical considerations for optimizing gate performance. Furthermore, we attempt to design a BJT amplifier using a generalized design that consists of three stages: the input buffer stage, the gain stage and the output stage. We actually perform the mathematical calculations using simple circuit analysis tools like Kirchhoff's laws for voltage and current. In addition to mathematical calculation, we were asked to justify our results by applying the circuits of each stage onto the MULTISIM simulation tool. Upon justification we ensured our results were correct with minimal error. After the BJT section we delve into square and triangular wave generation using op-amps.

The application of MOSFET logic gates are endless. They are widely used in digital circuits and computer, smartphones, and other smart devices, enabling them to perform complex computation tasks. Additionally, the BJT amplifier, with its three-stage design, serves as a critical component in audio systems, enhancing signal strength for clear sound reproduction by ensuring a reduced loss of data when the signal is amplified. This project was very interesting and enhanced our perspective on MOSFETs and BJTs.

BJT Amplifier applications: Audio Amplifier

In this section, our aim is to design a bipolar transistor audio amplifier that fulfills specific requirements, namely, delivering an average power of 0.1W to an $8\text{k}\Omega$ speaker from a microphone generating a 10mV peak sinusoidal signal with a source resistance of $10\text{k}\Omega$. To achieve this, we employ a generalized multistage amplifier configuration as depicted in Figure 1. This setup comprises three main stages: an input buffer stage, serving as an emitter-follower circuit (common collector amplifier), aimed at mitigating the loading effect of the $10\text{k}\Omega$ source resistance; an output stage, also employing an emitter-follower circuit to furnish the requisite output current and signal power; and a gain stage, featuring a two-stage common emitter amplifier to provide the necessary voltage gain. This design operates under the assumption of a 12-volt power supply bias for the amplifier system. It is important to note that biasing is the process of setting a starting point for the behavior of the circuit. In this case the amplifier is tuned to work with a power supply that provides a constant voltage of 12 volts. This ensures that the amplifier has enough power to operate and that the circuits electronic components such as transistors work correctly.

It is also important to note that the three stages in the BJT amplifier application design serve distinct purposes:

- **Input Buffer Stage:** This stage ensures efficient signal transfer from a high impedance source to the next stage without signal quality loss. It acts as an impedance matching component to prevent loading effects.
- **Gain Stage:** The central amplification stage where the weak input signal is strengthened. This stage is responsible for the majority of the signal amplification in the amplifier circuit.

- **Output Stage:** This final stage matches the impedance of the load for maximum power transfer and provides further amplification. It outputs the necessary output current and output signal power.

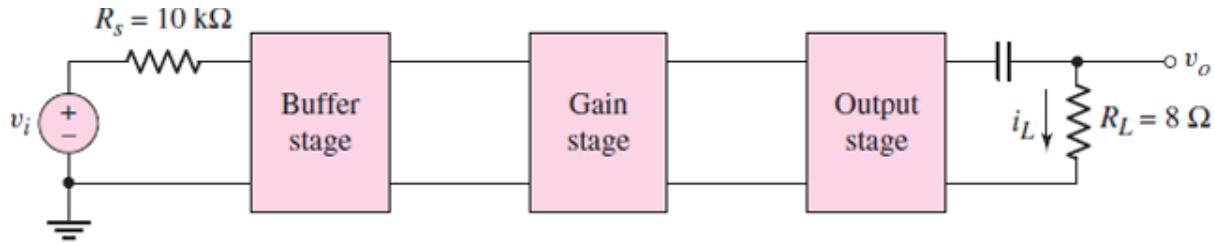


Figure 1. Generalized multistage amplifier design

Theoretical Calculations

To determine the voltage gain of the circuit, we undertake a two-step analysis which utilizes both DC and AC (small signal) analyses. Initially, we establish the DC operating point of the circuit to determine crucial parameters such as bias currents (I_B), collector currents (I_C), and collector voltages (V_C). Subsequently, we delve into small signal analysis, focusing on parameters like transconductance (g_m) and intrinsic resistance (r_π), which are essential for understanding the circuit's behavior under varying input signal conditions. The transconductance (g_m) measures a transistor's ability to convert variations in input voltage into changes in output current. Intrinsic resistance (r_π) on the other hand, characterizes the base-emitter resistance seen from the input side of the transistor and is crucial in small-signal analysis for calculating voltage gain. This comprehensive approach allows us to precisely quantify the voltage gain while considering both DC and AC characteristics of the circuit.

Input Buffer Stage:

The input buffer stage, depicted in Figure 2, utilizes an emitter-follower amplifier configuration. In this configuration, the emitter is directly connected to the output load, while the input signal is applied to the base of the BJT. While the voltage gain of an emitter follower does not significantly amplify the voltage of the input signal, it

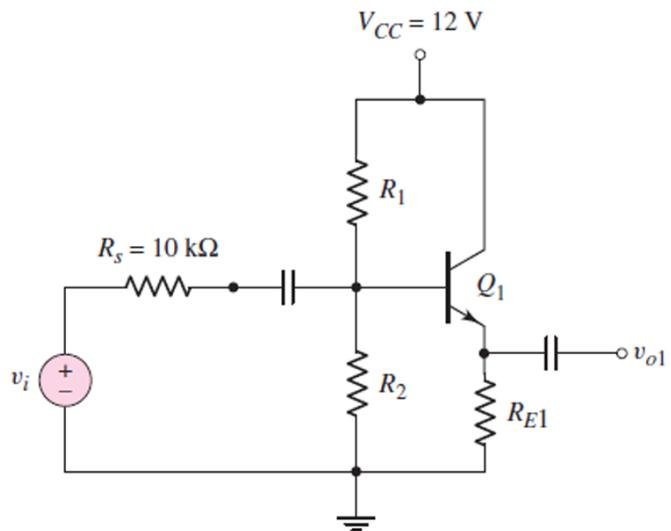


Figure 2. Input Buffer Stage Circuit Model

provides current amplification. This means that the emitter follower can deliver a higher current to the load than what is provided by the input signal alone. The emitter follower configuration is commonly used as a buffer stage between high-impedance signal sources and low impedance loads, providing current amplification while preserving the fidelity (shape, frequency, content, and amplitude) of the signal.

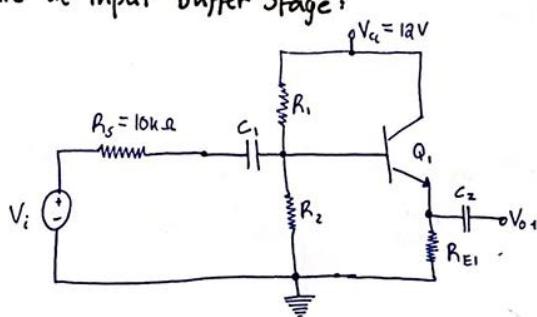
DC and AC Analysis:

Note that the given V_{CE} is greater than 0.2V which validates that the amplifier is functioning in the active mode.

Specifications and given parameters:

- Current gain $\beta_i = 100$
- Collector current $I_c = 1\text{mA}$
- Voltage at collector-emitter $V_{ce} = 6\text{V}$
- $R_1 \parallel R_2 = 100\text{k}\Omega$

The circuit at input buffer stage:



• Note that to solve this circuit will we conduct both DC and AC analysis

DC - Analysis

Step 1: We will only consider DC source. This means the capacitors C_1 and C_2 will be open circuited and our circuit will look like this (Fig 1.):

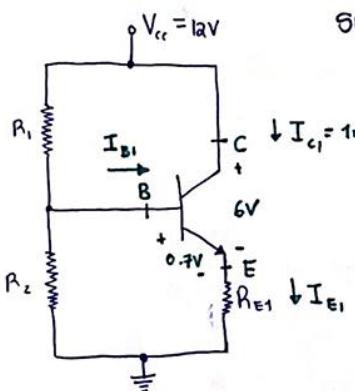


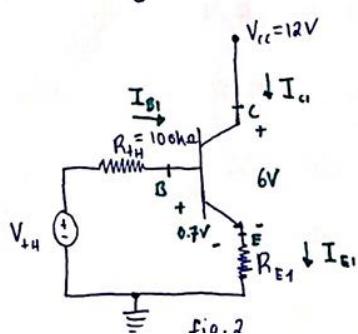
Fig.1

Step 2: Label the Base, collector, and emitter currents and calculate I_{B1} , I_{C1} , I_{E1} and R_1 and R_2

→ To Simplify this circuit we will find the Thevenin equivalent of the LITS of the circuit (fig 2.)

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \quad \text{and} \quad V_{TH} = V_{cc} \frac{R_2}{R_1 + R_2}$$

$$R_{TH} = 100\text{k}\Omega = \frac{R_1 R_2}{R_1 + R_2} \quad V_{TH} = 12 \frac{100\text{k}\Omega}{R_1}$$



→ Note that Amplifiers always operate in the active mode. This means $V_{BE} = 0.7\text{V}$ (the diode is ON at BE and OFF at BC)

→ let us find R_{E1} using Ohm's law at emitter:

$$6V = I_{E1} R_{E1} \quad \therefore \text{Given that } I_c = 1\text{mA} \text{ and that we are in the active mode}$$

$$R_{E1} = \frac{6V}{I_{E1}} \quad I_{c1} = \beta_1 I_{B1} \text{ and } I_{E1} = (\beta_1 + 1) I_{B1}$$

$$R_{E1} = \frac{6V}{1.01\text{mA}} \quad I_{B1} = \frac{1\text{mA}}{100} = 0.1\mu\text{A}$$

$$R_{E1} = 5940.594059\Omega \quad I_{E1} = (100 + 1) 0.1\mu\text{A} = 1.01\text{mA}$$

$$I_{B1} = 0.1\mu\text{A} \quad I_{E1} = 1.01\text{mA}$$

→ Now let us utilize KVL at lower loop of the circuit to find R_1 :

$$-V_{TH} + R_{TH} I_{B1} + 0.7 + R_{E1} I_{E1} = 0$$

$$12 \frac{100k\Omega}{R_1} \downarrow \quad 100k\Omega \downarrow \quad 0.1\text{mA} \quad \overbrace{6V}^{\sim} \quad \leftarrow \text{Substitute obtained values}$$

$$-12 \left(\frac{100k\Omega}{R_1} \right) + (100k\Omega)(0.1\text{mA}) + 0.7V + 6V = 0$$

$$R_1 = \frac{-12(100k\Omega)}{-(100k\Omega)(0.1\text{mA}) + 0.7V + 6V}$$

$$R_1 = 178837.5559\Omega \quad \leftarrow \text{Substitute } R_1 \text{ to find } V_{TH}$$

$$V_{TH} = 12 \frac{100k\Omega}{R_1} = 6.71V$$

→ Using our value of R_1 and the given $R_1 || R_2 = 100k\Omega$ we find R_2 :

$$\frac{R_1 R_2}{R_1 + R_2} = 100k\Omega$$

$$R_1 R_2 = 100k(R_1 + R_2)$$

$$R_1 R_2 = 100kR_1 + 100kR_2$$

$$R_1 R_2 - 100kR_2 = 100kR_1$$

$$(R_1 - 100k) R_2 = 100k R_1$$

$$R_2 = \frac{100k R_1}{R_1 - 100k} = \frac{100k + 178837.5559}{178837.5559 - 100k} = 226843.100\Omega$$

$$R_2 = 226843.100\Omega$$

\therefore Values obtained due to DC analysis of specifications:

$$I_{c1} = 1 \text{ mA}$$

$$R_{E1} = 5.94 \text{ k}\Omega$$

$$V_{TH} = 6.71 \text{ V}$$

$$I_{E1} = 1.01 \text{ mA}$$

$$R_1 = 179 \text{ k}\Omega$$

$$I_{B1} = 0.1 \mu\text{A}$$

$$R_2 = 227 \text{ k}\Omega$$

$$R_{TH} = 100.08 \text{ k}\Omega$$

AC-analysis

Step 1: Here, we consider the AC source only. This means all DC voltage sources are short-circuited (V_{DC}). Now the circuit looks like this (fig. 3). Note the capacitors become short circuited.

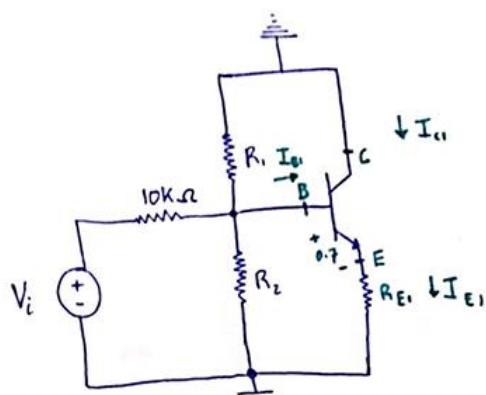


Fig. 3

Step 2: We draw the AC equivalent circuit to find the gain and r_n . See fig. 4

$$\rightarrow \text{We know that } r_n = \frac{V_T}{I_B} \text{ where}$$

$$V_T = 25 \text{ mV and } I_B = 0.1 \mu\text{A}$$

$$r_n = \frac{25 \text{ mV}}{0.1 \mu\text{A}} = 2500 \Omega$$

$$r_n = 2.5 \text{ k}\Omega$$

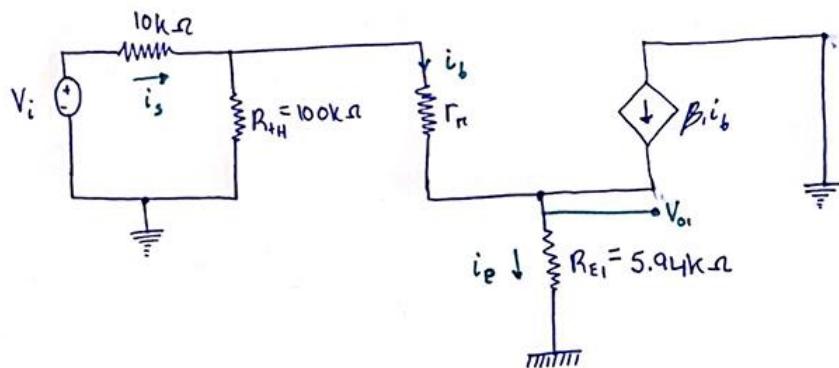


Fig. 4

Step 3: We find i_b , V_i and V_o to calculate the gain by analysing the AC small signal circuit (fig. 4)

$$i_b = i_s \frac{R_{HT}}{R_{HT} + r_n + (\beta+1)R_{EI}} \leftarrow \text{current division law}$$

$$i_b = i_s \frac{100k\Omega}{100k\Omega + 2.5k\Omega + 101(5.94k\Omega)} \text{ e.q. 1}$$

$$V_i = 10k\Omega(i_s) + (r_n + (\beta+1)R_{EI})i_b \leftarrow \text{KVL on LHS of the circuit}$$

$$V_o = i_{eI} R_{EI} \leftarrow \text{Ohm's law at emitter}$$

$$V_i = 10k\Omega(i_s) + (2.5k\Omega + 101(5.94k\Omega))i_b \text{ e.q. 2}$$

$$V_o = (\beta+1) \cdot i_b \cdot R_{EI} \text{ e.q. 3}$$

* Now we have three equations with three unknowns. With a little bit of algebra we can easily solve for i_b , V_o , V_i !

$$V_i = \left[\frac{10k\Omega}{100k\Omega} (100k\Omega + 2.5k\Omega + 101(5.94k\Omega)) + 2.5k\Omega + 101(5.94k\Omega) \right] i_b$$

$$V_i = 672684 i_b \leftarrow \text{Simplification of } V_i \text{ from eq. 2}$$

$$V_o = (101)(5.94k\Omega) i_b$$

$$V_o = 599 \text{ and } i_b \leftarrow \text{Simplification of } V_o \text{ from eq. 3}$$

* Now we can calculate the gain by cancelling out i_b ,

$$\text{gain} = \frac{V_o}{V_i} = \frac{672684 i_b}{599940 i_b} = 0.892$$

$$\text{gain} = 0.892$$

Gain Stage:

We observe the gain stage in Figure 4, which comprises a two-stage common-emitter amplifier configuration. Here, the buffer stage is capacitively coupled to the input of the amplifier, ensuring that no direct current (DC) passes through while allowing alternating current (AC) signals to transmit freely. Similarly, the two stages of the amplifier are capacitively coupled to each other in order to maintain signal integrity throughout the amplification process. Finally, the output of this amplifier is directly coupled to the output stage, facilitating efficient signal transmission without the need for additional coupling components.

The reason two BJTs are used in this stage is to increase the overall gain because the voltage gain of each stage is multiplied by the next. In addition to higher overall gain, two BJTs can achieve a higher input impedance and a lower output impedance, which can improve the overall performance of the amplifier. Furthermore, it ensures linearity of the system because if the system is non-linear it could lead to distortion of the signal.

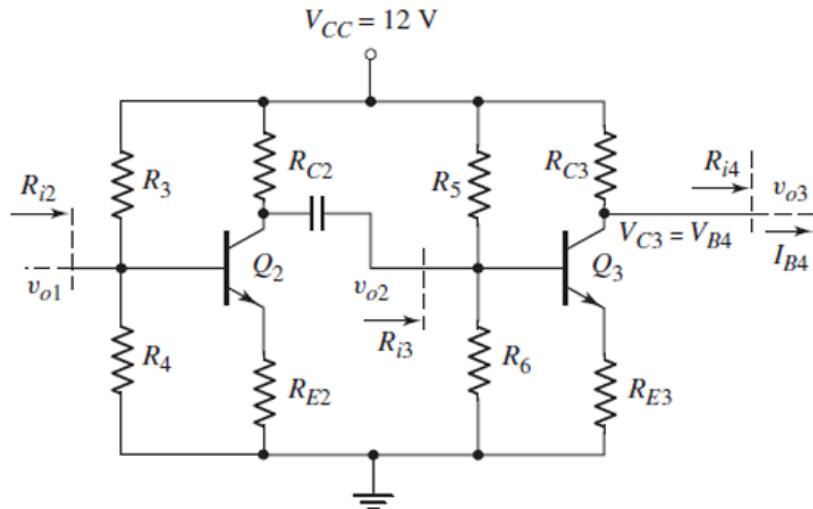
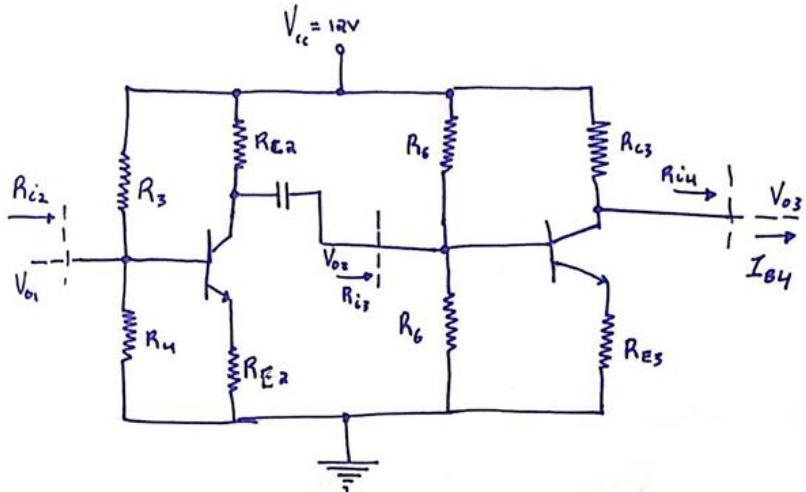


Figure 3. Gain Stage Circuit Model

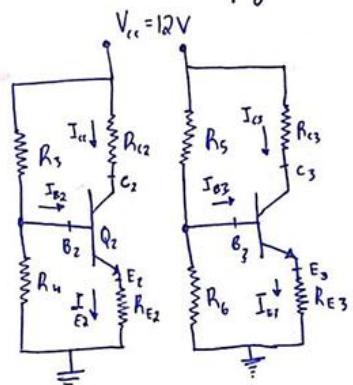
DC and AC analysis:

* To solve for the resistors values we will perform DC and AC analysis.



-DC Analysis

Step 1: Open circuit the capacitors given we are analyzing the DC mode of the circuit see fig.1

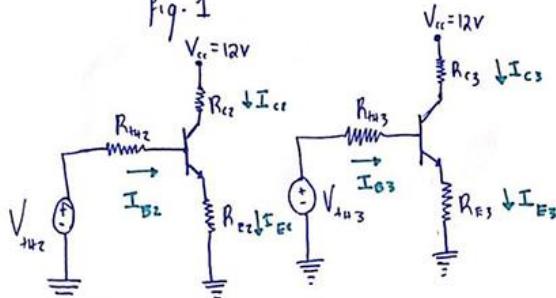


Step 2: To simplify the circuit we find the theorem equivalents of each circuit (fig 2 and fig 3)

$$R_{th2} = \frac{R_3 R_4}{R_3 + R_4} \quad V_{th2} = 12 \frac{R_4}{R_3 + R_4}$$

$$R_{th3} = \frac{R_5 R_6}{R_5 + R_6} \quad V_{th3} = 12 \frac{R_6}{R_5 + R_6}$$

fig. 1



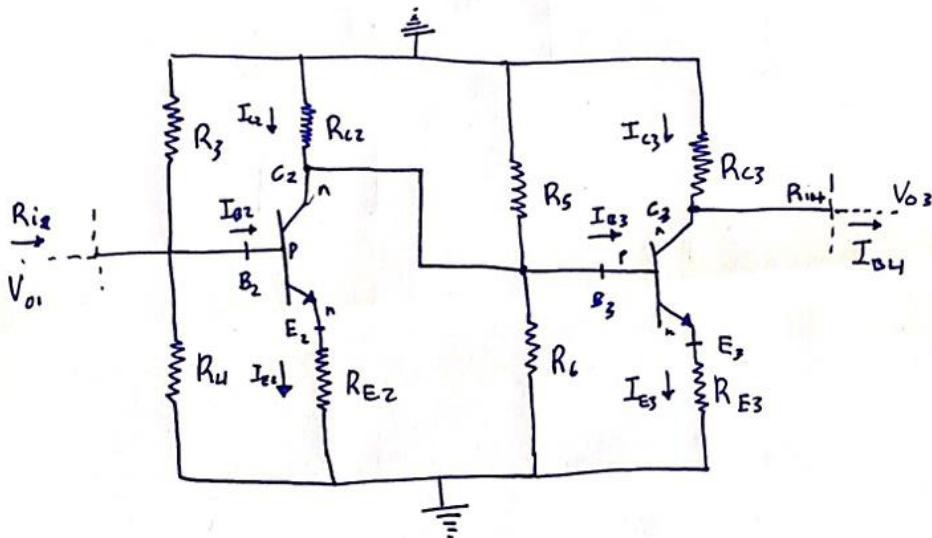
Step 3: Now we can assume the Resistors using the obtained gain. This means we'll need to perform AC analysis.

fig. 3

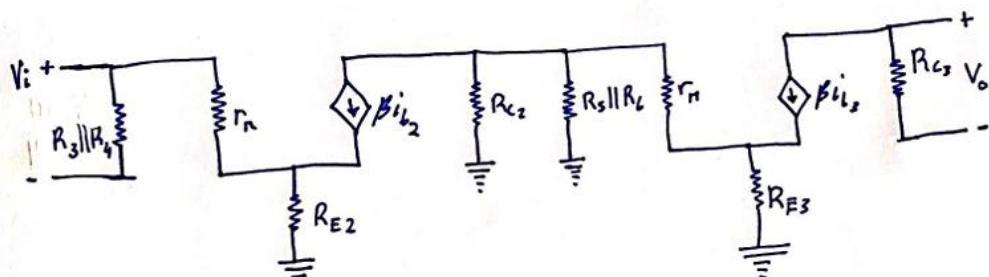
fig. 2

AC analysis :

↳ Since we are operating in AC mode, we will ground DC source short the capacitors



Step 1: Small signal circuit



$$I_{B3} = \left(\left(\frac{12 * R_3}{R_5 + R_6} \right) - 0.7 \right) / (R_S || R_6 + (\beta + 1) R_{E3})$$

$$R_6 = 103.3 \text{ k}\Omega$$

$$R_S = 96.9 \text{ k}\Omega$$

$$\text{gain} = \frac{1.269}{10 * 10^{-3}} = 126.5$$

$$\text{desired gain} = \frac{126.5}{0.892 * 0.05} = 144$$

Final:

$$R_3 = 155.84 \text{ k}\Omega$$

$$R_4 = 279.07 \text{ k}\Omega$$

$$R_{C2} = 450 \Omega$$

$$R_{E2} = 25 \Omega$$

$$R_S = 155.84 \text{ k}\Omega$$

$$R_6 = 279.07 \text{ k}\Omega$$

$$R_{E3} = 350 \Omega \quad R_{E4} = 12 \Omega$$

$$R_{..} = 10 \Omega$$

Output Stage:

In Figure 3, we observe the output stage, which is another emitter-follower amplifier circuit whereby the 8Ω speaker is connected to the amplifier's output through a decoupling capacitor. A decoupling capacitor is a type of capacitor that is usually used in power supplies and power sections of the circuit. They act as a local electrical energy reservoir that opposes quick changing voltage (AC signal) to provide the energy required to keep the voltage stable whenever the input voltage suddenly drops. They are commonly used in audio amplifiers or systems that require signal decoupling and isolation.. To deliver an average power of 0.1W to the load we calculate the root mean square (rms) value of the load current using the formula (see eq.1), yielding a rms load current (i_L) of approximately 0.112A :

$$P_L = i_{L(rms)}^2 * R_L \quad \text{eq. 1}$$

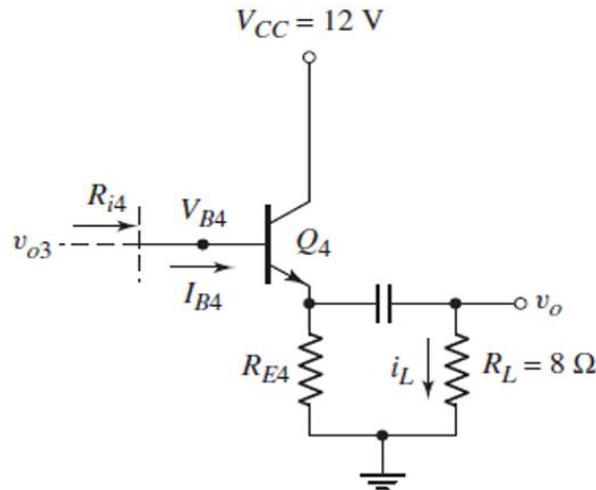


Figure 4. Output Stage Circuit Model

Power Analysis:

Specifications and given parameters:

$$\rightarrow \text{Average Power } P_L = 0.1W$$

$$\rightarrow \text{Load Current } i_L = 0.112A$$

$$\rightarrow \text{Load Resistance } R_L = 8\Omega$$

Step 1: Using eq.1 ($P_L = i_{rms}^2 R_L$) we can calculate i_{rms}

$$i_{rms} = \sqrt{\frac{P_L}{R_L}} = \sqrt{\frac{0.1}{8}} = 0.119A$$

$$i_{rms} = 0.119A$$

Step 2: Using i_{rms} we can find V_{rms}

$$V_{rms} = \frac{P_L}{i_{rms}} = \frac{0.1}{0.119} = 0.894V$$

$$V_{rms} = 0.894V$$

Step 3: We can then find V_{out} by simply multiplying V_{rms} with $\sqrt{2}$

$$V_{out} = \sqrt{2} V_{rms}$$

$$V_{out} = \sqrt{2} * 0.894V$$

$$V_{out} = 1.264V$$

Step 4: Lastly, we calculate the gain of the total circuit $\frac{V_{out}}{V_{in}}$.

* Note that $V_{in} = 10mV$

$$\frac{V_{out}}{V_{in}} = \frac{1.264}{10m} = 126.43$$

$$\frac{V_{out}}{V_{in}} = 126.43$$

Practical Simulation

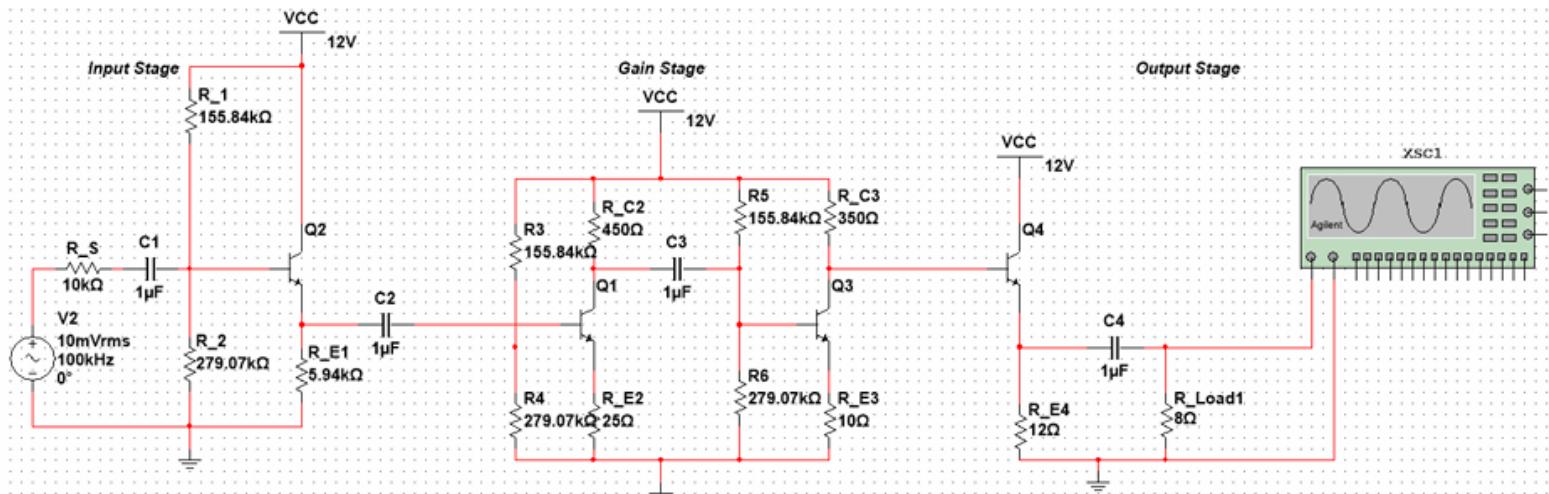


Figure 5. BJT Amplifier Complete Design

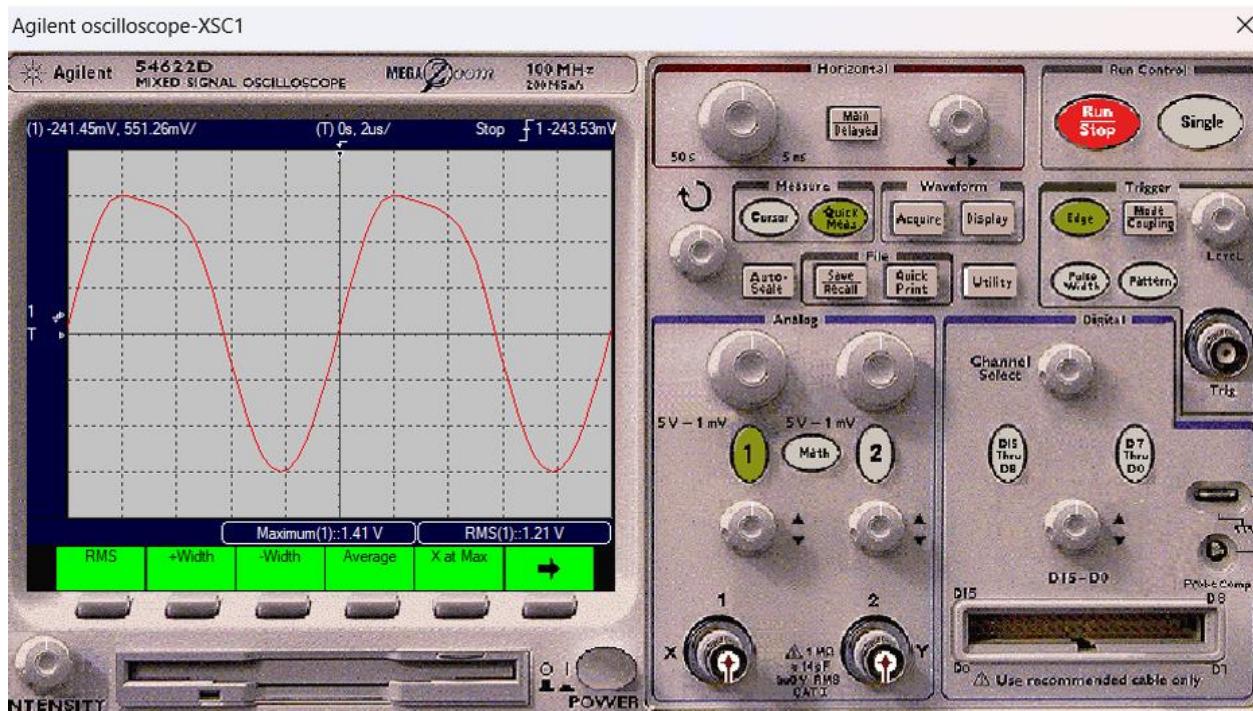


Figure 6. Oscilloscope Reading of BJT Amplifier

Comparison between Theoretical and Practical

Finally, the purpose of this section is to compare the theoretical predictions of our calculated values for resistances of the BJT amplifier. It is essential to validate our theoretical predictions with practical experimentation. This is because real life differs from handwritten mathematical equations. In reality, there are many external factors that can effect our circuitry and out results. Keeping these things into account can help improve the efficiency and liability of our system for future use and application. This comparison is also crucial at identifying any discrepancies that may arise during practical implementation of our design.

Firstly, we found that our obtained results for R_1 and R_2 were correct because they combined together to equate exactly 100.08k ohms. The margin of error could have resulted due to several factors, including variations in the tolerance of the resistors, temperature fluctuations affecting the resistance values, measurement inaccuracies with the testing equipment, and possible noise/interference in the circuit. To find the other values of R we simply repeated the same DC and AC analysis and ensured that we did not exceed the maximum voltage gain computed at the output stage. We applied this onto the simulation and found that our V_{rms} was equal to 1.21V (see figure 6) and the theoretical gain was 1.264. Calculating the percentage error using equation 2 we found that the error between theoretical and practical results was 4.27% which was fairly low.

$$\% \text{ Error} = \left| \frac{\text{Theoretical Value} - \text{Experimental Value}}{\text{Theoretical Value}} \right| \times 100 \quad \text{eq. 2}$$

By acknowledging and accounting for these potential sources of error, we can understand the limitations of our theoretical models and improve the precision of our practical designs.

Op-amp applications: A Square and a Triangle Signal Generator

A square wave Generator

In this section, we delve into an op-amp comparator that is used to design a square wave generator. The comparator is an electronic decision-making circuit that makes use of an operational amplifier's very high gain in its open-loop state, that is, there is no feedback resistor (see figure 8). Because the device is operating with no feedback when the positive input has a higher voltage than the negative input voltage, the output drives to the maximum voltage. Similarly, when the negative input voltage of the op-amp has a higher voltage than the positive input voltage, the output drives to the minimum voltage. To put it simply, the comparator compares two input voltages and changes its output state when one input exceeds the other.

In the design, the negative feedback path uses a capacitor while the positive feedback path does not. The capacitor in the negative feedback path causes a delay in the response of the circuit because when the input changes, the capacitor needs time to either charge up to the new voltage level or discharge to a lower voltage level (see figure 7). This allows the circuit to oscillate at a predictable rate depending on the capacitor's value.

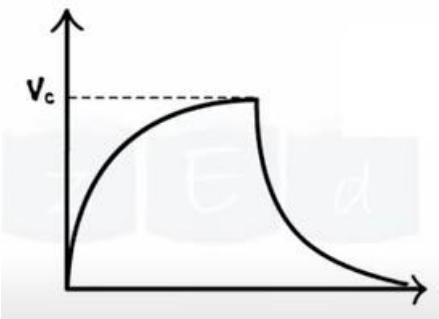


Figure 7. Capacitor charging when V_+ is greater than V_- and discharging when V_- voltage exceeds V_+

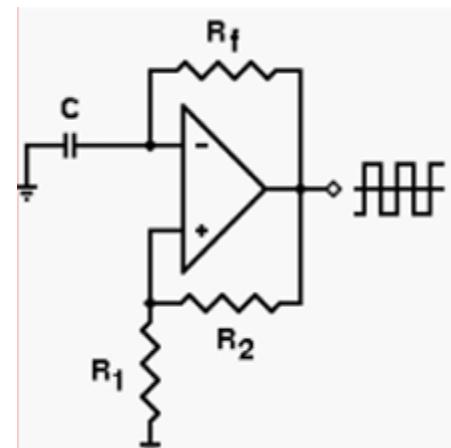


Figure 8. Schematic Diagram of a Square Wave Generator

Theoretical Calculations

This section explains the functioning of a comparator circuit without output voltage limitation. Initially set at -10 volts, the reference voltage at the positive ("+") input is determined by resistors R_1 and R_2 . This reference voltage remains fixed and negative. The circuit's output stays constant until the voltage at the negative ("−") input, connected to a capacitor (C) charging negatively through resistor R_f , surpasses the reference voltage. When this occurs, the output switches to +10 volts, causing the capacitor to begin charging positively. This cycle repeats continuously.

The output frequency of the circuit is given by the following equation:

$$f_{out} = \frac{1}{2Rf * C * \ln\left(\frac{2R_1}{R_2} + 1\right)} \quad eq. 2$$

In practice, the values of the circuit components are chosen such that R_1 is approximately $R_f/3$, and R_2 ranges from 2 to 10 times R_1 .

$R_1 = 27\text{ k}\Omega, R_2 = 100\text{ k}\Omega, R_f = 100\text{ k}\Omega, C = 0.01\mu\text{F}$

$$f_{out} = 1 / 2R_f \times C \times \ln\left(\frac{2R_1}{R_2} + 1\right)$$

$$f_{out} = 1 / 2 \times 100 \times 10^3 \times 0.01 \times 10^{-6} \times \ln\left(\frac{2 \times 27 \times 10^3}{100 \times 10^3} + 1\right)$$

$$f_{out} = 1157.990648 \approx 1.158 \text{ kHz}$$

Using Voltage Division:

$$V_f = (-10) \cdot \frac{R_1}{R_1 + R_2} = (-10) \cdot \frac{27 \times 10^3}{27 \times 10^3 + 100 \times 10^3} = -2.13 \text{ V}$$

- Therefore Voltage limit for Charging the Capacitor is = 2.13 V
- Because it repeats itself & is a Square wave the discharging limit for the Capacitor is = -2.13 V

Practical Simulation

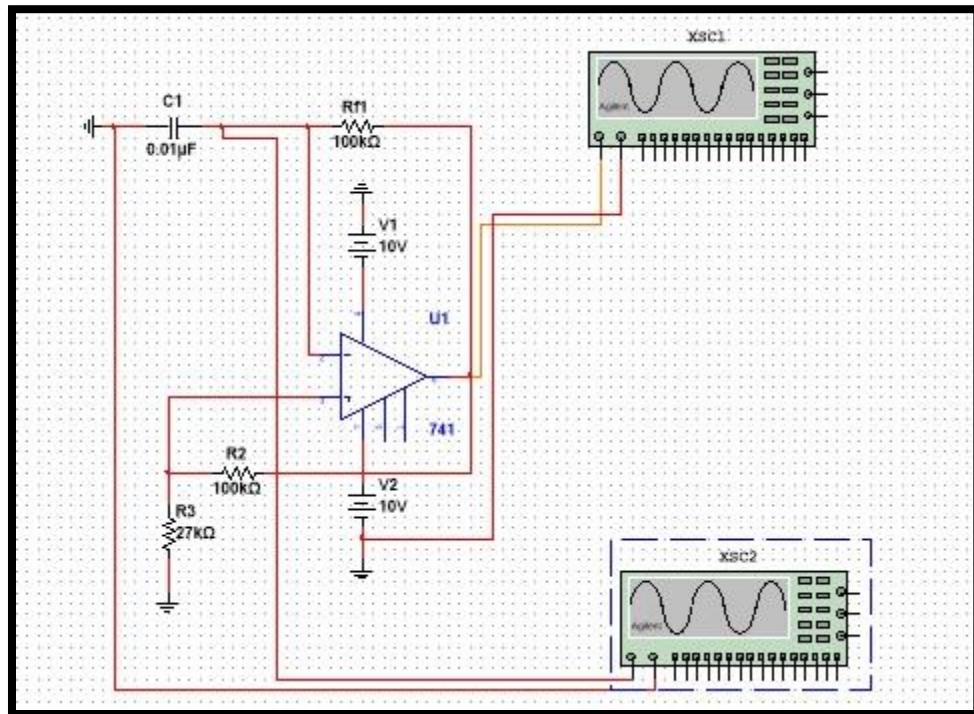


Figure 9. Multisim Simulation of Square Wave Generator

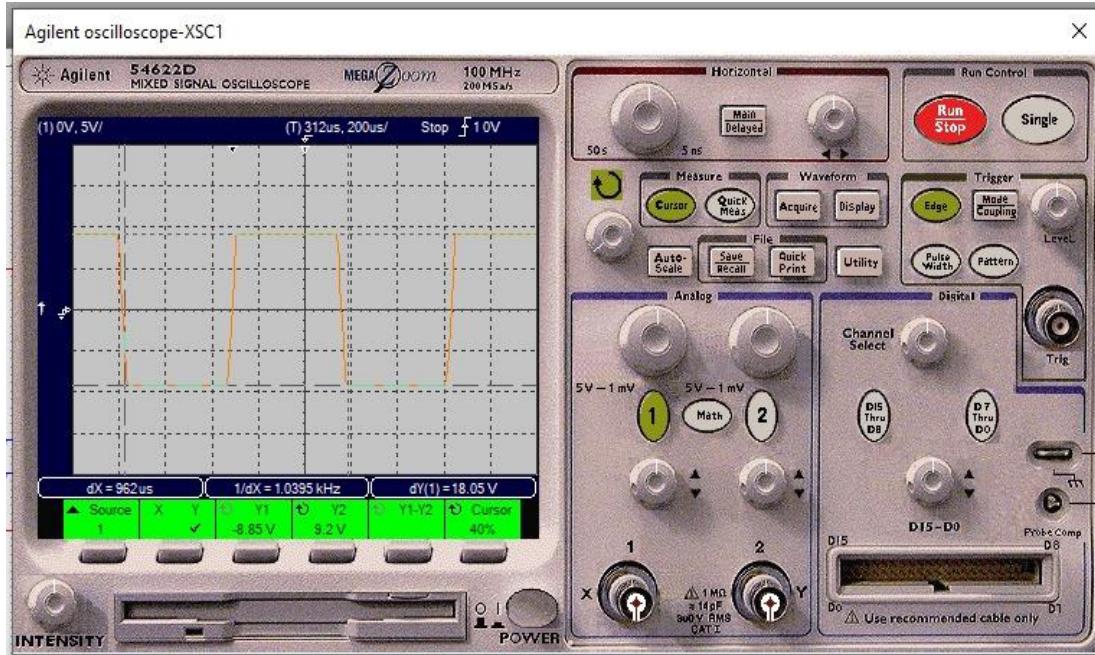


Figure 11. Oscilloscope Reading of Square Wave

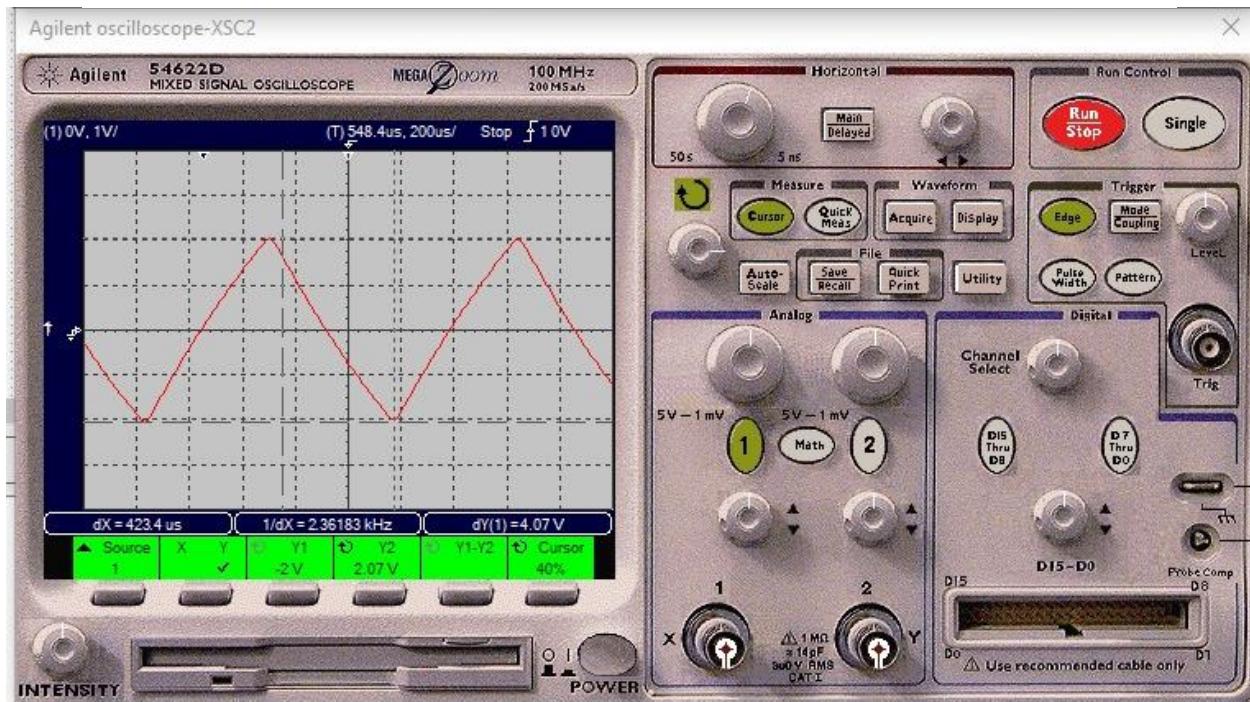


Figure 10. Oscilloscope of Triangle Wave input to Square Wave Generator Circuit

Comparison between Theoretical and Practical

Through calculations, we obtained a frequency of 1.158 kHz compared to the simulated reading of 1.0385 kHz (see figure 11). Using equation 2 we calculated the percentage error between these values to be approximately 10.3%. This error could arise from several sources, including component tolerances, where slight variations in resistors, capacitors, and inductors affect the frequency; parasitic elements such as unintended capacitances and inductances present in the physical circuit; and temperature variations that change the properties of electronic components. Additionally, discrepancies can stem from modeling assumptions that assume ideal behavior of components, which is not always the case in practice, and from measurement precision, as the accuracy and resolution of measuring instruments can introduce errors. The physical layout of the circuit can also introduce additional inductance or capacitance, altering the frequency from the theoretical value.

A triangular wave generator

We learned that if we input a square wave signal into an integrator we get a triangular wave. Additionally, from the previous section we identified that if we input a normal sinusoidal signal into the square wave generator, the generator outputs a square wave. So, in this section, to generate the triangular wave from a regular sinusoidal wave we connect a square wave generator to an integrator as shown in figure 12.

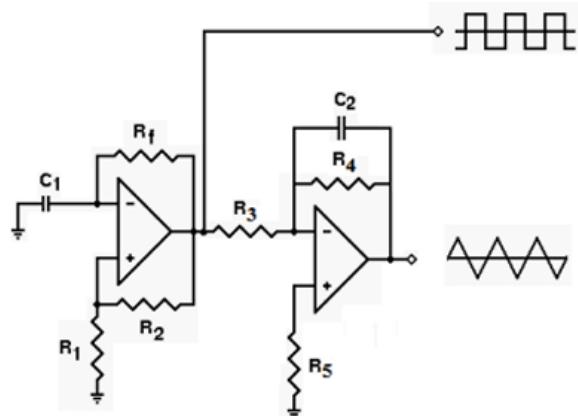


Figure 12. Schematic Diagram of triangular wave generator

Practical Simulation

Using multisim we generated figure 12 with the following values: $R_1 = 27 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$, $R_f = 100 \text{ k}\Omega$, $C_1 = 0.01 \mu\text{F}$, $C_2 = 0.1 \mu\text{F}$, $R_3 = 10 \text{ k}\Omega$, $R_4 = 100 \text{ k}\Omega$, and $R_5 = 10 \text{ k}\Omega$.

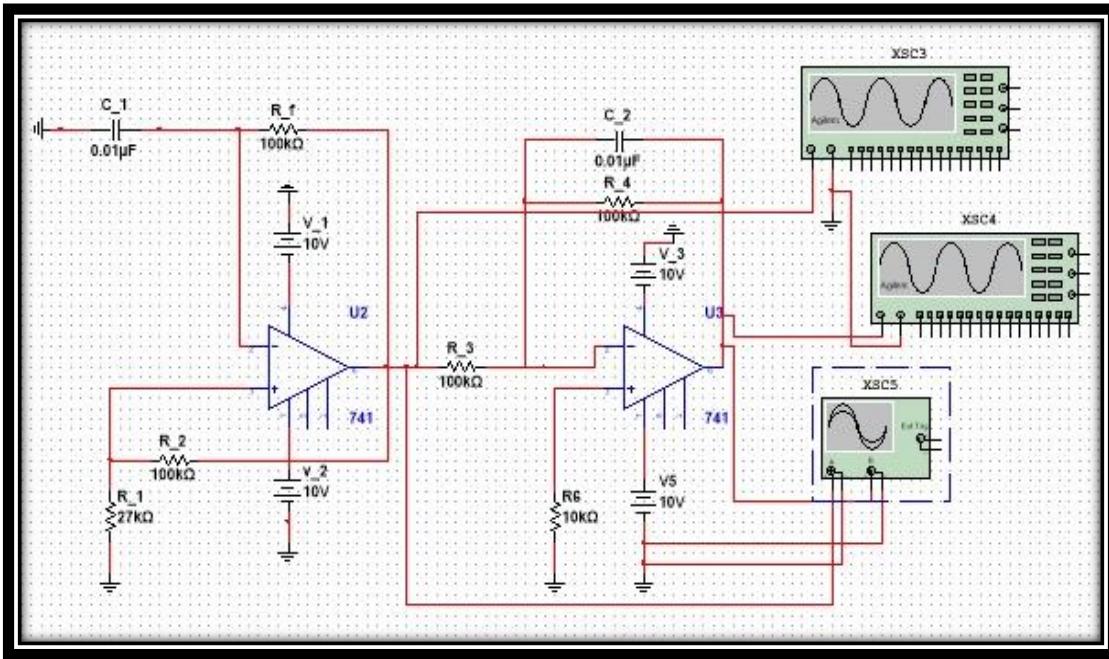


Figure 13. Multisim Simulation of Triangular Wave Generator

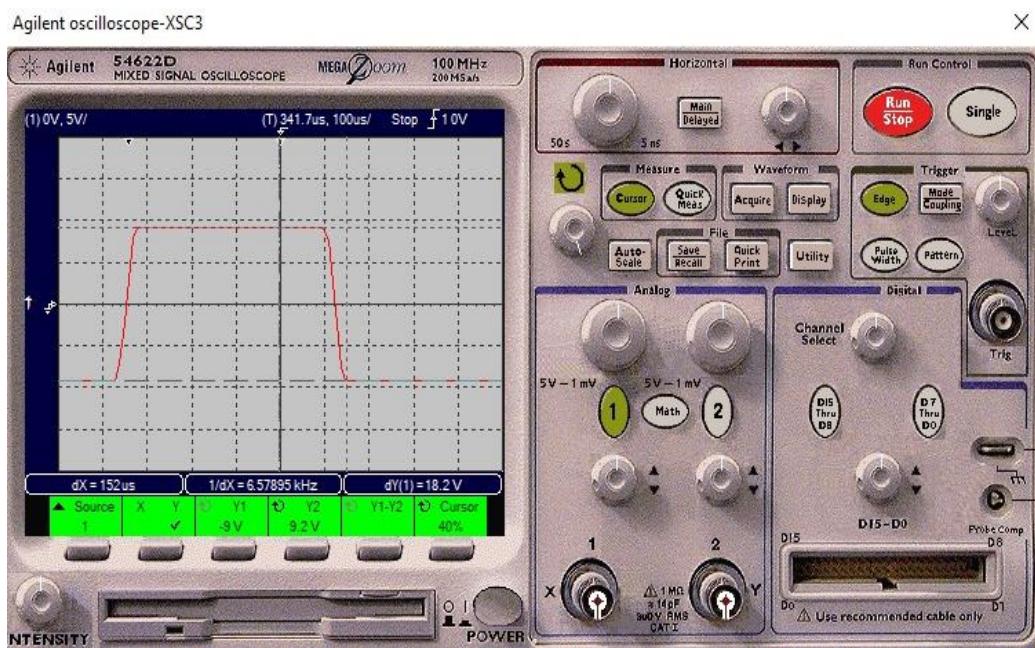


Figure 14. Oscilloscope Reading of Square wave before entering Integrator section of the circuit

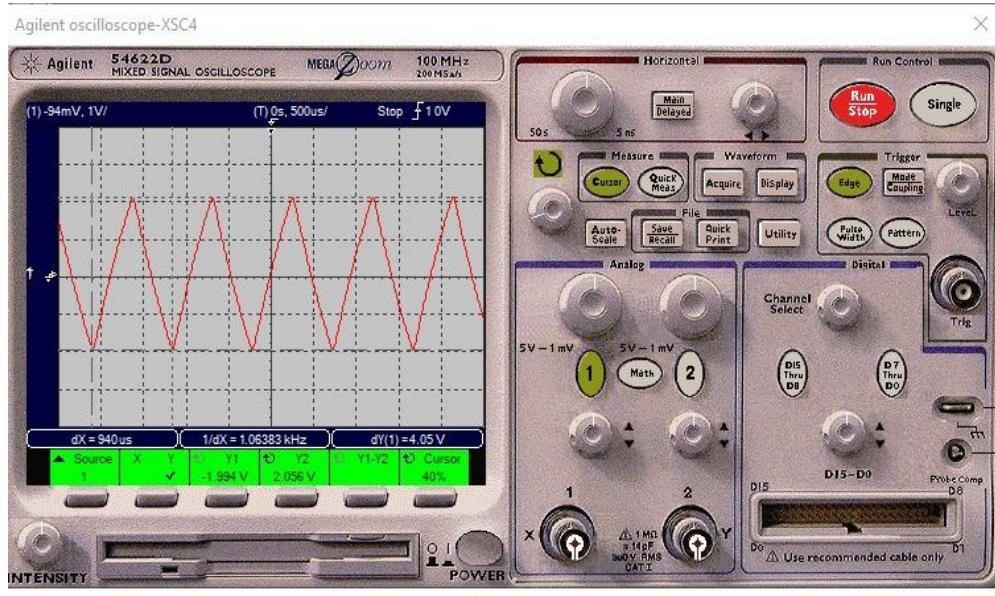


Figure 15. Oscilloscope Reading of generated a Triangular wave after square wave goes through the integrator part of the circuit

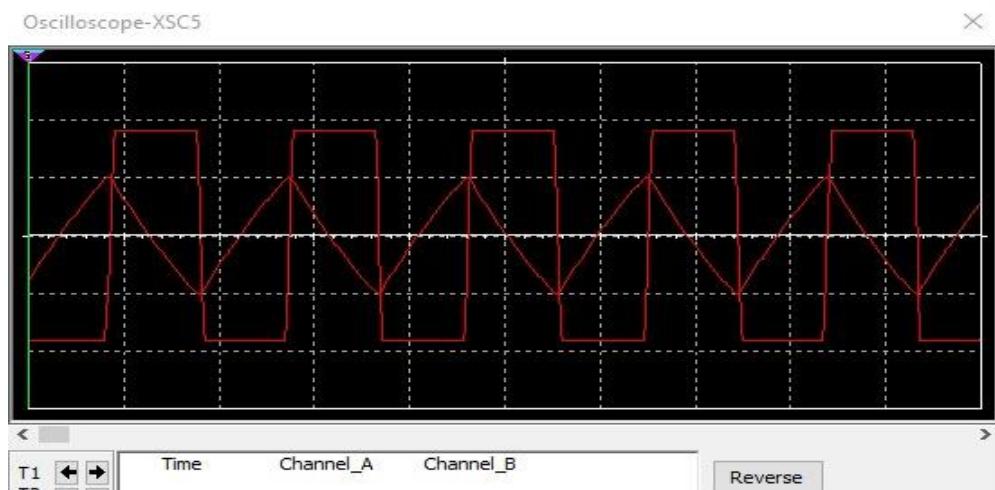


Figure 16. combination of both the square wave and triangular wave generated from the circuit

Looking at figure 16 we observe that the square wave has a higher amplitude than the triangular wave. This is because the integrator circuit averages the square wave's abrupt transitions into a linearly changing voltage, resulting in a waveform with a lower peak amplitude. This is a consequence of the mathematical process of integration, which converts the high amplitude steps of the square wave into the gradual slopes of the triangular wave.

CMOS applications: Logic Gates Implementation

In this section, we examine the transistor-level operation of a basic CMOS inverter, which uses enhancement-mode MOSFETs (E-type). The term “enhancement mode” means that the transistor is normally off when the gate-source voltage (V_{GS}) is zero which means the current is zero. They require an applied voltage between the gate and substrate to turn on, more specifically, when V_{GS} is above the threshold voltage V_{TH} the conductive channel forms. This allows current to flow from the drain to source for N-channel MOSFETs or from source to drain for P-channel MOSFETs. The upper transistor in the circuit is a P-channel MOSFET. When the substrate (connected to the positive voltage supply, V_{dd}) is more positive than the gate, the channel is enhanced, allowing current to flow between the source and drain. In this state, the P-channel MOSFET is on, providing a direct connection from V_{dd} to the output, making the output "high" (1) when the input is "low" (0). Meanwhile, the N-channel MOSFET, which requires a positive gate-to-substrate voltage to turn on, remains off because the input voltage is low. This creates a high resistance to ground, ensuring the output is solidly connected to V_{dd} .

When the input switch is moved to the other position, the lower transistor (N-channel MOSFET) turns on because it receives sufficient positive voltage between the gate and substrate. In this state, the N-channel MOSFET provides a low-resistance path to ground, making the output "low" (0). The upper P-channel MOSFET turns off due to zero voltage between its gate and substrate. This configuration illustrates the inverter or NOT gate behavior, where the output is always the opposite of the input. The use of both P-channel and N-channel MOSFETs in this complementary arrangement, known as CMOS (Complementary Metal-Oxide-Semiconductor), ensures that the output never floats and is capable of both sourcing and sinking current. This totem-

pole configuration is more efficient and simplified compared to earlier bipolar transistor designs, offering robust performance in digital circuits.

In general, when building any digital gate using MOSFETs, we follow three basic rules, the first being NFETs are used to pull the output down and PFETs are used to pull the output up. Second, never allow the output to be simultaneously pulled up and down. Lastly, we must always ensure that the output is either pulled-up or pulled-down, so that the output state is known. We applied these rules when constructing the inverter, NAND, NOR, AND, and OR gates out of MOSFETs.

Practical Simulation:

Inverter Gate

The simplest logic gate is composed of one NFET and one PFET as shown in figure. This satisfies rule number one of designing logic gates. The inverter outputs 0 when the input is 1 and 1 when the input is 0 (see Table 1). We connected both MOSFET gates to the same voltage (5V).

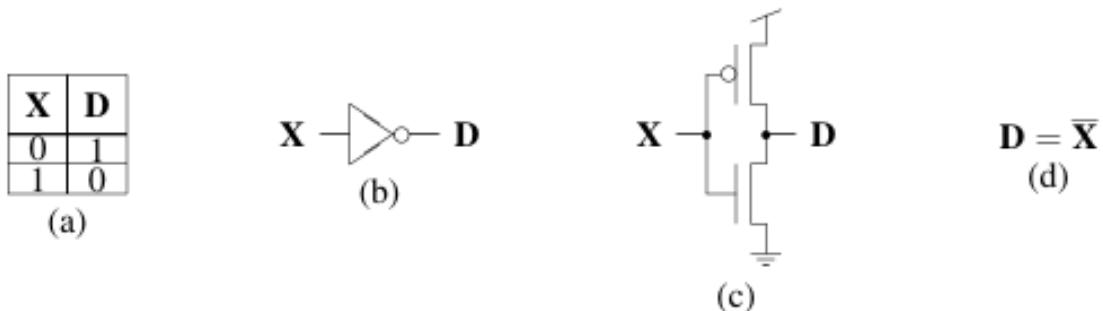


Figure 17. Inverter. (a). Truth table. (b) Symbol. (c) Schematic. (d) Boolean expression

To justify whether this configuration of N and P MOSFET gates, we applied the circuit in multisim and used a multimeter to read the voltage at the output (see figure 18 & 19). The output 1 was represented by the max voltage 5V, and the output 0 was represented as a very small number in the nanometers range.

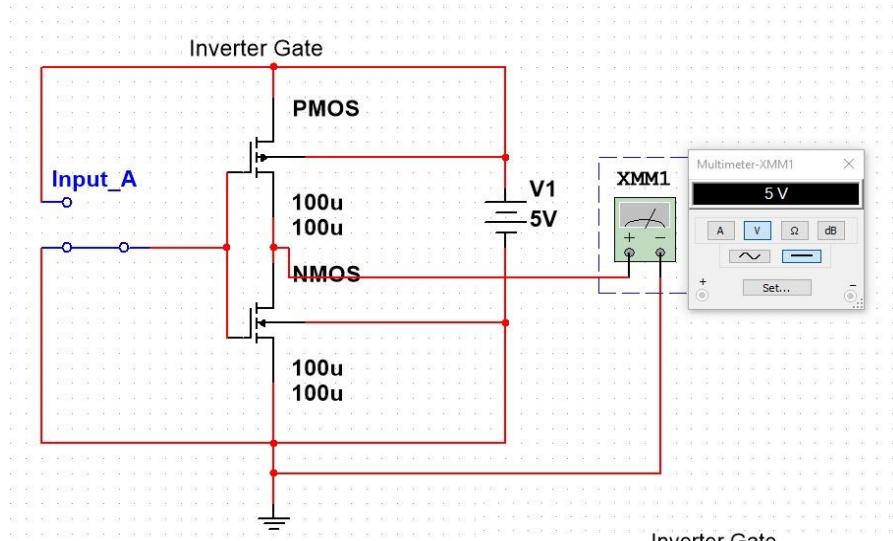


Figure 18. Multisim Simulation of Inverter gate when input is 0

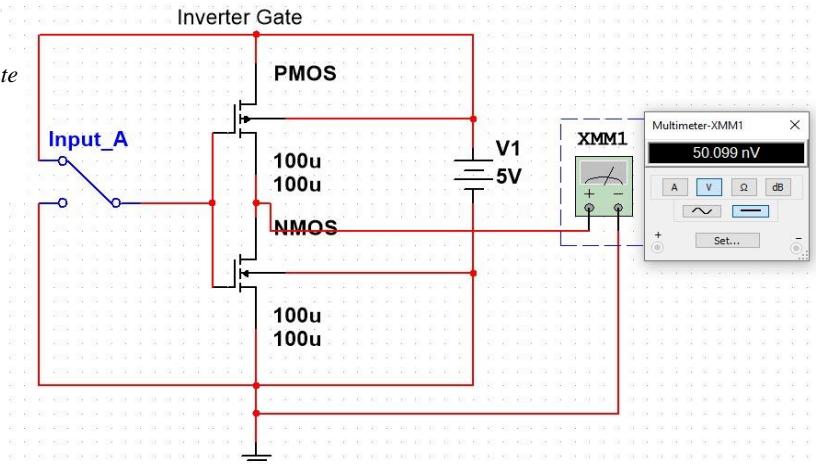


Figure 19. Multisim Simulation of Inverter gate when input is 1

NAND Gate

The next simple gate, the two input NAND gate, is comprised of two NFET gates connected together in series, and two PFETs in parallel. When the X and Y inputs of the NAND gate are both high the two NFETs turn on and pull the output down, while the two PFETs are both off, so neither is pulling the output high and we get 0. If either X or Y inputs are low, the NFETs will turn off, while the PFETs will turn on and pull the output high (see figure 20). An interesting point to note is that it is possible to extend the two input NAND gate into three inputs using three NFETs in series and three PFETs in parallel.

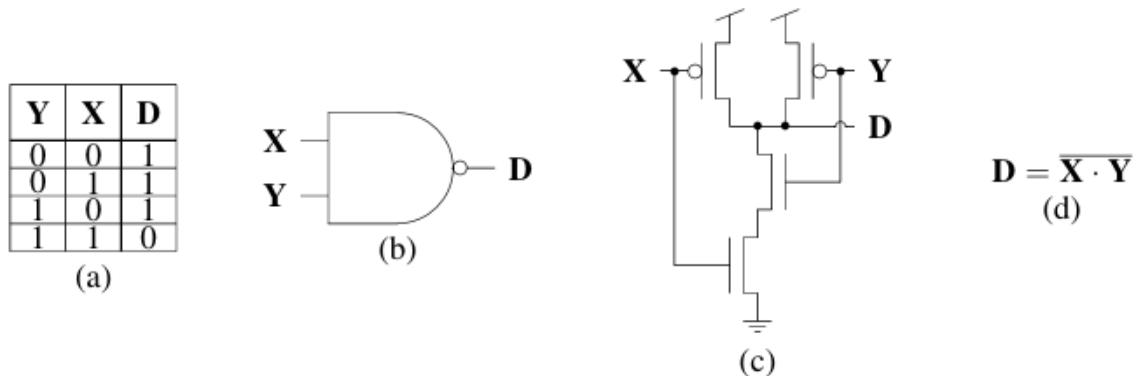


Figure 20. Two input NAND. (a) Truth Table. (b) Symbol. (c) Schematic. (d) Boolean Expression

To justify whether this configuration of N and P MOSFET gates, we applied the circuit in multisim and used a multimeter to read the voltage at the output (see figure 21, 22, 23, & 24). The output 1 was represented by the max voltage 5V, and the output 0 was represented as a very small number in the nanometers range.

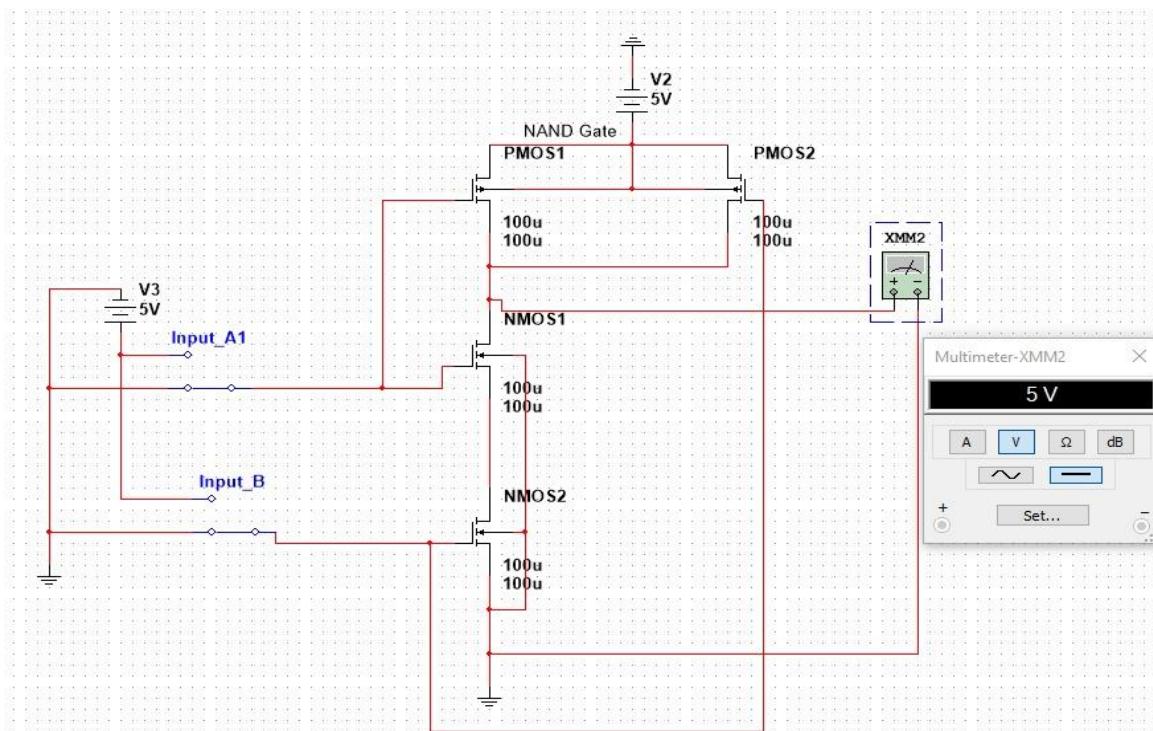


Figure 21. Multisim Simulation of NAND gate when both inputs are 0

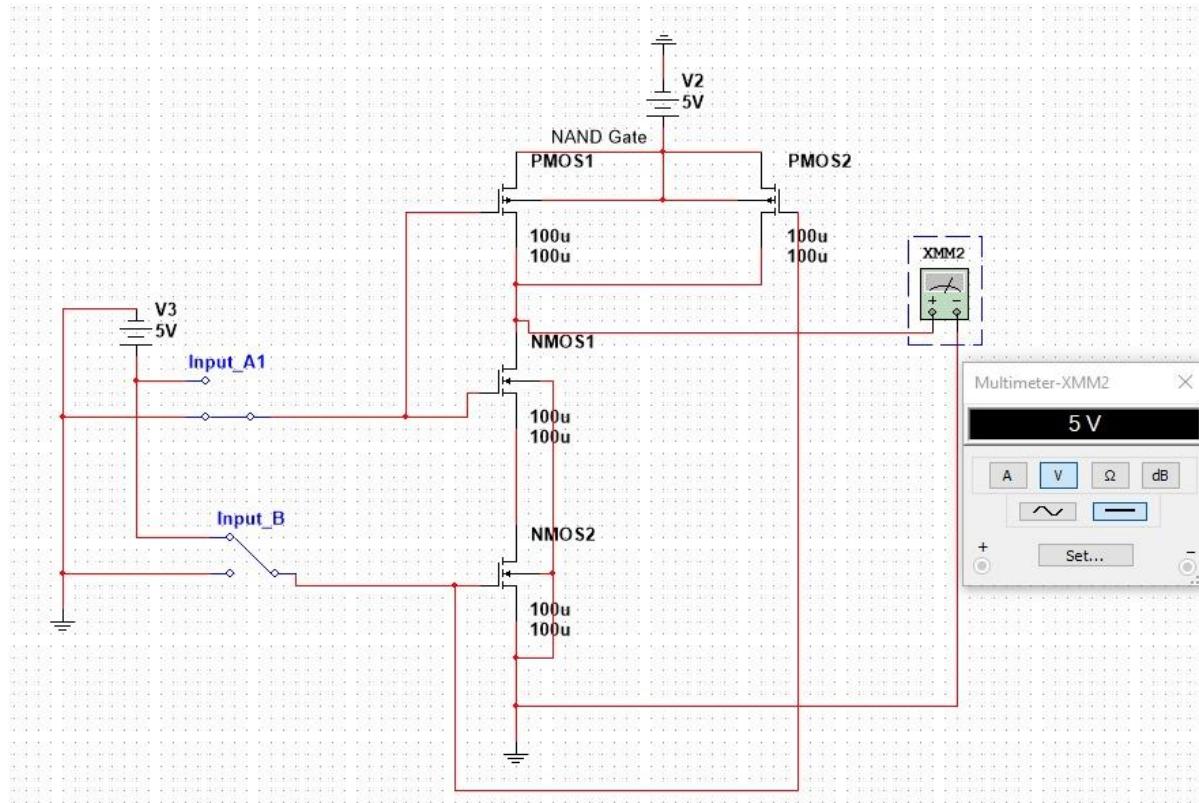


Figure 22. Multisim Simulation of NAND gate when input A is low and input B is high

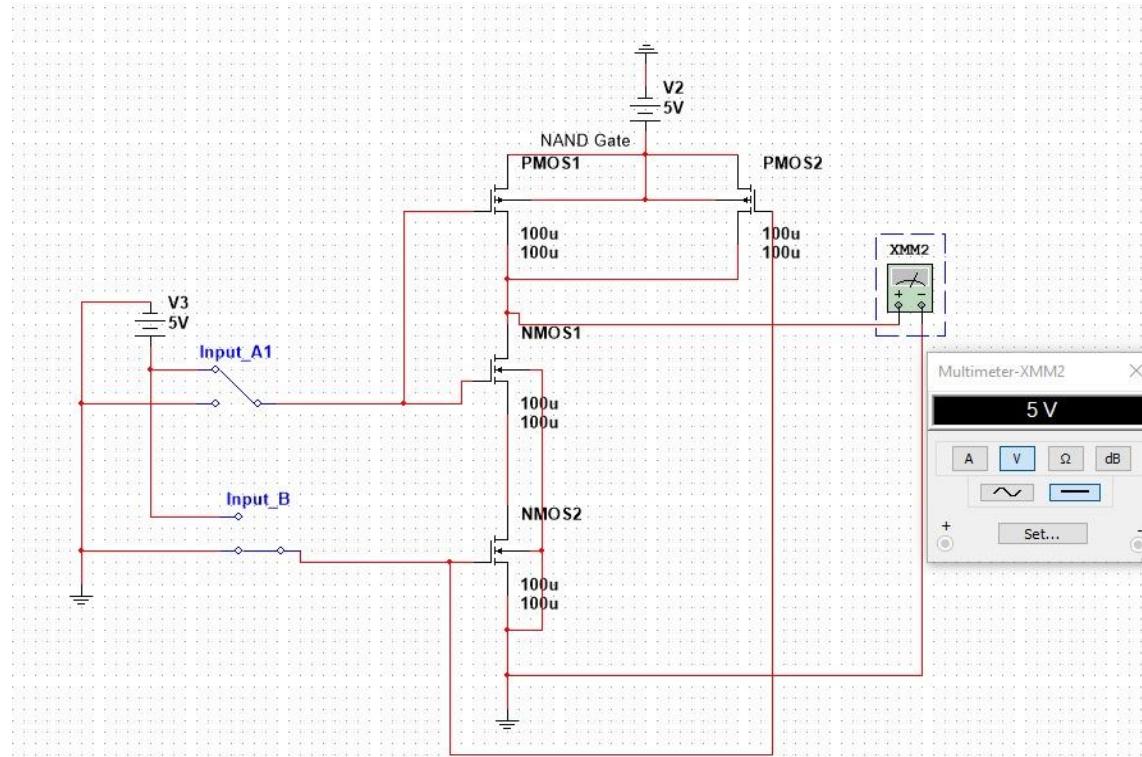


Figure 23. Multisim Simulation of NAND gate when input A is high and input B is low

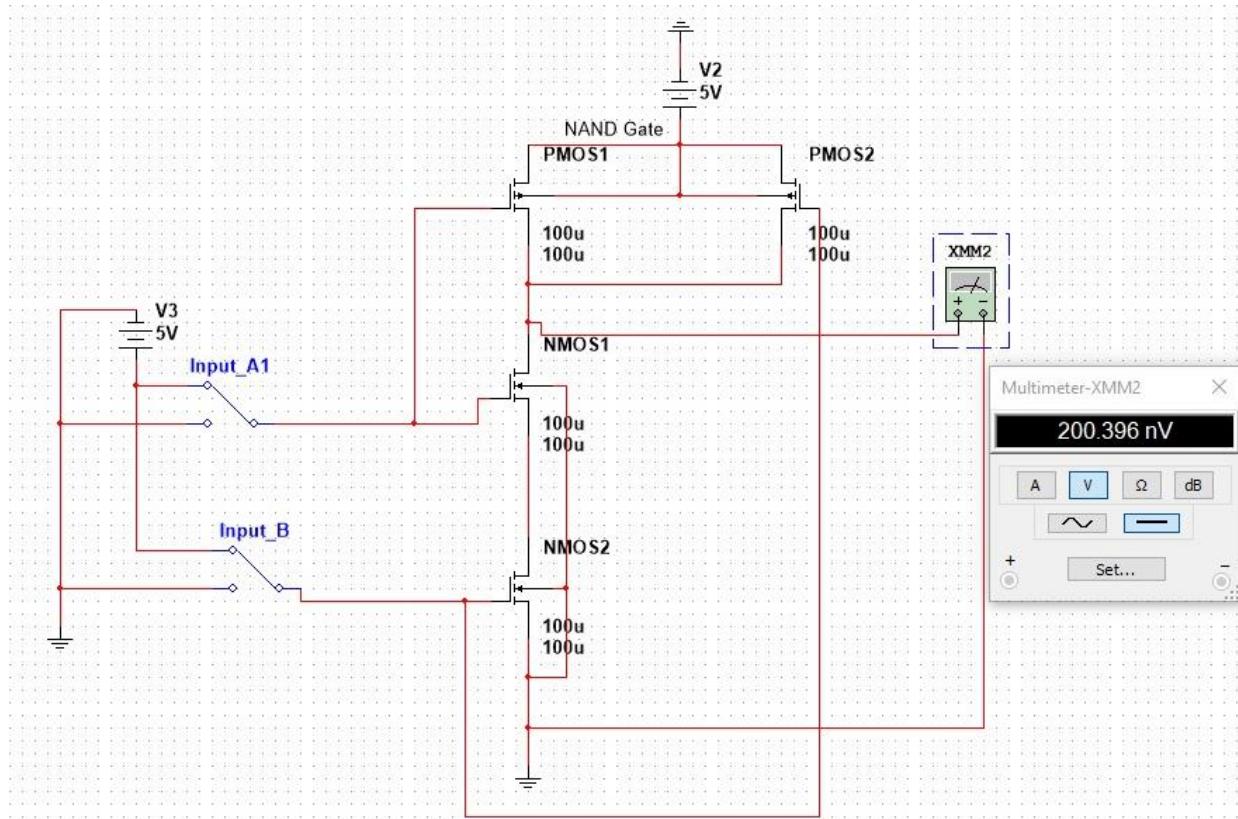


Figure 24. Multisim Simulation of NAND gate when both inputs are high

NOR Gate

If we take two input NAND gate and place the NFETs in parallel and the PFETs in series, we get a NOR gate as shown in figure 25. This gate also uses a combination of P and N MOSFETs through which when the X and Y inputs are low the output is high. Additionally, when one or both of the inputs are high the output is low.

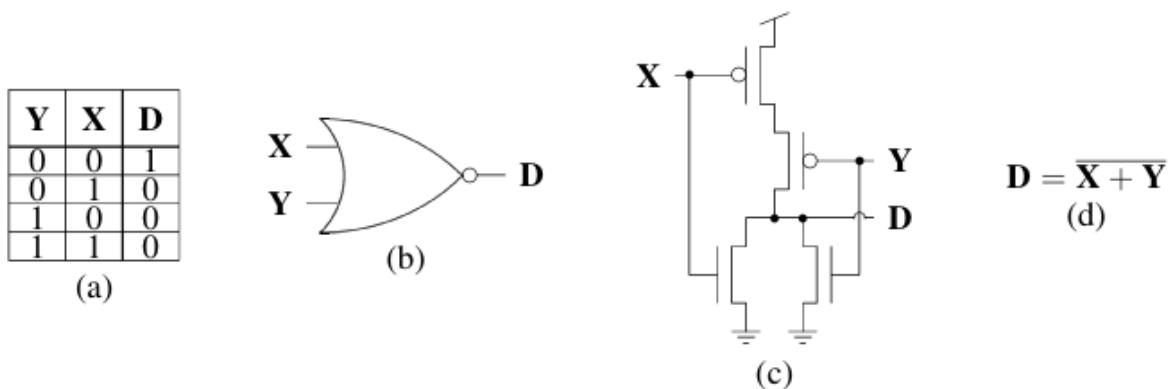


Figure 25. Two input NOR. (a) Truth Table. (b) Symbol. (c) Schematic. (d) Boolean expression

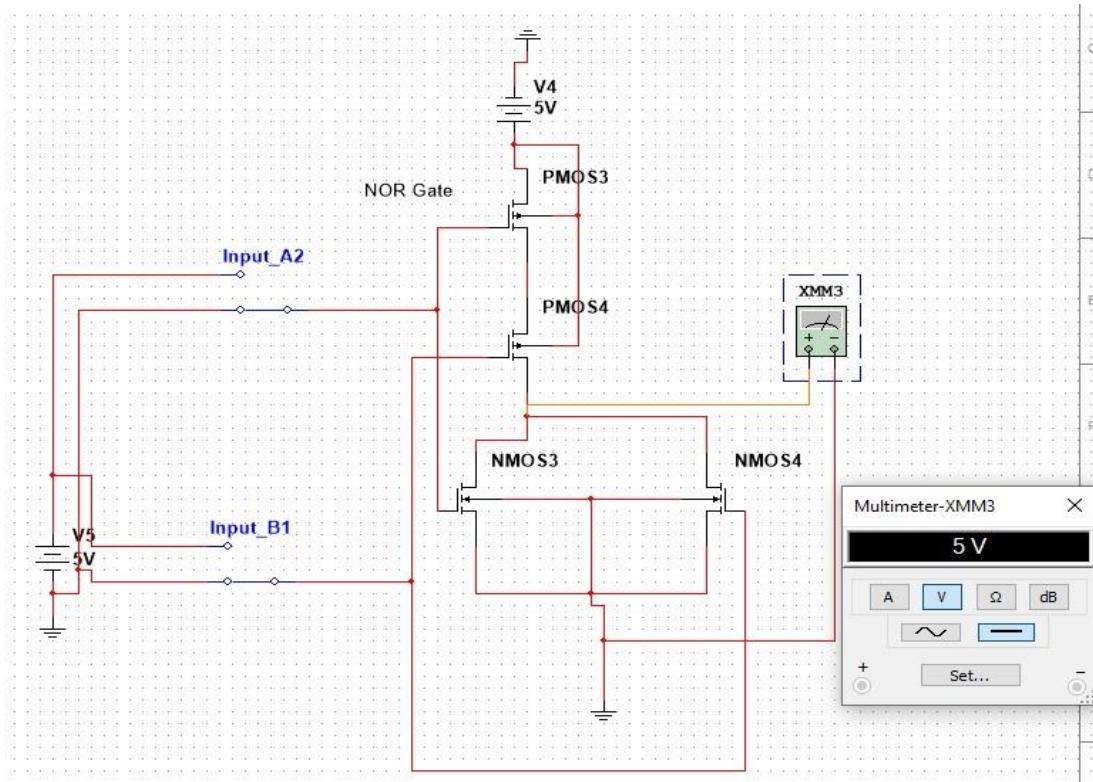


Figure 26. Multisim Simulation of NOR gate when both inputs are low the output is high

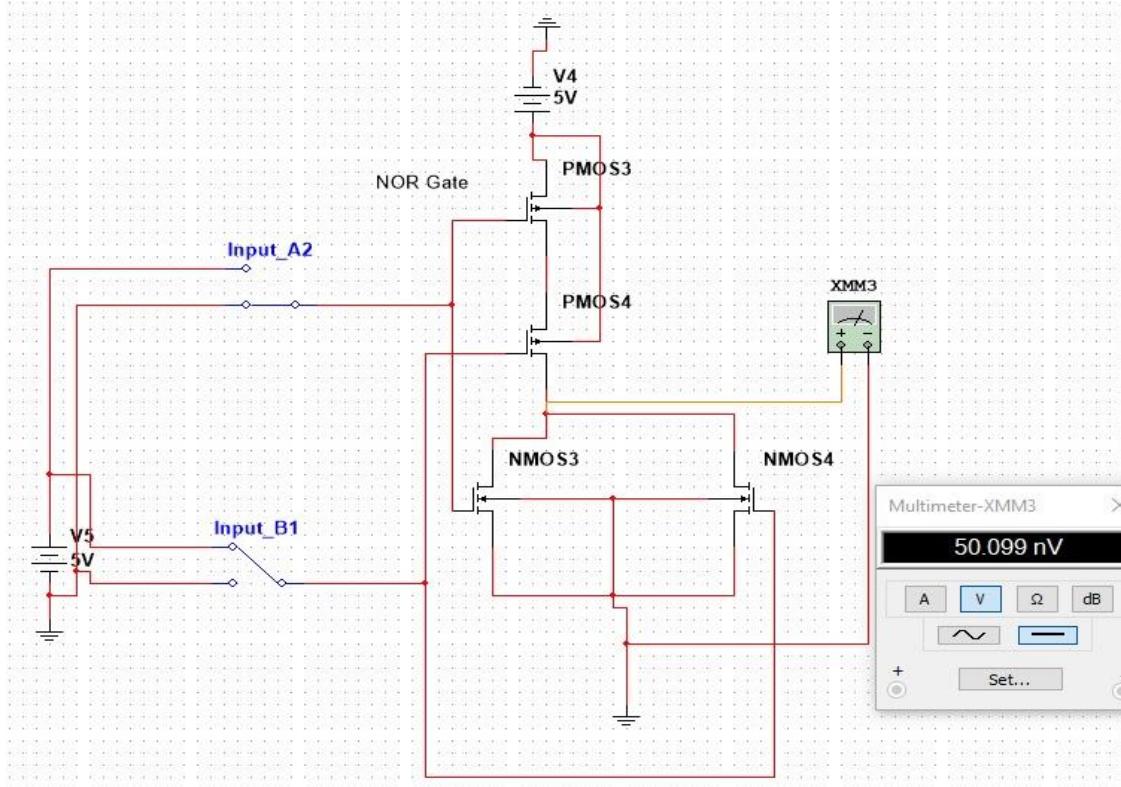


Figure 27. Multisim Simulation of NOR gate when input A and input B is high, the output is low

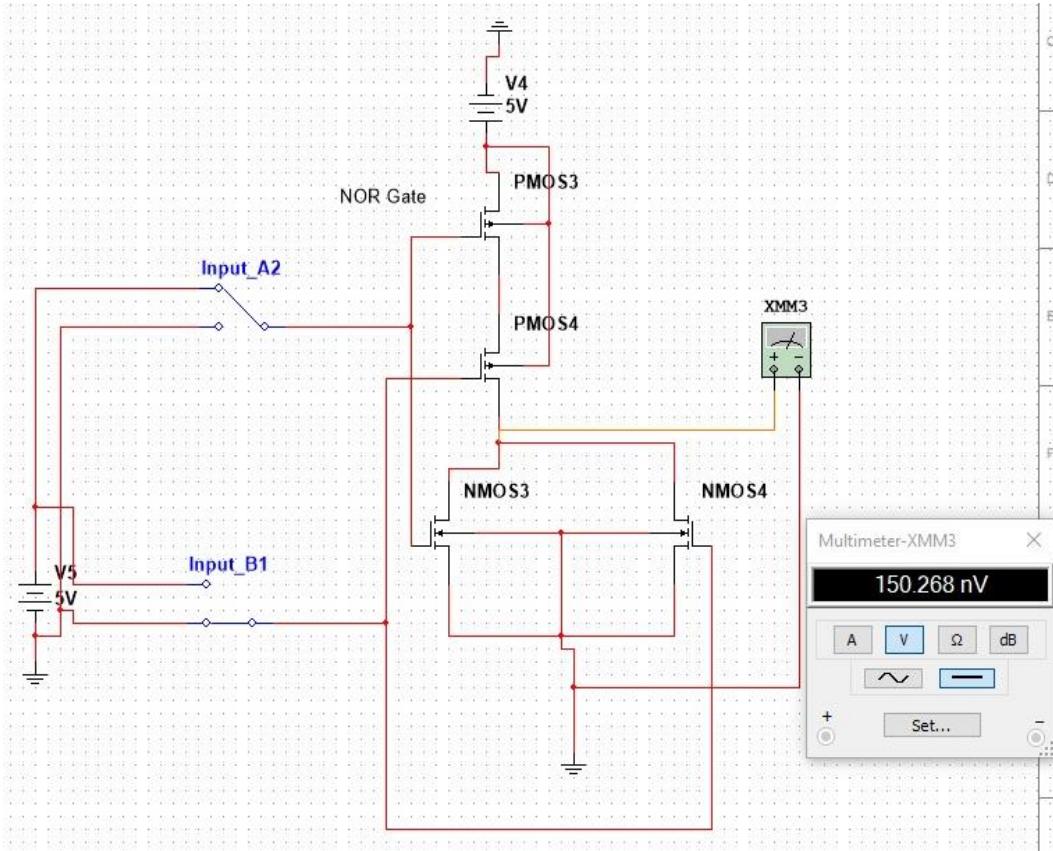


Figure 29. Multisim Simulation of NOR gate when input A is high and input B is low, the output is low

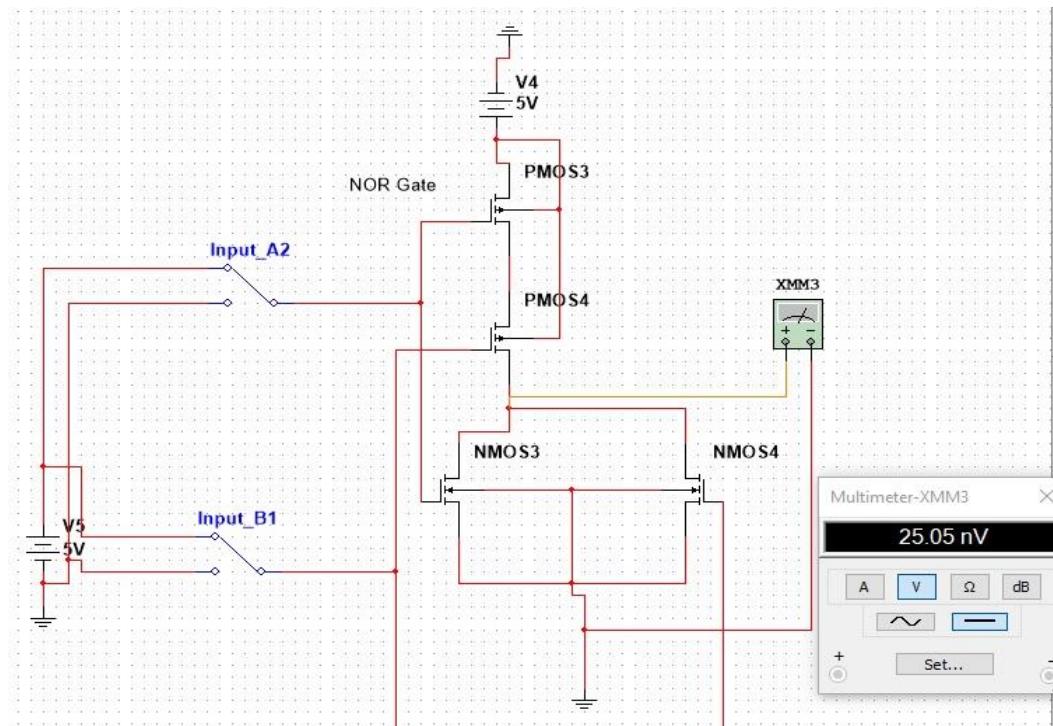


Figure 28. Multisim Simulation of NOR gate when both inputs are high, the output is low

AND Gate

To create an AND gate, two NAND gates are connected in series to each other. NAND gates and NOR gates are fundamental building blocks that can be used to design any type of logic gate. Examples include AND and OR gates. While our initial design for the AND and OR gates using NAND gates is straightforward and effective, further optimization could yield a more economical design.

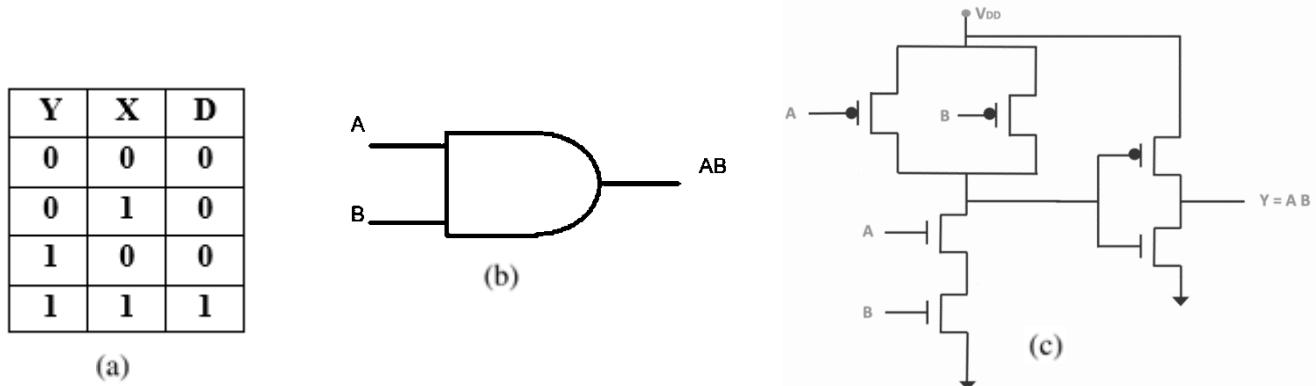


Figure 31. Two input AND. (a) Truth Table. (b) Symbol. (c) Schematic.

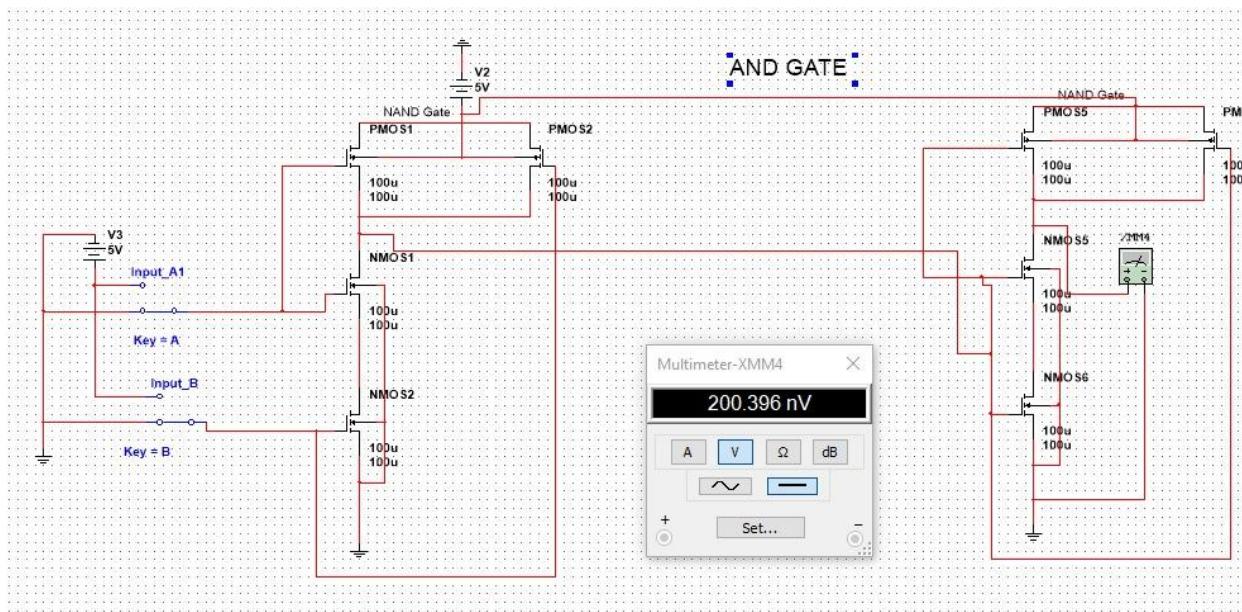


Figure 30. Multisim Simulation of AND gate when both inputs are low the output is low

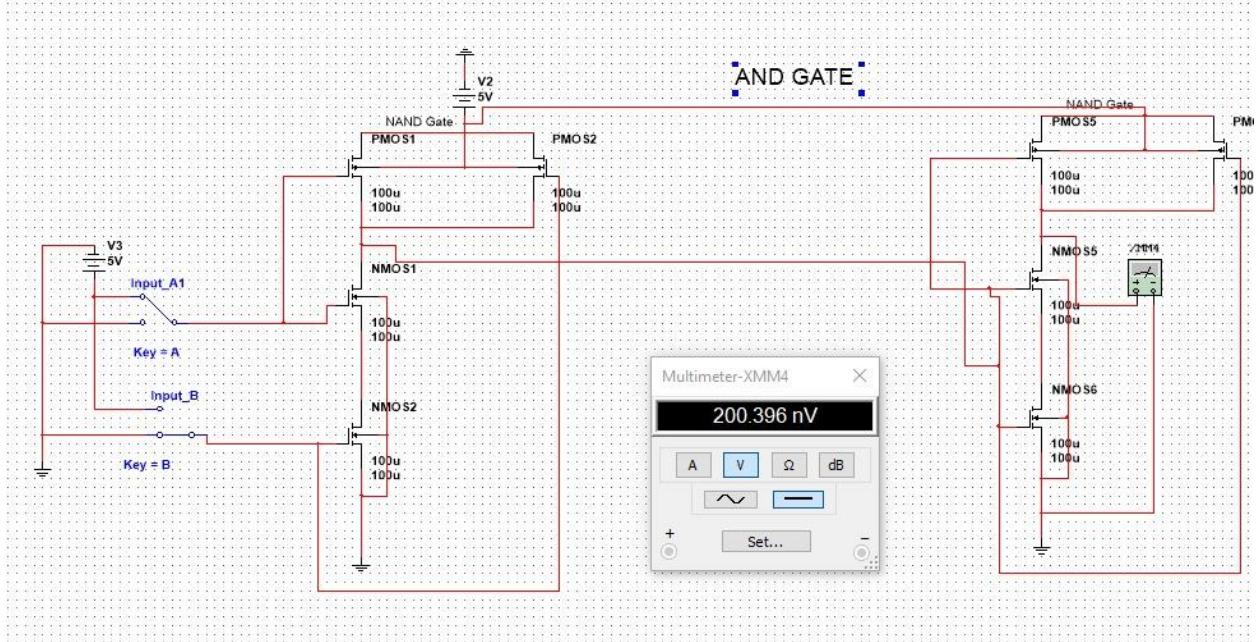


Figure 32. Multisim Simulation of AND gate when input A is high and input B is low, the output is low

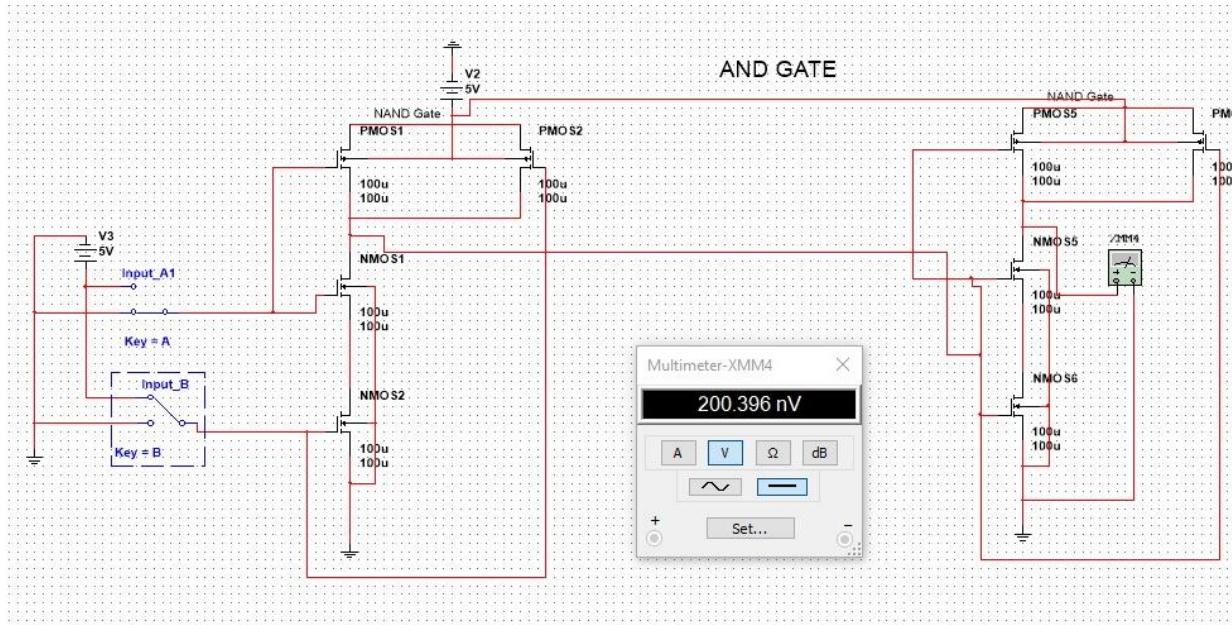


Figure 33. Multisim Simulation of AND gate when input A is low and input B is high, the output is low

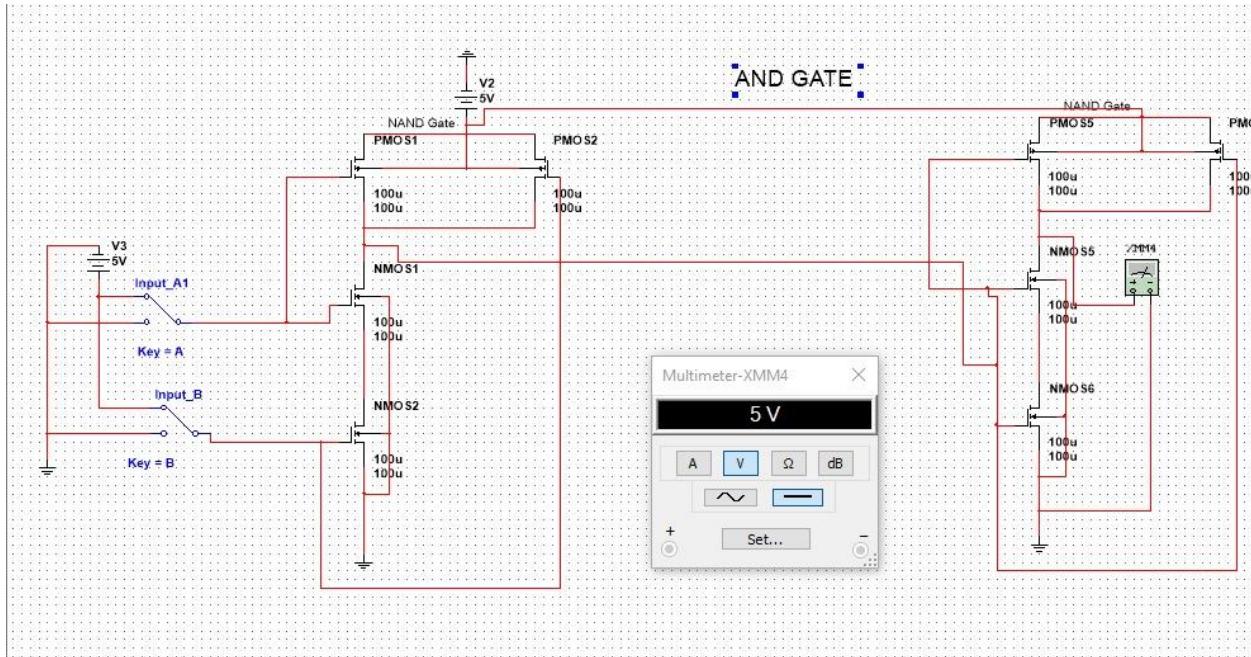


Figure 34. Multisim Simulation of AND gate when both inputs are high, the output is high

OR Gate

An OR gate can be constructed using two NOR gates or three NAND gates. This method leverages the versatility of NAND and NOR gates to build more complex logic gates. Like the AND gate design, this approach is straightforward, but additional simplification might lead to a more efficient and cost-effective solution for the OR gate.

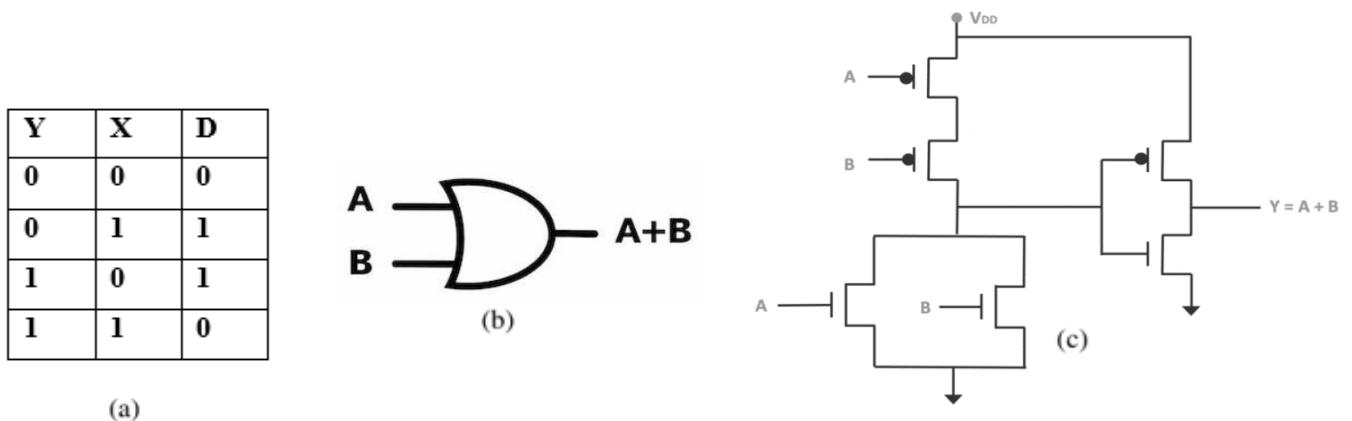


Figure 35. Two input OR. (a) Truth Table. (b) Symbol. (c) Schematic.

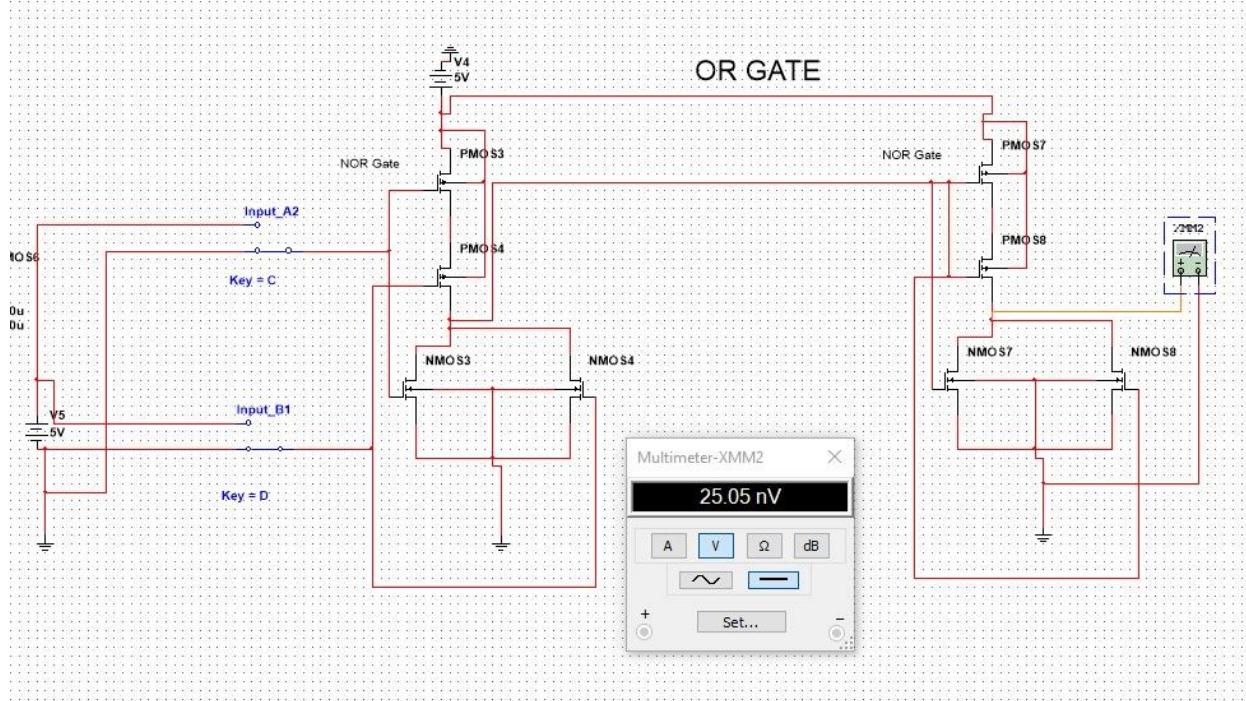


Figure 37. Multisim Simulation of OR gate when both inputs are low, the output is low

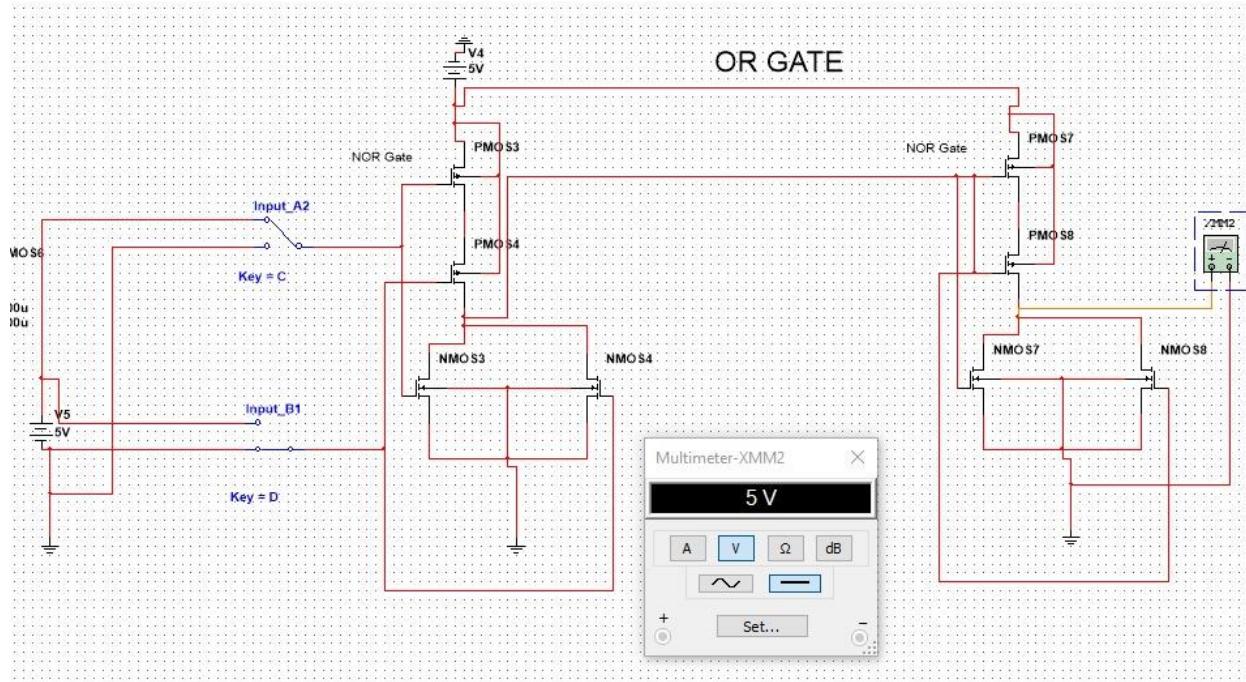


Figure 36. Multisim Simulation of OR gate when input A is high, and input B is low, the output is high

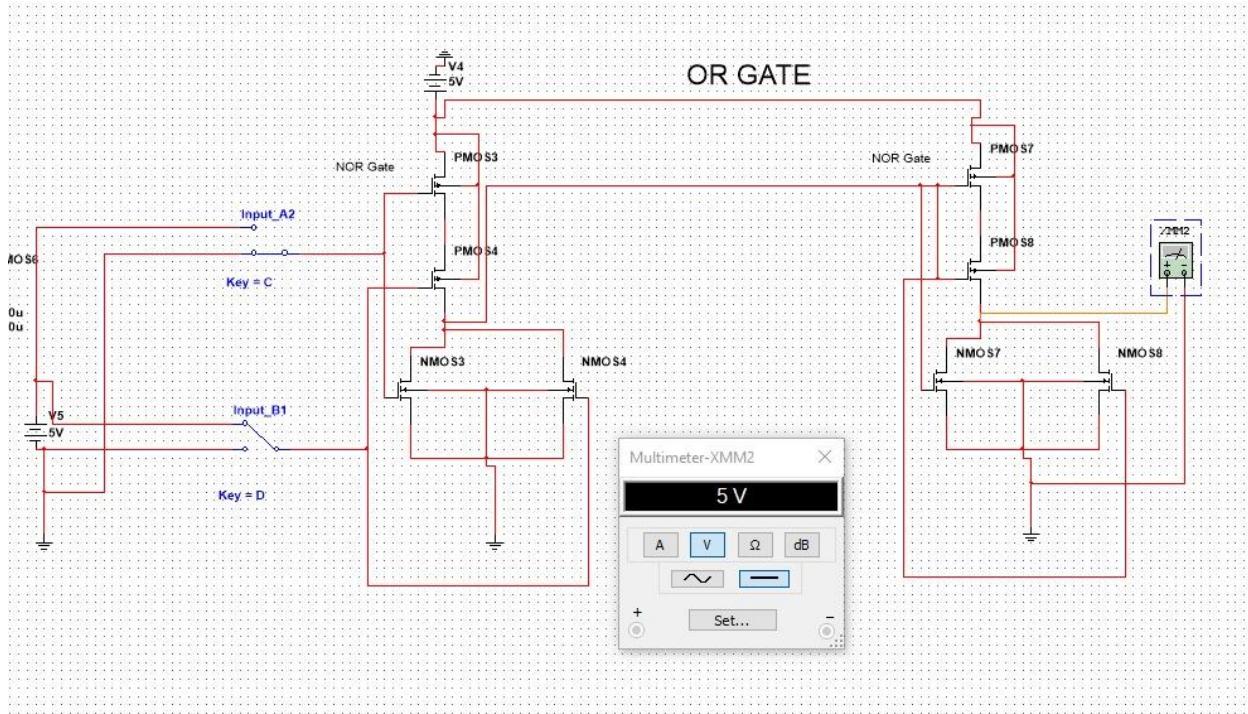


Figure 39. Multisim Simulation of OR gate, when input A is low and input B is high, the output is high

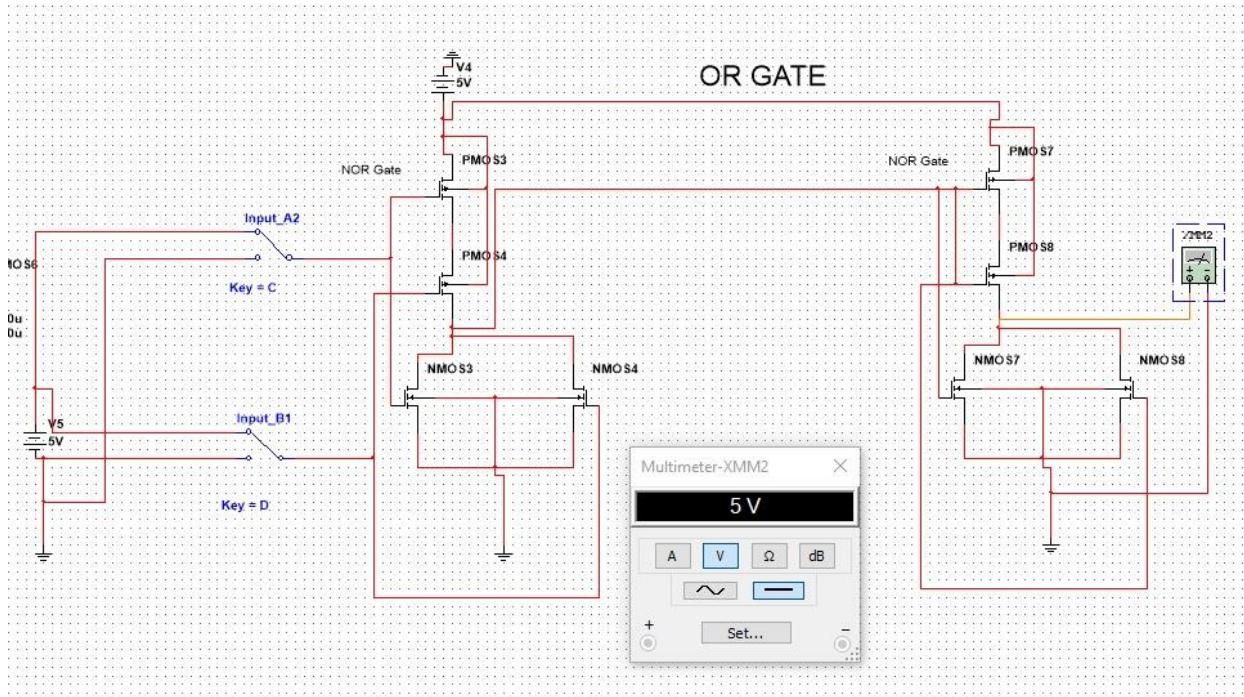


Figure 38. Multisim Simulation of OR gate, when both inputs are high, the output is high

Conclusion

In conclusion, this paper not only sheds light on the theoretical aspects of both MOSFET logic gates and BJTs amplifiers, but it also bridges the gap between theoretical calculations and design and practical simulations. By employing the circuit analysis tools and MULTISIM simulations, we have substantiated the reliability of our designs with minimal error. This was done with the guidance of the course TA and Professor Mohab. The subsequent exploration into wave generation further extends the practical applications of our research, paving the way for advancements in signal processing and electronic communication systems.

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