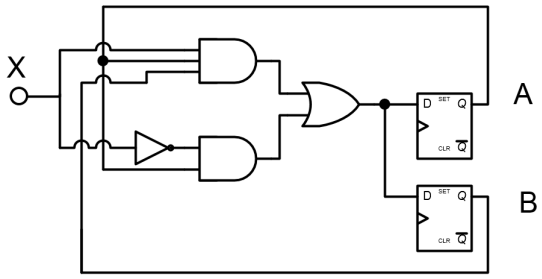
ELEC3500B Digital Electronics Exam April 2020 : DURATION 3 HOURS

VERSION 8

Instructions:

- Make sure you have downloaded the correct version of the exam.
- The exam version should match the last digit of your student number.
- For example, if you student number is 100973854 you use version 4.
- If the last digit of you student number is 0 you use version 10
- If you write the wrong exam you will received a mark of 0.
- For all questions select the best answer.
- Fill in the answers on the common answer spreadsheet that you downloaded from the CUlearn course webpage.
- Make sure you enter your name and student ID in the correct cells of the answer spreadsheet.
- Click on the correct option button for each question, do not modify the spreadsheet in any other way and save the spreadsheet without modifying the name or extension - save as exam.xlsx.
- You must upload the completed answer spreadsheet to the CUlearn course webpage within the allotted exam time or you will receive a mark of 0.

1. For the following FSM with state variables A and B and asynchronous input X, how many bad parent states are there (i.e. parent states that can result in bad state transitions)?

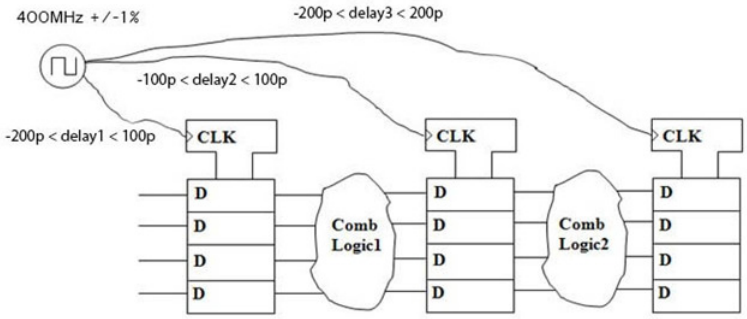


(a) 3 (b) 1 (c) 0 (d) 2

2. We represent time in verilog code using:

(a) ? symbol
(b) & symbol
(c) wait command
(d) all of the above

3. For the following timing circuit with $T_{SETUP} = 20$ps, $T_{HOLD} = -10$ps and $T_{CHQV} = 20$ps. If both combinational blocks have a minimum delay of 800ps and a maximum delay of 1100ps, how large could the clock frequency become (assume spread spectrum clock is still plus or minus 1%)?



(a) 739MHz (b) 746MHz (c) 799MHz (d) 688MHz

4. We like to use pipelining in FPGA circuits to:

   (a) increase operating frequency
   (b) increase input to output delay
   (c) decrease $T_{PD_{MIN}}$
   (d) increase $T_{PD_{MAX}}$

5. Why do we prefer to use clocked inverters instead of transmission gates in D latches?

   (a) easier to test
   (b) fewer transistors
   (c) lower power consumption
   (d) all of the above

6. How many errors does the following verilog test bench module code have?

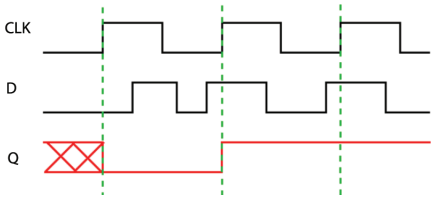
```
`timescale 1 ns/10 ps
module half_adder_tb;
    wire a, b, sum, carry;

    half_adder UUT (.a(a), .b(b), .sum(sum), .carry(carry));

    initial
        begin
            a = 0;
            b = 0;
            #100;
            a = 0;
            b = 1;
            #100;
            a = 1;
            b = 0;
            #100;
            a = 1;
            b = 1;
            #100;
        end
endmodule
```

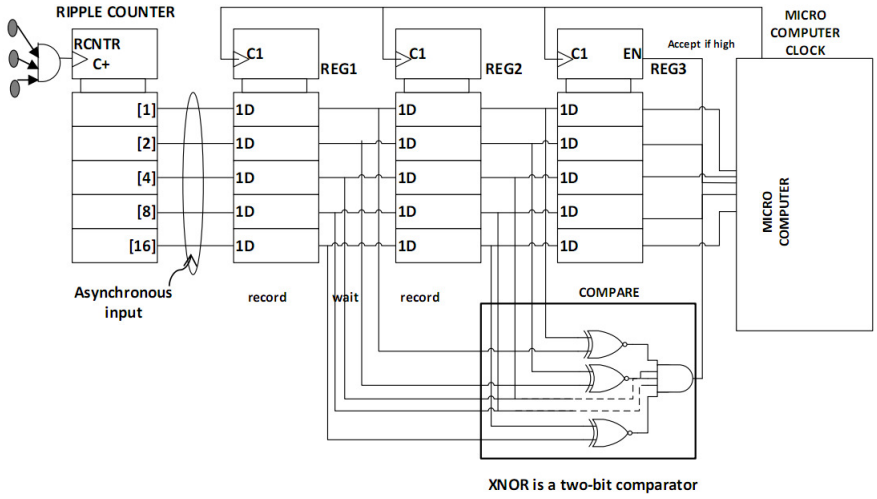
(a) 3 (b) 0 (c) 2 (d) 1

7. which circuit is the following timing diagram for?



(a) positive edge triggered D flip-flop
(b) transparent low D latch
(c) transparent high D latch
(d) negative edge triggered D flip-flop

8. For the coconut counter circuit with hardware debouncing shown below, how many micro computer clock cycles are required to provide new counter data to the inputs of the micro computer?



(a) 3 (b) 1 (c) 2 (d) 4

9. We use clock gating to:

   (a) decrease power consumption
   (b) decrease clock frequency
   (c) increase power consumption
   (d) increase clock frequency

10. The combination logic in SRAM based FPGAs is implemented using:

    (a) transmission gates
    (b) complex gates
    (c) NANDs, NORs and inverters
    (d) LUTs

11. What is common name for the circuit implemented by the following verilog code?

```
input [7:0] biti,
output bito;
    assign bito = ~^biti;
endmodule
```

    (a) LFSR
    (b) decoder
    (c) multiplexer
    (d) parity checker

12. An 8x1 element CMOS FPGA LUT uses 5 transistor latches, AND gates in its address decoder and NAND gates and inverters in the output mux. How many transistors will an 4x1 LUT require?

    (a) 208 (b) 202 (c) 90 (d) 458

13. The preferred reset signal is:

    (a) asynchronous apply, synchronous remove
    (b) synchronous apply, synchronous remove
    (c) synchronous apply, asynchronous remove
    (d) asynchronous apply, asynchronous remove

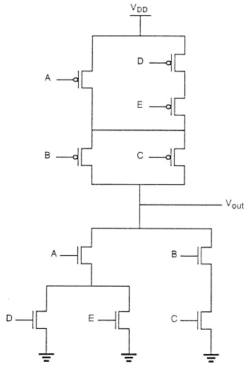
14. System Verilog uses random tests to:

    (a) increase simulation time
    (b) find stuck at faults
    (c) simplify the verification environment
    (d) find unexpected bugs

15. Verilog code of the from always@(negedge clk or posedge reset) would generate flip-flops with:

    (a) active high asynchronous reset
    (b) active low asynchronous reset
    (c) active low synchronous reset
    (d) active high synchronous reset

16. What is the logic function for Vout in the following CMOS circuit?



    (a) $\overline{(A * (D + E) + (B * C)}$
    (b) $\overline{A}$*($\overline{D}$+$\overline{E}$)+($\overline{B}$*$\overline{C}$)
    (c) $\overline{(A + (D * E) * (B + C)}$
    (d) A*(D+E)+(B*C)

17. A circuit that implemented the following truth tabled with input v[3:0] and output m[3:0] would be called a?

v[3:0]	m[3:0]
0000	0000
0001	0001
0010	0010
0011	0011
0100	0100
0101	0101
0110	0110
0111	0111
1000	1000
1001	1001
1010	0000
1011	0001
1100	0010
1101	0011
1110	0100
1111	0101

(a) grad code encoder
(b) priority encoder
(c) one hot encoder
(d) BCD encoder

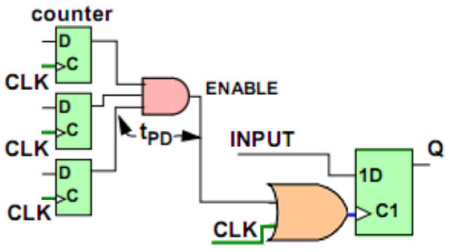
18. What percentage of design effort typically goes into verification?

(a) 40% (b) 50% (c) 60% (d) 70%

19. Which of the following is one of the most common sources of error in digital circuits?

(a) positional association
(b) hold time violations
(c) synchronous resets
(d) all of the above

20. For the following clock gating circuit with $T_{SETUP} = 20$ps, $T_{HOLD} = -10$ps, $T_{CHQV} = 20$ps and the clock frequency equal to 1GHz. The value of $T_{PD_{MIN}}$ for the AND gate that generates the enable signal will be?

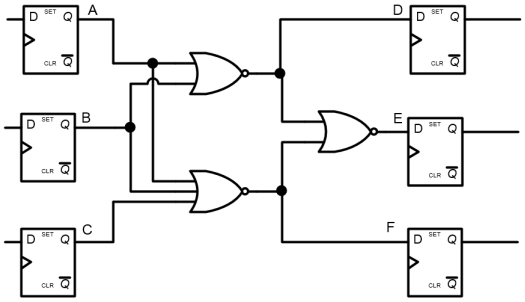


(a) 0ps (b) 480ps (c) 980ps (d) 30ps

21. We prefer to use an ASIC instead of an FPGA when:

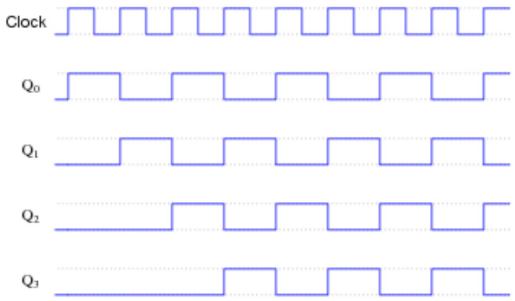
    (a) available design time is low
    (b) required power consumption is high
    (c) sales volumes are high
    (d) required operating frequency is low

22. For the sequential circuit below, if signals A,B and C are set to 0,0 and 0 respectively, how many stuck at faults (either 1 or 0) can be detected at nodes D,E and F, assuming you can only have one stuck at fault at any give time?



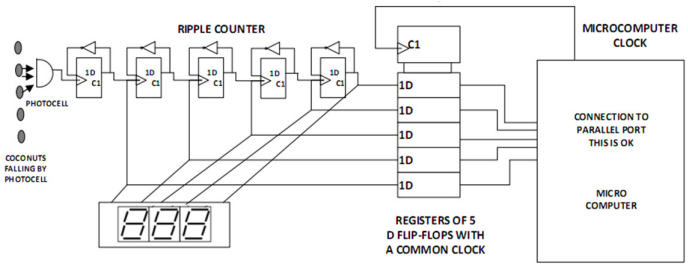
    (a) 3 (b) 1 (c) 2 (d) 4

23. What type of circuit with outputs Q[3:0] could give the following timing diagram?



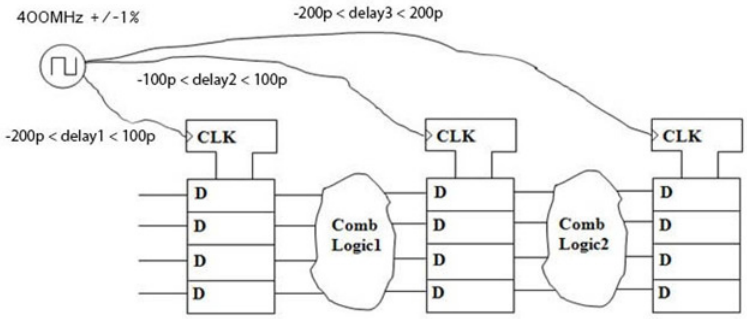
    (a) up counter
    (b) shift register
    (c) decoder
    (d) down counter

24. Why would replacing the ripple counter with a synchronous counter in the coconut counter circuit below make the multibit asynchrounous input signal capture problem worse?



(a) increased signal capture errors
(b) decreased signal capture errors
(c) decreased counter circuitry
(d) increased counter circuitry

25. For the following timing circuit with $T_{SETUP} = 20$ps, $T_{HOLD} = -10$ps and $T_{CHQV} = 20$ps. The clock is a spread spectrum clock with a nominal value of 400MHz plus or minus 1%. The value of $T_{PD_{MIN}}$ for combination logic2 will be?



(a) 270ps (b) 2135ps (c) 2160ps (d) 290ps

26. An asynchronous signal fed into a flip-flop will have a synchronous output if:

(a) $T_{CHQV} > T_{HOLD}$
(b) $T_{CHQV} < T_{HOLD}$
(c) $T_{SETUP} < T_{CHQV}$
(d) $T_{SETUP} > T_{CHQV}$

27. Negative clock skew will:

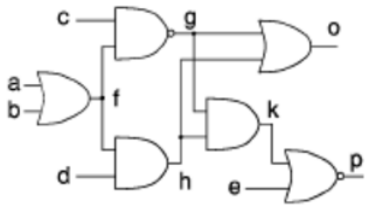
(a) increases $T_{PD_{MAX}}$ and increases $T_{PD_{MIN}}$
(b) decreases $T_{PD_{MAX}}$ and decreases $T_{PD_{MIN}}$
(c) decreases $T_{PD_{MAX}}$ and increases $T_{PD_{MIN}}$
(d) increases $T_{PD_{MAX}}$ and decreases $T_{PD_{MIN}}$

28. How many errors does the following verilog module code have?

```
module counter (out,enable,clk,reset);
input enable, clk, reset;
output [7:0] out;
wire enable, clk, reset;
always @(posedge clk)
    if (!reset) begin
        out = 8'b0 ;
    end else if (enable) begin
        out <= out + 1;
    end
endmodule
```

(a) 2 (b) 1 (c) 0 (d) 3

29. The following circuit is to be implemented using an FPGA that uses 16x1 element LUTs. What is the minimum number of LUTs required to implement the circuit?



(a) 5 (b) 4 (c) 3 (d) 2

30. What is common name for the circuit implemented by the following verilog code?

```
input a, b, c;
output [3:0] out;
wire [3:0] out;
reg [3:0] iout;
always @ (posedge a) begin
  if (b)
      iout <= 0;
  else if (c)
      iout <= iout + 1;
  end
assign out = { iout[3], (iout[3] ^ iout[2]),
              (iout[2] ^ iout[1]),(iout[1] ^ iout[0]) };
```

(a) LFSR
(b) one hot counter
(c) priority encoder
(d) gray code counter

Instructions:

- You finished the exam!
- Upload your answer spreadsheet.