



USB 3.1 Design Guide

Simulations by Tristan Huang

Supervisor: Daniel Wei

2015/12



Version

- **Version 1.0 (2014/11)**
- **Version 1.1 (2015/2)**
 - Add GND/Reference Void for Type-C
 - GND/Reference Void for ESD
 - GND/Reference Void for Chock
- **Version 1.2 (2015/12)**
 - Add GND/Reference Void for Capacitors (Case 2)
 - GND/Reference Void for Resistors
 - GND/Reference Void for ESD (Case 4 & Case 5)



Outline

- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
- GND/Reference Void for Chock
- GND/Reference Void for Resistors
- Balanced GND vias Vs. Unbalanced GND vias
- Distance from GND via to Signal via
- Routing: Arc Vs. 135-degree-angle



Outline

- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
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Stack up (based on ASM EV/demo boards)

L1	TOP	copper+plating	1.58 mils
		Prepreg	3.50 mils
L2		copper	1.30 mils
		core	48.40 mils
L3		copper	1.30 mils
		Prepreg	3.50 mils
L4	BOT	copper+plating	1.58 mils

4 layer

$$\epsilon_r = 4.3$$

$$\tan D = 0.02$$

L1	TOP	copper+plating	1.58 mils
		Prepreg	3.50 mils
L2	GND	copper	1.30 mils
		core	4.00 mils
L3	IN1	copper	1.30 mils
		Prepreg+core	38.00 mils
L4	IN2	copper	1.30 mils
		core	4.00 mils
L5	VCC	copper	1.30 mils
		Prepreg	3.50 mils
L6	Bottom	copper+plating	1.58 mils

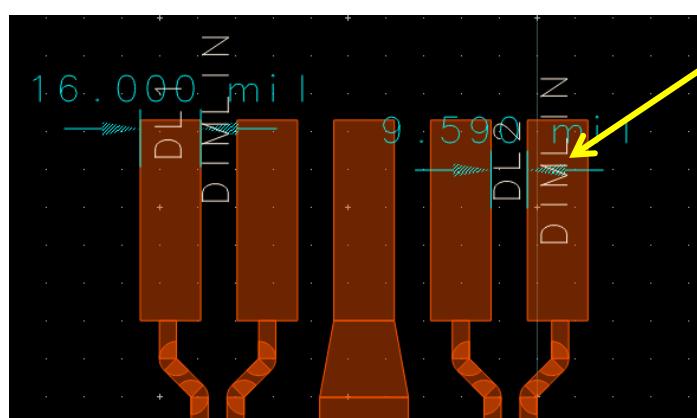
6 layer



Outline

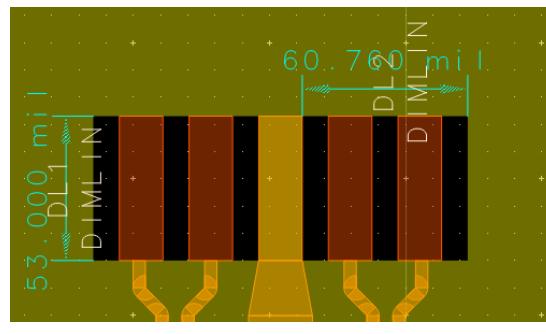
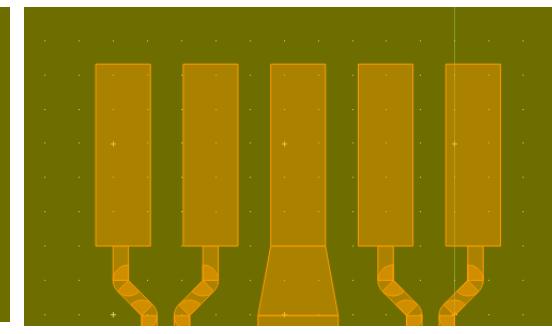
- Stack up (based on ASM EV/demo boards)
- **GND/Reference Void for Micro-B**
- **GND/Reference Void for Capacitors**
- **GND/Reference Void for Differential vias**
- **GND/Reference Void for Type-C**
- **GND/Reference Void for ESD**
- **GND/Reference Void for Chock**
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- **Balanced GND vias Vs. Unbalanced GND vias**
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- **Routing: Arc Vs. 135-degree-angle**

GND/Reference Void for Micro-B



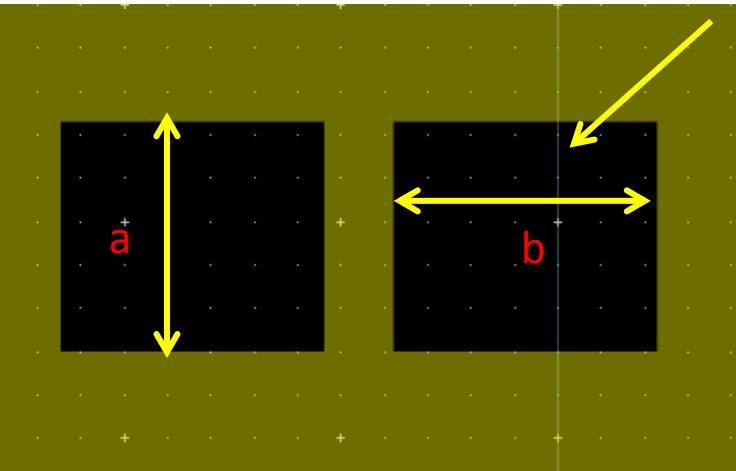
Layer 1

pad

Optimized void
(SI suggest)

No void

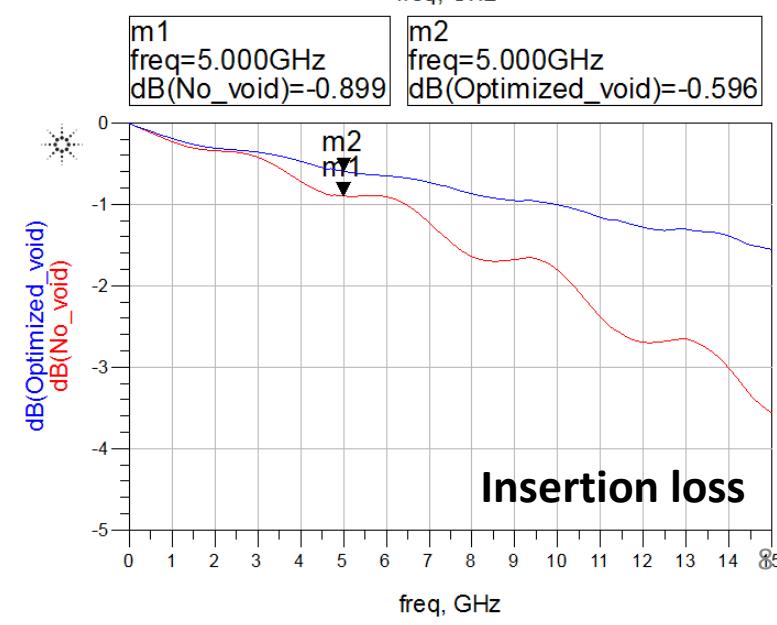
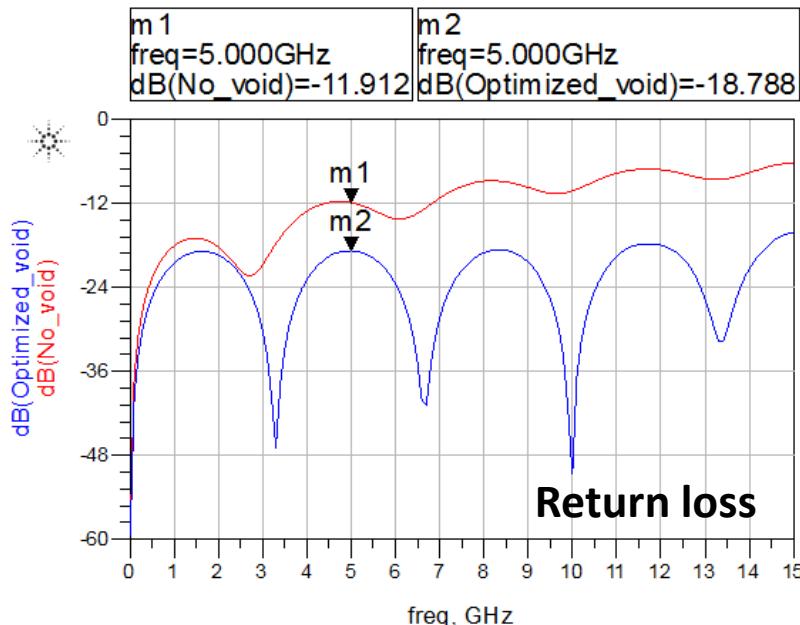
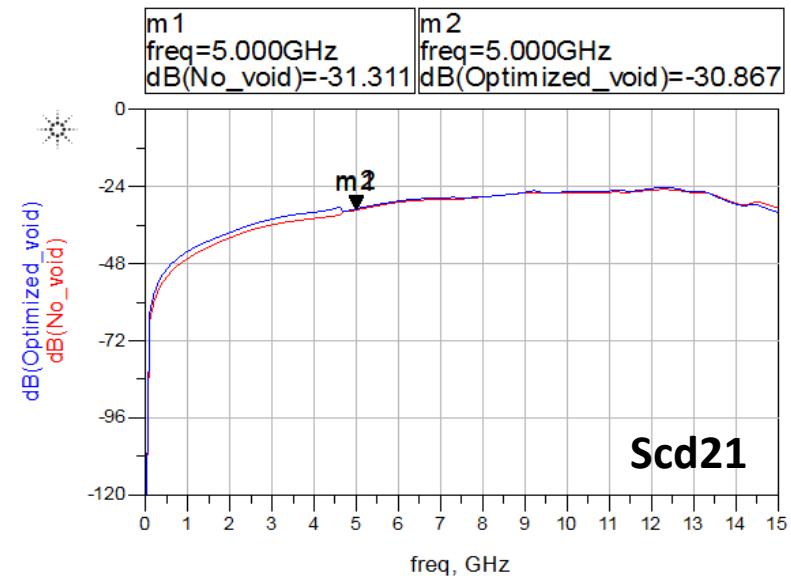
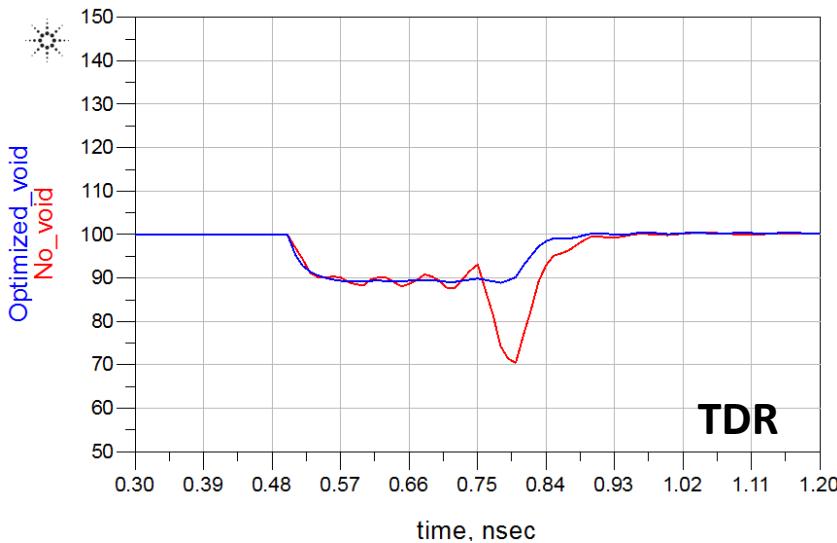
void



Layer 2

	Optimized void	No void
a	53 mil	0 mil
b	60.76 mil	0 mil

GND/Reference Void for Micro-B

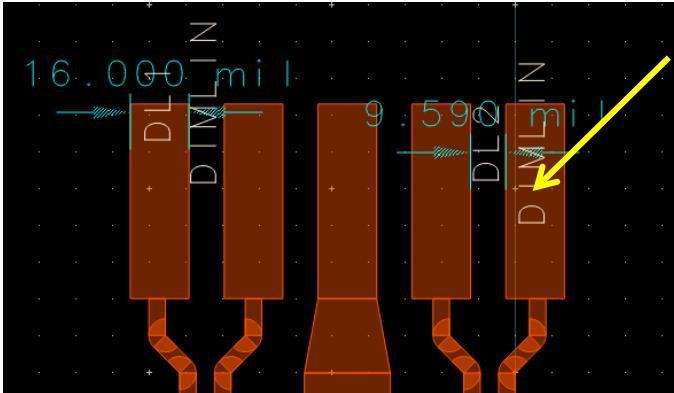


GND/Reference Void for Micro-B

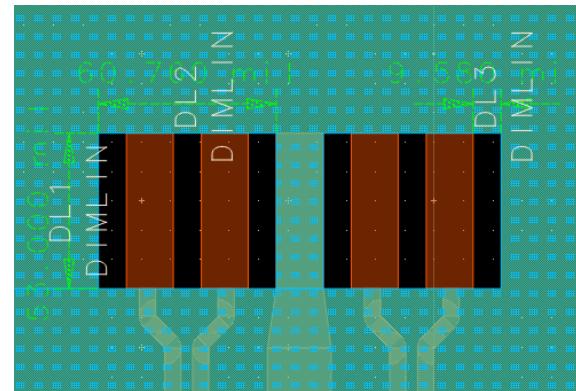
Summary:

For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

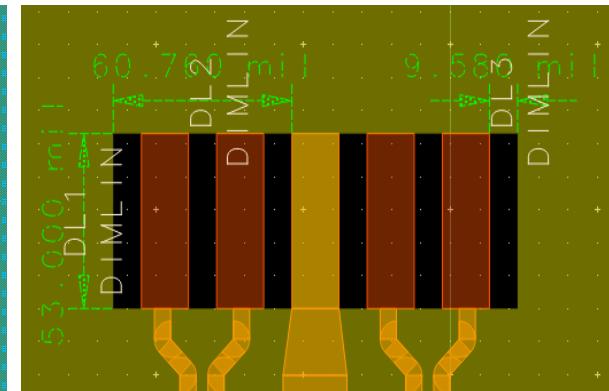
GND/Reference Void for Micro-B



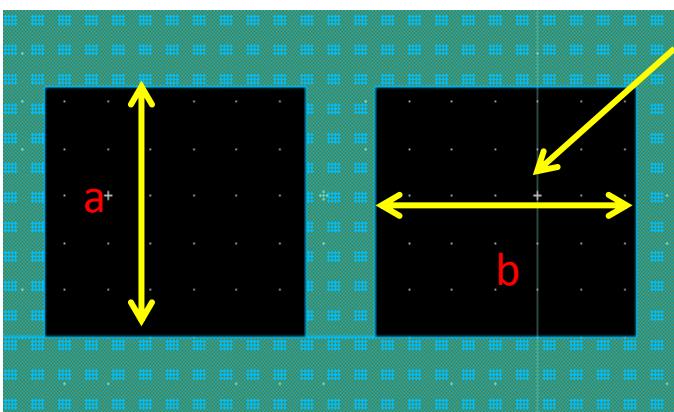
pad



**Layer 2 & 3 void
(SI suggest)**



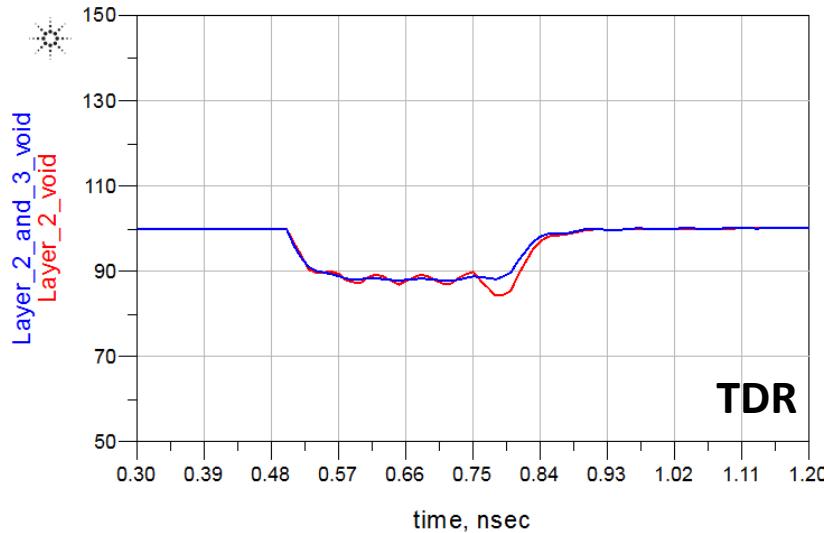
Layer 2 void



void

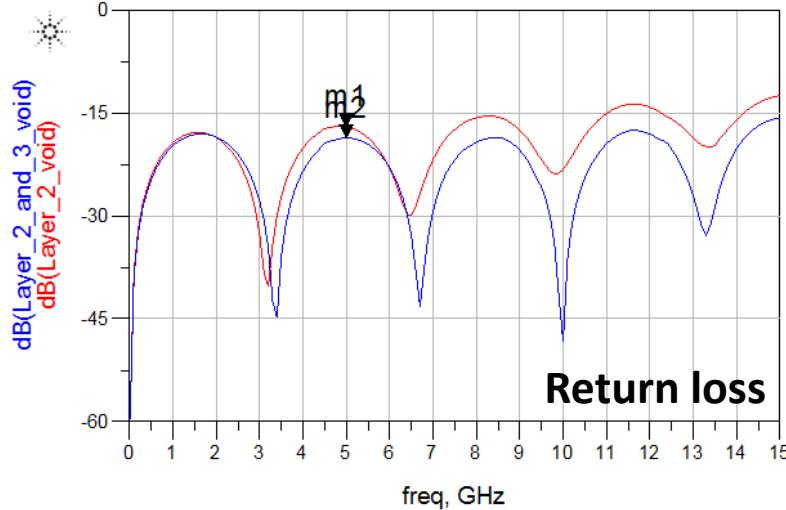
	Layer 2 & 3 void	Layer 2 void
a	53 mil	53 mil
b	60.76 mil	60.76 mil

GND/Reference Void for Micro-B

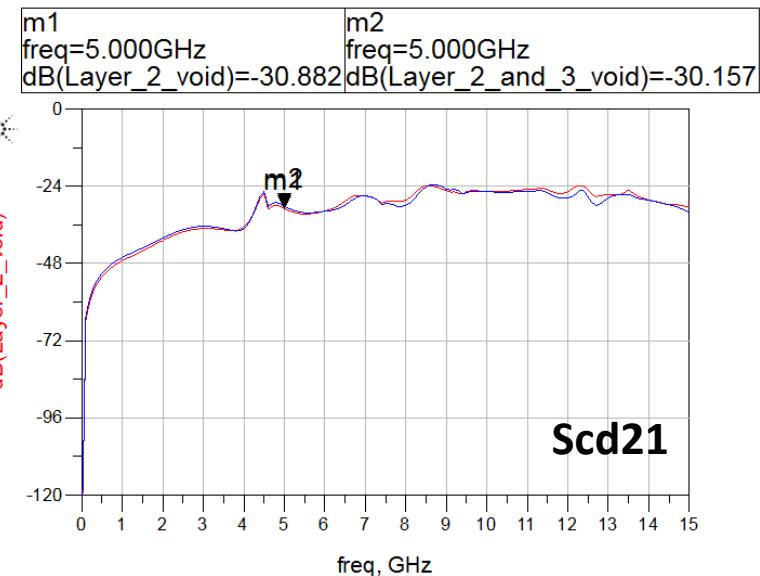


m1
freq=5.000GHz
dB(Layer_2_void)=-17.044

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-18.669



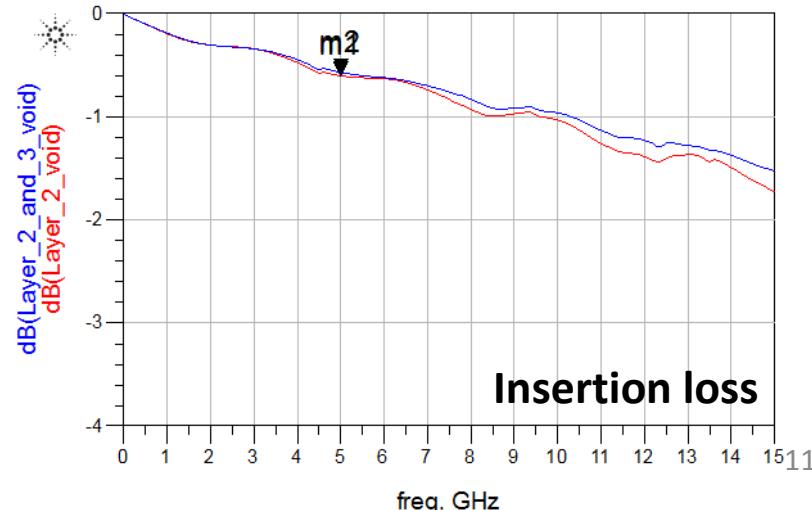
Return loss



Scd21

m1
freq=5.000GHz
dB(Layer_2_void)=-0.605

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-0.571



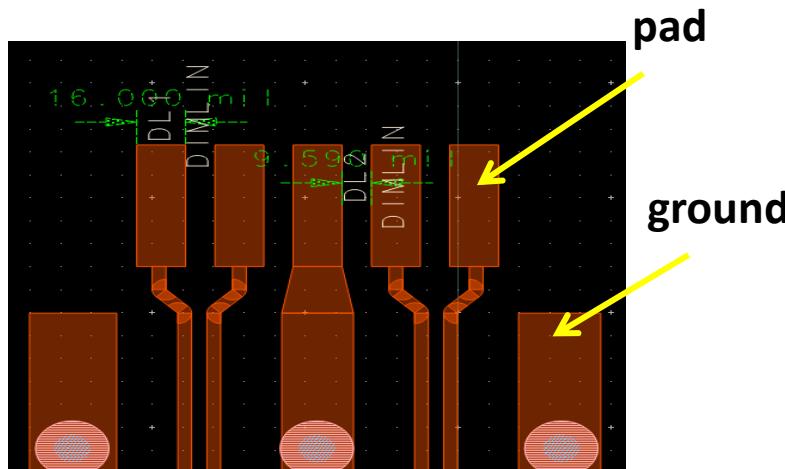
Insertion loss

GND/Reference Void for Micro-B

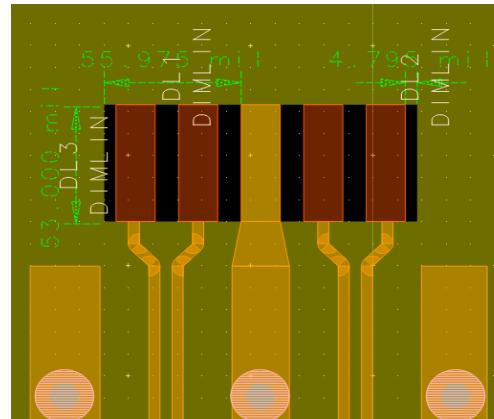
Summary:

For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.

GND/Reference Void for Micro-B

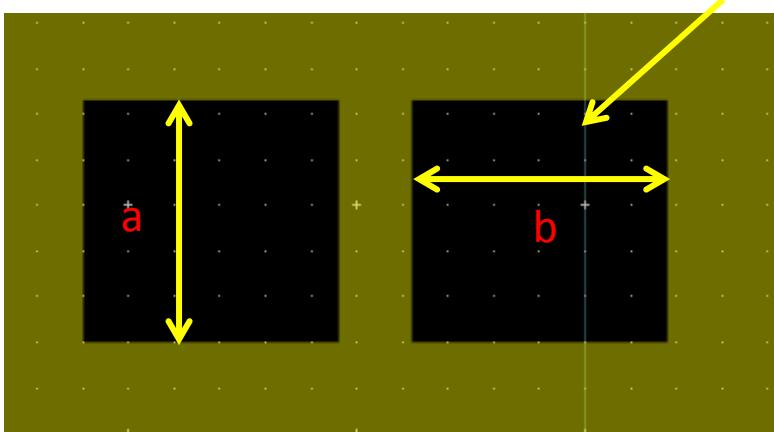


Layer 1



No void

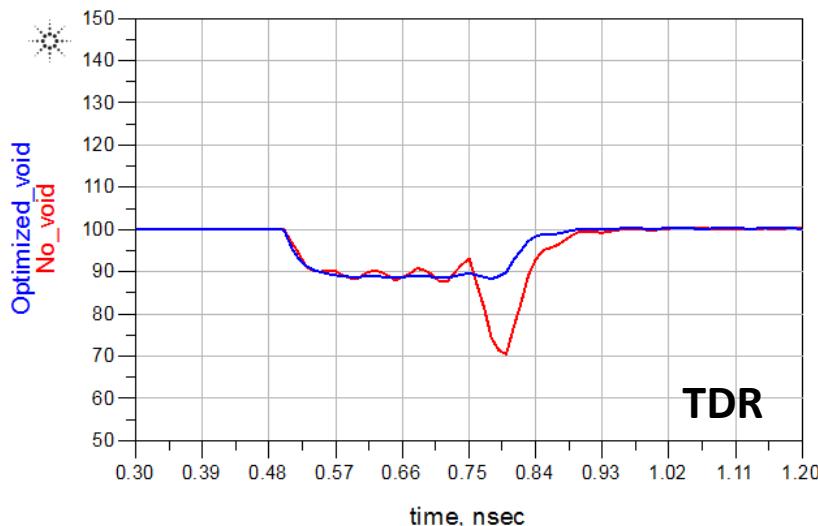
void



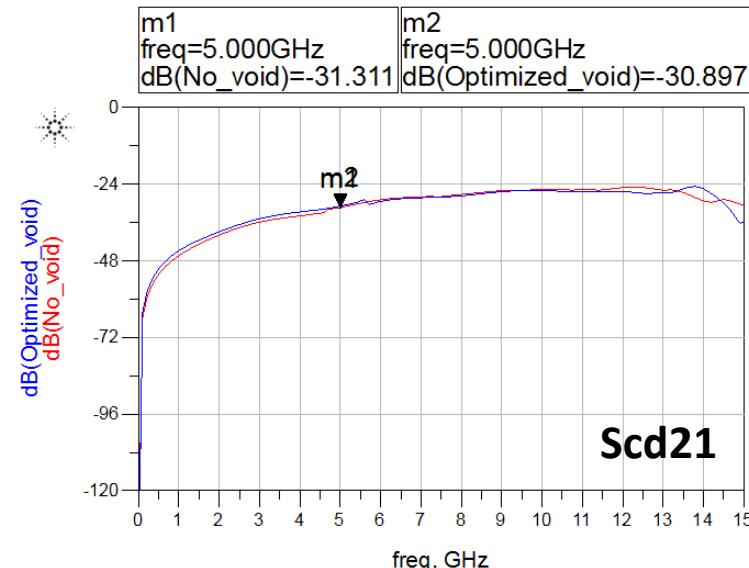
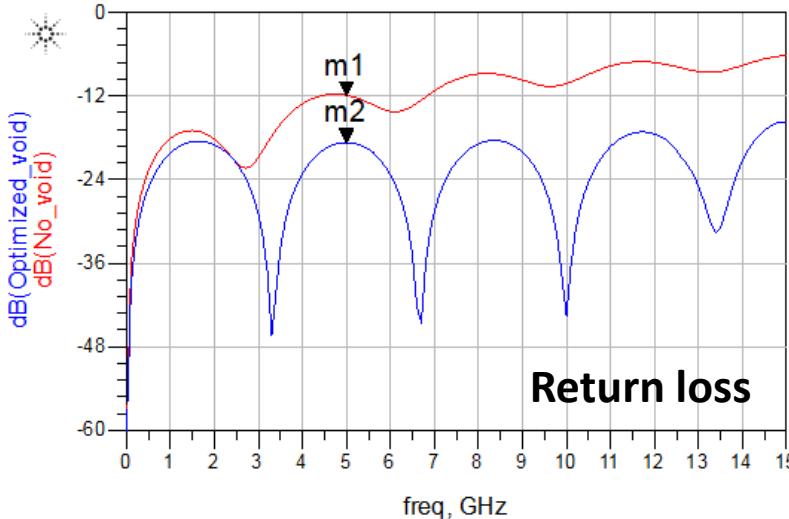
Layer 2

	Optimized void	No void
a	53 mil	0 mil
b	55.975 mil	0 mil

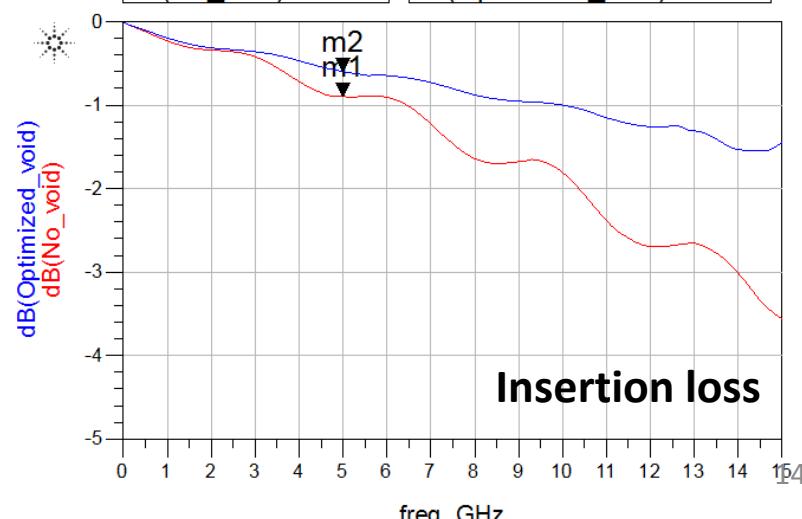
GND/Reference Void for Micro-B



m1 freq=5.000GHz dB(No_void)=-11.912	m2 freq=5.000GHz dB(Optimized_void)=-18.688
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m1 freq=5.000GHz dB(No_void)=-0.899	m2 freq=5.000GHz dB(Optimized_void)=-0.600
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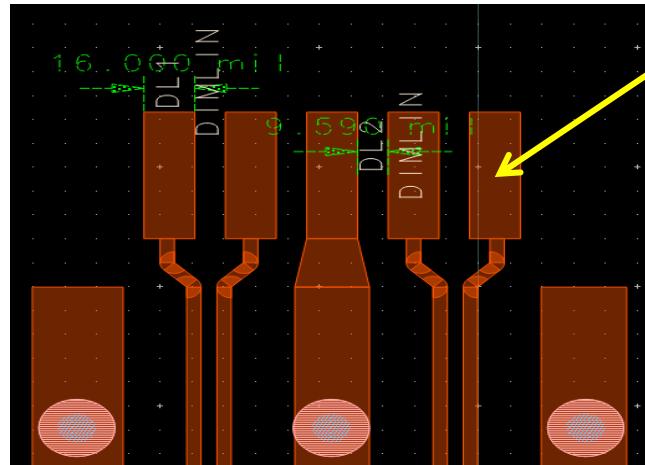


GND/Reference Void for Micro-B

Summary:

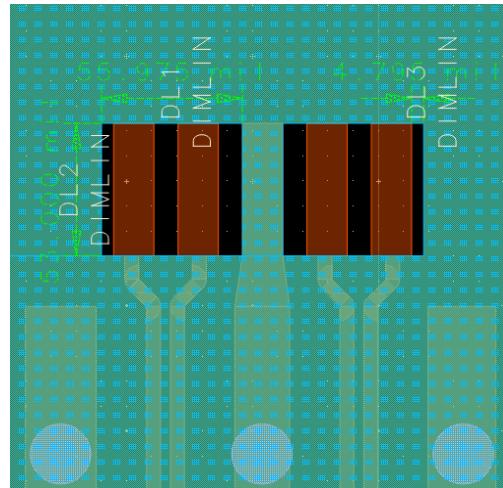
For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

GND/Reference Void for Micro-B

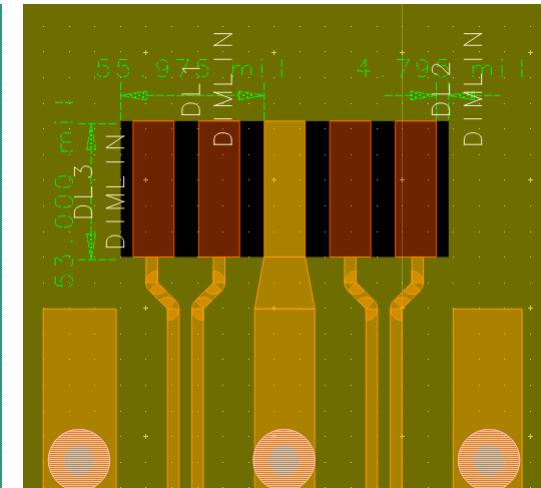


Layer 1

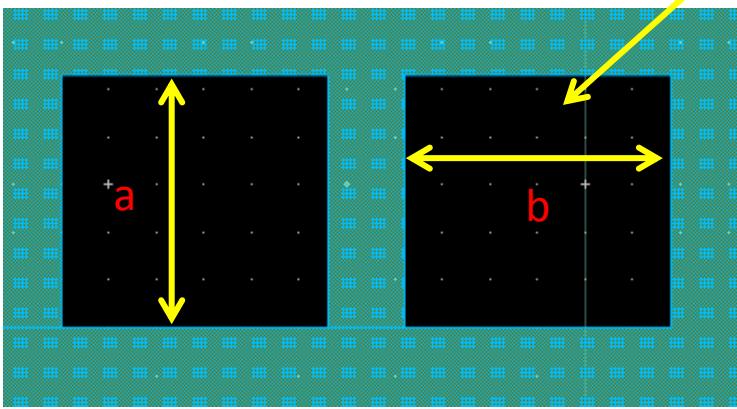
pad

Layer 2 & 3 void
(SI suggest)

void



Layer 2 void



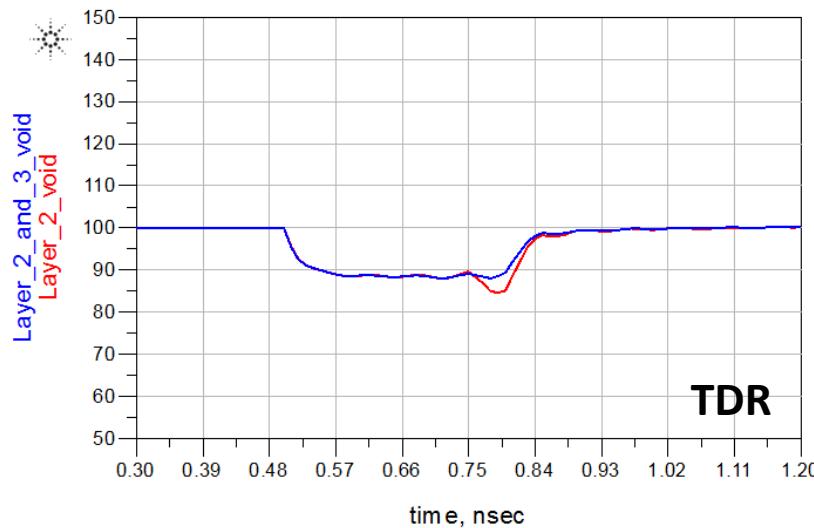
Layer 2 & 3

a

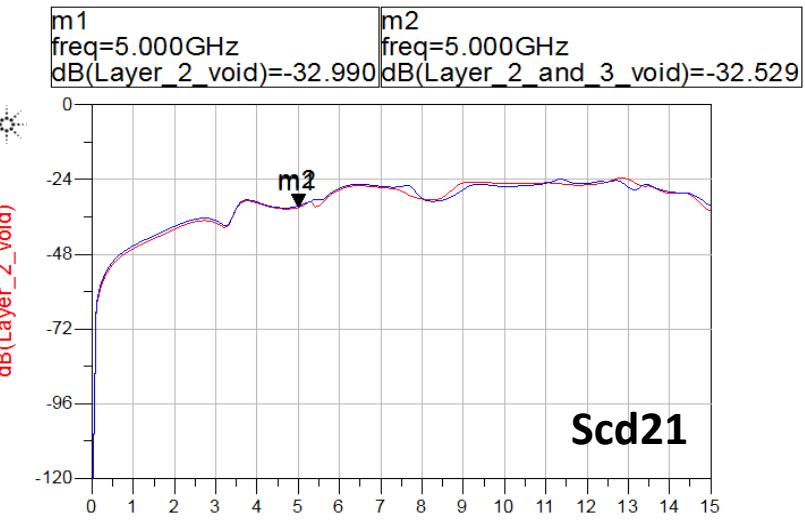
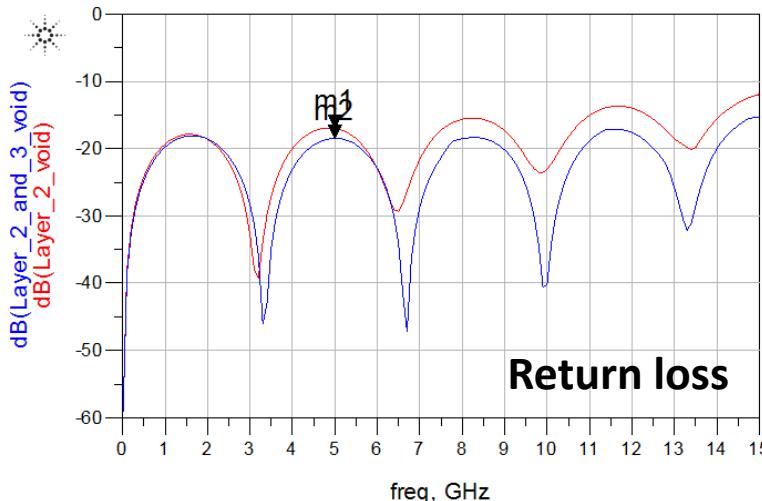
b

	Layer 2 & 3 void	Layer 2 void
a	53 mil	53 mil
B	55.975 mil	55.975 mil

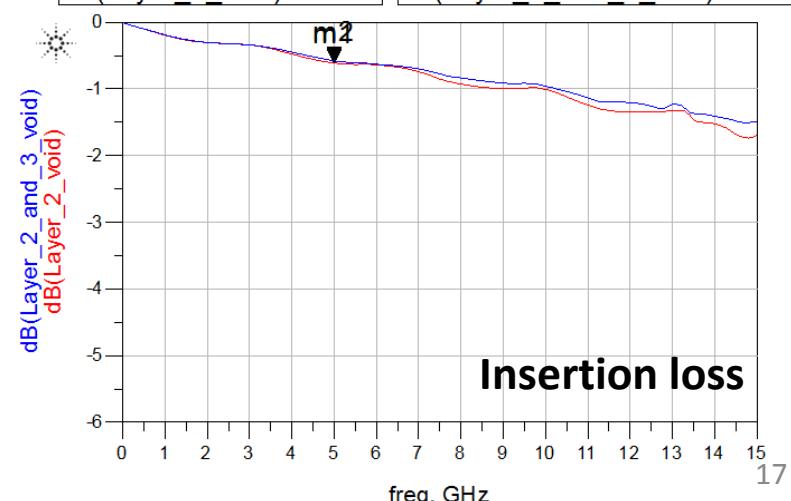
GND/Reference Void for Micro-B



m1 freq=5.000GHz dB(Layer_2_void)=-17.000	m2 freq=5.000GHz dB(Layer_2_and_3_void)=-18.484
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m1 freq=5.000GHz dB(Layer_2_void)=-0.612	m2 freq=5.000GHz dB(Layer_2_and_3_void)=-0.579
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GND/Reference Void for Micro-B

Summary:

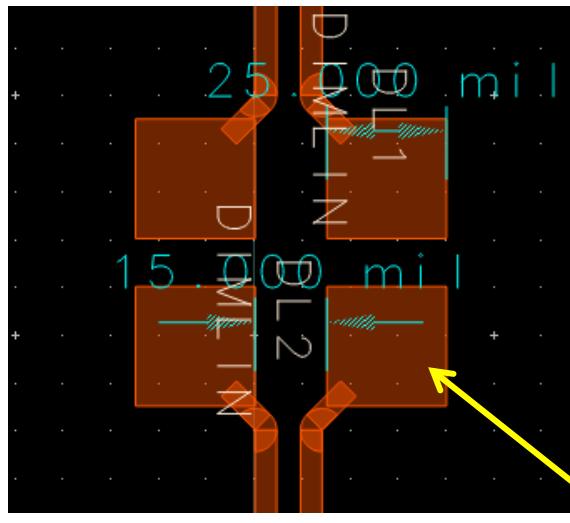
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.



Outline

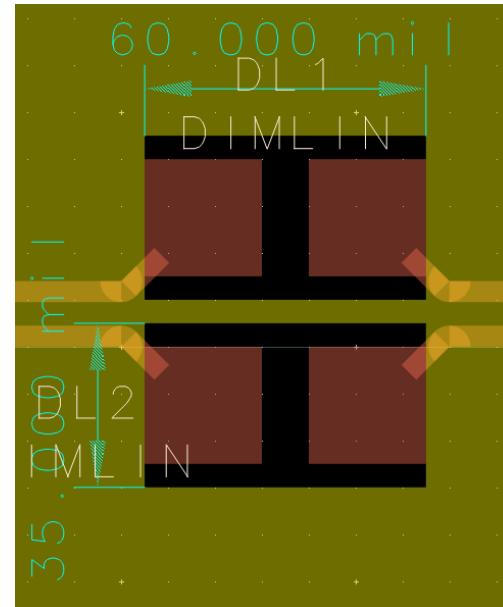
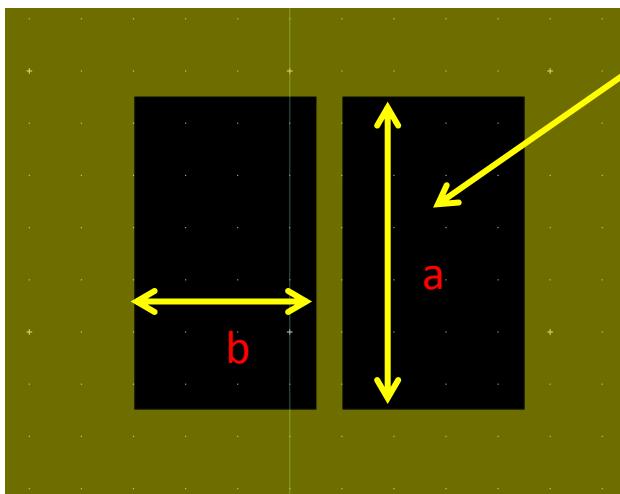
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GND/Reference Void for Capacitors

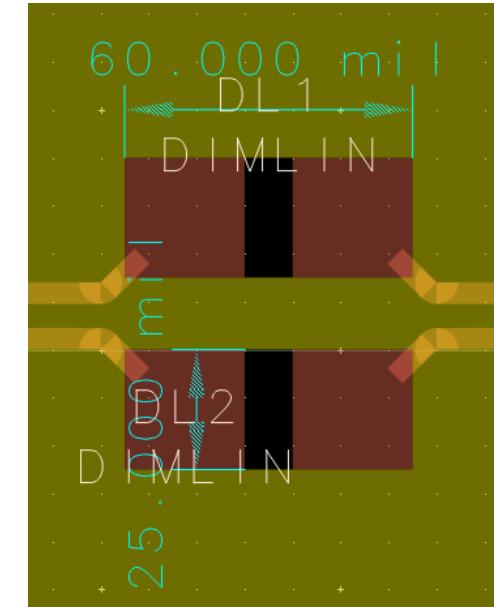


pad

void



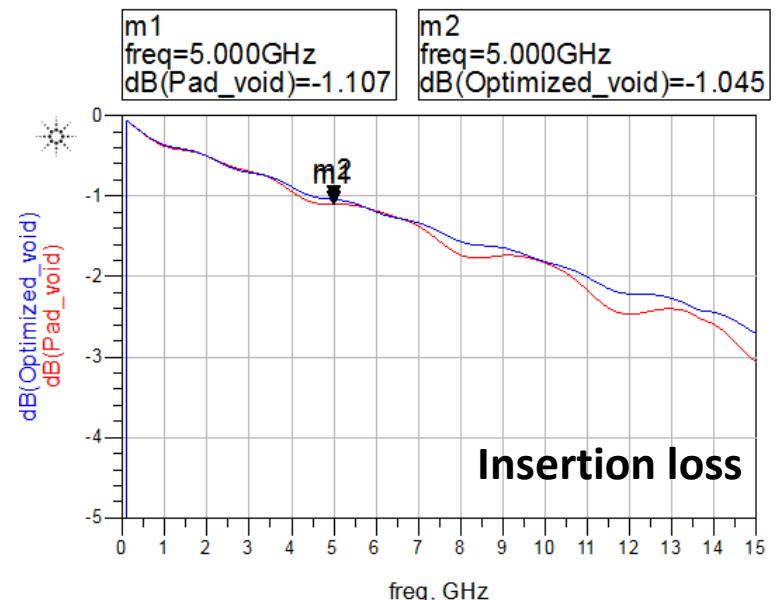
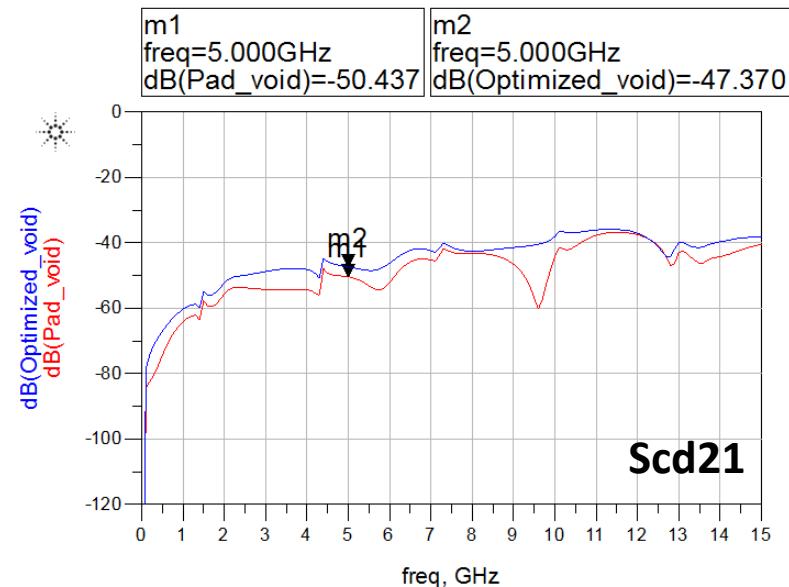
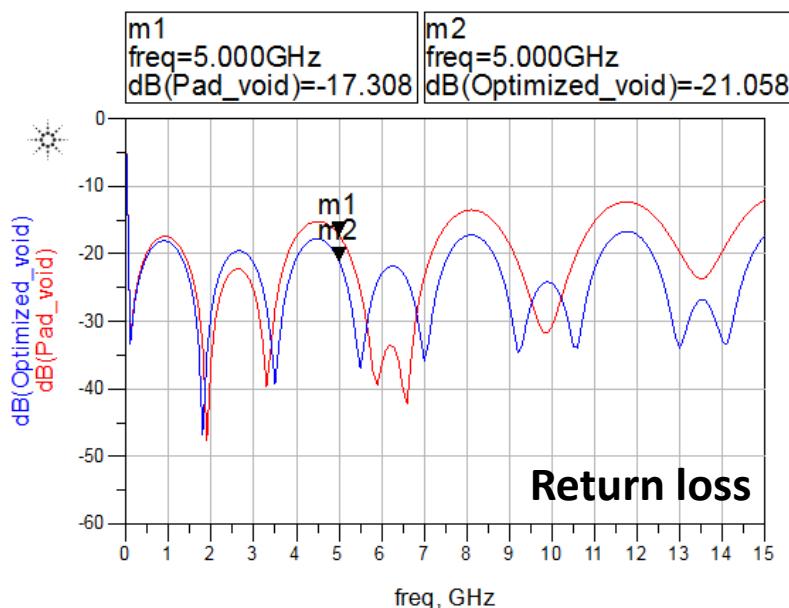
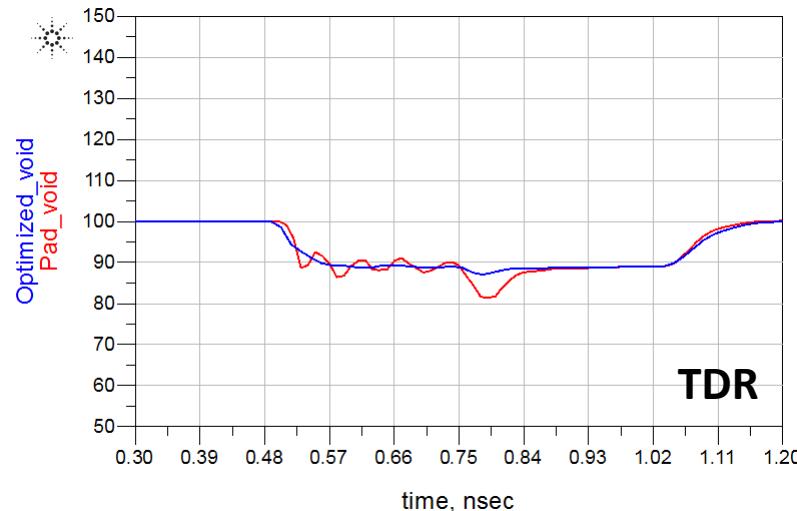
**Optimized void
(SI suggest)**



Pad void

	Optimized void	Pad void
a	60 mil (0402)	60 mil (0402)
b	35 mil	25 mil

GND/Reference Void for Capacitors

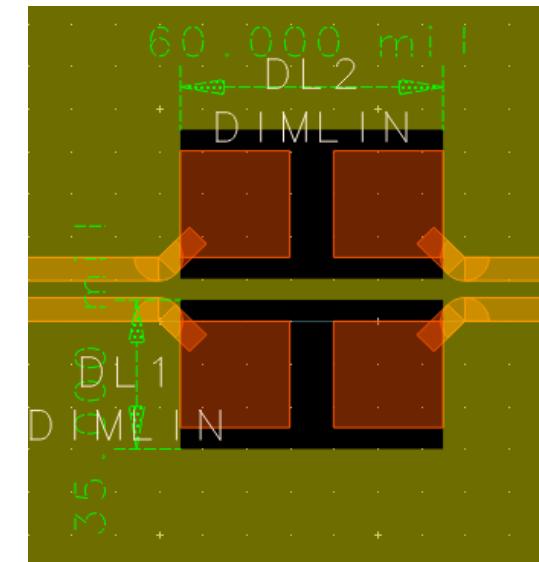
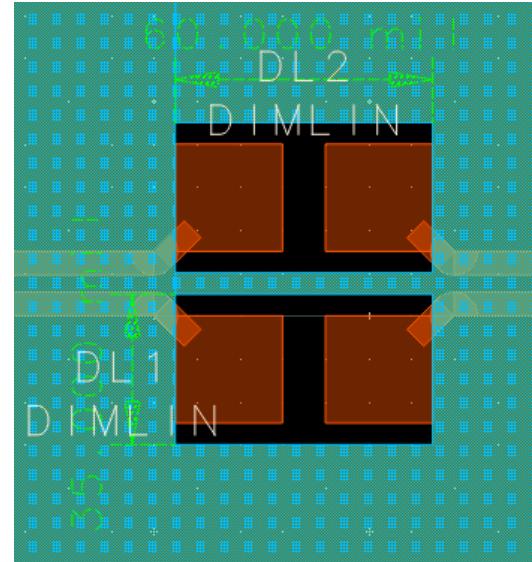
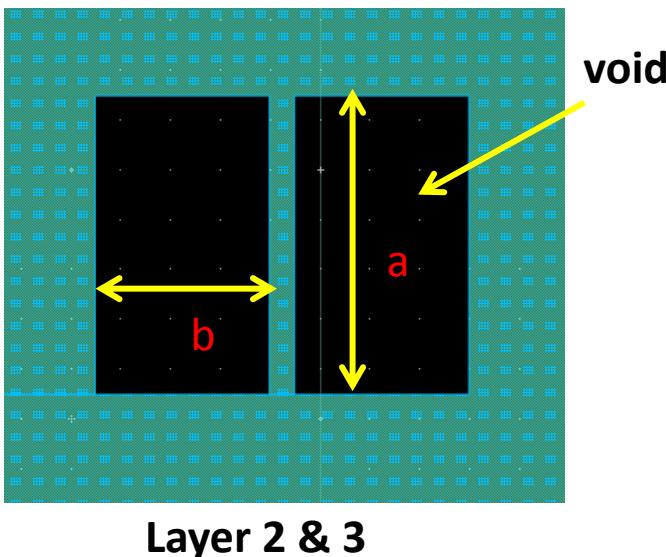
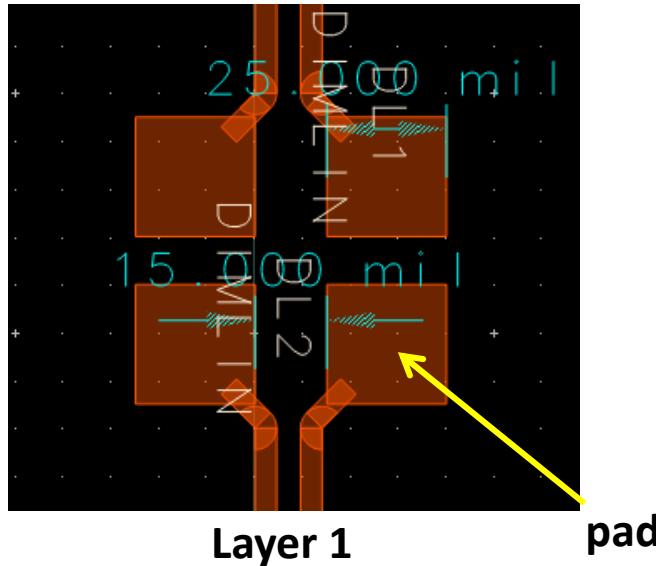


GND/Reference Void for Capacitors

Summary:

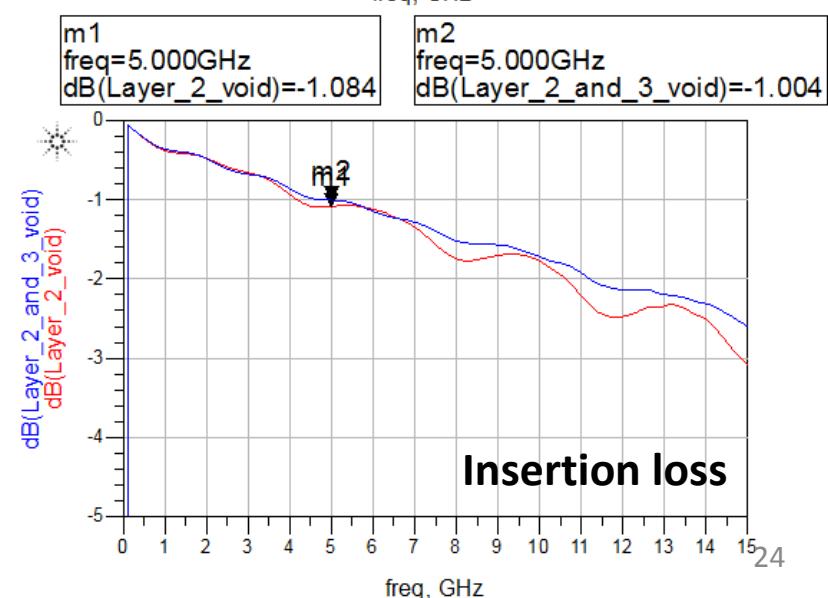
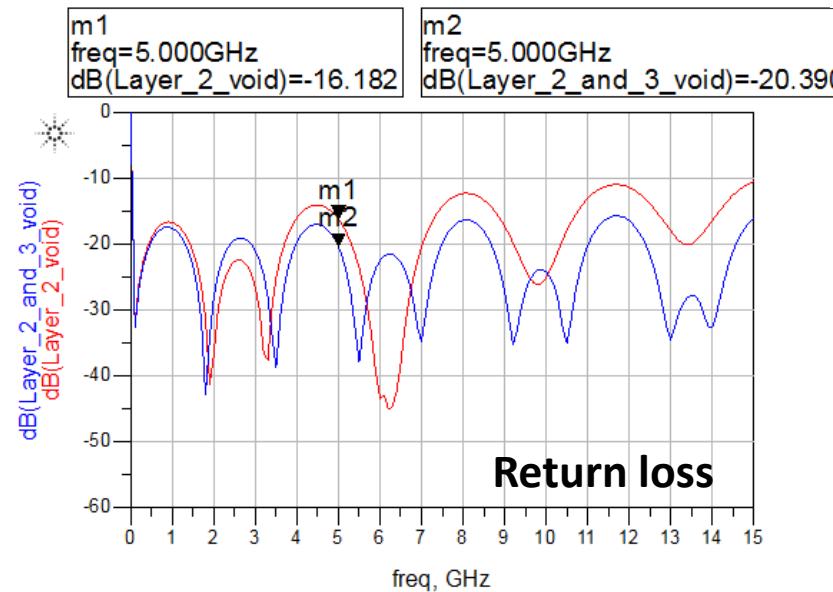
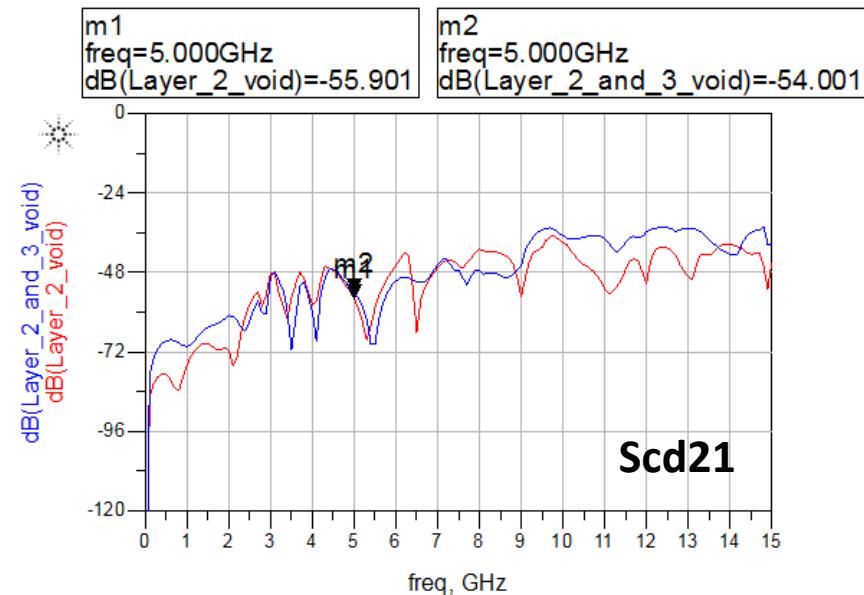
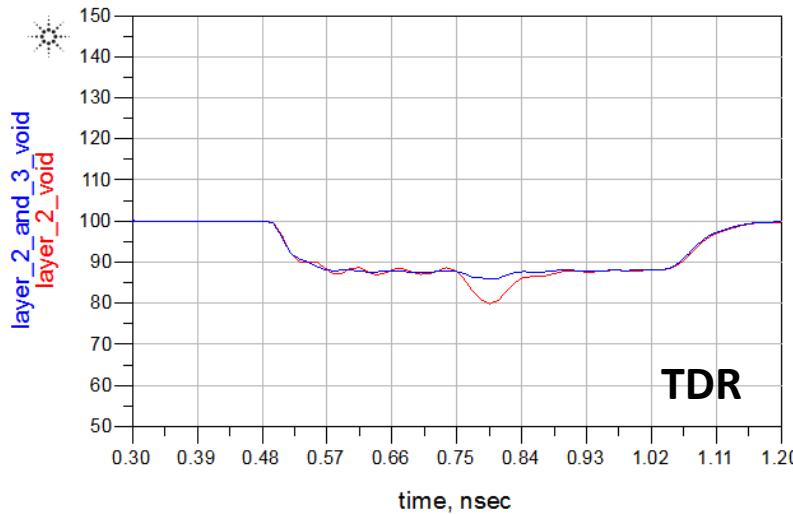
For 4 layers board, **SI-suggested void** is better than **Pad void** in frequency and time domain.

GND/Reference Void for Capacitors



	Layer 2 & 3 void	Layer 2 void
a	60 mil (0402)	60 mil (0402)
b	35 mil	35 mil

GND/Reference Void for Capacitors

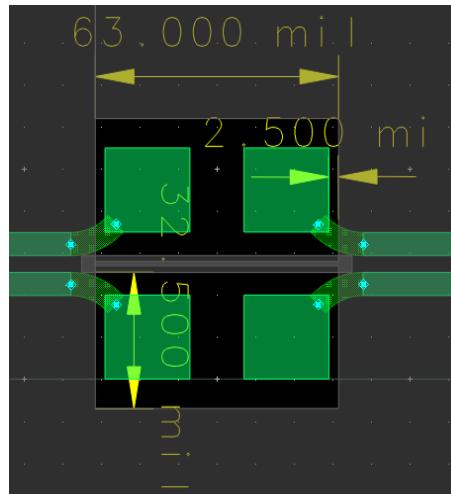
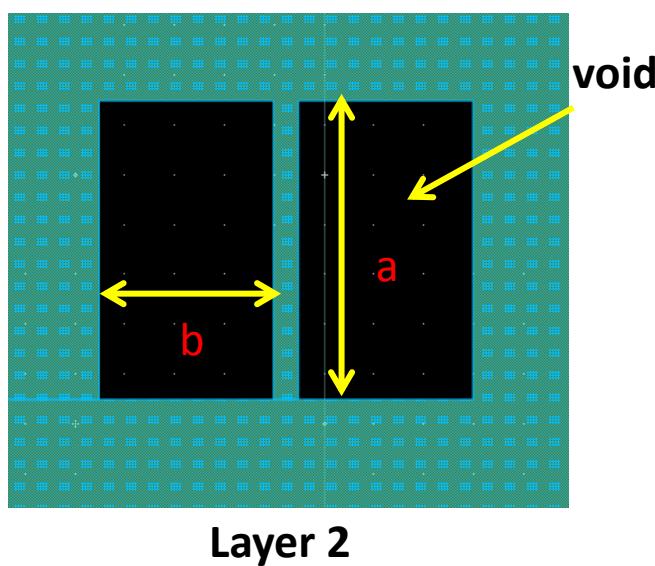
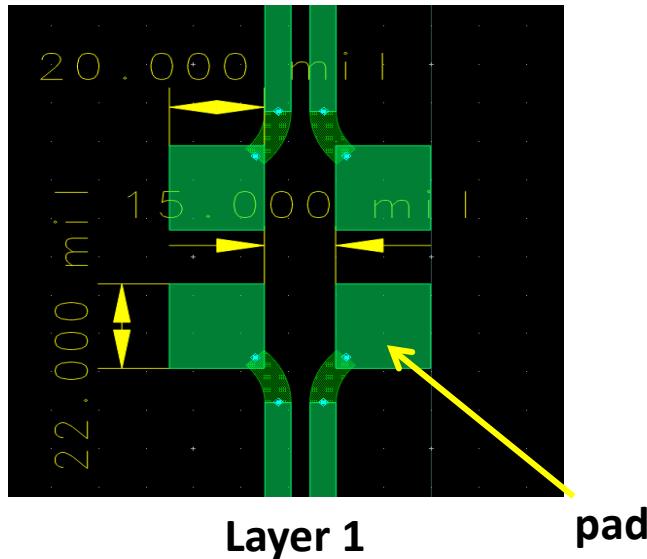


GND/Reference Void for Capacitors

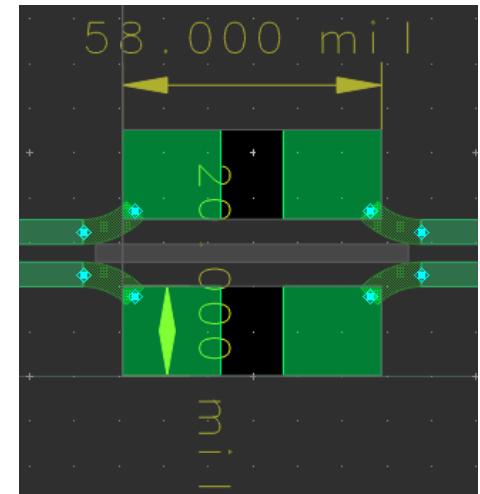
Summary:

For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.

GND/Reference Void for Capacitors



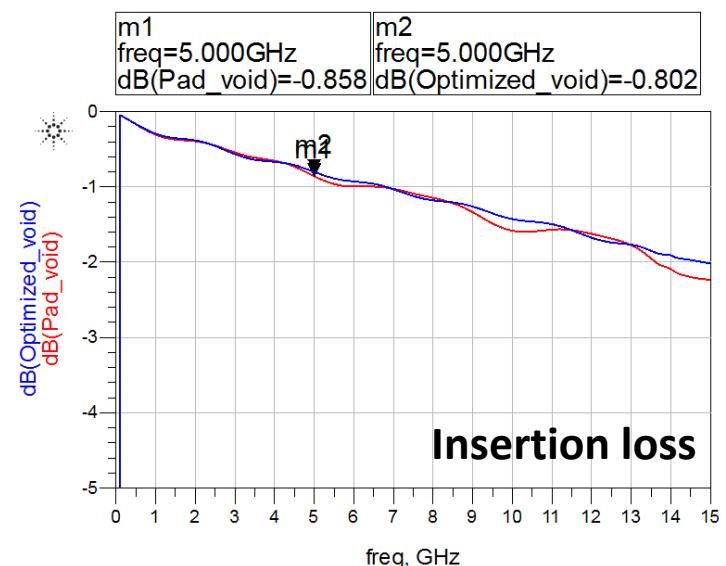
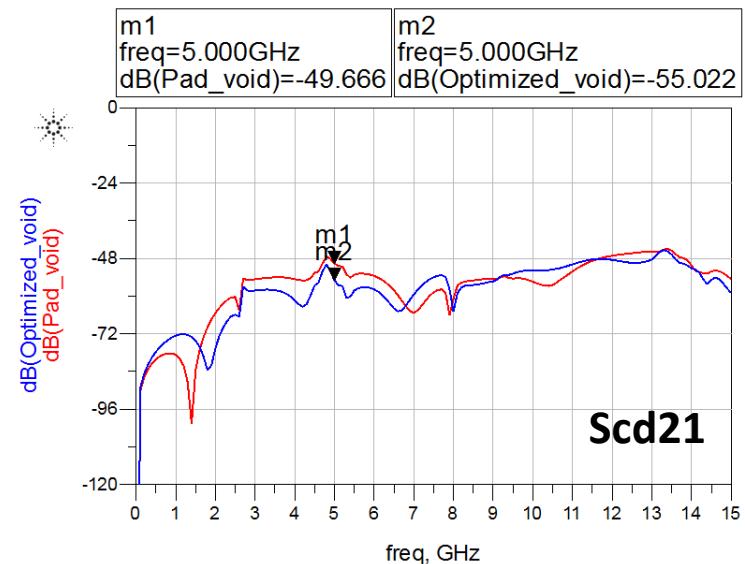
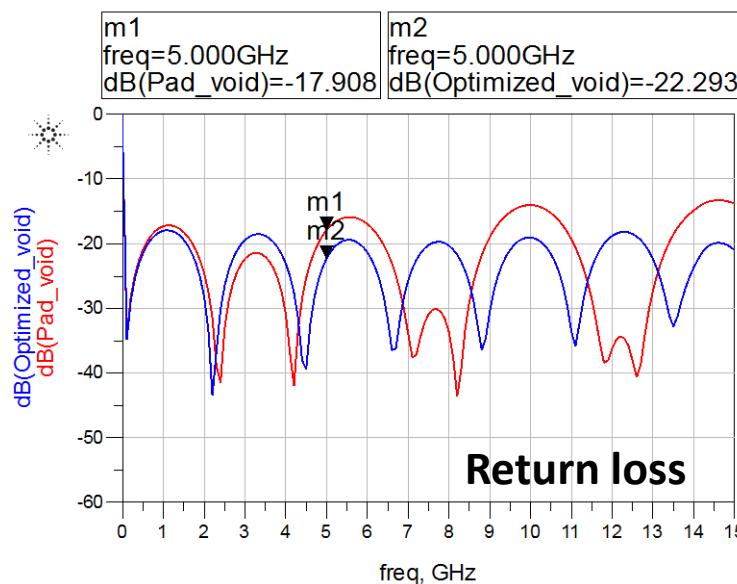
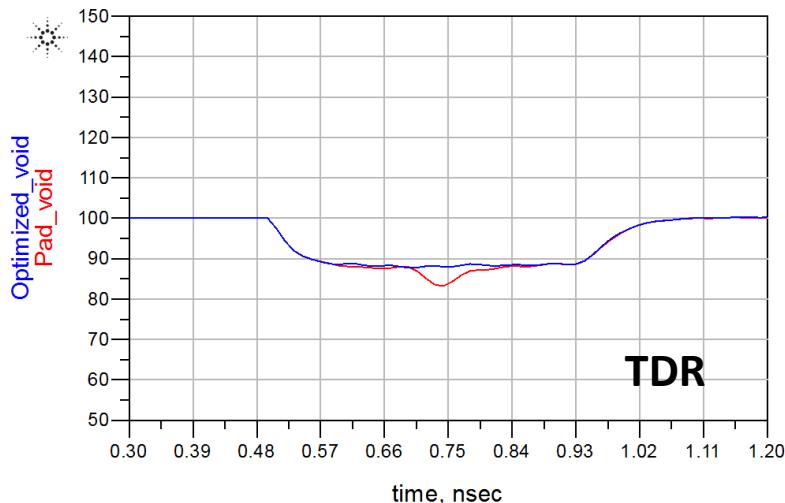
**Optimized void
(SI suggest)**



Pad void

	Optimized void	Pad void
a	63 mil (0402)	58 mil (0402)
b	32.5 mil	20 mil

GND/Reference Void for Capacitors

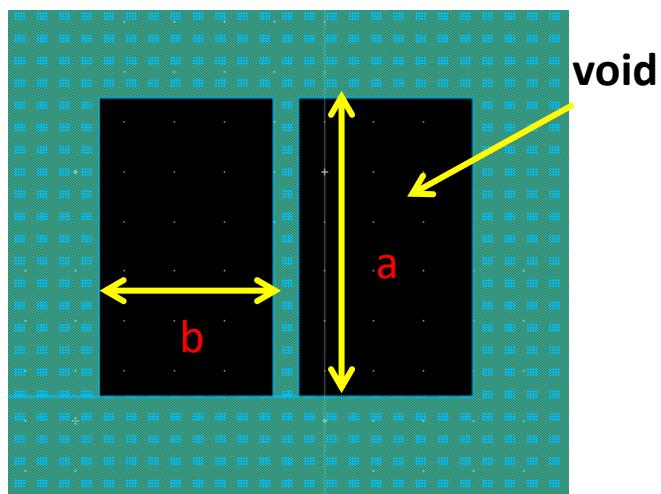
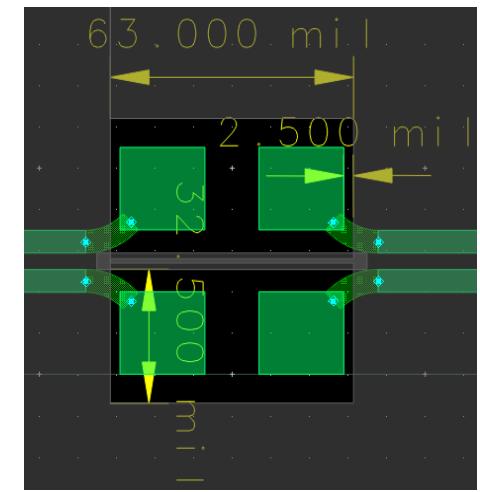
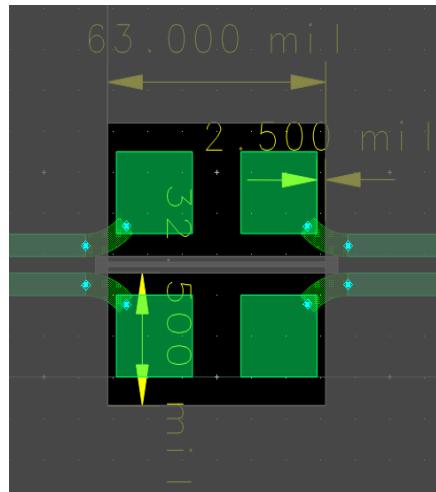
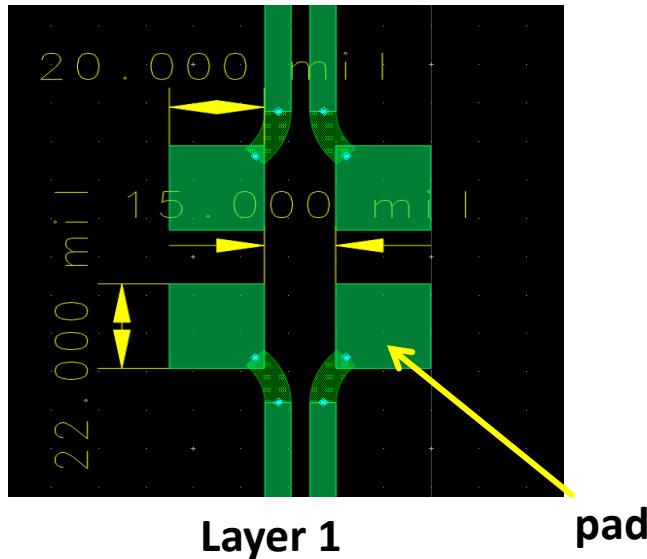


GND/Reference Void for Capacitors

Summary:

For 4 layers board, **SI-suggested void** is better than **Pad void** in frequency and time domain.

GND/Reference Void for Capacitors

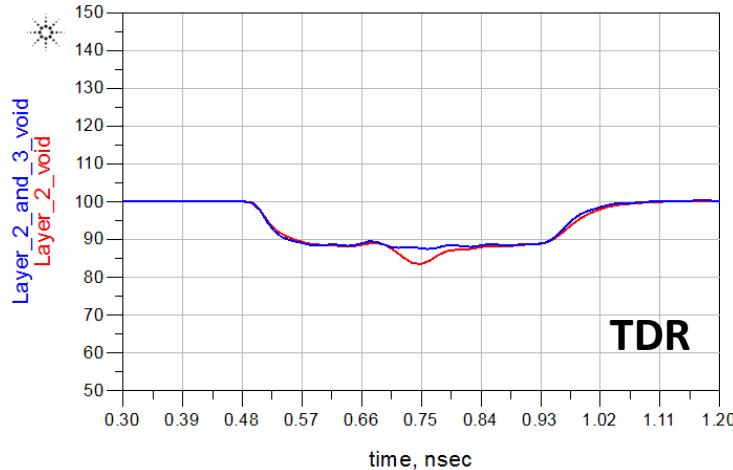


**Layer 2 & 3 void
(SI suggest)**

Layer 2 void

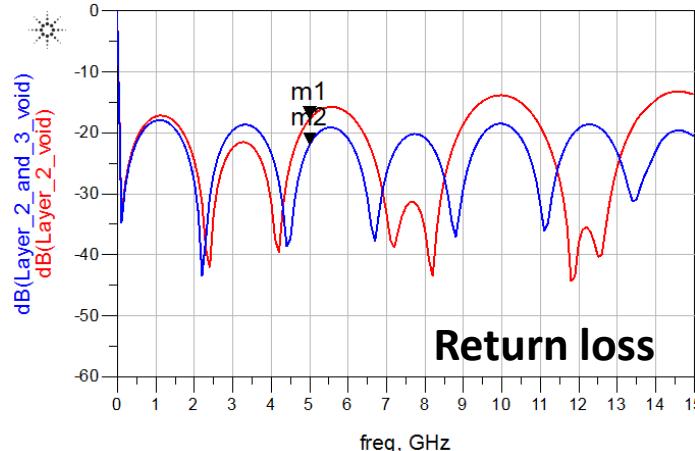
	Layer 2 & 3 void	Layer 2 void
a	63 mil (0402)	63 mil (0402)
b	32.5 mil	32.5 mil

GND/Reference Void for Capacitors



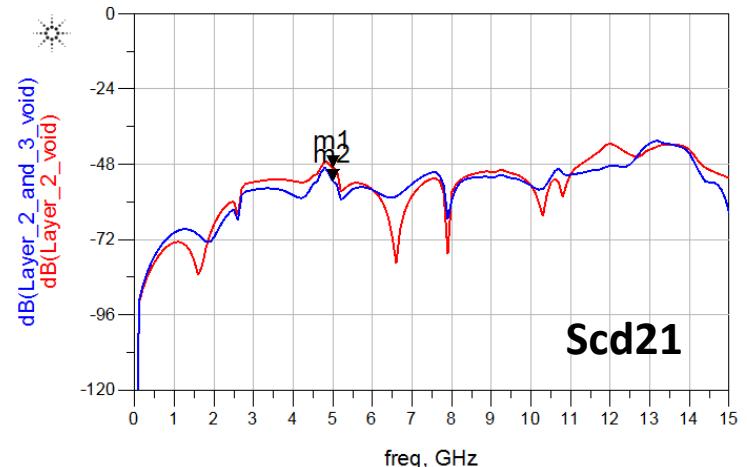
m1
freq=5.000GHz
dB(Layer_2_void)=-49.110

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-53.459



m1
freq=5.000GHz
dB(Layer_2_void)=-49.110

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-53.459



m1
freq=5.000GHz
dB(Layer_2_void)=-0.861

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-0.804



GND/Reference Void for Capacitors

Summary:

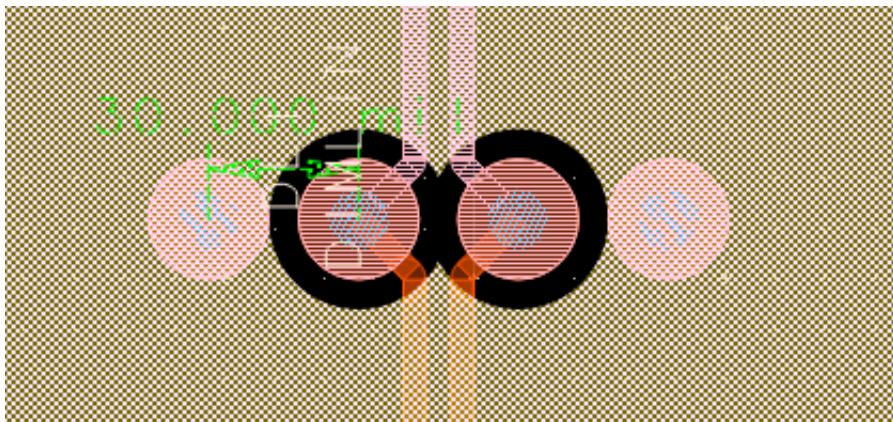
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.



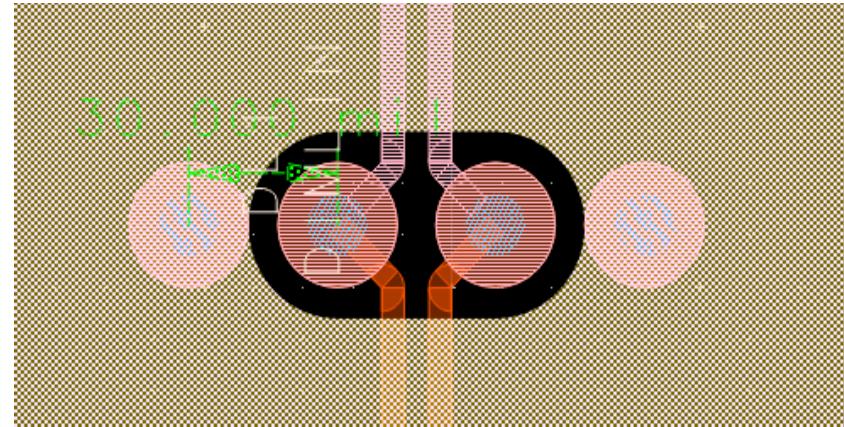
Outline

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- GND/Reference Void for Capacitors
- **GND/Reference Void for Differential vias**
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
- GND/Reference Void for Chock
- GND/Reference Void for Resistors
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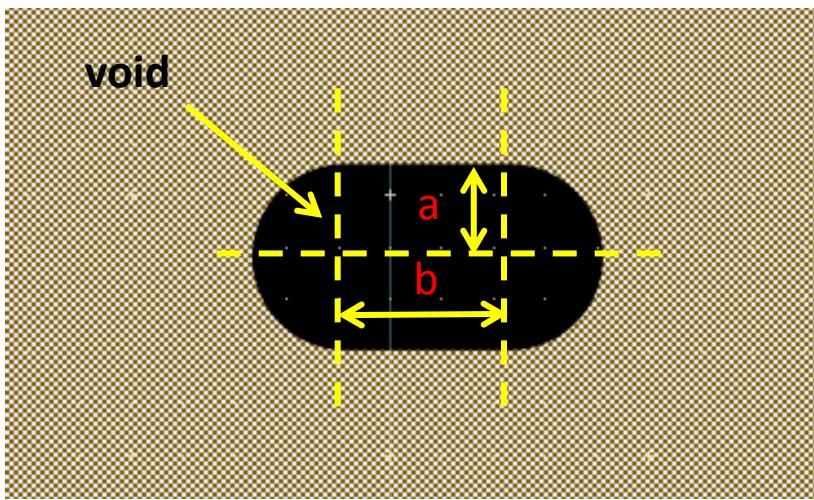
GND/Reference Void for Differential vias



Circular void



**Optimized void
(SI suggest)**

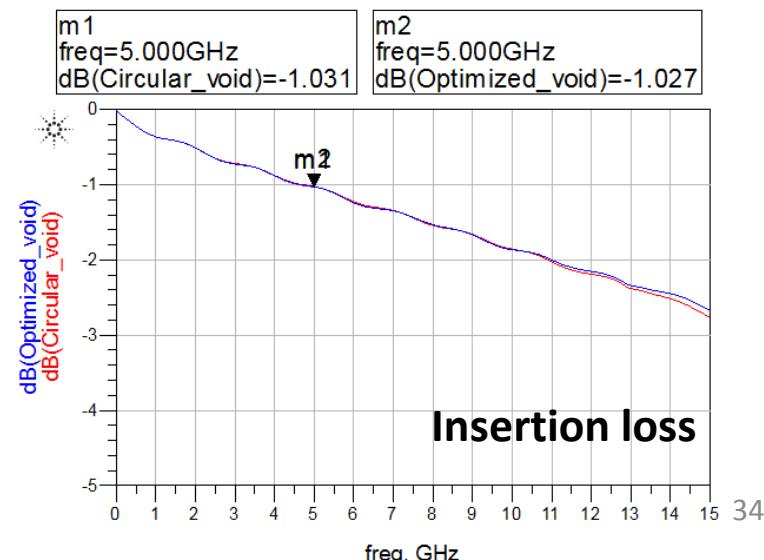
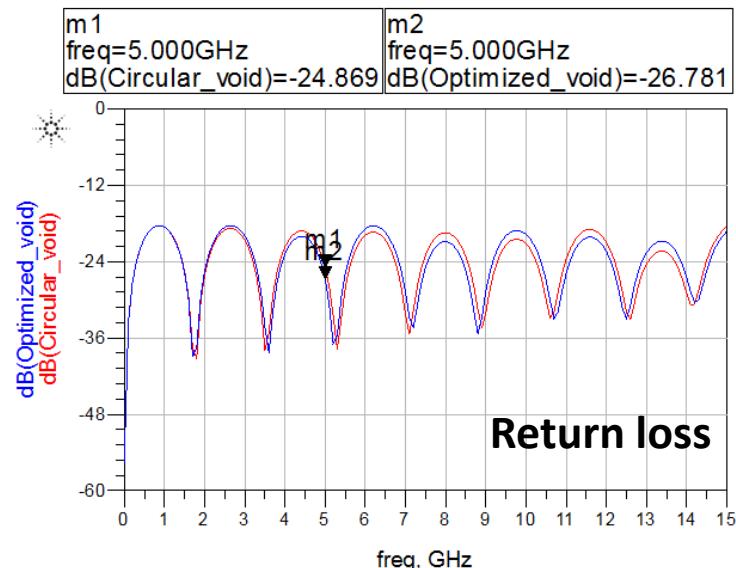
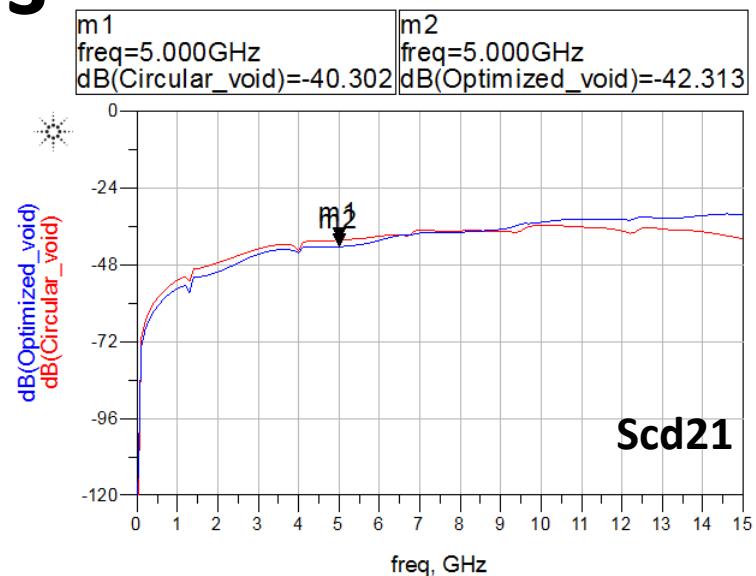
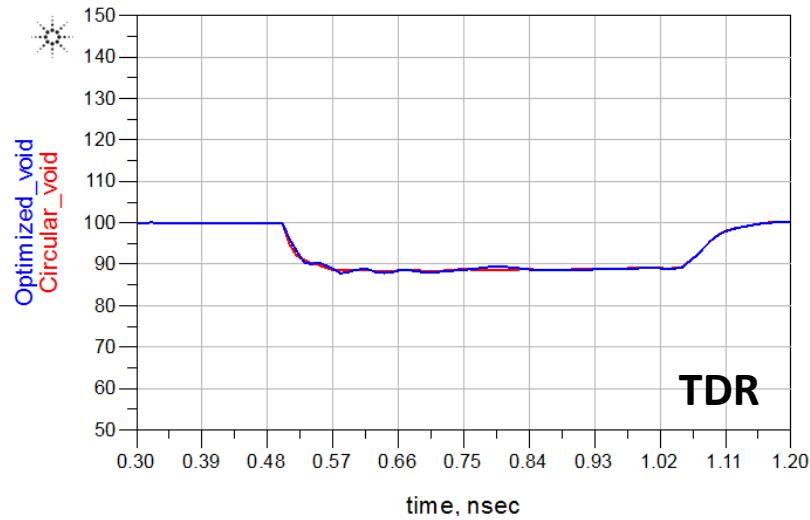


Layer 2 & 3

	Optimized void	Circular void
a	18 mil	18 mil
b	33.72 mil	33.72 mil

"PTH Ground Void for Standard A and B is the same as Ground Void of Differential Via "

GND/Reference Void for Differential vias

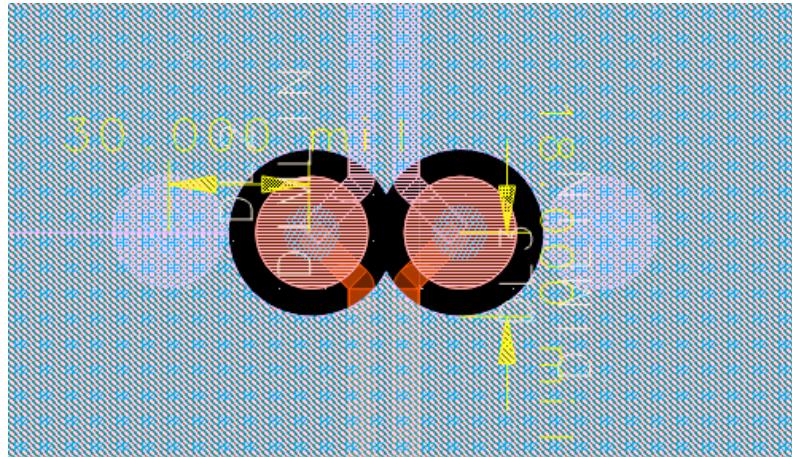


GND/Reference Void for Differential vias

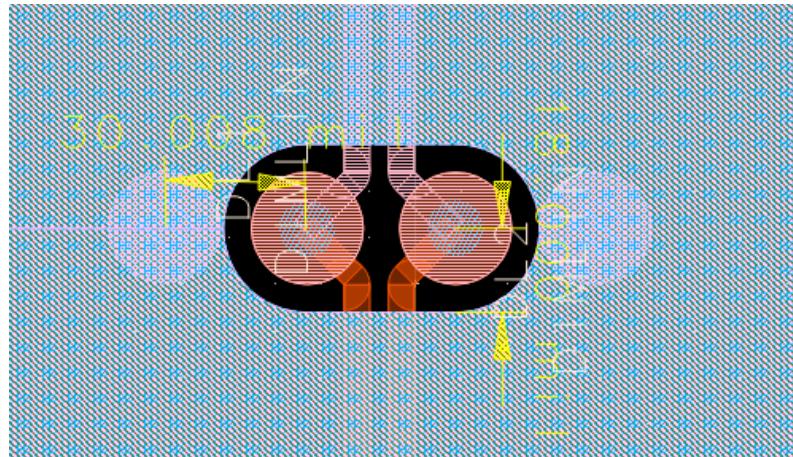
Summary:

For 4 layers board, **SI-suggested void** is better than **Circular void** in frequency and time domain.

GND/Reference Void for Differential vias

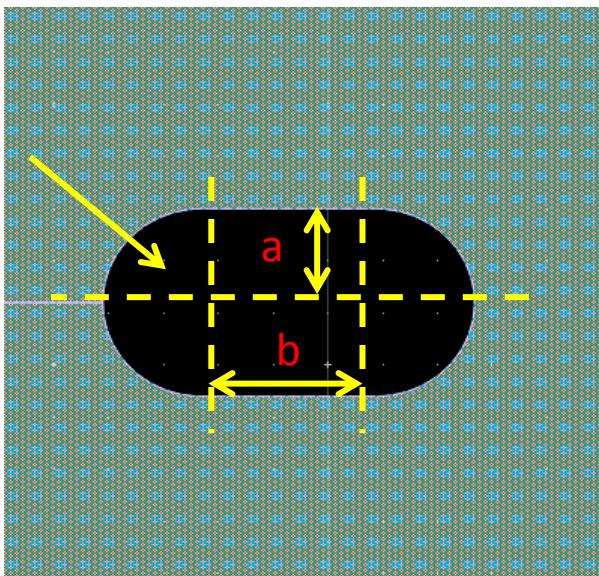


Circular void



**Optimized void
(SI suggest)**

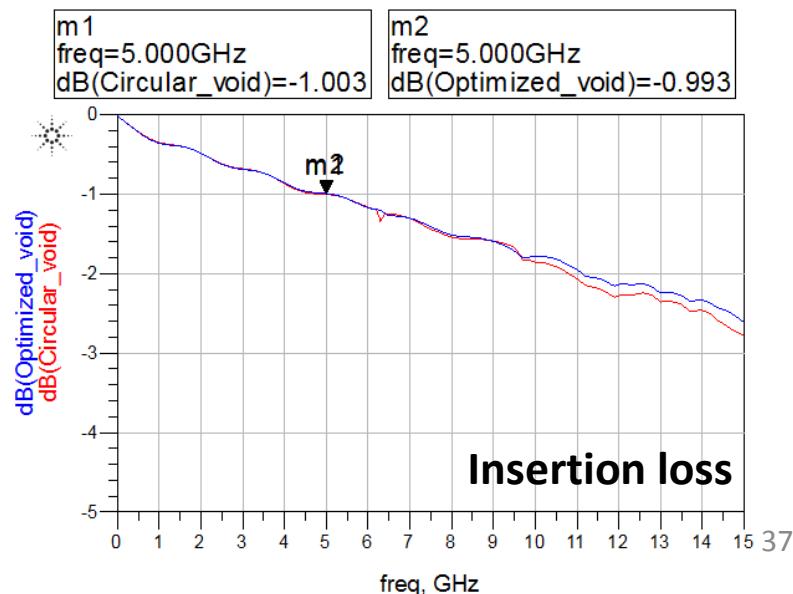
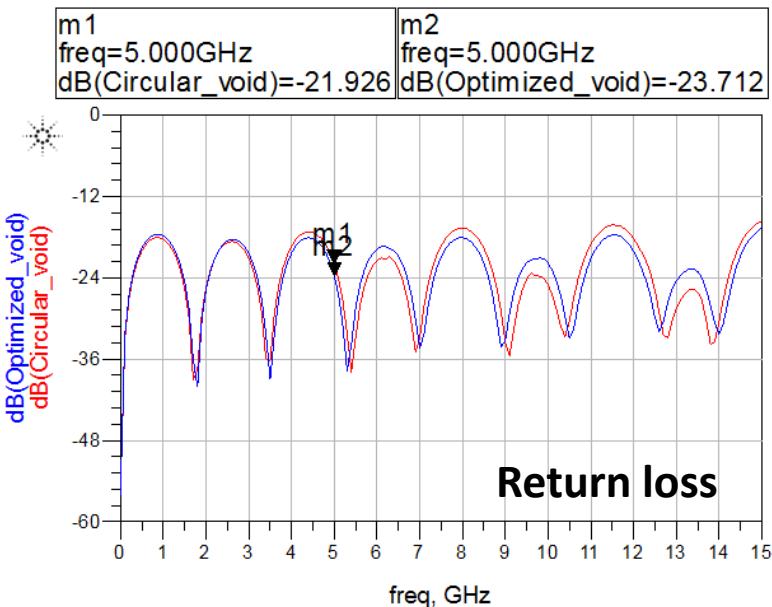
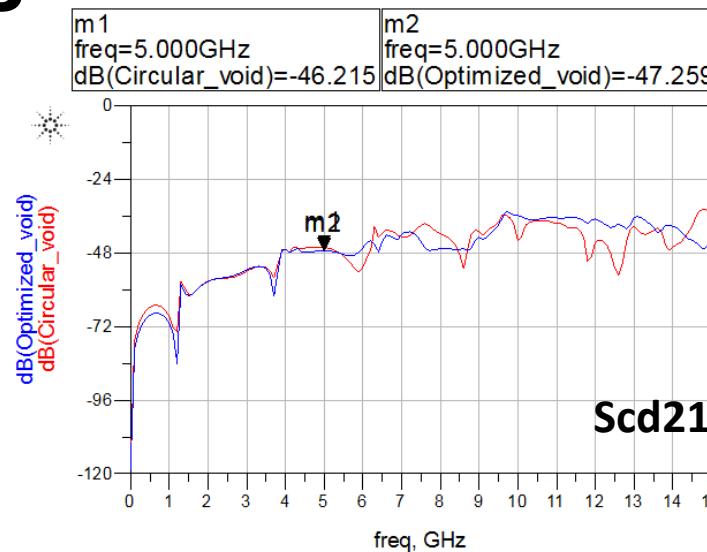
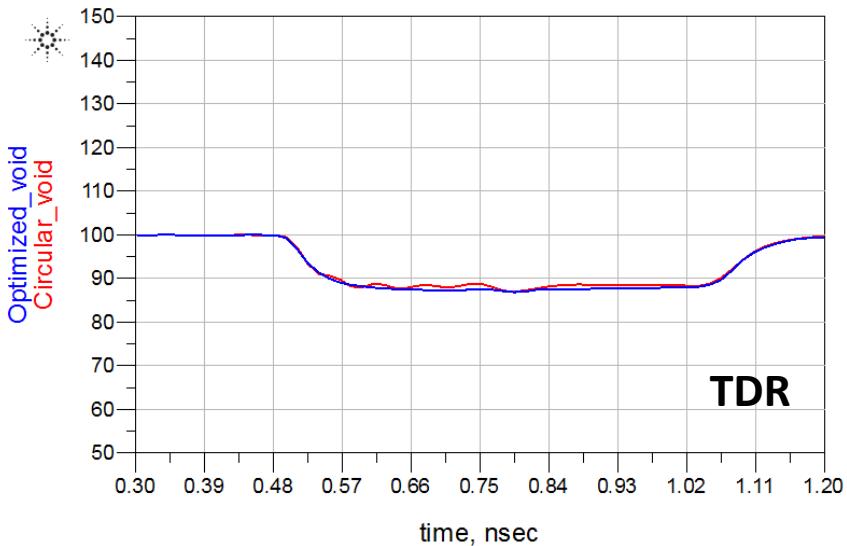
void



Layer 2 , 3 , 4 & 5

	Optimized void	Circular void
a	18 mil	18 mil
b	33.72 mil	33.72 mil

GND/Reference Void for Differential vias



GND/Reference Void for Differential vias

Summary:

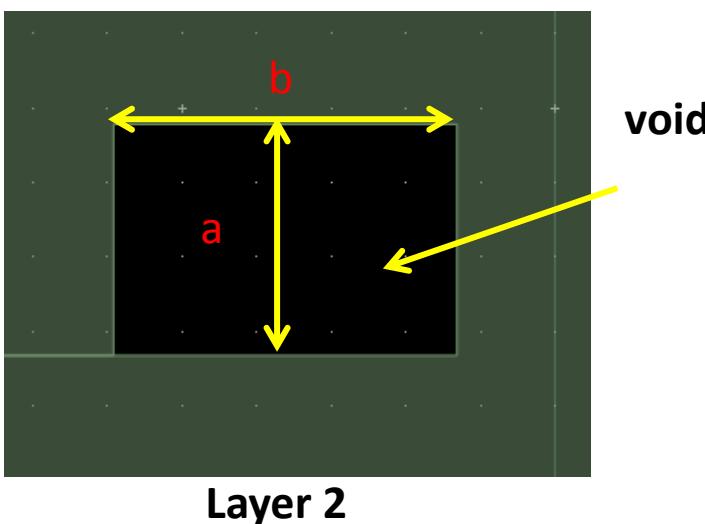
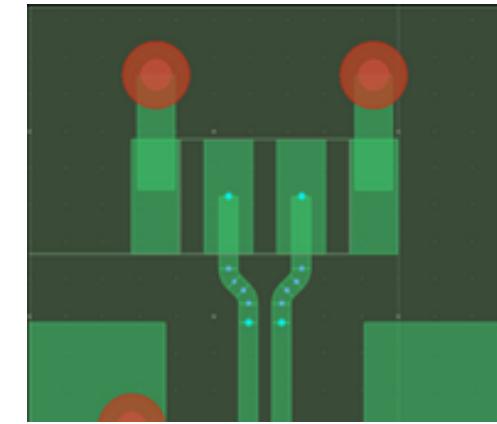
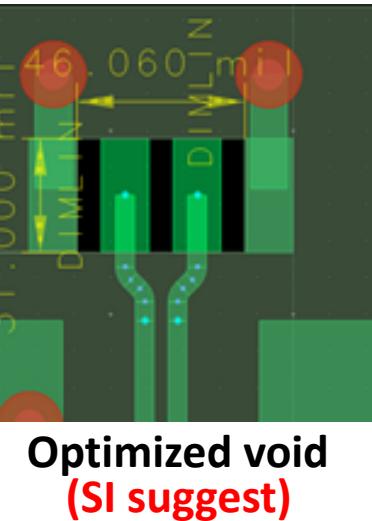
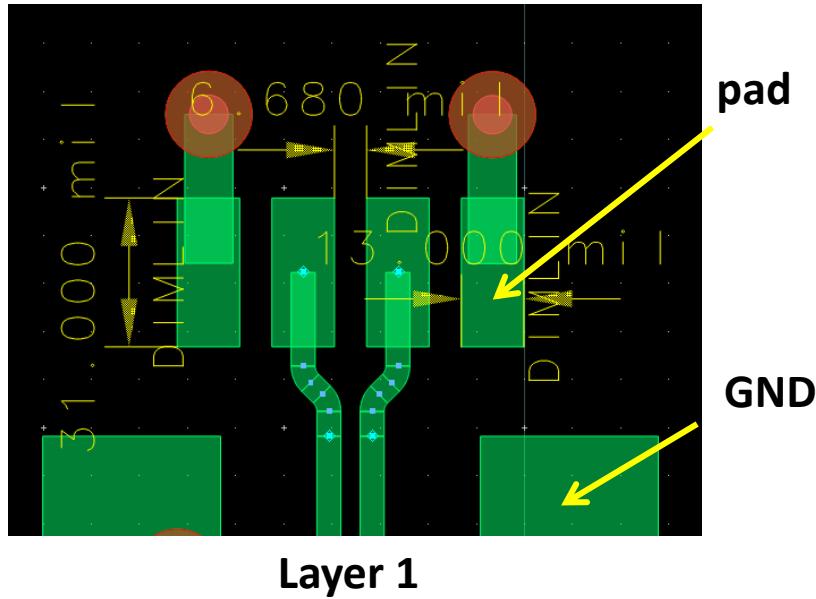
For 6 layers board, **SI-suggested void** is better than **Circular void** in frequency and time domain.



Outline

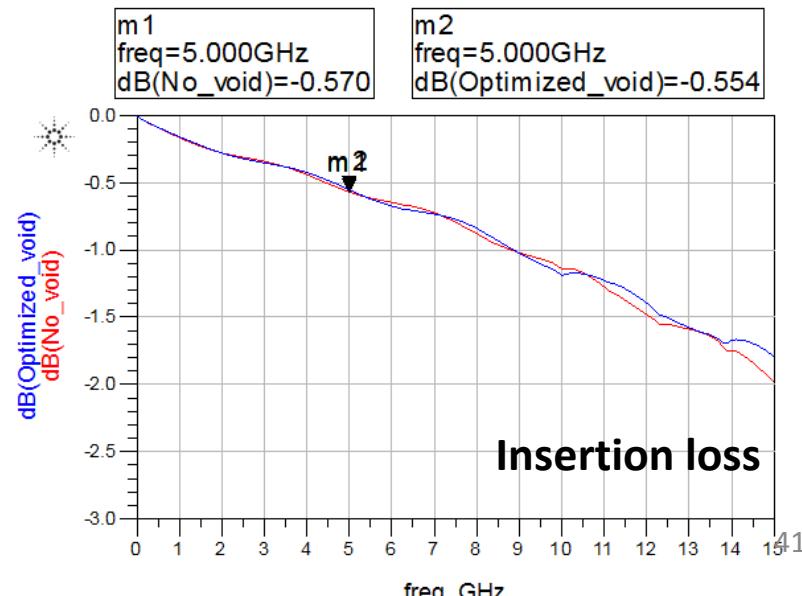
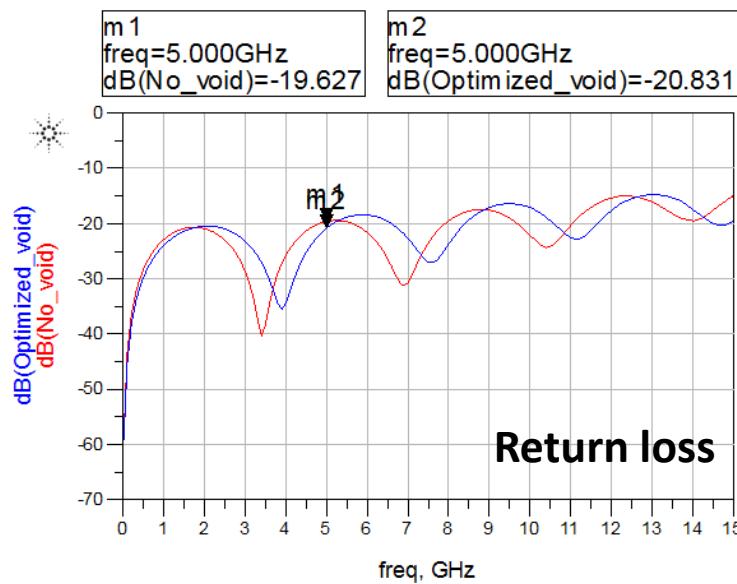
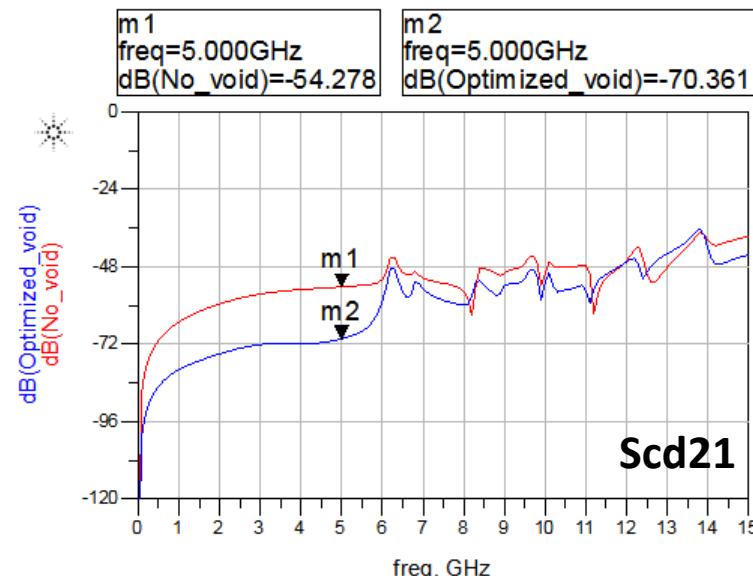
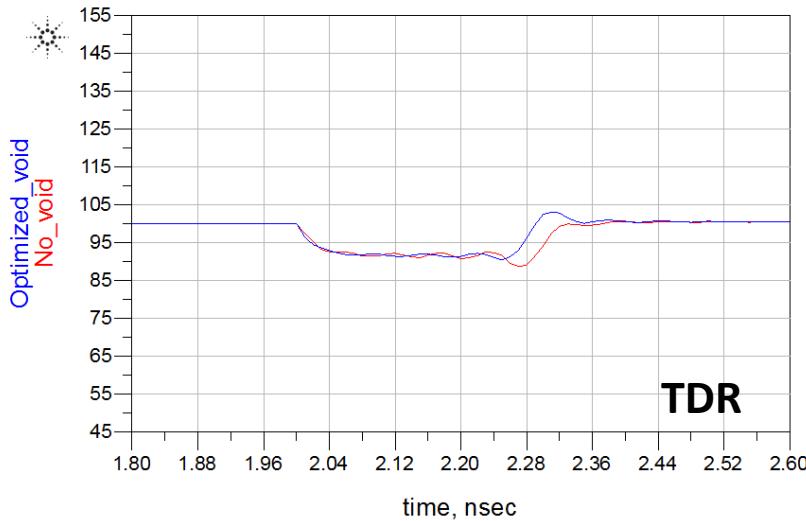
- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- **GND/Reference Void for Type-C**
- GND/Reference Void for ESD
- GND/Reference Void for Chock
- GND/Reference Void for Resistors
- Balanced GND vias Vs. Unbalanced GND vias
- Distance from GND via to Signal via
- Routing: Arc Vs. 135-degree-angle

GND/Reference Void for Type-C



	Optimized void	No void
a	31 mil	0 mil
b	46.06 mil	0 mil

GND/Reference Void for Type-C

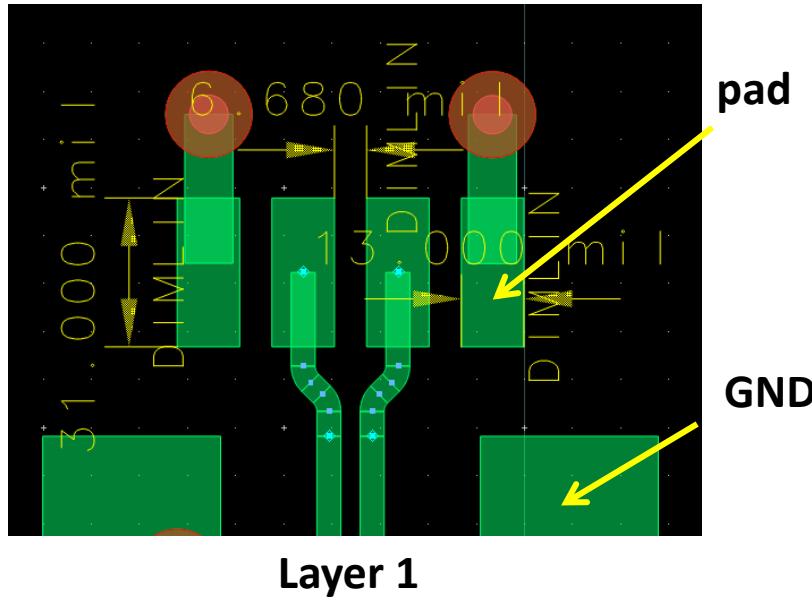


GND/Reference Void for Type-C

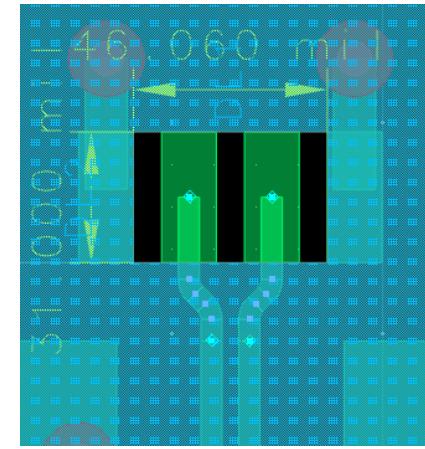
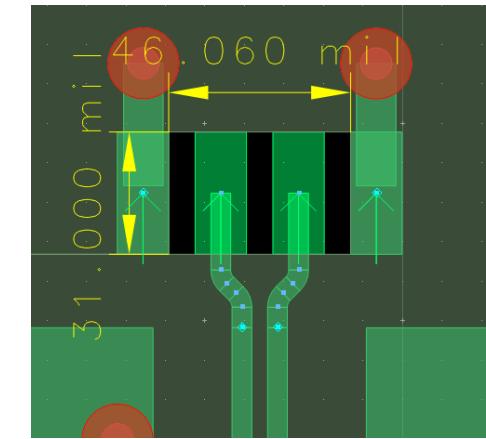
Summary:

For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

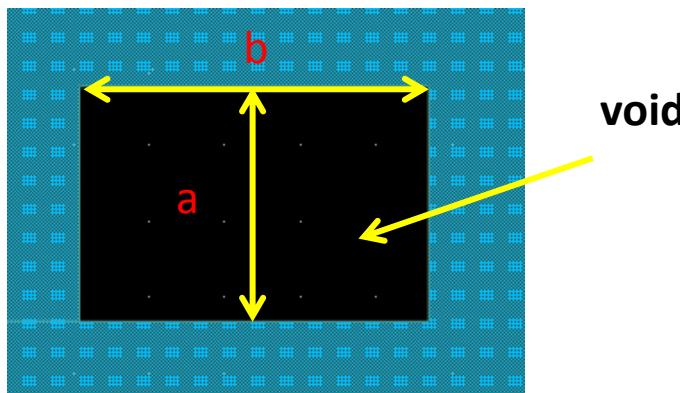
GND/Reference Void for Type-C



Layer 1

Layer 2 & 3 void
(SI suggest)

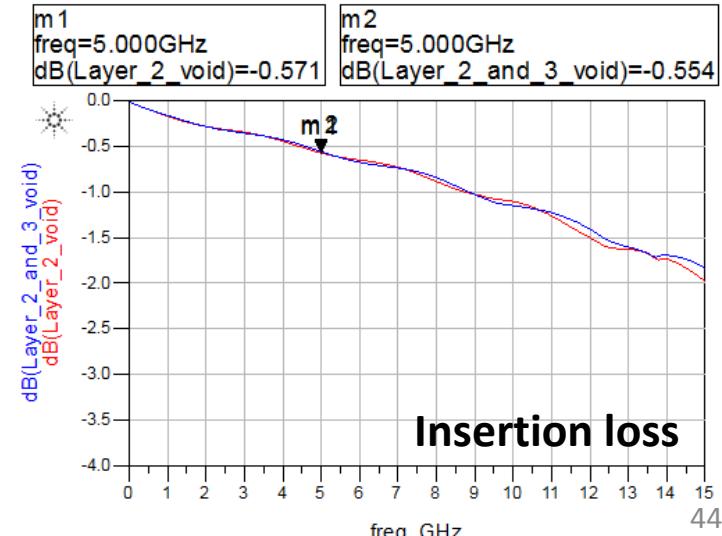
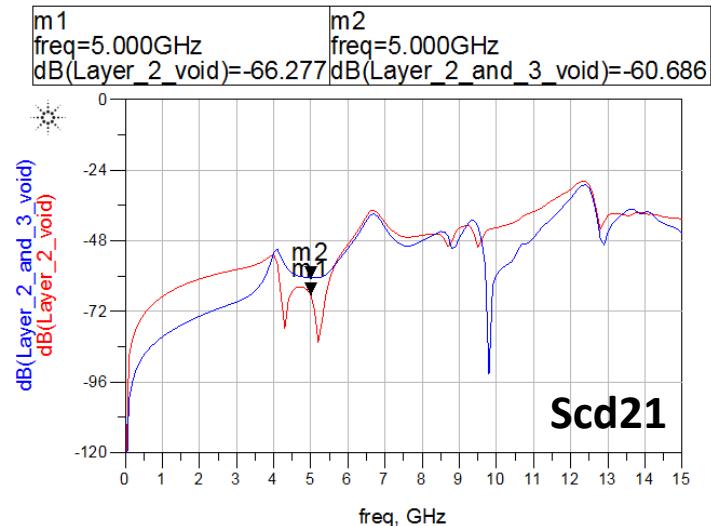
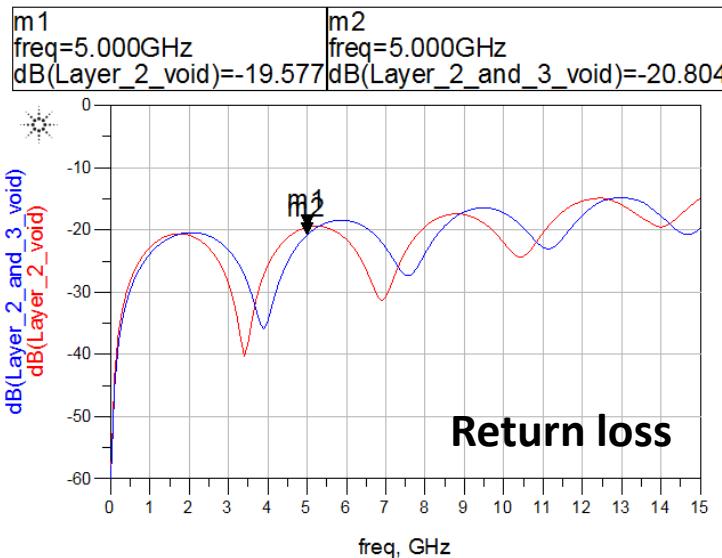
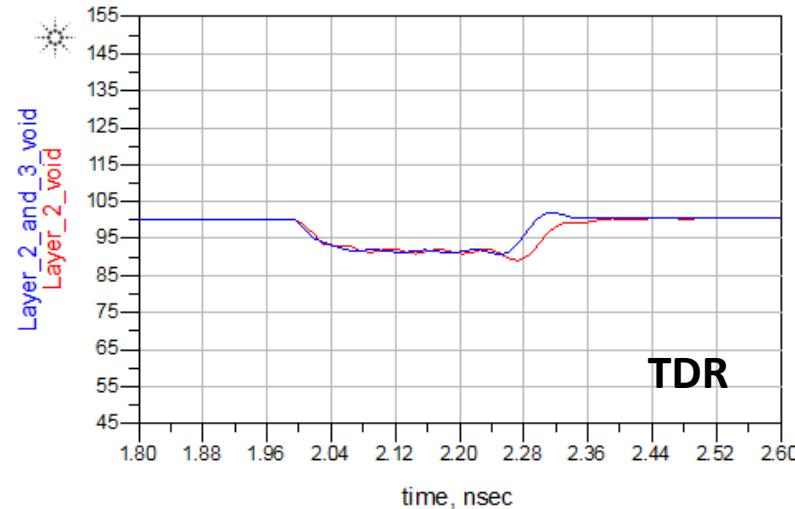
Layer 2 void



Layer 2 & 3

	Layer 2 & 3 void	Layer 2 void
a	31 mil	31 mil
b	46.06 mil	46.06 mil

GND/Reference Void for Type-C



GND/Reference Void for Type-C

Summary:

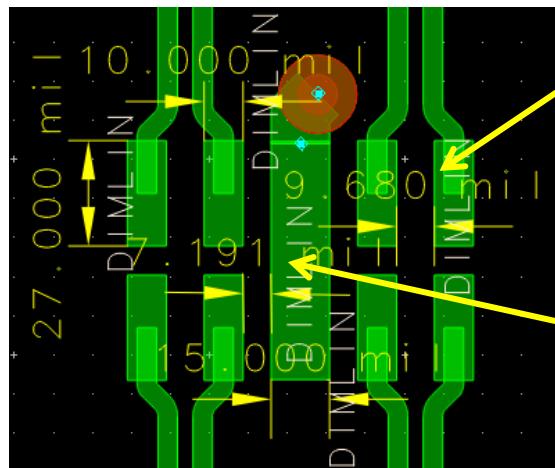
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.



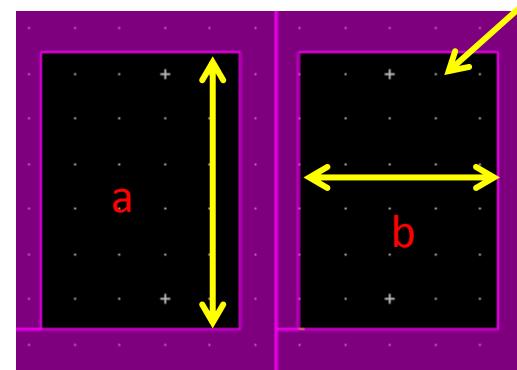
Outline

- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- **GND/Reference Void for ESD**
- GND/Reference Void for Chock
- GND/Reference Void for Resistors
- Balanced GND vias Vs. Unbalanced GND vias
- Distance from GND via to Signal via
- Routing: Arc Vs. 135-degree-angle

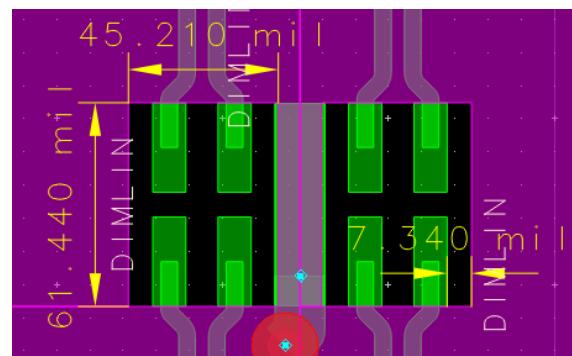
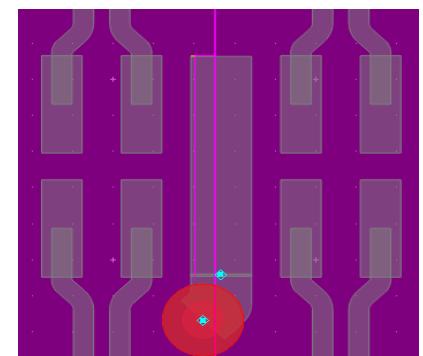
GND/Reference Void for ESD



Layer 1



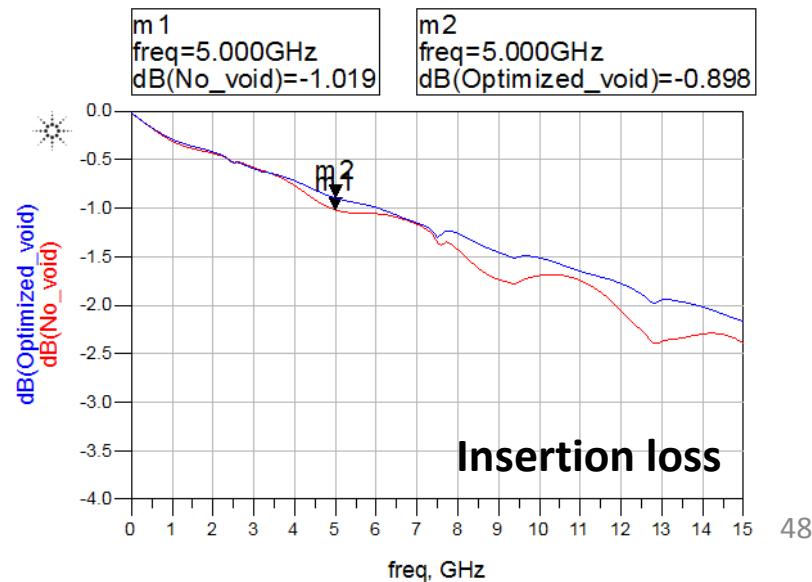
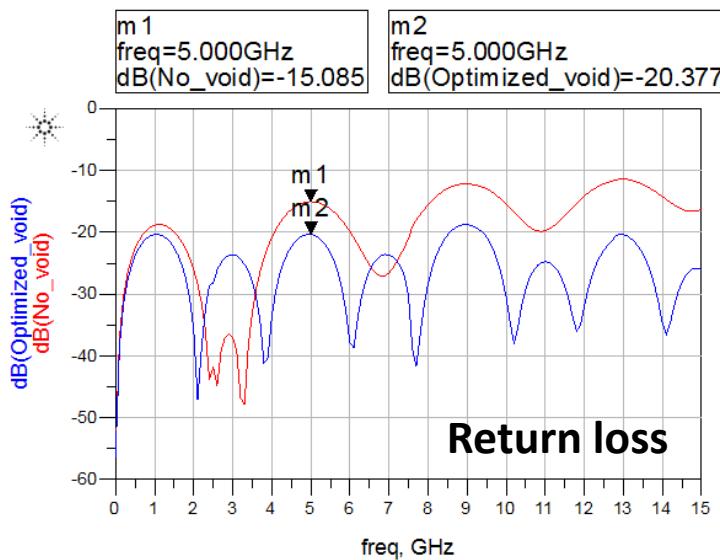
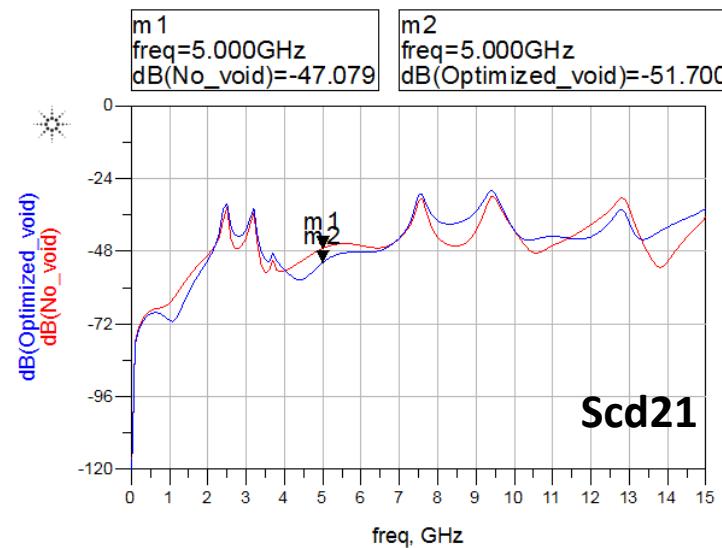
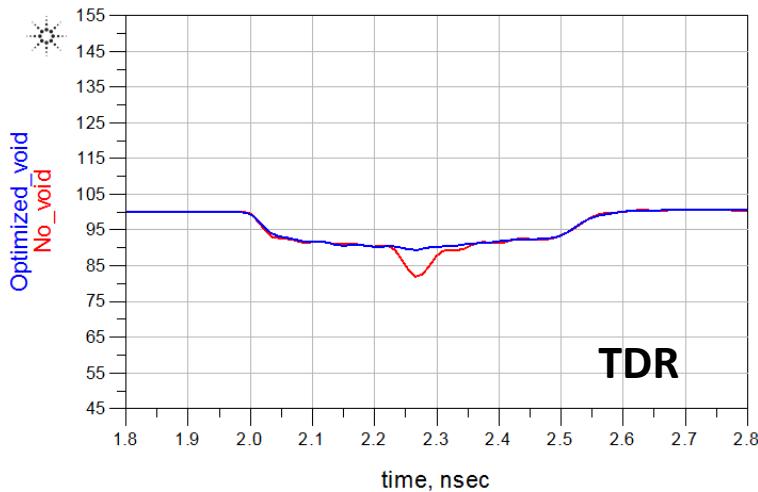
Layer 2

Optimized void
(SI suggest)

No void

	Optimized void	No void
a	61.44 mil	0 mil
b	45.21 mil	0 mil

GND/Reference Void for ESD

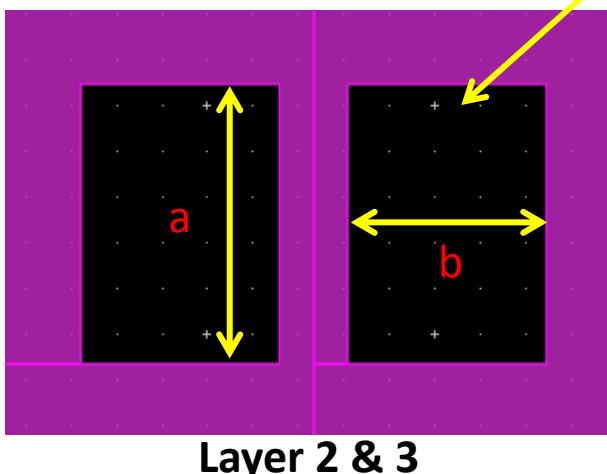
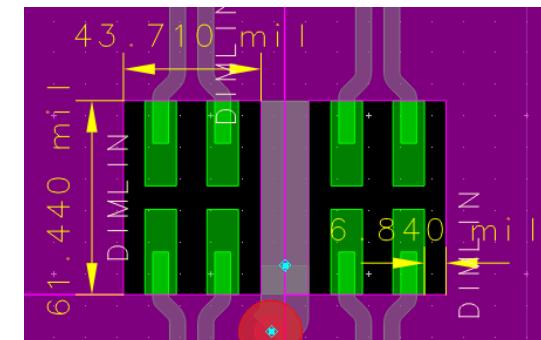
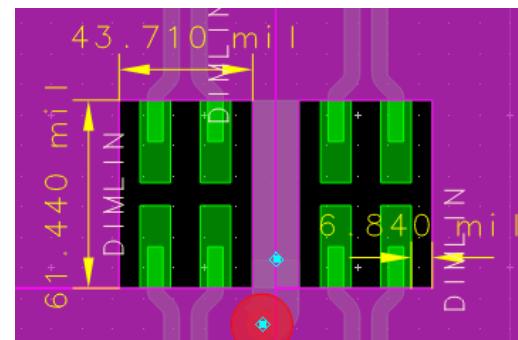
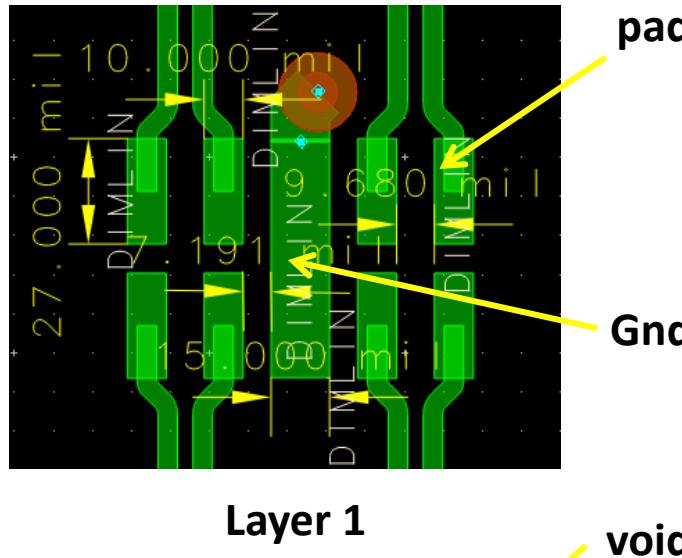


GND/Reference Void for ESD

Summary:

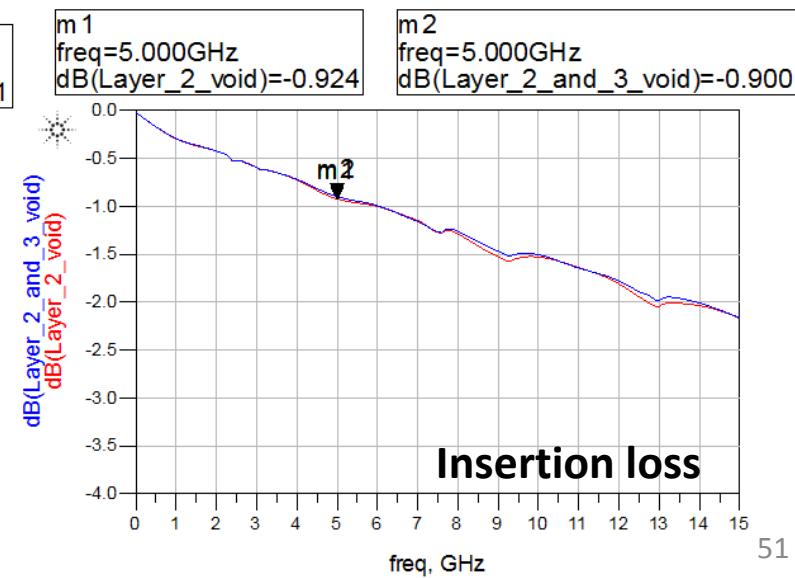
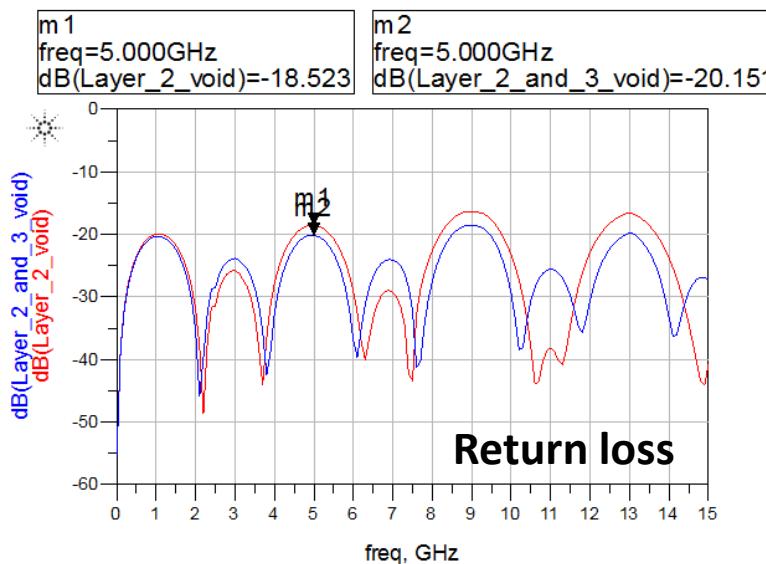
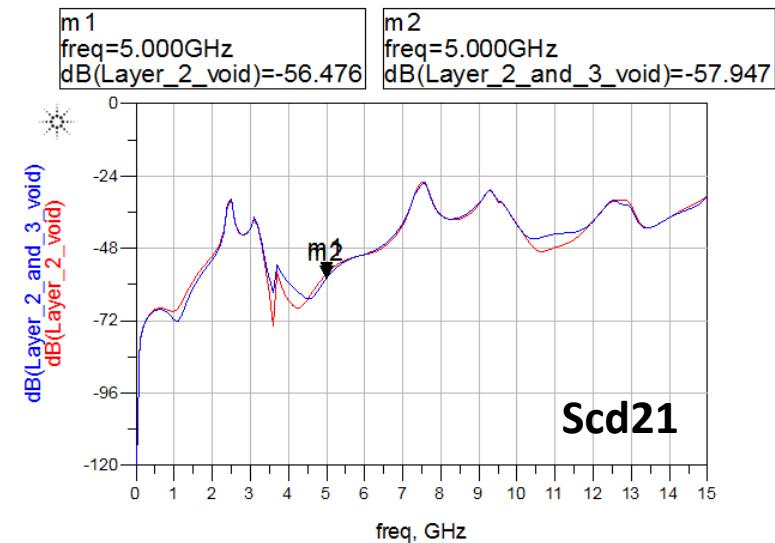
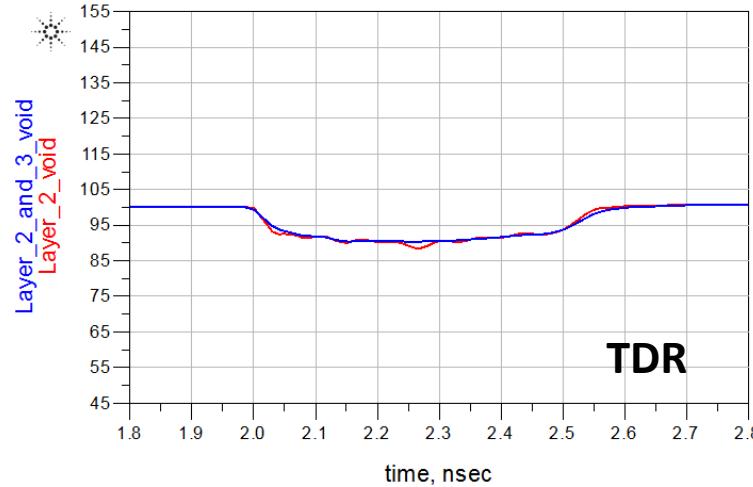
For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

GND/Reference Void for ESD



	Layer 2 & 3 void	Layer 2 void
a	61.44 mil	61.44 mil
b	43.71 mil	43.71 mil

GND/Reference Void for ESD

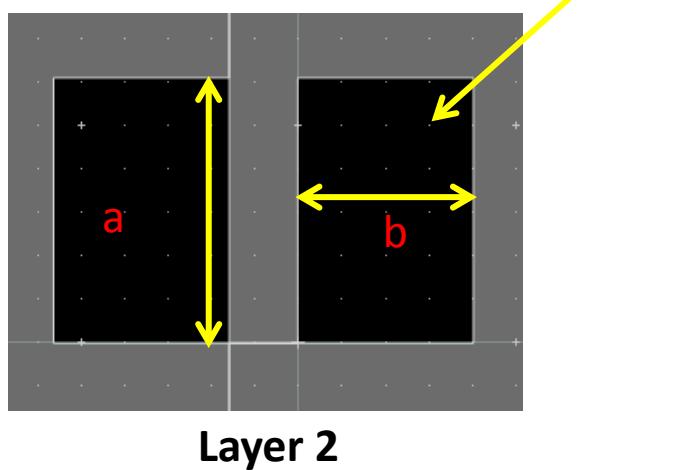
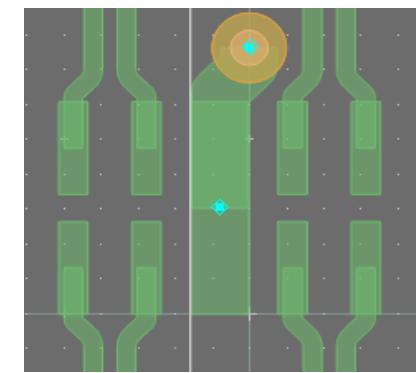
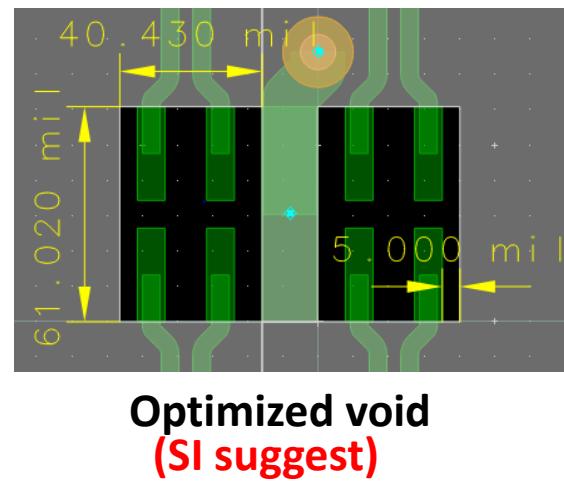
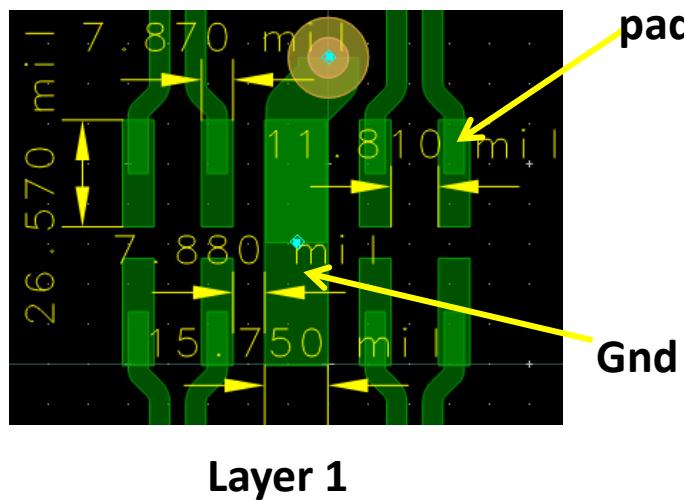


GND/Reference Void for ESD

Summary:

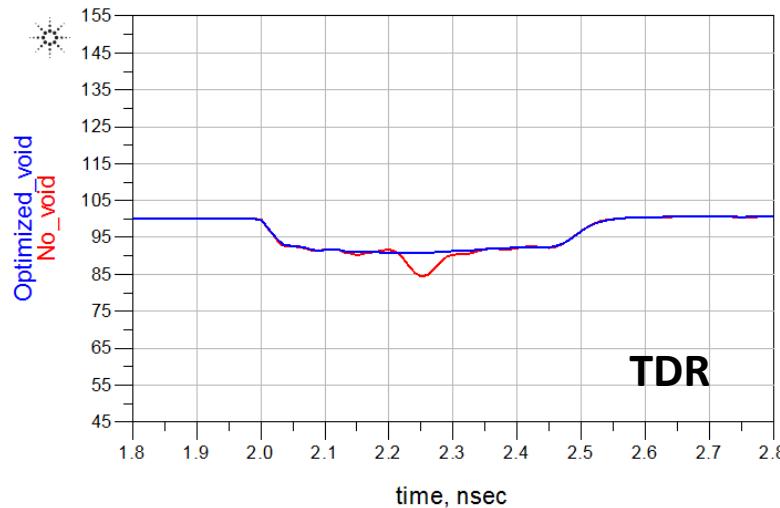
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.

GND/Reference Void for ESD



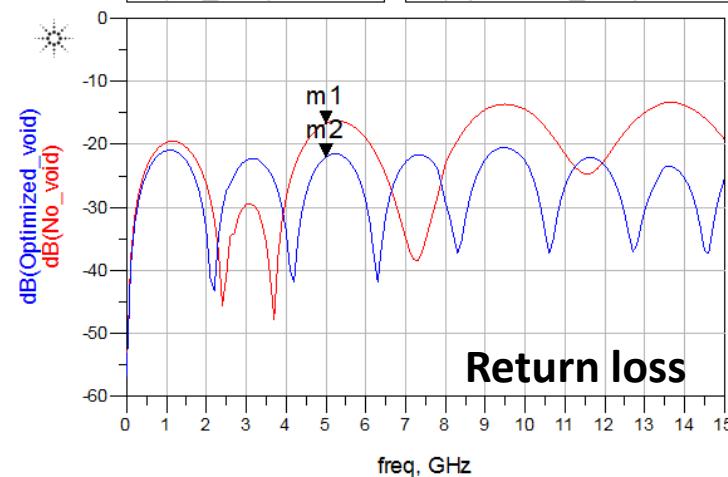
	Optimized void	No void
a	61.02 mil	0 mil
b	40.43 mil	0 mil

GND/Reference Void for ESD

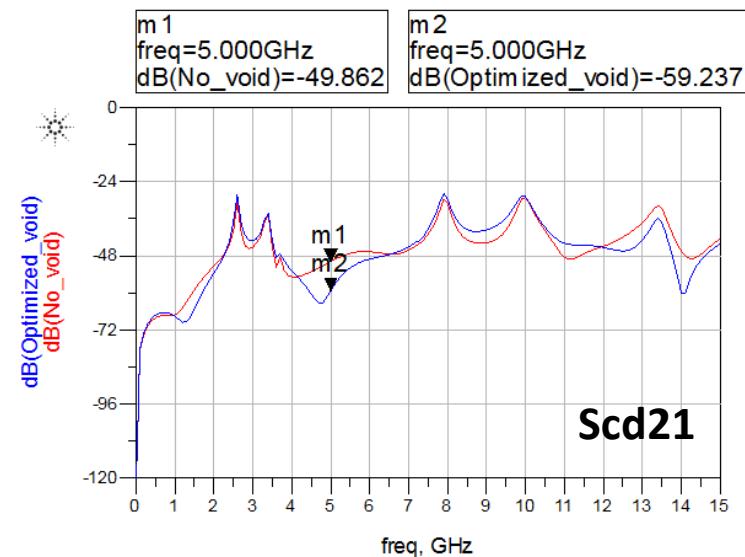


m 1
freq=5.000GHz
dB(No_void)=-16.671

m 2
freq=5.000GHz
dB(Optimized_void)=-21.982



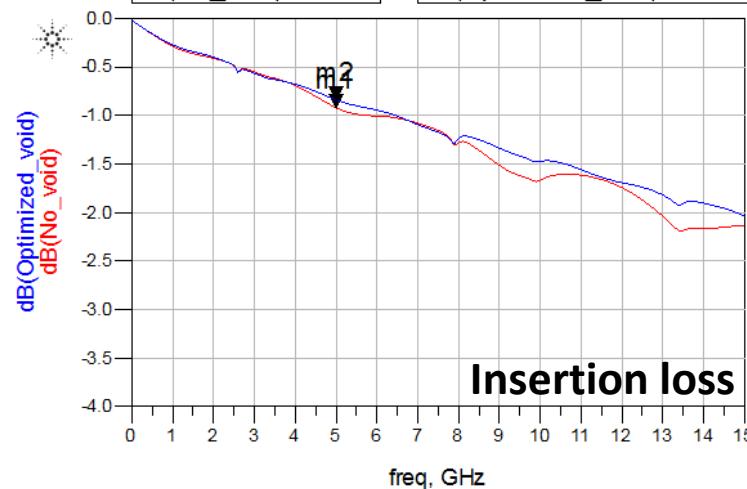
Return loss



Scd21

m 1
freq=5.000GHz
dB(No_void)=-0.921

m 2
freq=5.000GHz
dB(Optimized_void)=-0.839



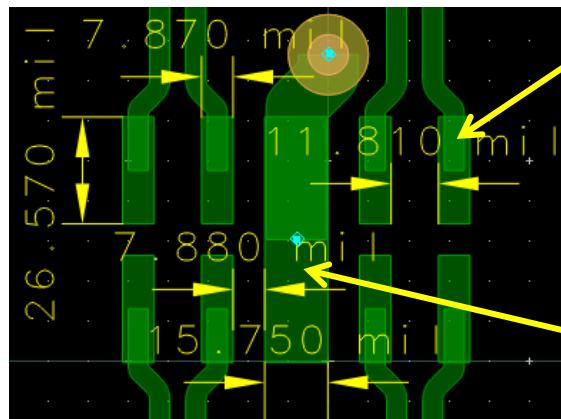
Insertion loss

GND/Reference Void for ESD

Summary:

For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

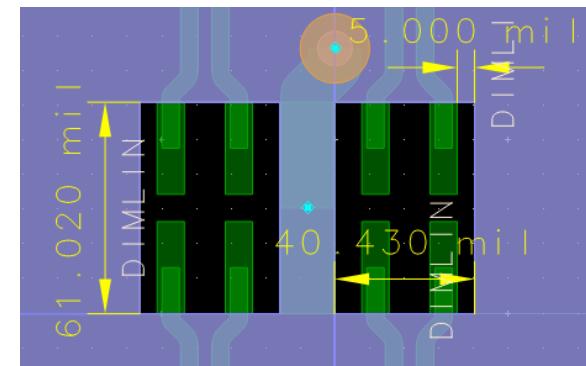
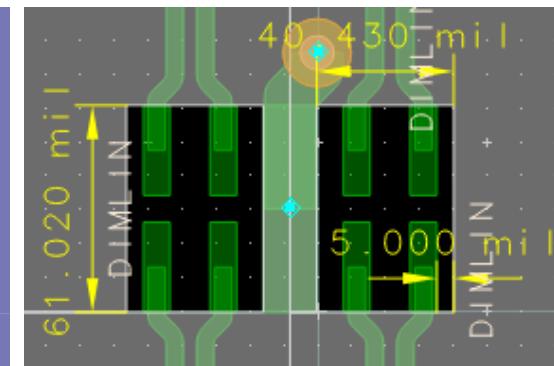
GND/Reference Void for ESD



Layer 1

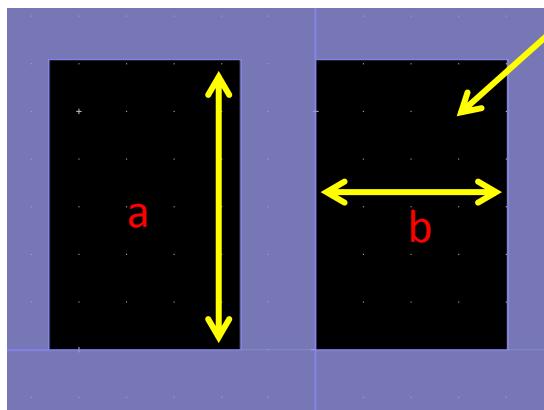
pad

Gnd

Layer 2 & 3 void
(SI suggest)

Layer 2 void

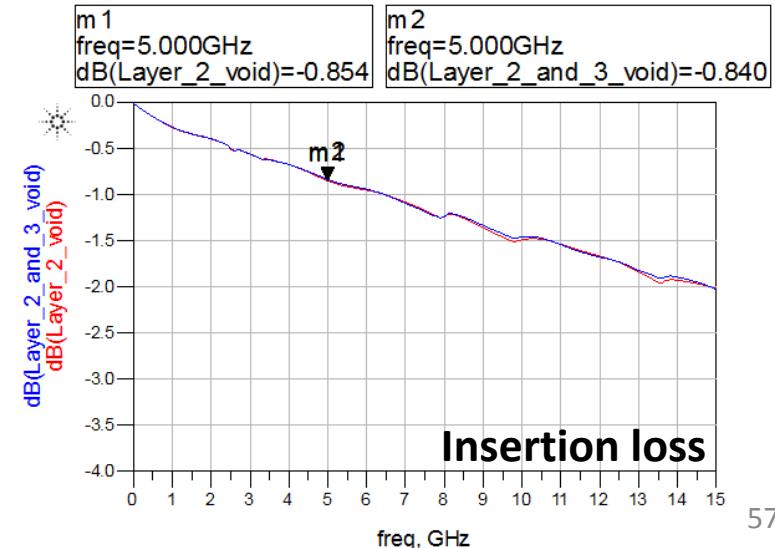
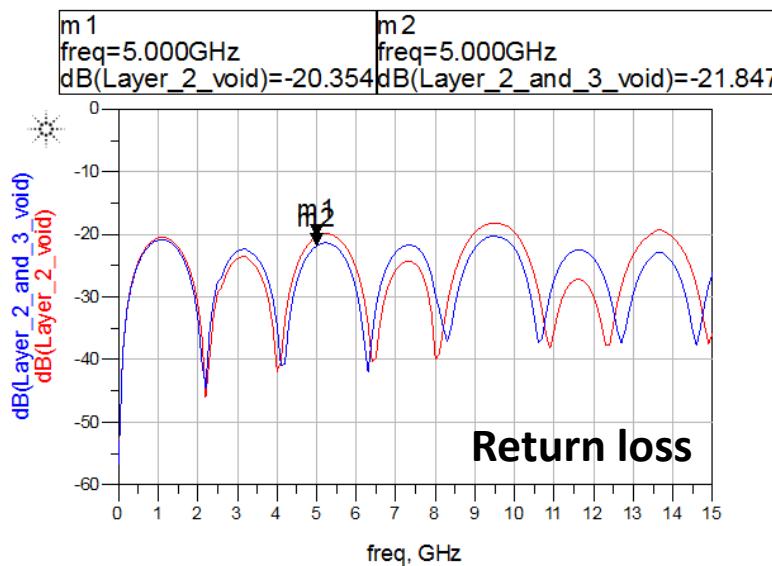
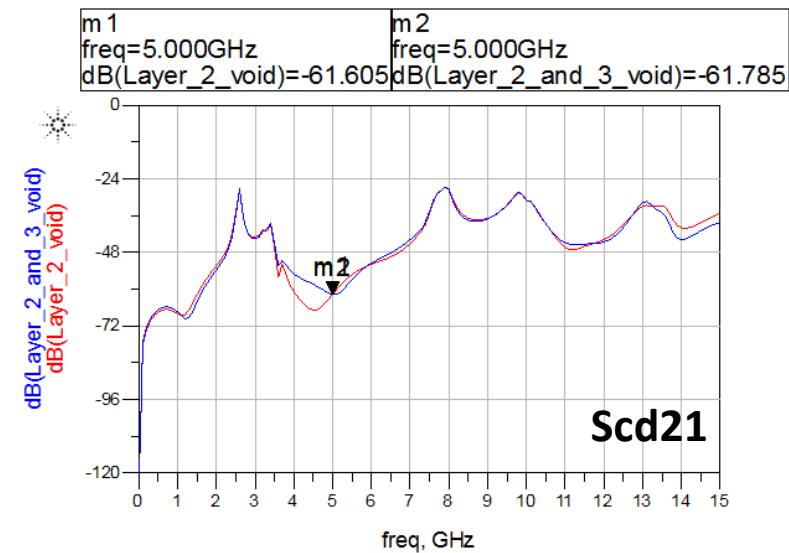
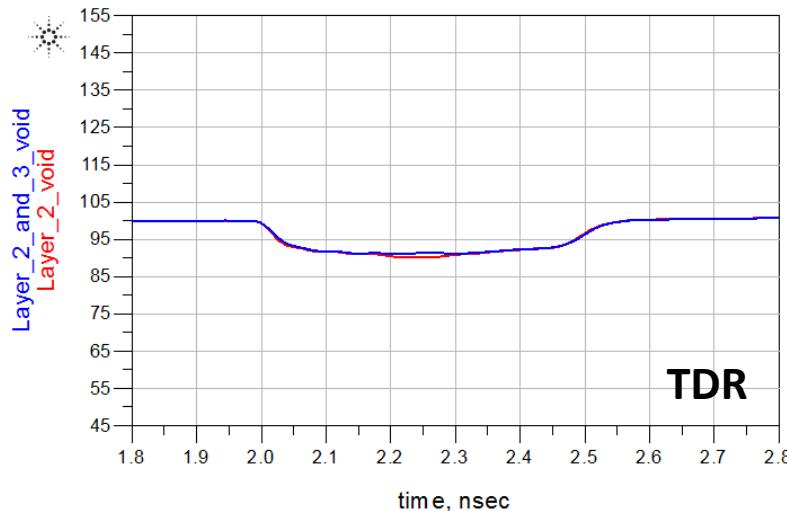
void



Layer 2 & 3

	Layer 2 & 3 void	Layer 2 void
a	61.02 mil	61.02 mil
b	40.43 mil	40.43 mil

GND/Reference Void for ESD

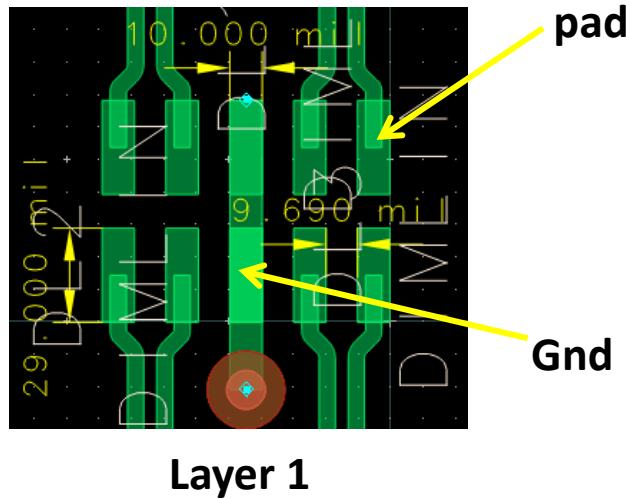


GND/Reference Void for ESD

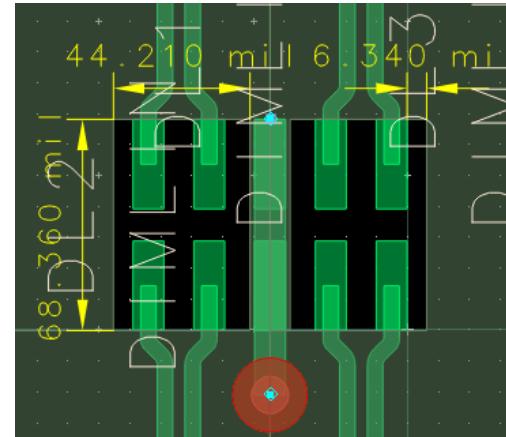
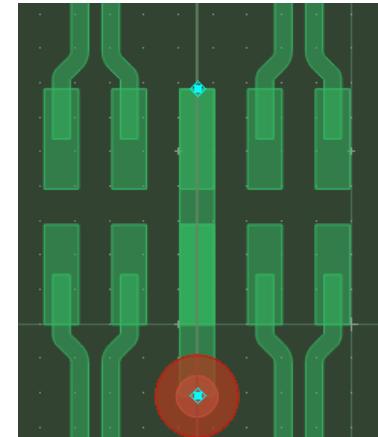
Summary:

For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.

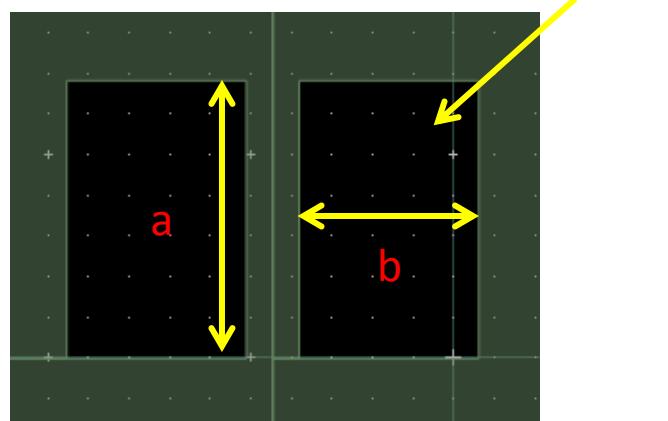
GND/Reference Void for ESD



Layer 1

Optimized void
(SI suggest)

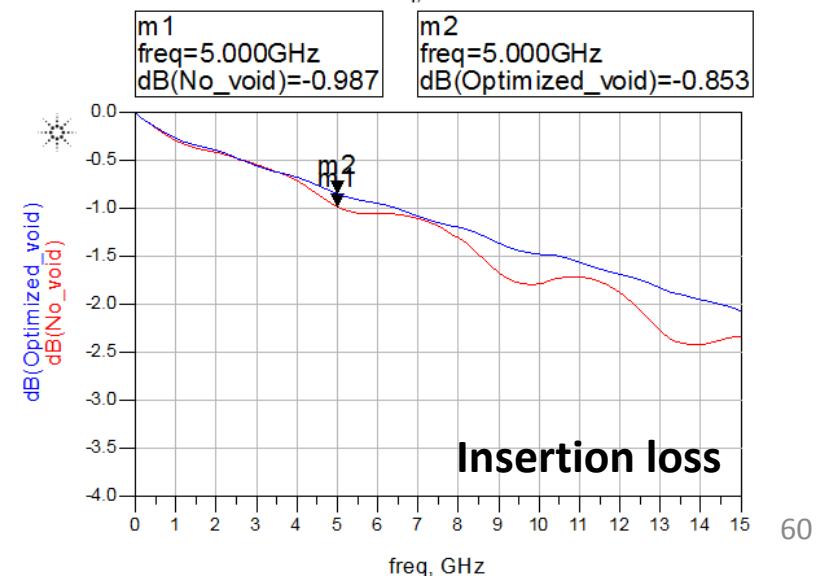
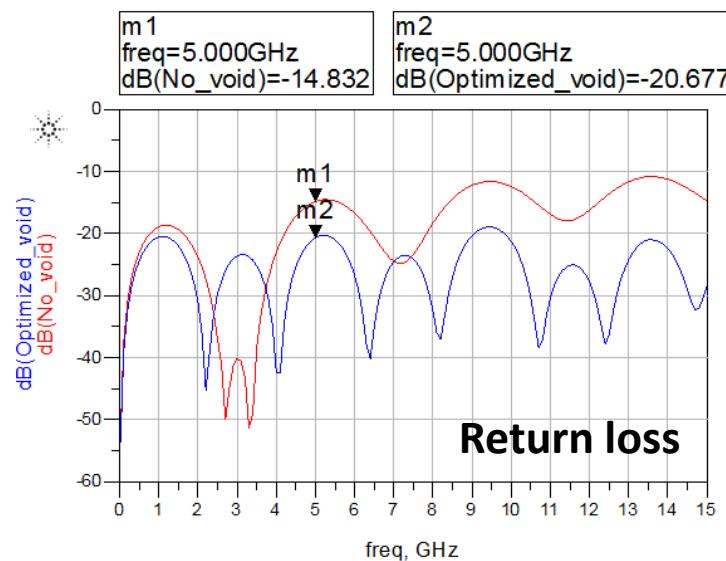
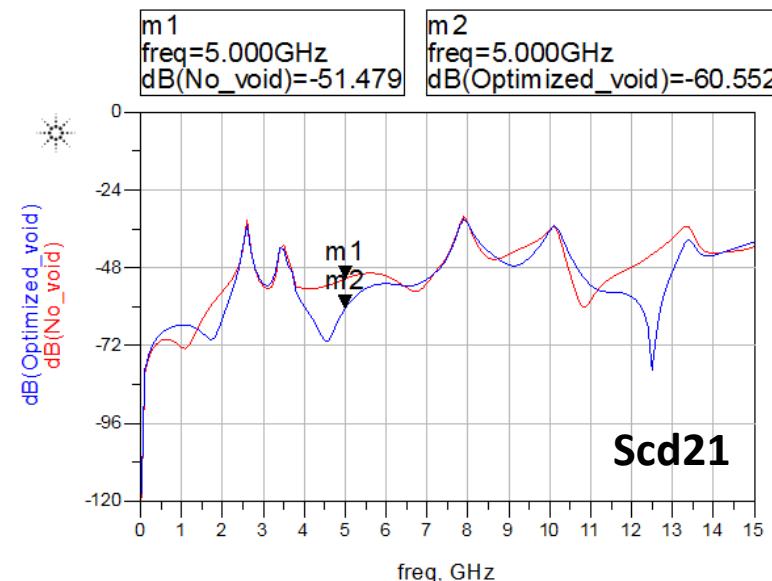
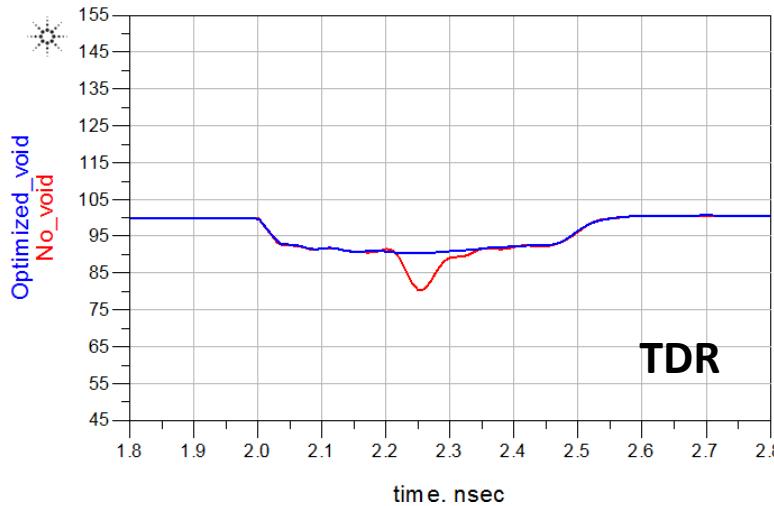
No void



Layer 2

	Optimized void	No void
a	68.36 mil	0 mil
b	44.21 mil	0 mil

GND/Reference Void for ESD

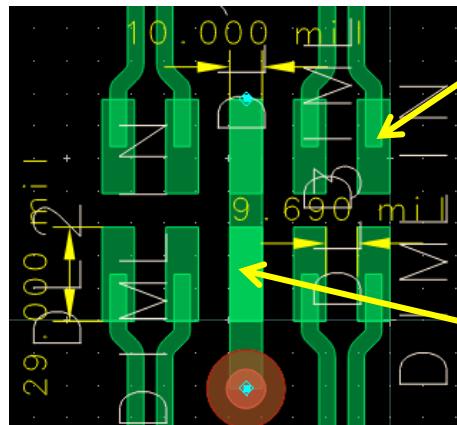


GND/Reference Void for ESD

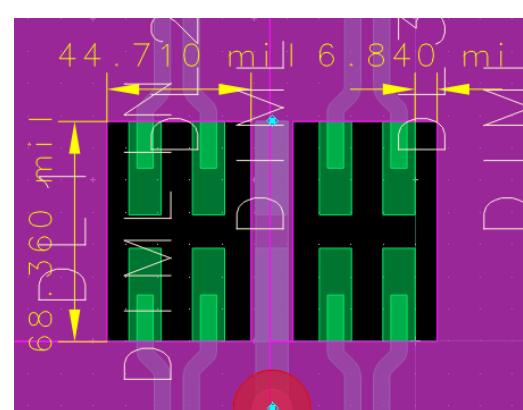
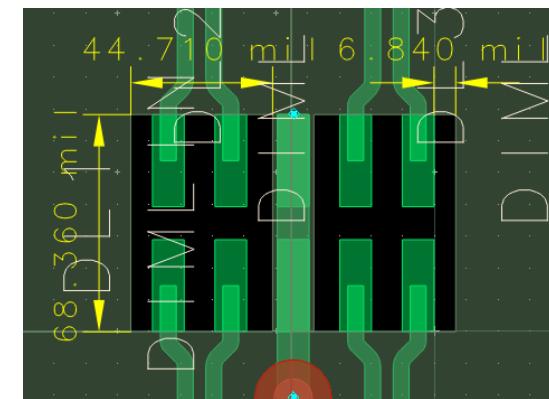
Summary:

For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

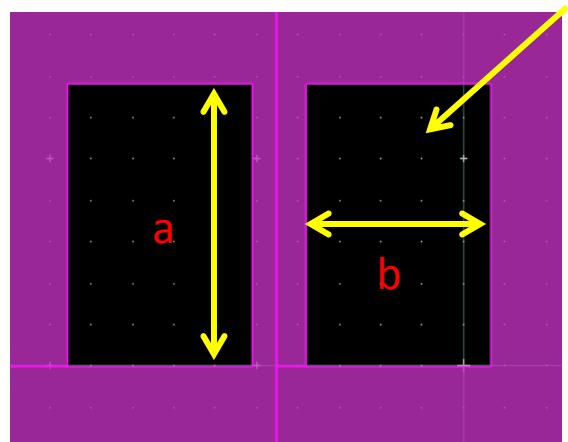
GND/Reference Void for ESD



Layer 1

Layer 2 & 3 void
(SI suggest)

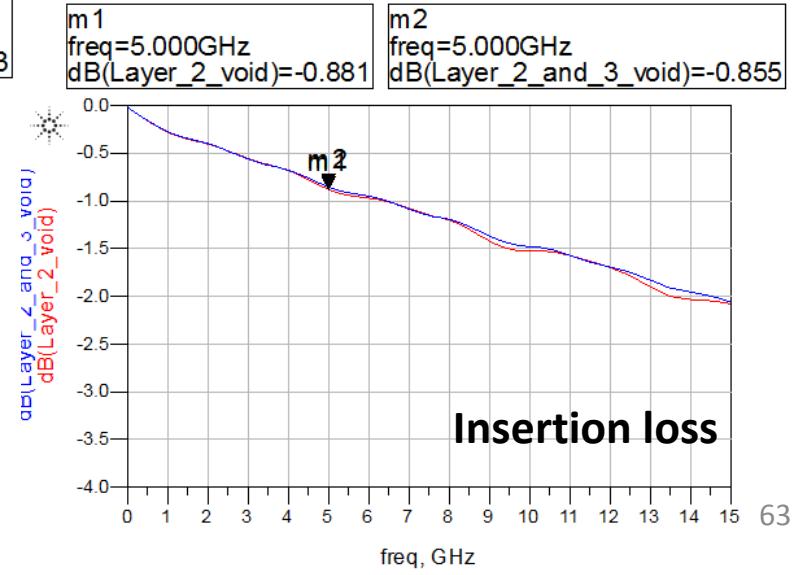
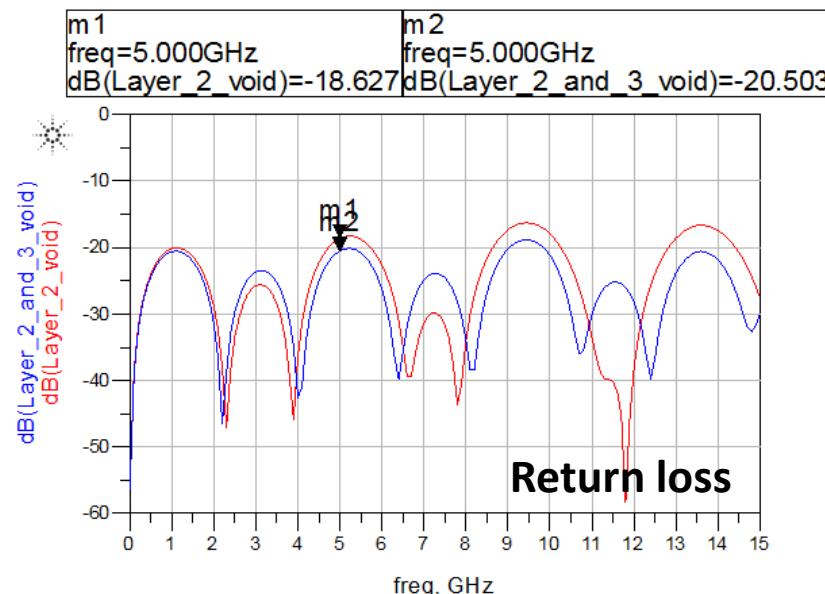
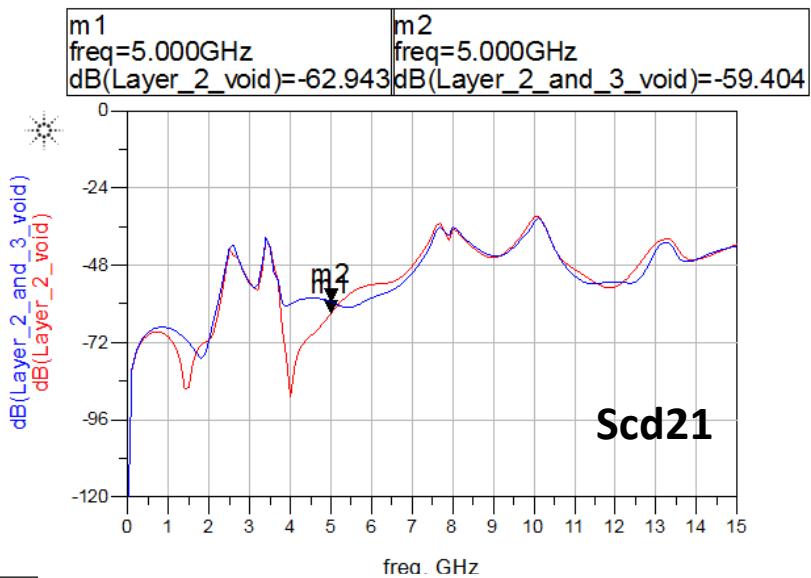
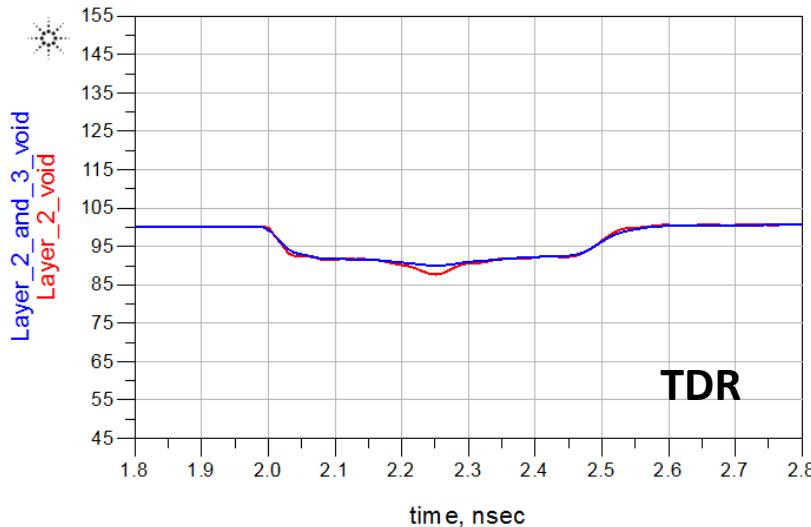
Layer 2 void



Layer 2 & 3

	Layer 2 & 3 void	Layer 2 void
a	68.36 mil	68.36 mil
b	44.71 mil	44.71 mil

GND/Reference Void for ESD

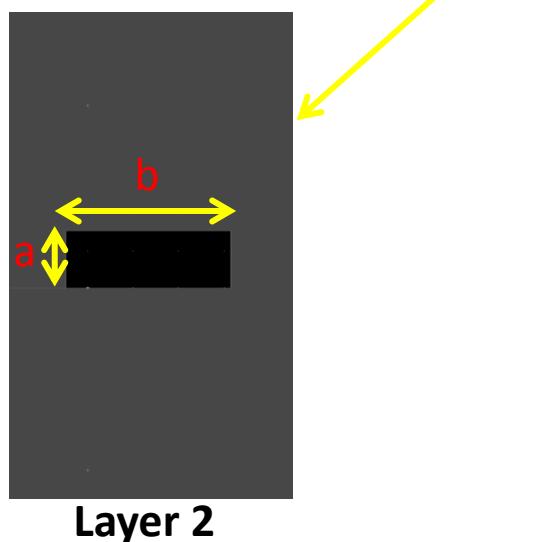
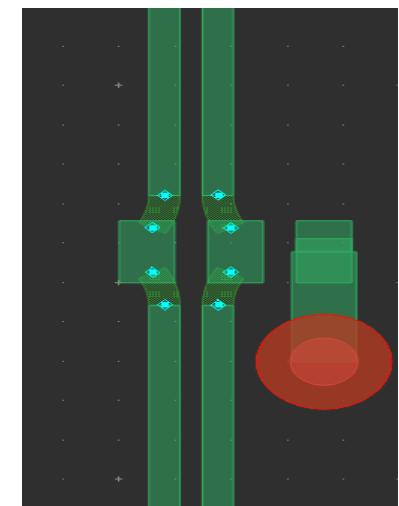
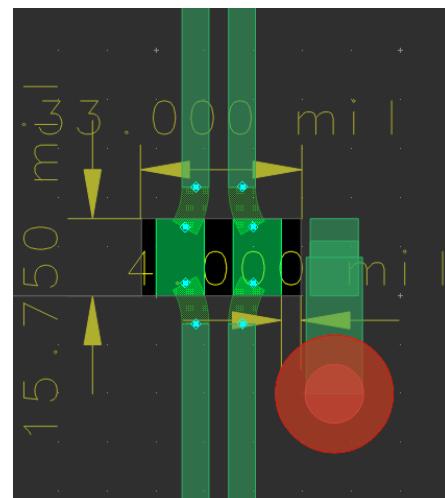
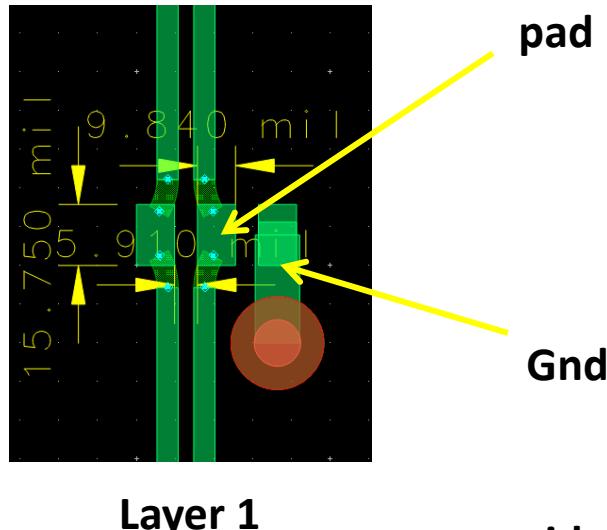


GND/Reference Void for ESD

Summary:

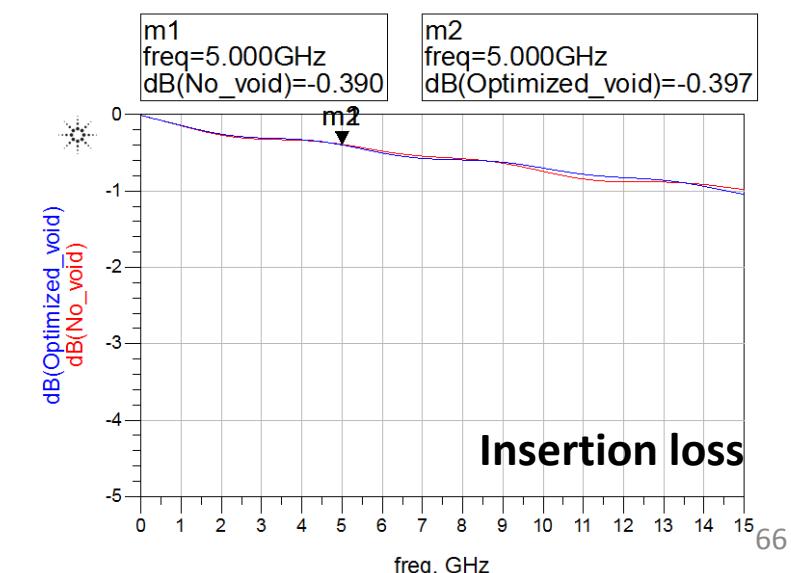
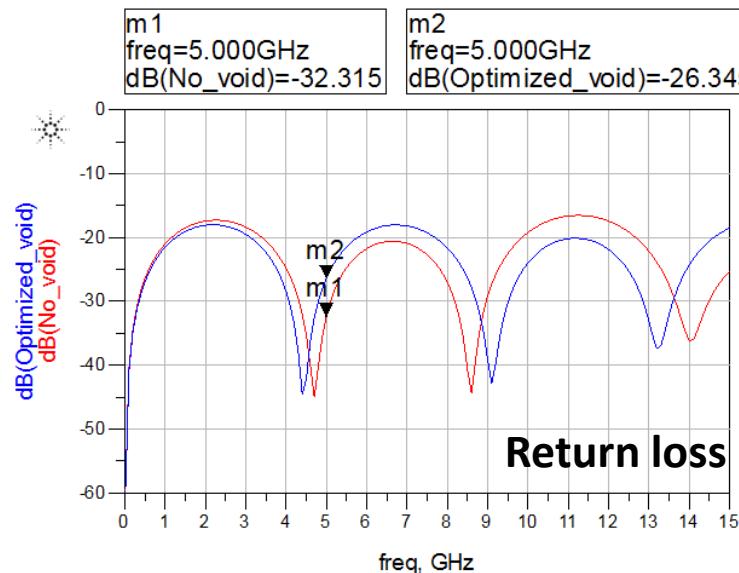
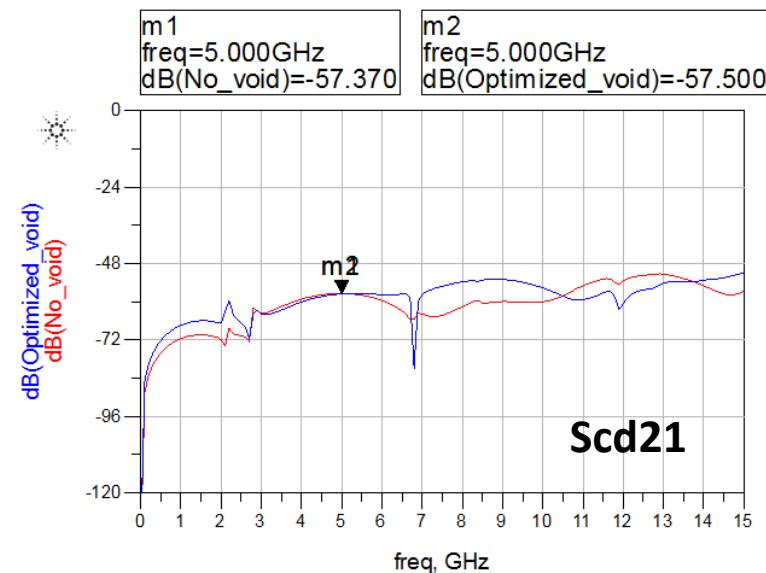
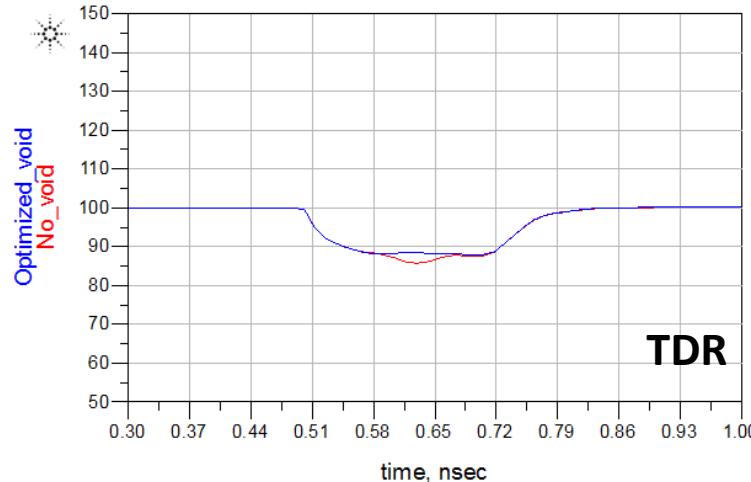
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.

GND/Reference Void for ESD



	Optimized void	No void
a	15.75 mil	0 mil
b	33 mil	0 mil

GND/Reference Void for ESD

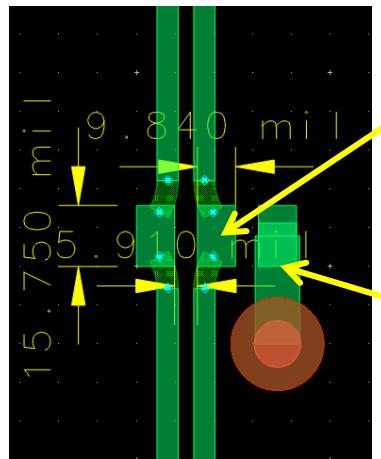


GND/Reference Void for ESD

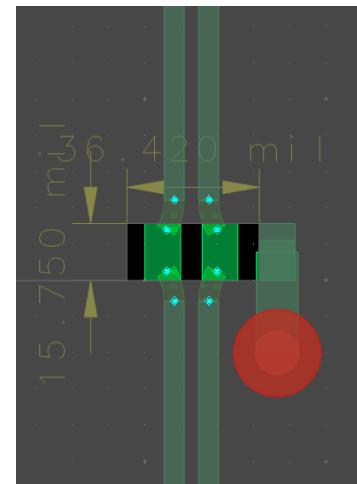
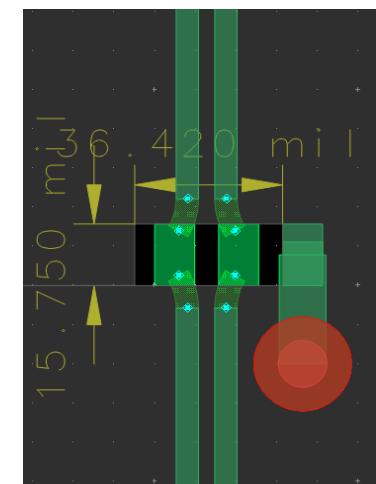
Summary:

For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

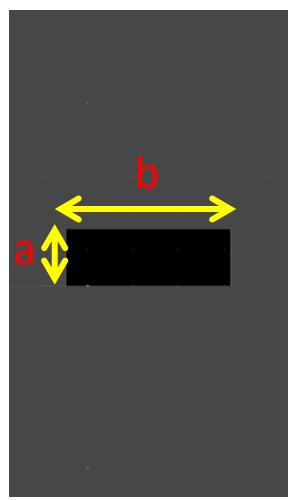
GND/Reference Void for ESD



Layer 1

Layer 2 & 3 void
(SI suggest)

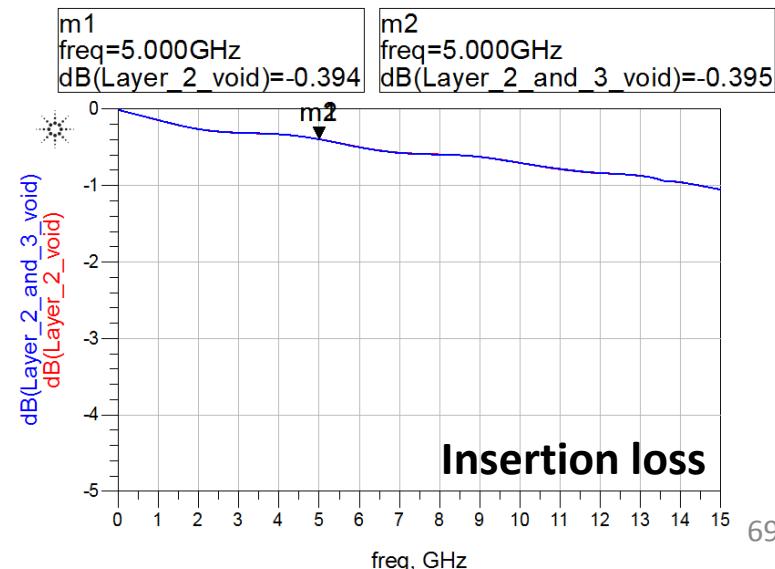
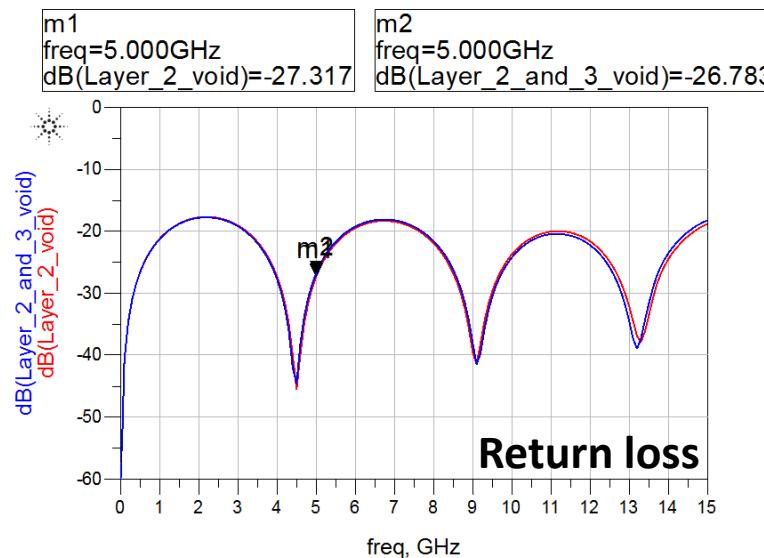
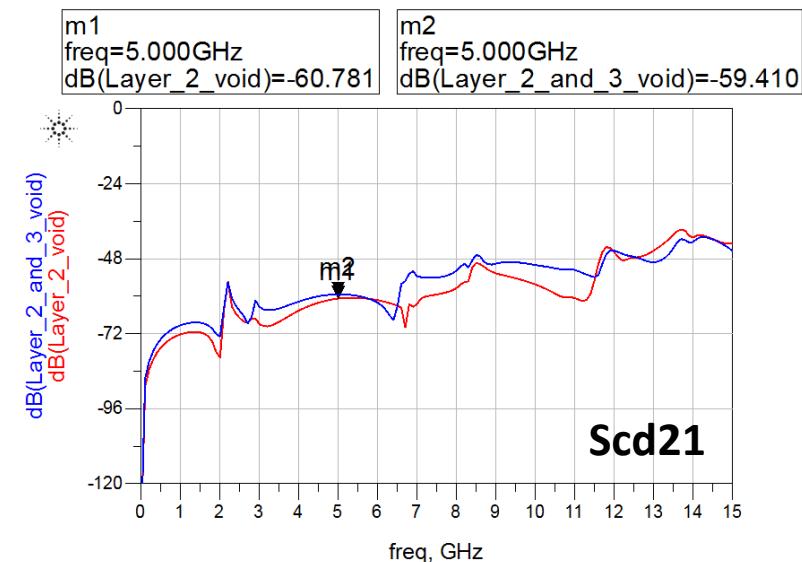
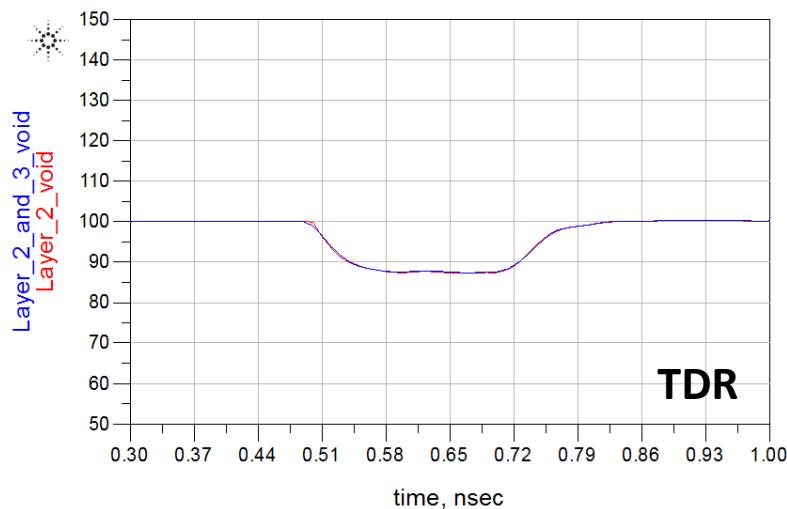
Layer 2 void



Layer 2 & 3

	Layer 2 & 3 void	Layer 2 void
a	15.75 mil	15.75 mil
b	36.42 mil	36.42 mil

GND/Reference Void for ESD

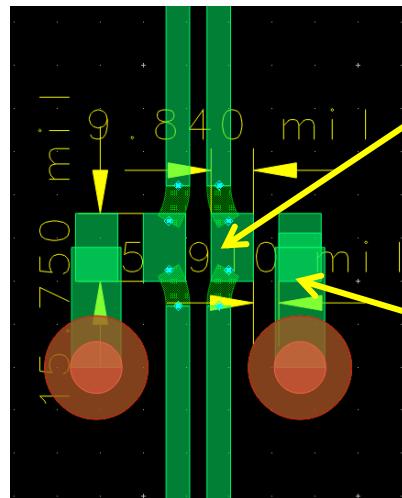


GND/Reference Void for ESD

Summary:

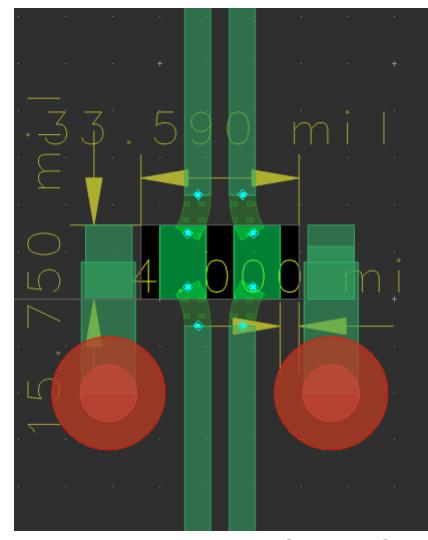
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.

GND/Reference Void for ESD

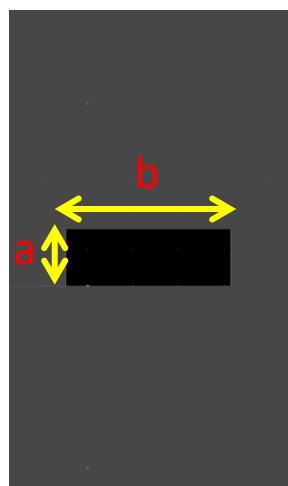


pad

Gnd



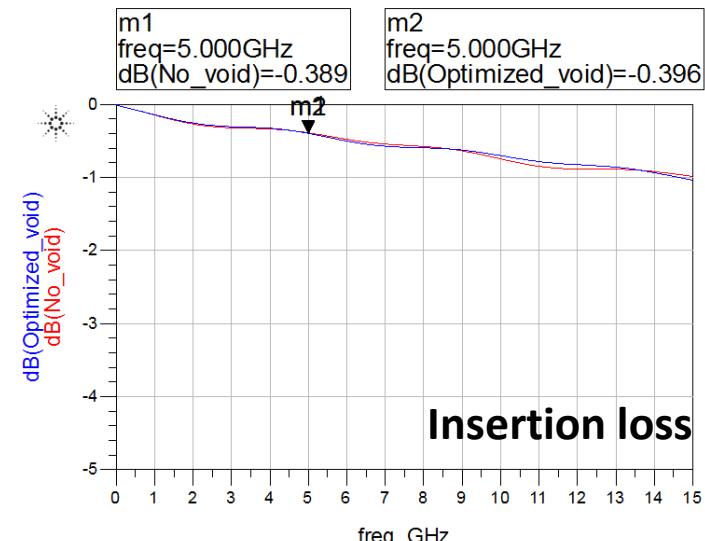
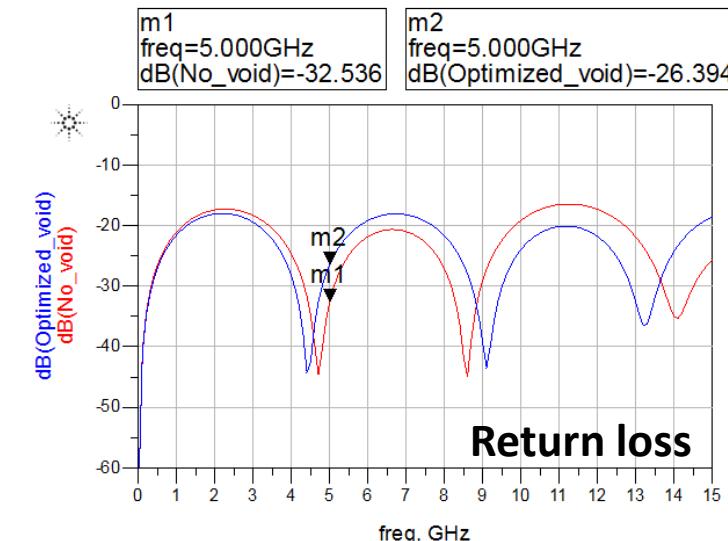
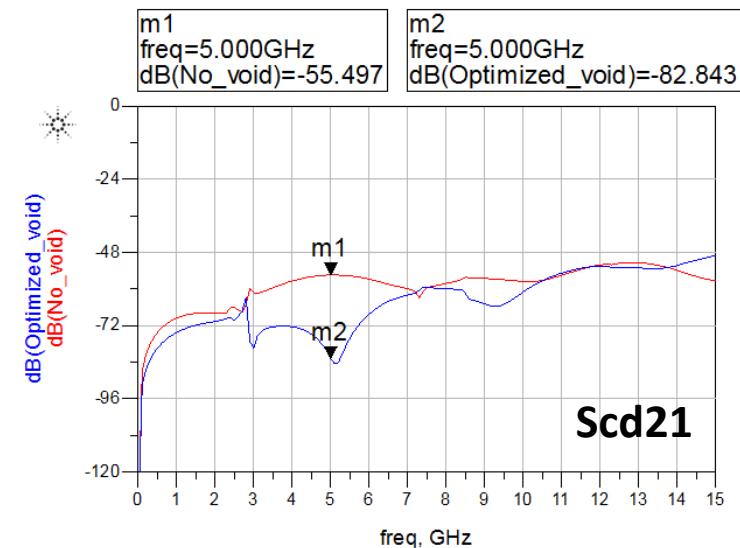
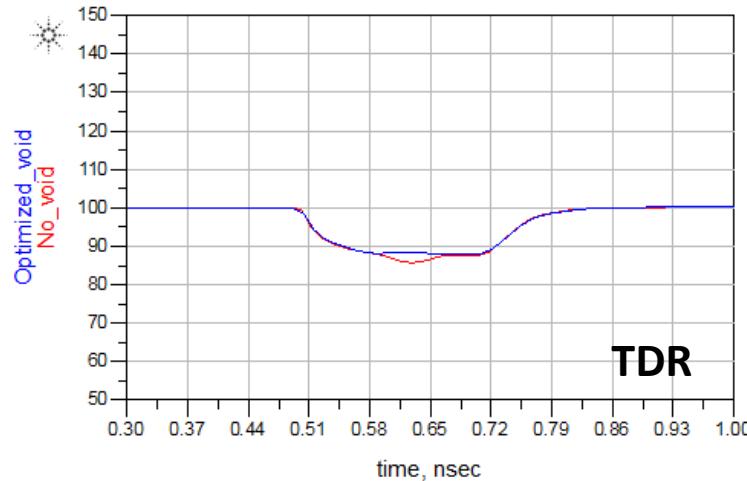
No void



void

	Optimized void	No void
a	15.75 mil	0 mil
b	33.59 mil	0 mil

GND/Reference Void for ESD

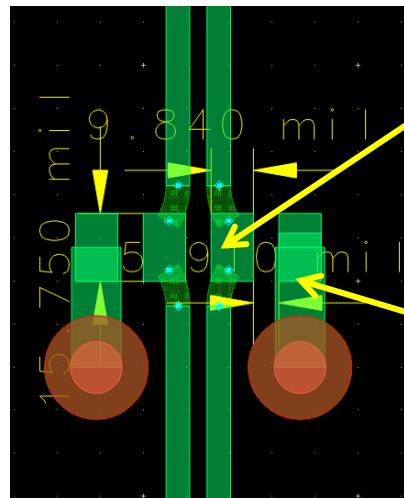


GND/Reference Void for ESD

Summary:

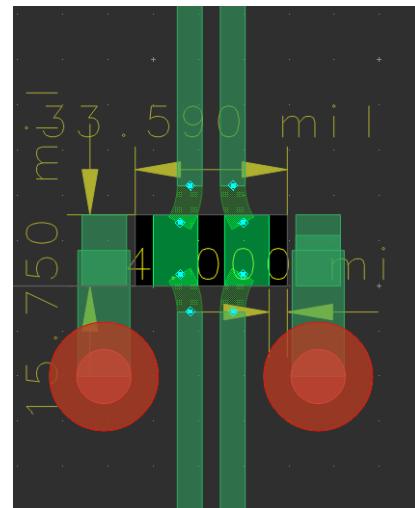
For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

GND/Reference Void for ESD

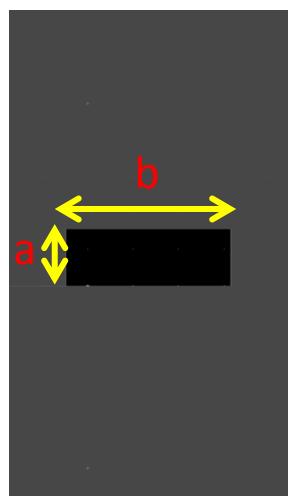
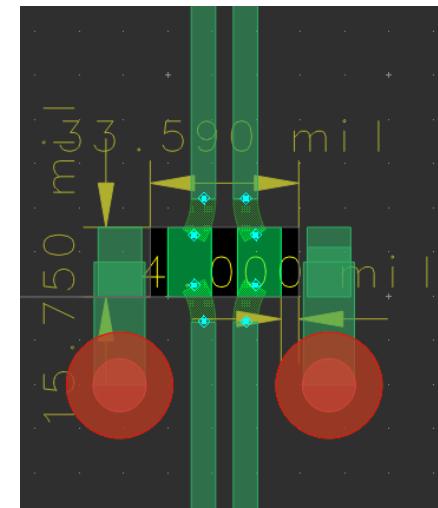


pad

Gnd



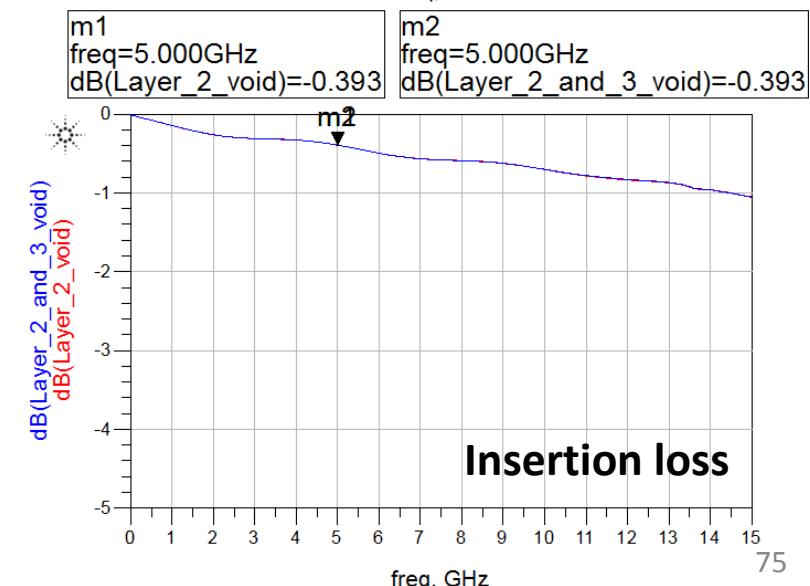
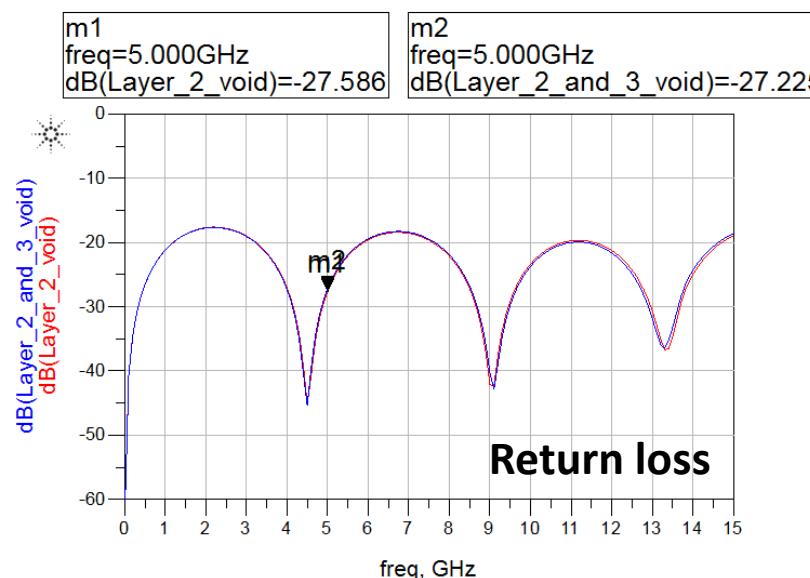
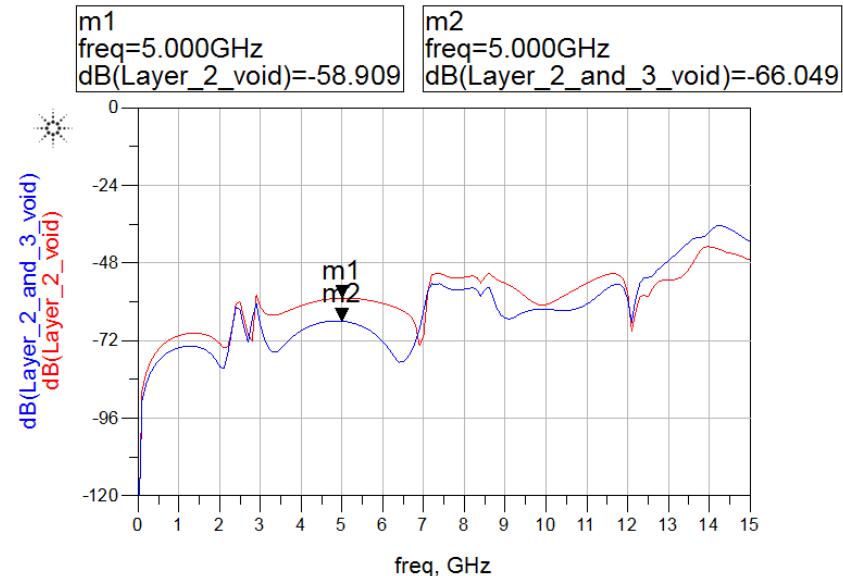
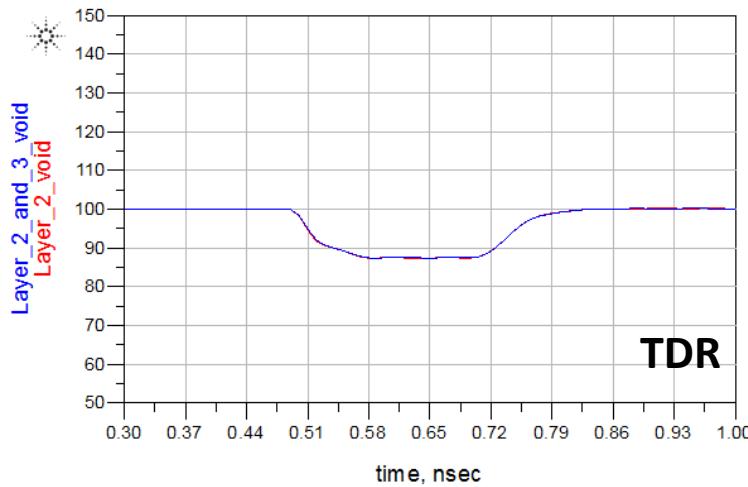
Layer 2 & 3 void
(SI suggest)



void

	Layer 2 & 3 void	Layer 2 void
a	15.75 mil	15.75 mil
b	33.59 mil	33.59 mil

GND/Reference Void for ESD



GND/Reference Void for ESD

Summary:

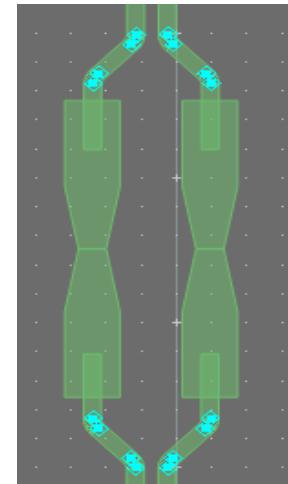
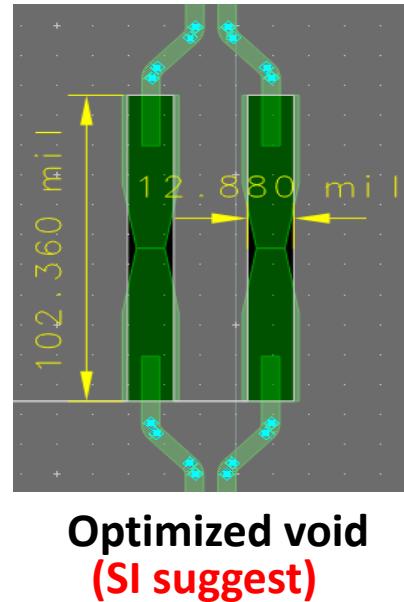
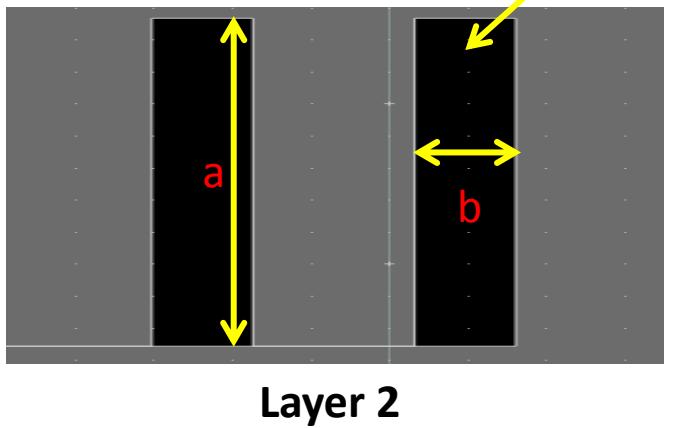
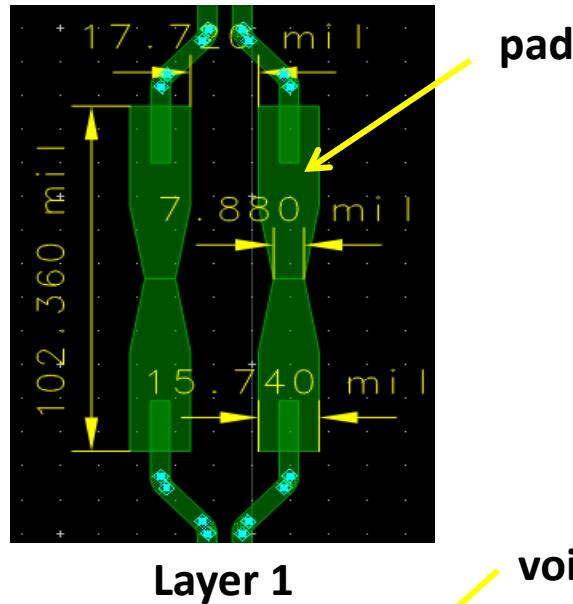
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.



Outline

- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
- **GND/Reference Void for Chock**
- GND/Reference Void for Resistors
- Balanced GND vias Vs. Unbalanced GND vias
- Distance from GND via to Signal via
- Routing: Arc Vs. 135-degree-angle

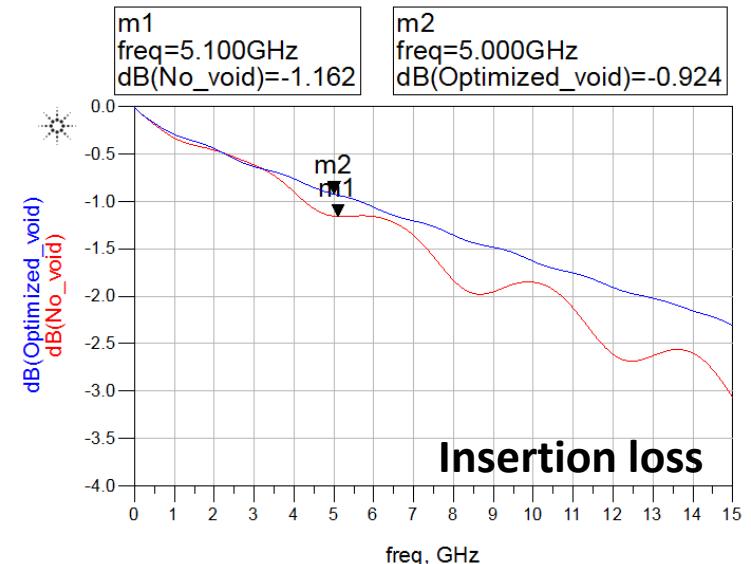
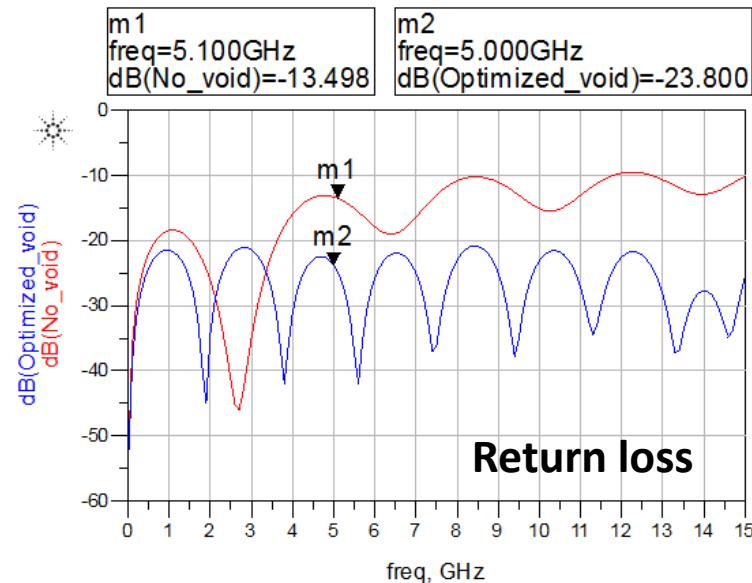
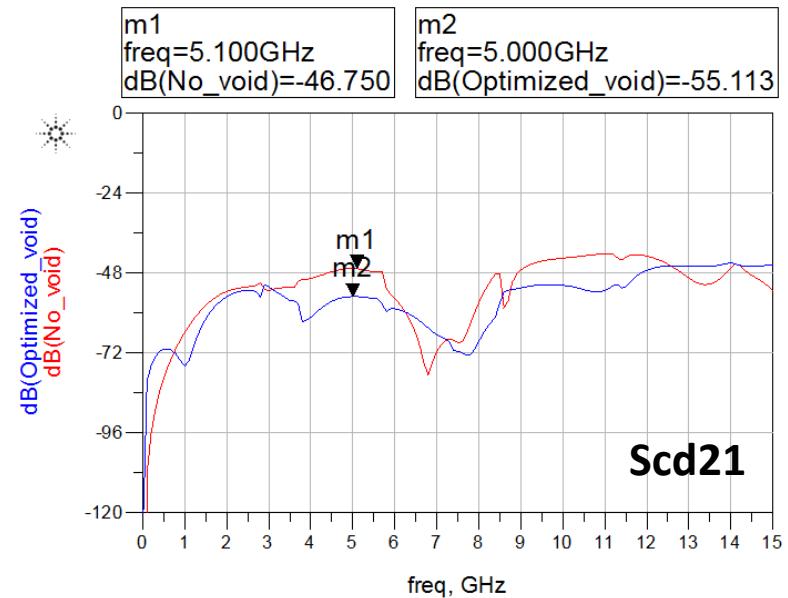
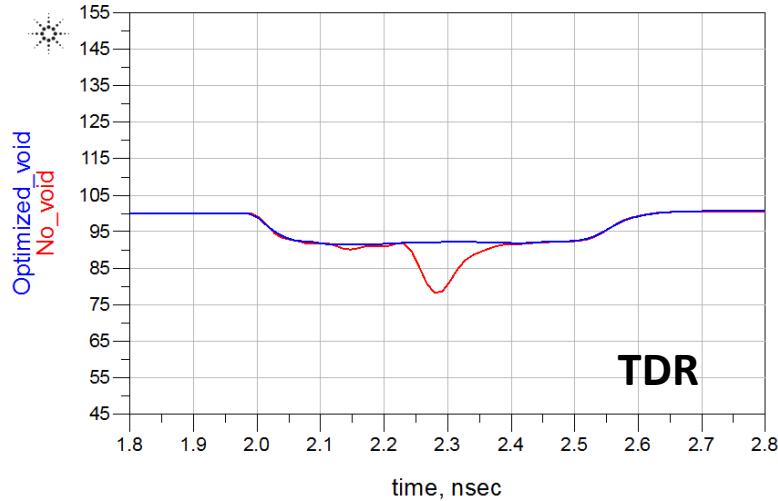
GND/Reference Void for Chock



Optimized void
(SI suggest)

	Optimized void	No void
a	102.36 mil	0 mil
b	12.88 mil	0 mil

GND/Reference Void for Chock

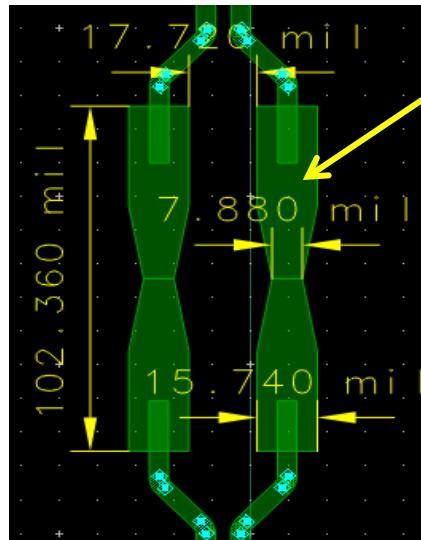


GND/Reference Void for Chock

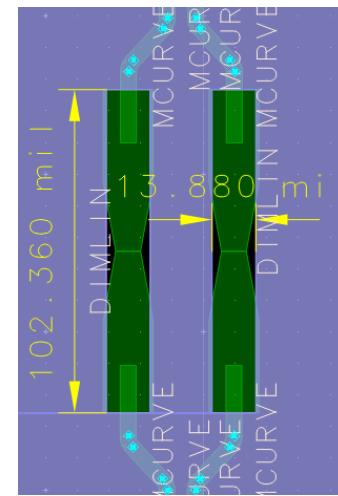
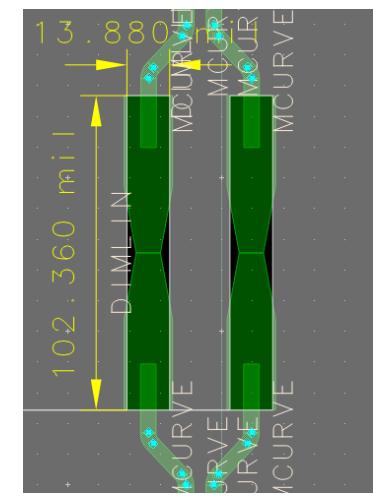
Summary:

For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

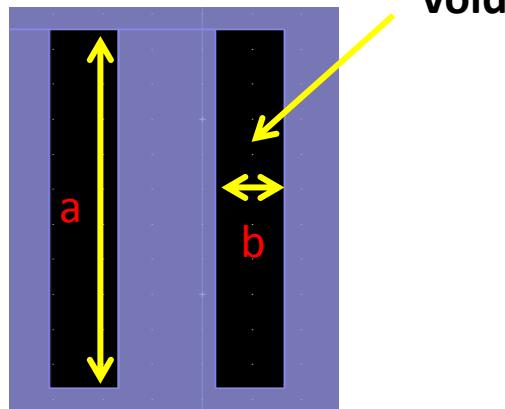
GND/Reference Void for Chock



Layer 1

Layer 2 & 3 void
(SI suggest)

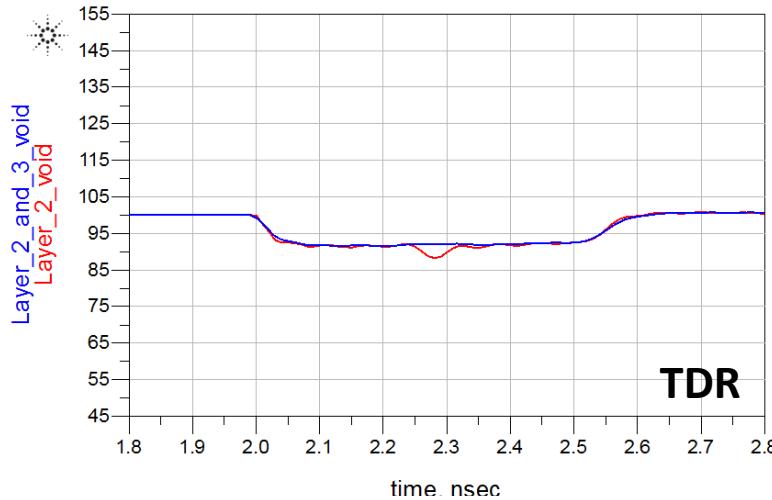
Layer 2 void



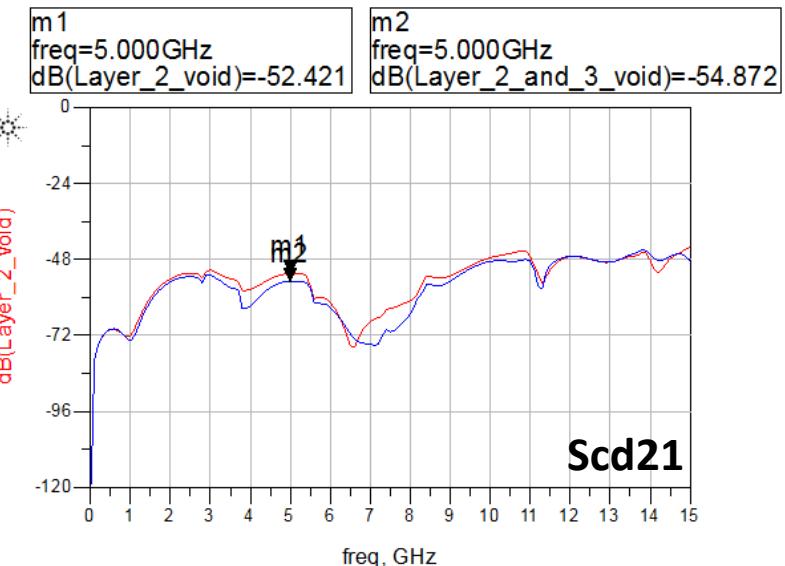
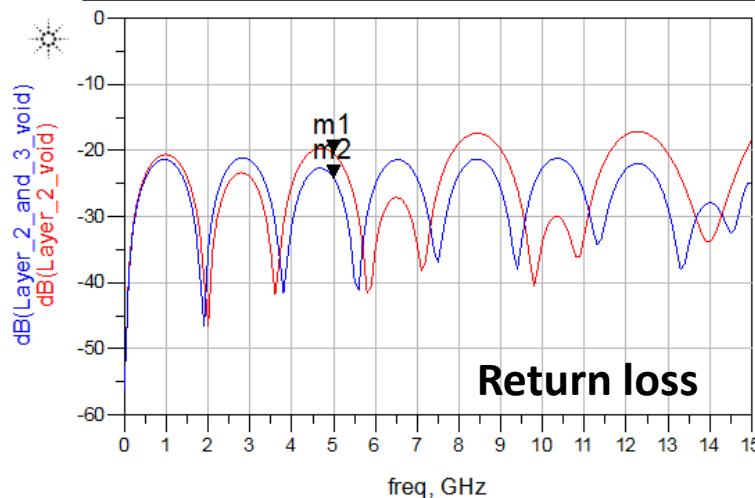
Layer 2 & 3

	Layer 2 & 3 void	Layer 2 void
a	102.36 mil	102.36 mil
b	13.88 mil	13.88 mil

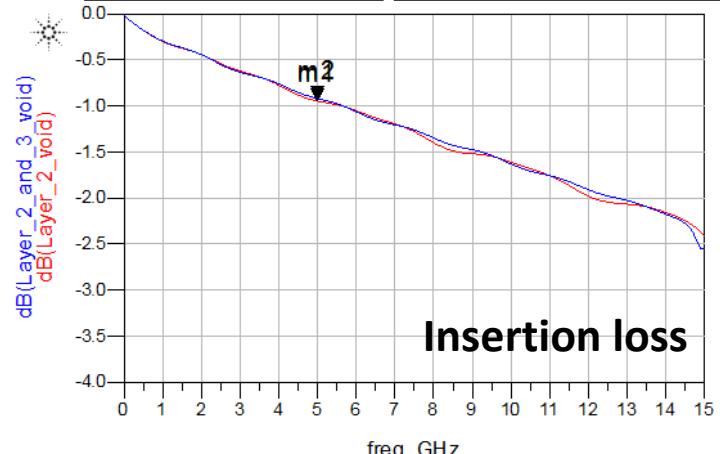
GND/Reference Void for Chock



m1 freq=5.000GHz dB(Layer_2_void)=-20.503	m2 freq=5.000GHz dB(Layer_2_and_3_void)=-24.181
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m1 freq=5.000GHz dB(Layer_2_void)=-0.947	m2 freq=5.000GHz dB(Layer_2_and_3_void)=-0.920
--	--

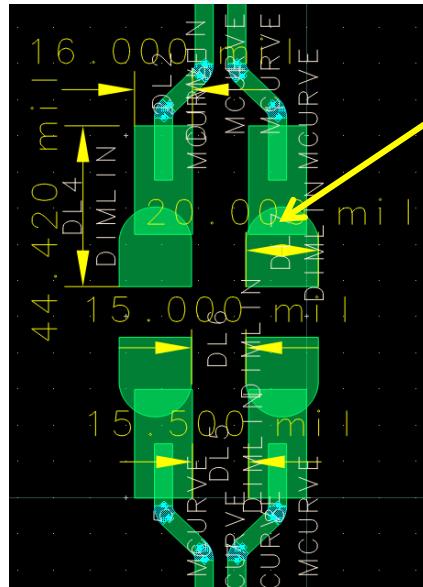


GND/Reference Void for Chock

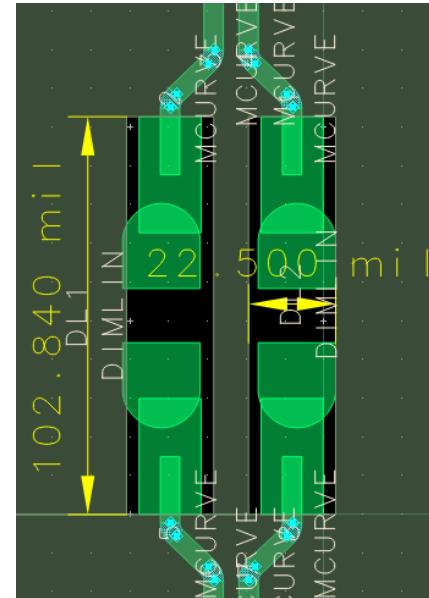
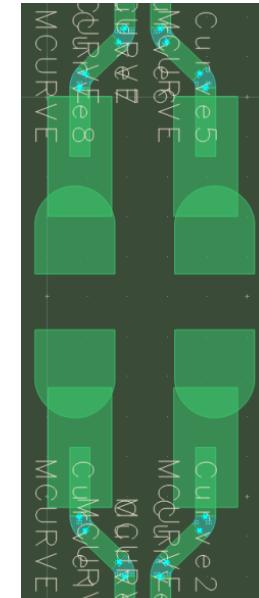
Summary:

For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.

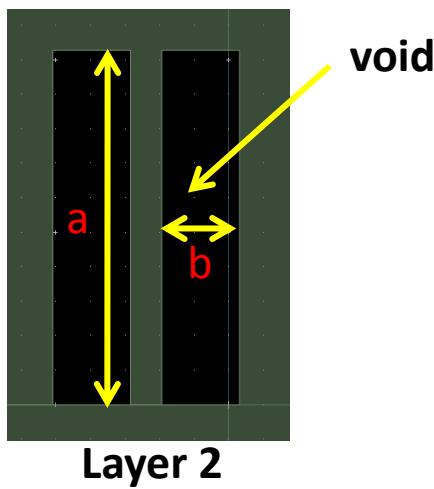
GND/Reference Void for Chock



Layer 1

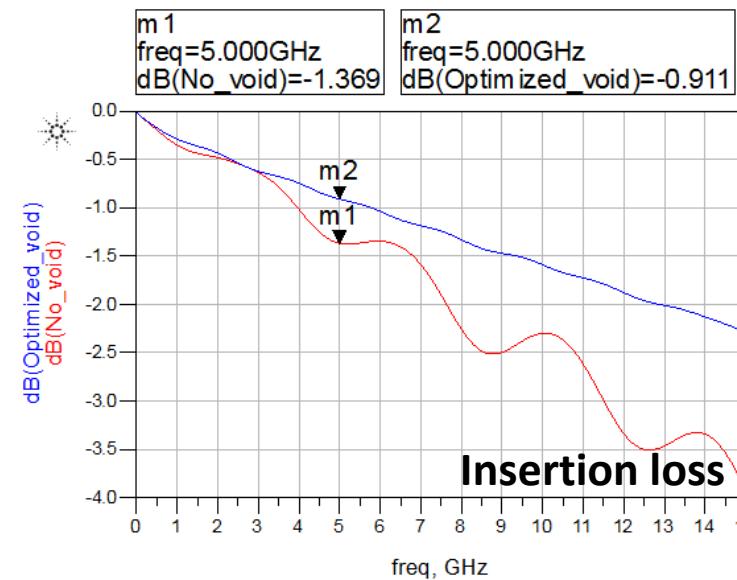
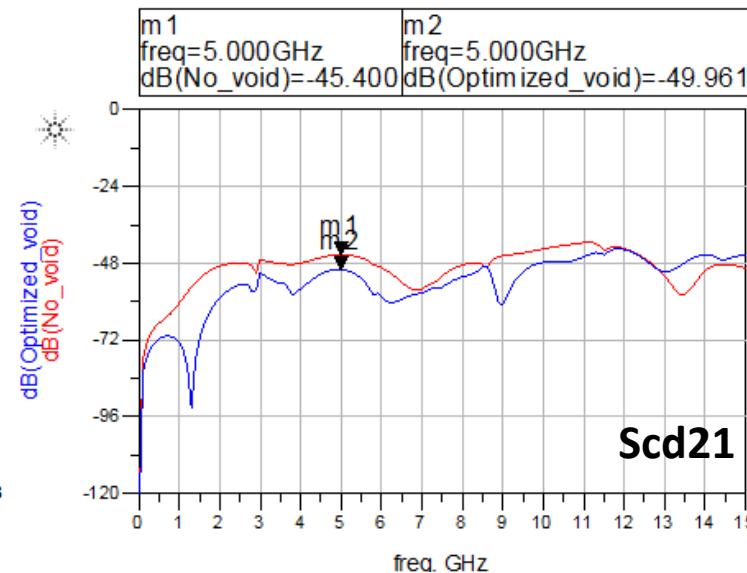
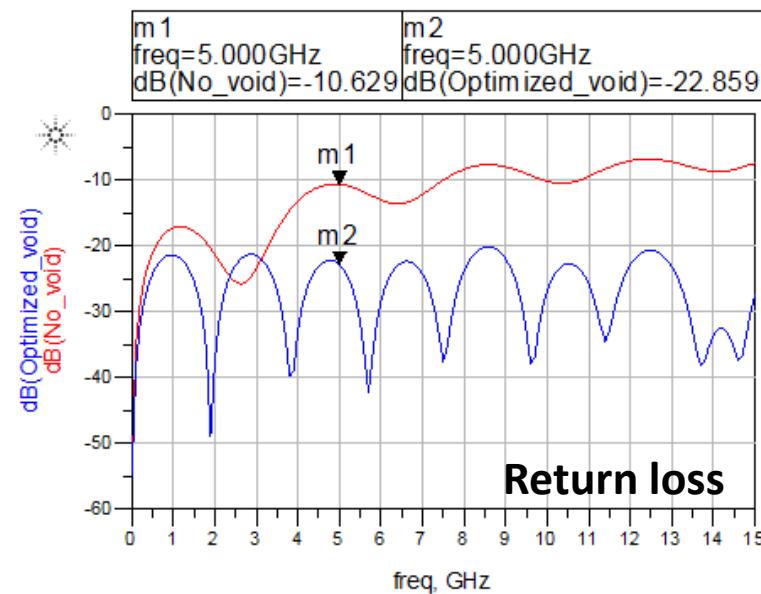
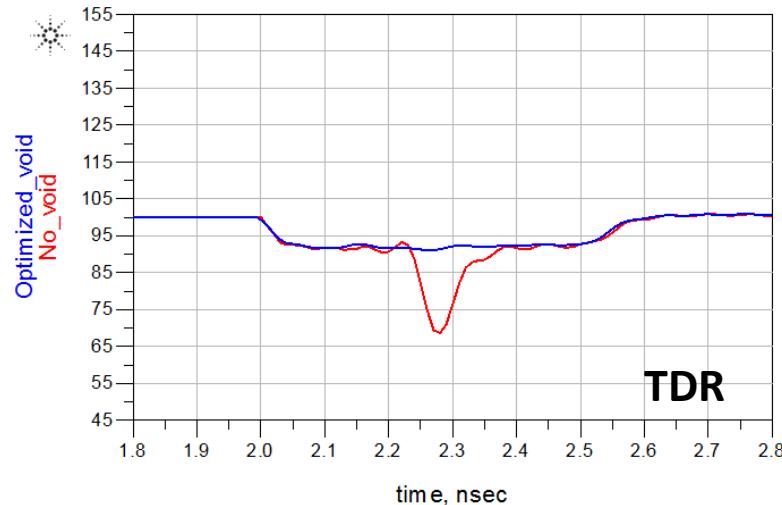
Optimized void
(SI suggest)

No void



	Optimized void	No void
a	102.84 mil	0 mil
b	22.5 mil	0 mil

GND/Reference Void for Chock

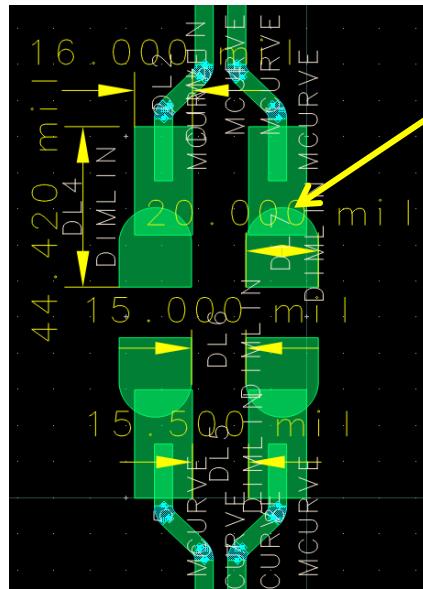


GND/Reference Void for Chock

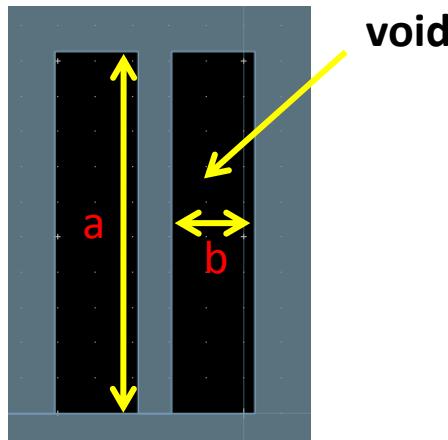
Summary:

For 4 layers board, **SI-suggested void** is better than **No void** in frequency and time domain.

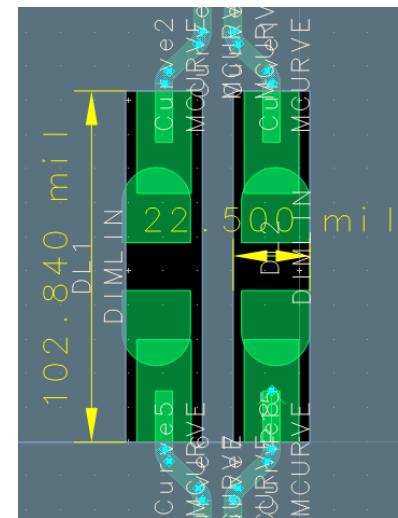
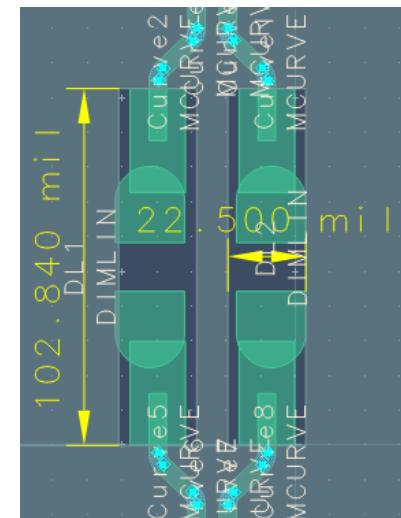
GND/Reference Void for Chock



Layer 1



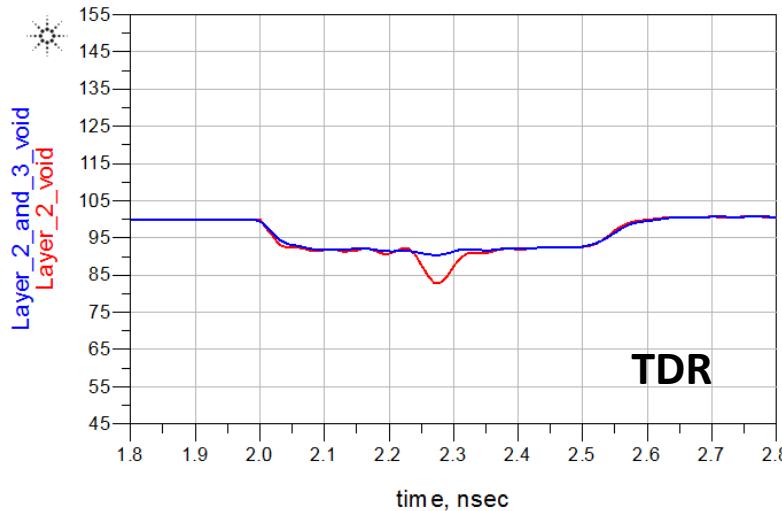
Layer 2

Layer 2 & 3 void
(SI suggest)

Layer 2 void

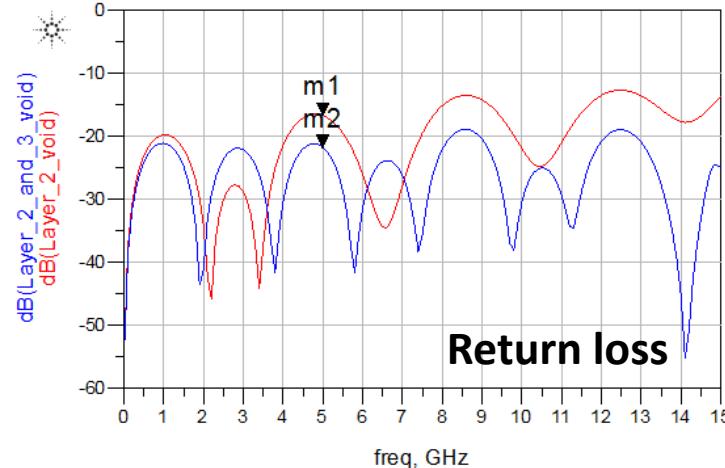
	Layer 2 & 3 void	Layer 2 void
a	102.84 mil	102.84 mil
b	22.5 mil	22.5 mil

GND/Reference Void for Chock

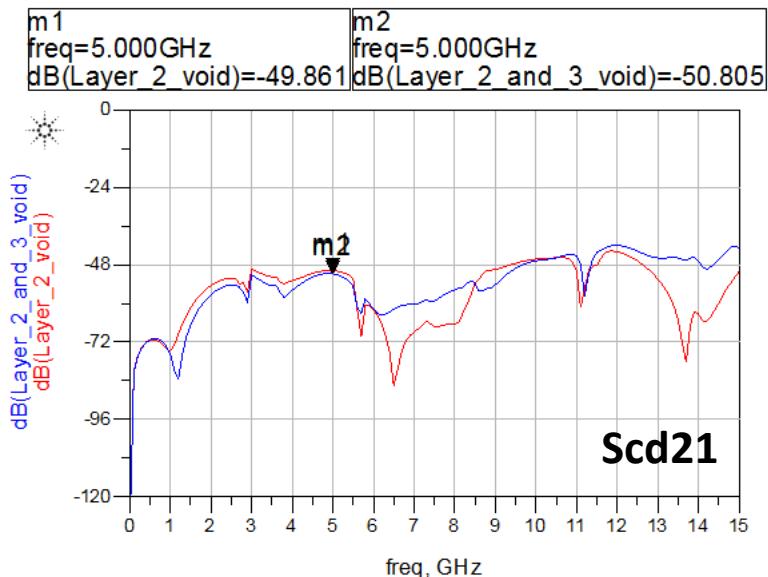


m1
freq=5.000GHz
dB(Layer_2_void)=-16.712

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-21.760



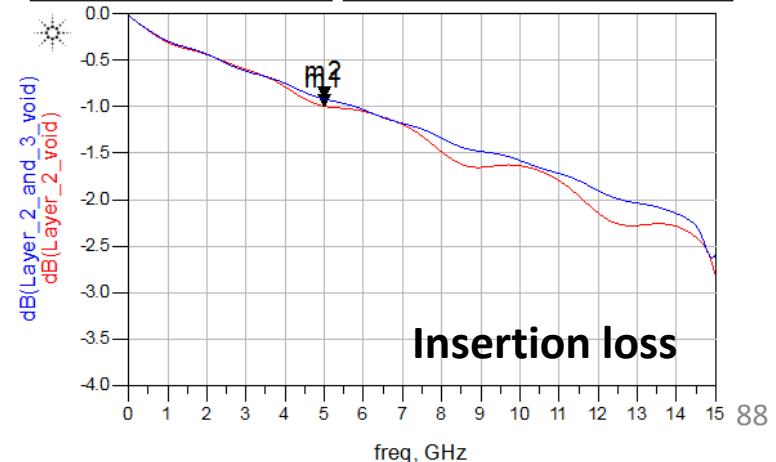
Return loss



Scd21

m1
freq=5.000GHz
dB(Layer_2_void)=-0.996

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-0.919



Insertion loss

GND/Reference Void for Chock

Summary:

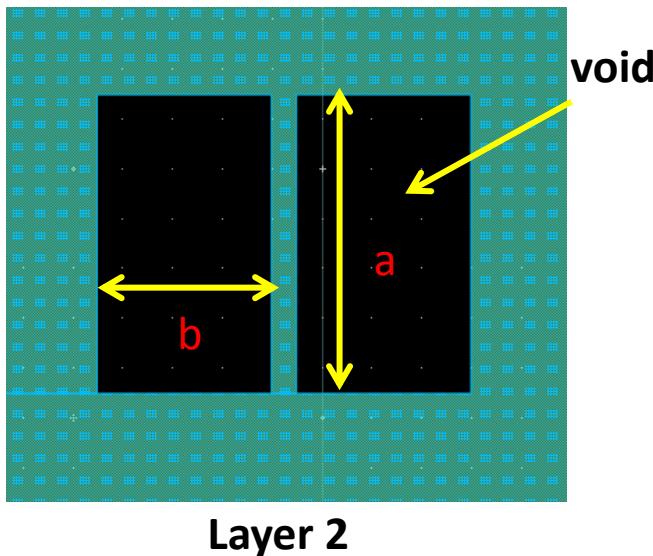
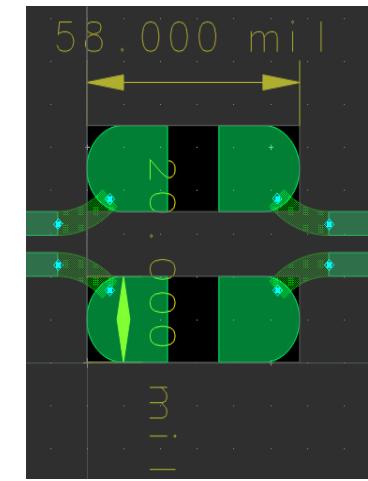
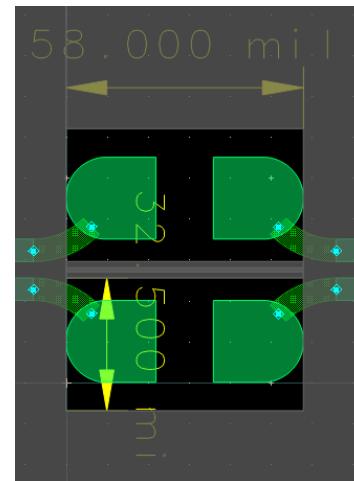
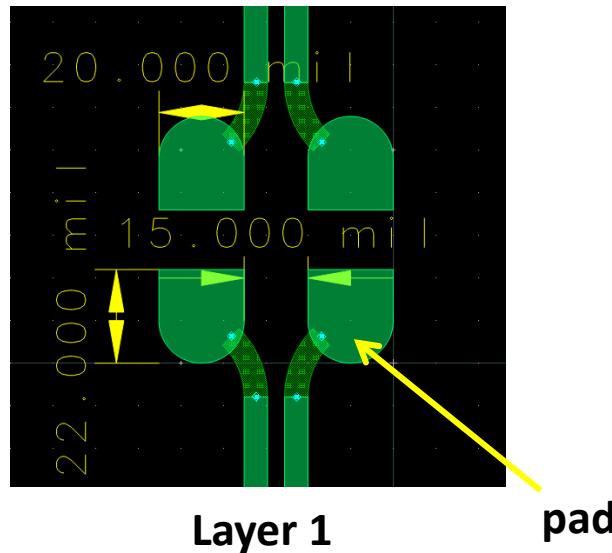
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.



Outline

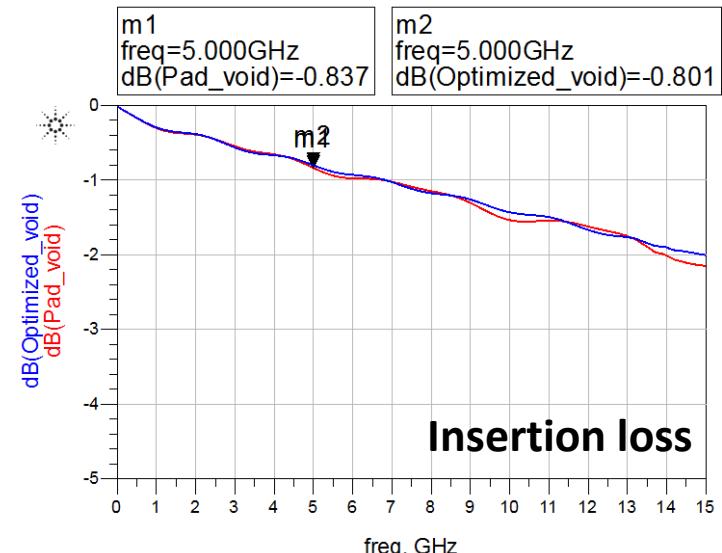
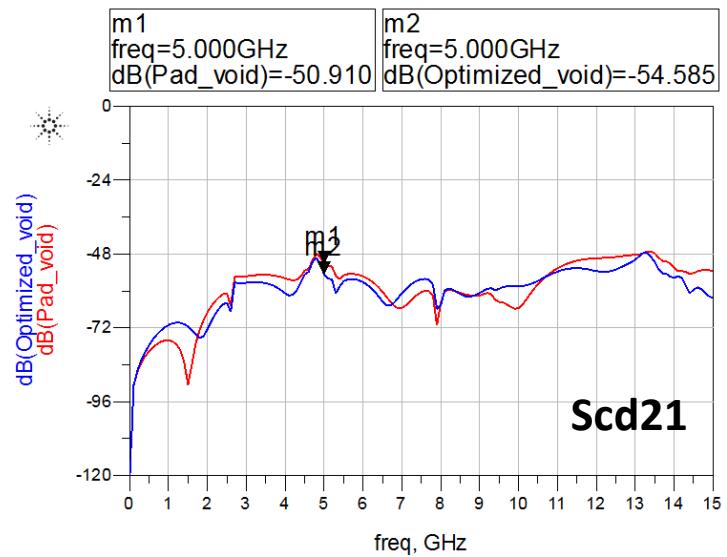
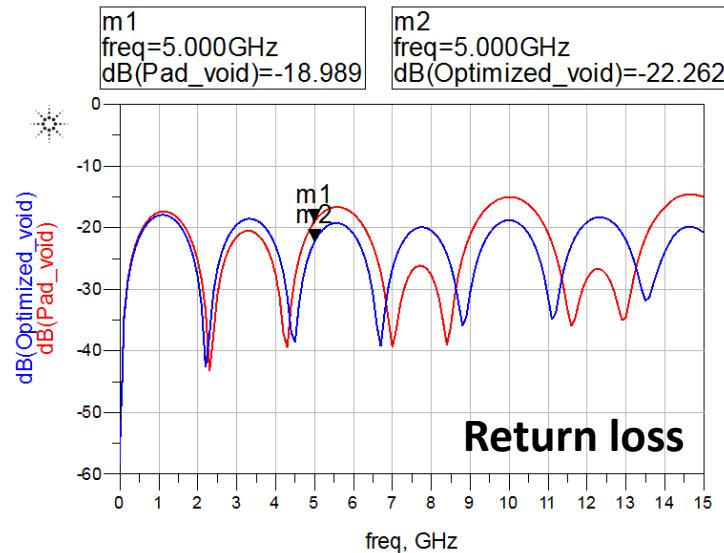
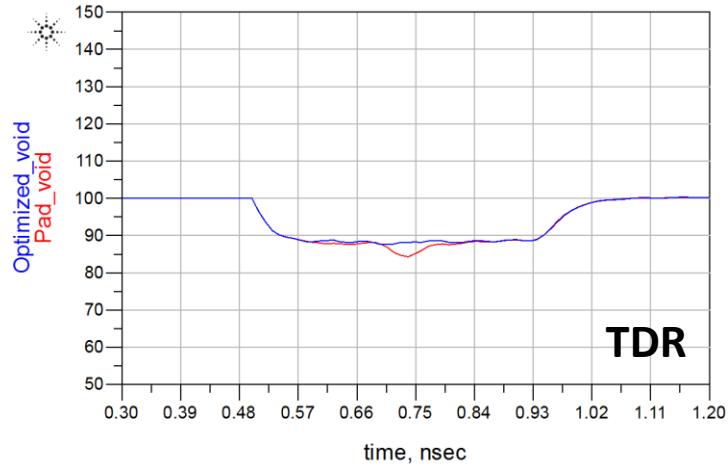
- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
- GND/Reference Void for Chock
- **GND/Reference Void for Resistors**
- Balanced GND vias Vs. Unbalanced GND vias
- Distance from GND via to Signal via
- Routing: Arc Vs. 135-degree-angle

GND/Reference Void for Resistors



	Optimized void	Pad void
a	58 mil (0402)	58 mil (0402)
b	32.5 mil	20 mil

GND/Reference Void for Resistors

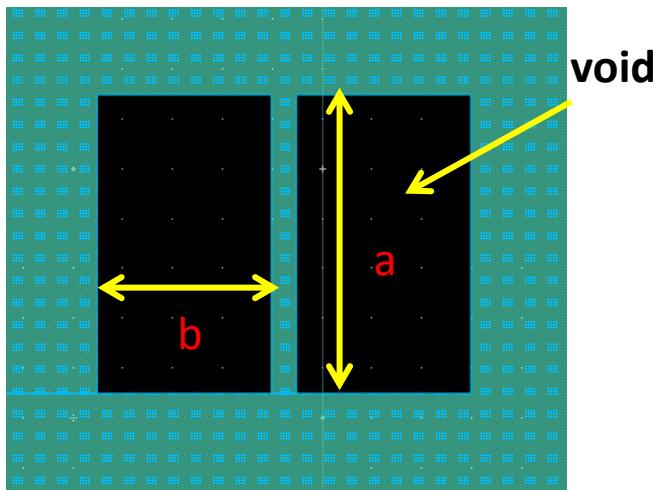
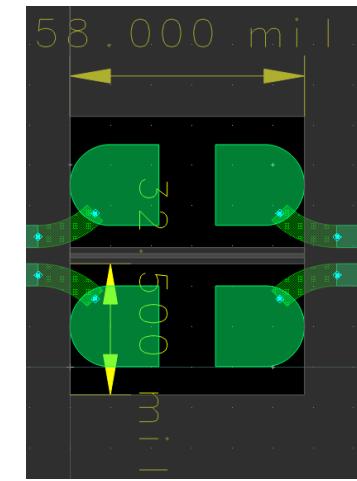
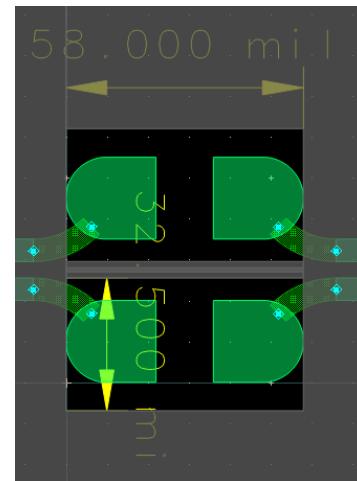
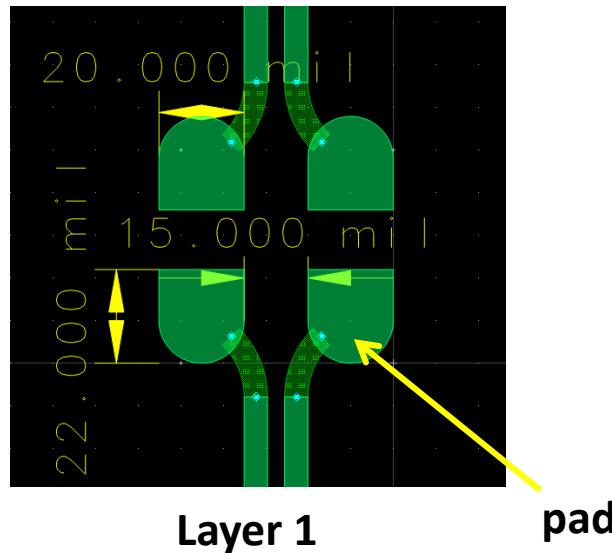


GND/Reference Void for Resistors

Summary:

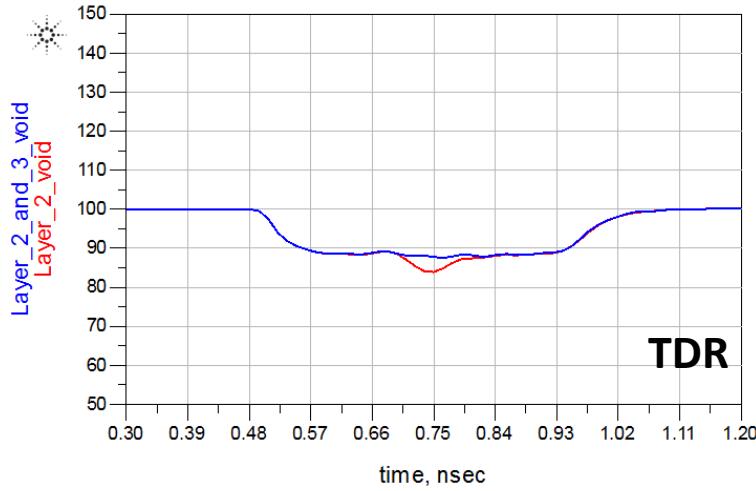
For 4 layers board, **SI-suggested void** is better than **Pad void** in frequency and time domain.

GND/Reference Void for Resistors



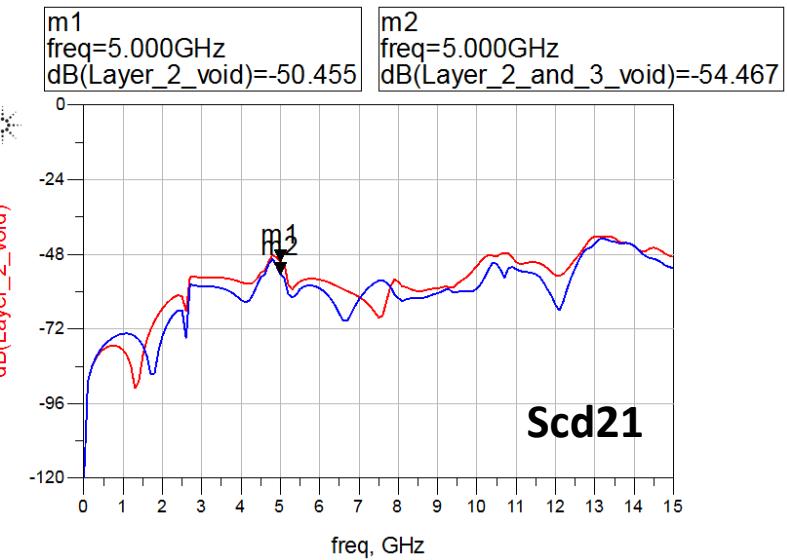
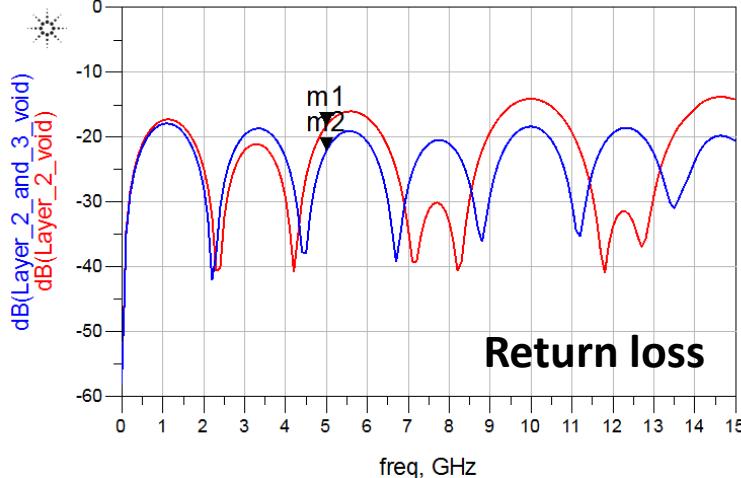
	Layer 2 & 3 void	Layer 2 void
a	58 mil (0402)	58 mil (0402)
b	32.5 mil	32.5 mil

GND/Reference Void for Resistors



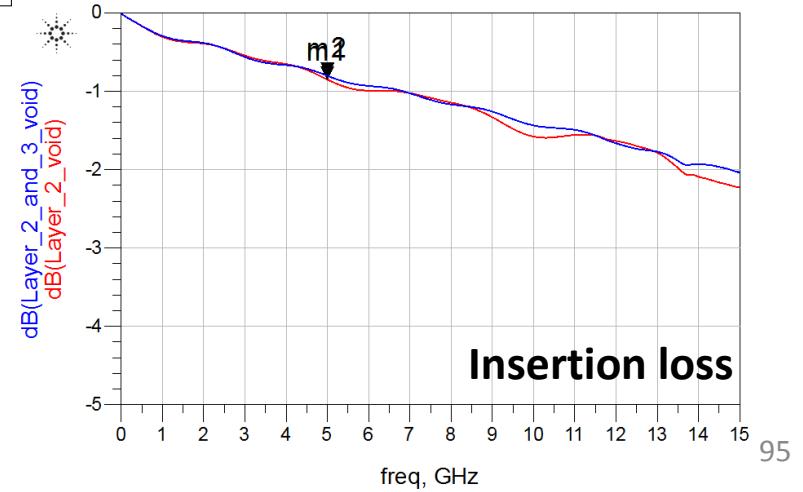
m1
freq=5.000GHz
dB(Layer_2_void)=-18.206

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-22.036



m1
freq=5.000GHz
dB(Layer_2_void)=-0.851

m2
freq=5.000GHz
dB(Layer_2_and_3_void)=-0.802



GND/Reference Void for Resistors

Summary:

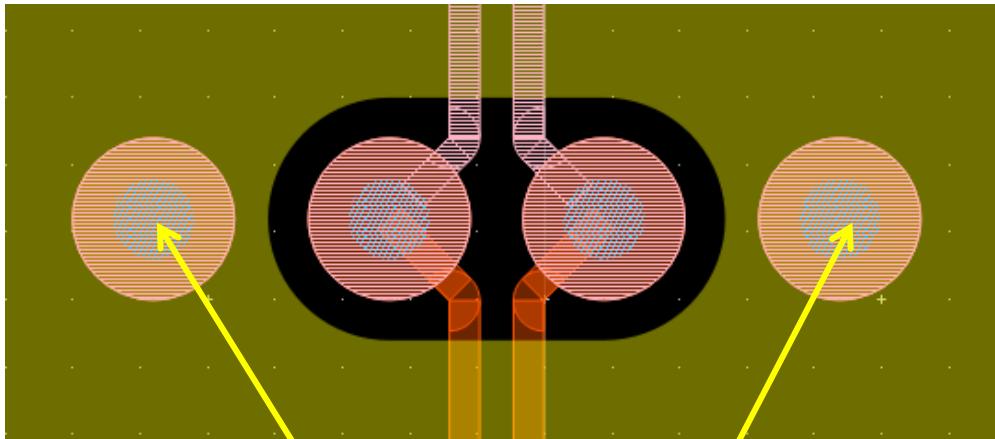
For 6 layers board, **SI-suggested void** is better than **Layer 2 void** in frequency and time domain.



Outline

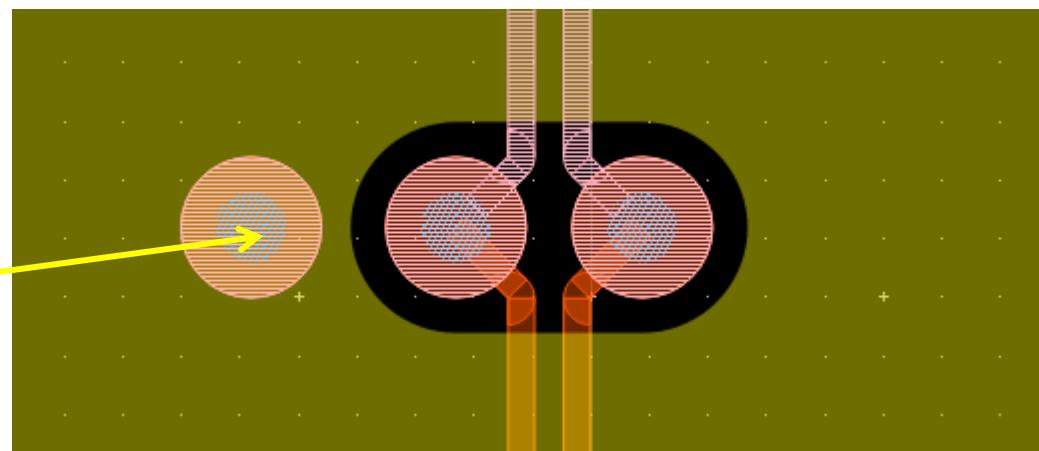
- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
- GND/Reference Void for Chock
- GND/Reference Void for Resistors
- **Balanced GND vias Vs. Unbalanced GND vias**
- Distance from GND via to Signal via
- Routing: Arc Vs. 135-degree-angle

Balanced GND vias Vs. Unbalanced GND vias



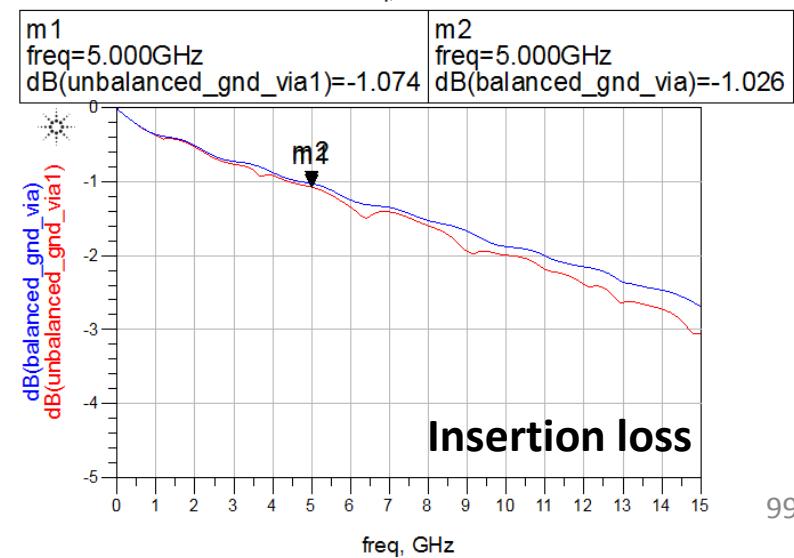
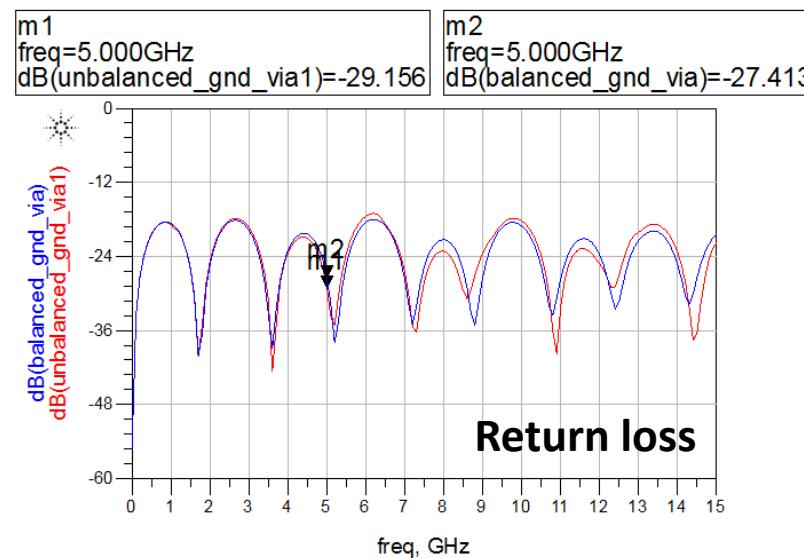
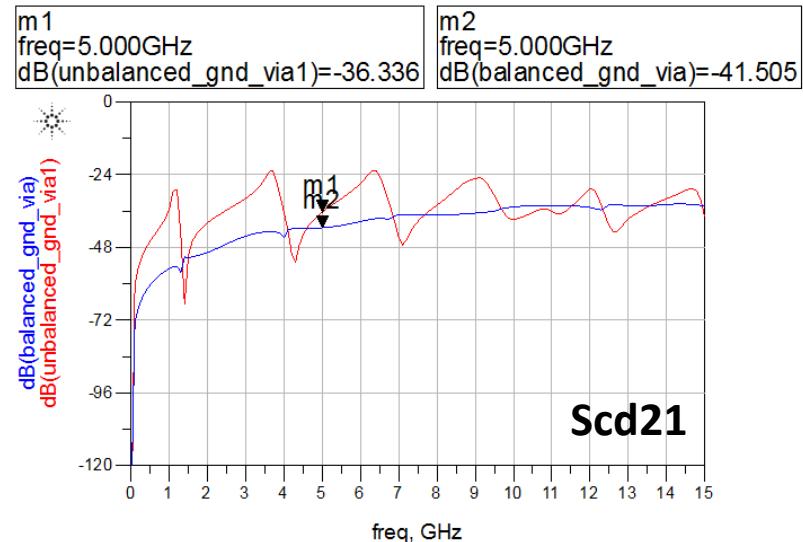
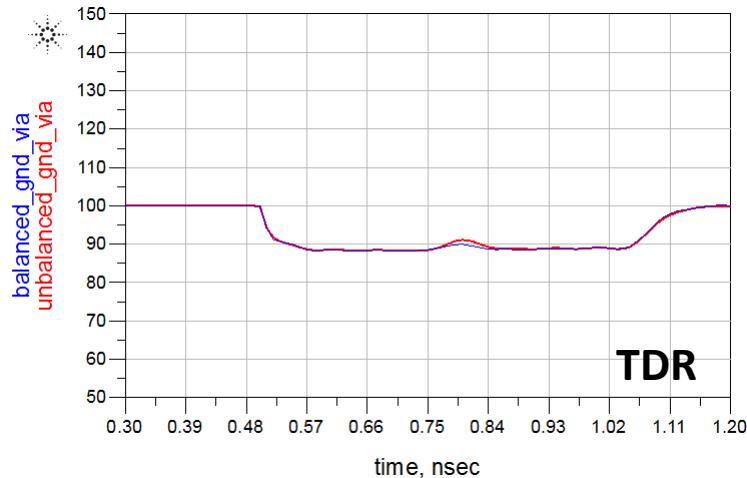
Balanced GND vias
(SI suggest)

GND via



Unbalanced GND vias

Balanced GND vias Vs. Unbalanced GND vias



Balanced GND vias Vs. Unbalanced GND vias

Summary:

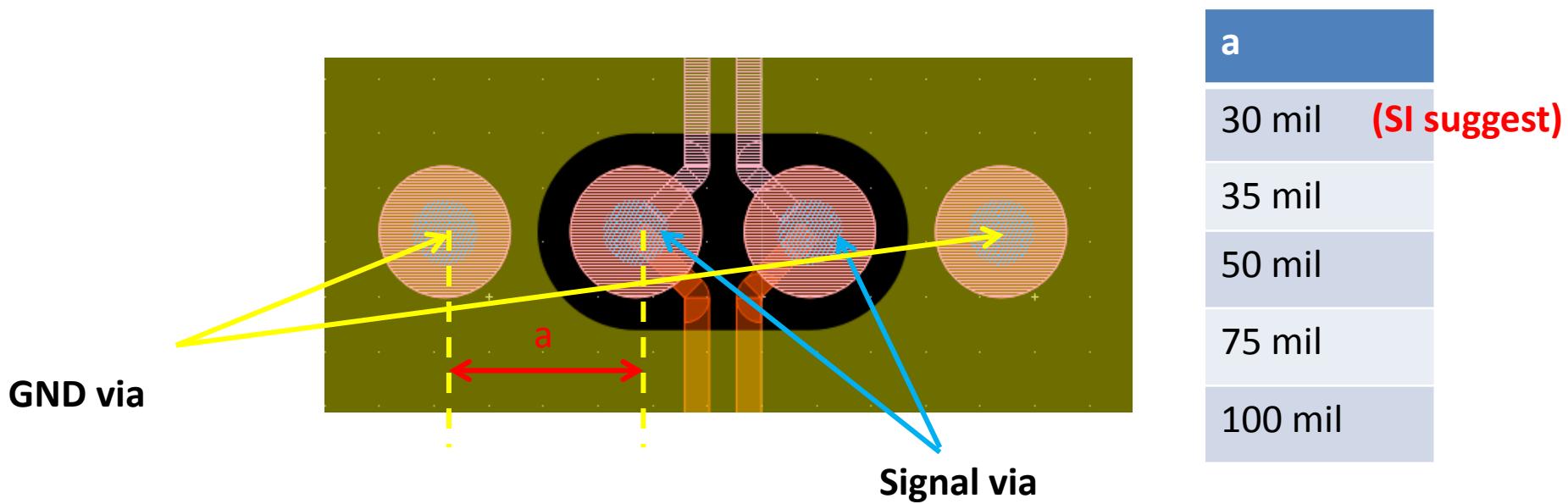
For 4 layers board, **Balanced GND vias** is smaller than **Unbalanced GND vias** in Scd21.



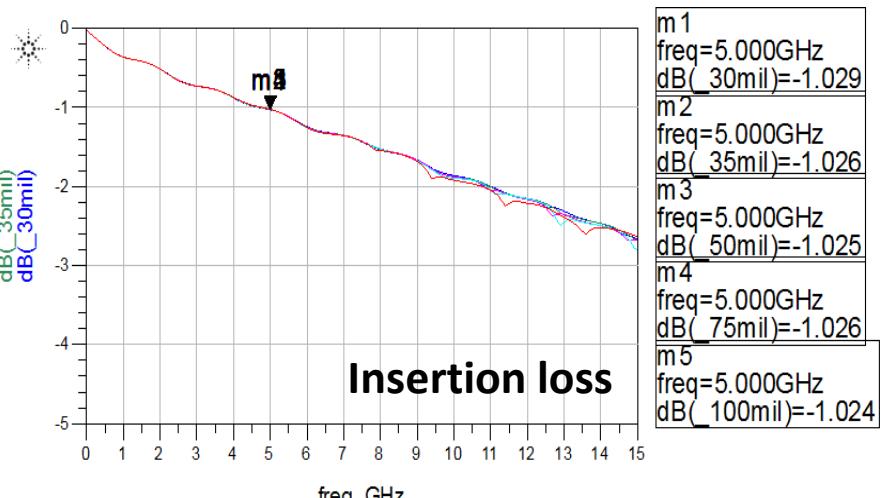
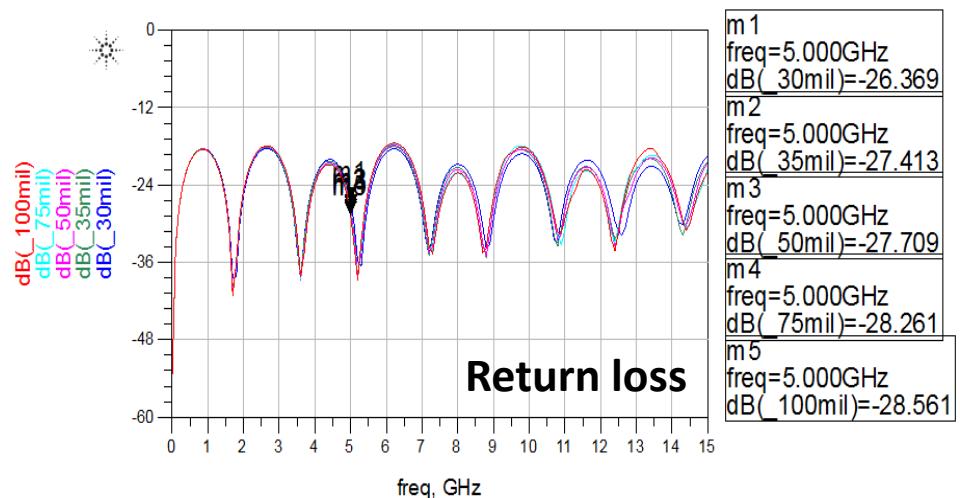
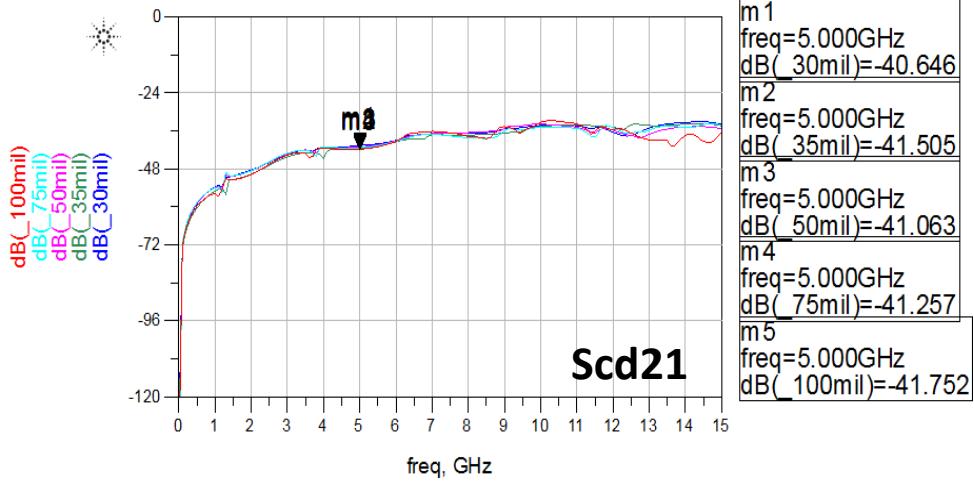
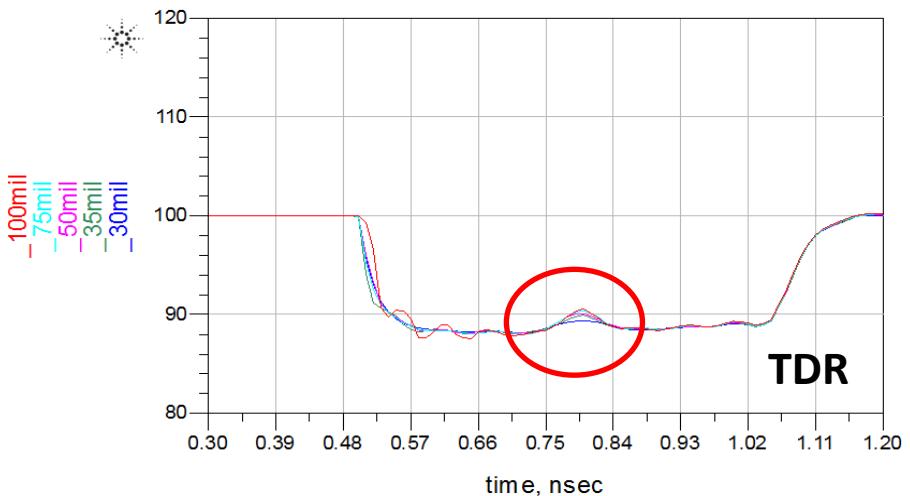
Outline

- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
- GND/Reference Void for Chock
- GND/Reference Void for Resistors
- Balanced GND vias Vs. Unbalanced GND vias
- Distance from GND via to Signal via
- Routing: Arc Vs. 135-degree-angle

Distance from GND via to Signal via



Distance from GND via to Signal via



Distance from GND via to Signal via

Summary:

For 4 layers board, impedance increase with distance between **GND via** and **Signal via** increasing in time domain.



Outline

- Stack up (based on ASM EV/demo boards)
- GND/Reference Void for Micro-B
- GND/Reference Void for Capacitors
- GND/Reference Void for Differential vias
- GND/Reference Void for Type-C
- GND/Reference Void for ESD
- GND/Reference Void for Chock
- GND/Reference Void for Resistors
- Balanced GND vias Vs. Unbalanced GND vias
- Distance from GND via to Signal via
- **Routing: Arc Vs. 135-degree-angle**

Routing: Arc Vs. 135-degree-angle

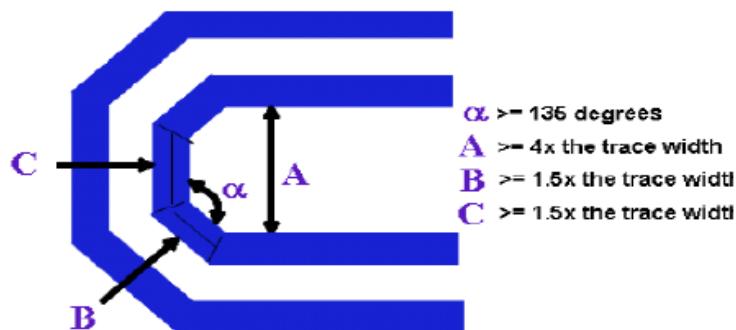
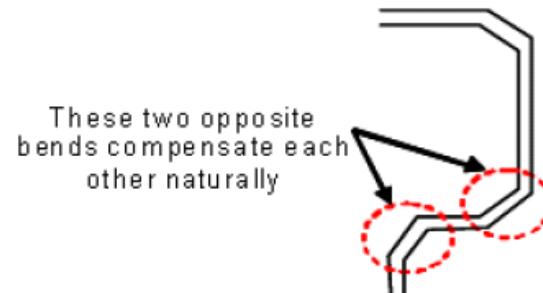
Bending Rules

The differential signals need to maintain 180 degree out of phase, otherwise some of the energy is converted to common mode and radiate.

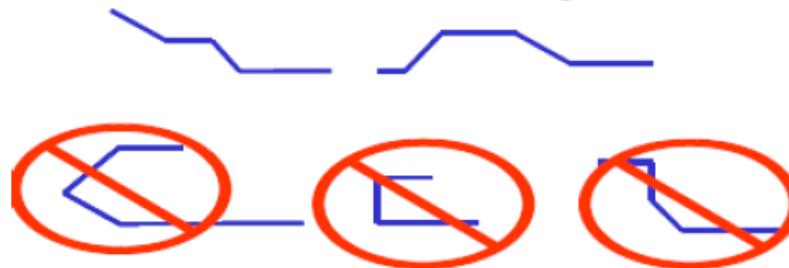
Maintain symmetrical routing

Avoid bends

- Otherwise, make the bend angle > 135 degree
- Match the number of left bends to the number of right bends for length



Preferred - Not Considered “Tight Bends”



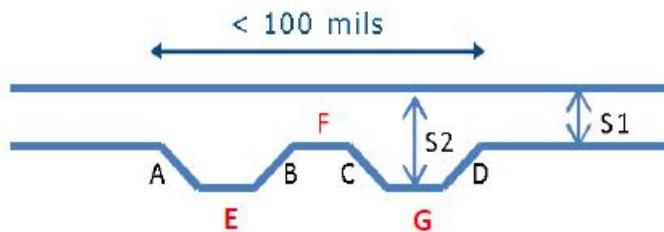
Avoid! -“Tight Bends”

Routing: Arc Vs. 135-degree-angle

Serpentine Routing Rule

Total length mismatch < 15 mil

- The length matching compensation should be made as close as possible to the point where the length variation occurs.



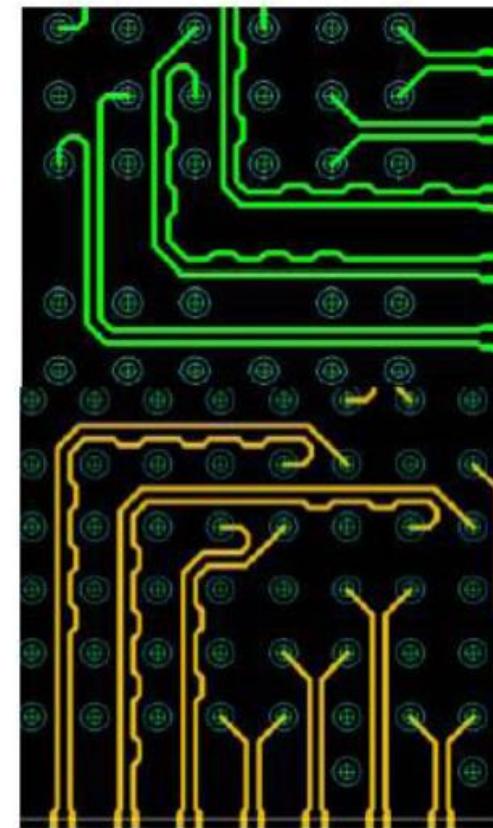
$$A=B=C=D$$

$$E=F=G=3W \text{ (} W = \text{trace width})$$

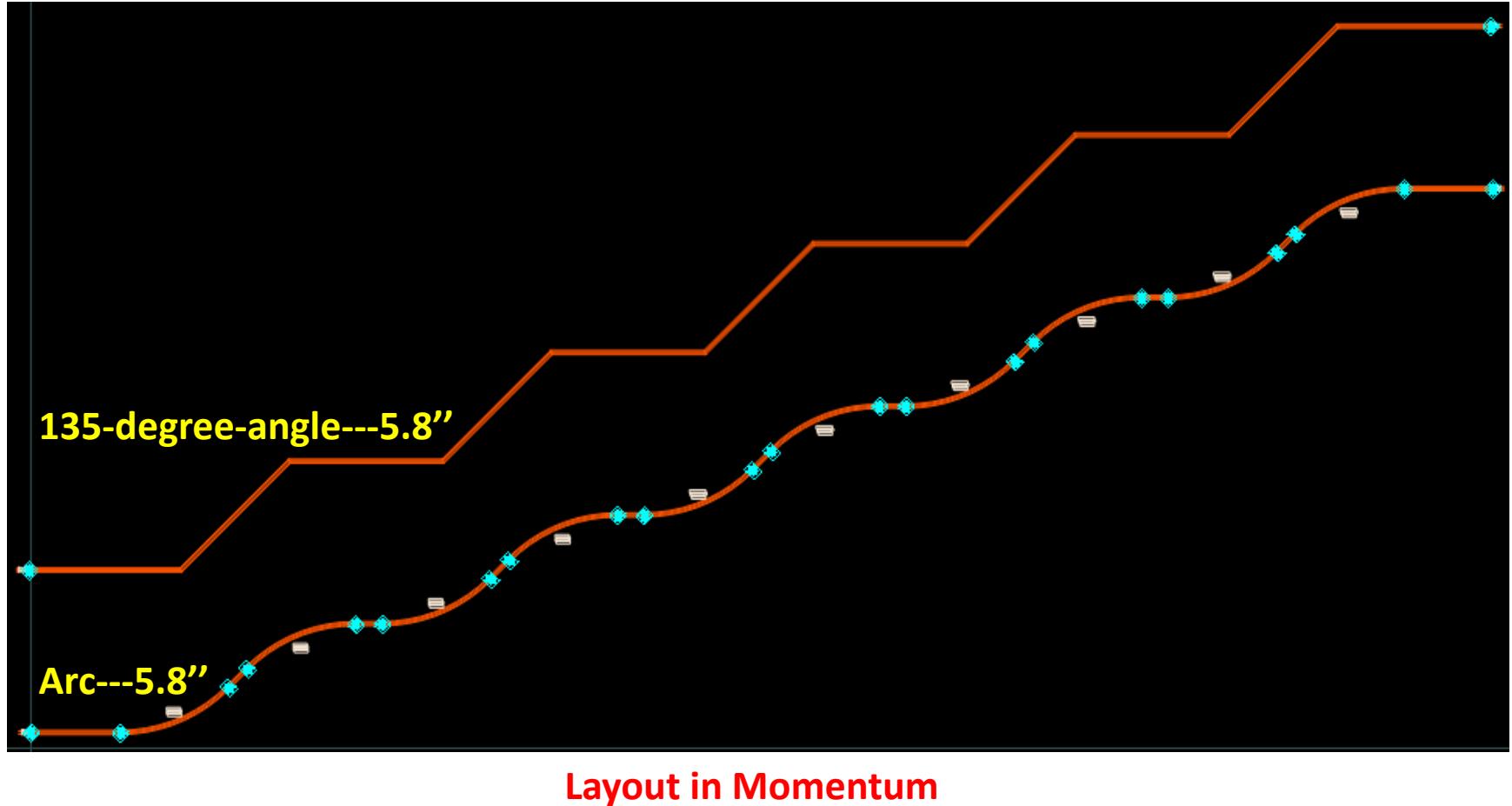
Length < 100 mils

45 degree bend

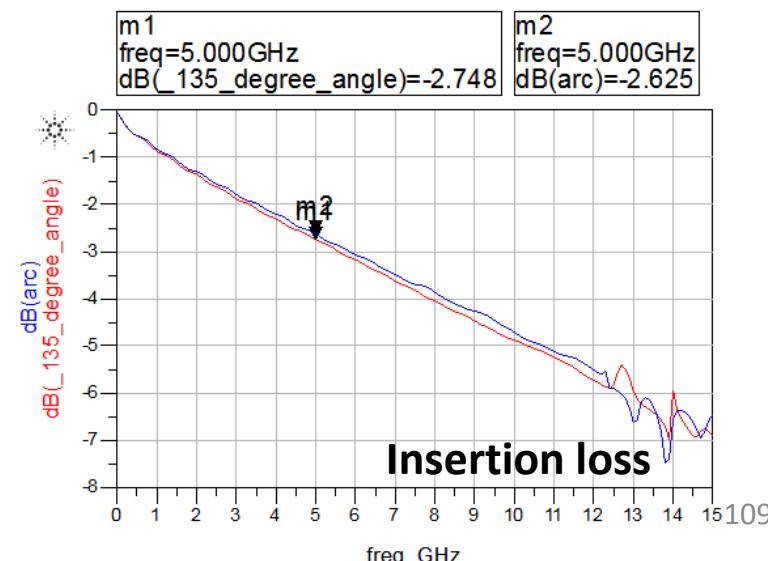
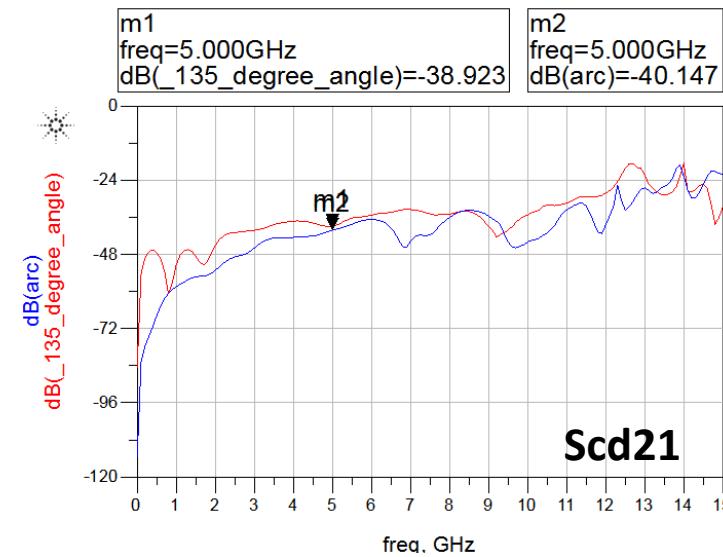
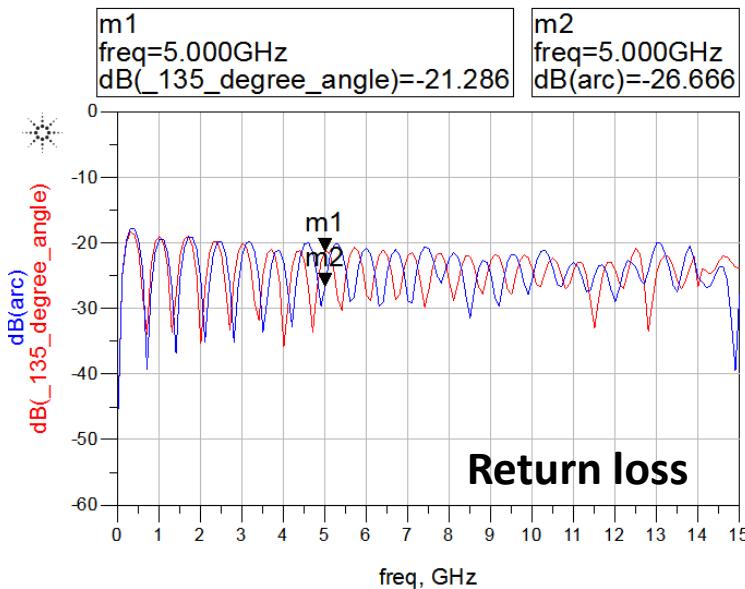
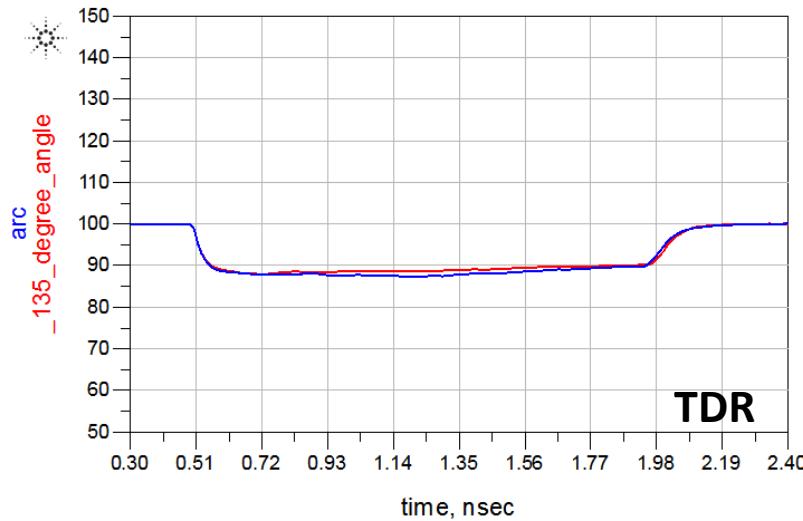
$S2 < 2 * S1$



Routing: Arc Vs. 135-degree-angle



Routing: Arc Vs. 135-degree-angle



Routing: Arc Vs. 135-degree-angle

Summary:

For 4 layers board, Arc is better than 135-degree-angle in frequency and time domain.

Reference

- *USB 3.1 Electrical Design*, USB 3.1 –1.0 Release Seminar, December 11, 2013.