Vienna University of Technology

Implementation report

Laboratory integrated circuits - Frequency Modulation

Group 4

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May 26, 2017

1 Introduction

Out task was to implement frequency modulation using the *sine_cordic* component we developed in the first task. The amplitude value of the input modulation signal had to be read from the ADC of the Xilinx board. Internally we generated a carrier signal with a rest frequency of 1 kHz. We altered the frequency of the carrier signal according to the amplitude of the input signal. We then wrote the carrier signal to the DAC to convert the signal back to an analog wave.

1.1 Frequency Modulation

Frequency modulation works by transmitting information in the form of altering a signals frequency as pictured in figure 1. The formula we used for this purpose was: $A_c sin(2\pi[f_c + f_d A_m sin(f_m 2\pi)])$

The meaning of the variables is explained in table 1.

2 Implementation

We structured our implementation in various components to keep the design modular and to lower complexity. The main components of our design are the *signal_generator* unit, the *moulator* unit and the *timekeeper* unit. These 3 components are wired together within the *frequency_modulation* unit. An overview of the structure of our design can be seen in figure 2.

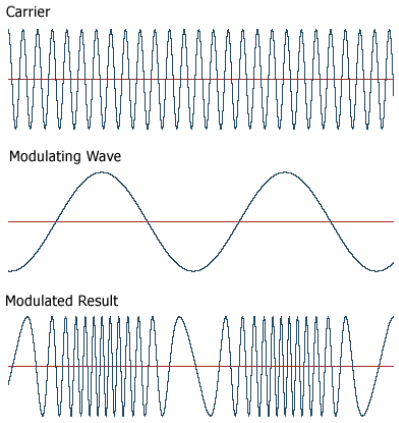

Figure 1: Frequency modulation pictured

Variable	**Description**
A_c	Amplitude of the carrier signal
f_c	Rest frequency of the carrier signal
f_d	Frequency deviation of the carrier signal
A_m	Amplitude of the modulation signal
f_m	Frequency of the modulation signal

Table 1: Explanation of the variables used in the frequency modulation formula

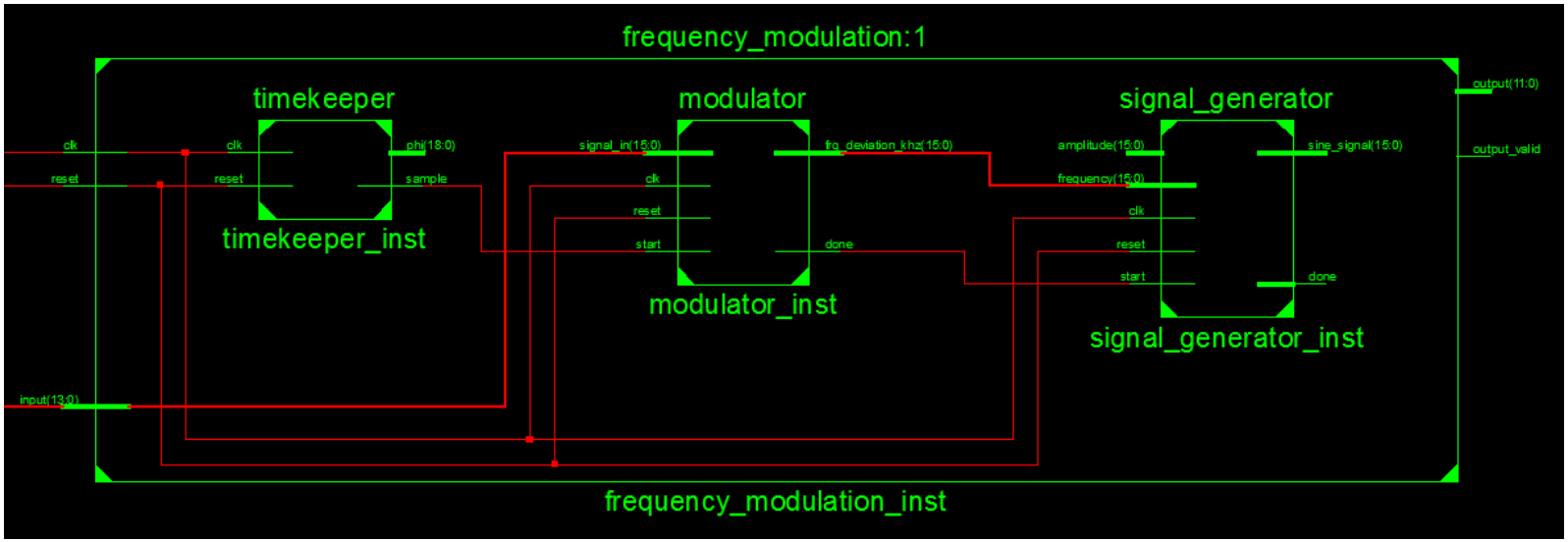

Figure 2: Structural overview of the frequency_modulation unit

2.1 timekeeper

Generic	Default	Description
DATA_WIDTH	8	Defines the bit width of the signals in this entity
CLK_FREQ	50000000	Tells the component the clock speed the desing is running on
BAUD_RATE	44000	That many impulse signals per second will be generated

Portname	Direction	Description
clk	in	Clock signal
reset	in	Reset signal
sample	out	Impulse to be used as start flag for other components
phi	out	Values between π and $-\pi$ to be used for testing

The timekeeper unit correlates real time and clock time by generating $BAUD\_RATE$ impulses per second to be used as start signals for the other components. It also generates different continuos values between π and $-\pi$ by incrementing an internal variable for the minimum precision 2^{DATA_WIDTH} times per second. This can be used for testing.

2.2 modulator

Generic	Default	Description
DATA_WIDTH	8	Defines the bit width of the signals in this entity
MAX_AMPLITUDE	1.0	Maximum expected amplitude of the input signal
MIN_AMPLITUDE	-1.0	Minimum expected amplitude of the input signal
FREQUENCY_DEV_KHZ	0.5	Maximum frequency deviation of the carrier rest frequency in
CARRIER_FREQUENCY_KHZ	1.0	Carrier rest frequency in kHz

Portname	Direction	Description
clk	in	Clock signal
reset	in	Reset signal
start	in	Start flag signals the component that it should start calculations
done	out	Done bit signals that calculations have been completed and the output is h
signal_in	in	Sample value of the modulation signal
frq_deviation_khz	out	Calculated frequency to be used as input for the signal generator

The modulator takes sample values of the modulation signal and translates them into a frequency. According to *MIN_AMPLITUDE* and *MAX_AMPLITUDE* it calculates a mean voltage level. A deviation from this voltage level translates to an increase or decrease of *frq_deviation_khz*. Negative deviation of the mean amplitude correlates to a decrease of *frq_deviation_khz* and positive deviation results in an increase. If there is no deviation at all the output shows the rest frequency of the carrier provided by the generic *CARRIER_FREQUENCY_KHZ*.

2.3 signal generator

Generic	Default	Description
DATA_WIDTH	8	Defines the bit width of the signals in this entity
BAUD_RATE	44000.0	The baudrate of the signal generator

Portname	Direction	Description
clk	in	Clock signal
reset	in	Reset signal
start	in	Start flag signals the component that it should start calculations
done	out	Done bit signals that calculations have been completed and the output is holding
frequency	in	The frequency of the generated sign signal
amplitude	in	The amplitde of the generated sign signal
sine_signal	out	The current sample of the generated sign signal

The *signal_generator* is the core component of the design. The component instantiates the *sine_cordic* component we developed for the first task to generate a continuous set of sine wave samples with frequency and amplitude according to its inputs.

2.4 frequency modulation

Generic	Default	Description
INTERNAL_DATA_WIDTH	16	Defines the bit width of the signals in this entity
INPUT_DATA_WIDTH	14	Data width of the ADC register
TIME_PRECISION	19	Time precision data width to be used in the *timekeeper*
OUTPUT_DATA_WIDTH	12	Data width of the DAC register
CLK_FREQ	50000000	The clock frequency of the design
BAUD_RATE	44000.0	The baudrate of the signal generator
CARRIER_FREQ	1.0	Maximum frequency deviation of the carrier rest frequency in kH
FREQUENCY_DEV_KHZ	0.5	Maximum frequency deviation of the carrier rest frequency in kH

Portname	Direction	Description
clk	in	Clock signal
reset	in	Reset signal
input	in	Sample of the ADC
output_valid	out	Valid data flag to be written to the DAC
output	out	Output value to be written in the DAC register

The frequency modulation component is wiring all the component together. It connects the sample impulse signals of the *timekeeper* to the input *start* ports of the other components. It wires the *input* port to the *signal_in* port if the modulator, the *frq_deviation_khz* output port of the *modulator* to the *frequency* input port of the *signal_generator* and the *sine_signal* output port of the *signal_generator* to the *output* port of the *frequency_modulator*

3 Testing and Results