《计算机系统结构》课程直播

2020. 3.26　习题课

请将ZOOM名称改为“姓名”；

听不到声音请及时调试声音设备，可以课间补签到

本节内容

- 作业难点讲解
- 存储习题习题讲解

补码、32位机器、有符号值使用算术右移，无符号值使用逻辑右移。

- int x = foo(); //调用某某函数，给x赋值
- int y = bar(); //调用某某函数，给y赋值
- unsigned ux = x;
- unsigned uy = y;
- 以下表达式是否为真，如果不真，给出使得它为假的x和y值；
- F: x+y == uy+ux
- G: x*~y + uy*ux == -x
- H: x*4 + y*8 == (x<<2)+(x<<3)
- I: ((x>>2)<<2)<=x

•Values of type int are 32 bits. They are represented in two's complement,

•Values of type unsigned are 32 bits. Values of type float are represented using the 32-bit IEEE floating point format, while values of type double use the 64-bit IEEE floating point format.

- int x = random();
- int y = random();
- int z = random();
- /* Convert to other forms */
- unsigned ux = (unsigned) x;
- unsigned uy = (unsigned) y;
- double dx = (double) x;
- double dy = (double) y;
- double dz = (double) z;

Expression	Always True?
`(x<y) == (-x>-y)`	Y N
`((x+y)<<4) + y-x == 17*y+15*x`	Y N
`~x+~y+1 == ~(x+y)`	Y N
`ux-uy == -(y-x)`	Y N
`(x >= 0) || (x < ux)`	Y N
`((x >> 1) << 1) <= x`	Y N
`(double)(float) x == (double) x`	Y N
`dx + dy == (double) (y+x)`	Y N
`dx + dy + dz == dz + dy + dx`	Y N
`dx * dy * dz == dz * dy * dx`	Y N

A four-way set-associative writeback cache has a 2^{11} ·89-bit tag store.

- The cache uses a custom replacement policy that requires 9 bits per set.
- The cache block size is 64 bytes.
- The cache is virtually-indexed and physically-tagged.
- Data from a given physical address can be present in up to eight different sets in the cache.

The system uses hierarchical page tables with two levels.

- Each level of the page table contains 1024 entries.
- A page table may be larger or smaller than one page.
- The TLB contains 64 entries.

1. How many bits of the virtual address are used to choose a set in the cache?
2. What is the size of the cache data store?
3. How many bits in the Physical Frame Number must overlap with the set index bits in the virtual address?
4. What is the page size?
5. What is the size of the virtual address space?
6. What is the size of the physical address space?

选择题

- 假定编译器将赋值语句“x=x+3；”转换为指令“add xaddt,3”，其中xaddt是x对应的存储单元地址，若执行该指令的计算机采用页式虚拟存储管理方式，并配有相应的TLB，且Cache使用直写（write through）方式，完成该指令的功能，需要访问主存的次数最少是（　　）次

- A. 0　　B. 1　　C. 2　　D. 3

- We have a 4 Kbyte cache operating with 256 byte lines.
- Consider two designs for this cache.
- The first is a direct mapped design. The second is a fully associative cache with an LRU replacement policy. Physical addresses are 16 bits.
- Provide a sequence of physical addresses (in hexadecimal notation) that when repeated indefinitely will result in a lower miss rate in the direct mapped cache than in the fully associative cache. The address stream should be accompanied by an explanation of this behavior.

下周二

- 指令系统

•再见