**Qiang Zhang**

Age: 29 • Work Experience: 5 years • Mobile: 13120403400 • Email: [johnson9009@163.com](mailto:johnson9009@163.com)

**Education**

**M.S. Computer Science, (Exam-exempted), Beijing University of Technology,** **(2012.9 – 2015.6)**

**B.S. Computer Science, Beijing University of Technology,** **(2008.9 – 2012.6)**

**TECHNICAL SKILLS**

* Proficient in C/C++, skilled with Python, Shell script, knowledge of Rust, JavaScript.
* Skilled with commonly used data structure and algorithm, design pattern, familiar with inter-process communication, multi-thread, coroutine, async IO and so on knowledge.
* Familiar with machine learning compiler Glow, MLIR, TVM, and traditional compiler front end, e.g., lexical analysis, syntax analysis.
* Familiar with machine learning, image recognition, object detection algorithm, solid understand of the structure and mechanism of CNN, familiar with deep learning optimization and quantization algorithm.
* Skilled with Linux performance, memory optimization, and relevant tools, e.g., Valgrind, GDB.
* Familiar with CI/CD system development and relevant tools, e.g., Git, CMake, GitLab, Docker, skilled with container relevant knowledge, basic knowledge of Kubernetes.
* Knowledge of commonly used GUI, Web development pattern, e.g., MVC, MVVM, and front-end back-end separated, high performance, high available architecture.
* Knowledge of ASIC, FPGA design method and flow, familiar with board level hardware design, with 2 years hardware board design and debug experience.

**Work Experience**

**2018.8 –** **Present Synopsys AI Lab Senior Software Engineer**

**2016.11 –** **2018.8 Cadence Design Systems SFE Software Engineer**

**2015.7 –** **2016.11 VIA Technologies SSD SSD Firmware Engineer**

**Project Experience**

**AI Chip Architecture Simulation and Analysis, 2018.8 – 2019.1**

**Providing AI chip hardware architecture modeling and neural network (NN) model analysis service for a famous AI chip company, help customer co-simulation their AI chip hardware with their software through architecture simulation and analyze tool Platform Architect (PA), and then iteratively optimizing their AI chip architecture according to the analysis results.**

* Develop NN model profiler using Python, analyzing kind and count of needed hardware unit for accelerate a Tensorflow model, and compute amount and memory size of each operator.
* Model some modules of customer’s AI chip using C++, create the whole chip simulation model in PA and build it as final executable simulation program.
* Run the NN model that compiled by customer’s compiler on the simulation program and resolve all bugs through debugging with GDB.

**Neural Network (NN) Compiler, 2019.2 – 2019.10**

**Refer to traditional compiler knowledge, importing the NN model and convert it to IR, then do lots of optimizations on IR, with the work that implement PA as a backend, at the code generation time the IR can be generated as the Tcl scripts that PA needed, finally customers can analyze the performance of running this NN model on their chip architecture through PA.**

* Develop the framework of NN compiler based on Glow, improve ONNX model supporting, control optimization passes, implement the PA backend to generate the optimized IR as Tcl scripts.
* Develop the framework of NN compiler based on MLIR, implement our IR as dialect and the PA backend.
* Develop the framework of NN compiler based on TVM, implement pass manager and PA backend.

**AI Chip Architecture Exploration and Simulation Platform, 2019.11 – Present**

**Through NN compiler optimize and compile the NN model to PA needed format, the chip designer only need model the AI chip architecture through GUI, then can get the performance of running NN models on this AI chip, then the chip designer can explore the chip architecture iteratively.**

* Take account of NN compiler and PA modeling method, complete the feasibility testing of the technical key point, e.g., performance and memory problem of PA running big NN model, dynamic behavior simulation method, automation of PA hardware modeling.
* Develop PA hardware modeling framework using C++, provide the infrastructure of modeling NVDLA modules efficiently for other colleagues.
* Design and implement the data format between NN compiler and AI chip simulation program based on Flatbuffers, through function multi-stream, segment load resolving the problem of PA running big NN model.
* Develop parallel build and regression test system, also include test result collection and reporting, setup distributed CI/CD system based on Docker and GitLab CI, automate the full develop flow.
* Develop tool that generate the PA hardware model from hardware description file.

**Refactor the Measurement Part of Circuit Simulation System (MDL),** **2017.3 – 2018.8**

**Through the new architecture decompose measurements and complex analyses, reuse complex analysis code, improve the stability of simulation system.**

* Design and implement the new architecture, resolve binding of measurement and analysis, real time computation of measurement, output text or waveform result and other critical issues step by step.
* Responsible for applying the new architecture to complex analyses such as Monte Carlo, sweep analysis.
* Responsible for resolving all the relevant regression test cases.

**Driver and Layer 3 of SSD firmware Development, 2015.8 – 2016.11**

**Designed and implemented firmware for the new generation SSD controller chip.**

* Development of NAND flash driver and XOR engine driver.
* Co-designed and completed the new hardware acceleration module XOR engine with logic colleagues, leading the unit and stress testing of XOR engine.
* Redesign error handling architecture.

**Remote Diagnosis and Maintenance System for POS, 2013.12 – 2015.2**

**Cooperated with well-known POS manufacturer, combining hardware and software technology, to provide a real-time fault diagnosis, alarm and remote maintenance system for POS machines.**

* Designed PCIe remote diagnosis and maintenance card hardware with Spartan6 FPGA chip.
* Developed firmware and bootloader of PCIe card.
* Developed diagnosis and network communication UEFI application.

**The Attractions and Monuments Touring System Based on Google Earth, 2011.12 – 2012.7**

**Capture motion of user through motion capture hardware, and then use it to control the tour in virtual sites of Google Earth.**

* Designed overall and detailed scheme.
* Designed hardware and firmware of six degrees freedom motion capture node by combining the use of accelerometers and gyroscopes.
* Designed hardware and firmware of Zigbee wireless transmission module.
* Organize and coordinate the team members.
* Developed sensor data fusion and filtering software, customized embedded version of Windows.

**Awards**

* Win the second prize in *2012 Intel Cup Undergraduate Electronic Design Contest - Embedded System Design Invitational Contest*.