2022 Analog IC Design Homework 4 **due date: 06/01/2022**

1. Design a differential to single-ended amplifier with $\mathbf{Vdd = 1.5V, C_L = 0.5pF}$ as shown in Fig. 1. (45%)

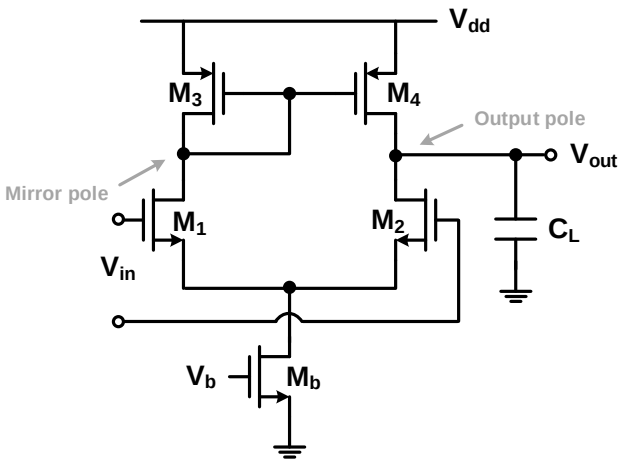

Fig.1.

(operation point)

(a) Please design the device size of M_1~M_4 , M_b, the input common mode voltage and V_b, to get voltage DC gain $\mathbf{A_v > 20\ dB}$ and its bandwidth (-3dB point to DC gain) has to be **larger than 5MHz**. (5%)
(Please note, since M_b serves as a current source, M_b must stay in the saturation region).

(b) Please use **.op** command to print out the small signal parameters of active devices from list file. Use .op's parameters to calculate the DC gain and check your calculation and the simulation results in (a). (10%)

(frequency response)

(c) The small signal -3dB bandwidth has to be **larger than 5MHz**. Please simulate and plot the frequency response of this gain stage. Use **.pz** to simulate and mark the poles/zeros on this curve. (5%)

(d) Please use **.op** command to print out the small signal parameters of active devices from list file. Use .op's parameters to calculate the output pole, mirror pole and the first zero of $V_{out}/V_{in}(s)$ frequency response. Check your calculation and the simulation results in (c). (10%)

(e) Here we define "Bandwidth (MHz) / tail current (uA)" as figure of merit (FOM).
Please try to make this FOM maximal. (5%)

(f) Please fill the following table and discuss your design for best FOM. (10%)

Working item	Specification	Simulation	Calculation
Vdd	1.5 V		
C_L	0.5 p		
Tail current (uA)	Open for design (#1)		
Voltage DC gain	> 20 dB		
Input common mode voltage	Open for design (V_{BS})		
Output common mode voltage	Open for design		
Tail current bias voltage	Open for design (V_b)		
Input size $M_{1,2}$	Open for design (W/L), m		
PMOS size $M_{3,4}$	Open for design (W/L), m		
Tail current MOS size M_b	Open for design (W/L), m		
Bandwidth (MHz)	> 5 MHz (#2)		
FOM	(#2)/(#1)		

★ ***Tips***

You can use the following command to simulate the differential input signal, it's a VCVS

Vac in gnd ac = 1

Vicm Vicm 0 dc = ___

Eacp Vip vicm in 0 0.5

Eacn Vin vicm in 0 -0.5

.pz V(Vout) Vac

2. Design a two-stage Op amp with $\mathbf{Vdd = 1.5V, C_L = 1pF}$ as shown in Fig. 2. (55%)

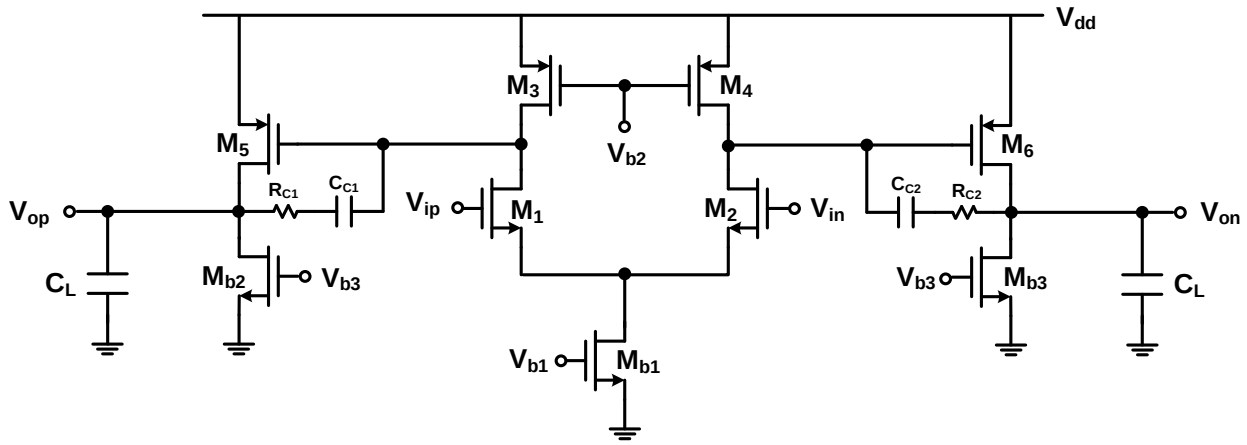

Fig.2.

★ In this design, the differential mode DC gain $> 60dB$, unity gain frequency $> 60MHz$, and phase margin $> 45°$.

(a) Operation point (10%)

A. Please **DESIGN and LIST** your bias MOS $(M_{b1} - M_{b3})$, amplifier $(M_1 - M_6)$ size, and $V_{b1} - V_{b3}$ to make the differential mode gain at DC larger than 60dB.

The information of the circuit			
M_{b1}		V_{b1}	
M_{b2}		V_{b2}	
M_{b3}		V_{b3}	
$M_{1,2}$		Input common mode voltage	
$M_{3,4}$		Output common mode voltage	
$M_{5,6}$			

B. Print out the results from **.op** command. And make sure all the devices are properly biased.

C. Use **.tf** command to print out the voltage gain.

D. Verify your DC gain with hand calculation.

(b) With compensation capacitor $C_{C1,2}$ and nulling resistor $R_{C1,2}$ (20%)

A. Please design your value of $R_{C1,2}$ and $C_{C1,2}$. Simulate and plot the frequency response (magnitude and phase) of your design in (a).
(Mark the (i) DC gain (ii) unity gain frequency, and (iii) phase margin on figure.)

★ Please note, your unity gain frequency must be larger than 60MHz and phase margin must larger than $45°$ in this case.

B. Use **.pz** to simulate and mark the poles/zeros and mark them on bode plot.

C. Verify the compensation with hand calculation.

(c) Remove $C_{C1,2}$ and $R_{C1,2}$ in Fig.2. (10%)

A. Simulate and plot the frequency response (magnitude and phase) of your design. (Mark the (i) DC gain (ii) unity gain frequency, and (iii) phase margin on figure.)

B. Use **.pz** to identify the poles and zeros, and mark them on bode plot.

C. Verify the first and second dominant poles and first RHP zeros with hand calculation.

(d) Compare the result in (b), (c) and comment what causes the difference. (15%)

(e) Please fill the following table.

Performance Table		
V_{DD}	1.5 V	
R_c , C_c		
Input common mode voltage		
Output common mode voltage		
Open-loop performance (after compensation)		
Differential mode DC gain (> 60dB)		
Unity gain frequency (1pF load)(> 60MHz)		
Phase margin (> 45°)		

★ ***All device in the circuit must be in Saturation Region !!!!!***

★ ***Tips***
You can use the following command to get the phase of the circuit
.probe AC Vp(Vop)

★ ***The following should be included in your report (a) schematic (b) HSPICE netlist (c) waveform with cursor values (d) comments.***