2022 Analog IC Design Final

107022204 邱孟瑋 109061217 林峻霆

A. Schematic with device size, component value, node voltage and branch current.

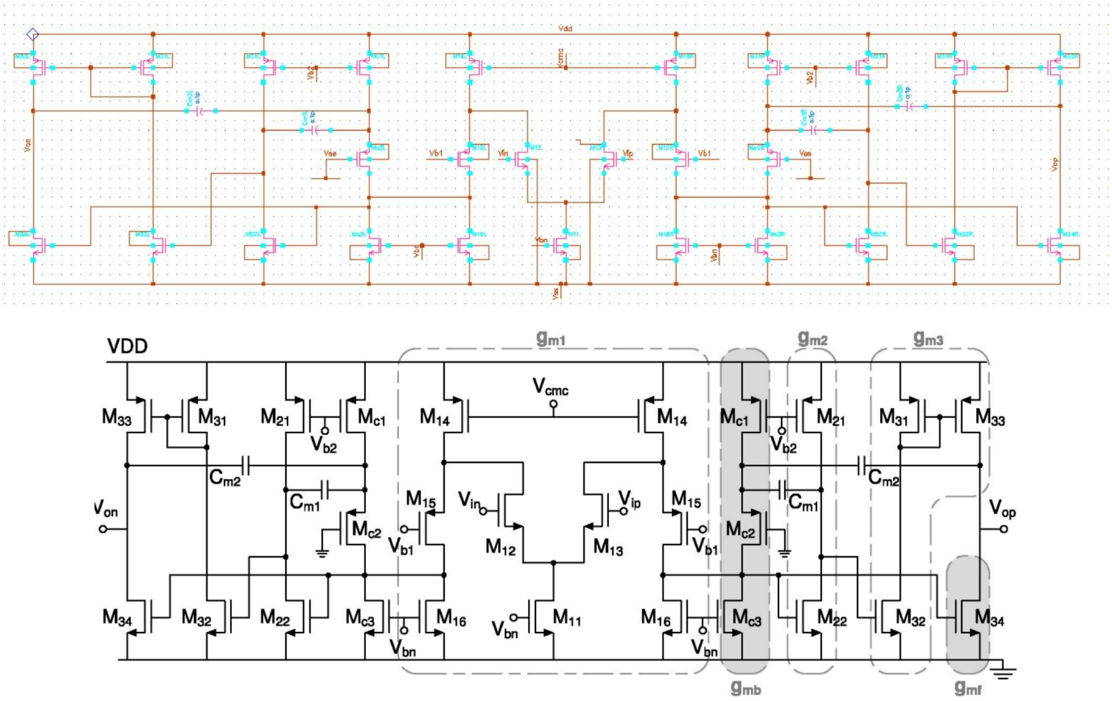


Fig.A.1 schematic of the proposed fully differential amplifier.

MOS	W(μm)	L(μm)	M
M11	1	1	200
M12	1	0.55	100
M13	1	1	100
M14	1	1	90
M15	1	1	140
M16	1.2	1	90
Mc1	1	1	13
Mc2	1.2	1.2	20
Mc3	2.4	2.4	30
M21	1.2	0.8	5
M22	2.5	1	50
M31	1.2	1.2	40
M32	2	2	10
M33	1.2	1.2	100
M34	2	2	100
Cm1	1.6pF		

Cm2	2pF

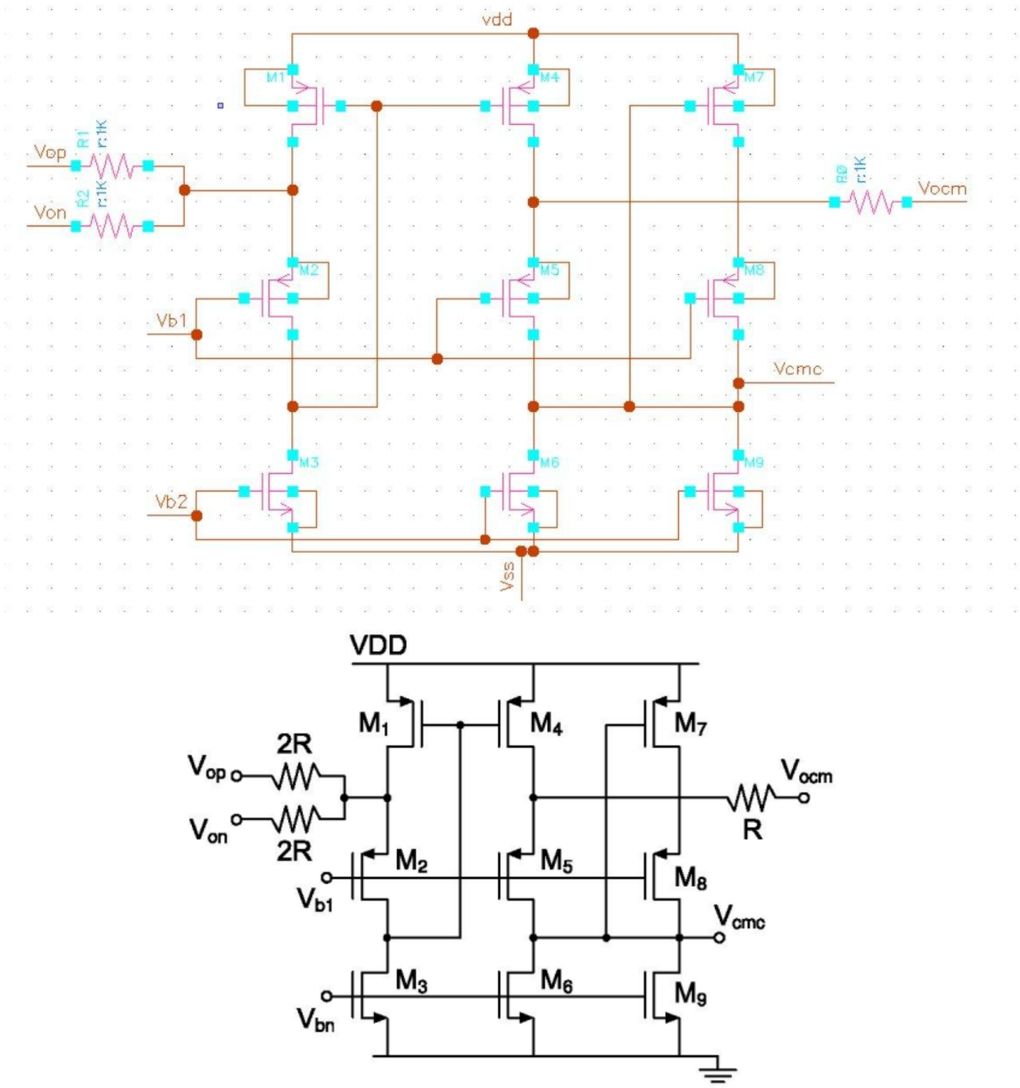


Fig. A.2. Current compared CMFB circuit.

MOS	W(μm)	L(μm)	M
M1	2	0.8	4
M2	2	0.8	4
M3	1.2	1	8
M4	2	0.8	4
M5	2	0.8	4
M6	1.2	1	8
M7	0.8	0.8	15
M8	1.1	0.8	15
M9	1.2	1	20
R	8kΩ		
2R	50kΩ		

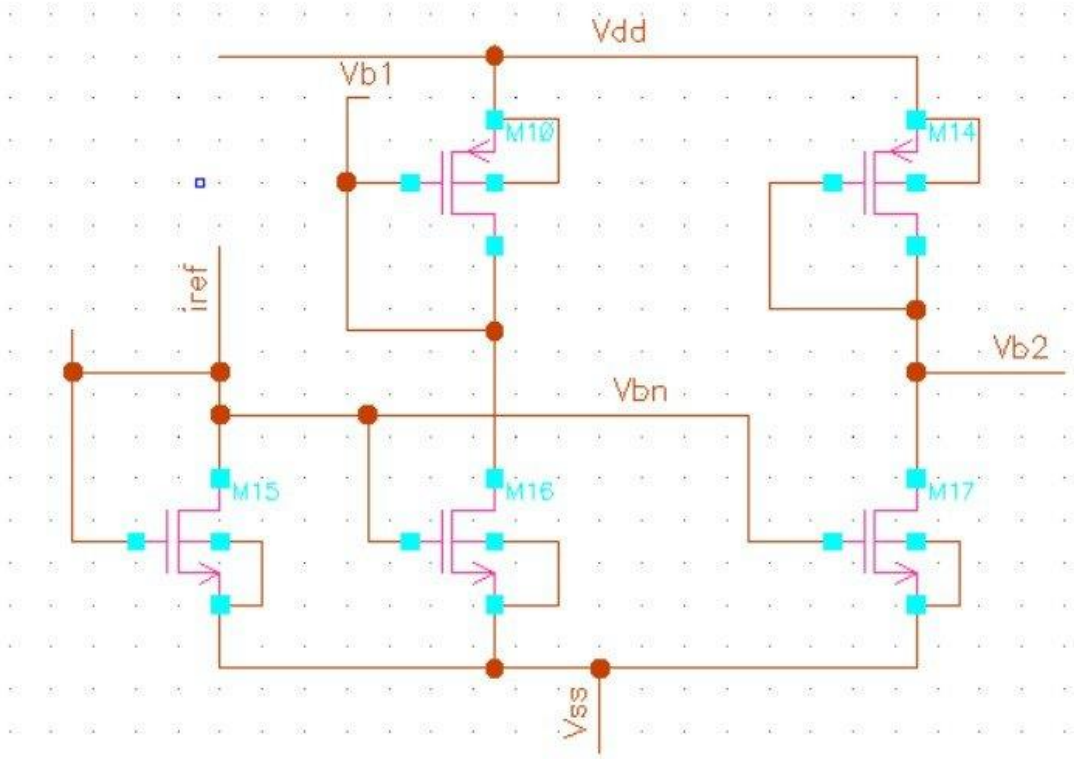


Fig. A.3. Biasing curcuit.

MOS	W(μm)	L(μm)	M
Mb10	1	1	30
Mb14	1	1	43
Mb15	1.2	1	40
Mb16	1.2	1	200
Mb17	1.2	1	200

B. Simulation results of each specification and contains all corners.

1. Power

TT: Total power dissipation = 2.4449056 m W

```
**** voltage sources

subckt
element  0:vdd      0:vgnd     0:vinn     0:vinp     0:vocm
 volts     1.4000     0.        700.0000m  700.0000m  700.0000m
 current  -1.7232m   1.5983m    0.         0.          23.3827u
 power     2.4124m   0.         0.         0.         -16.3679u

    total voltage source power dissipation=    2.3960m       watts



**** current sources

subckt
element  0:iref
 volts    940.4922m
 current   52.0000u
 power    -48.9056u


    total current source power dissipation= -48.9056u       watts
```

Fig. B1. TT-power

FF: Total power dissipation = 2.4238587 m W

```
**** voltage sources

subckt
element  0:vdd      0:vgnd     0:vinn     0:vinp     0:vocm
 volts     1.4000     0.        700.0000m  700.0000m  700.0000m
 current  -1.7095m   1.5980m    0.         0.          29.2830u
 power     2.3933m   0.         0.         0.         -20.4981u

    total voltage source power dissipation=    2.3728m       watts



**** current sources

subckt
element  0:iref
 volts    981.8990m
 current   52.0000u
 power    -51.0587u


    total current source power dissipation= -51.0587u       watts
```

Fig. B1. FF-power

SS: Total power dissipation = 2.4524253 m W

```
**** voltage sources

subckt
element  0:vdd       0:vgnd     0:vinn     0:vinp     0:vocm
 volts      1.4000     0.         700.0000m  700.0000m  700.0000m
 current   -1.7268m    1.5889m    0.         0.          15.9953u
 power      2.4175m    0.         0.         0.         -11.1967u

    total voltage source power dissipation=    2.4063m       watts



**** current sources

subckt
element  0:iref
 volts    887.0245m
 current   52.0000u
 power    -46.1253u


    total current source power dissipation= -46.1253u       watts
```

Fig. B1. SS-power

SF: Total power dissipation = 2.447153 m W

```
**** voltage sources

subckt
element  0:vdd       0:vgnd     0:vinn     0:vinp     0:vocm
 volts      1.4000     0.         700.0000m  700.0000m  700.0000m
 current   -1.7269m    1.5995m    0.         0.          23.9195u
 power      2.4177m    0.         0.         0.         -16.7436u

    total voltage source power dissipation=    2.4010m       watts



**** current sources

subckt
element  0:iref
 volts    887.0245m
 current   52.0000u
 power    -46.1253u


    total current source power dissipation= -46.1253u       watts
```

Fig. B1. SF-power

FS: Total power dissipation = 2.4465999 m W

```
**** voltage sources

subckt
element  0:vdd       0:vgnd     0:vinn     0:vinp     0:vocm
 volts      1.4000     0.        700.0000m  700.0000m  700.0000m
 current   -1.7253m    1.5997m    0.         0.         23.8900u
 power      2.4154m    0.         0.         0.        -16.7230u

    total voltage source power dissipation=    2.3987m       watts



**** current sources

subckt
element  0:iref
 volts    921.1520m
 current   52.0000u
 power    -47.8999u


    total current source power dissipation= -47.8999u       watts
```

Fig. B1. FS-power

Comparison:

$$Power_{SS} > Power_{SF} \geq Power_{FS} \geq Power_{TT} > Power_{FF}$$

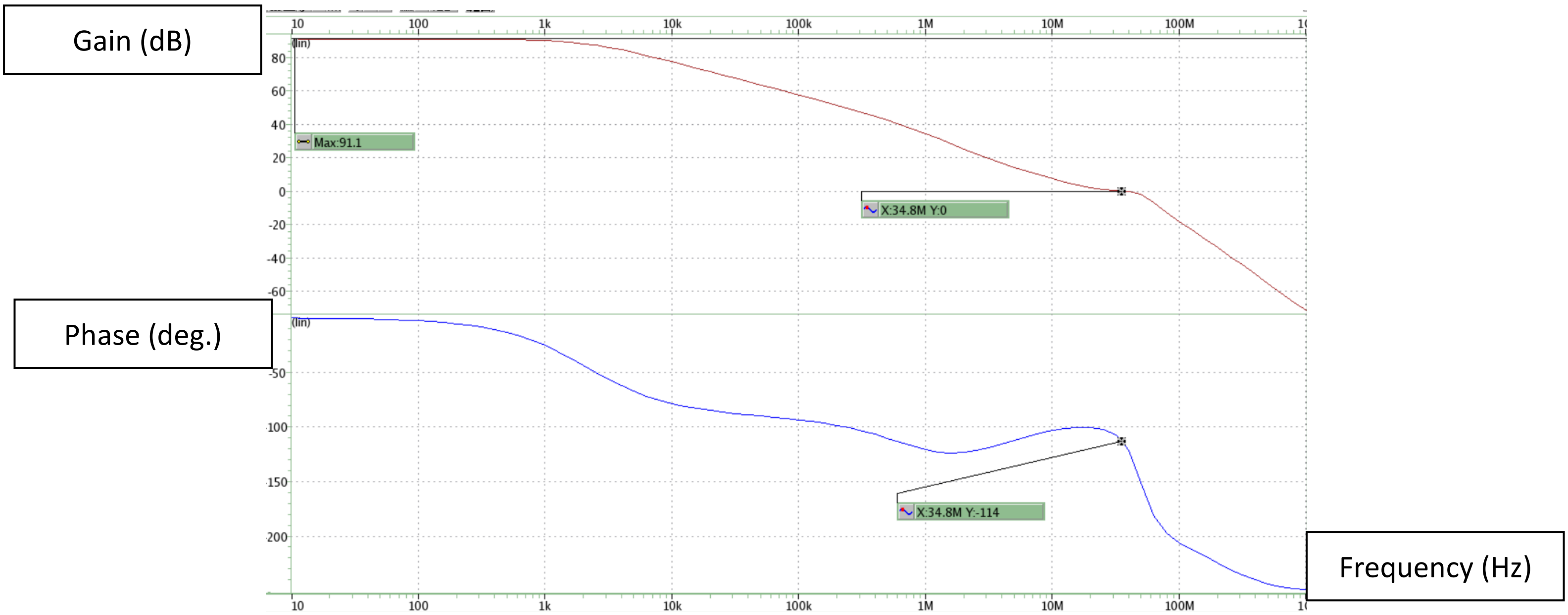
For Slow NMOS Slow PMOS corner, has the most higher power dissipation, can be conclude that the slow MOS has higher power dissipation then fast MOS.

2.DC gain, U.G.B., P.M.

TT: DC-Gain=91.1491dB, P.M.=66.4003deg. U.G.B =35.07MHz

dcgain_in_db	dcgain	unity_frequency	phase
phase_margin	temper	alter#	
91.1491	3.610e+04	3.507e+07	-113.5997
66.4003	25.0000	1	

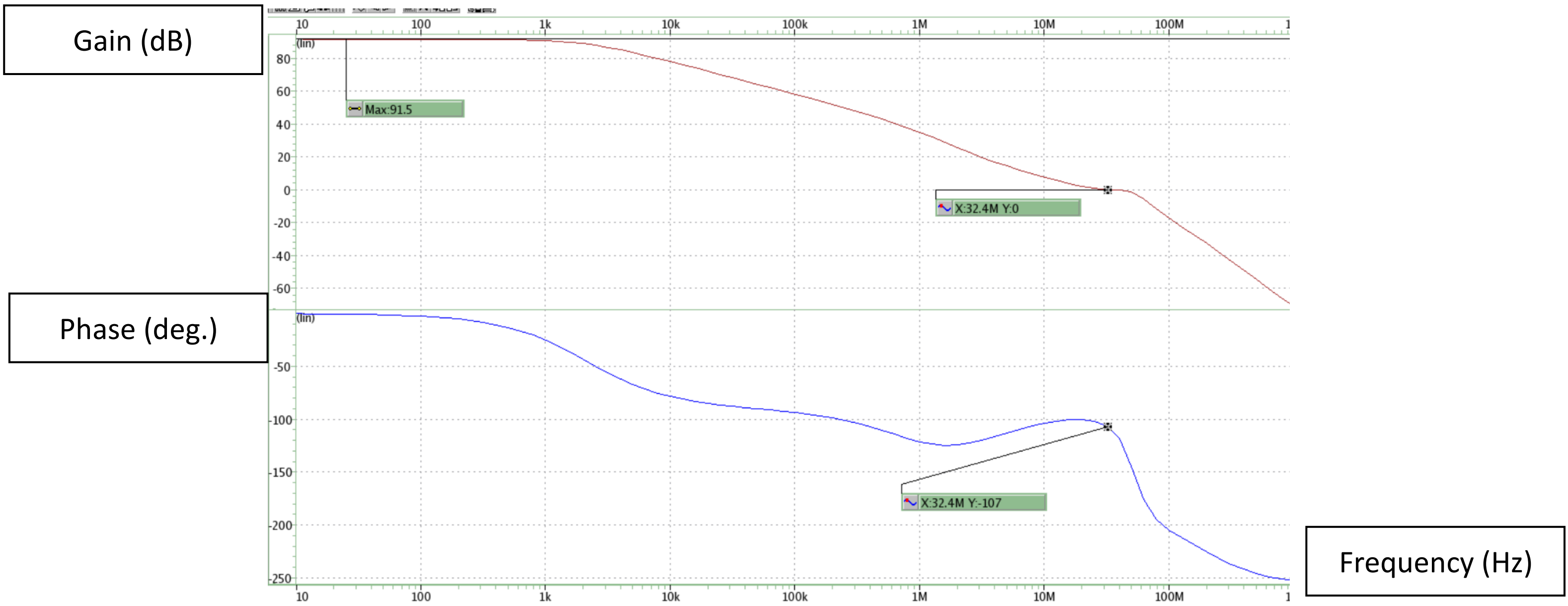
Fig. B2. TT-gain, P.M., UGB



FF: DC-Gain=91.5394dB, P.M.=72.6077deg. U.G.B =32.51MHz

dcgain_in_db	dcgain	unity_frequency	phase
phase_margin	temper	alter#	
91.5394	3.775e+04	3.251e+07	-107.3923
72.6077	25.0000	2	

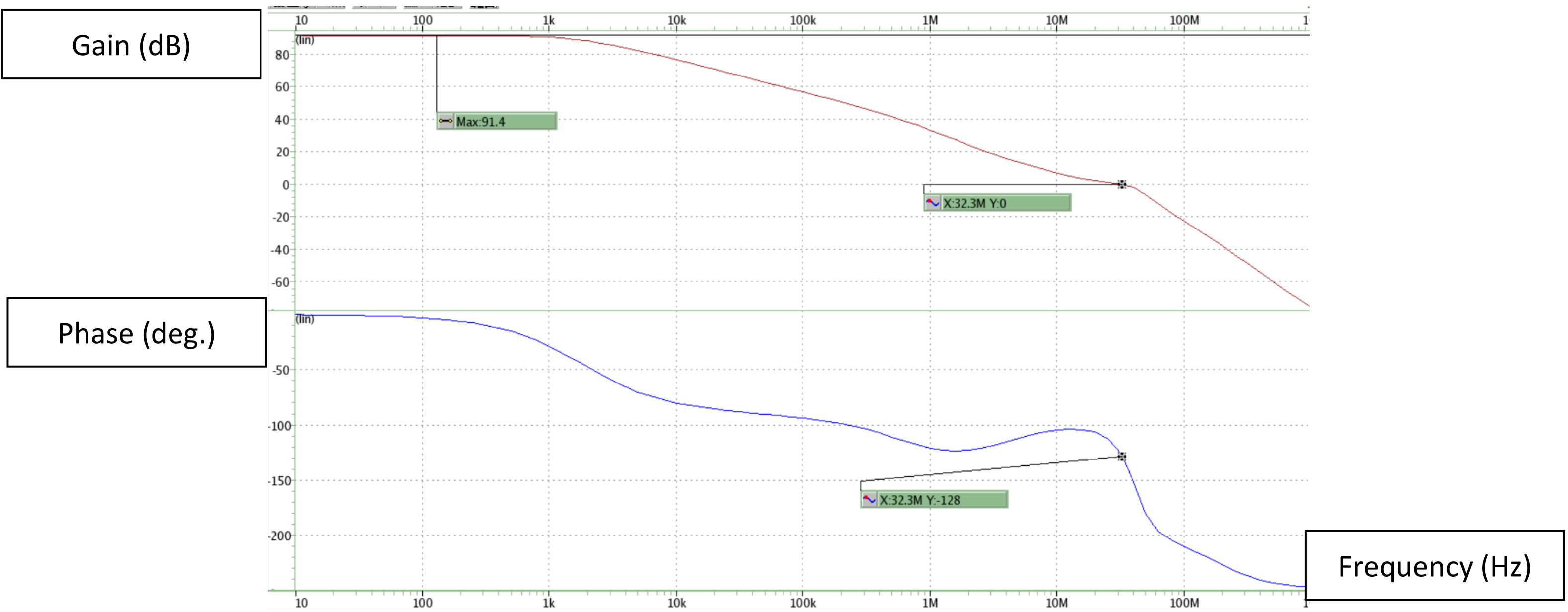
Fig. B2. FF-gain, P.M., UGB



SS: DC-Gain=91.4377dB, P.M.=51.5860deg. U.G.B =32.35MHz

dcgain_in_db	dcgain	unity_frequency	phase
phase_margin	temper	alter#	
91.4377	3.732e+04	3.235e+07	-128.4140
51.5860	25.0000	3	

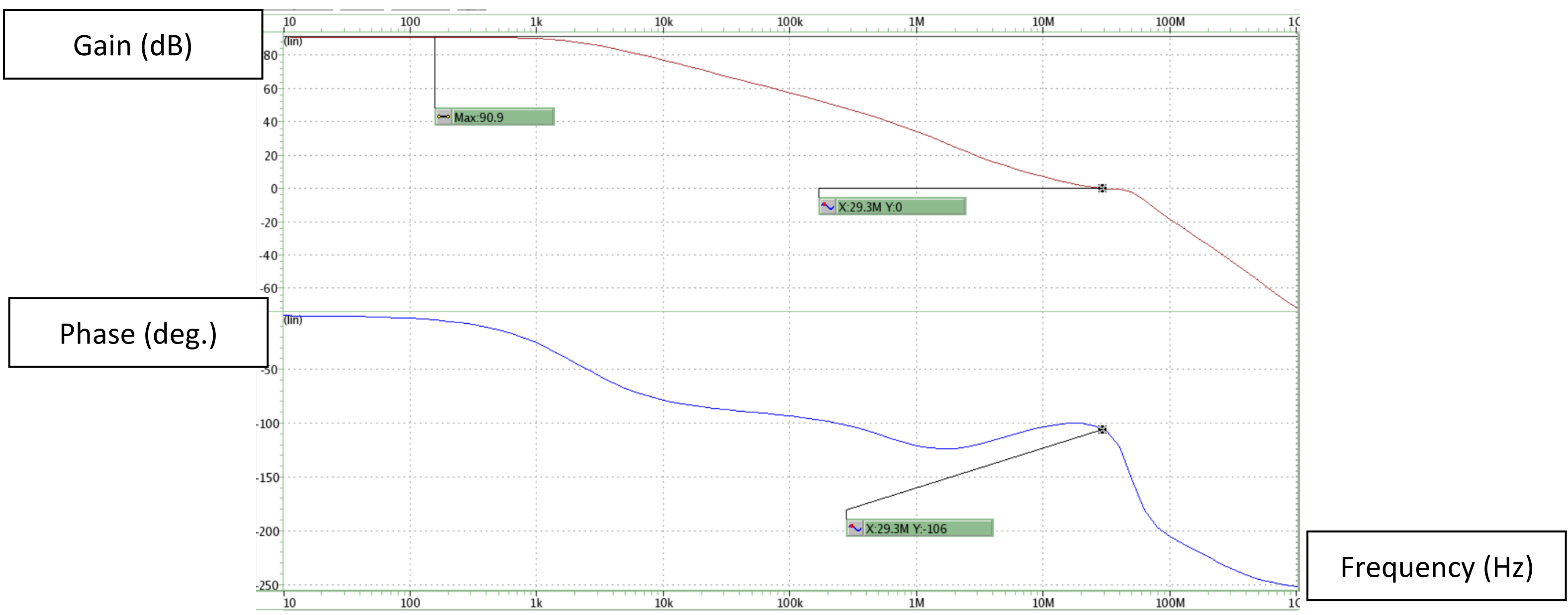
Fig. B2. SS-gain, P.M., UGB



SF: DC-Gain=91.20041dB, P.M.=74.0980deg. U.G.B =22.68MHz

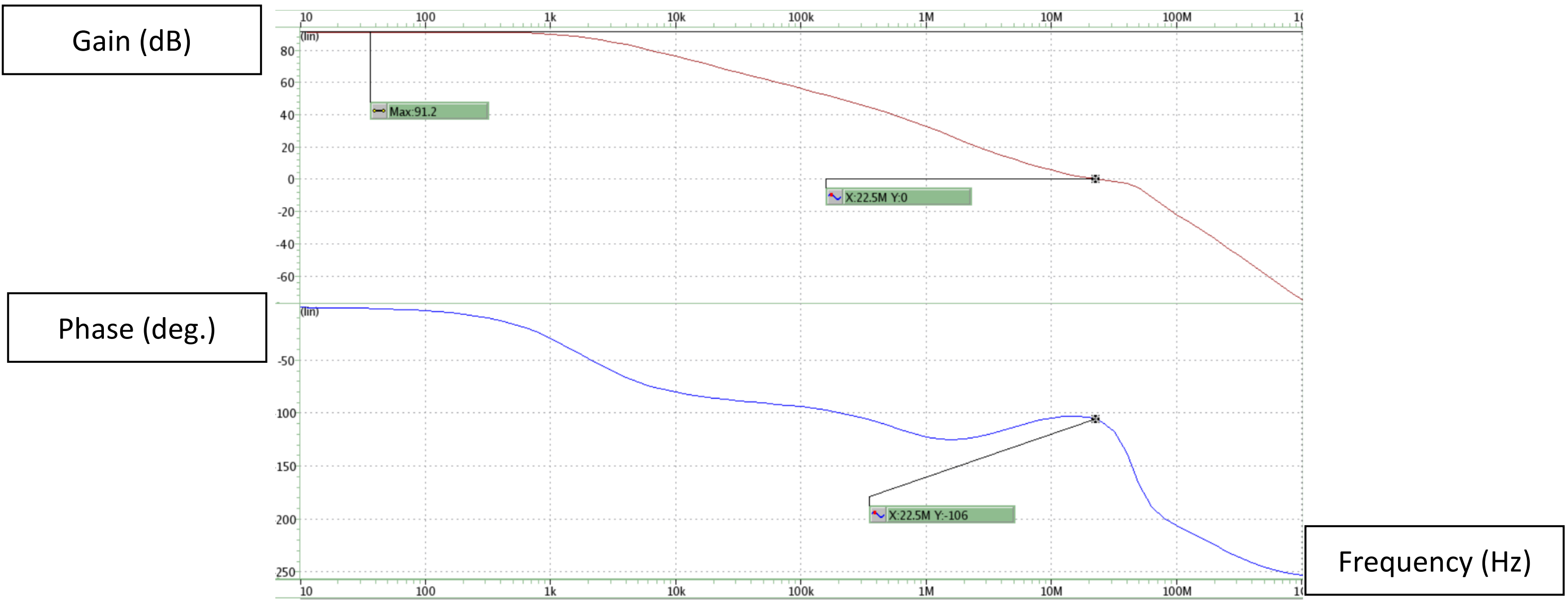
dcgain_in_db	dcgain	unity_frequency	phase
phase_margin	temper	alter#	
91.2004	3.631e+04	2.268e+07	-105.9020
74.0980	25.0000	4	

Fig. B2. FS-gain, P.M., UGB



FS: DC-Gain=90.9129dB, P.M.=73.934deg. U.G.B =29.46MHz

```
dcgain_in_db      dcgain           unity_frequency   phase
phase_margin      temper           alter#
  90.9129          3.513e+04        2.946e+07        -106.0660
  73.9340           25.0000        5
```



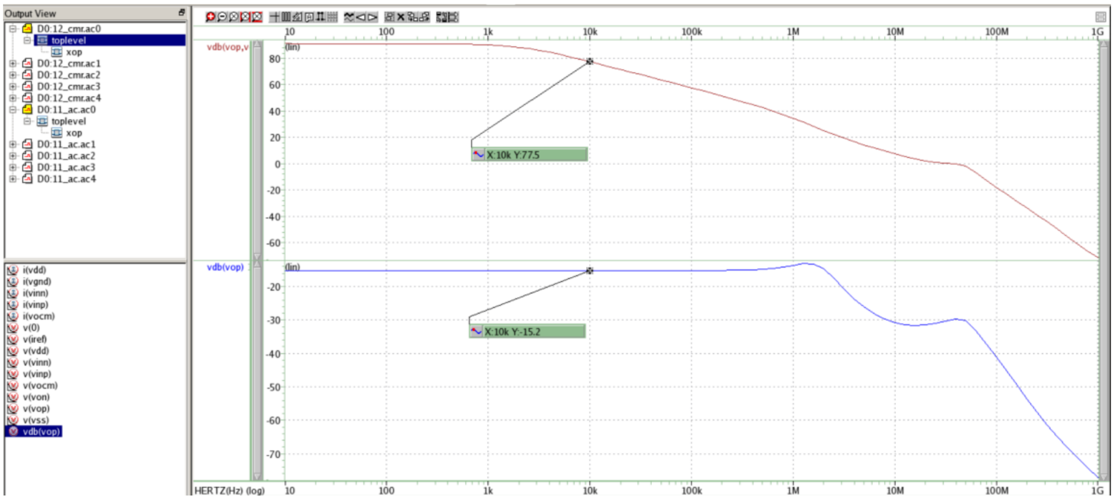
Comparison:

$$Gain_{SS} > Gain_{SF} \geq Gain_{FS} \geq Gain_{TT} > Gain_{FF}$$

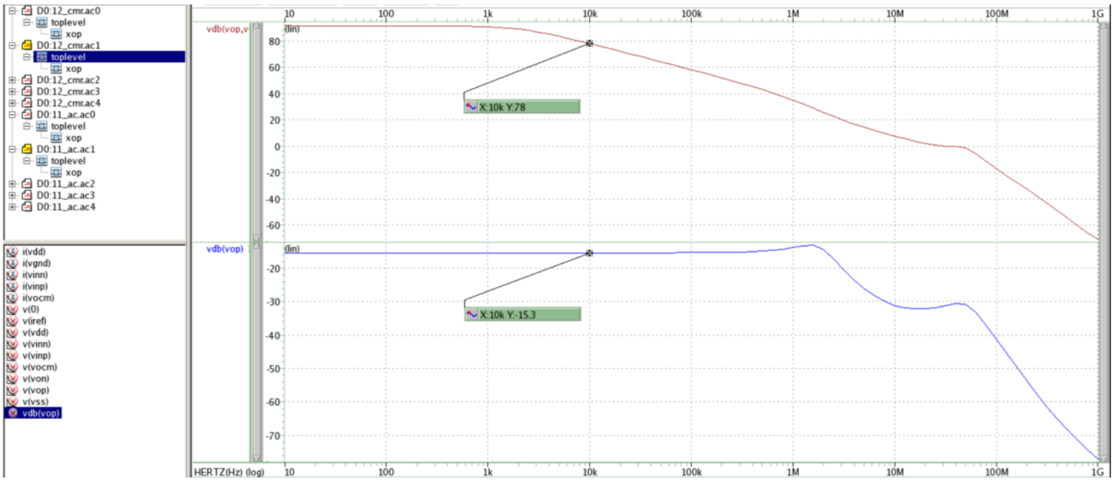
3. C.M.R.R.@10KHz

$$C.M.R.R \quad = \frac{A_{DM}}{A_{CM-DM}}$$

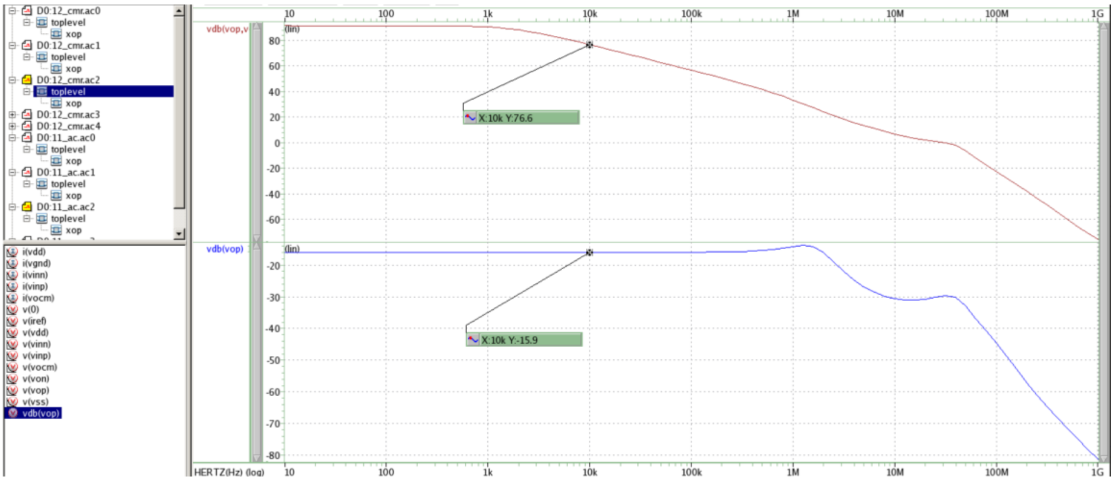
TT: C.M.R.R.@10KHz=77.5-(-15.2) dB = 92.7dB



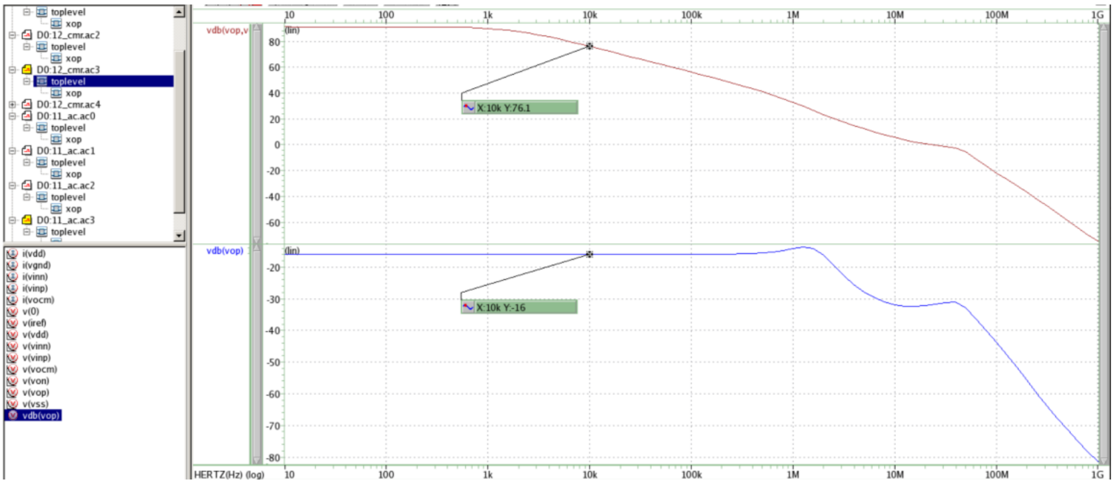
FF: C.M.R.R.@10KHz=78-(-15.3)dB = 93.3dB



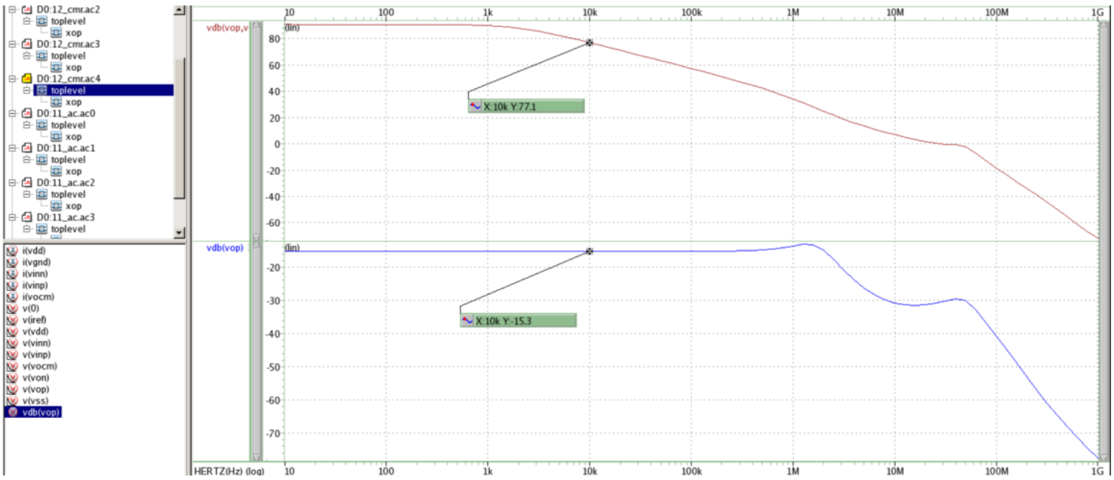
SS: C.M.R.R.@10KHz=76.6-(-15.9)dB = 92.5dB



SF: C.M.R.R.@10KHz=76.1-(-16)dB = 92.1dB



FS: C.M.R.R.@10KHz=77.1-(-15.3)dB = 92.4dB



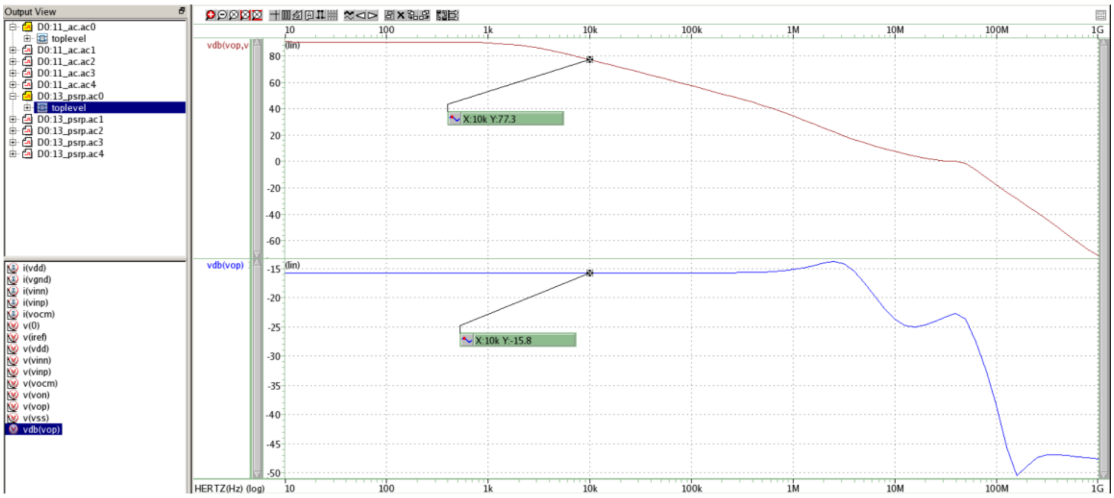
Comparison:

$$C.M.R.R_{SS} > C.M.R.R_{SF} \geq C.M.R.R_{FS} \geq C.M.R.R_{TT} > C.M.R.R_{FF}$$

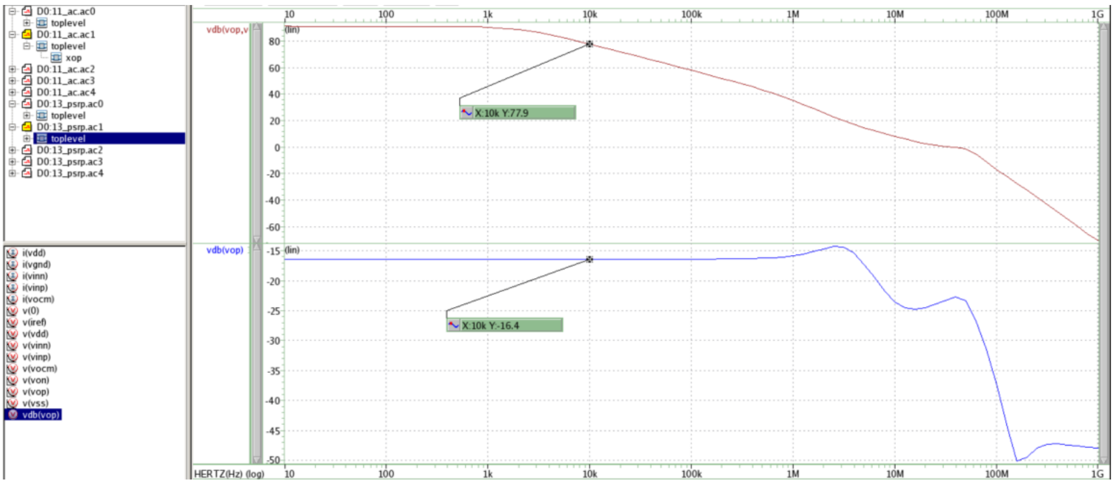
4. P.S.R.R.+@10KHz

$$P.S.R.R._+ = \frac{A_{DM}}{A_{Power\ supply}}$$

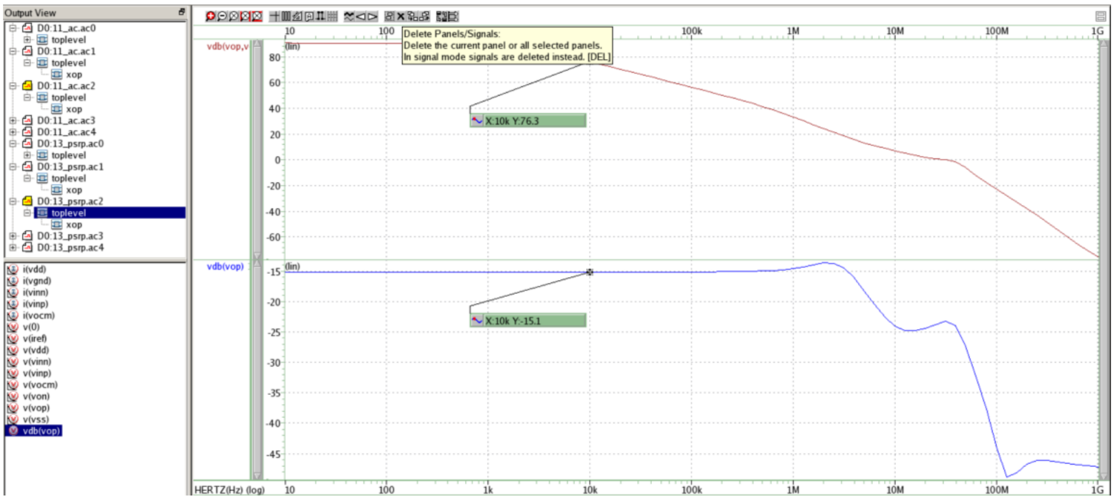
TT: P.S.R.R.+@10KHz=77.3-(-15.8)dB=93.1dB



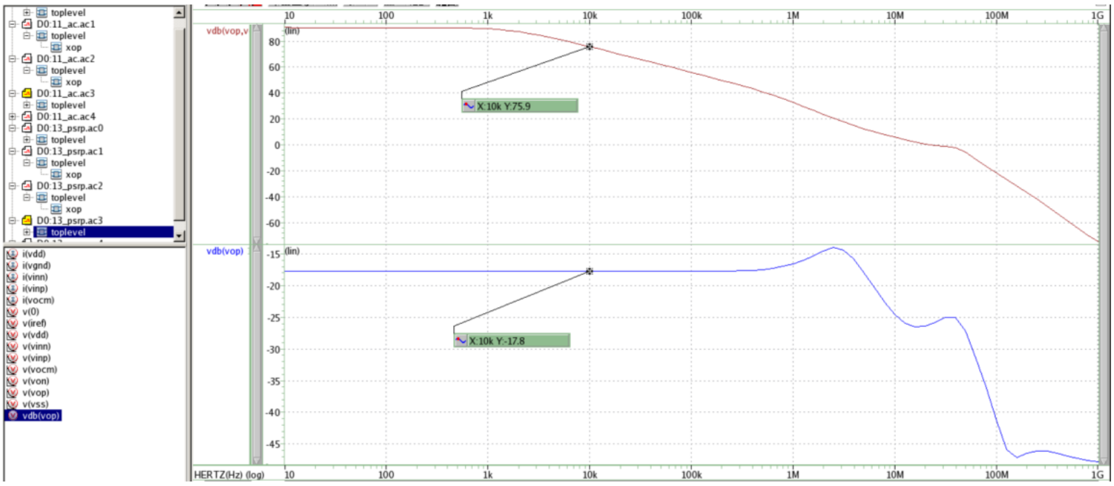
FF: P.S.R.R.+@10KHz=77.9-(-16.4)dB=94.3dB



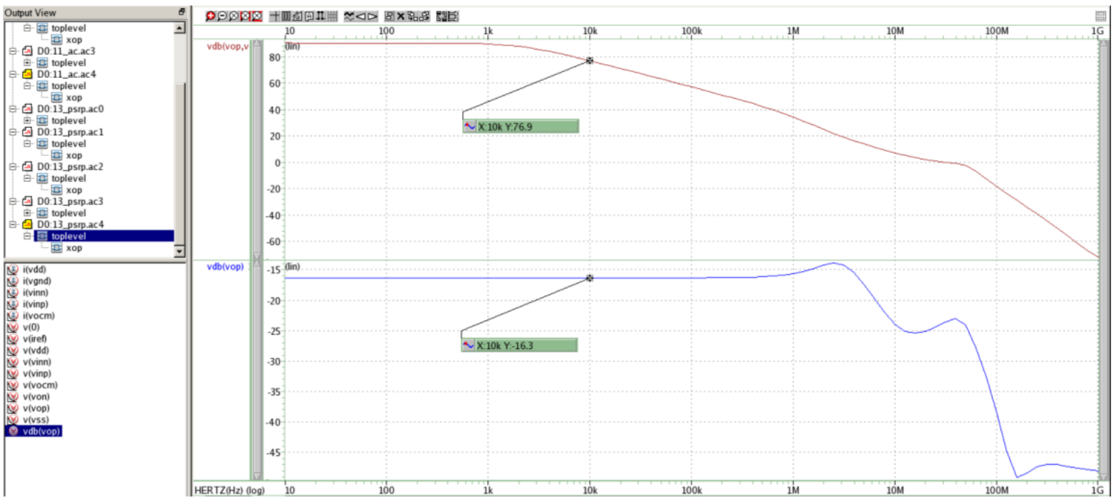
SS: P.S.R.R.+@10KHz=76.3-(-15.1)dB=91.4dB



SF: P.S.R.R.+@10KHz=75.9-(-17.8)dB=93.7dB



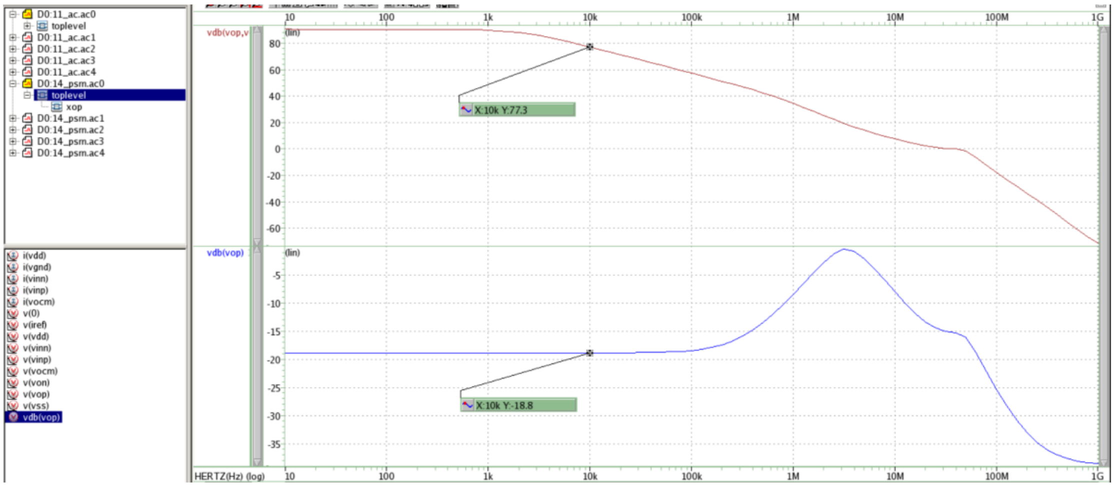
FS: P.S.R.R.+@10KHz=76.9-(-16.3)dB=93.2dB



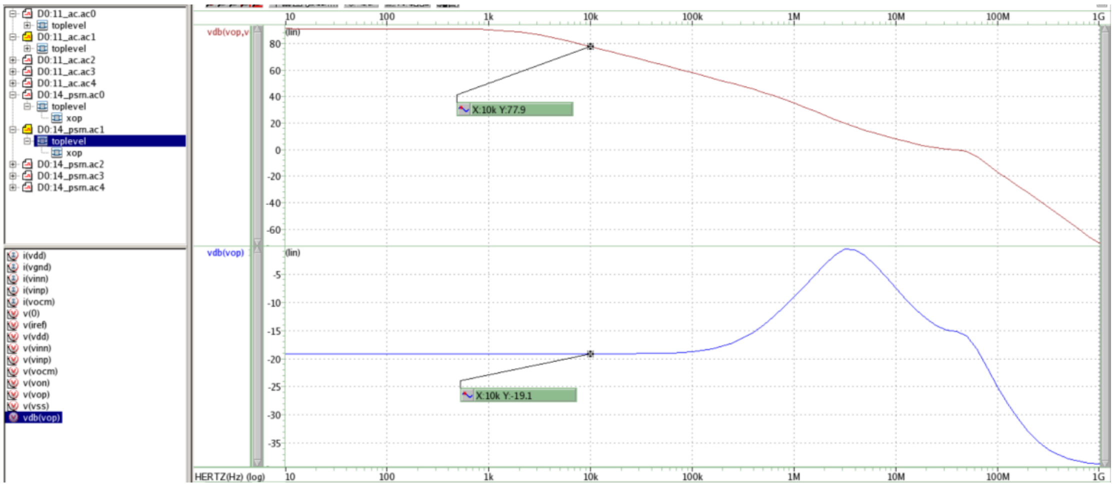
5. P.S.R.R.-@10KHz

$$P.S.R.R._{-} = \frac{A_{DM}}{A_{Vss}}$$

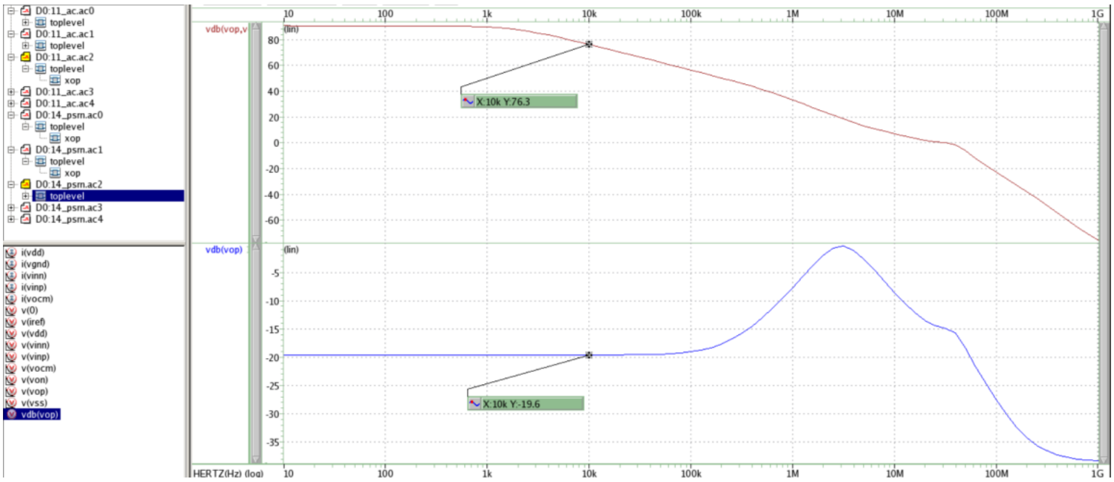
TT: P.S.R.R.-@10KHz=77.3-(-18.8)dB=96.1dB



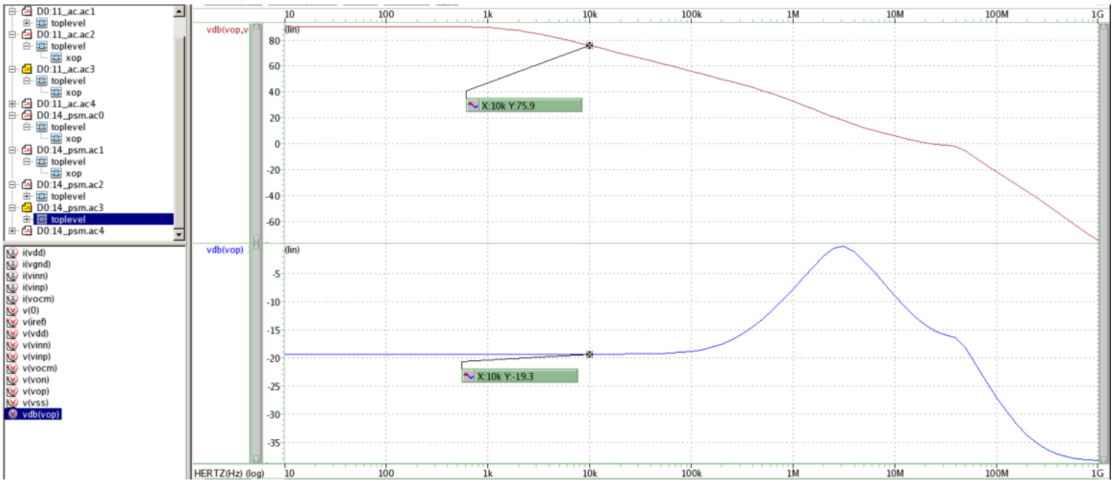
FF: P.S.R.R.-@10KHz=77.9-(-19.1)dB=97dB



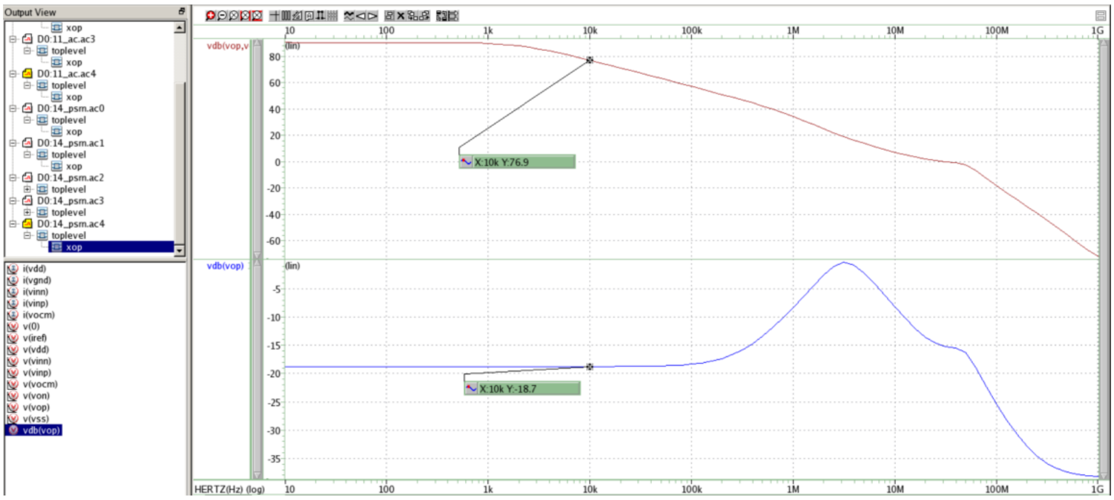
SS: P.S.R.R.-@10KHz=76.3-(-19.6)dB=95.9dB



SF: P.S.R.R.-@10KHz=75.9-(-19.3)dB=95.2dB



FS: P.S.R.R.-@10KHz=76.9-(-18.7)dB=95.6dB



6. S. R. +(10% ~ 90%)

TT: S. R. +(10% ~ 90%)=16.7832 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final= 499.9691m
hlimit= 500.4691m
llimit= 499.4691m
htime= 481.8986n
ltime= 447.2361n
pos_settling= 431.8986n
final1=   1.3200
hlimit1=   1.3213
llimit1=   1.3187
htime1= 385.1499n
ltime1= 225.6361n
pos_settling1= 335.1499n
final2= 820.0401m
hlimit2= 820.8601m
llimit2= 819.2200m
htime2= 352.8558n
ltime2= 475.7635n
pos_settling2= 425.7635n
srp_time=  47.6666n  targ= 107.7377n   trig=  60.0711n
srp=  16.7832x
```

FF: S. R. +(10% ~ 90%)=19.5585 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final= 499.9710m
hlimit= 500.4710m
llimit= 499.4710m
htime= 495.2060n
ltime= 440.5632n
pos_settling= 445.2060n
final1=   1.2882
hlimit1=   1.2895
llimit1=   1.2869
htime1= 364.1463n
ltime1= 449.5509n
pos_settling1= 399.5509n
final2= 788.2536m
hlimit2= 789.0418m
llimit2= 787.4653m
htime2= 334.9893n
ltime2= 490.9031n
pos_settling2= 440.9031n
srp_time=  40.9030n  targ= 100.7376n   trig=  59.8346n
srp=  19.5585x
```

SS: S. R. +(10% ~ 90%)=15.5583 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final= 499.9702m
hlimit= 500.4702m
llimit= 499.4703m
htime= 593.9138n
ltime= 659.4560n
pos_settling= 609.4560n
final1=   1.3502
hlimit1=   1.3515
llimit1=   1.3488
htime1= 449.3254n
ltime1= 516.0012n
pos_settling1= 466.0012n
final2= 850.2075m
hlimit2= 851.0577m
llimit2= 849.3573m
htime2= 500.2929n
ltime2= 573.8635n
pos_settling2= 523.8635n
srp_time=  51.4195n  targ= 113.7018n   trig=  62.2823n
srp=  15.5583x
```

SF: S. R. +(10% ~ 90%)=14.4232 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final= 499.9696m
hlimit= 500.4696m
llimit= 499.4697m
htime= 625.9974n
ltime= 690.2429n
pos_settling= 640.2429n
final1=   1.3420
hlimit1=   1.3433
llimit1=   1.3407
htime1= 485.4812n
ltime1= 400.5842n
pos_settling1= 435.4812n
final2= 842.0367m
hlimit2= 842.8788m
llimit2= 841.1947m
htime2= 545.4092n
ltime2= 612.5346n
pos_settling2= 562.5346n
srp_time=  55.4661n  targ= 117.7920n   trig=  62.3258n
srp=  14.4232x
```

FS: S. R. +(10% ~ 90%)=15.7838 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final= 499.9684m
hlimit= 500.4684m
llimit= 499.4684m
htime= 410.5438n
ltime= 463.0319n
pos_settling= 413.0319n
final1=   1.3267
hlimit1=   1.3280
llimit1=   1.3253
htime1= 409.0892n
ltime1= 332.7006n
pos_settling1= 359.0892n
final2= 826.7067m
hlimit2= 827.5334m
llimit2= 825.8800m
htime2= 448.1344n
ltime2= 295.7666n
pos_settling2= 398.1344n
srp_time=  50.6848n  targ= 111.0293n   trig=  60.3446n
srp=  15.7838x
```

7. S. R. −(10% ~ 90%)

TT: S. R. -(10% ~ 90%)=16.7832 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final=-499.9691m
hlimit=-500.4691m
llimit=-499.4691m
htime= 481.8986n
ltime= 447.2361n
pos_settling= 431.8986n
final1= 820.0401m
hlimit1= 820.8601m
llimit1= 819.2200m
htime1= 352.8558n
ltime1= 475.7635n
pos_settling1= 425.7635n
final2=   1.3200
hlimit2=   1.3213
llimit2=   1.3187
htime2= 385.1499n
ltime2= 225.6361n
pos_settling2= 335.1499n
srn_time=  47.6666n  targ= 107.7377n   trig=  60.0711n
srn=  16.7832x
```

FF: S. R. +(10% ~ 90%)=19.5585 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final=-499.9710m
hlimit=-500.4710m
llimit=-499.4710m
htime= 495.2060n
ltime= 440.5632n
pos_settling= 445.2060n
final1= 788.2536m
hlimit1= 789.0418m
llimit1= 787.4653m
htime1= 334.9893n
ltime1= 490.9031n
pos_settling1= 440.9031n
final2=   1.2882
hlimit2=   1.2895
llimit2=   1.2869
htime2= 364.1463n
ltime2= 449.5509n
pos_settling2= 399.5509n
srn_time=  40.9030n  targ= 100.7376n   trig=  59.8346n
srn=  19.5585x
```

SS: S. R. +(10% ~ 90%)=15.5583 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final=-499.9702m
hlimit=-500.4702m
llimit=-499.4703m
htime= 593.9138n
ltime= 659.4560n
pos_settling= 609.4560n
final1= 850.2075m
hlimit1= 851.0577m
llimit1= 849.3573m
htime1= 500.2929n
ltime1= 573.8635n
pos_settling1= 523.8635n
final2=   1.3502
hlimit2=   1.3515
llimit2=   1.3488
htime2= 449.3254n
ltime2= 516.0012n
pos_settling2= 466.0012n
srn_time=  51.4195n  targ= 113.7018n   trig=  62.2823n
srn=  15.5583x
```

SF: S. R. +(10% ~ 90%)=15.7838 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final= 499.9696m
hlimit= 500.4696m
llimit= 499.4697m
htime= 625.9974n
ltime= 690.2429n
pos_settling= 640.2429n
final1=   1.3420
hlimit1=   1.3433
llimit1=   1.3407
htime1= 485.4812n
ltime1= 400.5842n
pos_settling1= 435.4812n
final2= 842.0367m
hlimit2= 842.8788m
llimit2= 841.1947m
htime2= 545.4092n
ltime2= 612.5346n
pos_settling2= 562.5346n
srp_time=  55.4661n  targ= 117.7920n   trig=  62.3258n
srp=  14.4232x
```

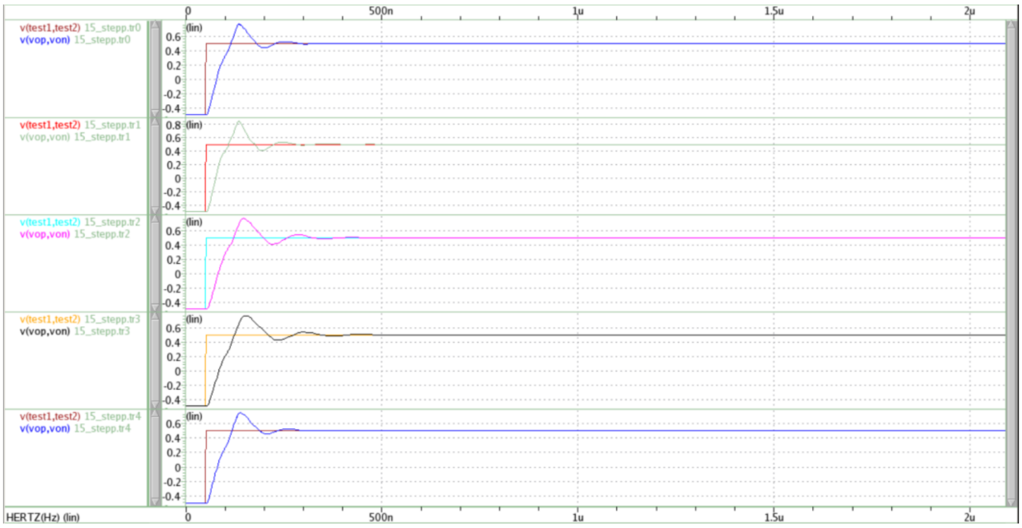
FS: S. R. +(10% ~ 90%)=15.7838 V/us

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final=-499.9684m
hlimit=-500.4684m
llimit=-499.4684m
htime= 410.5438n
ltime= 463.0319n
pos_settling= 413.0319n
final1= 826.7067m
hlimit1= 827.5334m
llimit1= 825.8800m
htime1= 448.1344n
ltime1= 295.7666n
pos_settling1= 398.1344n
final2=   1.3267
hlimit2=   1.3280
llimit2=   1.3253
htime2= 409.0892n
ltime2= 332.7006n
pos_settling2= 359.0892n
srn_time=  50.6848n   targ= 111.0293n   trig=  60.3446n
srn=  15.7838x
```

Comparison:

S.R.+ = S.R.- for all corners, since the opamp has symmetric structures, it’s quite reasonable for S.R.+ equal to S.R.-.

8. Settling +(1Vpp,0.01)



By Figure in SR+ (pos_sattling):

TT Settling +(1Vpp,0.01) = 431.8986ns

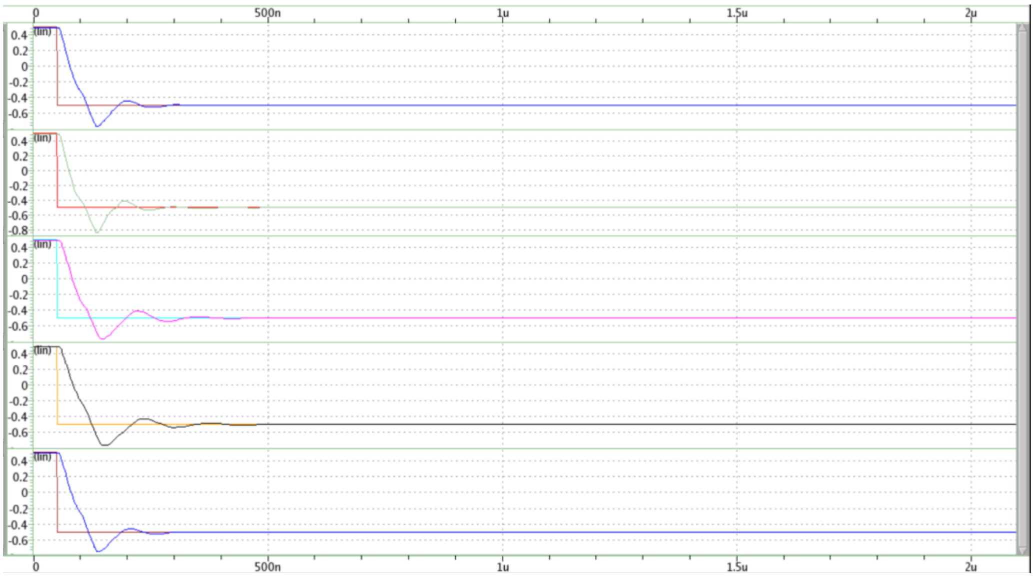
FF Settling +(1Vpp,0.01) = 445.2060ns

SS Settling +(1Vpp,0.01) = 609.4560ns

SF Settling +(1Vpp,0.01) = 640.2429ns

FS Settling +(1Vpp,0.01) = 413.0319ns

9. Settling –(1Vpp,0.01)



By Figure in SR+ (pos_sattling):

TT Settling +(1Vpp,0.01) = 431.8986ns

FF Settling +(1Vpp,0.01) = 445.2060ns

SS Settling +(1Vpp,0.01) = 609.4560ns

SF Settling +(1Vpp,0.01) = 640.2429ns

FS Settling +(1Vpp,0.01) = 413.0319ns

Comparison: settling time+ = settling time-, SF>SS>FF>RR>FS

C. Design procedure and consideration.

1. Fully differential amplifier

(a)gm1: folded cascode differential amplifier

The advantages of the folded cascode are high gain and large swing, by modulating the size of M12,13 and M15 we can achieve the desired gain:

$$A_{v1} = g_{m12} \times R_{out} = g_{m12}(g_{m15}r_{15}r_{14}||r_{16})$$

The first stage has relatively large output resistance, so the output pole of the first stage will directly effects the bandwidth and phase margin of overall opamp, so we must have a trade-off between the gain and pole frequency.

$$\omega_{out,1} = \frac{1}{C_{out}R_{out}} \quad , R_{out} = (g_{m15}r_{15}r_{14}||r_{16})$$

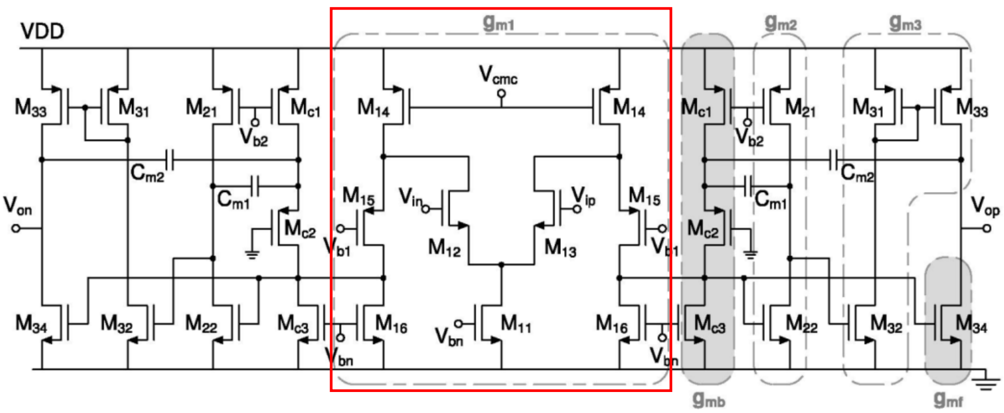


Fig C.a.1: First stage of opamp.

(b)gm2: second common source stage:

The second stage is used to contribute gain to the output, second stage is used so that the bandwidth can be maintain under the same gain:

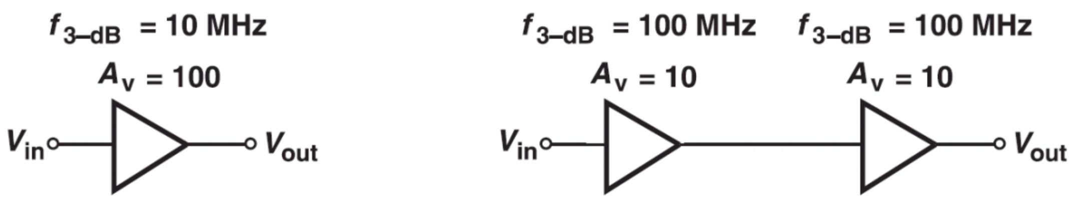


Fig C.b.1: compare of one stage and two stage bandwidth

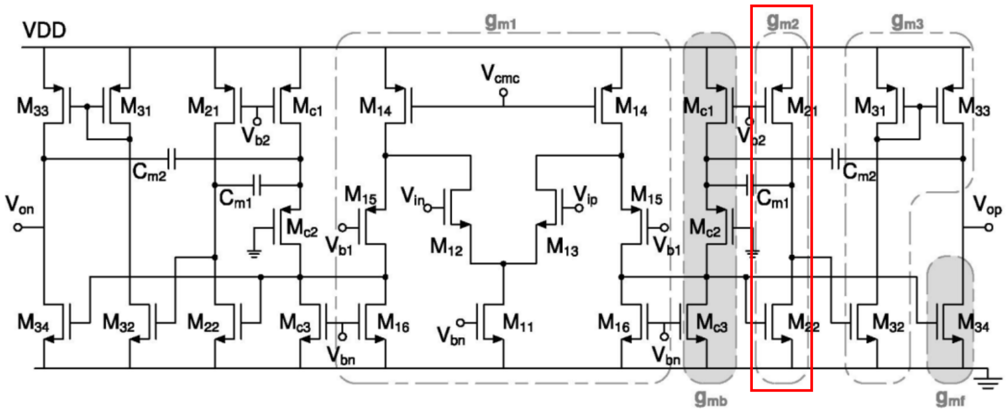


Fig C.b.2: Second stage of the opamp.

(c)gm3+gmf: common source with current mirror and feedforward stage

The feedforward stage, gmf, along with gm3 forms the output push pull stage to improve the slew rate, the slew rate is approximately Iss/Cout.

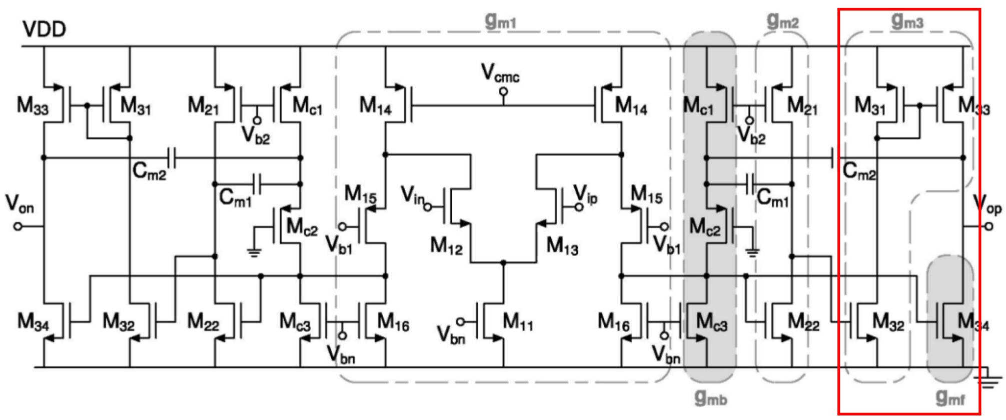


Fig C.c.1: Third stage and feedforward of the opamp.

(d)gmf: feedback stage

Common gate feedback stage gmb is inserted between the common end of two Miller capacitors Cm1 and Cm2, and the output of the gm1 stage. CG part ensure only feedback stage can pass through and eliminate RHS zeros of two miller compensation, thus stabilizes the output.

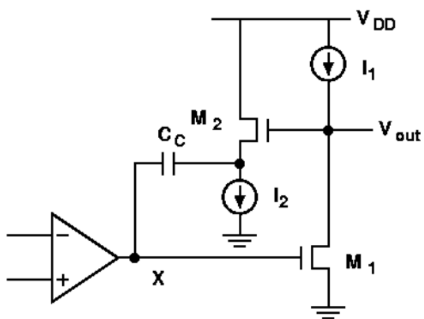


Fig C.c.1: CG feedback frequency compensation.

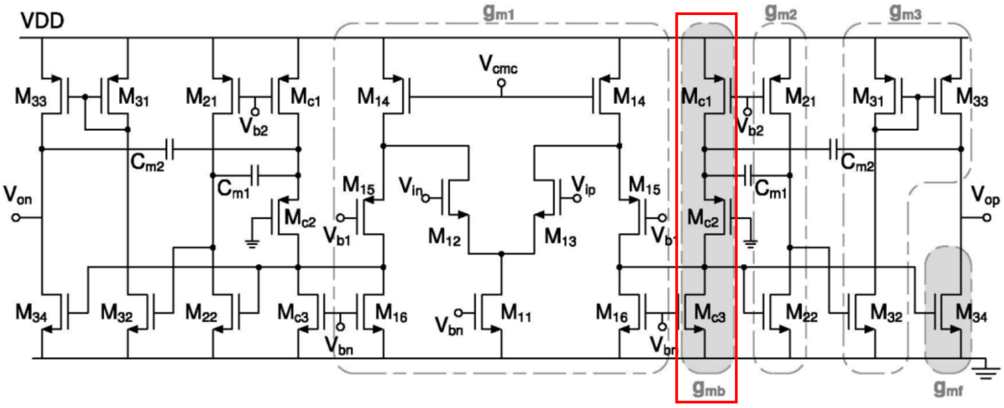


Fig C.c.2: Feedback stage of the opamp.

2. Current compared CMFB circuit

For a fully differential amplifier, a common mode feedback (CMFB) circuit is necessary to set up the common mode voltage of the two output nodes. To attain maximum output swing(0.7V).

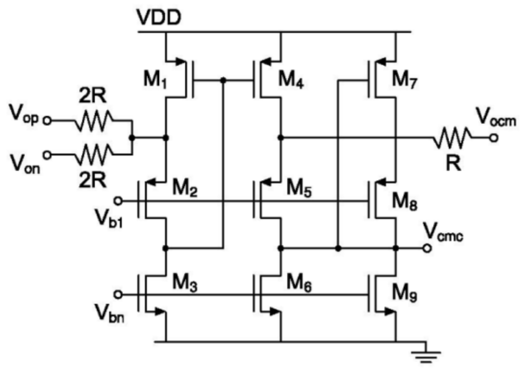


Fig. 4. Current compared CMFB circuit.

By sensing Vop and Von, Vo,cm is the input of the CMFB, when Vo,cm is too high $I_{33}>I_{34}$, Vcmc is lowered, Vgs14 lowered, Vd16=Vgs34 is raised, I_{34} is raised. Thus CMFB stabilizes the DC level.

3.Biasing circuit

We use the HW2.3 to biasing the opamp and CMFB circuits for a stable biasing in each corner, by modulating PMOS's size (W/L) varies the biasing voltage Vb1, Vb2. Iref is also relates to total power dissipation.

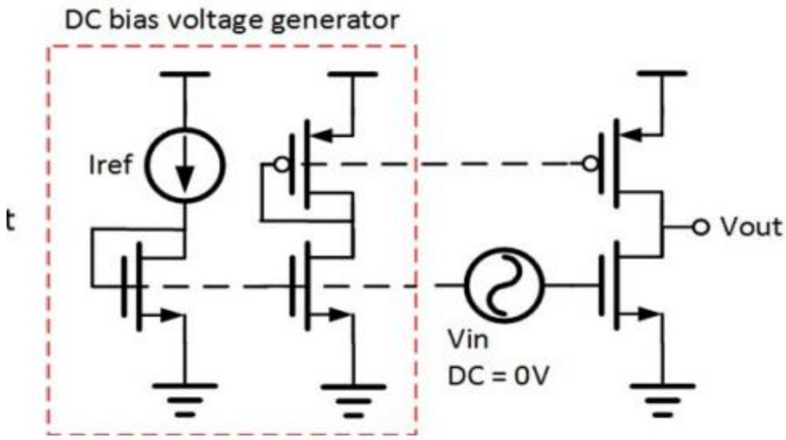


Fig. 3. (b)

Specification:

Design Items	Specifications	TT	SS	SF	FS	FF
Technology	CIC018 pseudo technology					
Supply voltage	<1.8V, low as possible	1.4V	1.4V	1.4V	1.4V	1.4V
Power	<2.5mW (10%) Small as possible	2.4449056 mW	2.4524253 mW	2.447153 mW	2.4465999 mW	2.4238587 mW
Loading	50pF / 15KΩ					
DC gain	> 80dB (10%) large as possible	91.1491dB	91.4377dB	91.20041dB	90.9129dB	91.5394dB
U.G.B.	> 35MHz (10%) large as possible	35.07MHz	**32.35MHz**	**22.68MHz**	**29.46MHz**	**32.51MHz**
P.M.	> 60^{o} (10%)	66.4003	**51.5860**	74.0980	73.934	72.6077
C.M.R.R.@10KHz	> 75db (5%)	92.7dB	92.5dB	92.1dB	92.4dB	93.3dB
P.S.R.R.+@10KHz	> 75db (7.5%)	93.1dB	91.4dB	93.7dB	93.2dB	94.3dB
P.S.R.R.-@10KHz	> 75db (7.5%)	96.1dB	95.9dB	95.2dB	95.6dB	97dB
Unity-gain configuration						
S. R. +(10% ~ 90%)	> 5V/us (7.5%)	16.7832	15.5583	14.4232	15.7838	19.5585
S. R. −(10% ~ 90%)	> 5V/us (7.5%)	16.7832	15.5583	14.4232	15.7838	19.5585
Settling +(1Vpp,0.01)	< 2us (7.5%)	0.4318986	0.4452060	0.6094560	0.6402429	0.4130319
Settling −(1Vpp,0.01)	< 2us (7.5%)	0.4318986	0.4452060	0.6094560	0.6402429	0.4130319
Figure of Merit (FoM)						
Small signal	$\frac{\text{U.G.B.(MHz)}}{\text{Power(mW)}}$ (5%)	14.34411	13.19102	9.267913	12.0412	13.4125
Large signal	$\frac{\text{S.R.(V/us)}}{\text{Power(mW)}}$ (5%)	6.86456	6.344046	5.893869	6.45132	8.069158

D. Discussion and conclusion.

這次的 final project 相較於作業來說難度真的很高，不只是 MOS 數量變多、要注意的所有的 corner，甚至有許多的 spec 要達成。再加上要在期末考週後馬上就要繳交，感覺很像在跟時間賽跑，但完成的瞬間很有成就感。

基本上我們先從閱讀教授提供的論文開始著手，至少要先讀懂這個電路各個部分的功用是甚麼，哪個是 gain stage、哪部分再做頻率補償，並嘗試運用上課所學的知識去推導論文中的公式。接下來我們將電路分成 3 塊：Opamp, CMFB, Bias Circuit 來達成。Opamp 的部分從 gain 和 power 的部分著手，因為我們認為這是最直觀、比較好達成的標準。Gain 可以依靠調大 gm 來達成，而 power 則可以透過降低 Vdd 來達到(因為論文中用的是 1.2V，我們的想法是應該不會用到 1.8V，可以再調低)，基本上因為是三個 gain stage 的 Opamp，所以要達成 gain > 80dB 難度我認為不大。接下來我們接上 CMFB 的部分，這部分最困難的就是不去影響到我們 Opamp 的偏壓狀況，在這部份我們調整 MOS 的 size 很多次來達到我們的目的。最後則是設計 bias circuit 的部分，這部份我們參考作業的作法，由於是作業時做過的，考試中也遇到過很多次，對架構相對熟悉，所以相較於前面的部分輕鬆許多。最後我們在掛上頻率補償用的電容，透過我們在論文中推導的公式去嘗試調整 phase margin 和 UGB，但這部份我們並沒有做到最完美，實在很難從 phase margin 和 UGB 的 trade off 中找到一組都符合 spec 的答案，這個問題記得在 HW4 時也有遇到，當時也時沒有很好的解決(記得是剛好壓線)算是有點可惜，但也完全應證類比電路就是不斷的在做 trade off 這句話，希望未來在累積更多經驗後能解決這部分的問題。

最後是修課心得的部分，當初修這門課的原因是因為電子學(一)修得不錯，再加上教授說這門課基本上是電子學(二)的範圍，對於電機系的學生來說應該要是必備知識，所以才會來修。然而我在第一次作業就發現我過去在電子學一學到的基本上就只是計算、分析電路的技巧，過於理論理想，現實的電路設計需要考慮各方因素，在其中做取捨，公式只是幫助我們找方向的工具，而這門課也讓我充分體會到這個過程。從一開始的 SPICE Monkey，逐漸進化成比較有設計想法的 SPICE Monkey(!?)，雖然每次電路都還是要調很久，但確實感受到自己有在進步，非常感謝教授這學期的指導。