1. Use composer and hsipce to simulate the capacitance characteristic of nMOS as shown in Fig. 1 with body connected to GND = 0V. (20%) (***hint***: .probe DC ctot=par("lx18(MN)"))(use CIC 0.18um hspice model)
   (a) Assume the W/L = 2um/0.2um, m=10, V_G = -1.8V ~ 1.8V. Plot $|C_{G\_total}|=|C_{GS}|+|C_{GD}|+|C_{GB}|$, $|C_{GS}|$ and $|C_{GD}|$ versus V_G .(10%)

   (b) Modify the W/L =20um/0.2um, m=1, redo the simulation and plot $|C_{G\_total}|$ only, comments the capacitance difference compared to (a). (10%)

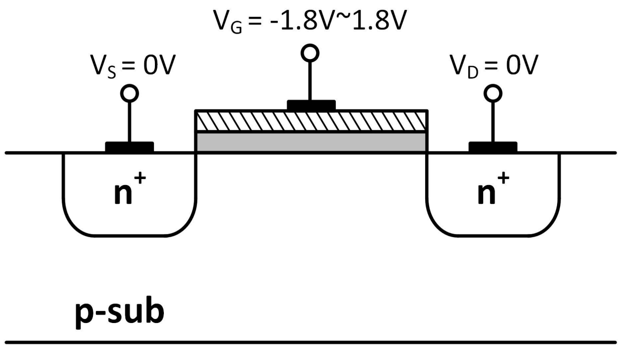

Fig. 1.

2. A common source as shown in Fig. 2 has V_{DD} = 1.8V, Output DC voltage=0.9V, and R=15k-**Ω**. (50%)
   (a) Choose the size (m=1) and the input DC voltage of M1. Use function ".tf v(out) vin" to find the AC gain>8. (5%)
   (b) Find the linear range (1. Definition: 10% gain deviation. 2. Range of both input and output) and gain of this common source with voltage transfer curve V_{in} vs. V_{out} only. (10%)
   (c) Use the same width and length with m=10 to find input DC voltage again. And redo the (b). (15%)
   (d) Comment on what makes the difference of gain and linear range between (b) and (c). (20%)

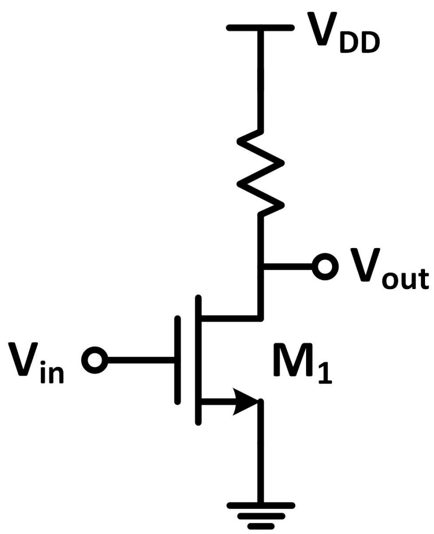

Fig. 2.

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3. Choose two nMOS (1.8V devices) with W/L = 5um/0.2um and W/L = 5um/2um. Use HSPICE DC sweep analysis to show the ID-VDS characteristic waveforms with VGS = 0, 0.3, 0.6, 0.9, 1.2, 1.5 and 1.8V as shown in Fig. 3. Comment the characteristics difference between long-channel and short-channel devices. (20%)

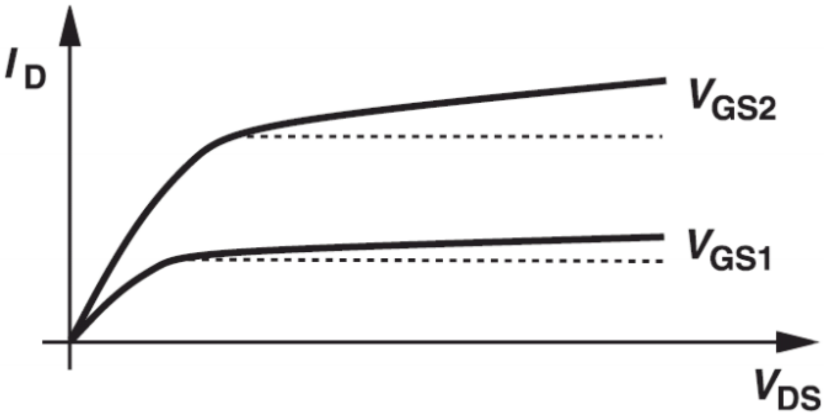

Fig. 3.

✧ ***The following should be included in your report (a) screenshot of Composer schematic and simulation waveform with cursor values (b) your comments.***

by CCHsieh