2022 Analog IC Design Homework 2 ***due date: 04/16/2022***

by CCHsieh

1. Design a source-follower amplifier with Vdd=1.8V as shown in Fig. 1. (30%)
   (a) Design the W/L sizes and Vb to get voltage gain Av=Vout/Vin>0.8 for Vin DC voltage from 0.5V to 1.8V. (10%)
   (b) Assume the deep-nwell is available. Design the W/L sizes and Vb to get voltage gain Av=Vout/Vin>0.96 for Vin DC voltage from 0.5V to 1.8V. (10%)
   (c) Comment on the differences between (a) and (b). (10%)

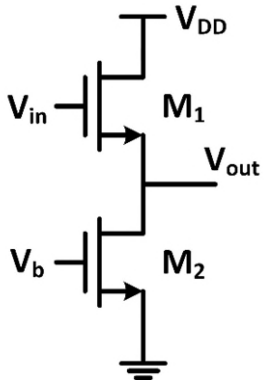

Fig. 1.

2. Design a common-source amplifier with cascode loading as shown in Fig. 2. (20%)
   (a) With Vdd=1.8V and Ibias=10uA, design the W/L sizes of M1~M4, the dc bias to get voltage gain Av=Vout/Vin>50dB and Vout-swing>1.2V. (10%)
   (b) Keep W/L as the same and double all of m(finger) in (a), check the differences of the bias current, voltage gain and output swing and make a comment. (10%)

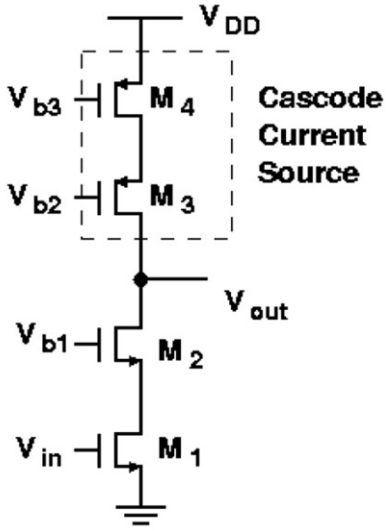

Fig.2

3. Design a common-source amplifier with Vdd=1.8V as shown in Fig. 3. (40%)
   (a) Design the W/L sizes and Vb as shown in Fig. 3.(a) to get voltage gain Av=Vout/Vin>100. (10%)
   (b) Keep everything the same and simulate the gain under the SF and FS corner.(10%)
   (c) Design the W/L sizes and Iref as shown in Fig. 3.(b) to get voltage gain Av=Vout/Vin>100 for all corners. (10%)
   (d) Comment on the differences between (b) and (c). (10%)

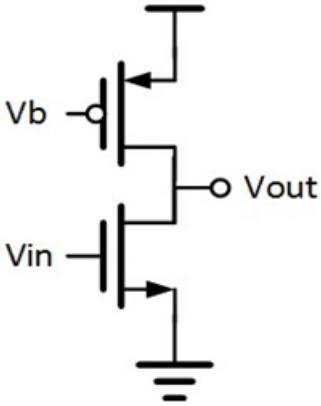

Fig. 3. (a)

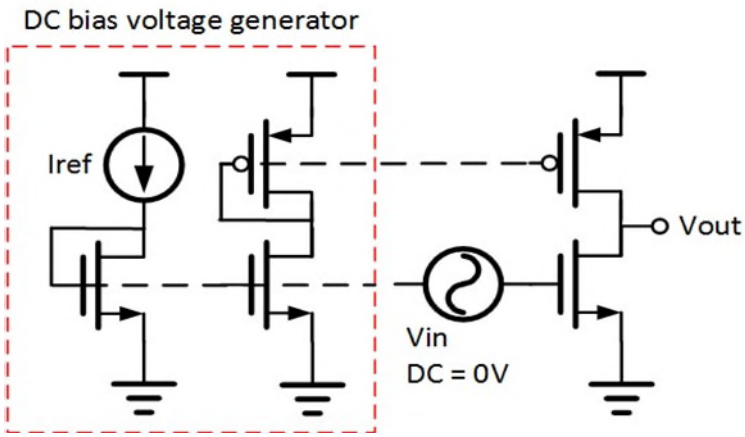

Fig. 3. (b)

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***

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