HW4　　109061217 林峻霆

1. Differential In Single-Ended Out

(a)(b)

這題要做一個 Differential In Single-ended Out 的 Amplifier。這題的難度我認為不大，因為 spec 只要求 A_V = 20dB 以及 BW = 5MHz。基本上只要讓所有的 MOS 偏壓在 Saturation 基本上就能達到了。下面列出 A_V 和 BW 的公式幫助我們找方向

$$A_v \approx g_{mN}(r_{ON} \parallel r_{OP}) = \frac{2}{(\lambda_N + \lambda_P)V_{ov}}$$

$$BW \approx \frac{1}{R_{out}C_L} = \frac{(\lambda_N + \lambda_P)I_D}{C_L}$$

而我們可以調的參數分別是：

1. Differential pair 的 MOS 的 size -> 影響 λ, Vov
2. Current Source 的 MOS 的 size -> 影響 Vov, I_D
3. V_b -> 影響 V_{ov}, I_D
4. V_{icm} -> 影響 operating point

可以看出 λ在 Gain 和 BW 之間是反向的關係，而 I_D 和 V_{ov} 雖然是正向關係，但一個在分母一個在分子，因此這個會是我們 design 的一個限制，我們必須在兩者間作 tradeoff。但 λ基本上只受 differential pair 的 size 中的 L 影響，所以我們可以不調整他們的 L，用其他來達成 spec。假設 C_L 固定，我的方向如下：**調高 ID -> Vov 變大, gain 變小**

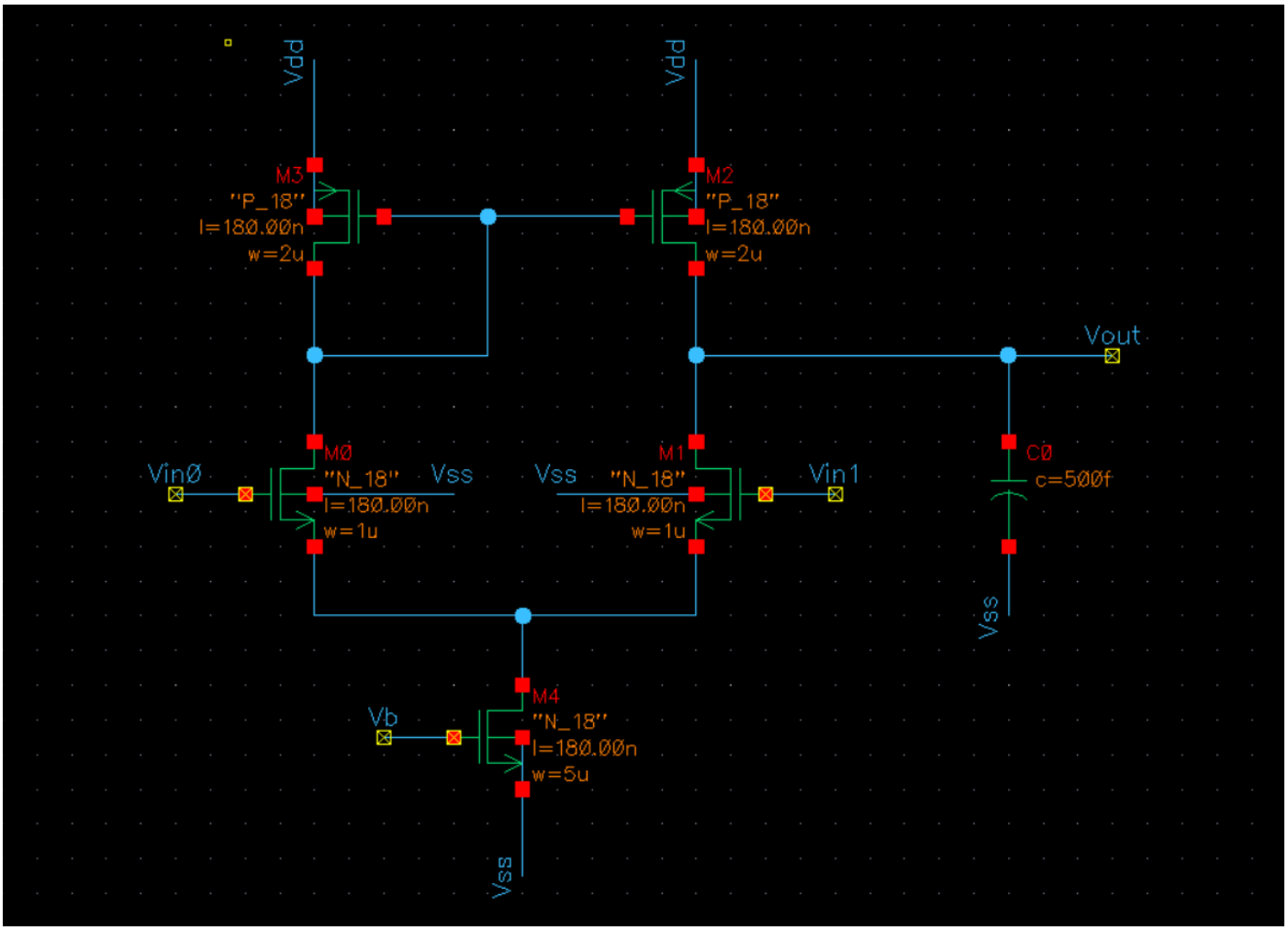
->調高 differential pair 的 W

->Vov 變小，gain 變大

事實上，我自己實作時只做完第一步就達成 spec 了。不過這個策略對後續的題目有幫助。

Schematic

我們取 Vb = 0.55V, Vicm = 1.3V



```
**** mosfets


subckt
element  0:mm3      0:mm2      0:mm1      0:mm0      0:mm4
model    0:p_18.1   0:p_18.1   0:n_18.1   0:n_18.1   0:n_18.1
region   Saturation Saturation Saturation Saturation Saturation
 id       -18.1314u  -18.1314u   18.1314u   18.1314u   36.2628u
 ibs      2.478e-21  2.478e-21  -50.4203a  -50.4203a -6.417e-21
 ibd       88.2657a   88.2657a -118.7050a -118.7050a -149.6343a
 vgs      -671.7110m -671.7110m  648.2353m  648.2353m  550.0000m
 vds      -671.7110m -671.7110m  476.5243m  476.5243m  351.7647m
 vbs        0.         0.       -351.7647m -351.7647m    0.
 vth      -534.5841m -534.5841m  548.5272m  548.5272m  512.5768m
 vdsat    -191.3452m -191.3452m  142.3676m  142.3676m  103.6204m
 vod      -137.1269m -137.1269m   99.7081m   99.7081m   37.4232m
 beta       1.1502m    1.1502m    1.9991m    1.9991m    9.9805m
 gam eff  557.0845m  557.0845m  516.4853m  516.4853m  507.4463m
 gm       183.4018u  183.4018u  209.3913u  209.3913u  564.9433u
 gds        6.5198u    6.5198u   11.2940u   11.2940u   29.4075u
 gmb       55.2108u   55.2108u   23.5626u   23.5626u   84.3221u
 cdtot      2.4229f    2.4229f    1.4042f    1.4042f    7.1957f
 cgtot      3.7584f    3.7584f    1.8202f    1.8202f    8.3931f
 cstot      5.4364f    5.4364f    2.5513f    2.5513f   12.0865f
 cbtot      4.6917f    4.6917f    2.4162f    2.4162f   12.6990f
 cgs        2.8008f    2.8008f    1.3109f    1.3109f    5.6226f
 cgd      707.5300a  707.5300a  359.5321a  359.5321a    1.8394f
```

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gaindb=  21.2022     at= 500.0000k
           from= 500.0000k    to=  12.5594g
band=   5.5010x
```

Hand Calculation : $A_v \approx g_{mN}(r_{ON} \,||\, r_{OP}) = 209.3913u * \frac{1}{11.2940u+6.5198u} = 11.754 = 21.4dB$

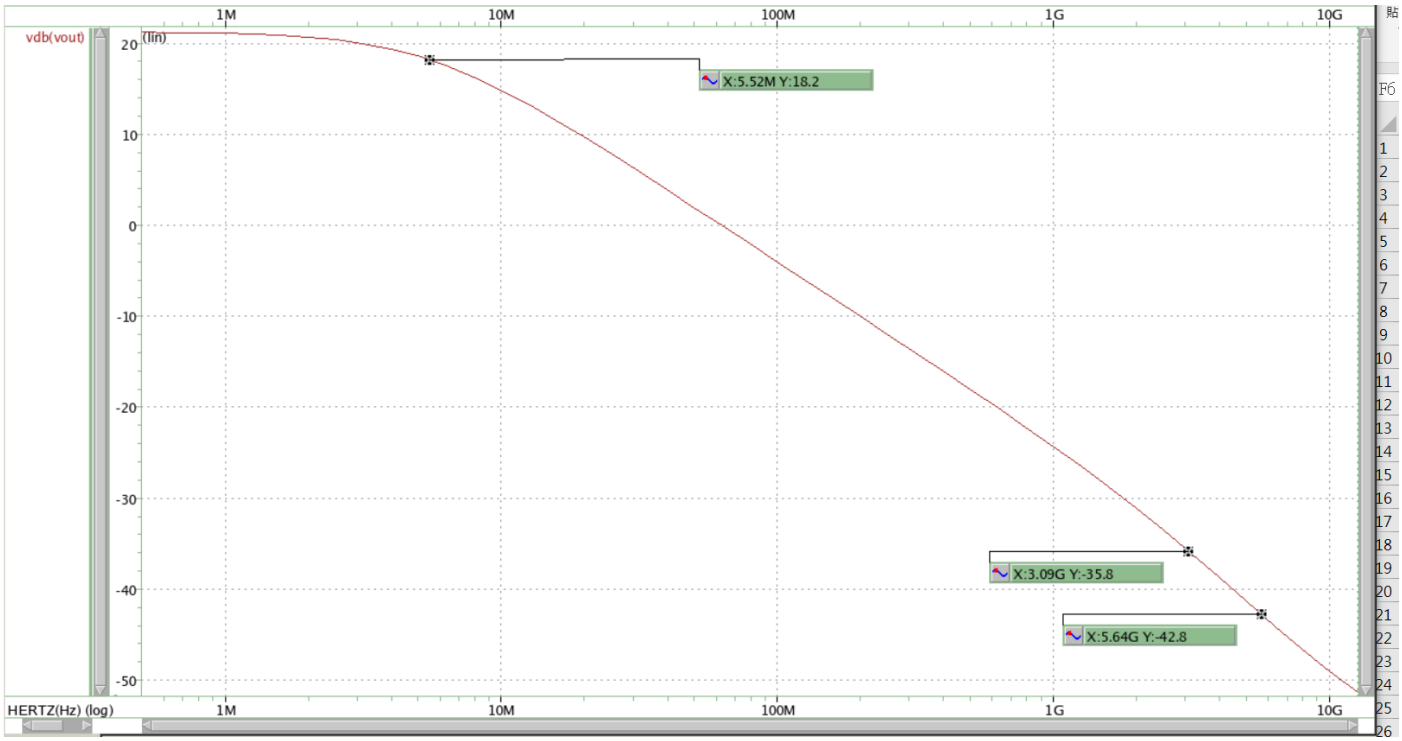
Simulation : 21.2022dB

基本上差距也不大，跟模擬跟計算結果十分接近。

(c)(d)

```
**************************************************
  ******   pole/zero analysis


    input =  0:vac          output = v(vout)

       poles (rad/sec)                poles ( hertz)
real            imag           real            imag
-34.3546x       0.             -5.46770x       0.
-19.3616g       0.             -3.08149g       0.
-42.9941g       0.             -6.84273g       0.

       zeros (rad/sec)                zeros ( hertz)
real            imag           real            imag
-35.3478g       0.             -5.62578g       0.
-48.4487g       0.             -7.71086g       0.
533.314g        0.             84.8796g        0.
```

```
   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:in      =   0.      0:net19   =  11.3439f 0:net22   =  12.2984f
+0:vb      =   8.3931f 0:vdd     =  20.2561f 0:vicm    =   0.
+0:vin0    =   1.8202f 0:vin1    =   1.8202f 0:vout    = 503.8272f
+0:vss     = 529.6180f
```



Hand Calculation :

1. **Output Pole** $\approx \frac{1}{R_{out}C_L} = \frac{1}{\frac{1}{11.2940u+6.5198u} * 503.8272f}$ = 35.357M(rad/s)

2. **Mirror Pole** $\approx \frac{g_{mp}}{C_E} = \frac{183.4018u}{12.2984f} = 14.9G(rad / s)$

3. **First Zero** $\approx 2\omega_{p2} = 29.8G(rad / s)$

Simulation :

1. **Ouput Pole** = 5.62578M * 2pi = 35.348M(rad / s)

2. **Mirror Pole** = 7.71086G * 2pi = 15.422G(rad / s)

3. **First Zero** = 5.62578G * 2pi = 35.348G(rad / s)

(e)(f)

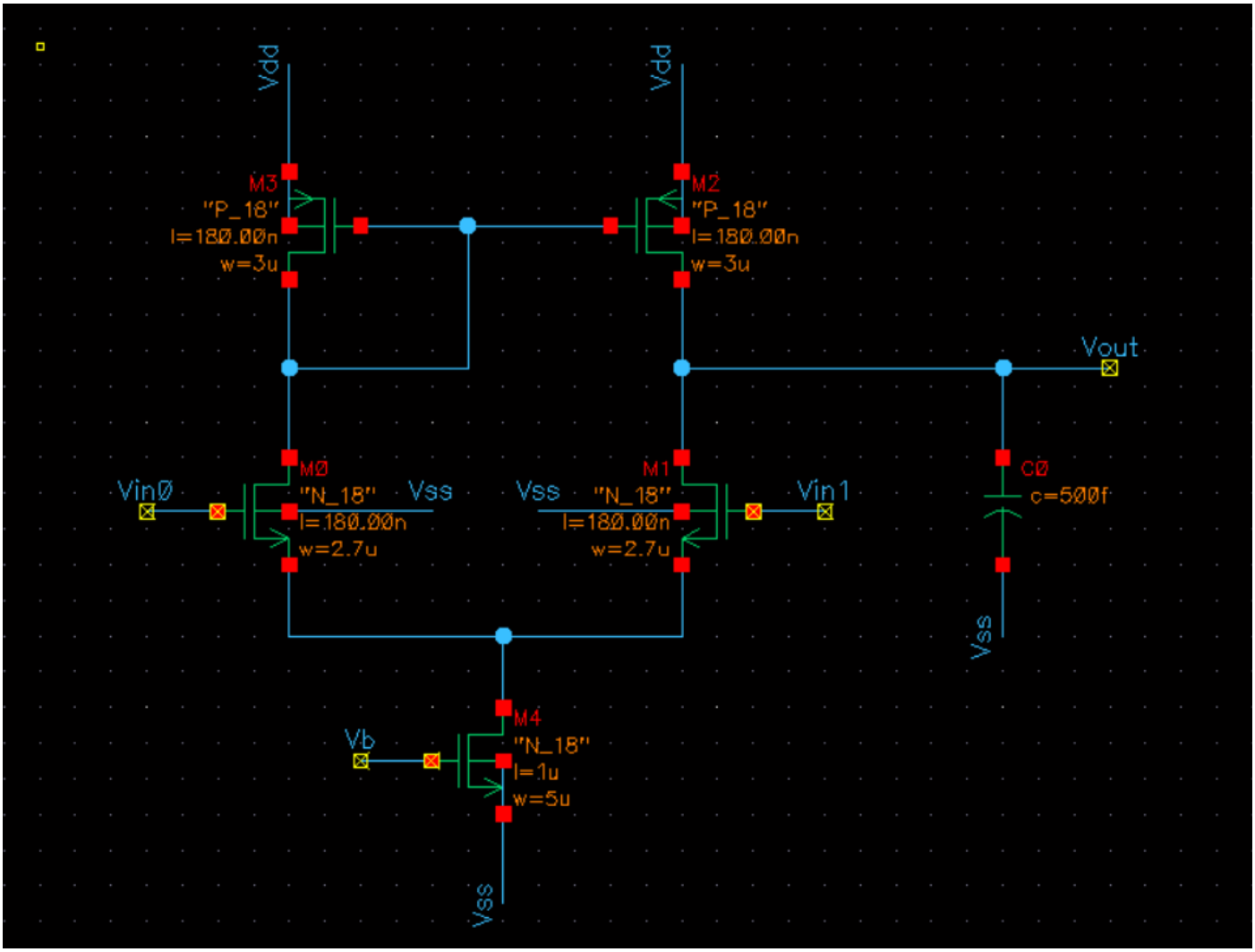
這題希望我們去 maximize FOM，這應該是這次作業最困難的部分。一樣我們先列個算式找方向

$$FOM = \frac{BW(MHz)}{Tail\ Current(uA)} = \frac{(\lambda_N + \lambda_P)I_D}{2I_D C_L} = \frac{(\lambda_N + \lambda_P)}{C_L}$$

可以看到基本上他只跟 λ和 C_L 有關。λ跟 Differential pair 的 MOS 的 L 有關，而 C_L 則與 W*L 有關 (MOS 本身的寄生電容並聯 load capacitance)。λ跟 1 / L 呈正比，但注意到我們在(a)中 L 已經是 0.18um(最小 L in CIC018)。在不做大修改之下 MOS 的寄生電容不太能影像 load capacitance，只能透過 V_{bias} 和 V_{icm} 進行微調來做精進。

另一種想法是，把 size 變大去影響 load capacitance，但是這要注意的地方是這個方法往往會大幅影響 gain，或者是掉出 saturation region。因此我最後是採取原先的架構進行微調，嘗試在 BW 不變的情況下去降低 Tail Current。

Schematic



With V_{icm} = 1.303V, V_b = 0.56V

**** mosfets

subckt					
element	0:mm3	0:mm2	0:mm1	0:mm0	0:mm4
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation
id	-11.9027u	-11.9027u	11.9027u	11.9027u	23.8053u
ibs	1.446e-21	1.446e-21	-180.9911a	-180.9911a	-4.213e-21
ibd	105.5285a	105.5285a	-236.2364a	-236.2364a	-292.5164a
vgs	-602.4497m	-602.4497m	615.3634m	615.3634m	560.0000m
vds	-602.4497m	-602.4497m	209.9137m	209.9137m	687.6366m
vbs	0.	0.	-687.6366m	-687.6366m	0.
vth	-534.1576m	-534.1576m	607.1894m	607.1894m	386.6257m
vdsat	-136.3237m	-136.3237m	93.0308m	93.0308m	167.9130m
vod	-68.2921m	-68.2921m	8.1740m	8.1740m	173.3743m
beta	1.7990m	1.7990m	5.4011m	5.4011m	1.5576m
gam eff	557.0846m	557.0846m	523.9725m	523.9725m	507.4462m
gm	167.5044u	167.5044u	204.2781u	204.2781u	232.5681u
gds	5.0874u	5.0874u	14.9580u	14.9580u	2.8022u
gmb	49.5661u	49.5661u	22.3644u	22.3644u	46.0179u
cdtot	3.6082f	3.6082f	3.5658f	3.5658f	6.7449f
cgtot	5.3455f	5.3455f	3.9996f	3.9996f	34.4447f
cstot	7.6037f	7.6037f	5.2838f	5.2838f	38.7294f
cbtot	6.9071f	6.9071f	5.7522f	5.7522f	18.7259f
cgs	3.8241f	3.8241f	2.5477f	2.5477f	30.0903f
cgd	1.0629f	1.0629f	1.0058f	1.0058f	1.7771f

```
gaindb=  20.0031     at= 500.0000k
           from= 500.0000k    to=  12.5594g
band=   6.0514x
```

nodal capacitance table

node	=	cap	node	=	cap	node	=	cap
+0:in	=	0.	0:net19	=	17.8649f	0:net22	=	17.3126f
+0:vb	=	34.4447f	0:vdd	=	29.0215f	0:vicm	=	0.
+0:vin0	=	3.9996f	0:vin1	=	3.9996f	0:vout	=	507.1740f
+0:vss	=	568.9597f						

Working item	Spec	Simulation	Calculation
Vdd	1.5V		
C_L	500fF		
Tail Current(uA)	Open	23.8053u	
Av(dB)	>20dB	20.0031	20.164
V_{icm}	>20dB	1.303V	
V_{ocm}	Open	23.8053uA	
V_b	Open	0.56V	
Size of NMOS	Open	$\frac{W}{L} = \frac{2.7u}{0.18u}$ $m = 1$	
Size of PMOS	Open	$\frac{W}{L} = \frac{3u}{0.18u}$ $m = 1$	
Size of Current Source	Open	$\frac{W}{L} = \frac{5u}{1u}$ $m = 1$	
BW(MHz)	>5MHz	6.0514	6.29
FOM	BW / Tail Current	0.254	0.264

Hand Calculation

1. $A_v \approx g_{mN}(r_{ON} \,||\, r_{OP}) = 204.2781u * \frac{1}{14.958u+5.087u} = 10.191 = 20.164dB$

2. BW $\approx \frac{1}{R_{out}C_L} = \frac{1}{\frac{1}{14.958u+5.087u}*507.174f} = 39.522$M(rad / s) = 6.29MHz

3. FOM = $\frac{BW(MHz)}{Tail\ Current(uA)} = \frac{6.29}{23.8053} = 0.264$

基本上都跟 simulation 差異不大，誤差基本上來自於數值誤差以及計算的公式本來就只是幫助我們找方向而已。

2. Two Stage Amplifier

(a)

這題要做一個 Two Stage Amplifier。他有兩個 Gain Stage，而我們希望能達到 Gain > 60dB、Unity Gain Frequency > 60MHz 以及 PM > 45^o，後兩者我們可以靠 frequency compensation 來達成，但前提要是我們希望還沒做頻率補償前的 Unity Gain Frequency 能 >60MHz 以及它是一個 stable system(negative phase at unity gain)。

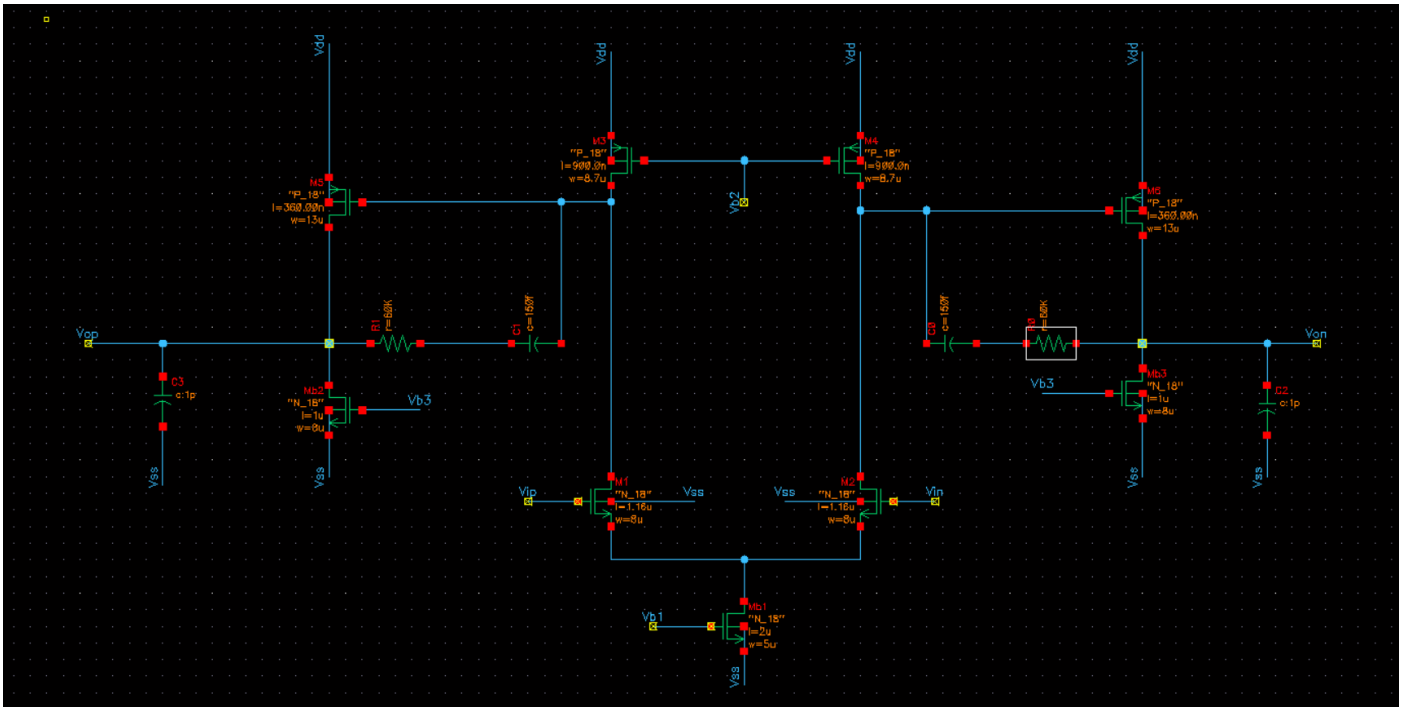
Gain > 60dB(也就是 gain > 1000)，基本上不難達成，因為它是一個 two stage Amplifier，而且兩個 stage 都有 high gain。所以我們應該把目標放在 Unity Gain Frequency，如果 first pole 太小，gain 會很快就 drop 到 unity gain。所以我們希望把 first pole 拉大。下面列出公式找方向：

$$A_v = g_{mn}(r_{o1} \parallel r_{o3}) \cdot g_{mp}(r_{o5} \parallel r_{omb2})$$

要把 pole 調大就是要把 capacitance 調小，也就是 Second Stage W*L 要小，size 不能太大。我的方向如下：

1. 相較於 gain，更在意 pole 的位置
2. 將 pole 和 negative phase at unity gain 這兩個 spec 先達成
3. 最後再透過調整 first stage 的 size 來幫助達成 60dB，並透過 bias 來讓所有 MOS 掉進 Saturation region。

Schematic



The information of the Circuit			
MOS	W/L	Bias	Voltage
M_{b1}	$\frac{5u}{2u}$	V_{b1}	0.45V
M_{b2}	$\frac{8u}{1u}$	V_{b2}	0.95V
M_{b3}	$\frac{8u}{1u}$	V_{b3}	0.48V
$M_{1,2}$	$\frac{8u}{1.16u}$	V_{icm}	1.29V
$M_{3,4}$	$\frac{8.7u}{0.9u}$	V_{ocm}	0.554V
$M_{5,6}$	$\frac{13u}{0.36u}$		

**** mosfets

subckt element	0:mm3	0:mm4	0:mm2	0:mm1	0:mm6	0:mmb3
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:n_18.1
region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation
id	-2.3220u	-2.3220u	2.3220u	2.3220u	-14.7403u	14.7403u
ibs	2.357e-22	2.357e-22	-492.9581a	-492.9581a	1.445e-21	-2.441e-21
ibd	246.4143a	246.4143a	-585.7830a	-585.7830a	579.7663a	-352.7806a
vgs	-550.0000m	-550.0000m	516.0774m	516.0774m	-580.3451m	480.0000m
vds	-580.3451m	-580.3451m	145.7323m	145.7323m	-946.1456m	553.8544m
vbs	0.	0.	-773.9226m	-773.9226m	0.	0.
vth	-496.1212m	-496.1212m	515.7103m	515.7103m	-510.4083m	386.1997m
vdsat	-94.0787m	-94.0787m	66.6708m	66.6708m	-114.6507m	113.4557m
vod	-53.8788m	-53.8788m	367.0445u	367.0445u	-69.9368m	93.8003m
beta	700.3310u	700.3310u	2.1587m	2.1587m	2.8229m	2.4890m
gam eff	557.0847m	557.0847m	525.7629m	525.7629m	557.0846m	507.4460m
gm	38.5668u	38.5668u	50.9119u	50.9119u	222.9552u	211.9540u
gds	148.0679n	148.0679n	1.2971u	1.2971u	1.7167u	2.4514u
gmb	11.5641u	11.5641u	7.3358u	7.3358u	65.7081u	43.0371u
cdtot	10.2389f	10.2389f	10.5130f	10.5130f	14.2914f	10.9838f
cgtot	45.8433f	45.8433f	40.0861f	40.0861f	32.1998f	54.0808f
cstot	52.2698f	52.2698f	38.0066f	38.0066f	41.1435f	60.5007f
cbtot	30.5267f	30.5267f	25.8339f	25.8339f	30.7396f	30.2449f
cgs	37.4762f	37.4762f	29.4700f	29.4700f	24.8505f	46.7345f
cgd	3.1270f	3.1270f	2.9757f	2.9757f	4.6648f	2.8497f

subckt element	0:mm5	0:mmb2	0:mmb1
model	0:p_18.1	0:n_18.1	0:n_18.1
region	Saturation	Saturation	Saturation
id	-14.7403u	14.7403u	4.6440u
ibs	1.445e-21	-2.441e-21	-8.218e-22
ibd	579.7663a	-352.7806a	-329.2259a
vgs	-580.3451m	480.0000m	450.0000m
vds	-946.1456m	553.8544m	773.9226m
vbs	0.	0.	0.
vth	-510.4083m	386.1997m	350.3152m
vdsat	-114.6507m	113.4557m	112.0485m
vod	-69.9368m	93.8003m	99.6848m
beta	2.8229m	2.4890m	759.2604u
gam eff	557.0846m	507.4460m	507.4460m
gm	222.9552u	211.9540u	65.5859u
gds	1.7167u	2.4514u	542.3017n
gmb	65.7081u	43.0371u	13.2093u
cdtot	14.2914f	10.9838f	6.6403f
cgtot	32.1998f	54.0808f	66.0516f
cstot	41.1435f	60.5007f	70.3517f
cbtot	30.7396f	30.2449f	27.4347f
cgs	24.8505f	46.7345f	58.5407f
cgd	4.6648f	2.8497f	1.7204f

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gaindb=  65.5038     at=   1.0000k
           from=   1.0000k    to=  10.0000g
unit_gain=  73.0526x
phase_p=-176.0957
```

Hand Calculation :

$$A_v = g_{mn}(r_{o1} \parallel r_{o3}) \cdot g_{mp}(r_{o5} \parallel r_{omb2})$$

$$= 50.9119u \cdot \frac{1}{1.2971u + 0.148u} \cdot 222.9552u \cdot \frac{1}{1.7167u + 2.4514u} = 1884 = 65.504dB$$

基本上滿接近的，沒什麼誤差，而且也有滿足我們的 spec

1. 65.5038dB > 60dB
2. 73.0526MHz > 60MHz
3. -180^o < Phase < 0^o (在 unity gain 前兩個 pole)。

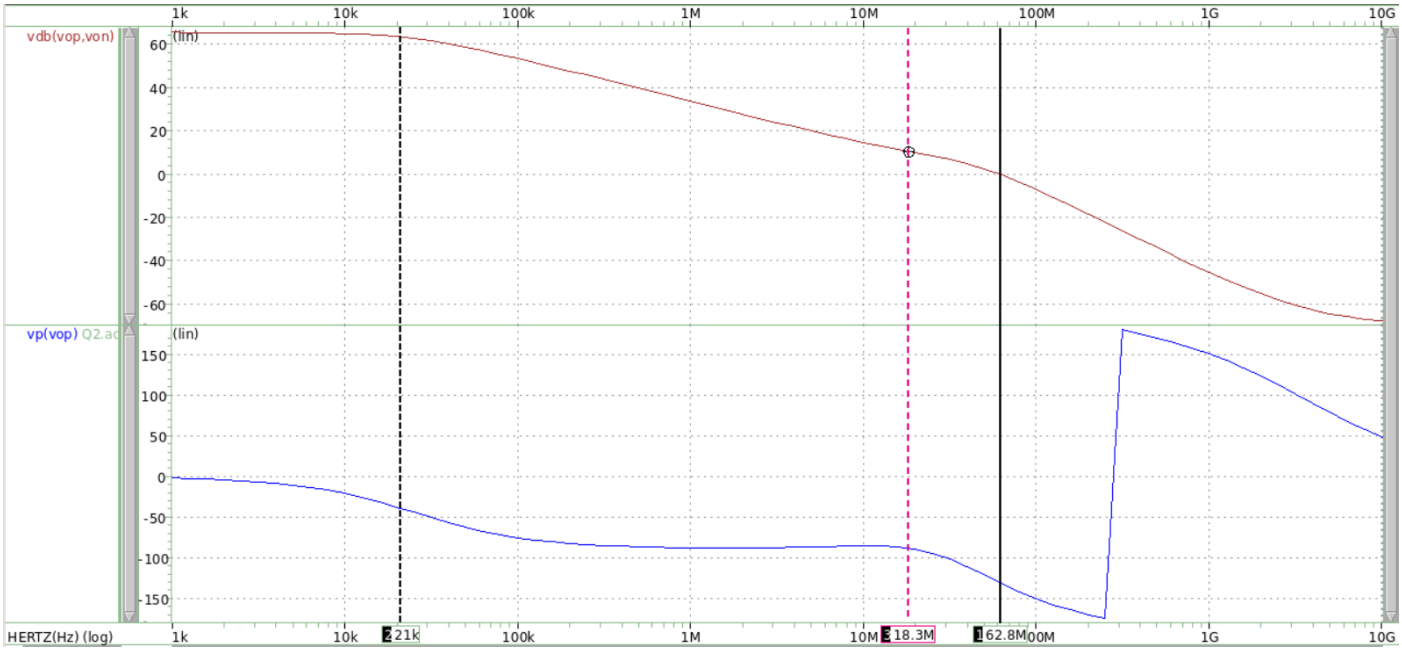
(b)

接著下面就開始做頻率補償啦！

以下是這個 design 用的 R_c 和 C_c，(e)的表格就先附在這裡了：

Performance Table		
Vdd	1.5V	
R_c, C_c	60kΩ	150fF
V_{icm}	1.29V	
V_{ocm}	0.554	
Open-Loop Performance		
A_{DM}(> 60dB)	65.4974dB	
Unity Gain frequency(1pF load)(>60MHz)	61.5079MHz	
Phase Margin(> 45^o)	49.5762^o	

下面是有做頻率補償的 bode plot



以下為 pole 和 zero 的位置：

1. First Pole 在 f = 21KHz = 131k(rad / s)，可以看到從這點開始，gain 開始 drop
2. Zero 在 f = 18.3MHz = 115k(rad / s)，在這個點 gain drop 的幅度變小，因為 zero 可以提供 +20dB/dec，剛好抵銷掉前一個 Pole 的影響。
3. Second Pole 出現在 62.8MHz = 394.6M(rad / s)，可以看到在這個點之後 gain 再次 drop。

```
******   pole/zero analysis


   input =  0:vac          output = v(vop,von)

      poles (rad/sec)                  poles ( hertz)
real            imag            real            imag
-162.604k       0.              -25.8793k       0.
-244.879x       -125.997x       -38.9737x       -20.0530x
-244.879x       125.997x        -38.9737x       20.0530x

      zeros (rad/sec)                  zeros ( hertz)
real            imag            real            imag
-120.064x       0.              -19.1088x       0.
13.7786g        0.              2.19293g        0.
44.1062g        0.              7.01973g        0.
```

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
gaindb=  65.4974     at=   1.0000k
           from=   1.0000k    to=  10.0000g
unit_gain=  61.5079x
phase_p=-130.4238
```

```
   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:in      =   0.      0:net15   = 202.9517f 0:net3    = 150.0000f
+0:net40   =  82.6536f 0:net41   = 202.9517f 0:net7    = 150.0000f
+0:vb1     =  66.0516f 0:vb2     =  91.6867f 0:vb3     = 108.1615f
+0:vdd     = 309.3594f 0:vicm    =   0.      0:vin     =  40.0861f
+0:vip     =  40.0861f 0:von     =   1.0253p 0:vop     =   1.0253p
+0:vss     =   2.3309p
```

$A_{v2} = 53.5$, Rs = $r_{o1,2} \parallel r_{o3,4} = 691961\,\Omega$,

$R_L = r_{o5,6} \parallel r_{omb2} = 239917\,\Omega$, $C_E = C_{gs} \approx 5\text{fF}$

Simulation

1. First Pole = 162.604k(rad / s)

2. Second Pole = $(244.879^2 + 125.997^2)^{1/2}$ M(rad / s) = 275.4M(rad / s)

3. Zero = -120.064M(rad / s)

Hand Calculation

Rs = $r_{o1,2} \parallel r_{o3,4} = 691961\Omega$, $R_L = r_{o5,6} \parallel r_{omb2} = 239917\Omega$, $C_E = C_{net41} \approx 53\text{fF}$

1. First Pole = $\omega_{p1} \approx \frac{1}{R_S\left((1+A_{v2})(C_c+C_{gd})+C_E\right)+R_L(C_c+C_{gd}+C_L)}$

$= \frac{1}{691961*\left((1+53.49)*155*10^{-15}+25*10^{-15}\right)+239917*1.155*10^{-12}} = 162.902\text{K(rad / s)}$

2. Second Pole = $\frac{g_{m5,6}}{C_E+C_L} =$ 274.395M(rad / s)

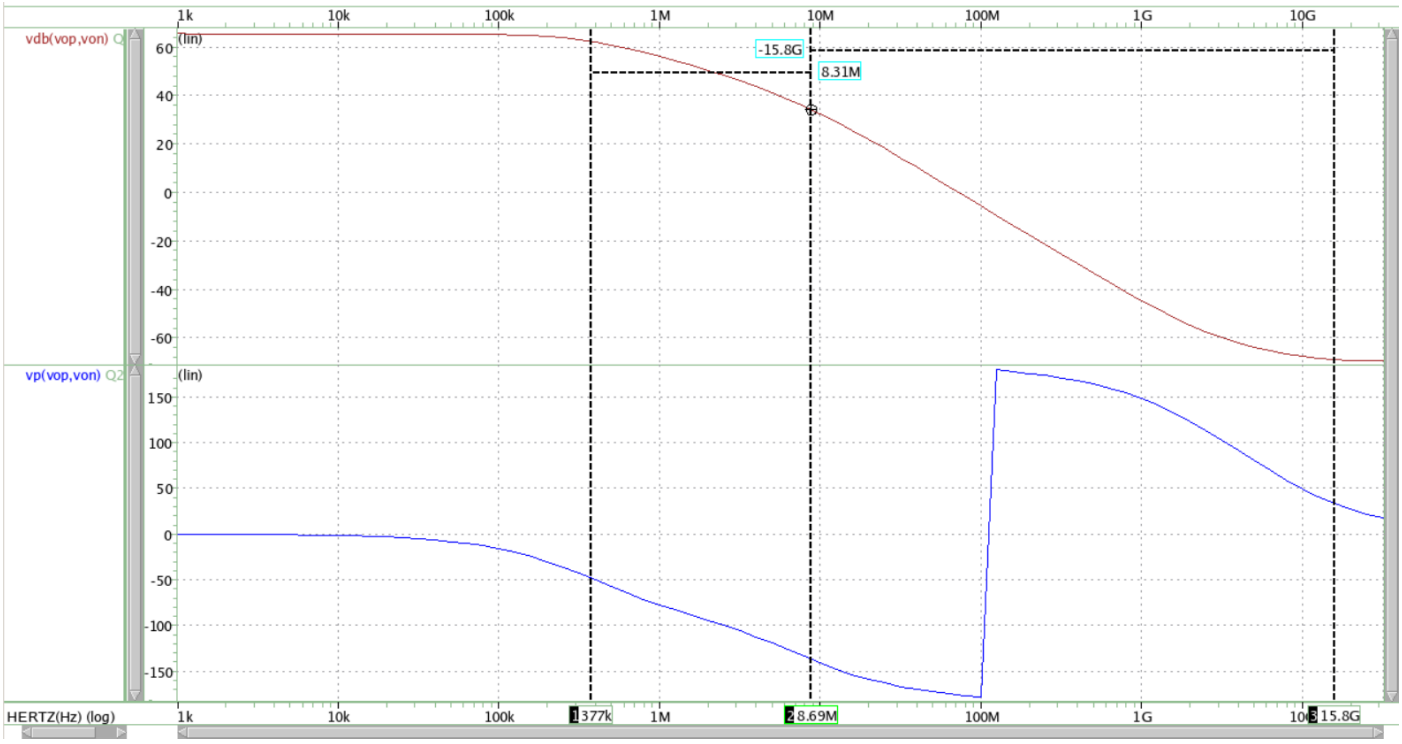
3. Zero = $\omega_z = \frac{1}{C_C(g_{m5,6}^{-1}-R_Z)} =$ -120M(rad / s)

基本上誤差都不大，second pole 的差距相對比較大。我認為誤差來自我們的計算公式是經過兩次簡化，本來誤差就會比較大。但確實能大致找到 pole 的位置。再加上 pole 有虛數，也就是會讓電路產生較不穩定的震盪，使其需要較久時間才可達到穩態

(c)

這題我們把 Compensate resistor and capacitor 拿掉，不做頻率補償，結果如下：

1. First Pole = 377kHz
2. Second Pole = 8.69MHz
3. Unity Gain frequency = 73.1MHz
4. Zero = 15.8GHz




```
******   pole/zero analysis

   input =  0:vac          output = v(vop,von)

      poles (rad/sec)                  poles ( hertz)
real             imag            real             imag
-2.30112x        0.              -366.234k        0.
-48.2326x        0.              -7.67645x        0.

      zeros (rad/sec)                  zeros ( hertz)
real             imag            real             imag
13.7786g         0.              2.19293g         0.
47.6606g         0.              7.58542g         0.
```

```
y
 gaindb=  65.5038     at=   1.0000k
             from=   1.0000k    to=  10.0000g
 unit_gain=  73.0526x
 phase_p=-176.0957
```

```
   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:in      =   0.      0:net15   =  52.9517f 0:net40   =  82.6536f
+0:net41   =  52.9517f 0:vb1     =  66.0516f 0:vb2     =  91.6867f
+0:vb3     = 108.1615f 0:vdd     = 309.3594f 0:vicm    =   0.
+0:vin     =  40.0861f 0:vip     =  40.0861f 0:von     =   1.0253p
+0:vop     =   1.0253p 0:vss     =   2.3309p
```

Simulation

1. First Pole = 2.3M(rad / s)
2. Second Pole = 48.2326M(rad / s)
3. Zero = 13.7786G(rad / s)

Hand Calculation

$$A_{v2} = 53.5 \text{ , Rs} = r_{o1,2} \parallel r_{o3,4} = 691961\ \Omega \text{ ,}$$

$$R_L = r_{o5,6} \parallel r_{omb2} = 239917\ \Omega \text{ , } C_E = C_{gs} \approx 25\text{fF}, \ C_{gd} \approx 5\text{fF}$$

1. First Pole $= \omega_{p1} \approx \frac{1}{R_S((1+A_{v2})Cgd+Cgs)}$

$$= \frac{1}{691961*((1+53.5)*5f+25f))} = 4.858M\text{(rad / s)}$$

2. Second Pole $= \omega_{p2} \approx \frac{R_S\left((1+A_{v2})C_{gd}+C_E\right)+R_L(C_{gd}+C_L)}{R_SR_L(C_EC_{gd}+C_{gd}C_L+C_LC_E)} =$ 41.211M(rad / s)
3. Zero $= \omega_z = \frac{g_{m5,6}}{C_{gd}} =$ 44.6G(rad / s)

可以看到我們的計算結果跟模擬有些差距。首先，first pole 和 second pole 的誤差都不大。但是我們算出來的 zero 反而不是 RHP First Zero，而是第二個 Zero。

(d)

頻率補償靠著額外加的電容，透過 miller effect 壓低 second pole 的位置，進而拉低 unity gain frequency，使 phase margin 拉大，讓這個電路變成 stable。原先的電路可能會因為有許多 pole，導致 phase 不斷變大，回授使其變成一個 unstable 的系統。但這個做法要付出的代價就是 BW 會降低，Unit Gain Bandwidth 提前到來的情況。而 Rc 在這個電路扮演的腳色在於控制又半平面的 pole，如果設計的好有機會與 pole 相消。

(e)

Performance Table		
Vdd	1.5V	
R_c, C_c	60kΩ	150fF
V_{icm}	1.29V	
V_{ocm}	0.554	
Open-Loop Performance		
A_{DM}(> 60dB)	65.4974dB	
Unity Gain frequency(1pF load)(>60MHz)	61.5079MHz	
Phase Margin(> 45^o)	49.5762^o	