The Mass Production of BSI CMOS Image Sensors

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The Mass Production of BSI CMOS Image Sensors

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Abstract

Numerous pixel design and process improvements have been driven by the need to maintain or improve image quality at an ever smaller pixel size. A major development in imager technology is the mass production of Backside Illumination (BSI) technology for image sensors at low cost and high yield. The Omnivision-TSMC R&D alliance has been focused on the development of a low cost BSI technology which enables high performance at the 1.4µm pixel node. We report the performance of two BSI products both in mass production, using the same BSI 1.4µm pixel design and process. For the 1.4µm pixel, peak quantum efficiencies of 43.8%, 53.6%, 51.6% has been achieved in the red, green and blue channels respectively, with low crosstalk, excellent Gb/Gr performance, no lag, no FPN, 2.3e total read noise, dark current of 27 e/sec at 50°C, and low white pixel defect density. For 1.75µm pixel products, the baseline BSI process has been re-optimized to achieve peak QE of 53%, 60.2%, and 60.4% in the red, green, and blue channels, respectively. This modified process also meets mass production targets for the three 1.75µm BSI products. Our reliability testing has found no reliability issue associated with OmniBSI™ architecture.

Introduction

Thirty years after the early seminal work on APS imagers,[1-5] the CMOS APS pixel rapidly shrunk as a result of using dedicated imager design rules and the development of unique process modules focused on driving improved electro-optical performance at each new technology node[6,7]. BSI has required the development of multiple new process modules for both the frontside (FS) and the backside (BS) process modules. For pixels sizes of 1.75µm and smaller, BSI provides several realized advantages over frontside illumination (FSI) sensors: quantum efficiency, crosstalk, color shading, sensitivity, stack height, 100% fill factor, better acceptance of higher speed lenses, and improved performance across the entire image plane. Another BSI key advantage is the elimination of the bulk substrate, which substantially reduces both the diffusion component of dark current and electrical crosstalk. The challenges of BSI have been:

- To marry the FS with the BS processing so that the generated electrons are effectively delivered to the target photodiode with high QE and low crosstalk
- To develop a low stress, void-free BS bonding of the device wafer to the handle wafer
- To develop a BS thinning process with tight thickness control
- To completely passivate the BS surface to achieve low dark current and white pixel defect density
- To develop the BS patterning and BS etching to enable a BS metal light shield
- To develop backside patterning with accurate alignment CFA and micron lens to enable a color CIS imager
- To do this with a low cost process at high yield

BSI Products, Design Rules, and Pixel Design

The data to be presented comes from the characterization of multiple products. The 1.4µm BSI pixel data comes from two BSI products in mass production. The 1.75µm BSI pixel data comes from three BSI products. All of these BSI products use a common 2-shared symmetric pixel design. Unlike the FSI image sensors where the BEOL design rules are pushed as much as possible to enhance the fill factor and copper technology may be employed, along with recessed array and light guide technology, to reduce stack height, the BSI design rules can be appropriately relaxed to save cost and achieve better angular response. The first generation Omnivision-TSMC jointly developed BSI technology, OmniBSI technology, uses a combination of 90 nm and 110 nm design rules using Al BEOL processing. The design rules are specifically tailored and pushed where needed to improve the pixel design and the image performance. The restrictions on metal thickness and the number of metal layers are relaxed, making it possible to reduce the chip size and increase speed by using more and thicker metal layers for peripheral circuits.

BSI Process
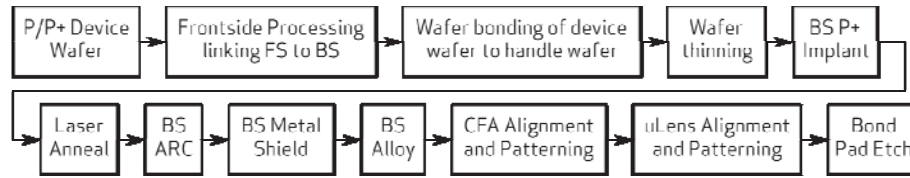
The process begins with a low cost p/p+ device wafer. We believe this is the first announced demonstration of the use of bulk silicon starting material to enable low cost BSI technology[8-10]. A new BSI frontside (FS) process module was developed to link a low noise, fully depleted, no lag FS photodiode with the BS surface. After FS processing the metalized side of the device wafer is bonded to a handle wafer with no voids and no added defects. The exposed BS surface of the device wafer is then thinned to the final target epi thickness. QE and crosstalk are critically dependent on both the FS processing and the BS thinning. A proprietary thinning process module to provide a reproducible final epi thickness on standard p/p+ device wafers is used. To achieve good blue response, low dark current, and low white pixel defect density, the BS surface is passivated with a BS P+ implant and laser anneal. A BS anti-reflection coating (ARC) is deposited to further improve QE at all wavelengths. BS metal is deposited and patterned to form the BS metal shield. A color filter array followed by a ulens is aligned and patterned on the backside surface of the thinned device wafer. The final step is the opening of the bond pads. See Figure 1 for a cross-section of the 1.4µm pixel. The finished wafer may be packaged using CLCC, CSP, aCSP™ (TSV) or OmniVision CameraCube™ Technology.
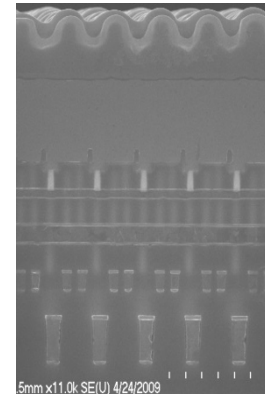

Figure 1. 1.4µm pixel cross-section
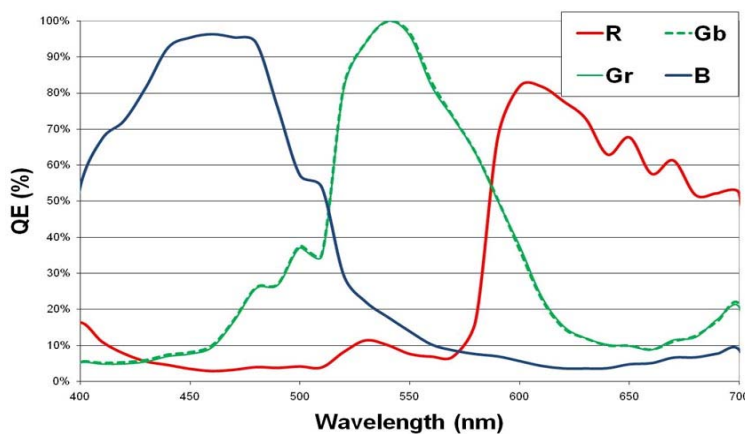
1.4µm BSI Pixel Performance

Figure 2. Quantum Efficiency R, G, and B channels vs Wavelength
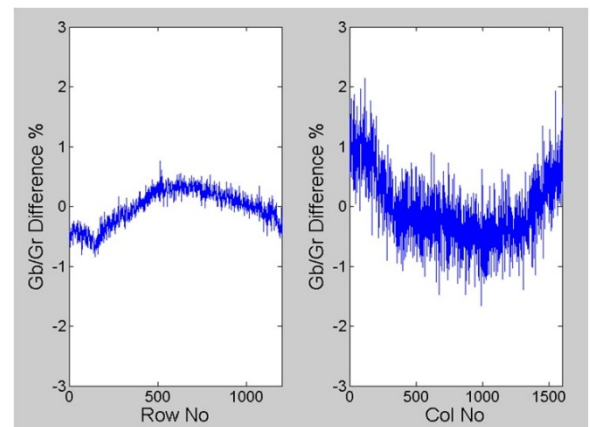

Figure 3. Measured Gb-Gr difference

Figure 2 displays the quantum efficiency of the R, G, and B channels vs wavelength. Peak quantum efficiencies of 44%, 54% and 52% are achieved at the R, G, and B channels, respectively, as well as low optical and electrical crosstalk. We calculate an effective black and white QE of 62% across the blue and green regions at the visible spectrum with a reduction to 46% in the red[11]. As there is no metal in the array, the micro lens fill factor is 100% and the micro-lenses serve to focus the incident radiation to improve crosstalk. The high blue QE is a strong indicator of effective passivation of the BS surface. A sensitivity of 671 mV/lux-sec is achieved at 530 nm. The Gb and Gr channels are explicitly shown in Figure 3 to demonstrate the nearly identical performance of these channels which is an indicator of low crosstalk and a symmetric pixel design.

The measured Gb-Gr difference is shown in Figure 3. An 18% grey patch was imaged at 1000 lux illumination. The raw image was collected and the Gb-Gr row average and column average differences calculated across the entire 8 Megapixel image plane. An advantage of low crosstalk is that raw images produce reasonable color reproduction without a CCM under all source illuminations. The low BSI stack height enables the use of high speed, low F/# lenses. It also provides wide acceptance angle so that high QE/low crosstalk performance is maintained across the entire image array.

In Figure 4, we show the color shading of the raw R, G, and B channels across the image array without any lens shading correction. The angular collection efficiency is a result of the low stack height and the high index of refraction of silicon which helps focus radiation towards the photodiode collector.

To measure the low light S/N performance of both the 1.4µm and the 1.75µm pixel, raw images through a F/2.8 lens are collected from an 18% gray patch from a 3200K light source. After AWB and CCM, the experimentally measured luma S/N is plotted in Figure 5 vs the incident Lux level on the gray patch. For the 1.4 µm pixel, S/N=10 is achieved at 110 Lux which agrees with the theoretically calculated performance

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of 105 Lux[12]. Low light S/N can be degraded by read noise and lag. The read noise at 8x analog gain has been broken down into the pixel component (1.9e) and the peripheral circuit component (1e) for a total read noise of 2.3e. Lag variation can be another noise source, appearing as pixel FPN. In Figure 6 we show lag as a function of light signal level. Lag is low across the entire signal range. As the floating diffusion fills up with electrons under higher signal measurement conditions, the voltage drop across the transfer gate is reduced and lag can increase to unacceptable levels. The data in Figure 6 clearly shows that lag is not an issue on the 1.4μm BSI pixel at all signal levels.
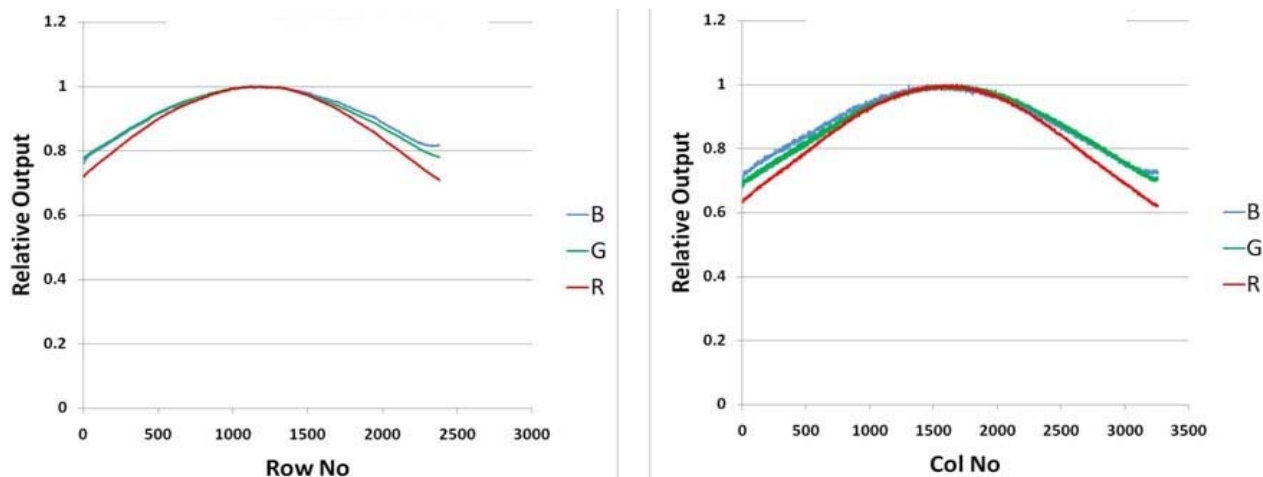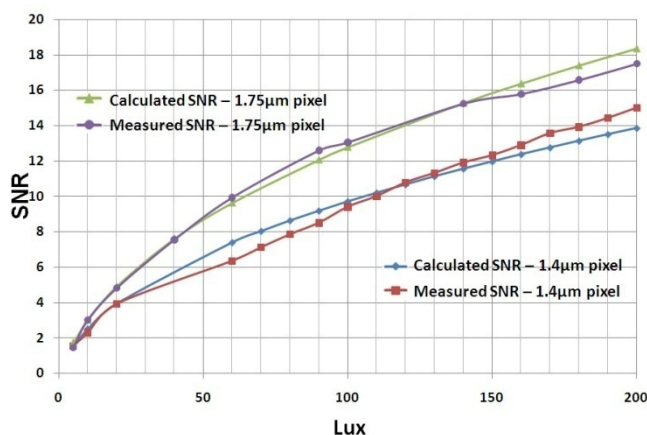

Figure 4. White color ratios

Figure 5. Luma S/N after CCM and AWB versus light level (Lux)
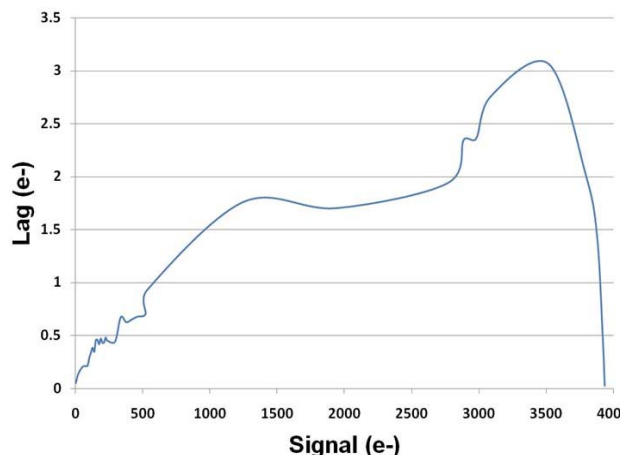
Figure 6. Lag(e) vs signal level (e) for 1.4μm pixel

Dark current and FPN are critical parameters for all image sensors. High dark current can impact low light performance, add FPN, and reduce yield. Shown in Figure 7 is a raw dark image taken with an integration time of 9 seconds at RT at 8x analog gain and 32x digital gain. The total FPN is 0.7e. No column or row FPN is observed.
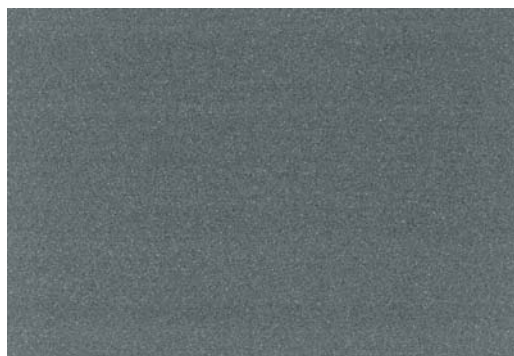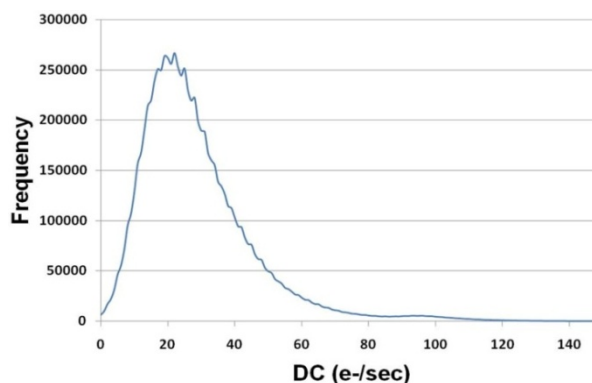

Figure 7. RAW dark image

Figure 8. Dark current histogram for 1.4μm pixel at 50°C

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A histogram of the individual pixel dark current at 50°C for the entire 8 Megapixel sensor is shown in Figure 8. The dark current peak at 50°C corresponds to 27 e/sec.

In Figure 9, we show the temperature dependence of the measured dark current for both 1.4μm and 1.75μm pixels measured after FS processing and parts measured after complete BS processing. Fully processed BS parts achieve 23-27 e/sec dark current at 50°C and <1e/sec at room temperature. An activation energy of 1.1 eV is measured for both FS and BS processed parts. We find that the FS and BS components contribute equally to the total dark current.
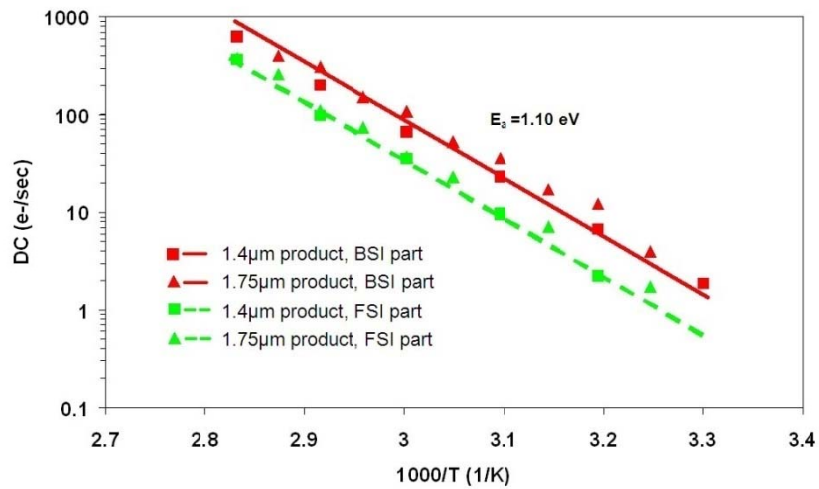

Figure 9. Dark current vs temperature

The color image performance of the 1/3.2" 8 Megapixel sensor is shown in figure 10 at 100 Lux and 15 fps.

Figure 10. 8 Megapixel at 100 Lux (15 fps)

Table 1 summarizes both the 1.4μm and the 1.75μm pixel performance. The excellent PRNU is a result of the low optical/electrical crosstalk.

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Table 1. 1.4µm and 1.75µm pixel performance

Parameter	1.4 µm	1.75 µm	Parameter	1.4 µm	1.75 µm
FWC	4500 e	6500e	B/G	31.80%	24.0%
Peak QE - R	43.8%	53.0%	G/R	35.20%	28.9%
Peak QE - Gb	53.5%	60.1%	B/R	7.30%	5.4%
Peak QE - Gr	53.6%	60.2%	Sensitivity (530nm)	671 mV/Lux-sec	1500 mV/lux-sec
Peak QE - B	51.6%	60.4%	Read Noise (pixel/periph)	1.9/1.3 e	2.1e/1.3e
R/B	5.70%	4.8%	PRNU	0.75%	0.8%
G/B	14.40%	11.4%	Lux for 10:1 SNR	110 Lux	60 Lux
R/G	11.20%	9.2%	Dark Current (50 C)	27 e/sec	22 e-/s

1.75µm BSI Pixel Performance

The 1.75µm BSI pixel uses the same basic pixel design, design rules, and process flow as the 1.4µm pixel technology. There is some re-optimization of the process for the larger pixel size. Table 1 displays the performance of the 1.75µm pixel/process that is in mass production. In Figure 11 we show the QE vs wavelength performance. Peak QE's of 53.0%, 60.2%, and 60.4% are achieved in the red, green, and blue channels. Figure 12 shows a dark current histogram for a baseline wafer with a measured dark current 22 e/sec at 50°C. The measured activation energy, Ea of this dark current is 1.10 eV as shown in figure 9. For this 1.75µm pixel a S/N=10 is achieved at 60 lux from experimentally measured images. This measured low light S/N performance agrees with our calculations as shown in figure 5, based on measured QE versus wavelength.
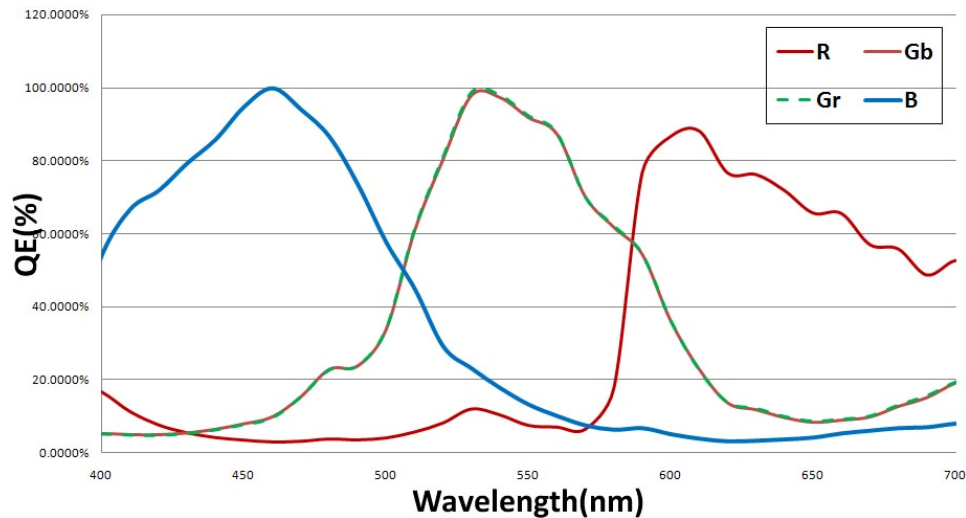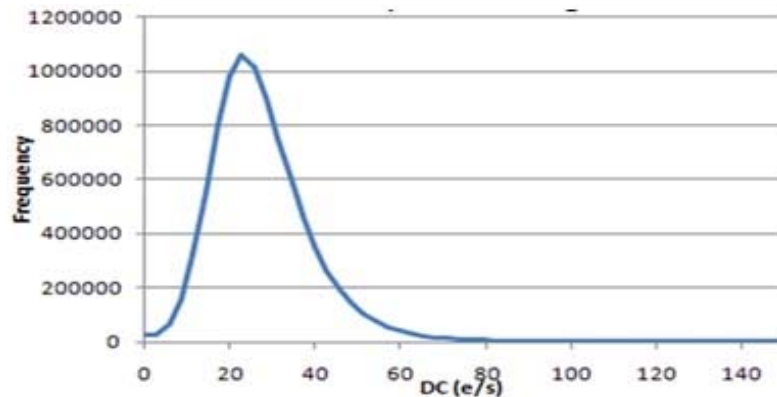

Figure 11. QE vs wavelength performance

Figure 12.   1.75µm dark current histogram at 50°C

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BSI Reliability

Omnivision's reliability qualification of OmniBSI architecture requires testing of of both CLCC and CSP packaged parts. The reliability tests include: 1) 1000 hours of High Temperature Operating Life (HTOL) at 125°C, 2) 1000 hours High Temperature Storage (HTS) at 125°C, 3) 1000 cycles of Temperature Cyling (TC) from -40°C to 125°C, 4) 1000 hours of unbiased Temperature Humidity (TH) at 85C/85% RHA, 5) ESD testing, and 6) Latch-up testing. To date a set of 4 separate lots have been tested with zero (0) fails for all tests at all readpoints. Calculations based on the 125°C HTOL data yield a FIT rate of 28.2 and a MTBF of 2,986 years at 55°C. Our reliability testing has found no reliability issue associated with OmniBSI architecture.

1.1μm and the 0.9μm SMP BSI Performance

With BSI in place it is now possible to continue the pixel shrink to the 1.1μm pixel technology node. By moving to 65 nm design rules the photodiode area can be made large enough to provide reasonable full well capacity at the 1.1μm pixel. By going to a buried channel source follower the read noise can be improved and dynamic range increased[13]. Similar to the constant DRAM challenge of getting enough cell capacitance into the shrinking DRAM cell, the imager technologist faces the issue to getting enough light collected. There is room for further QE and crosstalk improvements. We believe that reasonable sensitivity performance is possible using the standard RGB Bayer pattern for the 1.1μm pixel. Improving performance for the 0.9μm Sub-Micron Pixel (SMP) beyond S/N=10 at 245 Lux will require RGBClear, CMY, CMYClear, or a new photosensor technology [14,15].

Conclusions

CMOS Imagers have gone through an exciting period of process and pixel technology development driven by the need to maintain performance for ever shrinking pixels. To achieve best-in-class performance at 1.75μm pixel sizes and below, BSI is an enabling technology. What has been presented is BSI electro-optical and low defect performance for multiple products at two different pixel sizes. The ability to run multiple products at different pixel technology nodes is a demonstration of a BSI process that is under control and in mass production.

Acknowledgements

References

1   Peter Noble, IEEE Trans. El Dev. 15, p. 202-209, 1968
2   S. Chamberlain, IEEE J Solid-State Circuits SC-4 (6) p. 333-342, 1969
3   P. Weimer et al., IEEE Spectrum 6 (3): p. 52-65, 1969
4   P. Denyer et al, VSLI, p. 157-166, 1991
5   E.R. Fossum Proc. SPIE Vol 1900, p. 2-14, 1993
6   H. Rhodes et al., Workshop on Microelectronics and Electron Devices, p. 7-18, 2004.
7   C-R. Moon et al, IEDM Tech. Dig, p. 813-816, 2005
8   J. Prima et al., Int. Image Sensor Workshop, p. 5-8, 2007.
9   T. Joy et al., IEDM Tech. Dig., p. 1007-1010, 2007.
10   J. Ahn et al., IEDM Tech. Dig. p. 275-278, 2008.
11   Y.Wu, P. Cizdziel, H. Rhodes, SPIE Electronic Imaging Conference, 2009
12   J. Alakarhu, Int. Image Sensor Workshop, p. 1-4, 2007
13   X. Wang et al, Int. Image Sensor Workshop, p. 223-225, 2007
14   J. Ahn et al, IEDM Tech. Dig., p. 275-178, 2008
15   M. Ihama et al, Proc. SPIE, p. 6656, 2007