A 1392x976 2.8μm 120dB CIS with Per-Pixel Controlled Conversion Gain

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A rolling shutter HDR BSI CIS with 5T dual CG pixels is presented. Two HDR schemes are combined during readout: (i) OmniVision's DeepWell HDR [1] and (ii) Staggered HDR [2-5]. The former is based on reading out PD charge with both high and low CG, without destructive reset in between. Thus, 50ke- FW and 1e- rms RN (94dB DR) is achieved in one single exposure. The latter scheme splits the available frame time into one long and one short exposure. Thus, extending DR to 120dB or more.

Fig. 1 shows the 5T pixel and the readout architecture. CG is controlled by turning DFD on/off, corresponding to LCG=20uV/e- and HCG=220uV/e-, respectively. The in-pixel capacitor (C) is composed of an MOS device plus layout parasitics. Digital CDS is performed using 12b column-parallel SAR-ADCs with up to 8x analog gain controlled by scaling VREF.

Fig. 2 illustrates the CDS timing for DeepWell HDR. It starts with ADC sampling of reset level in LCG mode, followed by turning DFD off (HCG) and sampling a 2^{nd} reset level. TX is then pulsed and the signal level is sampled. Finally, DFD is turned back on (LCG) and another TX pulse is applied before executing a fourth and final ADC sampling.

Fig. 3 compares the frame timing of the proposed sensor (left) with a triple exposure staggered HDR sensor (right). Our proposed scheme benefits from one less exposure, which gives less motion artifacts (a.k.a. ghosting) after HDR combination.

Fig. 4 shows the chip architecture. Since DeepWell HDR doesn't require align buffers the two pixel values (HCG and LCG) can be combined on-chip to output a 16b linear value together with the staggered 12b short exposure value (VS).

Fig. 5 plots the QE curve with approximate max values of 86% Green, 80% RED, and 40% NIR 850nm.

Fig. 6 plots signal-to-noise versus light level for HCG and LCG. Notice there is no SNR drop at the HCG/LCG transition point because the noise is already dominated by photon shot noise at this point.

Fig. 7 illustrates a lag test by capturing a moving metronome. Lag is below 1% at 50ke-. Hence, there is no observable non-linearity or image artifacts along the moving edges besides regular motion blur.

Fig. 8 plots the histogram of the delta between two consecutive image frames. Gaussian and Lorentzian curve fitting models are included for modelling purposes. RTS noise level is small (no additional peak or extended tail in the histogram).

Fig. 9 is a plot of the cumulative read noise distribution on a semi-log y scale. The median value is 0.87e- rms.

Table 1 summarizes key performance parameters obtained for this sensor.

References:

[1] B. Fowler, "Achieving HDR – without motion artifacts and in every single exposure", IS Auto, USA, 2016
[2] T. Willassen et al., "A 1280x1080 4.2μm Split-diode Pixel HDR Sensor in 110 nm BSI CMOS Process", IISW 2015
[3] J. Solhusvik et al., "A comparison of high dynamic range CIS technologies for automotive applications", IISW 2013
[4] Yadid-Pecht et al, "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling", Workshop on CCDs and AIS, Bruges, 1999
[5] Egawa et al., "A 1/2.5 inch 5.2Mpixel, 96dB Dynamic Range CMOS Image Sensor with Fixed Pattern Noise Free, Double Exposure Time Read-Out Operation", ASSCC, 2006

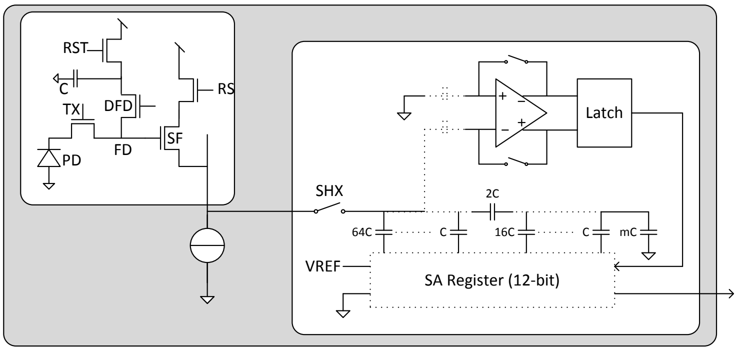

Figure 1

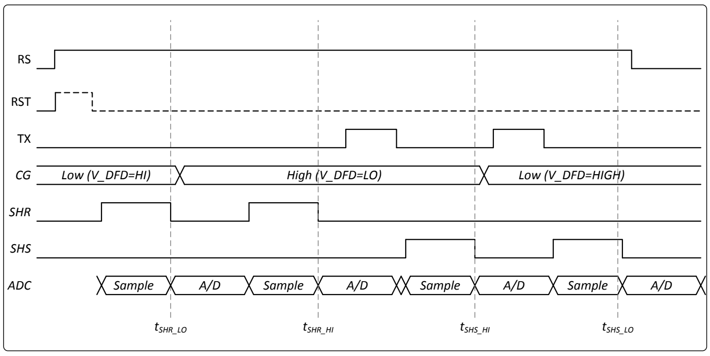

Figure 2

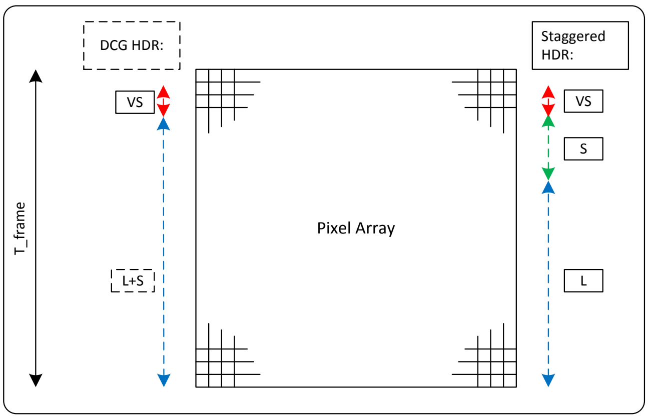

Figure 3

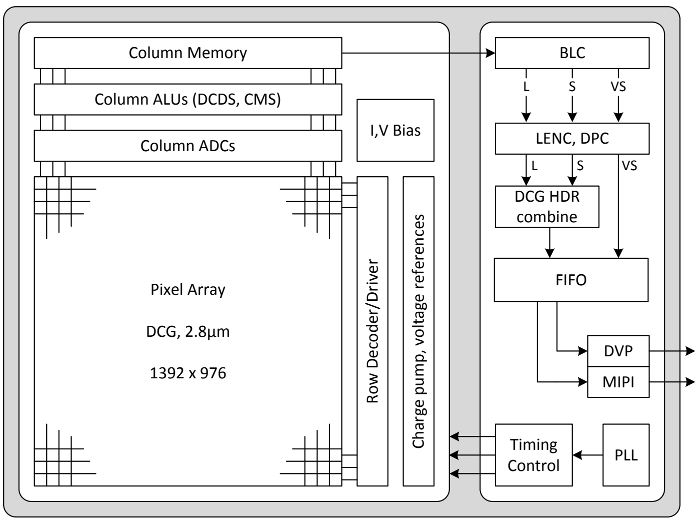

Figure 4

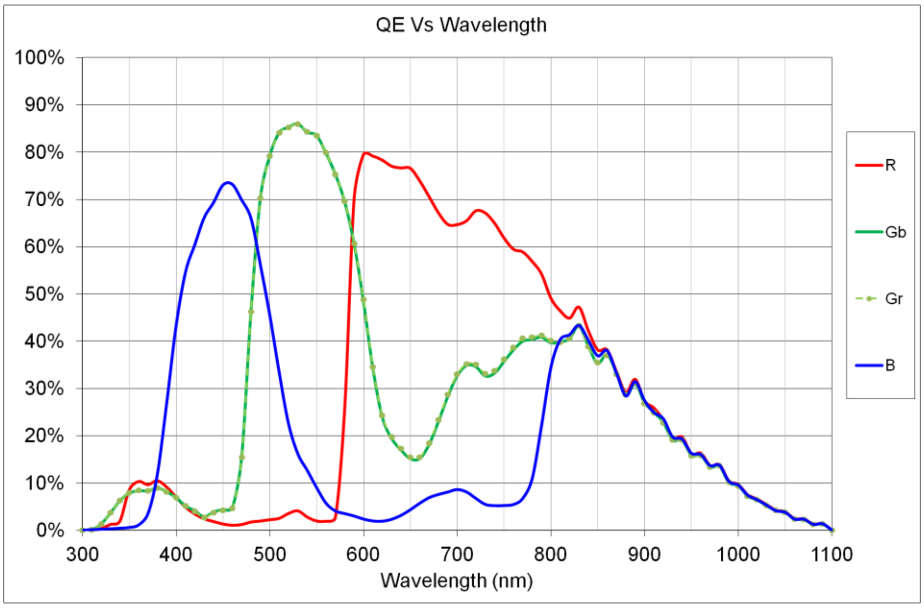

Figure 5

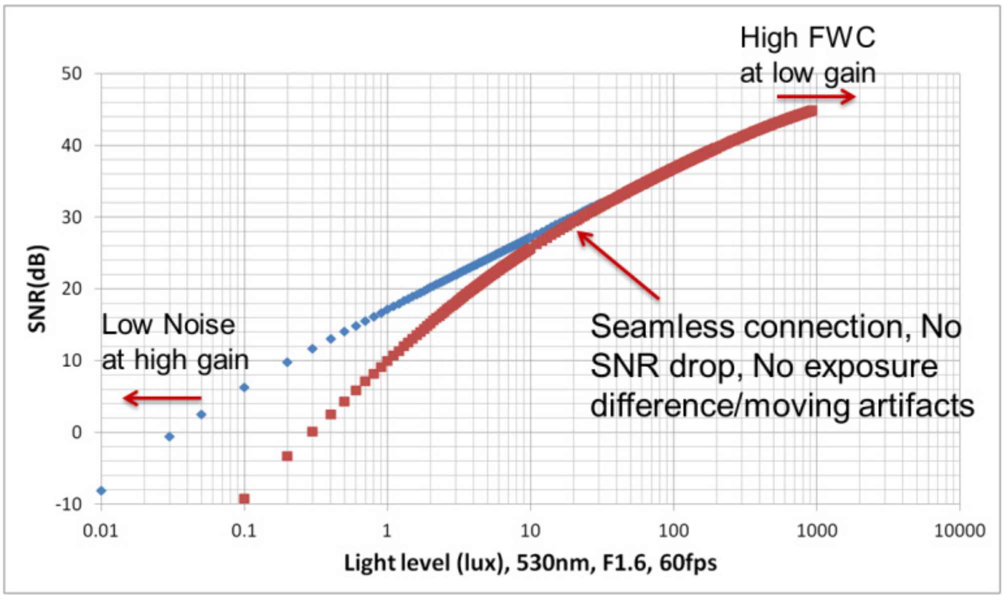

Figure 6

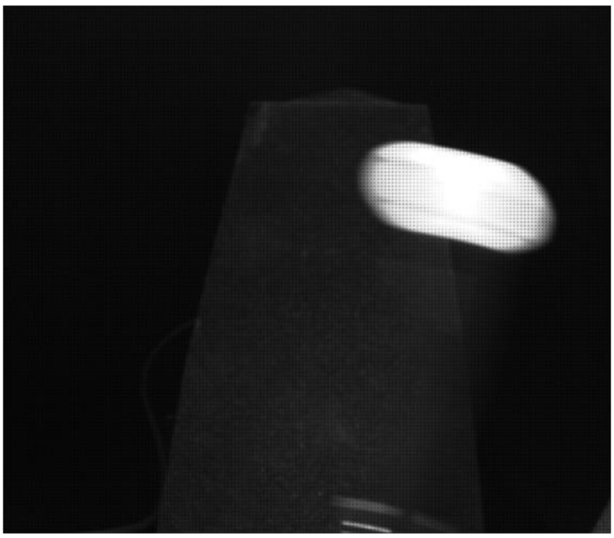

Figure 7

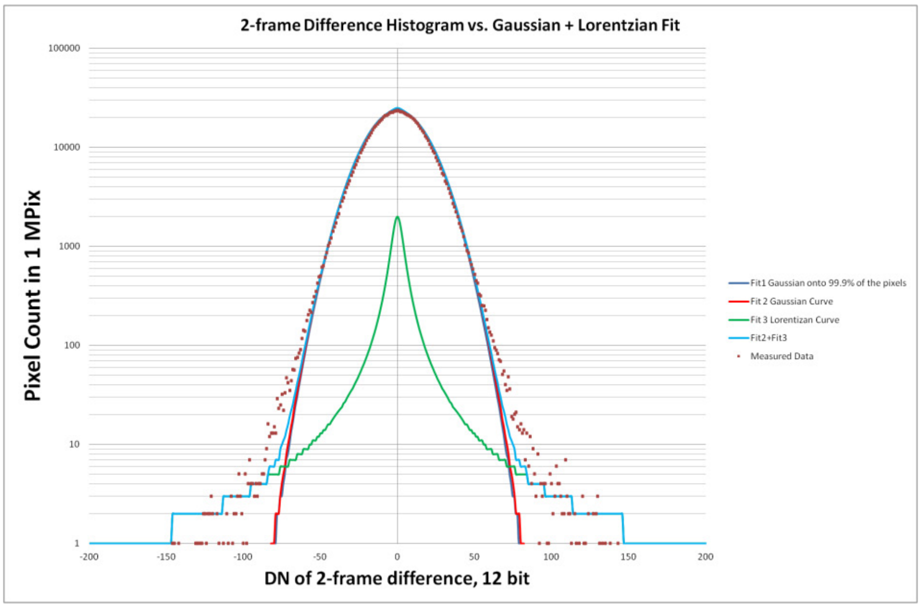

Figure 8

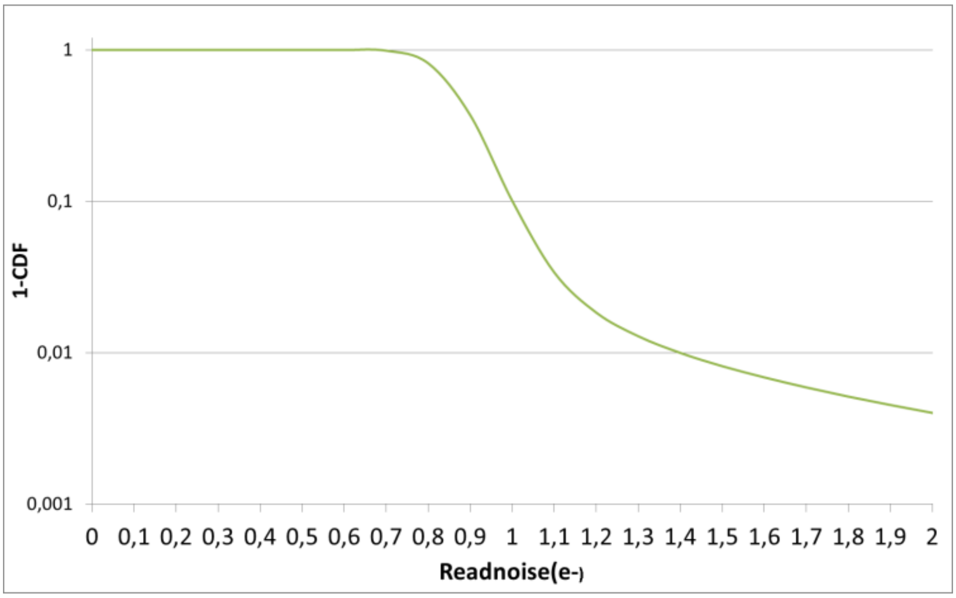

Figure 9

Parameter	Performance
Pixel Size(um)	2.8
Resolution and frame rate	1.3Meg/30fps
FWC(e-)	50000
Sensitivity(e-/lux.sec)	31K
QE(%, R/G/B/IR)	(80/85/73/38)
Xtalk(%)	14
PRNU(% rms)	0.4
RN(e- rms, 8xgain)	1.0
DC(e-/sec) 60C	20
SNR1(lux)	0.20
SNR1(Photon/pixel) @ 530nm (EMVA)	2.1
IntraScene DR(dB)	94
InterScene DR(dB) – 2 frame stagger HDR	120dB with 30dB minSNR

Table 1