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**SEMICONDUCTOR MANUFACTURING INTERNATIONAL  
CORPORATION**

**14nm SF+ 0.8 1.8V Design Rules**

**Version V1.0\_REV1**

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**1. Title:**

14nm SF+ 0.8 1.8V Design Rules

**2. Purpose:**

Patterns Design Guideline for 14nm SF+ Process

**3. Scope:**

SMIC TD

**4. Nomenclature:**

NA

**5. Reference:**

NA

**6. Responsibility:**

Technology Development Center

**7. Subject content:**

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## 7.1 User Guideline:

### 7.1.1 Design requirements

Designers should follow design requirement guidelines to reduce the OPC loading and then enhance the OPC efficiency.

Rule number	Description
GR.1	All the geometry design must be an integer multiple of 0.001um. 0.001um deviation is allowed for 45-degree polygon dimensions.
GR.2	Design shape geometry all vertices and intersections of 45-degree polygon must be on an integer multiple of 0.001um.
GR.3	Only shapes of geometry that are orthogonal or 45-degree angle are allowed.
GR.4	Shapes with acute angles between line segments are not allowed.
GR.5 <sup>[NC]</sup>	Only unidirectional, straight transistor channels are allowed.
GR.6 <sup>[NC]</sup>	Recommended to design simple rectangular shape geometry as possible, avoid L, U, H, or O shapes.
GR.7 <sup>[NC]</sup>	All line-end must be rectangular.
GR.8 <sup>[NC]</sup>	Self-intersecting shape are not allowed.
GR.9 <sup>[NC]</sup>	Design geometry shape must be polygons.
GR.10 <sup>[NC]</sup>	All the text or labels in the chip must be covered by the marker layer LOGO (26;0).
GR.11 <sup>[NC]</sup>	Make sure the designs are DRC clean.
GR.12 <sup>[NC]</sup>	Recommended to avoid small jogs ( $\leq 0.005\text{um}$ ) of geometry.
GR.13 <sup>[NC]</sup>	For the OPC layers, any edge of length $< 1.0x$ minimum width, the adjacent another edge of length must $\geq 1.0x$ minimum width The OPC layers: AA, NW, DG, GT, P2, LVN, LVP, SN, SP, M0, M0G, M1 and Mn
GR.14 <sup>[NC]</sup>	Recommended to organize the layout of designs with well hierarchical structure, put designs as low level cell in hierarchical layout as possible.
GR.15 <sup>[NC]</sup>	Recommended to put dummy filling patterns in a separate hierarchy from the main patterns and reduce the flattened dummy fill geometries as much as possible.
GR.16	It is not allowed that AA, GT, P2, NW, SN, SP, M0, M0G, M0C, M1, Mxy, 1.25xMy, 1.25xMn, 2xMn, 10xTMn, 14xTMn and UTM have one edge length $< 1x$ minimum width and another adjencent edge length $< 1x$ minimum width (except DMCMK1 and EFUSE region)

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Rule number	Description
GR.17	It is not allowed that LVT_N, LVT_P, SVT_N, SVT_P, ULVT_N, ULVT_P, HVT_N, HVT_P, LFN_N, LFN_P, LFN_N, LFN_P have one edge length < 1x minimum width and another adjacent edge length < 1x minimum width (except 0.18um edge adjacent to $\leq 0.048\text{um}$ edge, 0.135/0.144um edge adjacent to 0.002um edge)
GR.18a	AADOP/AADUM/ARDOP/ARDUM/AR_HDOP/AR_VDOP/GTDOP/GTDUM/P2DOP/P2DUM /SNDUM/SPDUM/M0DOP/M0DUM/M0CDOP/M0CDUM/M0GDOP/M0GDUM/V0DUM/V0D PDUM layers in chip design is not allowed, except DMCMK1 and MARKS regions. These layers are dedicated for SMIC FEOL and MEOL dummy auto-insertion utility usage, can't be used for manually drawn purpose.
GR.18b	M1DOP/M1DUM/M1DP/M1DPDOP/M1DPDUM/M2DUM/M2DOP/M2DP/M2DPDUM/ M2DPDOP/M3DUM/M3DOP/M3DP/M3DPDUM/M3DPDOP/M4DUM/M4DOP/M5DUM/M6D UM/M7DUM /V1DUM/V2DUM/V3DUM/V4DUM/V5DUM/V6DUM/ BV1DUM/BV2DUM/ B1DUM/B1DOP/B2DUM/B2DOP/UTMDUM/TM1DUM/TM2DUM/ALDUM layers in chip design is not allowed except DMCMK2 and MARKS region. These layers are dedicated for SMIC BEOL dummy auto-insertion utility usage, can't be used for manually drawn purpose.
GR.19	ALL_AA, CELLB, AR, DNW, NW, PSUB, SVT_N, SVT_P, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, DGV, DGUD, ALL_GT, GTMK1, GTMK2, ALL_P2, SN, SP, ALL_M0, ALL_M0C, ALL_M0G, V0, CHIPB, DIR, DIRDMP, RESP2, RESP1, MIM, CTOP must be orthogonal to grid. DRC waive SP/GT/M0 in the MARKS region.
GR.20	PPAA/AR_H/AR_V/PPAADB/ARBL layers in chip design is not allowed, except INST, OCOVL, DMCMK1 and MARKS regions.
GR.21	(AA OR DOP_AA) enclosure by ESDIO1, ESDIO2, DBESD, DBESD2, LDBK, DSTR, DMPNP, DIOMK1, DIOMK2, VARMOS and DNW must be $\leq 3\text{um}$ .
GR.22	O-shape AA is not allowed.

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### 7.1.2 Grid size

1. Minimum layout grid size is 0.001um.

### 7.1.3 Non-DRC check guideline

1. No DRC for the design rules with the superscript of [NC].
2. No DRC for Notes.

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#### 7.1.4 DRC check guideline

1. The rules with the superscript of [R] are recommended rules which require performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow recommended rules which purpose is to ensure better performance for process. Customers can waive violations based on their own judgment, and please consult with integration engineers if customers feel the need.

2. The seal ring area (marked with MARKS layer) should pass main rule checking except Seal-ring dedicated design. For seal ring design guideline and seal ring check rule, please refer 7.9 section.

3. For the density rules, DRC check should include dummy pattern, also doesn't flag if check window width is less than 1/4 checking window width. DRC does not flag AR and MIM low density check if the GDS has no AR or MIM. Default density check rule is for chip level, if "IP level density check" switch is turned on, density rule will follow "IP level density check rule" of below table. IP level density check is only for reference in IP design stage. "step\_number" in below table is 8.

Rule number	Chip level density check rule			IP level density check rule		
	Description	O pt.	Design Value	Description	O pt.	Design Value
AA.D.1	Full chip ALL_AA density	≥	25%	Full chip ALL_AA density	≥	25%
AA.D.2	Full chip ALL_AA density	≤	60%	Full chip ALL_AA density	≤	60%
AA.D.3	ALL_AA density (window 18um*18um, stepping 9um), except LOGO, OCOVL, (NODMF su 1um) region	≥	11.8%	ALL_AA density (window 18um*18um, stepping 18um/step_number), except LOGO, OCOVL, (NODMF su 1um) region	≥	12.4%
AA.D.4	ALL_AA density in ((RESP1 su 10um) NOT RESP1)	≥	20%	ALL_AA density in ((RESP1 su 10um) NOT RESP1)	≥	20%
AA.D.5	Maximum ALL_AA density in core region (window 100um*100um, stepping 50um)	≤	70%	Maximum ALL_AA density in core region (window 100um*100um, stepping 100um/step_number)	≤	66.5%
AA.D.6	Maximum ALL_AA density in I/O region (window 100um*100um, stepping 50um)	≤	80%	Maximum ALL_AA density in I/O region (window 100um*100um, stepping 100um/step_number)	≤	76%
AR.DN.1	Full chip ((AR OR (ARDUM sd 0.02um)) OR ARDOP) density	≥	5%	Full chip ((AR OR (ARDUM sd 0.02um)) OR ARDOP) density	≥	5%
AR.DN.2	Full chip ((AR OR (ARDUM sd 0.02um)) OR ARDOP) density	≤	10%	Full chip ((AR OR (ARDUM sd 0.02um)) OR ARDOP) density	≤	10%
AR.DN.3	((AR OR (ARDUM sd 0.02um)) OR ARDOP) density (window 18umx18um, stepping 9um), except OCOVL region	≤	15%	((AR OR (ARDUM sd 0.02um)) OR ARDOP) density (window 18umx18um, stepping 18um/step_number), except OCOVL region	≤	14.3%
GT.D.1	(ALL_GT NOT ALL_P2) full chip density	≥	14%	(ALL_GT NOT ALL_P2) full chip density	≥	14%
GT.D.2	(ALL_GT NOT ALL_P2) full chip density	≤	40%	(ALL_GT NOT ALL_P2) full chip density	≤	40%
GT.D.3	(ALL_GT NOT ALL_P2) density, except (NODMF su 1um), OCOVL, DIR, DIRDMP regions (window 10um*10um, stepping 5um)	≥	10%	(ALL_GT NOT ALL_P2) density, except (NODMF su 1um), OCOVL, DIR, DIRDMP regions (window 10um*10um, stepping 10um/step_number)	≥	10.5%
GT.D.4	(ALL_GT NOT ALL_P2) density for RESP1 region. (window 10um*10um, stepping 5um)	≥	6%	(ALL_GT NOT ALL_P2) density for RESP1 region. (window 10um*10um, stepping 10um/step_number)	≥	6%
GT.D.5	(ALL_GT NOT ALL_P2) density for core device region.	≤	50%	(ALL_GT NOT ALL_P2) density for core device region.	≤	47.5%

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Rule number	Chip level density check rule			IP level density check rule		
	Description		O pt.	Design Value	Description	
	O pt.	Design Value	O pt.	Design Value	O pt.	Design Value
	(window 10um*10um, stepping 5um)			(window 10um*10um, stepping 10um/step_number)		
GT.D.5a	(ALL_GT NOT ALL_P2) density for I/O device region (window 10um*10um, stepping 5um)	≤	60%	(ALL_GT NOT ALL_P2) density for I/O device region (window 10um*10um, stepping 10um/step_number)	≤	57%
GT.D.6	(ALL_GT NOT ALL_P2) density (window 140um*140um, stepping 70um)	≤	50%	(ALL_GT NOT ALL_P2) density (window 140um*140um, stepping 140um/step_number)	≤	47.5%
GT.D.7	(ALL_GT NOT ALL_P2) density difference between any two neighboring checking window (window 20um*20um, stepping 10um)	≤	35%	(ALL_GT NOT ALL_P2) density difference between any two neighboring checking window (window 20um*20um, stepping 20um/step_number)	≤	33.3%
P2.D.1a	Full chip ALL_P2 density	≤	15%	Full chip ALL_P2 density	≤	15%
P2.D.1b	Full chip ALL_P2 density	≥	5%	Full chip ALL_P2 density	≥	5%
P2.D.2	Maximum ALL_P2 density (window 20um*20um, stepping 10um), except INST region	≤	20%	Maximum ALL_P2 density (window 20um*20um, stepping 20um/step_number), except INST region	≤	19%
SSD.DN.1	PSR open ratio should be as uniform as possible over the chip. PSR open ratio definition: ((((((SP - INST) - PSRBL) su 0.095) sd 0.19) su 0.095) + (((((SP * INST) - PSRBL) su 0.086) sd 0.172) su 0.086)) + SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≥	5.8%	PSR open ratio should be as uniform as possible over the chip. PSR open ratio definition: ((((((SP - INST) - PSRBL) su 0.095) sd 0.19) su 0.095) + (((((SP * INST) - PSRBL) su 0.086) sd 0.172) su 0.086)) + SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≥	5.8%
SSD.DN.1a	PSR open ratio should be as uniform as possible over the chip. PSR open ratio definition: ((((((SP - INST) - PSRBL) su 0.095) sd 0.19) su 0.095) + (((((SP * INST) - PSRBL) su 0.086) sd 0.172) su 0.086)) + SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≤	18%	PSR open ratio should be as uniform as possible over the chip. PSR open ratio definition: ((((((SP - INST) - PSRBL) su 0.095) sd 0.19) su 0.095) + (((((SP * INST) - PSRBL) su 0.086) sd 0.172) su 0.086)) + SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≤	18%
SSD.DN.2	NSR open ratio be as uniform as possible over the chip . NSR open ratio definition: (((((((!SP) - RESNW) - NSRBL) - INST) su 0.095) sd 0.19) su 0.095) + (((((!SP) * INST) - NSRBL) su 0.086) sd 0.172) su 0.086)) - SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≥	5.8%	NSR open ratio be as uniform as possible over the chip . NSR open ratio definition: (((((((!SP) - RESNW) - NSRBL) - INST) su 0.095) sd 0.19) su 0.095) + (((((!SP) * INST) - NSRBL) su 0.086) sd 0.172) su 0.086)) - SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≥	5.8%
SSD.DN.2a	NSR open ratio should be as uniform as possible over the chip . NSR open ratio definition: (((((((!SP) - RESNW) - NSRBL) - INST) su 0.095) sd 0.19) su 0.095) + (((((!SP) * INST) - NSRBL) su 0.086) sd 0.172) su 0.086)) - SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≤	18%	NSR open ratio should be as uniform as possible over the chip . NSR open ratio definition: (((((((!SP) - RESNW) - NSRBL) - INST) su 0.095) sd 0.19) su 0.095) + (((((!SP) * INST) - NSRBL) su 0.086) sd 0.172) su 0.086)) - SPDUM) * ALL_AA) - (ALL_GT)) density across full chip	≤	18%

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Rule number	Chip level density check rule			IP level density check rule		
	Description	O pt.	Design Value	Description	O pt.	Design Value
M0.D.1	ALL_M0 density (window 125um*125um, stepping 62.5um), except MARKS, RESP1, LOGO regions	≥	5%	ALL_M0 density (window 125um*125um, stepping 125um/step_number), except MARKS, RESP1, LOGO regions	≥	5.3%
M0.D.2	ALL_M0 density (window 20um*20um, stepping 10um), except MARKS, LOGO, OCOVL, RESP1, (NODMF su 1um) regions	≥	1.2%	ALL_M0 density (window 20um*20um, stepping 20um/step_number), except MARKS, LOGO, OCOVL, RESP1, (NODMF su 1um) regions	≥	1.3%
M0.D.3	ALL_M0 density (window 20um*20um, stepping 10um), except INST, OCOVL regions	≤	40%	ALL_M0 density (window 20um*20um, stepping 20um/step_number), except INST, OCOVL regions	≤	40%
M0C.D.1	Full chip ALL_M0C density	≥	5%	Full chip ALL_M0C density	≥	5%
M0C.D.2	ALL_M0C density (window 125 um*125um, stepping 62.5um), except LOGO region	≥	5%	ALL_M0C density (window 125 um*125um, stepping 125um/step_number), except LOGO region	≥	5.3%
M0C.D.3	ALL_M0C density in window 125um*125 um, stepping 62.5um), except INST region	≤	40%	ALL_M0C density in window 125um*125 um, stepping 125um/step_number), except INST region	≤	38%
M0G.D.1	ALL_M0G density (window 125um*125um, stepping 62.5um), except 1. NODMF su 1um region. 2. MARKS su 1um region 3. LOGO, RESP1 region	≥	1%	ALL_M0G density (window 125um*125um, stepping 125um/step_number), except 1. NODMF su 1um region. 2. MARKS su 1um region 3. LOGO, RESP1 region	≥	1.1%
M0G.D.2	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density (window 125um*125um, stepping 62.5um), except RESP1 and LOGO region	≥	6%	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density (window 125um*125um, stepping 125um/step_number), except RESP1 and LOGO region	≥	6.3%
M0G.D.3	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density in RESP1 region (window 125um*125um, stepping 62.5um)	≥	5%	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density in RESP1 region (window 125um*125um, stepping 125um/step_number)	≥	5%
M0G.D.4	ALL_M0G density (window 20um x20um, stepping 10um), except OCOVL region	≤	20%	ALL_M0G density (window 20um x20um, stepping 20um/step_number), except OCOVL region	≤	19%
M0G.D.5	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density (window 20um*20um, stepping 10um), , except OCOVL region	≤	45%	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density (window 20um*20um, stepping 20um/step_number) , except OCOVL region	≤	42.8%
V0.D.1 <sup>[R]</sup>	(V0 OR RV0) density (window 5um*5um, stepping 2.5um)	<	7.7%	(V0 OR RV0) density (window 5um*5um, stepping 2.5um)	<	7.7%
M1.D.1	M1 density (window 125um*125um, stepping 62.5um)	≥	10%	M1 density (window 125um*125um, stepping 125um/step_number)	≥	10.5%
M1.D.2	M1 maximum density (window 125um*125um, stepping 62.5um)	≤	85%	M1 maximum density (window 125um*125um, stepping 125um/step_number)	≤	80.8%
M1.D.3	M1 density (window 50um*50um, stepping 25um), except the window (15% ≤ metal density < 25%) not interact 3um*3um empty area, except OCOVL, (NODMF su 1um) region	≥	25%	M1 density (window 50um*50um, stepping 50um/step_number), except the window (15.8% ≤ metal density < 26.3%) not interact 3um*3um empty area, except OCOVL, (NODMF su 1um) region	≥	26.3%
M1.D.4	M1 maximum density (window 50um*50um,	≤	65%	M1 maximum density (window 50um*50um,	≤	65%

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Rule number	Chip level density check rule			IP level density check rule		
	Description	O pt.	Design Value	Description	O pt.	Design Value
	stepping 25um), except dummy metal			stepping 25um), except dummy metal		
M1.D.5	M1 maximum density (window 50um*50um, stepping 25um)	≤	75%	M1 maximum density (window 50um*50um, stepping 50um/step_number)	≤	71.3%
M1.D.6	M1 density difference between any two neighboring checking windows (window 180 um*180um, stepping 180um).	≤	40%	M1 density difference between any two neighboring checking windows (window 180 um*180um, stepping 360um/step_number).	≤	38%
M1.D.7	M1 maximum density ratio of ((M1 or dummy M1) INTERACT M1DPMK) to (M1 or dummy M1) (window 72um*72um, stepping 36um)	≤	30%	M1 maximum density ratio of ((M1 or dummy M1) INTERACT M1DPMK) to (M1 or dummy M1) (window 72um*72um, stepping 72um/step_number)	≤	28.5%
Vy.D.1 <sup>[R]</sup>	(Vy OR RVy) density (window 5um*5um, stepping 2.5um)	<	7.7%	(Vy OR RVy) density (window 5um*5um, stepping 2.5um)	<	7.7%
Mxy.D.1	Mxy density (window 50um*50um, stepping 25um), except the window (15% ≤ metal density < 25%) not interact 3um*3um empty area, except OCOVL region, (NODMF su 1um)	≥	25%	Mxy density (window 50um*50um, stepping 50um/step_number), except the window (15.8% ≤ metal density < 26.3%) not interact 3um*3um empty area, except OCOVL region, (NODMF su 1um)	≥	26.3%
Mxy.D.2	Mxy maximum density (window 50um*50um, stepping 25um), except dummy metal	≤	65%	Mxy maximum density (window 50um*50um, stepping 25um), except dummy metal	≤	65%
Mxy.D.3	Mxy maximum density (window 50um*50um, stepping 25um)	≤	75%	Mxy maximum density (window 50um*50um, stepping 50um/step_number)	≤	71.3%
Mxy.D.4	Mxy density difference between any two neighboring checking windows (window 180 um*180um, stepping 90um)	≤	40%	Mxy density difference between any two neighboring checking windows (window 180 um*180um, stepping 180um/step_number)	≤	38%
Mxy.D.6	It is not allowed to have local density of all three consecutive metal (Mxy, Mxy+1, Mxy+2) over any 30um*30um (stepping 15um), except NODMF su 0.4um region.  The metal layers of Mxy+1 and Mxy+2 include Mxy, 1.25xMy, 1.25xMn, and relevant dummy metals.	≤	5%	It is not allowed to have local density of all three consecutive metal (Mxy, Mxy+1, Mxy+2) over any 30um*30um (stepping 30um/step_number), except NODMF su 0.4um region.  The metal layers of Mxy+1 and Mxy+2 include Mxy, 1.25xMy, 1.25xMn, and relevant dummy metals.	≤	5.3%
Mxy.D.7	Mxy density ratio of ((Mxy or dummy Mxy) INTERACT ((MxyDPMK OR MxyCA) OR MxyCB)) to (Mxy or dummy Mxy) in window 72um*72um, step size: 36um, except OCOVL region	≤	30%	Mxy density ratio of ((Mxy or dummy Mxy) INTERACT ((MxyDPMK OR MxyCA) OR MxyCB)) to (Mxy or dummy Mxy) in window 72um*72um, step size: 72um/step_number, except OCOVL region	≤	28.5%
1.25xMy.DN.1	1.25xMy Density (window 50um*50um, stepping 25um), except LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	≥	10%	1.25xMy Density (window 50um*50um, stepping 50um/step_number), except LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	≥	10.5%
1.25xMy.DN.1a	1.25xMy Density (window 50um*50um, stepping 25um), except the window not interact 3um*3um empty area, LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	≥	25%	1.25xMy Density (window 50um*50um, stepping 50um/step_number), except the window not interact 3um*3um empty area, LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	≥	26.3%
1.25xMy.DN.2 <sup>[R]</sup>	1.25xMy maximum density (window 50um*50um, stepping 25um), except dummy metal	≤	65%	1.25xMy maximum density (window 50um*50um, stepping 25um), except dummy metal	≤	65%

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Rule number	Chip level density check rule			IP level density check rule		
	Description	O pt.	Design Value	Description	O pt.	Design Value
1.25xMy.DN.3	1.25xMy maximum density (window 50um*50um, stepping 25um)	≤	75%	1.25xMy maximum density (window 50um*50um, stepping 50um/step_number)	≤	71.3%
1.25xMy.DN.4	1.25xMy density difference between two neighboring checking windows (window 180um*180um, stepping 180um), except (NODMF su 0.4um) region.	≤	50%	1.25xMy density difference between two neighboring checking windows (window 180um*180um, stepping 360um/step_number), except (NODMF su 0.4um) region.	≤	47.5%
1.25xMy.DN.5	It is not allowed to have local density < 5% of all 3 consecutive metal layers over any 30um*30um window (stepping 15um), except (NODMF su 0.4um) region.			It is not allowed to have local density < 5.3% of all 3 consecutive metal layers over any 30um*30um window (stepping 30um/step_number), except (NODMF su 0.4um) region.		
1.25xVn.D.1 <sup>[R]</sup>	(1.25xVn OR 1.25xRVn) density (window 5um*5um, stepping 2.5um)	<	12%	(1.25xVn OR 1.25xRVn) density (window 5um*5um, stepping 2.5um)	<	12%
1.25xMn.DN.1	1.25xMn Density (window 50um*50um, stepping 25um), except LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions.	≥	10%	1.25xMn Density (window 50um*50um, stepping 50um/step_number), except LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions.	≥	10.5%
1.25xMn.DN.1a	1.25xMn Density (window 50um*50um, stepping 25um), except the window not interact 3um*3um empty area, LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	≥	25%	1.25xMn Density (window 50um*50um, stepping 50um/step_number), except the window not interact 3um*3um empty area, LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	≥	26.3%
1.25xMn.DN.2 <sup>[R]</sup>	1.25xMn maximum density (window 50um*50um, stepping 25um), except dummy metal. DRC doesn't check (1.25xMn AND DUPMK1) region when the 1.25xMn layer is used as TM-1.	≤	65%	1.25xMn maximum density (window 50um*50um, stepping 25um), except dummy metal. DRC doesn't check (1.25xMn AND DUPMK1) region when the 1.25xMn layer is used as TM-1.	≤	65%
1.25xMn.DN.3	Maximum 1.25xMn density (window 50um*50um, stepping 25um). DRC doesn't check (1.25xMn AND DUPMK1) region when the 1.25xMn layer is used as TM-1.	≤	75%	Maximum 1.25xMn density (window 50um*50um, stepping 50um/step_number). DRC doesn't check (1.25xMn AND DUPMK1) region when the 1.25xMn layer is used as TM-1.	≤	71.3%
1.25xMn.DN.4	1.25xMn density difference between two neighboring checking windows (window 180um*180um, stepping 180um), except (NODMF) su 0.4um region	≤	50%	1.25xMn density difference between two neighboring checking windows (window 180um*180um, stepping 360um/step_number), except (NODMF) su 0.4um region	≤	47.5%
1.25xMn.DN.6	It is not allowed to have local density < 5% of all 3 consecutive metal layers over any 30um*30um window (stepping 15um), except (NODMF) su 0.4um region			It is not allowed to have local density < 5.3% of all 3 consecutive metal layers over any 30um*30um window (stepping 30um/step_number), except (NODMF) su 0.4um region		
2xMn.D.N.1	2xMn density (window 112um*112um, stepping 56um), except INDMY, LOGO regions	≥	10%	2xMn density (window 112um*112um, stepping 112um/step_number), except INDMY, LOGO regions	≥	10.5%
2xMn.D.N.2	2xMn density (window 112um*112um, stepping 56um), except INDMY region	≤	85%	2xMn density (window 112um*112um, stepping 112um/step_number), except INDMY region	≤	80.8%
2xMn.D.N.3a	2xMn density (window 760um*760um, stepping 380um)	≤	70%	2xMn density (window 760um*760um, stepping 760um/step_number)	≤	66.5%
2xMn.D.N.3b	Full chip 2xMn density	≥	20%	Full chip 2xMn density	≥	20%

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Rule number	Chip level density check rule			IP level density check rule		
	Description	O pt.	Design Value	Description	O pt.	Design Value
2xMn.D N.4	2xMn density (window 72um*72um, stepping 36um), except (NODMF) su 0.4um region	≥	1%	2xMn density (window 72um*72um, stepping 72um/step_number), except (NODMF) su 0.4um region	≥	1%
2xMn.D N.5	2xMn density difference (window 180um*180um, stepping 180um), except (NODMF) su 0.4um region	≤	50%	2xMn density difference (window 180um*180um, stepping 360um/step_number), except (NODMF) su 0.4um region	≤	47.5%
2xMn.D N.6	It is not allowed to have local density < 5% of all 3 consecutive metal (1.25xMy/1.25Mn, 2xMn, 2xMn+1) over any window 30*30um (stepping 15um).The metal layers include M1/Mn and dummy metals, except (NODMF) su 0.4um region			It is not allowed to have local density < 5.3% of all 3 consecutive metal (1.25xMy/1.25Mn, 2xMn, 2xMn+1) over any window 30*30um (stepping 30um/step_number).The metal layers include M1/Mn and dummy metals, except (NODMF) su 0.4um region		
10xTMn .DN.1	10xTMn density (window 112um*112um, stepping 56um), except DUPMK1, PAD, INDMY, LOGO regions	≥	10%	10xTMn density (window 112um*112um, stepping 112um/step_number), except DUPMK1, PAD, INDMY, LOGO regions	≥	10.5%
10xTMn .DN.2	10xTMn density (window 112um*112um, stepping 56um), except DUPMK, PAD, LOGO regions	≤	85%	10xTMn density (window 112um*112um, stepping 112um/step_number), except DUPMK, PAD, LOGO regions	≤	80.8%
10xTMn .DN.3	10xTMn density difference between any two neighboring checking windows (window 180um*180um, stepping 180um), except NODMF su 0.4um region.	≤	50%	10xTMn density difference between any two neighboring checking windows (window 180um*180um, stepping 360um/step_number), except NODMF su 0.4um region.	≤	47.5%
10xTMn .DN.4	10xTMn full chip density	≥	20%	10xTMn full chip density	≥	20%
14xTMn .DN.1	14xTMn density (window 112um*112um, stepping 56um), except DUPMK1, PAD and INDMY, LOGO regions	≥	10%	14xTMn density (window 112um*112um, stepping 112um/step_number), except DUPMK1, PAD and INDMY, LOGO regions	≥	10.5%
14xTMn .DN.2	14xTMn density (window 112um*112um, stepping 56um), except DUPMK1, PAD and INDMY, LOGO regions	≤	85%	14xTMn density (window 112um*112um, stepping 112um/step_number), except DUPMK1, PAD and INDMY, LOGO regions	≤	80.8%
14xTMn .DN.3	14xTMn density difference between any two neighboring checking windows (window 180um*180um, stepping 180um), except NODMF su 0.4um region.	≤	50%	14xTMn density difference between any two neighboring checking windows (window 180um*180um, stepping 360um/step_number), except NODMF su 0.4um region.	≤	47.5%
14xTMn .DN.4	14xTMn full chip density	≥	20%	14xTMn full chip density	≥	20%
UTM.D N.1	UTM full chip density	≥	20%	UTM full chip density	≥	20%
UTM.D N.2	UTM full chip density	≤	50%	UTM full chip density	≤	50%
UTM.D N.3	UTM density (window 112um*112um, stepping 56um), except DUPMK1, PAD, NODMF, MARKS, LOGO and INDMY regions	≥	10%	UTM density (window 112um*112um, stepping 112um/step_number), except DUPMK1, PAD, NODMF, MARKS, LOGO and INDMY regions	≥	10.5%
UTM.D N.4	UTM density (window 112um*112um, stepping 56um), except DUPMK1, PAD, NODMF, MARKS, LOGO regions	≤	85%	UTM density (window 112um*112um, stepping 112um/step_number), except DUPMK1, PAD, NODMF, MARKS, LOGO regions	≤	80.8%
ALPA.D N.1	ALPA full chip density	≥	10%	ALPA full chip density	≥	10%

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Rule number	Chip level density check rule			IP level density check rule		
	Description	O pt.	Design Value	Description	O pt.	Design Value
ALPA.D N.2	ALPA full chip density	≤	70%	ALPA full chip density	≤	70%
WBPAD .6	Wire bond pad design must have dense TV between TM and TM-1.  The TV density under wire bond pad.  DRC check the (wire bond pad sd 1um) area where density ratio = (TV area)/(wire bond pad area), with window size 10umx10um, step 5um.	≥	10%	Wire bond pad design must have dense TV between TM and TM-1.  The TV density under wire bond pad.  DRC check the (wire bond pad sd 1um) area where density ratio = (TV area)/(wire bond pad area), with window size 10umx10um, step 10um/step_number.	≥	10.5%
HR.DN. 1	(DIR OR DIRDMP) density in window 20umx20um,stepping 10um	≤	50%	(DIR OR DIRDMP) density in window 20umx20um,stepping 20um/step_number	≤	50%
HR.DN. 2	(DIR OR DIRDMP) full chip density	≤	30%	(DIR OR DIRDMP) full chip density	≤	30%
MIM.D. 7 <sup>[R]</sup>	MIM density, except LOGO region  Dummy MIM pattern is required if MIM density is less than 3%. Note that if dummy MIM is added, dummy CTOP need be added correspondingly.	≥	3%	MIM density, except LOGO region  Dummy MIM pattern is required if MIM density is less than 3%. Note that if dummy MIM is added, dummy CTOP need be added correspondingly.	≥	3%

## 4. DRC switch setting table:

Rule number	Default Turn On	Default Turn Off
V0.ORCS.1		Y
M1.ORCS.1/.2/.3/.1a		Y
Mxy.ORCS.1/.2/.3		Y
M1.D.8, Mxy.D.8		Y
ME rules		Y
TBS rules		Y
DFM priority-1 rule		Y
DFM priority-2 rule		Y
MIM.6 <sup>[R]</sup> , MIM.7 <sup>[R]</sup> , MIM.12 <sup>[R]</sup> , CTOP.6 <sup>[R]</sup> , 1.25xMy.DN.2 <sup>[R]</sup> , 1.25xMn.DN.2 <sup>[R]</sup> , V0.D.1 <sup>[R]</sup> , Vy.D.1 <sup>[R]</sup> , 1.25xVn.D.1 <sup>[R]</sup> , V0.R.6 <sup>[R]</sup> , Vy.R.10 <sup>[R]</sup> , 1.25xVn.R.10 <sup>[R]</sup>	Y	
OCCD, OCOVL rules	Y	

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Rule number	Default Turn On	Default Turn Off
FEOL(7.2.1~7.2.34, 7.3, 7.8.1~7.8.6)	Y	
BEOL(7.2.35~7.2.51, 7.4, 7.8.7~7.8.9)	Y	
DUMC rule	Y	
IP level density check		Y
<b>DOUBLE_PATTENING_RULES_CHECK</b> <i>(also check V0.OR.?, M1.OR.?, Mxy.OR.?, M1.S.19, M1.S.20, Mxy.R.2, Mxy.R.3, M1.OR.15.DFM, M1.ORCS.2.ME, V0.R.1.DFM)</i>	Y	
<b>DOUBLE_PATTENING_RULES_CHECK_ONLY</b> <i>(only check V0.OR.?, M1.OR.?, Mxy.OR.?, M1.S.19, M1.S.20, Mxy.R.2, Mxy.R.3, M1.OR.15.DFM, M1.ORCS.2.ME, V0.R.1.DFM)</i>		Y
Latch-Up(85°C) prevention layout guidelines	Y	
Latch-Up(85~125°C) prevention layout guidelines		Y

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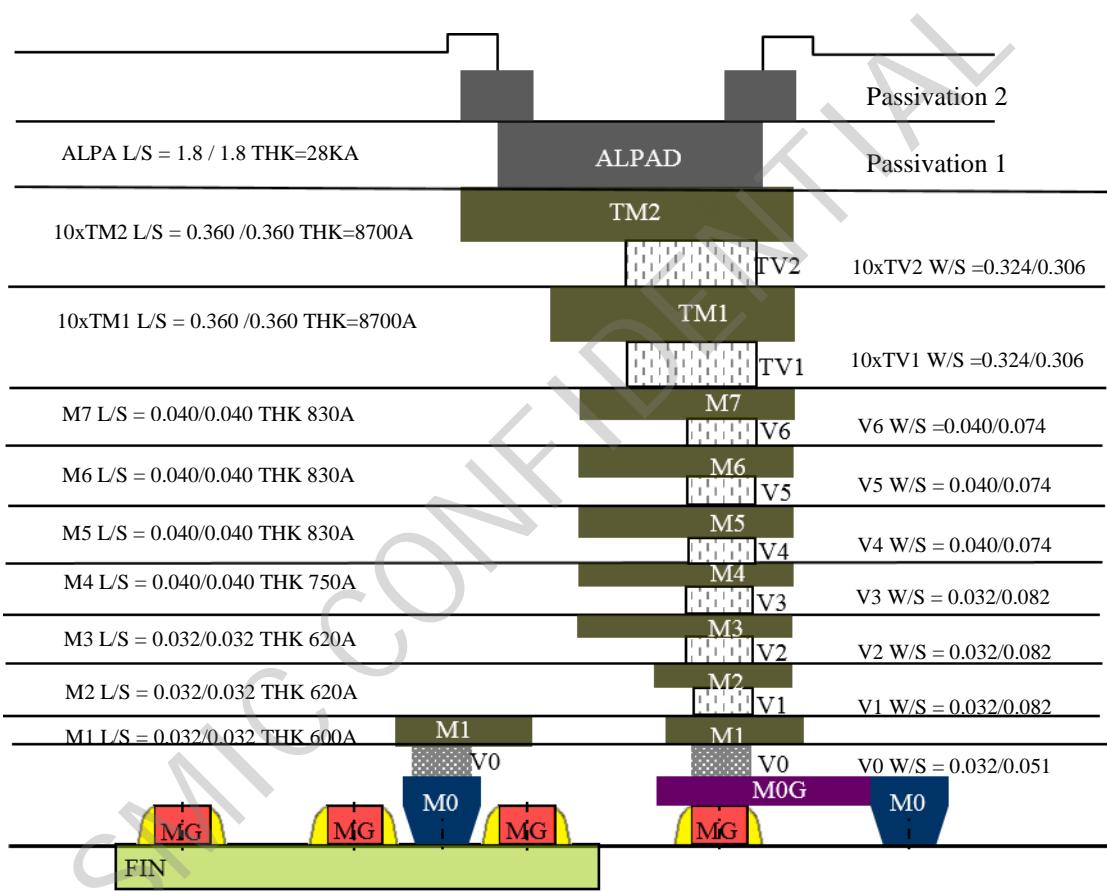
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### 7.1.5 Cross section

1. Cross section sample:

(1) 1P9M\_DV\_3DM\_Q1\_3Q2\_2TMa\_ALPA2



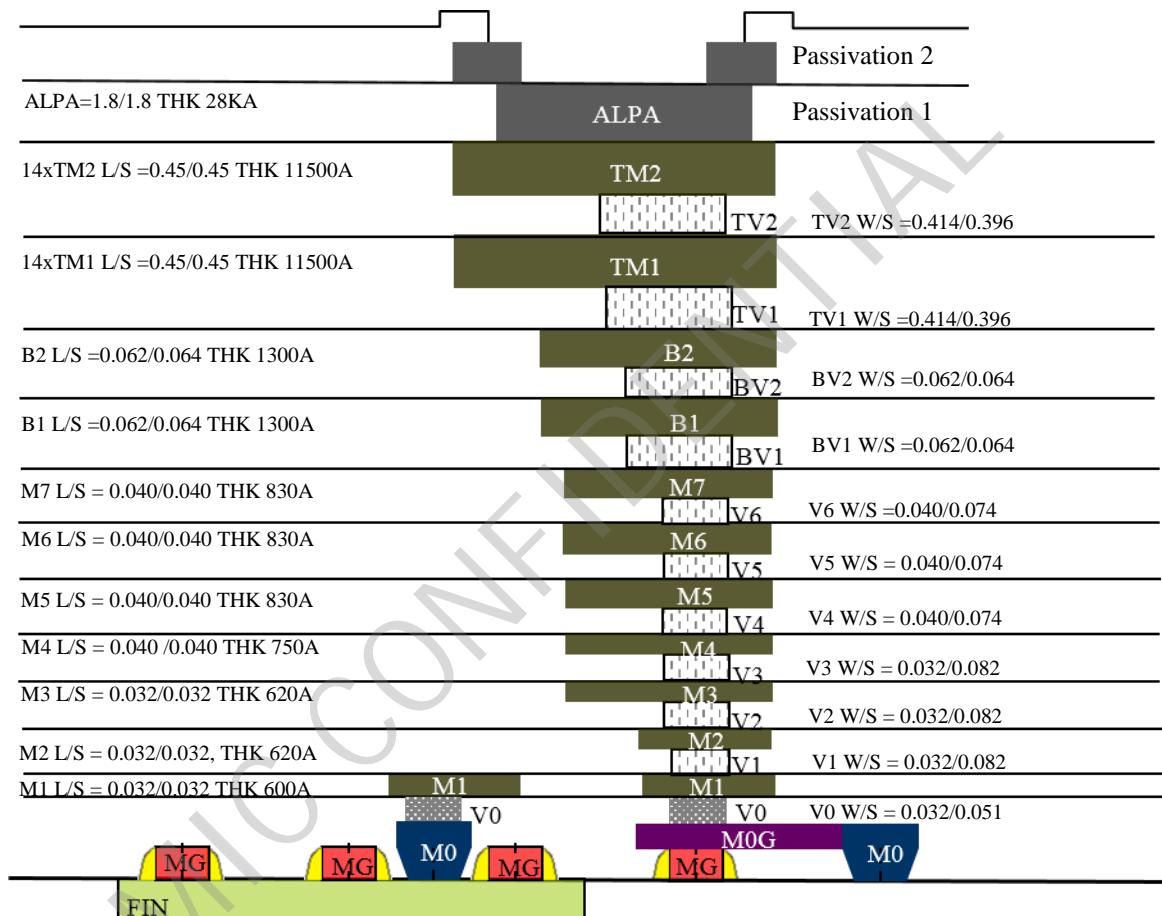
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(2) 1P11M\_DV\_3DM\_Q1\_3Q2\_2B\_2TMb\_ALPA2



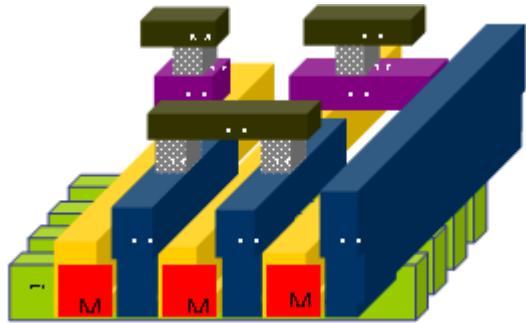
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## 2. Sketch map sample of 3D



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### 7.1.6 Metallization Options

1. 14nm metal options definition scheme was denoted in this section for metal layer and dielectric type, and is limited only to those materials present in the stack. The thickness in metal option table is only for customer general reference, please refer PCM spec table for the accurate value.

The scheme uses the following naming:

**xPyM\_pDV\_zDM\_aQ1\_bQ2\_eB\_mTMr\_nUTM\_ALPAu**

Where:

- P** = GT layers,
- M** = total metal layers excluding AL pad/Al RDL,
- DV** = Via layers with double patterning (including V0),
- DM** = Cu inter metal layers with double patterning (including M1),
- Q1** = Cu inter metal layers for 1.25xMy
- Q2** = Cu inter metal layers for 1.25xMn
- B** = Cu inter metal layers for 2xMn
- TM** = Cu top metal layers
- UTM** = Cu ultra thick metal layer
- ALPA** = AL pad/AL RDL layers,
- x** = number of GT layers,
- y** = number of total metal layers excluding ALPA, where  $y = z+a+b+e+m+n$
- p** = number of double patterning via layers (including V0)
- z** = number of double patterning metal layers (including M1)
- a** = number of 1.25xMy layers
- b** = number of 1.25xMn layers
- e** = number of 2xMn layers
- m** = number of 10xTMn/14xTMn layers
- n** = number of ultra thick metal layers
- r** = type of TM, type a for 10xTM, type b for 14xTM
- u** = type of AL, type 1 for AL14.5kA, type 2 for AL28kA

For the parameters of p, z, a, b,e, m and n:

- 1), if the value equal to "0", the relevant items should be removed from relevant scheme title, and
- 2), if the value equal to "1", then the character of 1 can be omitted in the relevant scheme title.

For example: **1P8M\_DV\_3DM\_Q1\_2Q2\_2TMa\_ALPA**



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Table 1: 10xTMn/UTM top metal options

Metallization Options Table			Mask Code	Mask Name	IP8M_DV_3DM_Q1_3Q 2_TMa_ALPA1	IP9M_DV_3DM_Q1_4Q 2_TMa_ALPA1	IP9M_DV_3DM_Q1_3Q 2_2TMA_ALPA1	IP10M_DV_3DM_Q1_4 Q2_2TMA_ALPA1	IP8M_DV_3DM_Q1_3Q 2_UTM_ALPA1	IP8M_DV_3DM_Q1_2Q 2_TMa_UTM_ALPA1	IP8M_DV_3DM_Q1_3Q 2_TMa_ALPA2	IP9M_DV_3DM_Q1_4Q 2_TMa_ALPA2	IP9M_DV_3DM_Q1_3Q 2_2TMA_ALPA2	IP10M_DV_3DM_Q1_4 Q2_2TMA_ALPA2	IP8M_DV_3DM_Q1_3Q 2_UTM_ALPA2	IP8M_DV_3DM_Q1_2Q 2_TMa_UTM_ALPA2
Total Cu metal					8	9	9	10	8	8	8	9	9	10	8	8
Double Patterning Metal layer (from M1)					3	3	3	3	3	3	3	3	3	3	3	3
V0 minimum W/S=0.032/0.051um (DP layer)	370/770	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0
M1 minimum W/S=0.032/0.032um (DP layer) M1 typical thickness: 600A M1 typical Sheet Resistance: 0.95 ohm/sq	160/760	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
Vy minimum W/S=0.032/0.082um Mxy minimum W/S=0.032/0.032um (DP layer) Mxy typical thickness: 620A Mxy typical Sheet Resistance: 0.95 ohm/sq	178	V1	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy
	180/780	M2	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy
	179	V2	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy
	181/781	M3	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy
	177	V3	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy
1.25xMy minimum W/S=0.04/0.04um 1.25xMy typical thickness: 750A 1.25xMy typical Sheet Resistance: 0.63 ohm/sq 1.25xVn minimum W/S=0.04/0.074um 1.25xMn minimum W/S=0.04/0.04um 1.25xMn typical thickness: 830A 1.25xMn typical Sheet Resistance: 0.54 ohm/sq	182	M4	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy
	176	V4	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn
	183	M5	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn
	175	V5	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn
	184	M6	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn
	174	V6	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn
	185	M7	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn

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Metallization Options Table														
10xTVn minimum W/S=0.324/0.306um 10xTMn minimum W/S=0.36/0.36um 10xTMn typical thickness: 8700A 10xTMn typical Sheet Resistance: 0.022 ohm/sq UTV minimum W/S=0.324/0.306um UTM minimum W/S=1.8/0.9um UTM typical thickness: 30000A UTM typical Sheet Resistance: 0.005 ohm/sq	Mask Code	Mask Name	1P8M_DV_3DM_Q1_3Q 2_TMa_ALPA1	1P9M_DV_3DM_Q1_4Q 2_TMa_ALPA1	1P9M_DV_3DM_Q1_3Q 2_2TMA_ALPA1	1P10M_DV_3DM_Q1_4 Q2_2TMA_ALPA1	1P8M_DV_3DM_Q1_3Q 2_UTM_ALPA1	1P8M_DV_3DM_Q1_2Q 2_TMa_UTM_ALPA1	1P8M_DV_3DM_Q1_3Q 2_TMa_ALPA2	1P9M_DV_3DM_Q1_4Q 2_TMa_ALPA2	1P9M_DV_3DM_Q1_3Q 2_2TMA_ALPA2	1P10M_DV_3DM_Q1_4 Q2_2TMA_ALPA2	1P8M_DV_3DM_Q1_3Q 2_UTM_ALPA2	1P8M_DV_3DM_Q1_2Q 2_TMa_UTM_ALPA2
	173	V7		1.25xVn		1.25xVn				1.25xVn		1.25xVn		
	186	M8		1.25xMn		1.25xMn				1.25xMn		1.25xMn		
	142	TV1			10xTVn	10xTVn		10xTVn		10xTVn		10xTVn		10xTVn
	141	TM1				10xTMn	10xTMn		10xTMn		10xTMn		10xTMn	
	324	CTOP				CTOP	CTOP				CTOP	CTOP		
	162	MIM				MIM	MIM				MIM	MIM		
	144	TV2	10xTVn	10xTVn	10xTVn	10xTVn	10xTVn		10xTVn	10xTVn	10xTVn	10xTVn		
	143	TM2	10xTMn	10xTMn	10xTMn	10xTMn	10xTMn		10xTMn	10xTMn	10xTMn	10xTMn		
	342	UTV					UTV	UTV					UTV	UTV
Passivation 1	107	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA
ALPA minimum W/S=1.8/1.8um (THK:14.5/28kA)	108	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA
Passivation 2	163	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD

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Table 2: 14xTMn top metal option

Metallization Options Table			Mask Code	Mask Name	1P9M_DV_3DM_Q1_3Q2 _2TMb_ALPA1	1P10M_DV_3DM_Q1_2Q _2_2B_2TMb_ALPA1	1P11M_DV_3DM_Q1_3Q _2_2B_2TMb_ALPA1	1P10M_DV_3DM_Q1_3Q2 _2TMb_ALPA1	1P10M_DV_3DM_Q1_2Q _2_2B_2TMb_ALPA2	1P11M_DV_3DM_Q1_3Q _2_2B_2TMb_ALPA2	1P10M_DV_3DM_Q1_3Q _2_2B_2TMb_ALPA2	
Total Cu metal					9	10	11	10	9	10	11	10
Double Patterning Metal layer (from M1)					3	3	3	3	3	3	3	3
V0 minimum W/S=0.032/0.051 (DP layer)	370/770	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0
M1 minimum W/S=0.032/0.032um (DP layer) M1 typical thickness: 600A M1 typical Sheet Resistance: 0.95 ohm/sq	160/760	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
Vy minimum W/S=0.032/0.082um Mxy minimum W/S=0.032/0.032um (DP layer) Mxy typical thickness: 620A Mxy typical Sheet Resistance: 0.95 ohm/sq	178	V1	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy
	180/780	M2	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy
	179	V2	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy
	181/781	M3	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy	Mxy
	177	V3	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy	Vy
1.25xMy minimum W/S=0.04/0.04um 1.25xMy typical thickness: 750A 1.25xMy typical Sheet Resistance: 0.63 ohm/sq 1.25xVn minimum W/S=0.04/0.074um 1.25xMn minimum W/S=0.04/0.04um 1.25xMn typical thickness: 830A 1.25xMn typical Sheet Resistance: 0.54 ohm/sq	182	M4	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy	1.25xMy
	176	V4	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn
	183	M5	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn
	175	V5	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn	1.25xVn
	184	M6	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn	1.25xMn
	174	V6	1.25xVn		1.25xVn	1.25xVn	1.25xVn		1.25xVn	1.25xVn	1.25xVn	1.25xVn
	185	M7	1.25xMn		1.25xMn	1.25xMn	1.25xMn		1.25xMn	1.25xMn	1.25xMn	1.25xMn
	173	V7										

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Metallization Options Table			Mask Code	Mask Name	IP9M_DV_3DM_Q1_3Q2 _2TMb_ALPA1	IP10M_DV_3DM_Q1_2Q _2_2B_2TMb_ALPA1	IP11M_DV_3DM_Q1_3Q _2_2B_2TMb_ALPA1	IP10M_DV_3DM_Q1_3Q2 _2TMb_ALPA2	IP10M_DV_3DM_Q1_2Q _2_2B_2TMb_ALPA2	IP11M_DV_3DM_Q1_3Q _2_2B_2TMb_ALPA2
186	M8									
2xVn minimum W/S=0.062/0.064um	371	BV1			2xVn	2xVn	2xVn		2xVn	2xVn
2xMn minimum W/S=0.062/0.064um	280	B1			2xMn	2xMn	2xMn		2xMn	2xMn
2xMn typical thickness: 1300A	372	BV2			2xVn	2xVn	2xVn		2xVn	2xVn
2xMn typical Sheet Resistance: 0.278 ohm/sq	281	B2			2xMn	2xMn	2xMn		2xMn	2xMn
14xTVn minimum W/S=0.414/0.396um	142	TV1	14xTVn	14xTVn	14xTVn			14xTVn	14xTVn	14xTVn
14xTMn minimum W/S=0.45/0.45um	141	TM1	14xTMn	14xTMn	14xTMn			14xTMn	14xTMn	14xTMn
14xTMn typical thickness: 11500A	144	TV2	14xTVn	14xTVn	14xTVn	14xTVn	14xTVn	14xTVn	14xTVn	14xTVn
14xTMn typical Sheet Resistance: 0.016ohm/sq	143	TM2	14xTMn	14xTMn	14xTMn	14xTMn	14xTMn	14xTMn	14xTMn	14xTMn
Passivation 1	107	PA	PA	PA	PA	PA	PA	PA	PA	PA
ALPA min W/S=1.8/1.8um (THK:14.5/28kA)	108	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA	ALPA
Passivation 2	163	MD	MD	MD	MD	MD	MD	MD	MD	MD



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2. Designer must follow the available metal option for layout design strictly and draw layout on correct #gds/data type among metal options.

Definition of Data Type Usage for #gds of 61~69 and 70~77:

- 1) Data Type 0 is used for V0/M1/Mxy
- 2) Data Type 40 is used for Vy and 1.25xMy for the direction of the minimum pitch of 1.25xMy is parallel to GATE poly direction of core device
- 3) Data Type 50 is used for 1.25xVn and 1.25xMn for the direction of the minimum pitch of 1.25xMn is parallel to GATE poly direction of core device
- 4) Data Type 55 is used for 1.25xMn for the direction of the minimum pitch of 1.25xMn is perpendicular to GATE poly direction of core device
- 5) Data Type 0 is used for 2xVn/2xMn

Definition of Data Type Usage for #gds of 120~123, 148, 150:

- 1) Data Type 0 is used for 10xTVn/10xTMn, UTV/UTM
- 2) Data Type 40 is used for 14xTVn/14xTM

Layer Name	Mask Code	Data Type/ GDS No	Mxy	1.25xMy	1.25xMn	2xMn	10xTMn	14xTMn	UTM
			Vy	Vy	1.25xVn	2xVn	10xTVn	14xTVn	UTV
V0	370	245	-	-	-	-	-	-	-
M1	160	61	-	-	-	-	-	-	-
V1	178/	70	40	-	-	-	-	-	-
M2	180	62	0	-	-	-	-	-	-
V2	179	71	40	-	-	-	-	-	-
M3	181	63	0	-	-	-	-	-	-
V3	177	72	40	40	-	-	-	-	-
M4	182	64	-	40	-	-	-	-	-
V4	176	73	-	-	50	-	-	-	-
M5	183	65	-	-	55	-	-	-	-
V5	175	74	-	-	50	-	-	-	-
M6	184	66	-	-	50	-	-	-	-
V6	174	75	-	-	50	-	-	-	-
M7	185	67	-	-	55	-	-	-	-
V7	173	76	-	-	50	-	-	-	-

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Layer Name	Mask Code	Data Type/ GDS No	Mxy	1.25xMy	1.25xMn	2xMn	10xTMn	14xTMn	UTM
			Vy	Vy	1.25xVn	2xVn	10xTVn	14xTVn	UTV
M8	186	68	-	-	50	-	-	-	-
BV1	371	135	-	-	-	0	-	-	-
B1	280	141	-	-	-	0	-	-	-
BV2	372	136	-	-	-	0	-	-	-
B2	281	142	-	-	-	0	-	-	-
TV1	142	121	-	-	-	-	0	40	-
TM1	141	120	-	-	-	-	0	40	-
TV2	144	123	-	-	-	-	0	40	-
TM2	143	122	-	-	-	-	0	40	-
UTV	342	148	-	-	-	-	-	-	0
UTM	352	150	-	-	-	-	-	-	0
PA	107	80	-	-	-	-	-	-	-
ALPA	108	83	-	-	-	-	-	-	-
MD	163	130	-	-	-	-	-	-	-

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### 7.1.7 Drawn layer Mapping Table

Design layer name	GDS layer No	GDS data type	Layer Description
CELLB	127	2	Cell boundary
CHIPB	127	3	Chip boundary, chip level must border layer
AA	10	0	Active Area
AADUM	10	1	AA auto-insertion Dummy Layer without OPC engineering
AADOP	10	7	AA auto-insertion Dummy layer with OPC engineering
AADMP	10	8	AA Manually drawn dummy layer with OPC engineering
AR	11	0	Fin cut layer for SDB
ARDUM	11	11	AR auto-insertion Dummy Layer without OPC engineering
ARDOP	11	17	AR auto-insertion Dummy pattern layer with OPC engineering
ARDUB	11	6	AR Dummy Blockage layer to block AR dummy insertion
AR_H	131	30	Fin cut off layer 1
AR_HDOP	131	27	Fin cut off layer 1 auto DUMMY
AR_V	131	31	Fin cut off layer 2
AR_VDOP	131	37	Fin cut off layer 2 auto DUMMY
ARBL	131	151	Blocking Layer for AR_H, AR_V generation
NW	14	0	NW
DNW	19	0	Deep N well
DG	29	0	1.8V IO layer
DGV	29	1	1.8V UD 1.2V marker layer
DGUD	29	3	1.8V UD 1.5V marker layer
DIR	119	0	TiN resistor layer
DIRDMP	119	8	TiN resistor manually drawn dummy
DMCMK1	131	159	FEOL Dummy cell maker layer

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Design layer name	GDS layer No	GDS data type	Layer Description
DMCMK2	131	160	BEOL Dummy cell maker layer
DMPNP	134	0	BJT marker layer
DSTR	138	0	Diode marker layer
FIN	13	50	Fin drawn
FUSE	81	0	Passivation opening for Al fuse window
GT	30	0	GT GATE
GTDUM	30	1	GT Dummy Layer
GTDOP	30	7	GT Dummy pattern layer for OPC engineering
GTDMMP	30	8	Manually drawn poly dummy layer with OPC engineering
INDMY	212	0	Inductor mark layer
KV	9	0	Alignment Mark Clear Out
LDBK	216	150	LDMOS mark layer
MIM	58	0	Top Plate of MIM Capacitor
MIMDUM	58	11	MIM auto-insertion Dummy Layer without OPC engineering
CTOP	222	0	Bottom Plate of MIM Capacitor for 32nm and below technology
CTOPDUM	222	11	CTOP auto-insertion Dummy Layer without OPC engineering
IDT	49	0	Inductor Trench/Inbuilt Deep Trench
MIMDMY	211	0	MIM Dummy Layer
NLDB	12	150	N+ LDD and pocket implant blockage/prevention
NPAA	12	0	Planar AA reservation
NSRDS1	5	51	NSR dummy treat 1
NSRBL	5	239	SiP blockage
P2	31	0	GT GATE trim slot
P2DUM	31	1	P2 Dummy Layer(For dummy P2 insertion)

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Design layer name	GDS layer No	GDS data type	Layer Description
P2DOP	31	7	P2 Dummy pattern layer is referenced in OPC engineering
P2DMP	31	8	Manually drawn P2 dummy layer with OPC engineering
PLDB	13	150	P+ LDD and pocket implant blockage/prevention
PLRES	96	3	LVS and DRC mark layer for H-R resistor type 2
PPAA	13	0	Pre-FIN
PSRDS1	6	51	PSR dummy treat 1
PSRBL	6	239	SiGe blockage
PSUB	85	0	Marking layer for native device
RESNW	95	0	Marking layer for NW resistor
RESP1	96	0	LVS and DRC mark layer for H-R resistor
RESP2	96	2	Marking layer for H-R & Metal resistor portion
RFDEV	181	0	Dummy layer for LVS to recognize RF Device
RSPMK1	131	153	Restricted Special Pattern Maker Layer 1
SMMK	84	239	Marking layer for area of SMT stress nitride
SNBL	12	138	Marking layer for blockage of N+ S/D Implant
SN	40	0	N+ S/D Implant
SNDUM	40	1	SN dummy layer
SPBL	13	239	Marking layer for blockage of P+ S/D Implant
SP	43	0	P+ S/D Implant
SPDUM	43	1	SP dummy layer
HVT_N	159	156	Marking layer for N-type high-Vt devices
HVT_P	159	166	Marking layer for P-type high-Vt devices
LVT_N	159	158	Marking layer for N-type low-Vt devices
LVT_P	159	168	Marking layer for P-type low-Vt devices

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Design layer name	GDS layer No	GDS data type	Layer Description
SVT_N	159	157	Marking layer for N-type standard-Vt devices
SVT_P	159	167	Marking layer for P-type standard-Vt devices
ULVT_N	159	159	Marker layer for N-type Ultra low Vth device
ULVT_P	159	169	Marker layer for P-type Ultra low Vth device
VARMOS	93	0	Block Layer to cover all MOS-type varactor
M0	59	0	Contact on AA
M0DUM	59	1	Metal-0 Dummy Layer (For dummy M0 insertion)
M0DOP	59	7	Metal-0 dummy pattern layer is referenced in OPC engineering
M0DMP	59	8	Manually drawn M0 dummy layer with OPC engineering
M0G	208	0	Contact on GT
M0GDUM	208	1	M0G dummy Layer (For dummy M0G insertion)
M0GDOP	208	7	M0G dummy pattern layer is referenced in OPC engineering
M0GDMP	208	8	Manually drawn M0G dummy layer with OPC engineering
M0C	246	0	M0 cut
M0CDUM	246	1	M0C Dummy Layer(For dummy M0C insertion)
M0CDOP	246	7	M0C Dummy pattern layer is referenced in OPC engineering
M0CDMP	246	8	Manually drawn M0C dummy layer with OPC engineering
V0	245	0	V0
V0DUM	245	1	V0 Dummy Layer(For dummy via insertion)
V0RB	245	8	Via-0 blockage layer to skip redundant via insertion
V0RM	245	10	Via-0 marker layer to identify redundant via
V0DPMK	245	20	Via-0 same color marker layer
V0CA	245	110	Marking layer for V0 color A
V0CB	245	120	Marking layer for V0 color B

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Design layer name	GDS layer No	GDS data type	Layer Description
V0DP	171	0	Via-0 Double Patterning 2 <sup>nd</sup> Mask
V0DPDUM	171	1	V0DP Dummy Layer(For dummy via insertion)
V1DUM	70	1	Via-1 dummy Layer (For dummy Via-1 insertion)
V1DOP	70	7	Via-1 dummy pattern layer is referenced in OPC engineering
V1RB	70	8	Via-1 blockage layer to skip redundant via insertion
V1RM	70	10	Via-1 mark layer to identify redundant via
V1_40	70	40	Via-1 Hole for data type 40 (Vy)
V2DUM	71	1	Via-2 Dummy Layer
V2DOP	71	7	Via-2 dummy data type 7
V2RB	71	8	Via-2 blockage layer to skip redundant via insertion
V2RM	71	10	Via-2 mark layer to identify redundant via
V2_40	71	40	Via-2 Hole for data type 40 (Vy)
V3DUM	72	1	via-3 Dummy Layer
V3DOP	72	7	V3 dummy data type 7
V3RB	72	8	Via-3 blockage layer to skip redundant via insertion
V3RM	72	10	V3 mark layer to identify redundant via
V3_40	72	40	Via-3 Hole for data type 40 (Vy)
V4DUM	73	1	via-4 Dummy Layer
V4DOP	73	7	V4 dummy data type 7
V4RB	73	8	Via-4 blockage layer to skip redundant via insertion
V4RM	73	10	V4 mark layer to identify redundant via
V4_50	73	50	Via-4 Hole for data type 50 (1.25xVn)
V5DUM	74	1	Via-5 Dummy Layer
V5DOP	74	7	V5 dummy data type 7

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Design layer name	GDS layer No	GDS data type	Layer Description
V5RB	74	8	Via-5 blockage layer to skip redundant via insertion
V5RM	74	10	V5 mark layer to identify redundant via
V5_50	74	50	Via-5 Hole for data type 50 (1.25xVn)
V6DUM	75	1	via-6 Dummy Layer
V6DOP	75	7	V6 dummy data type 7
V6RB	75	8	Via-6 blockage layer to skip redundant via insertion
V6RM	75	10	V6 mark layer to identify redundant via
V6_50	75	50	Via-6 Hole for data type 50 (1.25xVn)
V7DUM	76	1	via-7 Dummy Layer
V7DOP	76	7	V7 dummy data type 7
V7RB	76	8	Via-7 blockage layer to skip redundant via insertion
V7RM	76	10	V7 mark layer to identify redundant via
V7_50	76	50	Via-7 Hole for data type 50 (1.25xVn)
BV1	135	0	First 2X Via Hole (Only for 20nm and advanced technology)
BV1DUM	135	1	BV1 Dummy Layer(For dummy via insertion)
BV1DOP	135	7	BV1 Dummy pattern layer is referenced in OPC engineering
BV1RB	135	8	BV1 blockage layer to skip redundant via insertion
BV1RM	135	10	BV1 marker layer to identify redundant via
BV2	136	0	Second 2X Via Hole (Only for 20nm and advanced technology)
BV2DUM	136	1	BV2 Dummy Layer(For dummy via insertion)
BV2DOP	136	7	BV2 Dummy pattern layer is referenced in OPC engineering
BV2RB	136	8	BV2 blockage layer to skip redundant via insertion
BV2RM	136	10	BV2 marker layer to identify redundant via
TV1	121	0	Top Via 1

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Design layer name	GDS layer No	GDS data type	Layer Description
TV1DUM	121	1	TV-1 Dummy Layer
TV1RB	121	8	First top via blockage layer to skip redundant via insertion
TV1RM	121	10	TV1 mark layer to identify redundant via
TV1_40	121	40	First Top Via Hole for data type 40 (14xTV1)
TV2	123	0	Top Via 2
TV2DUM	123	1	TV-2 Dummy Layer
TV2RB	123	8	Second top via blockage layer to skip redundant via insertion
TV2RM	123	10	TV2 mark layer to identify redundant via
TV2_40	123	40	Second Top Via Hole for data type 40 (14xTV2)
UTV	148	0	Ultra Thick Via Hole
UTVDUM	148	1	UTV Dummy Layer(For dummy via insertion)
UTVDOP	148	7	UTV dummy pattern layer is referenced in OPC engineering
UTVRB	148	8	UTV blockage layer to skip redundant via insertion
UTVRM	148	10	UTV marker layer to identify redundant via
M1	61	0	Metal-1
M1DUM	61	1	Metal1 Dummy Layer
M1DOP	61	7	Metal 1 Dummy pattern layer for OPC engineering
M1DPMK	61	20	M1 same color marker layer
M1CA	61	110	Marking layer for M1 color A
M1CB	61	120	Marking layer for M1 color B
M1DP	175	0	Metal-1 Double Patterning 2 <sup>nd</sup> Mask, for internal usage only
M1DPDUM	175	1	M1DP Dummy Layer(For dummy via insertion)
M1DPDOP	175	7	M1DP dummy pattern layer is referenced in OPC engineering
M2	62	0	Metal-2

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Design layer name	GDS layer No	GDS data type	Layer Description
M2DUM	62	1	Metal2 Dummy Layer
M2DOP	62	7	Metal 2 Dummy pattern layer for OPC engineering
M2DPMK	62	20	M2 same color marker layer
M2CA	62	110	Marking layer for M2 color A
M2CB	62	120	Marking layer for M2 color B
M2DP	176	0	Metal-2 Double Patterning 2 <sup>nd</sup> Mask, for internal usage only
M2DPDUM	176	1	M2DP Dummy Layer(For dummy via insertion) (use for 20nm and advanced tech only)
M2DPDOP	176	7	M2DP dummy pattern layer is referenced in OPC engineering
M3	63	0	Metal-3
M3DUM	63	1	Metal3 Dummy Layer
M3DOP	63	7	Metal 3 Dummy pattern layer for OPC engineering
M3DPMK	63	20	M3 same color marker layer
M3CA	63	110	Marking layer for M3 color A
M3CB	63	120	Marking layer for M3 color B
M3DP	177	0	Metal-3 Double Patterning 2 <sup>nd</sup> Mask, for internal usage only
M3DPDUM	177	1	M3DP Dummy Layer(For dummy via insertion) (use for 20nm and advanced tech only)
M3DPDOP	177	7	M3DP dummy pattern layer is referenced in OPC engineering
M4DUM	64	1	Metal4 Dummy Layer
M4DOP	64	7	Metal 4 Dummy pattern layer for OPC engineering
M4_40	64	40	Metal-4 for data type 40 (1.25xMy)
M5DUM	65	1	Metal5 Dummy Layer
M5DOP	65	7	Metal 5 Dummy pattern layer for OPC engineering
M5_55	65	55	Metal-5 for data type 55 (1.25xMn)

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Design layer name	GDS layer No	GDS data type	Layer Description
M6DUM	66	1	Metal6 Dummy Layer
M6DOP	66	7	Metal 6 Dummy pattern layer for OPC engineering
M6_50	66	50	Metal-6 for data type 50 (1.25xMn)
M7DUM	67	1	Metal7 Dummy Layer
M7DOP	67	7	Metal 7 Dummy pattern layer for OPC engineering
M7_55	67	55	Metal-7 for data type 55 (1.25xMn)
M8DUM	68	1	Metal8 Dummy Layer
M8DOP	68	7	Metal 8 Dummy pattern layer for OPC engineering
M8_50	68	50	Metal-8 for data type 50 (1.25xMn)
B1	141	0	First-level 2x metal line in the ultralow-k dielectric # 2x Metal-1
B1DUM	141	1	2x Metal-1 Dummy Layer
B1SLOT	141	2	B1 Slot
B1DOP	141	7	2x Metal-1 Dummy Layer for OPC engineering (Only for 32nm and below technology use)
B2	142	0	Second-level 2x metal line in the ultralow-k dielectric # 2x Metal-2
B2DUM	142	1	2x Metal-2 Dummy Layer
B2SLOT	142	2	B2 Slot
B2DOP	142	7	2x Metal-2 Dummy Layer for OPC engineering (Only for 32nm and below technology use)
TM1	120	0	Top Metal 1
TM1DUM	120	1	TM-1 Dummy Layer
TM1_40	120	40	First Top Metal for data type 40 (14xTM1)
TM2	122	0	Top Metal 2
TM2DUM	122	1	TM2 Dummy Layer
TM2_40	122	40	Second Top Metal for data type 40 (14xTM2)

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Design layer name	GDS layer No	GDS data type	Layer Description
UTM	150	0	Ultra Thick Metal
UTMDUM	150	1	UTM Dummy Layer (For dummy metal insertion)
UTMSLOT	150	2	UTM Slot
UTMDOP	150	7	UTM Dummy pattern layer is referenced in OPC engineering
BIPOLA	159	1	Placed over emitters. It is used to generate PH and eliminate halos to improve bipolar performance
OTPMK1	89	160	OTP type 1 mark
PA	80	0	Passivation 1
ALPA	83	0	AL Bonding Pad and RDL
ALDUM	83	11	ALPA Dummy Layer
MD	130	0	Passivation 2 opening
BCB1	165	0	Repassivation for bump process
BUMP	168	0	UBM for bump
LFN_N	159	160	LFN_N device marker layer
LFN_P	159	170	LFN_P device marker layer

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### 7.1.8 CAD layer Mapping Table

Layer name	GDS No	Data Type	Description
ALDUB	83	6	ALPA Dummy block layer for ALPA dummy fill
AAOPM	10	30	AA OPC marking layer
ACMK1	89	166	DRC marker layer for analog circuit design
ANMK0	131	230	Marking layer for analog normal level matching device
ANMK1	131	172	Marking layer for analog medium level matching device
ANMK2	131	173	Marking layer for analog high level matching device
VDDMK1	131	175	Marking layer for Power (Vdd) PAD for DRC use
VSSMK1	131	176	Marking layer for Power (Vss) PAD for DRC use
LUWMK1	131	177	Marking layer for designer to waive some latch up rules
ALPAR	83	1	LVS marker layer for ALPA Resistor
ALPATXT	83	2	ALPA Text Layer, label text
BORDER	127	0	Marking layer for chip edge
PRBOUN	127	1	PR boundary
DCTY	139	0	Area with no Extraction for LVS
DFI	139	1	DFI Filler Cell Area with no LVS extraction
DGOPM	29	30	DG OPC marking layer
DGLOM	29	31	DG marking layer for special logic operation
DIFRES	97	3	LVS mark layer for AA resistor extraction.
DIOMK1	131	161	STI bounded diode recognized layer
DIOMK2	131	162	Poly bounded diode recognized layer
LUAREA1	131	163	DRC marking layer for area IO latch up rule check
IOMK1	131	164	Marking layer for IO PAD for DRC use
RES2H	131	178	Resistor mark layer for DRC LU check

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Layer name	GDS No	Data Type	Description
RESH	131	179	DRC marking layer to identify resistor with resistance below 200ohm, but customer consider it is safe to break connectivity for latch up check.
DMCB1	127	4	Dummy cell boundary for type 1
DMCB2	127	5	Dummy cell boundary for type 2
DMC1	131	181	Dummy cell for type 1
DMC2	131	182	Dummy cell for type 2
DMC3	131	183	Dummy cell for type 3
DMC4	131	184	Dummy cell for type 4
DMC5	131	185	Dummy cell for type 5
DMC6	131	186	Dummy cell for type 6
DMC7	131	187	Dummy cell for type 7
DMC8	131	188	Dummy cell for type 8
DMC9	131	189	Dummy cell for type 9
DMC10	131	190	Dummy cell for type 10
DMC11	131	191	Dummy cell for type 11
DMC12	131	192	Dummy cell for type 12
DMC13	131	193	Dummy cell for type 13
DMC14	131	194	Dummy cell for type 14
DMC15	131	195	Dummy cell for type 15
DMC16	131	196	Dummy cell for type 16
DMC17	131	197	Dummy cell for type 17
DMC18	131	198	Dummy cell for type 18
DMC19	131	199	Dummy cell for type 19
DMC20	131	200	Dummy cell for type 20

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Layer name	GDS No	Data Type	Description
MFDMY	131	202	LVS mark layer for multiple MOS device
DNWTR	19	2	LVS mark layer for DNW MOS and parasitic diode extraction
DTDMY	191	3	Marker layer for different net AA
DUMBA	91	0	Block Layer for Dummy operation on AA
DUMBP	92	0	Block Layer for Dummy operation on GT
DUPMK1	89	156	Marking layer for DUP(pad with device underneath)
ESDIO1	133	0	Dummy layer for SMIC Internal ESD devices and protection circuits
ESDIO2	133	3	DRC marking layer for I/O ESD protection devices and circuits identification.
ESD5V	133	1	Cascaded ESD component identification mark layer
DBESD	133	10	Marking layer for drain ballasted ESD MOS
DBESD2	133	11	Marking layer for the identificationdrain of drain side of drain ballasted ESD MOS
ESDCLP	41	2	Placed over ESD RC-triggered power clamp structures connected to a power supply pad and used for checking
ESD1	41	0	ESD Implant layer
ESDMK1	89	151	ESD component identification mark layer
EXDFM	239	1	DFM erorrs waive
EXLFD	239	2	LFD errors waive
FINAA	13	20	Fin after Fin cut
MTFUSE	81	3	Marking layer for metal fuse function area
FUSEAD	81	4	Marking layer for fuse anode side
EFUSE	81	2	e fuse component mark layer
FUSEMK1	81	152	Marking layer for fuse bitcell
GTMK1	89	154	Marking layer of edge gate 1

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Layer name	GDS No	Data Type	Description
GTMK2	89	168	Marking layer of edge gate 2
GT_P96	89	194	Marking layer of 96nm poly pitch
HRBL	34	239	Marking layer for blocking poly resistor implant and poly N+ doping
GTOPM	30	30	GT OPC marking layer
INDR	212	1	LVS mark layer for inductor radius calculation
JVARDUM	183	0	Junction Varactor recognition for DRC/LVS
LOGO	26	0	LOGO;L mark area
M0_B1	59	13	Butted M0 marking layer type1
M0_B2	59	14	Butted M0 marking layer type2
M0TXT	59	250	M0 Text Layer
MARKF	190	0	Fuse area mark for Fuse DRC check
MARKG	189	0	Guard ring mark for DRC check
MARKS	189	151	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage
MOMDMY	211	1	MOM Dummy layer
MOMTEM	211	2	LVS mark layer for MOM terminal
MOMP1	211	3	MOM capacitor mesh terminal one
MOMP2	211	4	MOM capacitor mesh terminal one
MOMMES	211	5	MOM capacitor mesh LVS marking layer
MOMCOL	211	7	LVS marker layer for MOM
MOMROW	211	8	LVS marker layer for MOM
MOMMK1	211	11	Marking layer for M1 MOM
MOMMK2	211	12	Marking layer for M2 MOM
MOMMK3	211	13	Marking layer for M3 MOM

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Layer name	GDS No	Data Type	Description
MOMMK4	211	14	Marking layer for M4 MOM
MOMMK5	211	15	Marking layer for M5 MOM
MOMMK6	211	16	Marking layer for M6MOM
MOMMK7	211	17	Marking layer for M7 MOM
MOMNW	211	34	LVS mark layer for N-well MOM shielding
MOMPW	211	35	LVS mark layer for P-well MOM shielding
MOMSHD1	211	36	LVS mark layer for MOM M1 shielding
MOMSHD2	211	37	LVS mark layer for MOM M2 shielding
MOMSHD3	211	38	LVS mark layer for MOM M3 shielding
MOMSHD4	211	39	LVS mark layer for MOM M4 shielding
MOMSHD5	211	40	LVS mark layer for MOM M5 shielding
MOMSHD6	211	41	LVS mark layer for MOM M6 shielding
MOMSHD7	211	42	LVS mark layer for MOM M7 shielding
MOMM1	211	53	MOM capacitor mesh minus one
MOMM2	211	54	MOM capacitor mesh minus two
OCCD	91	4	On chip CD mark layer
OCCDFH	91	6	Marker layer of FEOL OCCD
OCCDB	91	10	Marker layer of BEOL OCCD
OCCDM1	91	11	Marker layer of BEOL M1 OCCD cell
OCCDM2	91	12	Marker layer of BEOL M2 OCCD cell
OCCDM3	91	13	Marker layer of BEOL M3 OCCD cell
OCCDM4	91	14	Marker layer of BEOL M4 OCCD cell
OCCDM5	91	15	Marker layer of BEOL M5 OCCD cell
OCCDM6	91	16	Marker layer of BEOL M6OCCD cell

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Layer name	GDS No	Data Type	Description
OCCDM7	91	17	Marker layer of BEOL M7 OCCD cell
OCCDM8	91	18	Marker layer of BEOL M8 OCCD cell
OCCDB1	91	21	Marker layer of BEOL 2xB1 OCCD cell
OCCDB2	91	22	Marker layer of BEOL 2xB2 OCCD cell
OCOVL	91	5	On chip overlay mark layer
OCOVLAR	91	31	Mark layer for AR-to-PPAA OCOVL
OCOVLARH	91	32	Mark layer for ARH-to-PPAA OCOVL
OCOVLARV	91	33	Mark layer for ARV-to-PPAA OCOVL
OCOVLGT1	91	34	Mark layer for GT-to-PPAA OCOVL
OCOVLGT2	91	35	Mark layer for GT-to-AR OCOVL
OCOVLP2A	91	36	Mark layer for P2-to-PPAA OCOVL
OCOVLP2B	91	37	Mark layer for P2-to-GT OCOVL
OCOVLM0C	91	38	Mark layer for M0C-to-GT OCOVL
OCOVLM0	91	39	Mark layer for M0-to-GT OCOVL
OCOVLM0G1	91	40	Mark layer for M0G-to-GT OCOVL
OCOVLM0G2	91	41	Mark layer for M0G-to-M0C OCOVL
OCOVLM1CA	91	44	Mark layer for M1-to-M0 OCOVL
OCOVLM1CB	91	45	Mark layer for M1CB-to-M1CA OCOVL
OCOVLM2CA	91	46	Mark layer for M2-to-M1 OCOVL
OCOVLM4	91	47	Mark layer for M4-to-M3 OCOVL
OCOVLV0	91	48	Mark layer for V0-to-M1 OCOVL
MOSCKT	131	2	LVS dummy layer to distinguish bsim mos and subckt mos
NCAP	93	1	Mark layer for NFET in n-well capacitors
NFDMK	131	5	LVS marking layer for mos multiple fingers

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Layer name	GDS No	Data Type	Description
NLLLOM	35	10	NLL marking layer for special logic operation
NODMF	180	0	Area not to add AA/GT/Metal dummies
NSRLOM	5	10	NSR marking layer for special logic operation
PCAP	93	2	Mark layer for PFET in p-well capacitors
P4OPM	33	30	P4 OPC marking layer
P4LOM	33	31	P4 marking layer for special logic operation
PLDMK	131	4	LVS marking layer for device dummy poly
POWRING	133	2	DRC dummy layer for power ring identification
PWMK1	89	165	Marking layer for EDA modeling
RESCKT	131	3	LVS dummy layer for subckt resistor
RESP3T	96	1	LVS Dummy layer for Poly-1 Resistor with 3 terminal
RF3T	183	2	DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM
RFDN6T	181	4	6-terminal RF MOS in deep NWELL for LVS, the sixth terminal is psub.
RFMK1	181	6	Marking layer for RF device
RFDN5T	181	7	5T RF mark layer for 5T MOS
RFMOM	211	6	LVS mark layer for RF MOM
RFMOSD	182	0	DRC/LVS mark layer for RF mos drain terminal
RFSD	181	3	RF MOS of even finger with S/D permute for LVS
PLLLOM	38	10	PLL marking layer for special logic operation
PPAALOM	13	10	PPAA marking layer for special logic operation
PPAADB	13	60	Pre Fin PPAA reserve, auto PPAA blockage
PSRLOM	6	10	PSR marking layer for special logic operation
SDOP	99	0	SRAM pass gate mark layer

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Layer name	GDS No	Data Type	Description
SNLOM	40	10	SN markinglayer for special logic operation
SPLOM	43	10	SP markinglayer for special logic operation
SUBD	131	1	Substrate Dummy Layer
VARJUN	94	0	LVS mark Layer to cover all Junction type varactor
VSIA	63	63	VSIA tagging layer(Text Only)
M0OPM	59	30	M0 OPC marking layer
M0LOM	59	31	M0 marking layer for special logic operation
M0COPM	246	30	M0C OPC marking layer
M0CLOM	246	31	M0C marking layer for special logic operation
M0GOPM	208	30	M0G OPC marking layer
M0GLOM	208	31	M0G marking layer for special logic operation
M1CAOPRT	61	111	M1CA retargeting marker layer
M1CBOPRT	61	121	M1CB retargeting marker layer
M1_0V	61	200	DRC and LVS marking layer for 0.0V M1
M1_0d1V	61	201	DRC and LVS marking layer for 0.1V M1
M1_0d2V	61	202	DRC and LVS marking layer for 0.2V M1
M1_0d3V	61	203	DRC and LVS marking layer for 0.3V M1
M1_0d4V	61	204	DRC and LVS marking layer for 0.4V M1
M1_0d5V	61	205	DRC and LVS marking layer for 0.5V M1
M1_0d6V	61	206	DRC and LVS marking layer for 0.6V M1
M1_0d7V	61	207	DRC and LVS marking layer for 0.7V M1
M1_0d8V	61	208	DRC and LVS marking layer for 0.8V M1
M1_0d9V	61	209	DRC and LVS marking layer for 0.9V M1
M1_1d0V	61	210	DRC and LVS marking layer for 1.0V M1

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Layer name	GDS No	Data Type	Description
M1_1d1V	61	211	DRC and LVS marking layer for 1.1V M1
M1V12	89	16	DRC and LVS marking layer for 1.2V M1
M1_1d3V	61	213	DRC and LVS marking layer for 1.3V M1
M1_1d4V	61	214	DRC and LVS marking layer for 1.4V M1
M1V15	89	17	DRC and LVS marking layer for 1.5V M1
M1_1d6V	61	216	DRC and LVS marking layer for 1.6V M1
M1_1d7V	61	217	DRC and LVS marking layer for 1.7V M1
M1V18	89	11	DRC and LVS marking layer for 1.8V M1
M1V25	89	12	DRC and LVS marking layer for 2.5V M1
M1V33	89	13	DRC and LVS marking layer for 3.3V M1
M1V50	89	15	DRC and LVS marking layer for 5V M1
M1V70	61	228	DRC and LVS marking layer for 7V M1
M1_V_Hi	61	230	DRC and LVS marking layer for Highest voltage M1
M1_V_Lo	61	231	DRC and LVS marking layer for Lowest voltage M1
M1_V_Hi_TOP	61	232	M1 high voltage top text layer
M1_V_Lo_TOP	61	233	M1 low voltage top text layer
M1_SYNC	61	234	M1 voltage sync mark layer
M2CAOPRT	62	111	M2CA retargeting marker layer
M2CBOPRT	62	121	M2CB retargeting marker layer
M2_0V	62	200	DRC and LVS marking layer for 0.0V M2
M2_0d1V	62	201	DRC and LVS marking layer for 0.1V M2
M2_0d2V	62	202	DRC and LVS marking layer for 0.2V M2
M2_0d3V	62	203	DRC and LVS marking layer for 0.3V M2
M2_0d4V	62	204	DRC and LVS marking layer for 0.4V M2

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Layer name	GDS No	Data Type	Description
M2_0d5V	62	205	DRC and LVS marking layer for 0.5V M2
M2_0d6V	62	206	DRC and LVS marking layer for 0.6V M2
M2_0d7V	62	207	DRC and LVS marking layer for 0.7V M2
M2_0d8V	62	208	DRC and LVS marking layer for 0.8V M2
M2_0d9V	62	209	DRC and LVS marking layer for 0.9V M2
M2_1d0V	62	210	DRC and LVS marking layer for 1.0V M2
M2_1d1V	62	211	DRC and LVS marking layer for 1.1V M2
M2V12	89	26	DRC and LVS marking layer for 1.2V M2
M2_1d3V	62	213	DRC and LVS marking layer for 1.3V M2
M2_1d4V	62	214	DRC and LVS marking layer for 1.4V M2
M2V15	89	27	DRC and LVS marking layer for 1.5V M2
M2_1d6V	62	216	DRC and LVS marking layer for 1.6V M2
M2_1d7V	62	217	DRC and LVS marking layer for 1.7V M2
M2V18	89	21	DRC and LVS marking layer for 1.8V M2
M2V25	89	22	DRC and LVS marking layer for 2.5V M2
M2V33	89	23	DRC and LVS marking layer for 3.3V M2
M2V50	89	25	DRC and LVS marking layer for 5V M2
M2V70	62	228	DRC and LVS marking layer for 7V M2
M2_V_Hi	62	230	DRC and LVS marking layer for Highest voltage M2
M2_V_Lo	62	231	DRC and LVS marking layer for Lowest voltage M2
M2_V_Hi_TOP	62	232	M2 high voltage top text layer
M2_V_Lo_TOP	62	233	M2 low voltage top text layer
M2_SYNC	62	234	M2 voltage sync mark layer
M3CAOPRT	63	111	M3CA retargeting marker layer

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Layer name	GDS No	Data Type	Description
M3CBOPRT	63	121	M3CB retargeting marker layer
M3_0V	63	200	DRC and LVS marking layer for 0.0V M3
M3_0d1V	63	201	DRC and LVS marking layer for 0.1V M3
M3_0d2V	63	202	DRC and LVS marking layer for 0.2V M3
M3_0d3V	63	203	DRC and LVS marking layer for 0.3V M3
M3_0d4V	63	204	DRC and LVS marking layer for 0.4V M3
M3_0d5V	63	205	DRC and LVS marking layer for 0.5V M3
M3_0d6V	63	206	DRC and LVS marking layer for 0.6V M3
M3_0d7V	63	207	DRC and LVS marking layer for 0.7V M3
M3_0d8V	63	208	DRC and LVS marking layer for 0.8V M3
M3_0d9V	63	209	DRC and LVS marking layer for 0.9V M3
M3_1d0V	63	210	DRC and LVS marking layer for 1.0V M3
M3_1d1V	63	211	DRC and LVS marking layer for 1.1V M3
M3V12	89	36	DRC and LVS marking layer for 1.2V M3
M3_1d3V	63	213	DRC and LVS marking layer for 1.3V M3
M3_1d4V	63	214	DRC and LVS marking layer for 1.4V M3
M3V15	89	37	DRC and LVS marking layer for 1.5V M3
M3_1d6V	63	216	DRC and LVS marking layer for 1.6V M3
M3_1d7V	63	217	DRC and LVS marking layer for 1.7V M3
M3V18	89	31	DRC and LVS marking layer for 1.8V M3
M3V25	89	32	DRC and LVS marking layer for 2.5V M3
M3V33	89	33	DRC and LVS marking layer for 3.3V M3
M3V50	89	35	DRC and LVS marking layer for 5V M3
M3V70	63	228	DRC and LVS marking layer for 7V M3

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Layer name	GDS No	Data Type	Description
M3_V_Hi	63	230	DRC and LVS marking layer for Highest voltage M3
M3_V_Lo	63	231	DRC and LVS marking layer for Lowest voltage M3
M3_V_Hi_TOP	63	232	M3 high voltage top text layer
M3_V_Lo_TOP	63	233	M3 low voltage top text layer
M3_SYNC	63	234	M3 voltage sync mark layer
M4CAOPRT	64	111	M4CA retargeting marker layer
M4CBOPRT	64	121	M4CB retargeting marker layer
M4_0V	64	200	DRC and LVS marking layer for 0.0V M4
M4_0d1V	64	201	DRC and LVS marking layer for 0.1V M4
M4_0d2V	64	202	DRC and LVS marking layer for 0.2V M4
M4_0d3V	64	203	DRC and LVS marking layer for 0.3V M4
M4_0d4V	64	204	DRC and LVS marking layer for 0.4V M4
M4_0d5V	64	205	DRC and LVS marking layer for 0.5V M4
M4_0d6V	64	206	DRC and LVS marking layer for 0.6V M4
M4_0d7V	64	207	DRC and LVS marking layer for 0.7V M4
M4_0d8V	64	208	DRC and LVS marking layer for 0.8V M4
M4_0d9V	64	209	DRC and LVS marking layer for 0.9V M4
M4_1d0V	64	210	DRC and LVS marking layer for 1.0V M4
M4_1d1V	64	211	DRC and LVS marking layer for 1.1V M4
M4V12	89	46	DRC and LVS marking layer for 1.2V M4
M4_1d3V	64	213	DRC and LVS marking layer for 1.3V M4
M4_1d4V	64	214	DRC and LVS marking layer for 1.4V M4
M4V15	89	47	DRC and LVS marking layer for 1.5V M4
M4_1d6V	64	216	DRC and LVS marking layer for 1.6V M4

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Layer name	GDS No	Data Type	Description
M4_1d7V	64	217	DRC and LVS marking layer for 1.7V M4
M4V18	89	41	DRC and LVS marking layer for 1.8V M4
M4V25	89	42	DRC and LVS marking layer for 2.5V M4
M4V33	89	43	DRC and LVS marking layer for 3.3V M4
M4V50	89	45	DRC and LVS marking layer for 5V M4
M4V70	64	228	DRC and LVS marking layer for 7V M4
M4_V_Hi	64	230	DRC and LVS marking layer for Highest voltage M4
M4_V_Lo	64	231	DRC and LVS marking layer for Lowest voltage M4
M4_V_Hi_TOP	64	232	M4 high voltage top text layer
M4_V_Lo_TOP	64	233	M4 low voltage top text layer
M4_SYNC	64	234	M4 voltage sync mark layer
M5_0V	65	200	DRC and LVS marking layer for 0.0V M5
M5_0d1V	65	201	DRC and LVS marking layer for 0.1V M5
M5_0d2V	65	202	DRC and LVS marking layer for 0.2V M5
M5_0d3V	65	203	DRC and LVS marking layer for 0.3V M5
M5_0d4V	65	204	DRC and LVS marking layer for 0.4V M5
M5_0d5V	65	205	DRC and LVS marking layer for 0.5V M5
M5_0d6V	65	206	DRC and LVS marking layer for 0.6V M5
M5_0d7V	65	207	DRC and LVS marking layer for 0.7V M5
M5_0d8V	65	208	DRC and LVS marking layer for 0.8V M5
M5_0d9V	65	209	DRC and LVS marking layer for 0.9V M5
M5_1d0V	65	210	DRC and LVS marking layer for 1.0V M5
M5_1d1V	65	211	DRC and LVS marking layer for 1.1V M5
M5V12	89	56	DRC and LVS marking layer for 1.2V M5

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Layer name	GDS No	Data Type	Description
M5_1d3V	65	213	DRC and LVS marking layer for 1.3V M5
M5_1d4V	65	214	DRC and LVS marking layer for 1.4V M5
M5V15	89	57	DRC and LVS marking layer for 1.5V M5
M5_1d6V	65	216	DRC and LVS marking layer for 1.6V M5
M5_1d7V	65	217	DRC and LVS marking layer for 1.7V M5
M5V18	89	51	DRC and LVS marking layer for 1.8V M5
M5V25	89	52	DRC and LVS marking layer for 2.5V M5
M5V33	89	53	DRC and LVS marking layer for 3.3V M5
M5V50	89	55	DRC and LVS marking layer for 5V M5
M5V70	65	228	DRC and LVS marking layer for 7V M5
M5_V_Hi	65	230	DRC and LVS marking layer for Highest voltage M5
M5_V_Lo	65	231	DRC and LVS marking layer for Lowest voltage M5
M5_V_Hi_TOP	65	232	M5 high voltage top text layer
M5_V_Lo_TOP	65	233	M5 low voltage top text layer
M5_SYNC	65	234	M5 voltage sync mark layer
M6_0V	66	200	DRC and LVS marking layer for 0.0V M6
M6_0d1V	66	201	DRC and LVS marking layer for 0.1V M6
M6_0d2V	66	202	DRC and LVS marking layer for 0.2V M6
M6_0d3V	66	203	DRC and LVS marking layer for 0.3V M6
M6_0d4V	66	204	DRC and LVS marking layer for 0.4V M6
M6_0d5V	66	205	DRC and LVS marking layer for 0.5V M6
M6_0d6V	66	206	DRC and LVS marking layer for 0.6V M6
M6_0d7V	66	207	DRC and LVS marking layer for 0.7V M6
M6_0d8V	66	208	DRC and LVS marking layer for 0.8V M6

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Layer name	GDS No	Data Type	Description
M6_0d9V	66	209	DRC and LVS marking layer for 0.9V M6
M6_1d0V	66	210	DRC and LVS marking layer for 1.0V M6
M6_1d1V	66	211	DRC and LVS marking layer for 1.1V M6
M6V12	89	66	DRC and LVS marking layer for 1.2V M6
M6_1d3V	66	213	DRC and LVS marking layer for 1.3V M6
M6_1d4V	66	214	DRC and LVS marking layer for 1.4V M6
M6V15	89	67	DRC and LVS marking layer for 1.5V M6
M6_1d6V	66	216	DRC and LVS marking layer for 1.6V M6
M6_1d7V	66	217	DRC and LVS marking layer for 1.7V M6
M6V18	89	61	DRC and LVS marking layer for 1.8V M6
M6V25	89	62	DRC and LVS marking layer for 2.5V M6
M6V33	89	63	DRC and LVS marking layer for 3.3V M6
M6V50	89	65	DRC and LVS marking layer for 5V M6
M6V70	66	228	DRC and LVS marking layer for 7V M6
M6_V_Hi	66	230	DRC and LVS marking layer for Highest voltage M6
M6_V_Lo	66	231	DRC and LVS marking layer for Lowest voltage M6
M6_V_Hi_TOP	66	232	M6 high voltage top text layer
M6_V_Lo_TOP	66	233	M6 low voltage top text layer
M6_SYNC	66	234	M6 voltage sync mark layer
M7_0V	67	200	DRC and LVS marking layer for 0.0V M7
M7_0d1V	67	201	DRC and LVS marking layer for 0.1V M7
M7_0d2V	67	202	DRC and LVS marking layer for 0.2V M7
M7_0d3V	67	203	DRC and LVS marking layer for 0.3V M7
M7_0d4V	67	204	DRC and LVS marking layer for 0.4V M7

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Layer name	GDS No	Data Type	Description
M7_0d5V	67	205	DRC and LVS marking layer for 0.5V M7
M7_0d6V	67	206	DRC and LVS marking layer for 0.6V M7
M7_0d7V	67	207	DRC and LVS marking layer for 0.7V M7
M7_0d8V	67	208	DRC and LVS marking layer for 0.8V M7
M7_0d9V	67	209	DRC and LVS marking layer for 0.9V M7
M7_1d0V	67	210	DRC and LVS marking layer for 1.0V M7
M7_1d1V	67	211	DRC and LVS marking layer for 1.1V M7
M7V12	89	76	DRC and LVS marking layer for 1.2V M7
M7_1d3V	67	213	DRC and LVS marking layer for 1.3V M7
M7_1d4V	67	214	DRC and LVS marking layer for 1.4V M7
M7V15	89	77	DRC and LVS marking layer for 1.5V M7
M7_1d6V	67	216	DRC and LVS marking layer for 1.6V M7
M7_1d7V	67	217	DRC and LVS marking layer for 1.7V M7
M7V18	89	71	DRC and LVS marking layer for 1.8V M7
M7V25	89	72	DRC and LVS marking layer for 2.5V M7
M7V33	89	73	DRC and LVS marking layer for 3.3V M7
M7V50	89	75	DRC and LVS marking layer for 5V M7
M7V70	67	228	DRC and LVS marking layer for 7V M7
M7_V_Hi	67	230	DRC and LVS marking layer for Highest voltage M7
M7_V_Lo	67	231	DRC and LVS marking layer for Lowest voltage M7
M7_V_Hi_TOP	67	232	M7 high voltage top text layer
M7_V_Lo_TOP	67	233	M7 low voltage top text layer
M7_SYNC	67	234	M7 voltage sync mark layer
M8_0V	68	200	DRC and LVS marking layer for 0.0V M8

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Layer name	GDS No	Data Type	Description
M8_0d1V	68	201	DRC and LVS marking layer for 0.1V M8
M8_0d2V	68	202	DRC and LVS marking layer for 0.2V M8
M8_0d3V	68	203	DRC and LVS marking layer for 0.3V M8
M8_0d4V	68	204	DRC and LVS marking layer for 0.4V M8
M8_0d5V	68	205	DRC and LVS marking layer for 0.5V M8
M8_0d6V	68	206	DRC and LVS marking layer for 0.6V M8
M8_0d7V	68	207	DRC and LVS marking layer for 0.7V M8
M8_0d8V	68	208	DRC and LVS marking layer for 0.8V M8
M8_0d9V	68	209	DRC and LVS marking layer for 0.9V M8
M8_1d0V	68	210	DRC and LVS marking layer for 1.0V M8
M8_1d1V	68	211	DRC and LVS marking layer for 1.1V M8
M8V12	89	86	DRC and LVS marking layer for 1.2V M8
M8_1d3V	68	213	DRC and LVS marking layer for 1.3V M8
M8_1d4V	68	214	DRC and LVS marking layer for 1.4V M8
M8V15	89	87	DRC and LVS marking layer for 1.5V M8
M8_1d6V	68	216	DRC and LVS marking layer for 1.6V M8
M8_1d7V	68	217	DRC and LVS marking layer for 1.7V M8
M8V18	89	81	DRC and LVS marking layer for 1.8V M8
M8V25	89	82	DRC and LVS marking layer for 2.5V M8
M8V33	89	83	DRC and LVS marking layer for 3.3V M8
M8V50	89	85	DRC and LVS marking layer for 5V M8
M8V70	68	228	DRC and LVS marking layer for 7V M8
M8_V_Hi	68	230	DRC and LVS marking layer for Highest voltage M8
M8_V_Lo	68	231	DRC and LVS marking layer for Lowest voltage M8

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Layer name	GDS No	Data Type	Description
M8_V_Hi_TOP	68	232	M8 high voltage top text layer
M8_V_Lo_TOP	68	233	M8 low voltage top text layer
M8_SYNC	68	234	M8 voltage sync mark layer
B1_0d0V	141	200	DRC and LVS marking layer for 0.0V B1
B1_0d1V	141	201	DRC and LVS marking layer for 0.1V B1
B1_0d2V	141	202	DRC and LVS marking layer for 0.2V B1
B1_0d3V	141	203	DRC and LVS marking layer for 0.3V B1
B1_0d4V	141	204	DRC and LVS marking layer for 0.4V B1
B1_0d5V	141	205	DRC and LVS marking layer for 0.5V B1
B1_0d6V	141	206	DRC and LVS marking layer for 0.6V B1
B1_0d7V	141	207	DRC and LVS marking layer for 0.7V B1
B1_0d8V	141	208	DRC and LVS marking layer for 0.8V B1
B1_0d9V	141	209	DRC and LVS marking layer for 0.9V B1
B1_1d0V	141	210	DRC and LVS marking layer for 1.0V B1
B1_1d1V	141	211	DRC and LVS marking layer for 1.1V B1
B1_1d3V	141	213	DRC and LVS marking layer for 1.3V B1
B1_1d4V	141	214	DRC and LVS marking layer for 1.4V B1
B1_1d6V	141	216	DRC and LVS marking layer for 1.6V B1
B1_1d7V	141	217	DRC and LVS marking layer for 1.7V B1
B1V18	89	91	DRC and LVS marking layer for 1.8V B1
B1V25	89	92	DRC and LVS marking layer for 2.5V B1
B1V33	89	93	DRC and LVS marking layer for 3.3V B1
B1V42	89	94	DRC and LVS marking layer for 4.2V B1
B1V50	89	95	DRC and LVS marking layer for 5V B1

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Layer name	GDS No	Data Type	Description
B1V12	89	96	DRC and LVS marking layer for 1.2V B1
B1V15	89	97	DRC and LVS marking layer for 1.5V B1
B1V70	141	228	DRC and LVS marking layer for 7V B1
B1_V_Hi	141	230	DRC and LVS marking layer for Highest voltage B1
B1_V_Lo	141	231	DRC and LVS marking layer for Lowest voltage B1
B1_V_Hi_TOP	141	232	B1 high voltage top text layer
B1_V_Lo_TOP	141	233	B1 low voltage top text layer
B1_SYNC	141	234	B1 voltage sync mark layer
B2_0d0V	142	200	DRC and LVS marking layer for 0.0V B2
B2_0d1V	142	201	DRC and LVS marking layer for 0.1V B2
B2_0d2V	142	202	DRC and LVS marking layer for 0.2V B2
B2_0d3V	142	203	DRC and LVS marking layer for 0.3V B2
B2_0d4V	142	204	DRC and LVS marking layer for 0.4V B2
B2_0d5V	142	205	DRC and LVS marking layer for 0.5V B2
B2_0d6V	142	206	DRC and LVS marking layer for 0.6V B2
B2_0d7V	142	207	DRC and LVS marking layer for 0.7V B2
B2_0d8V	142	208	DRC and LVS marking layer for 0.8V B2
B2_0d9V	142	209	DRC and LVS marking layer for 0.9V B2
B2_1d0V	142	210	DRC and LVS marking layer for 1.0V B2
B2_1d1V	142	211	DRC and LVS marking layer for 1.1V B2
B2_1d3V	142	213	DRC and LVS marking layer for 1.3V B2
B2_1d4V	142	214	DRC and LVS marking layer for 1.4V B2
B2_1d6V	142	216	DRC and LVS marking layer for 1.6V B2
B2_1d7V	142	217	DRC and LVS marking layer for 1.7V B2

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Layer name	GDS No	Data Type	Description
B2V18	89	101	DRC and LVS marking layer for 1.8V B2
B2V25	89	102	DRC and LVS marking layer for 2.5V B2
B2V33	89	103	DRC and LVS marking layer for 3.3V B2
B2V42	89	104	DRC and LVS marking layer for 4.2V B2
B2V50	89	105	DRC and LVS marking layer for 5V B2
B2V12	89	106	DRC and LVS marking layer for 1.2V B2
B2V15	89	107	DRC and LVS marking layer for 1.5V B2
B2V70	142	228	DRC and LVS marking layer for 7V B2
B2_V_Hi	142	230	DRC and LVS marking layer for Highest voltage B2
B2_V_Lo	142	231	DRC and LVS marking layer for Lowest voltage B2
B2_V_Hi_TOP	142	232	B2 high voltage top text layer
B2_V_Lo_TOP	142	233	B2 low voltage top text layer
B2_SYNC	142	234	B2 voltage sync mark layer
BTXT	88	0	Text for Block
CTXT	89	0	Text for Cell
DIFTXT	163	0	Diffusion Pin Text Layer
POLYTXT	164	0	Poly Pin Text Layer
SUBTXT	161	0	Substrate Pin Text Layer
TTXT	87	0	Text for Top Structure
WELTXT	162	0	Wells Pin Text Layer
M1TXT	61	250	Metal-1 Text Layer
M2TXT	62	250	Metal-2 Text Layer
M3TXT	63	250	Metal-3 Text Layer
M4TXT	64	250	Metal-4 Text Layer

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Layer name	GDS No	Data Type	Description
M5TXT	65	250	Metal-5 Text Layer
M6TXT	66	250	Metal-6 Text Layer
M7TXT	67	250	Metal-7 Text Layer
M8TXT	68	250	Metal-8 Text Layer
B1TXT	141	250	2xmetal 1 text Layer, label text
B2TXT	142	250	2xmetal 2 text Layer, label text
TM1_0V	120	200	DRC and LVS marking layer for 0.0V TM1
TM1_0d1V	120	201	DRC and LVS marking layer for 0.1V TM1
TM1_0d2V	120	202	DRC and LVS marking layer for 0.2V TM1
TM1_0d3V	120	203	DRC and LVS marking layer for 0.3V TM1
TM1_0d4V	120	204	DRC and LVS marking layer for 0.4V TM1
TM1_0d5V	120	205	DRC and LVS marking layer for 0.5V TM1
TM1_0d6V	120	206	DRC and LVS marking layer for 0.6V TM1
TM1_0d7V	120	207	DRC and LVS marking layer for 0.7V TM1
TM1_0d8V	120	208	DRC and LVS marking layer for 0.8V TM1
TM1_0d9V	120	209	DRC and LVS marking layer for 0.9V TM1
TM1_1d0V	120	210	DRC and LVS marking layer for 1.0V TM1
TM1_1d1V	120	211	DRC and LVS marking layer for 1.1V TM1
TM1V12	120	212	DRC and LVS marking layer for 1.2V TM1
TM1_1d3V	120	213	DRC and LVS marking layer for 1.3V TM1
TM1_1d4V	120	214	DRC and LVS marking layer for 1.4V TM1
TM1V15	120	215	DRC and LVS marking layer for 1.5V TM1
TM1_1d6V	120	216	DRC and LVS marking layer for 1.6V TM1
TM1_1d7V	120	217	DRC and LVS marking layer for 1.7V TM1

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Layer name	GDS No	Data Type	Description
TM1V18	120	218	DRC and LVS marking layer for 1.8V TM1
TM1V25	120	225	DRC and LVS marking layer for 2.5V TM1
TM1V33	120	226	DRC and LVS marking layer for 3.3V TM1
TM1V50	120	227	DRC and LVS marking layer for 5V TM1
TM1V70	120	228	DRC and LVS marking layer for 7V TM1
TM1_V_Hi	120	230	DRC and LVS marking layer for Highest voltage TM1
TM1_V_Lo	120	231	DRC and LVS marking layer for Lowest voltage TM1
TM1_V_Hi_TOP	120	232	TM1 high voltage top text layer
TM1_V_Lo_TOP	120	233	TM1 low voltage top text layer
TM1_SYNC	120	234	TM1 voltage sync mark layer
TM2_0V	122	200	DRC and LVS marking layer for 0.0V TM2
TM2_0d1V	122	201	DRC and LVS marking layer for 0.1V TM2
TM2_0d2V	122	202	DRC and LVS marking layer for 0.2V TM2
TM2_0d3V	122	203	DRC and LVS marking layer for 0.3V TM2
TM2_0d4V	122	204	DRC and LVS marking layer for 0.4V TM2
TM2_0d5V	122	205	DRC and LVS marking layer for 0.5V TM2
TM2_0d6V	122	206	DRC and LVS marking layer for 0.6V TM2
TM2_0d7V	122	207	DRC and LVS marking layer for 0.7V TM2
TM2_0d8V	122	208	DRC and LVS marking layer for 0.8V TM2
TM2_0d9V	122	209	DRC and LVS marking layer for 0.9V TM2
TM2_1d0V	122	210	DRC and LVS marking layer for 1.0V TM2
TM2_1d1V	122	211	DRC and LVS marking layer for 1.1V TM2
TM2V12	122	212	DRC and LVS marking layer for 1.2V TM2
TM2_1d3V	122	213	DRC and LVS marking layer for 1.3V TM2

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Layer name	GDS No	Data Type	Description
TM2_1d4V	122	214	DRC and LVS marking layer for 1.4V TM2
TM2V15	122	215	DRC and LVS marking layer for 1.5V TM2
TM2_1d6V	122	216	DRC and LVS marking layer for 1.6V TM2
TM2_1d7V	122	217	DRC and LVS marking layer for 1.7V TM2
TM2V18	122	218	DRC and LVS marking layer for 1.8V TM2
TM2V25	122	225	DRC and LVS marking layer for 2.5V TM2
TM2V33	122	226	DRC and LVS marking layer for 3.3V TM2
TM2V50	122	227	DRC and LVS marking layer for 5V TM2
TM2V70	122	228	DRC and LVS marking layer for 7V TM2
TM2_V_Hi	122	230	DRC and LVS marking layer for Highest voltage TM2
TM2_V_Lo	122	231	DRC and LVS marking layer for Lowest voltage TM2
TM2_V_Hi_TOP	122	232	TM2 high voltage top text layer
TM2_V_Lo_TOP	122	233	TM2 low voltage top text layer
TM2_SYNC	122	234	TM2 voltage sync mark layer
ALPA_V_Hi_TO_P	83	232	ALPA high voltage top text layer
ALPA_V_Lo_TO_P	83	233	ALPA low voltage top text layer
ALPA_V_Hi	83	230	DRC and LVS marking layer for Highest voltage ALPA
ALPA_V_Lo	83	231	DRC and LVS marking layer for Lowest voltage ALPA
ALPA_SYNC	83	234	ALPA voltage sync mark layer
M0G_V_Hi	208	230	DRC and LVS marking layer for Highest voltage M0G
M0G_V_Lo	208	231	DRC and LVS marking layer for Lowest voltage M0G
M0_V_Hi	59	230	DRC and LVS marking layer for Highest voltage M0
M0_V_Lo	59	231	DRC and LVS marking layer for Lowest voltage M0

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Layer name	GDS No	Data Type	Description
AA_V_Hi	10	230	DRC and LVS marking layer for Highest voltage AA
AA_V_Lo	10	231	DRC and LVS marking layer for Lowest voltage AA
GT_V_Hi	30	230	DRC and LVS marking layer for Highest voltage GT
GT_V_Lo	30	231	DRC and LVS marking layer for Lowest voltage GT
TM1TXT	120	3	Top metal 1 Text Layer, label text
TM2TXT	122	3	Top metal 2 Text Layer, label text
UTMTXT	150	250	Ultra Thick Metal Text Layer
M1PIN	61	251	Metal-1 pin layer
M2PIN	62	251	Metal-2 pin layer
M3PIN	63	251	Metal-3 pin layer
M4PIN	64	251	Metal-4 pin layer
M5PIN	65	251	Metal-5 pin layer
M6PIN	66	251	Metal-6 pin layer
M7PIN	67	251	Metal-7 pin layer
M8PIN	68	251	Metal-8 pin layer
B1PIN	141	251	B1 pin layer
B2PIN	142	251	B2 pin layer
TM1PIN	120	251	TM-1 pin layer
TM2PIN	122	251	TM-2 pin layer
UTMPIN	150	251	UTM pin layer
M1NET	61	253	Metal-1 net layer, reserved for customer internal usage
M2NET	62	253	Metal-2 net layer, reserved for customer internal usage
M3NET	63	253	Metal-3 net layer, reserved for customer internal usage
M4NET	64	253	Metal-4 net layer, reserved for customer internal usage

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Layer name	GDS No	Data Type	Description
M5NET	65	253	Metal-5 net layer, reserved for customer internal usage
M6NET	66	253	Metal-6 net layer, reserved for customer internal usage
M7NET	67	253	Metal-7 net layer, reserved for customer internal usage
M8NET	68	253	Metal-8 net layer, reserved for customer internal usage
B1NET	141	253	B1 net layer, reserved for customer internal usage
B2NET	142	253	B2 net layer, reserved for customer internal usage
TM1NET	120	253	TM-1 net layer, reserved for customer internal usage
TM2NET	122	253	TM-2 net layer, reserved for customer internal usage
UTMNET	150	253	UTM net layer, reserved for customer internal usage
M1LABEL	61	254	Metal-1 label layer, reserved for customer internal usage
M2LABEL	62	254	Metal-2 label layer, reserved for customer internal usage
M3LABEL	63	254	Metal-3 label layer, reserved for customer internal usage
M4LABEL	64	254	Metal-4 label layer, reserved for customer internal usage
M5LABEL	65	254	Metal-5 label layer, reserved for customer internal usage
M6LABEL	66	254	Metal-6 label layer, reserved for customer internal usage
M7LABEL	67	254	Metal-7 label layer, reserved for customer internal usage
M8LABEL	68	254	Metal-8 label layer, reserved for customer internal usage
B1LABEL	141	254	B1 label layer, reserved for customer internal usage
B2LABEL	142	254	B2 label layer, reserved for customer internal usage
TM1LABEL	120	254	TM-1 label layer, reserved for customer internal usage
TM2LABEL	122	254	TM-2 label layer, reserved for customer internal usage
UTMLABEL	150	254	UTM label layer, reserved for customer internal usage
M1B	151	0	Metal-1 Blockage Layer(For Place & Route use)
M2B	152	0	Metal-2 Blockage Layer(For Place & Route use)

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Layer name	GDS No	Data Type	Description
M3B	153	0	Metal-3 Blockage Layer(For Place & Route use)
M4B	154	0	Metal-4 Blockage Layer(For Place & Route use)
M5B	155	0	Metal-5 Blockage Layer(For Place & Route use)
M6B	156	0	Metal-6 Blockage Layer(For Place & Route use)
M7B	157	0	Metal-7 Blockage Layer(For Place & Route use)
M8B	158	0	Metal-8 Blockage Layer(For Place & Route use)
B1B	181	150	B1 Blockage Layer(For Place & Route use)
B2B	181	151	B2 Blockage Layer(For Place & Route use)
TM1B	193	0	TM1 Blockage Layer(For Place & Route use)
TM2B	194	0	TM2 Blockage Layer(For Place & Route use)
UTMB	181	158	UTM Blockage Layer(For Place & Route use)
M0DUB	59	6	M0 Dummy Blockage (For dummy M0 insertion) and exclude dummy insertion
M0CDUB	246	6	M0C Dummy Blockage (For dummy metal insertion) and exclude dummy insertion
M0GDUB	208	6	M0G Dummy Blockage (For dummy M0G insertion) and exclude dummy insertion
P2DUB	31	6	P2 Dummy Blockage (For dummy metal insertion) and exclude dummy insertion
V0_B0	245	2	Butted V0 marking layer type1
V0DUB	245	6	Via-0 Dummy Blockage.
V0CAOPRT	245	111	V0CA retargeting marker layer
V0CBOPRT	245	121	V0CB retargeting marker layer
V1DUB	70	6	Via-1 Dummy Blockage.
V2DUB	71	6	Via-2 Dummy Blockage.
V3DUB	72	6	Via-3 Dummy Blockage.

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Layer name	GDS No	Data Type	Description
V4DUB	73	6	Via-4 Dummy Blockage.
V5DUB	74	6	Via-5 Dummy Blockage.
V6DUB	75	6	Via-6 Dummy Blockage.
V7DUB	76	6	Via-7 Dummy Blockage.
BV1DUB	135	6	2x Via dummy Blockage
BV2DUB	136	6	Second 2x Via dummy Blockage
M1DUB	151	1	Metal-1 Dummy Block layer for M1 dummy fill
M2DUB	152	1	Metal-2 Dummy Block layer for M2 dummy fill
M3DUB	153	1	Metal-3 Dummy Block layer for M3 dummy fill
M4DUB	154	1	Metal-4 Dummy Block layer for M4 dummy fill
M5DUB	155	1	Metal-5 Dummy Block layer for M5 dummy fill
M6DUB	156	1	Metal-6 Dummy Block layer for M6 dummy fill
M7DUB	157	1	Metal-7 Dummy Block layer for M7 dummy fill
M8DUB	158	1	Metal-8 Dummy Block layer for M8 dummy fill
B1DUB	141	6	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of B1FILL shapes.
B2DUB	142	6	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of B2FILL shapes.
TM1DUB	193	1	Top Metal 1 Dummy Block layer for TM1 dummy fill
TM2DUB	194	1	Top Metal 2 Dummy Block layer for TM2 dummy fill
UTMDUB	150	6	UTM Dummy Blockage (For dummy metal insertion) and exclude dummy insertion
MIMDUB	58	6	MIM Dummy Blockage layer for dummy insertion
CTOPDUB	222	6	CTOP Dummy Blockage layer for dummy insertion
M1R	181	161	Metal-1 Resistor

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Layer name	GDS No	Data Type	Description
M2R	181	162	Metal-2 Resistor
M3R	181	163	Metal-3 Resistor
M4R	181	164	Metal-4 Resistor
M5R	181	165	Metal-5 Resistor
M6R	181	166	Metal-6 Resistor
M7R	181	167	Metal-7 Resistor
M8R	181	168	Metal-8 Resistor
B1R	194	154	2xmetal 1 resistor layer
B2R	194	155	2xmetal 2 resistor layer
TM1R	201	0	TM1 resistor layer
TM2R	202	0	TM2 resistor layer
UTMR	194	157	UTM Resistor
INST	60	0	Marker shape of SRAM bitcell, edge cell, strap cell or Instance Outline
STSRAM	60	1	Marker shape of HDSP 6T type A SRAM cell (SPD0734)
DNSRAM	60	2	Marker shape of HCSP 6T SRAM cell (SPD0907)
UDSRAM	60	3	Marker shape to allow LVS to identity 14nm SPSRAM (SPD0691)
DPSRAM	60	4	Marker shape of HCDP 8T SRAM cell (DPD194)
LRSRAM	60	5	Marker shape of HPSP 6T SRAM cell (SPD108)
U2SRAM	60	10	Marker shape to allow LVS to identity 14nm SPSRAM (SPD0864)
D2SRAM	60	11	Marker shape to allow LVS to identity 14nm DPSRAM D194
SRAMR2	60	15	Marker shape to allow LVS to identity 14nm 2PSRAM D138 A-type
TRCMK	60	105	Marking layer for SRAM tracking cell

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Layer name	GDS No	Data Type	Description
6TMK	60	151	Marker shape of 6T in 8T or 10T SRAM cell (for 2PD138)
M0GTXT	208	61	M0G Text Layer
MIMCKT	131	6	LVS marker layer for subckt MIM
WTPMK	80	4	Marking layer for internal WAT test PAD

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### 7.1.9 Mask layer Mapping Table

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description
900	0M	C	Drawn	Zero Mask
292	DNW	C	Drawn	Deep N well
126	PPAA	D	Generated	Pre fin
127	NPAA	D	Generated	Planar AA reservation
121	AR	D	Drawn	Fin cut layer for SDB
190	CL(AR_H)	C	Drawn	Fin cut layer 1 AR_H
119	CPT(AR_V)	C	Drawn	Fin cut layer 2 AR_V
192	NW	C	Drawn	NW implant
191	PW	C	Generated	PW implant
491	PWH	C	Generated	IO PW 1.8V
595	LVP	C	Generated	LVT PMOS Vt and HVT PMOS Vt/ Varactor implant
596	LVN	C	Generated	LVT NMOS Vt and HVT NMOS Vt/ Varactor implant
130	GT	D	Drawn	GT
132	P2	C	Drawn	GT cut
114	NLH	C	Generated	NMOS LDD Implant for 1.8v device
201	PSR	C	Generated	eSiGe PFET Si recess
200	NSR	C	Generated	eSiC NFET Si recess
197	SP	C	Drawn	P+ S/D Implant
198	SN	C	Drawn	N+ S/D Implant
131	DG	D	Drawn	1.8V IO mark layer; DG mask
195	TP	C	Generated	Core SVT_P, HVT_P, IO PMOS, SRAM PU, DIOMK2 work function formation
196	TN	C	Generated	Core SVT_N, HVT_N, IO NMOS, SRAM PD/PG/readport , DIOMK2 work function formation
134	P4	C	Generated	LVT, ULVT and VARMOS NMOS work function formation
122	DIR	D	Drawn	HR mask
168	M0C	D	Drawn	M0 cut
161	M0	D	Drawn	Contact on AA
461	M0G	D	Drawn	Contact on GT
370	V0	D	Drawn	Via-0

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Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description
770	V0DP	D	Generated	Via-0 Double Patterning 2 <sup>nd</sup> Mask
160	M1	D	Drawn	Metal-1
760	M1DP	D	Generated	Metal-1 Double Patterning 2 <sup>nd</sup> Mask
178	V1	D	Drawn	Via-1
180	M2	D	Drawn	Metal-2
780	M2DP	D	Generated	Metal-2 Double Patterning 2 <sup>nd</sup> Mask
179	V2	D	Drawn	Via-2
181	M3	D	Drawn	Metal-3
781	M3DP	D	Generated	Metal-3 Double Patterning 2 <sup>nd</sup> Mask
177	V3	D	Drawn	Via-3
182	M4	C	Drawn	Metal-4
176	V4	D	Drawn	Via-4
183	M5	C	Drawn	Metal-5
175	V5	D	Drawn	Via-5
184	M6	C	Drawn	Metal-6
174	V6	D	Drawn	Via-6
185	M7	C	Drawn	Metal-7
173	V7	D	Drawn	Via-7
186	M8	C	Drawn	Metal-8
371	BV1	C	Drawn	First 2X Via Hole (Only for 20nm and advanced technology)
280	B1	C	Drawn	First-level 2x metal line in the ultralow-k dielectric # 2x Metal-1
372	BV2	C	Drawn	Second 2X Via Hole (Only for 20nm and advanced technology)
281	B2	C	Drawn	Second-level 2x metal line in the ultralow-k dielectric # 2x Metal-2
324	CTOP	D	Drawn	Top Plate of MIM Capacitor;Bottom Plate of MIM Capacitor for 32nm and below technology
162	MIM	D	Drawn	Top Plate of MIM Capacitor
142	TV1	C	Drawn	10x First Top Via Hole
141	TM1	C	Drawn	Top Metal 1
144	TV2	C	Drawn	10x Second Top Via Hole
143	TM2	C	Drawn	Top Metal 2

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Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description
342	UTV	C	Drawn	Ultra Thick Via
352	UTM	C	Drawn	Ultra Thick Metal
107	PA	C	Drawn	Passivation 1
108	ALPA	D	Drawn	AL Bonding Pad and RDL
163	MD	C	Drawn	Passivation 2 opening
106	FUSE	C	Drawn	Passivation opening for Al fuse window

Notes: Please refer DCC document PM-DATA-02-2001 layer mapping table 1



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### 7.1.10 Device Layout Truth Table

Table 1a:

Layer Name	Device type	Description	CELLB	GT	AA	DIR	DNW	NW	Psub	SP	SN	LVT_N	LVT_P	SVT_N	SVT_P	ULVT_N	ULVT_P	HVT_N	HVT_P	LFN_N	LFN_P	DGUD	DGV	RESP1	PLRES	RESNW	RESP3T	RESP2	DSTR
Layer No			2	127																									
Data type																													
Core	LVT_N	nlvt08_ckt	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		nlvt08_dnw_ckt	1	1	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	LVT_P	plvt08_ckt	1	1	1	0	*	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		n08_ckt	1	1	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	SVT_N	n08_dnw_ckt	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		n08_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	SVT_P	p08_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		nulvt08_ckt	1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	ULVT_N	nulvt08_dnw_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
		pulvt08_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	ULVT_P	nhvt08_ckt	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
		nhvt08_dnw_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	HVT_N	phvt08_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
		phvt08_dnw_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	HVT_P	pln08_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		nln08_ckt	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	LFN_N	nln08_dnw_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
		pln08_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
I/O 1.8V	N_IO18	n18_ckt	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
		n18_dnw_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	P_IO18	p18_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
		n18ud15_ckt	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

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Layer Name	Device type	Description	CELLB	CELLB	AA	GT	DIR	DNW	NW	Psub	SP	SN	LVT_N	LVT_P	SVT_N	SVT_P	ULVT_N	ULVT_P	HVT_N	HVT_P	LFN_N	LFN_P	DG	DGUD	DGV	RESP1	PLRES	RESPW	RESP3T	RESP2	DSTR		
Layer No			2	127																													
Data type																																	
		n18ud15_dnw_ckt	1	1	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	P_IO18UD15	p18ud15_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	N_IO18UD12	n18ud12_ckt	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	P_IO18UD12	n18ud12_dnw_ckt	1	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	P_IO18UD12	p18ud12_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
High Resistor	TiN resistor	rhrpo_2t_ckt	*	0	0	1	*	*	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	0	0	0	1	0
		rhrpo_3t_ckt	*	0	0	1	*	*	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	0	0	1	1	0	
NW resistor	Under STI	rnwsti_2t_ckt	1	0	*	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0		
		rnwsti_3t_ckt	1	0	*	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0		
BJT	NPN with Emitter 1.632*1.632um^2	Emitter	npn08a2p56_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Base		1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Collector		1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	NPN with Emitter 2.04*2.16um^2	Emitter	npn08a4_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Base		1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Collector		1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	PNP with Emitter 1.632*1.632um^2	Emitter	pnp08a2p56_ckt	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Base		1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Collector		1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	PNP with Emitter 2.04*2.16um^2	Emitter	pnp08a4_ckt	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Base		1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		Collector		1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	NPN with	Emitter	npn18a3_ckt	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

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Layer Name	Device type	Description	CELLB	CELLB	AA	GT	DIR	DNW	NW	Psub	SP	SN	LVT_N	LVT_P	SVT_N	SVT_P	ULVT_N	ULVT_P	HVT_N	HVT_P	LFN_N	LFN_P	DG	DGUD	DGV	RESP1	PLRES	RESPNW	RESP3T	RESP2	DSTR		
Layer No			2	127	0	10	0	30	0	119	0	0	158	159	157	159	167	159	159	159	160	159	170	159	0	1	0	0	0	0			
Data type																																	
Emitter 4.08*0.72um^2	Base		1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Collector		1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	NPN with Emitter 4.08*1.968um^2	Emitter	1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Base	npn18a8_ckt	1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Collector		1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	PNP with Emitter 4.08*0.72um^2	Emitter	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Base	pnp18a3_ckt	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Collector		1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	PNP with Emitter 4.08*1.968um^2	Emitter	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Base	pnp18a8_ckt	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Collector		1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Diode	core P+/NW	Diode	pdio08_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Pick up			1	1	1	0	*	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	core N+/PW	Diode	ndio08_ckt	1	1	1	0	*	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Pick up			1	1	1	0	*	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	NW/PSUB Diode	Diode	nwadio	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*	0	0	0	0	0	0
	Pick up			1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*	0	0	0	0	0	0
	IO18 P+/NW	Diode	pdio18_ckt	1	1	1	0	*	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Pick up			1	1	1	0	*	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	IO18 N+/PW	Diode	ndio18_ckt	1	1	1	0	*	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	*	0	0	0	0	0	0
	Pick up			1	1	1	0	*	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	*	0	0	0	0	0	0
	PW/DNW	Diode	rwdio	1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*	0	0	0	0	0	0

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TD-LO14-DR-2017		2	V1.0_REV1	80/610

Layer Name	Device type	Description	CELLB	2	127	AA	GT	DIR	DNW	NW	Psub	SP	SN	LVT_N	LVT_P	SVT_N	SVT_P	ULVT_N	ULVT_P	HVT_N	HVT_P	LFN_N	LFN_P	DG	DGUD	DGV	RESP1	PLRES	RESPNW	RESP3T	RESP2	DSTR							
Layer No					2	0	10	0	0	0	30	119	0	0	0	0	0	0	158	159	168	159	157	159	167	159	159	166	159	0	*	*	*	0	0	0	0	0	1
Data type																																							
	Diode	Pick up		1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1					
	DNW/PSUB Diode	Diode	dnwdio	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1					
	Pick up			1	1	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1						
MOS Varactor	Core N+/NW	pvar08_ckt		1	1	1	0	*	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	IO18 N+/NW	pvar18_ckt		1	1	1	0	*	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
Poly Bounded Diode	IO N	ngdio18_esd		1	1	1	0	*	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	IO P	pgdio18_esd		1	1	1	0	*	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
STI Bounded Diode	IO N-STI Diode	ndio18_esd		1	1	1	0	*	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	IO P-STI Diode	pdio18_esd		1	1	1	0	*	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
MOM	MOM	mom_2t/3t/4t/5t_1p25		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*						
MIM	MIM capacitor	mim_ckt		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*						
ESD	ESD IO device	n18_esd		1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
E fuse element				*	0	0	0	*	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
SRAM	HDSP D0734	PU	stpl_ckt	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
		PD	stnpl_ckt	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
		PG	stnpg_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	HCSP D0907	PU	dnnpl_ckt	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
		PD	dnnpd_ckt	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	HPSP D108	PG	dnnpg_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
		PU	lrpl_ckt	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	PD	lrnpd_ckt		0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						

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Layer Name	Device type	Description	CELLB	CELLB	AA	GT	DIR	DNW	NW	Psub	SP	SN	LVT_N	LVT_P	SVT_N	SVT_P	ULVT_N	ULVT_P	HVT_N	HVT_P	LFN_N	LFN_P	DG	DGUD	DGV	RESP1	PLRES	RESPNW	RESP3T	RESP2	DSTR	
Layer No			2	127																												
Data type																																
HCDP D194	PG	lrnpg_ckt	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	PU	dppl_ckt	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PD	dnpd_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PGA	dnpnga_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PGB	dnpngb_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TS SP D0691	PU	udpl_ckt	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PD	udnpd_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PG	udnpg_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TS SP D0864	PU	utpl_ckt	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PD	utnpd_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PG	utnpg_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TS 2P D138	PU	tppl_ckt	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PD	tppnd_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	PG	tppng_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RPD	tpnrd_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RPG	tpnrpg_ckt	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 1b:

Layer Name	Device type	Description	VARMOS	93	
Layer No	Data type		BIPOLA	159	
			DMPPNP	134	
core	LVT_N	nlvt08_ckt	0	0	0
		nlvt08_dnw_ckt	0	0	0
	LVT_P	plvt08_ckt	0	0	0
		n08_ckt	0	0	0
	SVT_N	n08_dnw_ckt	0	0	0
		p08_ckt	0	0	0
	SVT_P	nulvt08_ckt	0	0	0
		nulvt08_dnw_ckt	0	0	0
HVT_N	ULVT_N	pulvt08_ckt	0	0	0
		nhvt08_ckt	0	0	0
	ULVT_P	nhvt08_dnw_ckt	0	0	0

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Layer Name	Device type	Description	VARMOS	BIPOLA	DMPNP	DIOMK1	DIOMK2	MOMDMY	RFDEV	INDMY	EFUSE	MIFUSE	FUSEAD	SDOP	INST	STSRAM	DNSRAM	UDSRAM	DPSRAM	LRSRAM	U2SRAM	SRAMR2	MIM	CTOP	MIMDMY	ESDIO2	DBESD2	DBESD	ESDCLP
Layer No																													
Data type																													
	HVT_P	phvt08_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	LFN_N	nln08_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
		nln08_dnw_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	LFN_P	pln08_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	N_IO18	n18_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*		
		n18_dnw_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	P_IO18	p18_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	0	*	
	I/O 1.8V N_IO18UD15	n18ud15_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	0	0	
		n18ud15_dnw_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	0	0	
	P_IO18UD15	p18ud15_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	0	0	
	N_IO18UD12	n18ud12_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	0	0	
		n18ud12_dnw_ckt	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	0	0	

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TD-LO14-DR-2017		2	V1.0_REV1	84/610

Layer Name	Device type	Description	VARMOS	BIPOLA	DMPNP	DIOMK1	DIOMK2	MOMDMY	RFDEV	INDMY	EFUSE	MTFUSE	FUSEAD	SDOP	INST	STSRAM	DNSRAM	UDSRAM	DPSRAM	LRSRAM	U2SRAM	SRAMR2	MIM	CTOP	MIMDMY	ESDIO2	DBESD2	DBESD	ESDCLP	
Layer No			0 93	0 1 159	0 134	161 131	162 131	1 211	0 181	0 212	2 81	3 81	4 81	0 99	0 60	1 60	2 60	3 60	4 60	5 60	10 60	15 60	151 60	0 58	0 222	0 211	3 133	11 133	10 133	2 41
Data type																														
	P_IO18UD12	p18ud12_ckt	0 0 0 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
High Resistor	TiN resistor	rhrpo_2t_ckt	0 0 0 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
		rhrpo_3t_ckt	0 0 0 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
NW resistor	Under STI	rnwsti_2t_ckt	0 0 0 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
		rnwsti_3t_ckt	0 0 0 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
BJT	NPN with Emitter 1.632*1.632um^2	Emitter	npn08a2p56_ckt	0 1 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
		Base		0 0 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
		Collector		0 0 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
	NPN with Emitter 2.04*2.16um^2	Emitter	npn08a4_ckt	0 1 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
		Base		0 0 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
		Collector		0 0 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
	PNP with Emitter 1.632*1.632um^2	Emitter	pnp08a2p56_ckt	0 1 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		
		Base		0 0 1 0 0	* 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0		

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Layer Name	Device type	Description	VARMOS	BIPOLA	DMPNP	DIOMK1	DIOMK2	MOMDMY	RFDEV	INDMY	EFUSE	MIFUSE	FUSEAD	SDOP	INST	STSRAM	DNSRAM	UDSRAM	DPSRAM	LRSRAM	U2SRAM	SRAMR2	MIM	CTOP	MIMDMY	ESDIO2	DBESD2	DBESD	ESDCLP
Layer No																													
Data type																													
PNP with Emitter 2.04*2.16um^2	Collector	pnp08a4_ckt	0	0	1	0	0	*	0	0	0	2	81	0	99	0	0	0	0	0	0	0	0	0	0	0	0		
	Emitter		0	1	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Base		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Collector		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
NPN with Emitter 4.08*0.72um^2	Emitter	npn18a3_ckt	0	1	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Base		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Collector		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
NPN with Emitter 4.08*1.968um^2	Emitter	npn18a8_ckt	0	1	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Base		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Collector		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
PNP with Emitter 4.08*0.72 um^2	Emitter	pnp18a3_ckt	0	1	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Base		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Collector		0	0	1	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

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Layer Name	Device type	Description	VARMOS	BIPOLA	DMPNP	DIOMK1	DIOMK2	MOMDMY	RFDEV	INDMY	EFUSE	MTFUSE	FUSEAD	SDOP	INST	STSRAM	DNSRAM	UDSRAM	DPSRAM	LRSRAM	U2SRAM	SRAMR2	MIM	CTOP	MIMDMY	ESDIO2	DBESD2	DBESD	ESDCLP	
Layer No			0 93	1 159	0 134	161 131	162 131	1 211	0 181	0 212	2 81	3 81	4 81	0 99	0 60	1 60	2 60	3 60	4 60	5 60	10 60	15 60	151 60	0 58	0 222	0 211	3 133	11 133	10 133	2 41
Data type			0 1	1 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
PNP with Emitter 4.08*1.968 um^2	Emitter	pnp18a8_ckt	0 0	1 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
	Base		0 0	1 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
	Collector		0 0	1 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
Diode	core P+/NW	Diode	pdio08_ckt	0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
		Pick up		0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
Diode	core N+/PW	Diode	ndio08_ckt	0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
		Pick up		0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
Diode	NW/PSUB Diode	Diode	nwdio	0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
		Pick up		0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
Diode	IO18 P+/NW	Diode	pdio18_ckt	0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
		Pick up		0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
Diode	IO18 N+/PW	Diode	ndio18_ckt	0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	
		Pick up		0 0	0 0	0 0	0 0	*	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	*	*	0 0	0 0	0 0	0 0	

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Layer Name	Device type	Description	VARMOS	BIPOLA	DMPNP	DIOMK1	DIOMK2	MOMDMY	RFDEV	INDMY	EFUSE	MIFUSE	FUSEAD	SDOP	INST	STSRAM	DNSRAM	UDSRAM	DPSRAM	LRSRAM	U2SRAM	SRAMR2	MIM	CTOP	MIMDMY	ESDIO2	DBESD2	DBESD	ESDCLP
Layer No																													
Data type																													
PW/DNW Diode	Diode	rwdio	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Pick up		0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	DNW/PSUB Diode	Diode	dnwdio	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Pick up	0		0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
MOS Varactor	Core N+/NW	pvar08_ckt	1	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	IO18 N+/NW	pvar18_ckt	1	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Poly Bounded Diode	IO N	ngdio18_esd	0	0	0	0	1	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	1	0	0	
	IO P	pgdio18_esd	0	0	0	0	0	1	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	1	0	0	
STI Bounded Diode	IO N-STI Diode	ndio18_esd	0	0	0	1	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	
	IO P-STI Diode	pdio18_esd	0	0	0	1	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	
MOM	MOM	mom_2t/3t/4t/5t_1p25	*	*	*	*	*	1	*	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*	*	0	0
MIM	MIM capacitor	mim_ckt	*	*	*	*	*	*	*	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	*	*	0	0

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Layer Name	Device type	Description	VARMOS	BIPOLA	DMPNP	DIOMK1	DIOMK2	MOMDMY	RFDEV	INDMY	EFUSE	MIFUSE	FUSEAD	SDOP	INST	STSRAM	DNSRAM	UDSRAM	DPSRAM	LRSRAM	U2SRAM	SRAMR2	MIM	CTOP	MIMDMY	ESDIO2	DBESD2	DBESD	ESDCLP
Layer No																													
Data type																													
TS SP D0691	PGA	dpnpga_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	PGB	dpnpgb_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	PU	udpl_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0		
	PD	udnpd_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0		
	PG	udnpg_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0		
	PU	utpl_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0		
TS SP D0864	PD	utnpd_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0		
	PG	utnpg_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0		
	PU	tppl_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0		
TS 2PD138	PD	tpnpd_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0		
	PG	tpnpg_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0		
	RPD	tpnrpd_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0		
	RPG	tpnrg_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0		
	PU	tpnra_ckt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0		

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Symbol Note	1	must have
	0	no need
	*	optional, part of the component

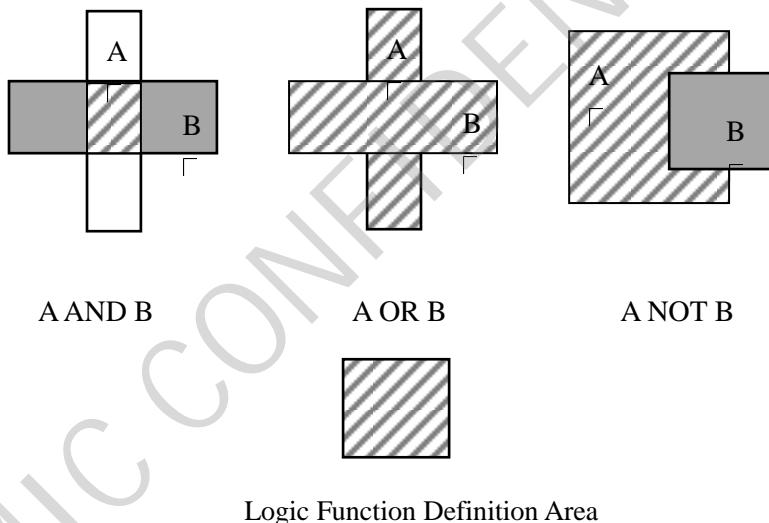
1. Following connection/cut layers are not shown in this table: P2,M0,M0C,M0G, metals, vias, passivations, Al layer
2. LDMOS indicate include channel and source drain parts
3. Diode do not indicate the pickup part, only “NW/PSUB” include the diode and pick up part. Other diodes only the center diode part.
4. BJT component here denotes emitter area layers.
5. RESP2 is used for the resistor outmost mark layer for logic operation related purpose
6. For ESD device,designer is required to use ESD IO NMOS.
7. E fuse and the progaming driver pack mark layer FUSEMK1 not shown in this table. This table only denote the fuse element part.
8. Some MOM may not RF related, and RFDEV maybe not marked in the component. If the MOM is 3 terminal, then RF3T may need to mark the MOM
9. ESDIO1, ESDIO2 are to distinguish SMIC and non-SMIC ESD components.

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### 7.1.11 Design Rules Nomenclatures and Abbreviations

#### (A) Logic Function Definition

Logic Function	Definition
A AND B	Define the intersection area of A and B.
A OR B	Define the union area of A and B.
A NOT B	Define the area of A excluding the common area of A and B.



#### (B) Nomenclatures and Abbreviations

Name	Definitions
PW	Any chip area NOT (NW OR PSUB).
GATE	(GT NOT GTMK1 ) AND (AA NOT AR)
Channel Length	The dimension (from GATE edge to GATE edge) over AA.
Channel Width	The dimension (from AA edge to AA edge) over GATE.
MOS AA	MOS AA refers to an AA that is part of a transistor active area. When a GT pattern is on top of an (AA NOT AR), the AA is treated as MOS AA. If there is no GT pattern on top of an (AA NOT AR), the AA is not a MOS AA. Dummy AA is not a MOS AA.
N+AA	((AA NOT AR) AND SN) NOT NW)

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Name	Definitions
P+AA	((AA NOT AR) AND SP) AND NW)
ACTIVE	(N+AA OR P+AA)
N+ pick-up AA	((AA NOT AR) AND SN) AND NW )
P+ pick-up AA	((AA NOT AR) AND SP) NOT NW)
Pick-up	(N+ pick-up AA) OR (P+ pick-up AA)
STI	NOT ((AA or AA dummy) NOT AR)
Dummy	If there is no special remark, dummy include all the design of data type 1 and 7 in general, and for double patterning process layer (layout need to do decomposition), the dummy include two mask all design of data type 1 and 7.
Different or same net	Electrically based connectivity using all conducting layers (unless otherwise noted), including AA, GT, and all back-end-of-line (BEOL) metal and via layers in the stack (M1 through last metal). It also includes connectivity through the substrate, through n-wells and p-wells and between n-wells through the deep n-well (for triple-well designs).
Source/Drain (S/D)	((AA NOT AR) INTERACT GATE) NOT ALL_GT) NOT Pick-up
DOP_AA	(AADOP OR AADMP)
AOP_AA	(AA OR DOP_AA)
DUM_AA	(AADUM OR DOP_AA)
ALL_AA	(AA OR DUM_AA)
ALL_AR_H	(AR_H OR AR_HDOP)
ALL_AR_V	(AR_V OR AR_VDOP)
DOP_GT	(GTDOP OR GTDMP)
AOP_GT	(GT OR DOP_GT)
DUM_GT	(GTDUM OR DOP_GT)
ALL_GT	(GT OR DUM_GT)
DOP_P2	(P2DOP OR P2DMP)
AOP_P2	(P2 OR DOP_P2)

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Name	Definitions
DUM_P2	(P2DUM OR DOP_P2)
ALL_P2	(P2 OR DUM_P2)
DOP_M0	(M0DOP OR M0DMP)
AOP_M0	(M0 OR DOP_M0)
DUM_M0	(M0DUM OR DOP_M0)
ALL_M0	(M0 OR DUM_M0)
DOP_M0C	(M0CDOP OR M0CDMP)
AOP_M0C	(M0C OR DOP_M0C)
DUM_M0C	(M0CDUM OR DOP_M0C)
ALL_M0C	(M0C OR DUM_M0C)
DOP_M0G	(M0GDOP OR M0GDMP)
AOP_M0G	(M0G OR DOP_M0G)
DUM_M0G	(M0GDUM OR DOP_M0G)
ALL_M0G	(M0G OR DUM_M0G)
Dummy_Cell	DMCB1
Dummy_Cell_WO_IMP	(DMCB1 NOT DMC1)
Dummy_Cell_WI_IMP	(DMCB1 AND DMC1)
DUM_AR	(ARDUM OR ARDOP)
DUM_V0	(V0DUM OR V0DPDUM)
DUM_M1	((M1DUM OR M1DOP) OR M1DPDUM) OR M1DPDOP)
DUM_M2	((M2DUM OR M2DOP) OR M2DPDUM) OR M2DPDOP)
DUM_M3	((M3DUM OR M3DOP) OR M3DPDUM) OR M3DPDOP)
DUM_M4	(M4DUM OR M4DOP)
DUM_M5	(M5DUM OR M5DOP)

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Name	Definitions
DUM_M6	(M6DUM OR M6DOP)
DUM_M7	(M7DUM OR M7DOP)
DUM_M8	(M8DUM OR M8DOP)
DUM_B1	(B1DUM OR B1DOP)
DUM_B2	(B2DUM OR B2DOP)
DUM_V1	(V1DUM OR V1DOP)
DUM_V2	(V2DUM OR V2DOP)
DUM_V3	(V3DUM OR V3DOP)
DUM_V4	(V4DUM OR V4DOP)
DUM_V5	(V5DUM OR V5DOP)
DUM_V6	(V6DUM OR V6DOP)

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### 7.1.12 Definition of connectivity used in DRC methodology

1. NW and DNW connectivity:
  - NW interact with DNW
2. Pick-up connectivity:
  - N+pick-up interact with NW;
  - P+pick-up interact with (NOT NW)
3. Poly connectivity:
  - Interconnect poly = (GT NOT P2)
4. Local interconnect metal connectivity:
  - Local interconnect metal = ((M0 NOT M0C) OR M0G);
  - S/D interact with local interconnect metal;
  - Interconnect poly interact with local interconnect metal;
  - Pick-up interact with local interconnect metal
5. BEOL connectivity:
  - Local interconnect metal connected with M1 by V0;
  - BEOL metal (NOT metal slot), via are defined as conducting layers by default, metal dummy is excluded;
  - Metal resistors and inductors are treated as conducting metal
6. MIM connectivity:

MIM is placed between TM2 and TM1

  - MIM is treated as blocking the via between metal layers of the layer above and below.
  - The via above MIM is treated as connecting MIM and its above metal layer TM2
  - The via above CTOP is treated as connecting CTOP and its above metal layer TM2

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### 7.1.13 Definition of net voltage in DRC methodology

#### Pri-1: TEXT label (Mn\_V\_Hi\_TOP, Mn\_V\_Lo\_TOP, Mn\_V\_Hi, Mn\_V\_Lo)

For high voltage label: Mn\_V\_Hi\_TOP, Mn\_V\_Hi

For low voltage label: Mn\_V\_Lo\_TOP, Mn\_V\_Lo

Designers add TEXT label with a voltage number (positive or negative numbers) is attached on metal/poly/local connect shape by using the layers that defined for the TEXT labels. This TEXT label indicates that a numeric-type property is created by converting the text value into a floating-point number, and this number will be assigned on the net as a voltage.

(a) If there is Mn\_V\_Hi\_TOP, Mn\_V\_Lo\_TOP labels, the associate voltage (the highest and or lowest voltage) is assigned to the value from the top labels on the net

(b) If there is only Mn\_V\_Hi, Mn\_V\_Lo labels, then the associate voltage will be assigned to the highest and the lowest value on the net.

Note:

1. Mn\_V\_Hi\_TOP, Mn\_V\_Lo\_TOP has a higher priority than Mn\_V\_Hi, Mn\_V\_Lo

#### Pri-2: Metal voltage marker

Mn\_0d1V, Mn\_0d2V, Mn\_0d3V, Mn\_0d4V, Mn\_0d5V, Mn\_0d6V, Mn\_0d7V, Mn\_0d8V, Mn\_0d9V, Mn\_0d10V, Mn\_0d11V, Mn\_0d13V, Mn\_0d14V, Mn\_0d16V, Mn\_0d17V, MnVxx (where xx belong to (12, 15, 18, 25, 33, 42, 50))

(a) If there is a metal marker shape on the net, then the associate voltage will be assigned on the net.

(b) If there are different voltage markers on the same net, the highest voltage will be assigned.

#### Pri-3: P-pickup

If the net connect to a p substrate pick-up, the net voltage is 0v

#### Pri-4: Core MOS device

If the net is connected to core MOS, the net voltage is 0.8v.

#### Pri-5: IO MOS device

If the net is connected to IO MOS, the net voltage is as follow.

#### Global priority for Pri-4 and Pri-5:

1. Default: lower voltage first, and P-pickup > PMOS > NMOS > VARMOS > GATE poly on the same voltage.
2. Switch “IO\_voltage\_first” on: higher voltage first, and P-pickup > PMOS > NMOS > VARMOS > GATE poly on the same voltage.

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3. Switch “SD\_voltage\_first” on: higher SD voltage > lower SD voltage > lower GATE voltage > higher GATE voltage, and P-pickup > PMOS > NMOS > VARMOS on the same voltage.

**Delta voltage calculation note:**

1. If Mn\_SYNC is not used between net A and net B, delta voltage calculate stratagem:

$$\text{Delta V} = \text{MAX} \{ \{\text{max (net voltage A)} - \text{min (net voltage B)}\}, \{\text{max (net voltage B)} - \text{min (net voltage A)}\} \}$$

2. If Mn\_SYNC is used between net A and net B, delta voltage calculate stratagem:

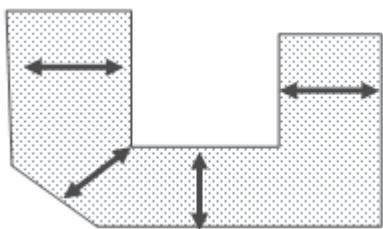
$$\text{Delta V} = \text{MAX} \{ \{\text{max (net voltage A)} - \text{max (net voltage B)}\}, \{\text{min (net voltage B)} - \text{min (net voltage A)}\} \}$$

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### 7.1.14 Definition of terminology

#### 1. Width

- The distance of interior-facing sides of one layer edges.



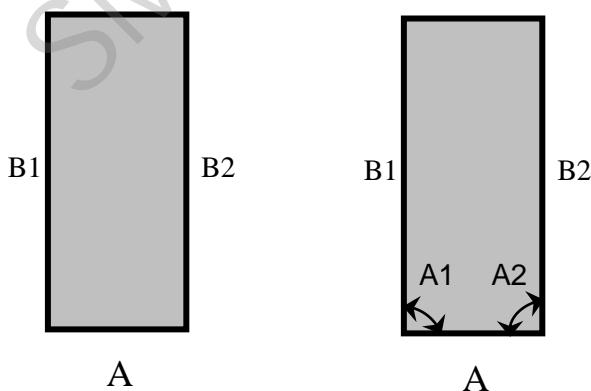
#### 2. Length

- Distance from one inside edge to a parallel inside edge within a same rectangular shape along the longer dimension of the shape.



#### 3. Line / Line-end

- Line: the line is defined for the edges with length  $> 0.08\mu m$  in general. (edge B1 or B2)
- Line-end: the line-end is defined for the edges with length  $\leq 0.08 \mu m$  in general (or the shorter edges for rectangular shape) and the edges formed by two consecutive 90 degree inner vertex. (edge A)

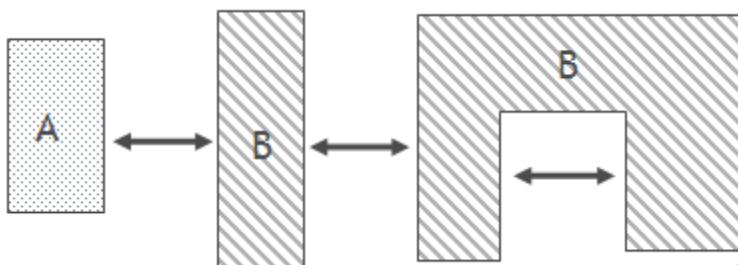


#### 4. Space

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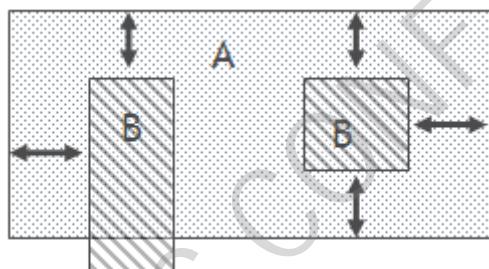
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- The distance of exterior-facing sides of one or two layer edges.



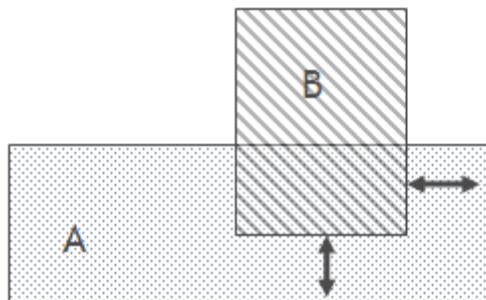
## 5. Enclosure

- The distance between the interior-facing sides of layer A edges and the exterior-facing sides of layer B edges.



## 6. Extension

- The distance between the interior-facing sides of layer A edges and the exterior-facing sides of layer B edges.

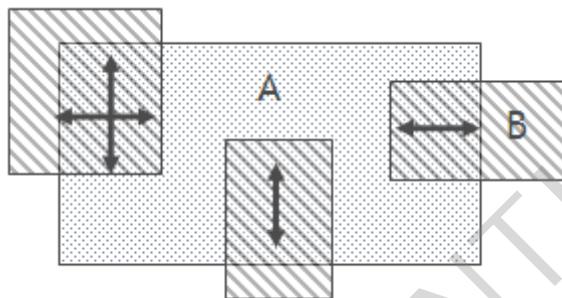


## 7. Overlap

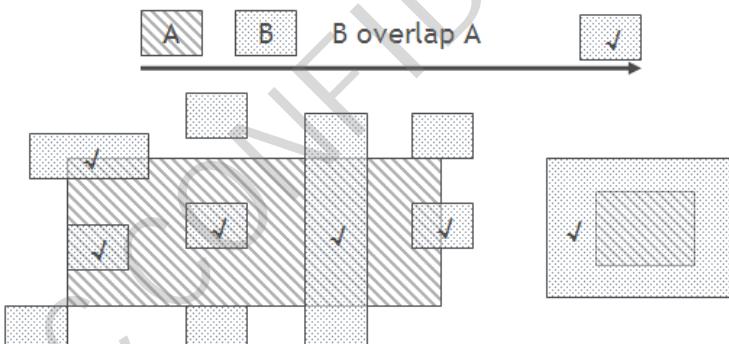
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- For the overlap-required rule: The distance between the interior-facing sides of layer A edges and the interior-facing sides of layer B edges



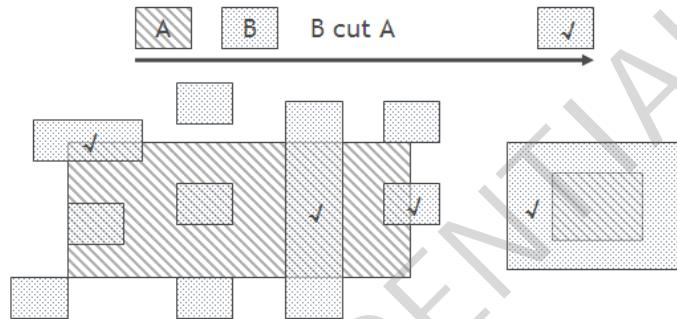
- For the non-overlap-required rule: Two layers share part (or all) of area.



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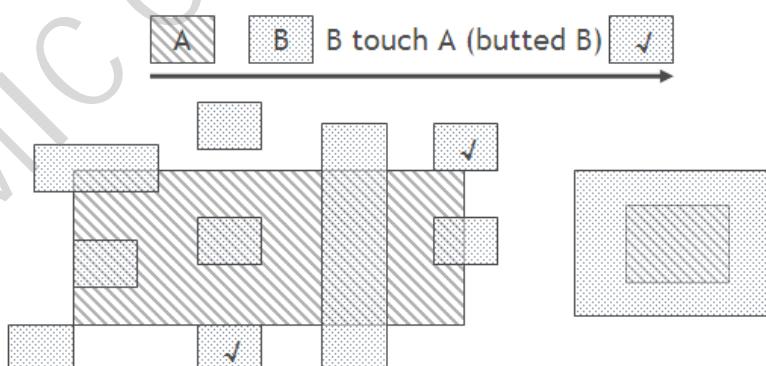
## 8. Cut

- A cut B: A share part (not all) of area with B;
- B cut A: B share part (not all) of area with A.



## 9. Butted

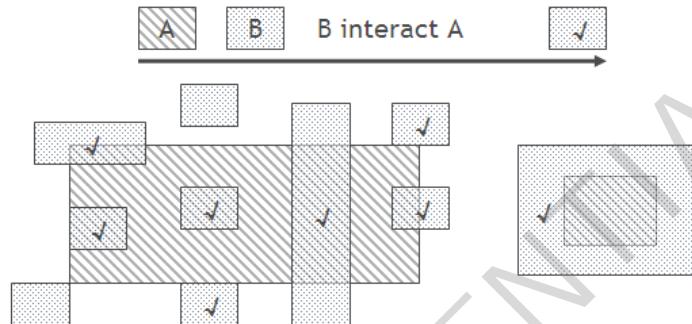
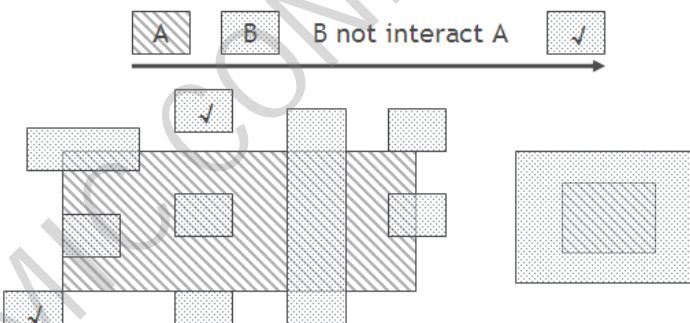
- Butted A: A share at least one edge (or edge segment) with B from outside;
- Butted B: B share at least one edge (or edge segment) with A from outside;



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**10. Interact**

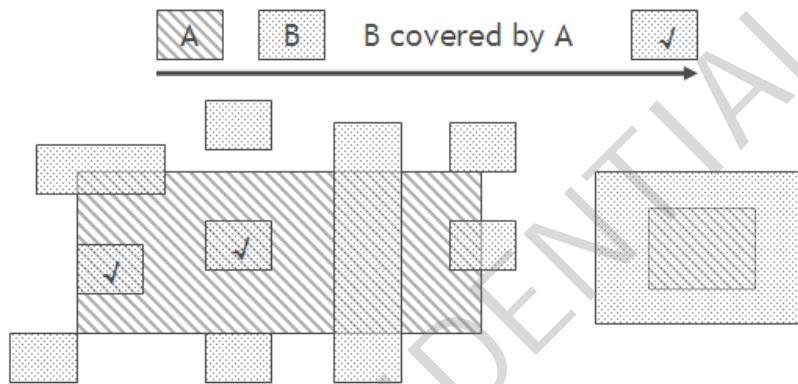
- A interact B: A touch or overlap B;
- B interact A: B touch or overlap A.

**11. Not Interact**

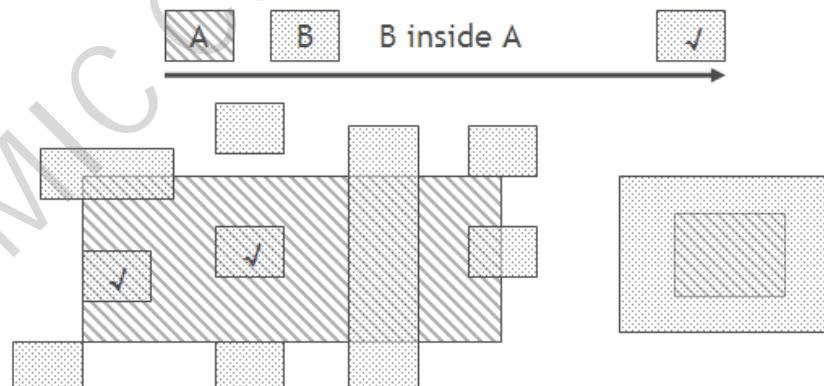
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**12. Cover**

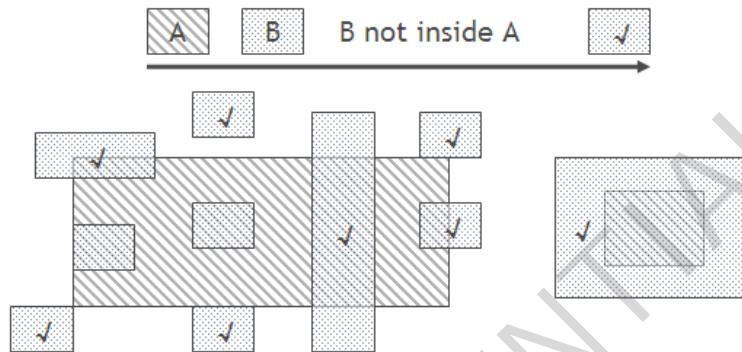
- A covered by B: A share all area with B;
- B covered by A: B share all area with A;

**13. Inside**

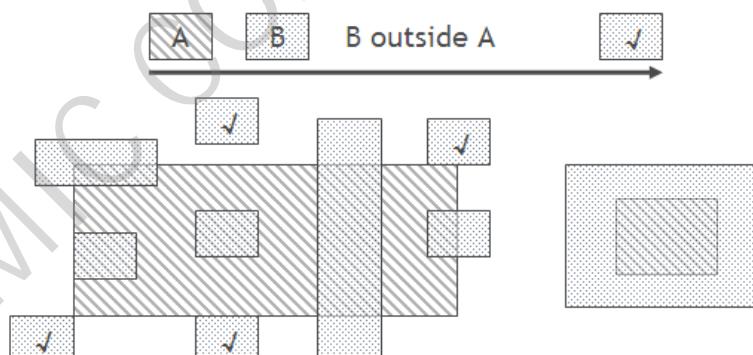
- A inside B (A covered by B): A share all area with B;
- B inside A (B covered by A): B share all area with A.



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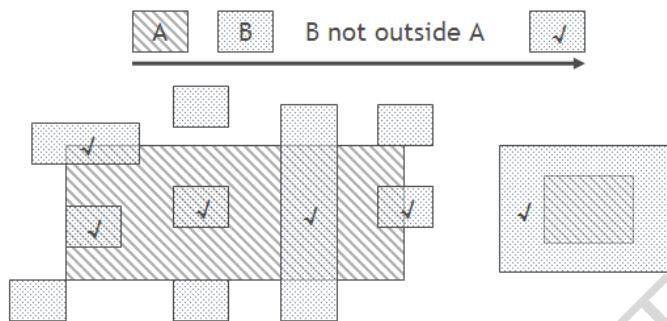
**14. Not Inside****15. Outside**

- A outside B: A doesn't share any area with B;
- B outside A: B doesn't share any area with A.



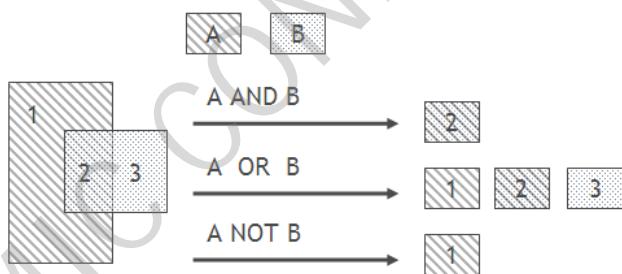
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## 16. Not Outside



## 17. AND / OR / NOT

- A AND B: Output the shared area of A and B;
- A OR B: A and B merge as one layer;
- A NOT B: A exclude the shared area of A and B.



## 18. GATE

- GATE = AA AND GT;
- Channel Length (L in figure): The distance between interior-facing sides of poly edge segments inside AA;
- Channel Width (W in figure): The distance between interior-facing sides of AA edge segments inside poly;
- ENDCAP: poly extension outside GATE in the channel width direction.

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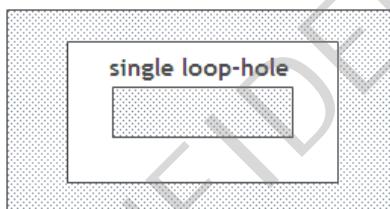
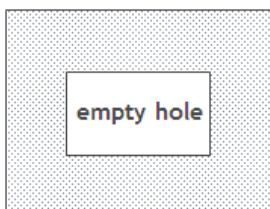
## 19. Area

- The area of the polygon.



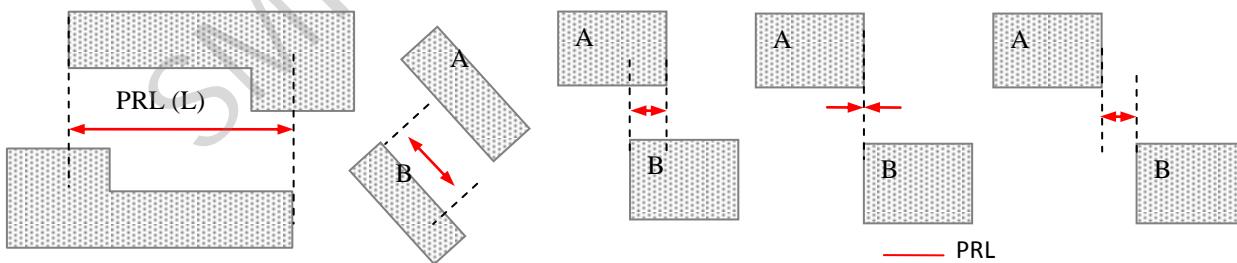
## 20. Enclosed Area

- The area of empty hole or single loop-hole.



## 21. Parallel Run Length

- Parallel Run Length is the projection length between two polygons, and PRL is the abbreviation for "Parallel Run Length".



PRL is the projection length between two polygons (in vertical, horizontal or 45 degree direction)

**Example:**  
PRL > 0 in 45 degree (or long side) direction

**Example 1:**  
PRL > 0 in horizontal (or long side) direction

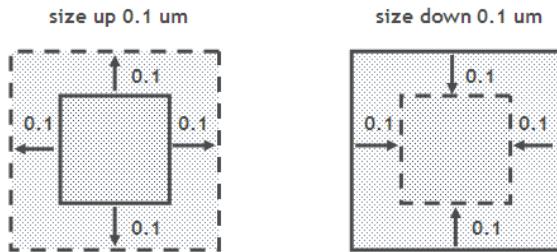
**Example 2:**  
PRL = 0 in horizontal (or long side) direction

**Example 3:**  
PRL < 0 in horizontal (or long side) direction

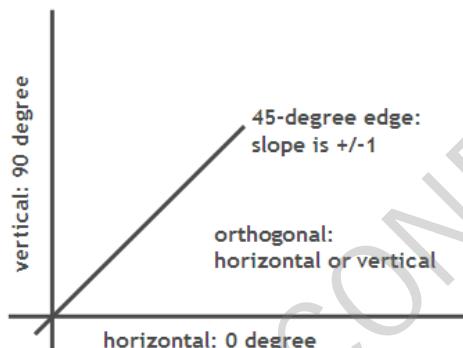
## 22. Size Up / Size Down

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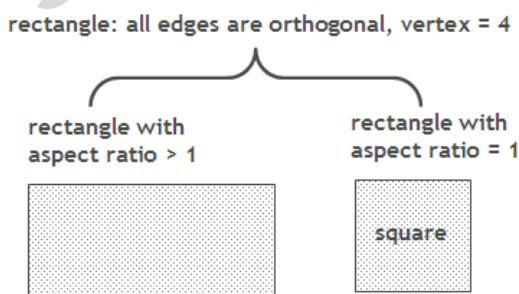


### 23. Horizontal / Vertical / 45-degree / Orthogonal



### 24. Rectangle / Square

- Rectangle: Orthogonal polygon with 4 vertexes;
- Square: Rectangle with aspect ratio equal to 1.



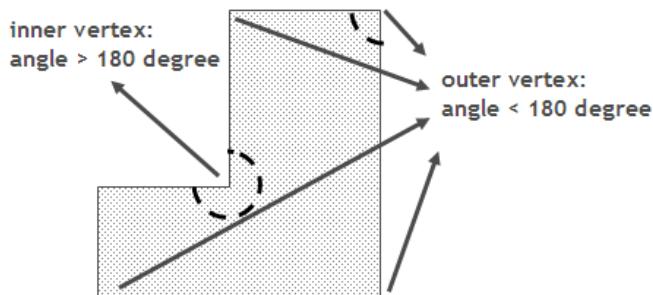
### 25. Vertex / Inner Vertex / Outer Vertex

- Inner Vertex (Concave Corner): angle > 180 degree measured inside polygon;

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- Outer Vertex (Convex Corner): angle < 180 degree measured inside polygon.



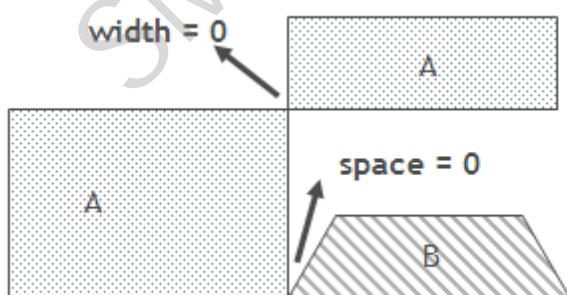
## 26. Single L/T/U/Z-shape / O-shape

Vertex = 8, with two consecutive 90-270-90 degree concave corner which have no coincide edge



## 27. Single-Point-Interaction

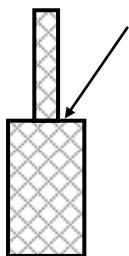
- One or two layers share one vertex from outside.



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**28. Poly jog**

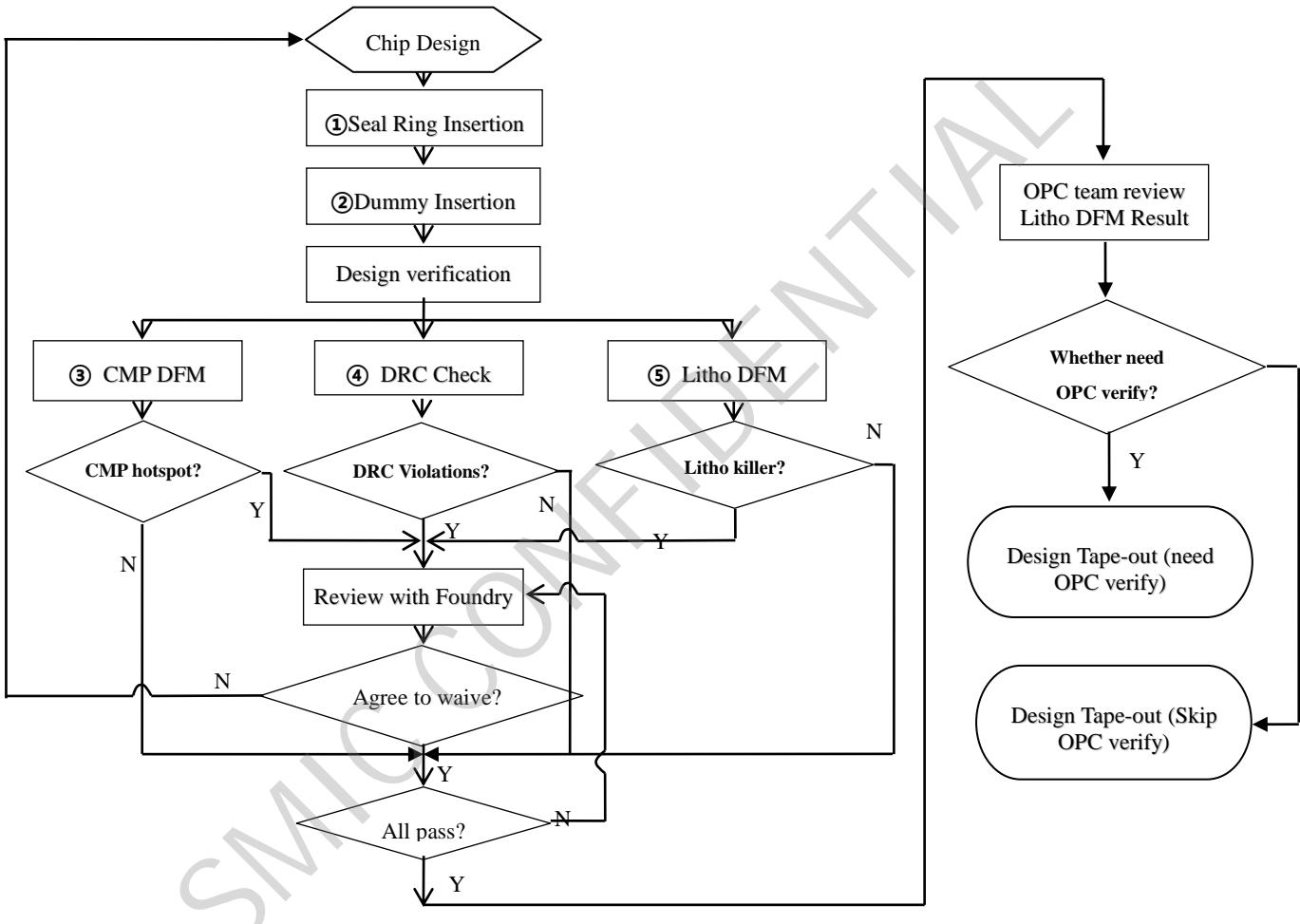
- The edge between consecutive 90-270-90 degree corners and adjacent edge is not line end.



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## 7.1.15 Design Check Flow for Tape out

### 7.1.15.1 Design Check Flow before Tape out



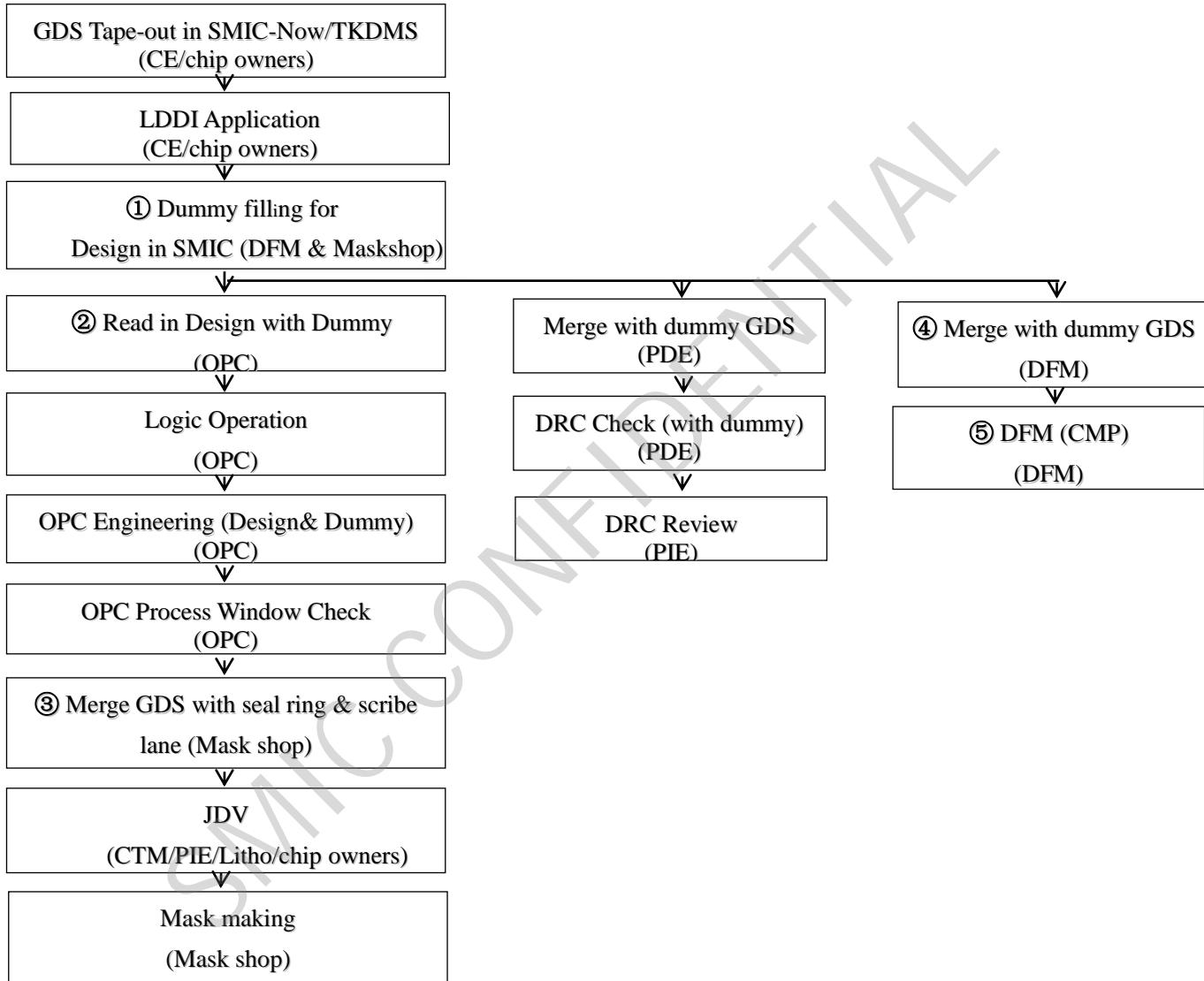
Notes:

1. Designer must clean DRC and DFM litho killer errors before tape-out. Non-cleans can not be waived unless SMIC does so after reviews.
2. Recommend designers to add seal ring (Step①) before DRC and DFM check following SMIC 14nm seal ring GDS sample.
3. Recommend designers to do dummy insertions (Step②) before DRC and DFM check. Without dummy inserted, design verification, CMP DFM, and DRC results related to dummy patterns will not be accurate.
4. Recommend designers to do the steps of ③, ④ and ⑤ by themselves. SMIC can help to do the work before tape out if designers have concerns.

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### 7.1.15.2 Post-Tape out Working Flow



Notes:

- If designers have inserted dummies and do not request SMIC to add dummy. Dummy patterns will be treated as design patterns. Steps of ① related with dummy will be skipped.
- If designers revised GDS layout (mask re-tooling) for the layers which need dummy insertion, in the step ①, all layers' dummies of this GDS should be generated again by DFM team, and then DFM team will pass the new version dummy file to relative departments.
- If designers have added seal ring before tape out, seal ring merge in the step of ③ will be skipped.

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4. DRC violations and DFM litho killer errors must be clean before tape-out. Designers must pass the results to SMIC.
5. If designers have added dummy filling and performed DFM CMP simulation before tape-out, step ④ and ⑤ can be skipped.

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2017-11-02



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## 7.2 Layout design rules

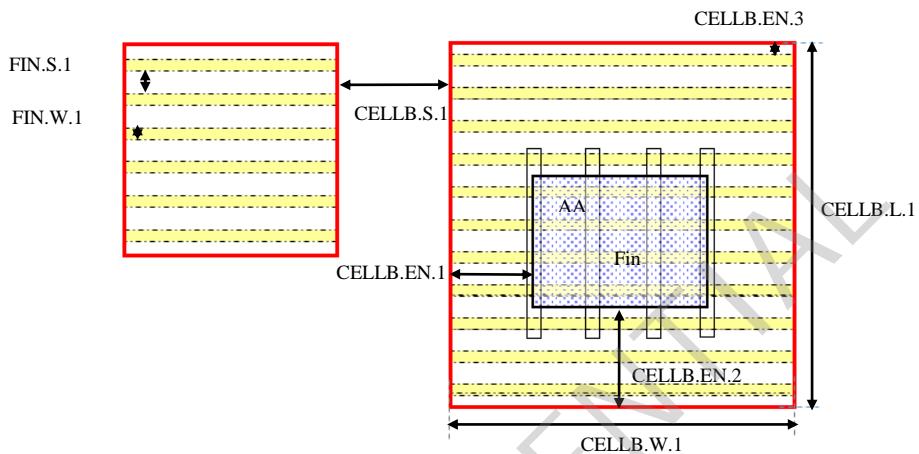
### 7.2.1 CELLB design rules

CELLB is a drawn layer and used to define cell edge, designers must draw CELLB layer following CELLB design rules below, FIN is a derived layer from CELLB by EDA tool, GATE poly direction grade  $0.048*n$  um,  $n \geq 0$  and  $n$  is an integer.

Rule number	Description	Opt.	Design Value	Unit
<b>FIN.W.1</b>	FIN width in GATE poly direction	=	0.01	um
<b>FIN.S.1</b>	FIN exact space in CELLB region along GATE poly direction, FIN vertical edge must align with CELLB	=	0.038	um
<b>FIN.R.1</b>	FIN must be an orthogonal rectangle.			
<b>FIN.R.2</b>	FIN must inside CELLB, except INST region			
<b>CELLB.W.1</b>	CELLB width in S/D direction	$\geq$	0.43	um
<b>CELLB.W.2</b>	CELLB width in GATE poly direction	=	$0.288+0.048*n$	um
<b>CELLB.W.3</b>	DMCB1 width in GATE poly direction.	=	$0.288+0.048*n$	um
<b>CELLB.W.4</b>	DMCB1 horizontal edge length	$\geq$	0.388	um
<b>CELLB.S.1</b>	CELLB space in S/D direction when PRL > -0.096um	$\geq$	0.11	um
<b>CELLB.S.2</b>	CELLB space in GATE poly direction when PRL > -0.11um	=	$0.096+0.048*n$	um
<b>CELLB.L.1</b>	(CELLB OR DMCB1) vertical edge length	=	$0.048+0.048*n$	um
<b>CELLB.EN.1</b>	CELLB enclosure of ALL_AA in S/D direction, except DMCB1 region	$\geq$	0.08	um
<b>CELLB.EN.2</b>	CELLB enclosure of ALL_AA in GATE poly direction, except DMCB1 region	=	$0.048+0.048*n$	um
<b>CELLB.EN.3</b>	CELLB enclosure of the outmost FIN within CELLB in GATE poly direction	=	0.019	um
<b>CELLB.R.1</b>	ALL_AA must be fully covered by CELLB, except DMCMK1, INST and MARKS regions.			
<b>CELLB.R.2</b>	CELLB interact with INST is not allowed.			
<b>CELLB.R.3</b>	CELLB edge must be orthogonal to grid, and 45-degree bent CELLB is not allowed.			

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### 7.2.2 AA design rules

AA is a drawn layer and AA width in GATE poly direction must grade  $0.048*n$  um ( $n \geq 0$  and  $n$  is an integer).

Rule number	Description	Opt.	Design Value	Unit
<b>AA.W.1</b>	ALL_AA width, except INST region	$\geq$	0.09	um
<b>AA.W.2</b>	ALL_AA width for I/O region, except DMC7 region.	$\geq$	0.144	um
<b>AA.W.3a</b>	ALL_AA width in GATE poly direction, except INST region	$=$	$0.096+0.048*n$	um
<b>AA.W.3b</b>	ALL_AA width in GATE poly direction for I/O region, except DMC7 region	$=$	$0.144+0.048*n$	um
<b>AA.W.4a</b>	Channel width of core device, except DMPNP, ESDIO1, ESDIO2, INST regions	$=$	$0.096+0.048*n$	um
<b>AA.W.4b</b>	Channel width of I/O device, except (pick-up NOT VARMOS)	$=$	$0.192+0.048*n$	um
<b>AA.W.5</b>	ALL_AA width in GATE poly direction, except INST region	$\leq$	0.96	um
<b>AA.L.2</b>	(AOP_AA AND FIN) length in S/D direction	$=$	0.09~105	um
<b>AA.L.3</b>	(DOP_AA AND FIN) length in S/D direction	$=$	0.09~11	um
<b>AA.L.4</b>	AA horizontal edge length between two consecutive 90-270 degree corners	$\geq$	0.27	um
<b>AA.L.5</b>	AA vertical edge length between two consecutive 270-90 degree corners	$\leq$	0.384	um
<b>AA.L.6</b>	AA horizontal edge length between two consecutive 270-270 degree corners	$\geq$	0.27	um
<b>AA.L.7</b>	Non-rectangle AA horizontal edge length between two consecutive 90-90 degree corners, except LDBK region	$\geq$	0.18	um
<b>AA.S.1</b>	Space between ALL_AA, except INST region	$\geq$	0.09	um
<b>AA.S.2</b>	Space between ALL_AA for I/O region (including core to I/O)	$\geq$	0.192	um
<b>AA.S.2a</b>	Space between ALL_AA (AA vertical edge extend 1/2 GT width) for I/O region in S/D direction	$\geq$	0.117	um
<b>AA.S.3a</b>	Space between ALL_AA in GATE poly direction when	$=$	$0.096+0.048*n$	um

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Rule number	Description	Opt.	Design Value	Unit
	PRL > -0.09um, except INST region			
<b>AA.S.3b</b>	Space between ALL_AA in GATE poly direction for I/O region when PRL > -0.198um	=	0.192+0.048*n	um
<b>AA.S.4</b>	Space between ALL_AA in GATE poly direction when at least one side ALL_AA horizontal edge length = 0.09um and PRL > -0.09um	=	0.096, $\geq$ 0.288+0.048*n	um
<b>AA.S.5a</b>	Space between NW and N+AA in PW, except INST and DIOMK2 regions	$\geq$	0.048	um
<b>AA.S.5b</b>	Space between NW and N+AA (AA vertical edge extend 1/2 GT width) in PW in S/D direction, except INST and DIOMK2 regions	$\geq$	0.065	um
<b>AA.S.6a</b>	Space between NW and P+ pick-up AA, except INST and DIOMK2 regions	$\geq$	0.048	um
<b>AA.S.6b</b>	Space between NW and P+ pick-up AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST and DIOMK2 regions	$\geq$	0.065	um
<b>AA.S.7a</b>	Space between NW and N+AA in I/O area, except DIOMK2 region	$\geq$	0.144	um
<b>AA.S.7b</b>	Space between NW and N+AA (AA vertical edge extend 1/2 GT width) in I/O area in S/D direction, except DIOMK2 region	$\geq$	0.162	um
<b>AA.S.8a</b>	Space between NW and N+AA (AA vertical edge extend 1/2 GT width) in GATE poly direction, when space in S/D direction < 0.079um at PW corner, except resistor NW and LDBK region	$\geq$	0.061	um
<b>AA.S.8b</b>	Space between NW and AA (AA vertical edge extend 1/2 GT width) in S/D direction, when space in GATE poly direction < 0.061um at PW corner, except resistor NW and LDBK region.	$\geq$	0.079	um
<b>AA.S.9</b>	Space between NW vertical edge (edge length $\leq$ 0.296um between two concave corners with both sides length $\geq$ 0.09um) and AA (AA vertical edge extend 1/2 GT width) in S/D direction	$\geq$	0.079	um
<b>AA.S.9a</b>	Space between AA line-end (AA vertical edge extend 1/2 GT width) and NW space-end in GATE poly direction	$\geq$	0.071	um

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Rule number	Description	Opt.	Design Value	Unit
	when space in S/D direction $\leq 0.14\text{um}$ , except INST region.  NW space-end: vertical space $< 0.24\text{um}$ between two consecutive 270-270 degree corners with both sides length $\geq 0.09\text{um}$ .  AA line-end: vertical width $\leq 0.096\text{um}$ between two consecutive 90-90 degree corners.			
AA.S.9b	Space between AA line-end (AA vertical edge extend 1/2 GT width) and NW space-end in S/D direction when space in GATE poly direction $\leq 0.061\text{um}$ , except INST region.  NW space-end: vertical space $< 0.24\text{um}$ between two consecutive 270-270 degree corners with both sides length $\geq 0.09\text{um}$ .  AA line-end: vertical width $\leq 0.096\text{um}$ between two consecutive 90-90 degree corners.	$\geq$	0.088	um
AA.S.10	Space between ACTIVE AA and pick-up AA in S/D direction, except DSTR and INST regions	$\geq$	0.18	um
AA.S.11a	Space between AOP_AA (AA vertical edge extend 1/2 GT width) in S/D direction (maximum delta V $\geq 1.32\text{V}$ (1.2V + 10%))  DRC waive violation between S/D sharing one GATE	$\geq$	0.117	um
AA.S.11b	Space between AOP_AA (maximum delta V $\geq 1.32\text{V}$ , 1.2V + 10%)	$\geq$	0.096	um
AA.S.11c	Space between AOP_AA in S/D direction (AA vertical edge extend 1/2 GT width) (maximum delta V $\geq 1.98\text{V}$ , 1.8V + 10%)  DRC waive violation between S/D sharing one GATE	$\geq$	0.148	um
AA.S.11d	Space between AOP_AA (maximum delta V $\geq 1.98\text{V}$ , 1.8V + 10%)	$\geq$	0.144	um
AA.S.11e	Space between AOP_AA (AA vertical edge extend 1/2 GT width) in S/D direction (maximum delta V $\geq 3.63\text{V}$ , 3.3V + 10%)  DRC waive violation between S/D sharing one GATE	$\geq$	0.248	um

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Rule number	Description	Opt.	Design Value	Unit
<b>AA.S.11f</b>	Space between AOP_AA (maximum delta V $\geq$ 3.63V, 3.3V + 10%)	$\geq$	0.24	um
<b>AA.S.12a</b>	Space between NW and N+ ACTIVE (Maximum delta V > 3.63V, 3.3V+10%)	$\geq$	0.144	um
<b>AA.S.12b</b>	Space between NW and N+ ACTIVE (AA vertical edge extend 1/2 GT width) in S/D direction (Maximum delta V > 3.63V, 3.3V+10%)	$\geq$	0.162	um
<b>AA.S.13</b>	Empty ALL_AA space, except RESNW, RESP1, OCOVL, (NODMF su 1um) and LOGO regions. This rule is a local density related rule. DRC flags if (((Chip NOT ALL_AA) sd 1.05um) su 1.05um) region greater than 2.1*2.1um.	$\leq$	2.1	um
<b>AA.S.14</b>	Empty ALL_AA space in RESNW and RESP1 regions. This rule is a local density related rule. DRC flags if (((Chip NOT ALL_AA) sd 2.55um) su 2.55um) region greater than 5.1*5.1um.	$\leq$	5.1	um
<b>AA.S.15</b>	Space between NPAA and AA (overlap is not allowed) (NPAA in chip is not allowed, this rule only for SMIC internal test structure usage).	$\geq$	0.5	um
<b>AA.S.16</b>	Space between AA vertical edge (edge length $\leq$ 0.144um between two consecutive 270-90 degree corners) when 0 < PRL $\leq$ 0.048um	$\geq$	0.18	um
<b>AA.S.17</b>	Forbidden space between ALL_AA (width = 0.096um) at both side and ALL_AA in GATE poly direction	=	0.144	um
<b>AA.S.18</b>	(purposely blank)			
<b>AA.S.19</b>	Forbidden space between (ALL_AA vertical edge expand 0.089um) in GATE poly direction when both two adjacent space = 0.096um, and the space between two 0.096um space region is 0.048um in GATE poly direction.	=	0.24	um
<b>AA.EN.1a</b>	P+AA enclosure by NW, except INST and DIOMK2 regions	$\geq$	0.048	um
<b>AA.EN.1b</b>	N+ pick-up AA enclosure by NW, except INST and DIOMK2 regions	$\geq$	0.048	um

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Rule number	Description	Opt.	Design Value	Unit
<b>AA.EN.1c</b>	P+AA (AA vertical edge extend 1/2 GT width) enclosure by NW in S/D direction, except INST and DIOMK2 regions	$\geq$	0.065	um
<b>AA.EN.1d</b>	N+ pick-up AA (AA vertical edge extend 1/2 GT width) enclosure by NW in S/D direction, except INST and DIOMK2 regions	$\geq$	0.065	um
<b>AA.EN.1f</b>	P+AA enclosure by NW in I/O region, except DIOMK2 region	$\geq$	0.144	um
<b>AA.EN.1g</b>	P+AA (AA vertical edge extend 1/2 GT width) enclosure by NW in I/O region in S/D direction, except DIOMK2 region	$\geq$	0.162	um
<b>AA.EN.2</b>	The outmost FIN enclosure by ALL_AA in GATE poly direction, except LDBK, DMCMK1, INST and MARKS regions	=	0.019	um
<b>AA.EN.2a</b>	P+AA (AA vertical edge extend 1/2 GT width) enclosure by NW corner in GATE poly direction when enclosure in S/D direction $< 0.079\text{um}$	$\geq$	0.061	um
<b>AA.EN.2b</b>	P+AA (AA vertical edge extend 1/2 GT width) enclosure by NW corner in S/D direction when enclosure in GATE poly direction $< 0.061\text{um}$	$\geq$	0.079	um
<b>AA.EN.2c</b>	AA (AA vertical edge extend 1/2 GT width) enclosure by NW line-end in S/D direction (line-end vertical width $\leq 0.296\text{um}$ between two consecutive 90-90 degree corners with both sides length $\geq 0.09\text{um}$ )	$\geq$	0.079	um
<b>AA.EN.2d</b>	AA line-end (AA vertical edge extend 1/2 GT width) enclosure by NW line-end in GATE poly direction when enclosure in S/D direction $\leq 0.14\text{um}$ , except INST region.  NW line-end: vertical width $< 0.24\text{um}$ between two consecutive 90-90 degree corners with both sides length $\geq 0.09\text{um}$ .  AA line-end: vertical width $\leq 0.096\text{um}$ between two consecutive 90-90 degree corners.	$\geq$	0.071	um
<b>AA.EN.2e</b>	AA line-end (AA vertical edge extend 1/2 GT width)	$\geq$	0.088	um

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Rule number	Description	Opt.	Design Value	Unit
	enclosure by NW line-end in S/D direction when enclosure in GATE poly direction $\leq 0.061\text{um}$ , except INST region.  NW line-end: vertical width $< 0.24\text{um}$ between two consecutive 90-90 degree corners with both sides length $\geq 0.09\text{um}$ .  AA line-end: vertical width $\leq 0.096\text{um}$ between two consecutive 90-90 degree corners.			
<b>AA.EN.3a</b>	NW enclosure of P+ ACTIVE (Maximum delta V $> 3.63\text{V}, 3.3\text{V}+10\%$ )	$\geq$	0.144	um
<b>AA.EN.3b</b>	NW enclosure of P+ ACTIVE (AA vertical edge extend 1/2 GT width) in S/D direction (Maximum delta V $> 3.63\text{V}, 3.3\text{V}+10\%$ )	$\geq$	0.162	um
<b>AA.A.1</b>	AOP_AA area, except INST region	$\geq$	0.0138	um <sup>2</sup>
<b>AA.A.2</b>	AOP_AA area in I/O region, except DMC7 region	$\geq$	0.0285	um <sup>2</sup>
<b>AA.A.3</b>	AOP_AA area (length = 0.09um in S/D direction)	$\geq$	0.0172	um <sup>2</sup>
<b>AA.A.4</b>	Total area of ((ACTIVE INTERACT GT) NOT GT) in the same AA for NMOS or PMOS device	$\leq$	100	um <sup>2</sup>
<b>AA.D.1</b>	Full chip ALL_AA density	$\geq$	25%	
<b>AA.D.2</b>	Full chip ALL_AA density	$\leq$	60%	
<b>AA.D.3</b>	ALL_AA density (window 18um*18um, stepping 9um), except LOGO, OCOVL, (NODMF su 1um) region	$\geq$	11.8%	
<b>AA.D.4</b>	ALL_AA density in ((RESP1 su 10um) NOT RESP1)	$\geq$	20%	
<b>AA.D.5</b>	Maximum ALL_AA density in core region (window 100um*100um, stepping 50um)	$\leq$	70%	
<b>AA.D.6</b>	Maximum ALL_AA density in I/O region (window 100um*100um, stepping 50um)	$\leq$	80%	
<b>AA.R.1</b>	ALL_AA must be fully covered by (SN OR SP), except DMCMK1 and MARKS regions.			
<b>AA.R.2</b>	NPAA in chip design is not allowed.			
<b>AA.R.3</b>	DOP_AA overlap AA, GT is not allowed.			

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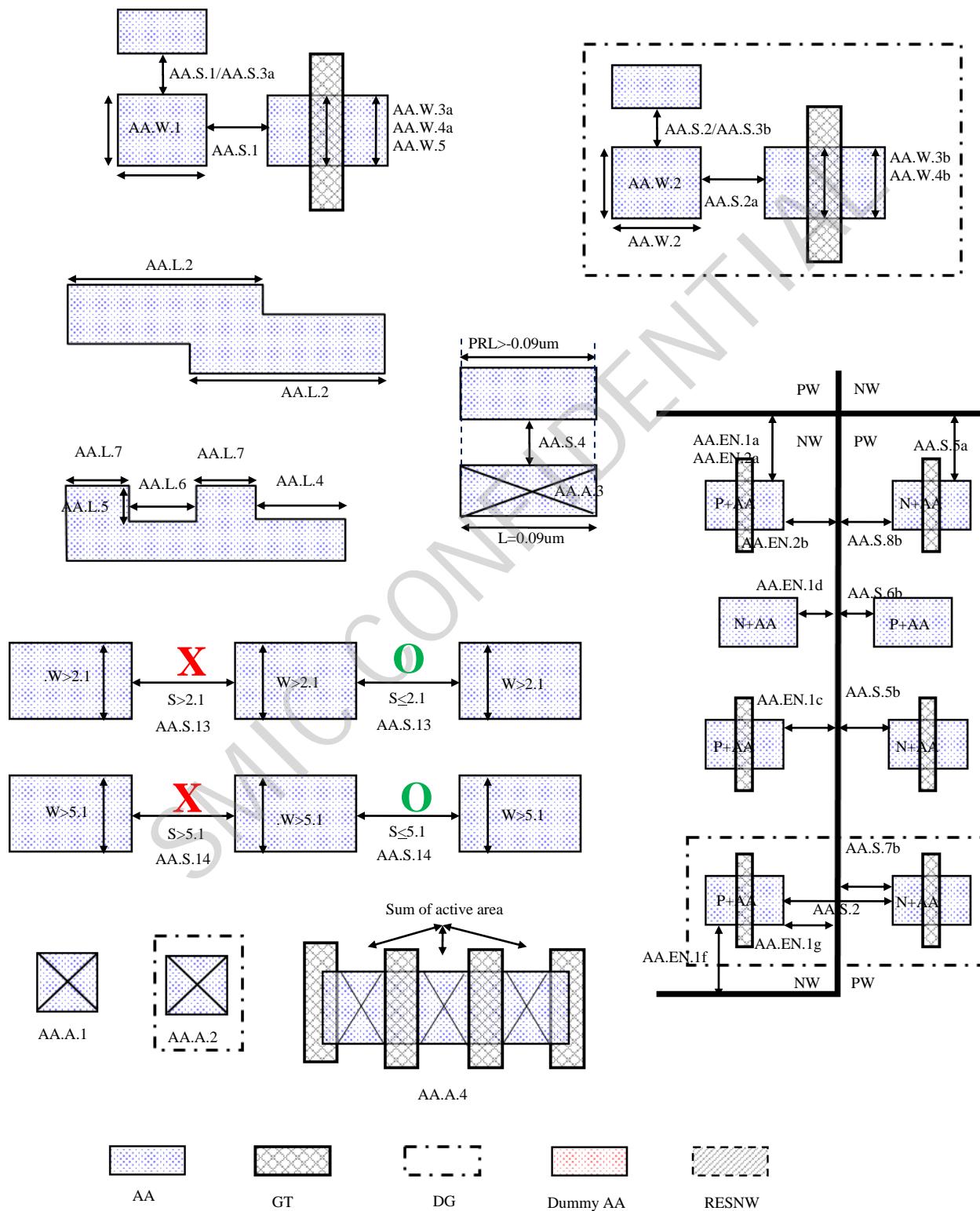
Rule number	Description	Opt.	Design Value	Unit
<b>AA.R.5</b>	AA must be orthogonal to grid (Single Z-shape AA is not allowed).			
<b>AA.R.6</b>	AA interacted with GT (width $\geq$ 0.032um) must be rectangular.			
<b>AA.R.7</b>	DUM_AA must be rectangle			

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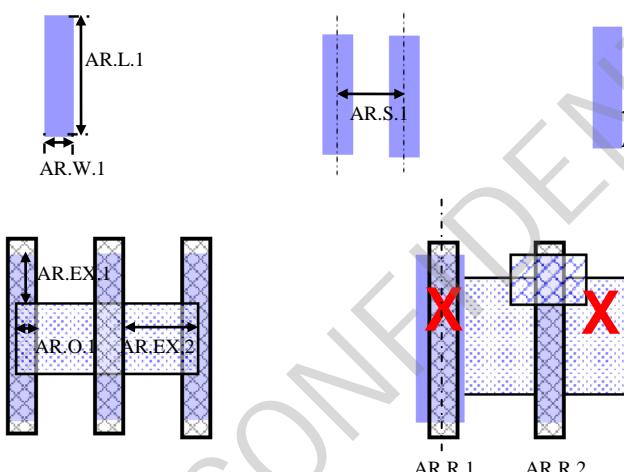
### 7.2.3 AR design rules

Rule number	Description	Opt.	Design Value	Unit
<b>AR.W.1</b>	AR width in S/D direction, except OCOVL region	=	0.02	um
<b>AR.S.1</b>	AR pitch in S/D direction	$\geq$	0.09	um
<b>AR.S.2</b>	Space between AR and ALL_AA	$\geq$	0.048	um
<b>AR.S.3</b>	Space between AR in GATE poly direction	$\geq$	0.144	um
<b>AR.EX.1</b>	AR extension outside of AA in GATE poly direction (extension $\leq 0$ is not allowed)	=	0.048 +0.048*n	um
<b>AR.EX.2</b>	AA extension outside of AR in S/D direction	=	-0.01, $\geq 0.17$	um
<b>AR.O.1</b>	AA overlap AR in S/D direction	=	0.01, 0.02	um
<b>AR.L.1</b>	AR length in GATE poly direction, except OCOVL region	$\geq$	0.24	um
<b>AR.L.2</b>	Length of (ALL_AR AND ((ALL_AA with vertical edge extend 1/2 GT width) horizontal edge extend 0.12um)) in GATE poly direction	$\leq$	52	um
<b>AR.A.1</b>	AR area	$\geq$	0.0048	um <sup>2</sup>
<b>AR.DN.1</b>	Full chip ((AR OR (ARDUM sd 0.02um)) OR ARDOP) density	$\geq$	5%	
<b>AR.DN.2</b>	Full chip ((AR OR (ARDUM sd 0.02um)) OR ARDOP) density	$\leq$	10%	
<b>AR.DN.3</b>	((AR OR (ARDUM sd 0.02um)) OR ARDOP) density (window 18umx18um, stepping 9um), except OCOVL region	$\leq$	15%	
<b>AR.R.1</b>	AR vertical edge must align with GT, except small GT jog $\leq 0.004\text{um}$ , except OCOVL region			
<b>AR.R.2</b>	M0G overlap ((GT NOT P2) INTERACT AR) is not allowed.			
<b>AR.R.3</b>	AR must inside CELLB, except OCOVL region.			
<b>AR.R.4</b>	AR interact pick-up AA, DSTR, DMCMK1, DG or INST is not allowed.			
<b>AR.R.5</b>	AR must be vertical rectangle.			

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Rule number	Description	Opt.	Design Value	Unit
<b>AR.R.6</b>	Maximum delta V > 1.15V between two S/D active beside AR is not allowed.			
<b>AR.R.7</b>	AR must overlap AOP_GT, except OCOVL region.			



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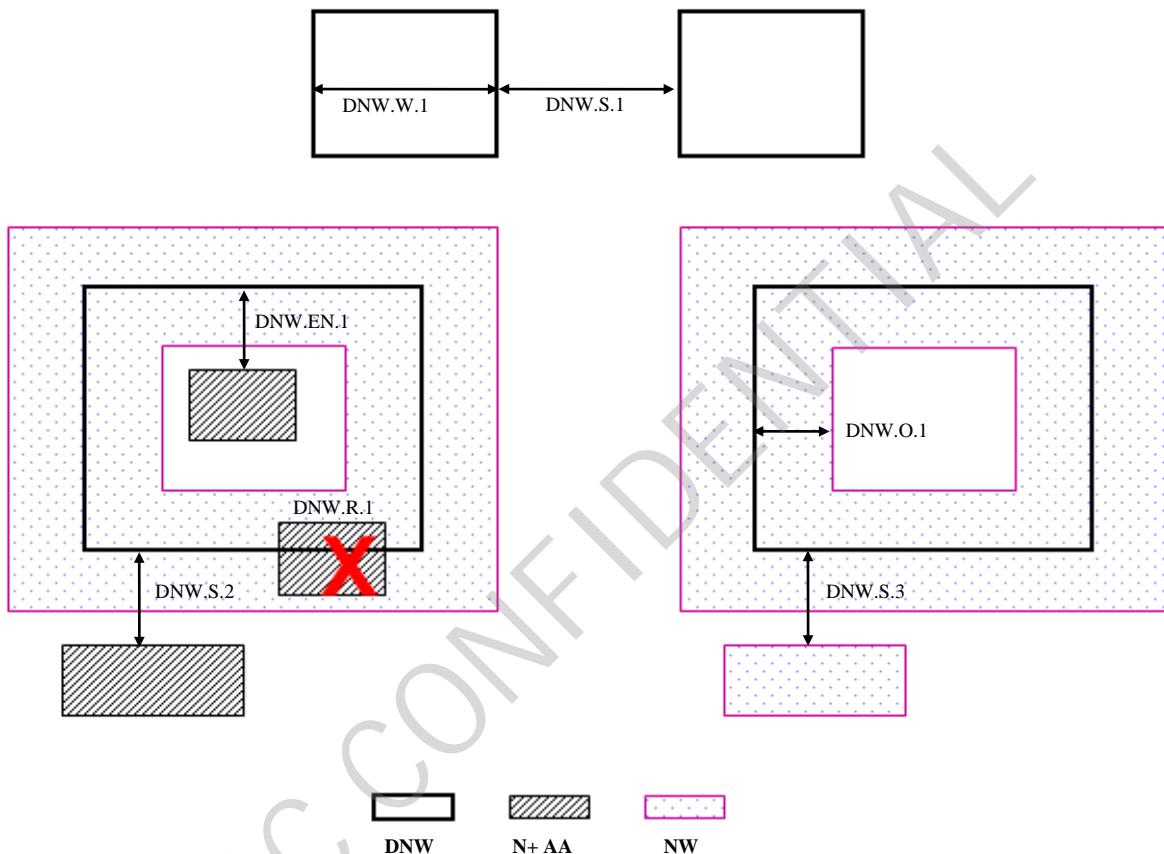
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#### 7.2.4 DNW design rules

Rule number	Description	Opt.	Design Value	Unit
<b>DNW.W.1</b>	DNW width	≥	1.49	um
<b>DNW.S.1</b>	Space between two DNWs	≥	3.1	um
<b>DNW.S.2</b>	Space between DNW and N+AA (N+AA outside of DNW or NW)	≥	1.48	um
<b>DNW.S.3</b>	Space between DNW and NW at different net	≥	1.49	um
<b>DNW.S.4</b>	Space between (NW hole in DNW) and ((NW hole in DNW) OR PW) at different net	≥	0.52	um
<b>DNW.S.5</b>	Space between (NW hole in DNW) and (((NW hole in DNW) OR PW) INTERACT DG) at different net	≥	0.896	um
<b>DNW.EN.1</b>	N+AA enclosure by DNW	≥	0.42	um
<b>DNW.O.1</b>	Overlap of NW and DNW	≥	0.358	um
<b>DNW.R.1</b>	N+AA cut DNW is not allowed.			
<b>DNW.R.2<sup>[NC]</sup></b>	Floating NW hole in DNW is not recommended to avoid unstable device performance			
<b>DNW.R.3</b>	Maximum delta V ≥ 5.6V is not allowed, when: 1. Space between DNW and DNW/NW is < 5um 2. Space between RW and RW/PW is < 5um			

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### 7.2.5 NW design rules

Core\_NW = NW NOT DG      Core\_PW = NOT (DG OR NW)

IO\_NW = NW AND DG      IO\_PW = DG NOT NW

Rule number	Description	Opt.	Design Value	Unit
<b>NW.W.1</b>	NW width, except INST region	≥	0.214	um
<b>NW.W.2</b>	IO_NW width	≥	0.214	um
<b>NW.W.2a</b>	IO_PW width, except INST region	≥	0.238	um
<b>NW.W.3.1</b>	Core_NW width, except INST region	≥	0.214	um
<b>NW.W.3.2</b>	(NW OR DG) width, except INST region	≥	0.214	um
<b>NW.W.4a</b>	NW width, when the space ≤ 0.235um, except INST region	≤	0.365	um
<b>NW.W.4b</b>	Core_NW width, when the space ≤ 0.235um, except INST region	≤	0.365	um
<b>NW.W.4d</b>	IO_NW width, when the space ≤ 0.235um, except INST region	≤	0.365	um
<b>NW.W.4e</b>	IO_PW width, when the space ≤ 0.235um, except INST region	≤	0.365	um
<b>NW.W.5</b>	(NW OR DG) width, when the space ≤ 0.235um	≤	0.365	um
<b>NW.S.1</b>	NW space, except INST region	≥	0.214	um
<b>NW.S.1a.1</b>	(NW OR DG) space, except INST region	≥	0.214	um
<b>NW.S.1a.2</b>	Core_NW space, except INST region	≥	0.214	um
<b>NW.S.1a.3</b>	IO_PW space, except INST region	≥	0.214	um
<b>NW.S.1b</b>	IO_NW space	≥	0.238	um
<b>NW.S.2.d</b>	NW space, when the width ≤ 0.235um, expect INST region	≤	0.365	um
<b>NW.S.2.e</b>	Core_NW space, when the width ≤ 0.235um, expect INST region	≤	0.365	um
<b>NW.S.2.f</b>	(NW OR DG) space, when the width ≤ 0.235um, expect INST region	≤	0.365	um
<b>NW.S.2a.1</b>	IO_NW space, when the width ≤ 0.235um	≤	0.365	um
<b>NW.S.2a.2</b>	IO_PW space, when the width ≤ 0.235um	≤	0.365	um
<b>NW.S.3a</b>	Space between NWs when PRL ≥ 0.255um, except INST region	≥	0.248	um

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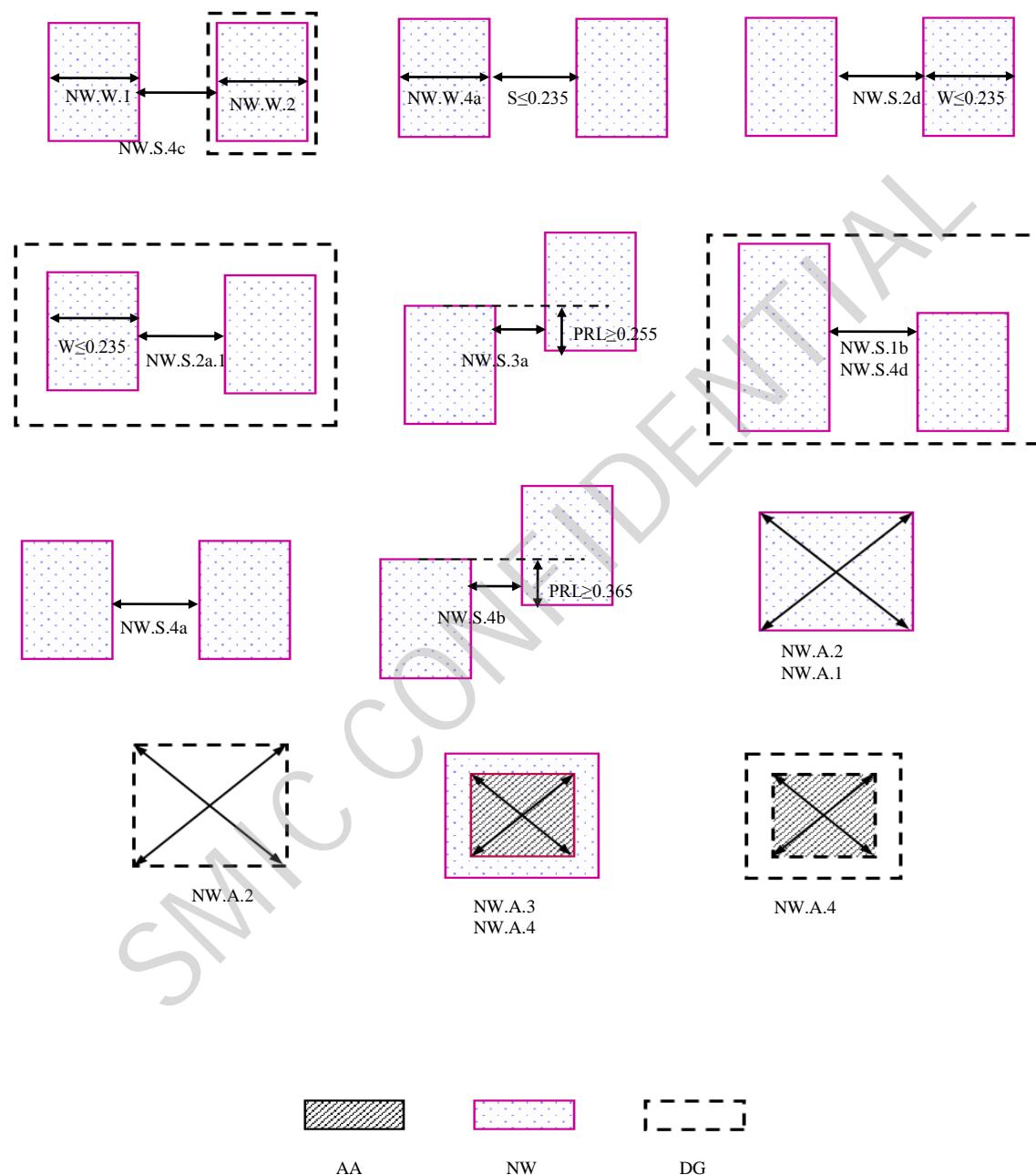


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Rule number	Description	Opt.	Design Value	Unit
<b>NW.S.4a</b>	Space between core NWs at different net, except INST region	$\geq$	0.38	um
<b>NW.S.4b</b>	Space between core NWs at different net when PRL $\geq$ 0.365um	$\geq$	0.475	um
<b>NW.S.4c</b>	Space between core NW and IO_NW at different net	$\geq$	0.896	um
<b>NW.S.4d</b>	Space between IO_NWs at different net	$\geq$	0.896	um
<b>NW.S.5</b>	Space between NWs (maximum delta V > 3.63V, 3.3V+10%)	$\geq$	1.75	um
<b>NW.S.6a</b>	Space between NW and DOP_AA (DOP_AA CUT NW is not allowed) , except ((DOP_AA INSIDE DMCB1) NOT DMC1)	$\geq$	0.048	um
<b>NW.S.6b</b>	Space between NW and DOP_AA (AA vertical edge extend 1/2 GT width) in S/D direction (DOP_AA CUT NW is not allowed), except ((DOP_AA INSIDE DMCB1) NOT DMC1)	$\geq$	0.065	um
<b>NW.EN.1</b>	NW enclosure of DOP_AA (Except Dummy_Cell_WO_IMP)	$\geq$	0.048	um
<b>NW.EN.1a</b>	NW enclosure of DOP_AA (AA vertical edge extend 1/2 GT width) in S/D direction, except Dummy_Cell_WO_IMP	$\geq$	0.065	um
<b>NW.A.1</b>	NW area, except 1.546um*0.196um NW in INST region	$\geq$	0.32	um <sup>2</sup>
<b>NW.A.2</b>	Area of Core_NW, Core_PW, IO_NW, IO_PW, except 1.546um*0.196um Core_NW in INST region	$\geq$	0.32	um <sup>2</sup>
<b>NW.A.3</b>	NW enclosed area	$\geq$	0.32	um <sup>2</sup>
<b>NW.A.4</b>	Enclosed area of Core_NW, Core_PW, IO_NW, IO_PW, except Core_PW enclosed area is 1.546um*0.196um in INST region	$\geq$	0.32	um <sup>2</sup>
<b>NW.R.1<sup>[NC]</sup></b>	Unintentional floating well is not recommend to avoid unstable device performance.			
<b>NW.R.2</b>	Maximum delta V $\geq$ 5.6V is not allowed, when: 1. Space between NWs is < 1.8um 2. Space between NW and N+AA/P+ pick-up AA is < 1.65um 3. Space between PW and P+AA/N+ pick-up AA is < 1.65um			

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### 7.2.6 PSUB design rules

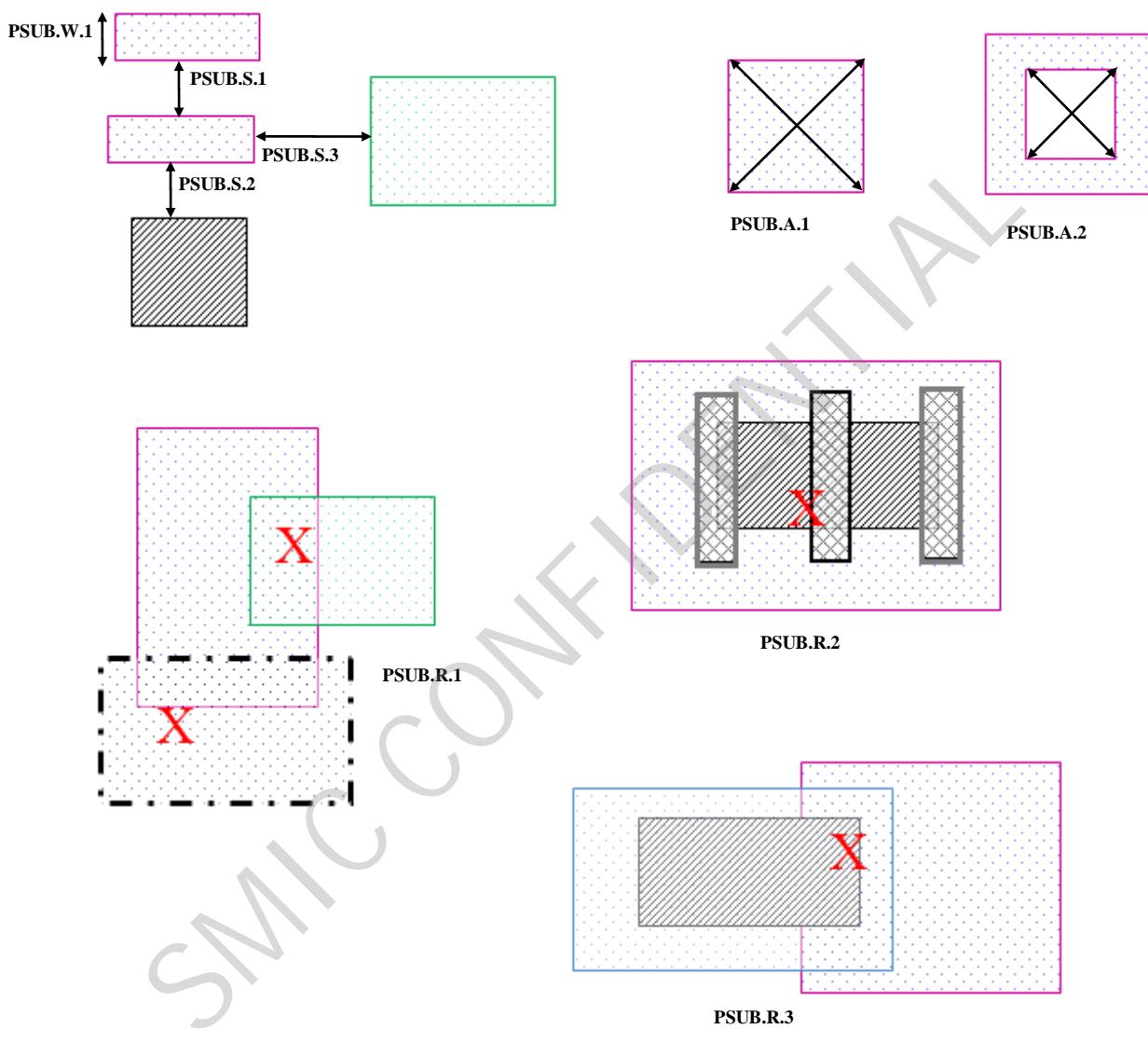
Rule number	Description	Opt.	Design Value	Unit
<b>PSUB.W.1</b>	PSUB width	$\geq$	0.214	um
<b>PSUB.S.1</b>	Space between two PSUBs	$\geq$	0.214	um
<b>PSUB.S.2</b>	Space between PSUB and AA	$\geq$	0.34	um
<b>PSUB.S.3</b>	Space between PSUB and NW	$\geq$	0.718	um
<b>PSUB.A.1</b>	PSUB area	$\geq$	0.32	um
<b>PSUB.A.2</b>	PSUB enclosure area	$\geq$	0.32	um
<b>PSUB.R.1</b>	PSUB overlap (NW OR DNW) is not allowed.			
<b>PSUB.R.2</b>	PSUB overlap (GATE NOT GTMK2) is not allowed, except ESD region			
<b>PSUB.R.3</b>	AA cut PSUB is not allowed.			

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### 7.2.7 SVT\_N design rules

A drawn SVT\_N layer is needed to define N-type standard Vt MOS devices. SVT\_N is for 0.8V core N-type standard Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
SVT_N.W.1	<p>SVT_N width, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) SVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.192	um
SVT_N.W.2	<p>SVT_N width in S/D direction, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) SVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.27	um
SVT_N.W.3	<p>SVT_N width in S/D direction, when one SVT_N vertical edge CUT (GTMK1 OR AR) and ABUT HVT_N</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.315	um
SVT_N.W.4	SVT_N width in GATE poly direction when SVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	$\geq$	0.238	um

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Rule number	Description	Opt.	Design Value	Unit
SVT_N.S.1	Space between SVT_N, single-point-interaction is allowed.  DRC waive: 1) SVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.192	um
SVT_N.S.2	Space between SVT_N in S/D direction, single-point-interaction is allowed.  DRC waive: 1) SVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
SVT_N.S.3a	Space between SVT_N in S/D direction, when just one SVT_N vertical edge CUT (GTMK1 OR AR) and abut LVT_N or ULVT_N  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.315	um
SVT_N.S.3b	Space between SVT_N in S/D direction, when both SVT_N vertical edge CUT (GTMK1 OR AR) and abut LVT_N or ULVT_N  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two	$\geq$	0.36	um

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Rule number	Description	Opt.	Design Value	Unit
	consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
<b>SVT_N.S.4</b>	Space between SVT_N when PRL $\geq$ 0.29um	$\geq$	0.248	um
<b>SVT_N.S.5</b>	SVT_N space in GATE poly direction when SVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um in GATE poly direction	$\geq$	0.238	um
<b>SVT_N.S.6</b>	Space between SVT_N and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
<b>SVT_N.S.6a</b>	Space between SVT_N and ALL_AA in GATE poly direction	$\geq$	0.048	um
<b>SVT_N.S.7</b>	Space between SVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs $\leq$ 0.004um	$\geq$	0.024	um
<b>SVT_N.S.7a</b>	Space between SVT_N and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
<b>SVT_N.S.7b</b>	Space between SVT_N and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
<b>SVT_N.S.8</b>	Space between SVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
<b>SVT_N.S.8a</b>	Space between SVT_N and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
<b>SVT_N.S.9a</b>	Space between SVT_N and GATE (when channel length= 0.016/0.018/0.02um) respectively in S/D direction, (GATE CUT SVT_N is not allowed), except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
<b>SVT_N.S.9b</b>	Space between SVT_N and GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT SVT_N is not allowed)	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>SVT_N.S.10</b>	Space between SVT_N vertical edge (edge length $\leq$ 0.238um between two concave corners with both sides length $\geq$ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
<b>SVT_N.S.11</b>	Space between SVT_N and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space to (ALL_GT NOT P2) $\leq$ 0.04um (SVT_N vertical edge length = 0.073~0.15um, between	$\geq$	0.054	um

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Rule number	Description	Opt.	Design Value	Unit
	two consecutive 90-270 degree corners)			
<b>SVT_N.S.12</b>	Space between SVT_N, SVT_P, LVT_N, LVT_P, HVT_N, HVT_P, LFN_N, LFN_P, ULVT_N and ULVT_P inside GT in GATE poly direction when PRL = 0um, and at least one vertical edge CUT (GTMK1 OR AR))  DRC flags if more than one Vt horizontal edge inside (((GT NOT P2) INTERACT (GTMK1 OR AR)) NOT (AA OR GTMK1)))	=	0	um
<b>SVT_N.EX.1</b>	SVT_N extension outside of ALL_AA (vertical edge abut AA edge is allowed)	≥	0.045	um
<b>SVT_N.EX.2</b>	SVT_N extension outside of ALL_AA in GATE poly direction	≥	0.048	um
<b>SVT_N.EX.3</b>	SVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jog ≤ 0.004um.	≥	0.024	um
<b>SVT_N.EX.4</b>	SVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>SVT_N.EX.5</b>	SVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>SVT_N.EX.6</b>	SVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>SVT_N.EX.7</b>	SVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>SVT_N.EX.8</b>	SVT_N extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>SVT_N.EX.9</b>	SVT_N extension outside of GATE (when channel length = 0.016/0.018/0.02/0.022/0.024 um) respectively INSIDE GT_P96 in S/D direction.	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>SVT_N.EX.10</b>	SVT_N (line-end vertical width ≤ 0.238um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>SVT_N.EX.11</b>	SVT_N extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure ≤ 0.04um by SVT vertical edge (edge length = 0.073~0.15um, between two	≥	0.054	um

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Rule number	Description	Opt.	Design Value	Unit
	consecutive 90-270 degree corners)			
SVT_N.EX.12	(ALL_GT NOT P2) extension outside of SVT_N, except small ALL_GT jogs $\leq 0.004\text{um}$ , Dummy_Cell_WO_IMP, and SVT_N vertical edge CUT (GTMK1 OR AR) (channel length $\leq 0.024\text{um}$ , centerline abut SVT_N vertical edge)	$\geq$	0.083	um
SVT_N.O.1	Overlap of (ALL_GT NOT P2) and SVT_N, except small ALL_GT jogs $\leq 0.004\text{um}$ , Dummy_Cell_WO_IMP, and SVT_N vertical edge CUT (GTMK1 OR AR) (channel length $\leq 0.024\text{um}$ , centerline abut SVT_N vertical edge)	$\geq$	0.083	um
SVT_N.A.1	SVT_N area	$\geq$	0.085	$\text{um}^2$
SVT_N.A.2	SVT_N enclosed area	$\geq$	0.085	$\text{um}^2$
SVT_N.A.3	Area of ((ALL_GT NOT P2) AND SVT_N)	$\geq$	0.00158	$\text{um}^2$
SVT_N.R.1	(ALL_AA interact GT (width $\geq 0.032\text{um}$ )) CUT SVT_N is not allowed.			
SVT_N.R.2	SVT_N overlap with P+AA, SVT_P, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
SVT_N.R.3	(ALL_AA NOT AR) straddle on SVT_N horizontal edge is not allowed.			
SVT_N.R.4	Vertical edge of (SVT_N, LVT_N, ULVT_N, HVT_N, LFN_N) abut (SVT_P, LVT_P, ULVT_P, HVT_P, LFN_P) interact GT is not allowed.			
SVT_N.R.5	(SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, HVT_N, HVT_P, LFN_N, LFN_P) overlap with MARKS is not allowed.			
SVT_N.R.6	((GT NOT P2) NOT INTERACT (GTMK1 OR AR) (channel length $\leq 0.024\text{um}$ )) straddle on vertical edge of SVT_N, SVT_P, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P is not allowed.			
SVT_N.R.7	(DUM_GT NOT P2) CUT SVT_N, SVT_P, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N or LFN_P is not allowed.			
SVT_N.R.8	ALL_GT must be covered by (SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, HVT_N, HVT_P, LFN_N, LFN_P), except			

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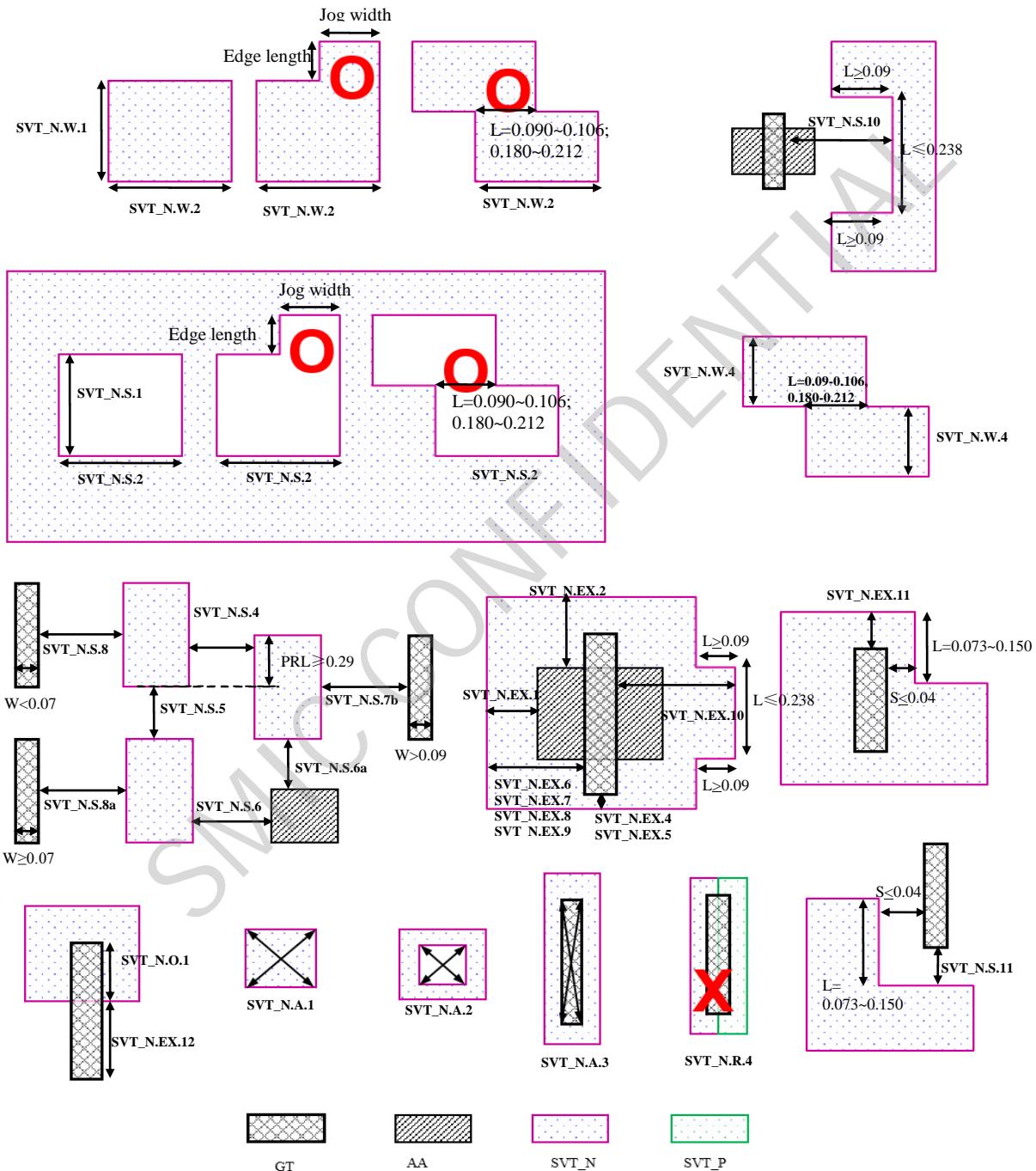
Rule number	Description	Opt.	Design Value	Unit
	INST, DSTR, DMPNP, VARMOS, DG, RESNW, RESP1 DMCMK1, MARKS, OCCD, OCOVL, RESP3t region for 3t resistor bulk regions.			
SVT_N.R.9	ACTIVE must be covered by (SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, HVT_N, HVT_P, LFN_N, LFN_P) , except INST, DSTR, DMPNP, VARMOS, DG, RESNW, DMCMK1, MARKS, OCCD regions.			
SVT_N.R.10	ALL_AA CUT (SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, HVT_N, HVT_P, LFN_N, LFN_P) horizontal edge is not allowed.			

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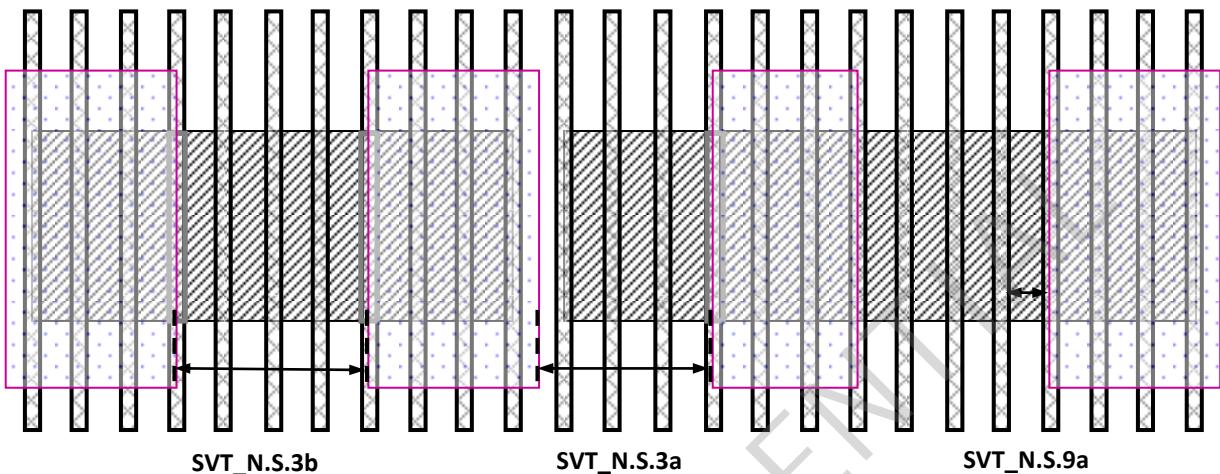


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### 7.2.8 SVT\_P design rules

A drawn SVT\_P layer is needed to define P-type standard Vt MOS devices. SVT\_P is for 0.8V core P-type standard Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
SVT_P.W.1	SVT_P width, single-point-interaction is allowed. DRC waive: 1) SVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.192	um
SVT_P.W.2	SVT_P width in S/D direction, single-point-interaction is allowed. DRC waive: 1) SVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.27	um
SVT_P.W.3	SVT_P width in S/D direction, when SVT_P vertical edge CUT (GTMK1 OR AR) and ABUT HVT_P DRC waive: 1) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.315	um
SVT_P.W.4	SVT_P width in GATE poly direction when SVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	≥	0.238	um
SVT_P.S.1	Space between SVT_P, single-point-interaction is allowed.	≥	0.192	um

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Rule number	Description	Opt.	Design Value	Unit
	DRC waive: 1) SVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
SVT_P.S.2	Space between SVT_P in S/D direction, single-point-interaction is allowed.  DRC waive: 1) SVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.27	um
SVT_P.S.3a	Space between SVT_P in S/D direction, when just one SVT_P vertical edge CUT (GTMK1 OR AR) and abut LVT_P or ULVT_P.  DRC waive: 1) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.315	um
SVT_P.S.3b	Space between SVT_P in S/D direction, when both SVT_P's vertical edges CUT (GTMK1 OR AR) and abut LVT_P or ULVT_P.  DRC waive: 1) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D	≥	0.36	um

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Rule number	Description	Opt.	Design Value	Unit
	direction			
<b>SVT_P.S.4</b>	Space between SVT_P when PRL $\geq$ 0.29um	$\geq$	0.248	um
<b>SVT_P.S.5</b>	SVT_P space in GATE poly direction when SVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
<b>SVT_P.S.6</b>	Space between SVT_P and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
<b>SVT_P.S.6a</b>	Space between SVT_P and ALL_AA in GATE poly direction	$\geq$	0.048	um
<b>SVT_P.S.7</b>	Space between SVT_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs $\leq$ 0.004um)	$\geq$	0.024	um
<b>SVT_P.S.7a</b>	Space between SVT_P and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
<b>SVT_P.S.7b</b>	Space between SVT_P and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
<b>SVT_P.S.8</b>	Space between SVT_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
<b>SVT_P.S.8a</b>	Space between SVT_P and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
<b>SVT_P.S.9a</b>	Space between SVT_P and GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, (GATE CUT SVT_P is not allowed), except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
<b>SVT_P.S.9b</b>	Space between SVT_P and GATE (when channel length = 0.016/0.018/0.02//0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT SVT_P is not allowed)	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>SVT_P.S.10</b>	Space between SVT_P vertical edge (edge length $\leq$ 0.238um between two concave corners with both sides length $\geq$ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
<b>SVT_P.S.11</b>	Space between SVT_P and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space $\leq$ 0.04um (SVT_P vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	$\geq$	0.054	um

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Rule number	Description	Opt.	Design Value	Unit
<b>SVT_P.EX.1</b>	SVT_P extension outside of ALL_AA (vertical edge abut AA edge is allowed)	≥	0.045	um
<b>SVT_P.EX.2</b>	SVT_P extension outside of ALL_AA in GATE poly direction	≥	0.048	um
<b>SVT_P.EX.3</b>	SVT_P extension outside of (ALL_GT width < 0.07um) (ALL_GT NOT P2), except small ALL_GT jog ≤ 0.004um.	≥	0.024	um
<b>SVT_P.EX.4</b>	SVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>SVT_P.EX.5</b>	SVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>SVT_P.EX.6</b>	SVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>SVT_P.EX.7</b>	SVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>SVT_P.EX.8</b>	SVT_P extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>SVT_P.EX.9</b>	SVT_P extension outside of GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>SVT_P.EX.10</b>	SVT_P (line-end vertical width ≤ 0.238um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>SVT_P.EX.11</b>	SVT_P extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure ≤ 0.04um by SVT_P vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>SVT_P.EX.12</b>	(ALL_GT NOT P2) extension outside of SVT_P, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and SVT_P vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut SVT_P vertical edge)	≥	0.083	um
<b>SVT_P.O.1</b>	Overlap of (ALL_GT NOT P2) and SVT_P, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and SVT_P	≥	0.083	um

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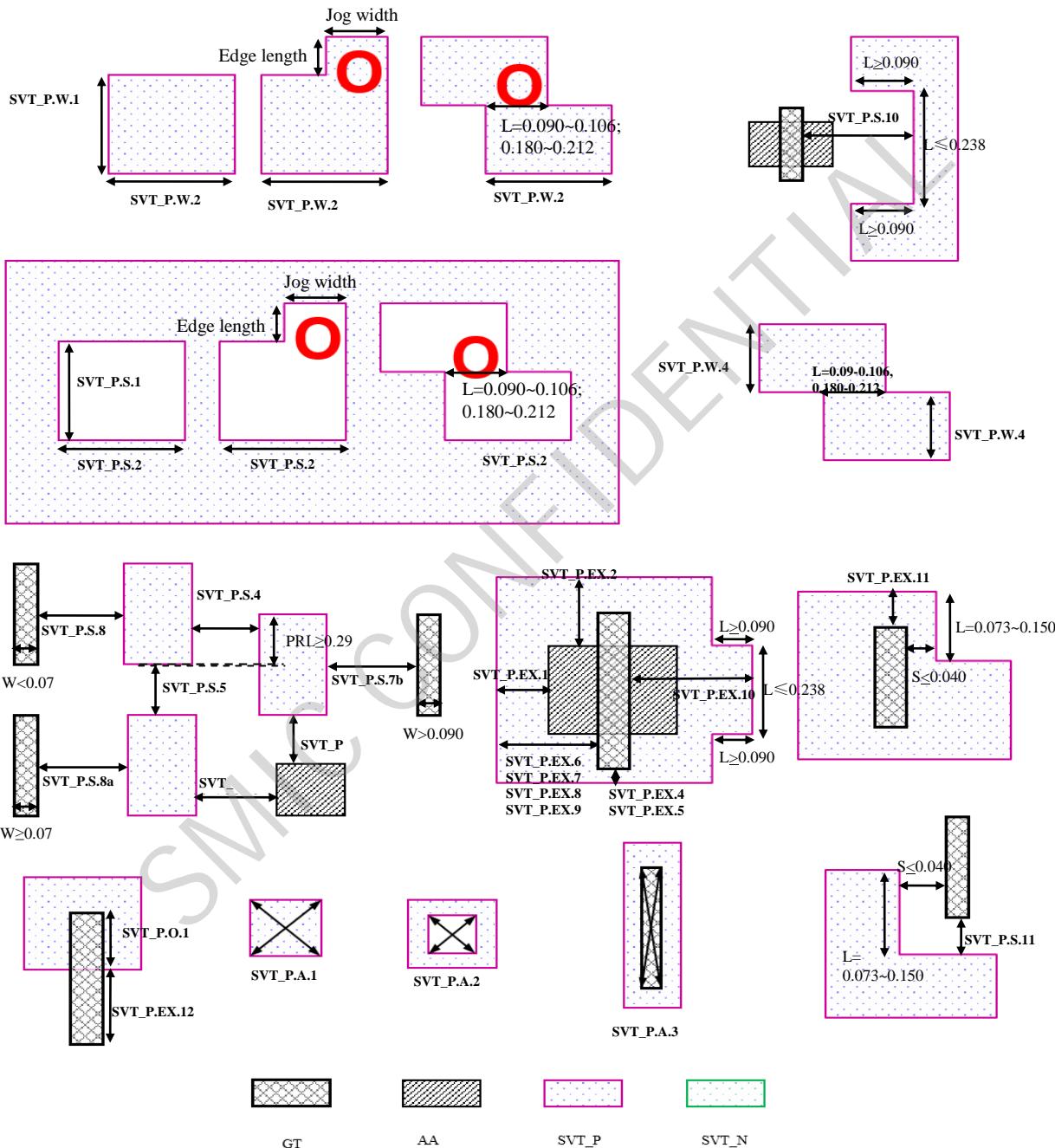
Rule number	Description	Opt.	Design Value	Unit
	vertical edge CUT (GTMK1 OR AR) (Channel length $\leq$ 0.024um, centerline abut SVT_P vertical edge)			
<b>SVT_P.A.1</b>	SVT_P area	$\geq$	0.085	um <sup>2</sup>
<b>SVT_P.A.2</b>	SVT_P enclosed area	$\geq$	0.085	um <sup>2</sup>
<b>SVT_P.A.3</b>	Area of ((ALL_GT NOT P2) AND SVT_P)	$\geq$	0.00158	um <sup>2</sup>
<b>SVT_P.R.1</b>	(ALL_AA interact GT (width $\geq$ 0.032um)) CUT SVT_P is not allowed.			
<b>SVT_P.R.2</b>	SVT_P overlap with N+AA, SVT_N, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
<b>SVT_P.R.3</b>	(ALL_AA NOT AR) straddle on SVT_P horizontal edge is not allowed.			

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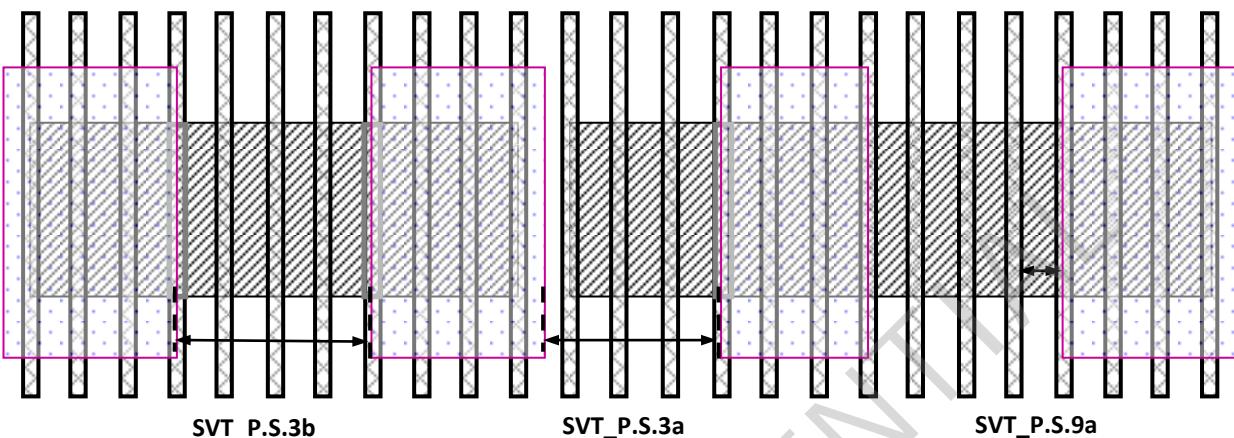


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### 7.2.9 HVT\_N design rules

A drawn HVT\_N layer is needed to define N-type high Vt MOS devices. HVT\_N is for 0.8V core N-type high Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
HVT_N.W.1	HVT_N width, single-point-interaction is allowed.  DRC waive: 1) HVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.192	um
HVT_N.W.2	HVT_N width in S/D direction, single-point-interaction is allowed.  DRC waive: 1) HVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.27	um
HVT_N.W.3	HVT_N width in GATE poly direction when HVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	≥	0.238	um
HVT_N.S.1	Space between HVT_N, single-point-interaction is allowed.  DRC waive: 1) HVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.192	um

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Rule number	Description	Opt.	Design Value	Unit
HVT_N.S.2	Space between HVT_N in S/D direction, single-point-interaction is allowed.  DRC waive: 1) HVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
HVT_N.S.3a	Space between HVT_N in S/D direction, when just one HVT_N's vertical edge CUT (GTMK1 OR AR)  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.315	um
HVT_N.S.3b	Space between HVT_N in S/D direction, when both HVT_N's vertical edge CUT (GTMK1 OR AR)  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.36	um
HVT_N.S.4	Space between HVT_N when PRL $\geq$ 0.29um	$\geq$	0.248	um
HVT_N.S.5	HVT_N space in GATE poly direction when HVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
HVT_N.S.6	Space between HVT_N and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
HVT_N.S.6a	Space between HVT_N and ALL_AA in GATE poly direction	$\geq$	0.048	um

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Rule number	Description	Opt.	Design Value	Unit
<b>HVT_N.S.7</b>	Space between HVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs ≤ 0.004um.	≥	0.024	um
<b>HVT_N.S.7a</b>	Space between HVT_N and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>HVT_N.S.7b</b>	Space between HVT_N and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>HVT_N.S.8</b>	Space between HVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>HVT_N.S.8a</b>	Space between HVT_N and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>HVT_N.S.9a</b>	Space between HVT_N and GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction (GATE CUT HVT_N is not allowed), except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>HVT_N.S.9b</b>	Space between HVT_N and GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT HVT_N is not allowed)	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>HVT_N.S.10</b>	Space between HVT_N vertical edge (edge length ≤ 0.238um between two concave corners with both sides length ≥ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>HVT_N.S.11</b>	Space between HVT_N and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space ≤ 0.04um (HVT_N vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>HVT_N.EX.1</b>	HVT_N extension outside of ALL_AA (vertical edge abut AA edge is allowed)	≥	0.045	um
<b>HVT_N.EX.2</b>	HVT_N extension outside of ALL_AA in GATE poly direction	≥	0.048	um
<b>HVT_N.EX.3</b>	HVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jog ≤ 0.004um.	≥	0.024	um
<b>HVT_N.EX.4</b>	HVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>HVT_N.EX.5</b>	HVT_N extension outside of (ALL_GT NOT P2) (ALL_GT	≥	0.058	um

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Rule number	Description	Opt.	Design Value	Unit
	width > 0.09um)			
<b>HVT_N.EX.6</b>	HVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>HVT_N.EX.7</b>	HVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>HVT_N.EX.8</b>	HVT_N extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction., except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>HVT_N.EX.9</b>	HVT_N extension outside GATE (when channel length = 0.016/0.018/ 0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>HVT_N.EX.10</b>	HVT_N (line-end vertical width ≤ 0.238um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>HVT_N.EX.11</b>	HVT_N extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure ≤ 0.04um by HVT_N vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>HVT_N.EX.12</b>	(ALL_GT NOT P2) extension outside of HVT_N, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and HVT_N vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut HVT_N vertical edge)	≥	0.083	um
<b>HVT_N.O.1</b>	Overlap of (ALL_GT NOT P2) and HVT_N, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and HVT_N vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut HVT_N vertical edge)	≥	0.083	um
<b>HVT_N.A.1</b>	HVT_N area	≥	0.085	um <sup>2</sup>
<b>HVT_N.A.2</b>	HVT_N enclosed area	≥	0.085	um <sup>2</sup>
<b>HVT_N.A.3</b>	Area of ((ALL_GT NOT P2) AND HVT_N)	≥	0.00158	um <sup>2</sup>
<b>HVT_N.R.1</b>	(ALL_AA interact GT (width ≥ 0.032um)) CUT HVT_N is not allowed.			

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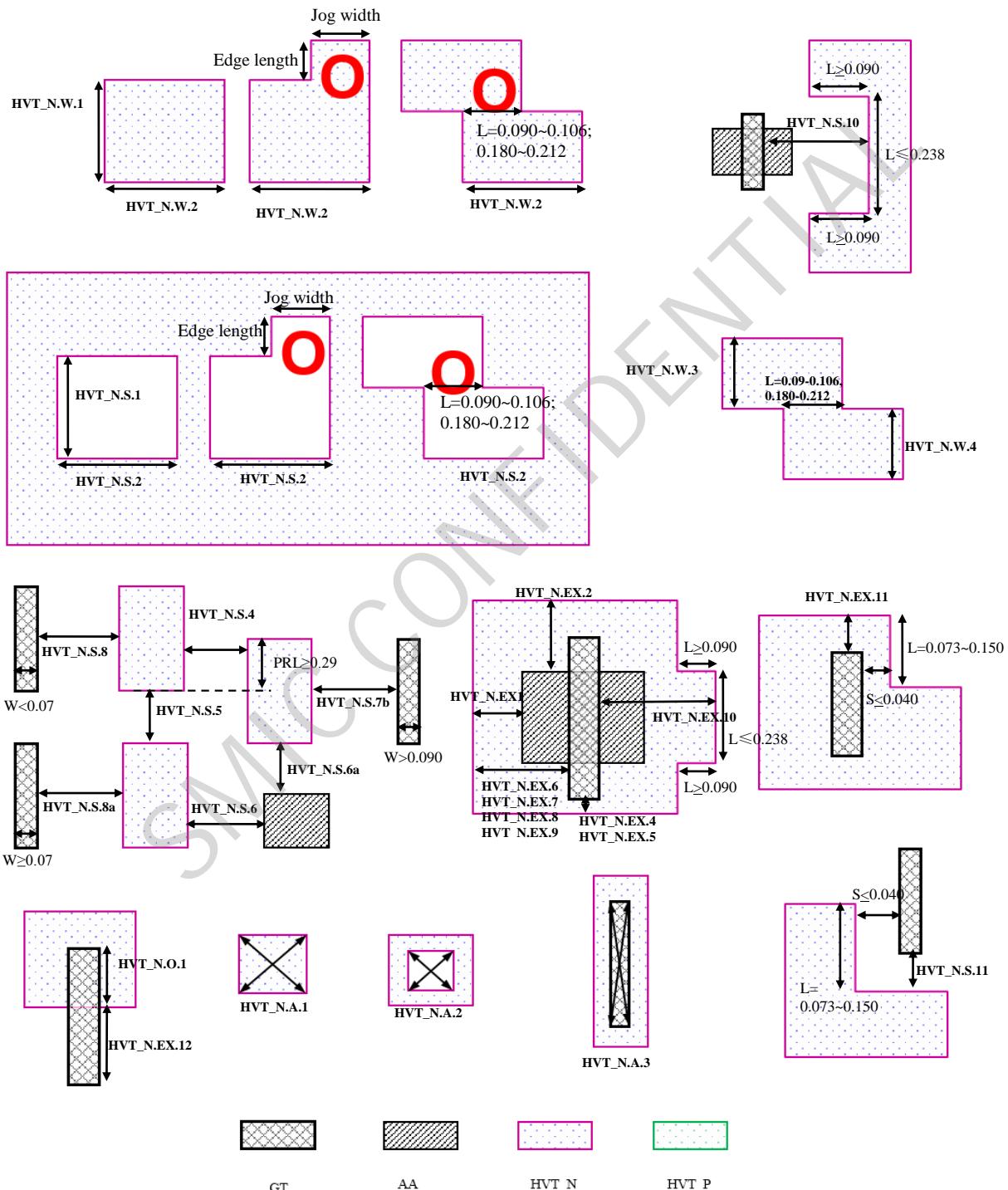
Rule number	Description	Opt.	Design Value	Unit
HVT_N.R.2	HVT_N overlap with P+AA, SVT_N, SVT_P, HVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
HVT_N.R.3	(ALL_AA NOT AR) straddle on HVT_N horizontal edge is not allowed.			

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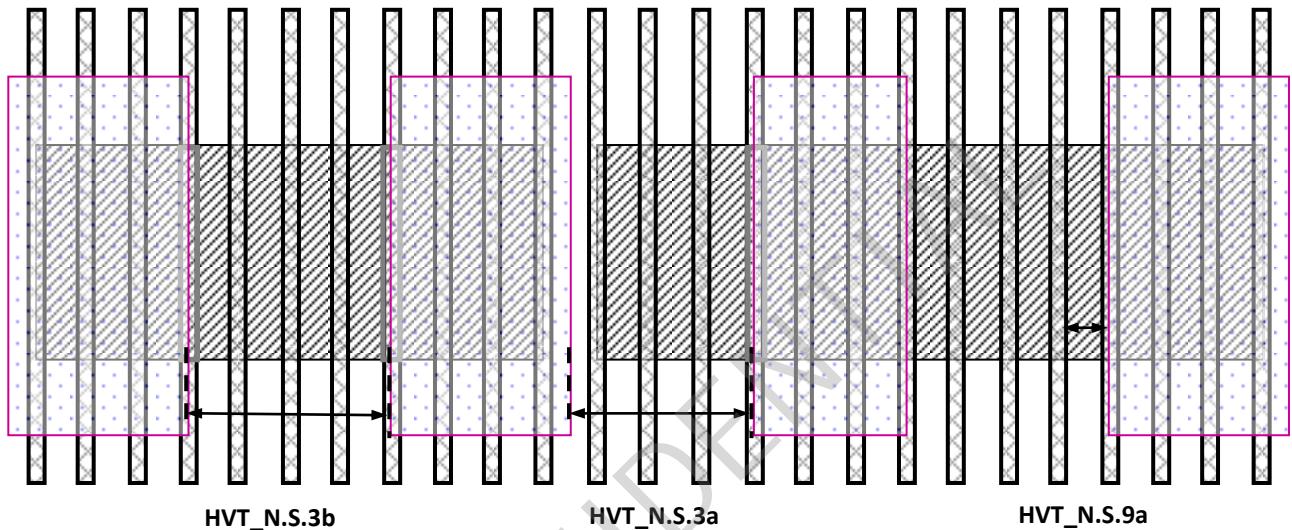


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### 7.2.10 HVT\_P deisgn rules

A drawn HVT\_P layer is needed to define P-type low Vt MOS devices. HVT\_P is for 0.8V core P-type low Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
HVT_P.W.1	<p>HVT_P width, single-point-interaction is allowed. DRC waive: 1) HVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</p>	$\geq$	0.192	um
HVT_P.W.2	<p>HVT_P width in S/D direction, single-point-interaction is allowed. DRC waive: 1) HVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</p>	$\geq$	0.27	um
HVT_P.W.3	<p>HVT_P width in GATE poly direction when HVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)</p>	$\geq$	0.238	um
HVT_P.S.1	<p>Space between HVT_P, single-point-interaction is allowed. DRC waive: 1) HVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</p>	$\geq$	0.192	um

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Rule number	Description	Opt.	Design Value	Unit
HVT_P.S.2	Space between HVT_P in S/D direction, single-point-interaction is allowed.  DRC waive: 1) HVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
HVT_P.S.3a	Space between HVT_P when just one vertical edge CUT (GTMK1 OR AR) in S/D direction.  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.315	um
HVT_P.S.3b	Space between HVT_P when both vertical edge CUT (GTMK1 OR AR) in S/D direction.  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.36	um
HVT_P.S.4	Space between HVT_P when PRL $\geq$ 0.29um	$\geq$	0.248	um
HVT_P.S.5	Space between HVT_P in GATE poly direction when HVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
HVT_P.S.6	Space between HVT_P and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
HVT_P.S.6a	Space between HVT_P and ALL_AA in GATE poly direction	$\geq$	0.048	um

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Rule number	Description	Opt.	Design Value	Unit
<b>HVT_P.S.7</b>	Space between HVT_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs ≤ 0.004um.	≥	0.024	um
<b>HVT_P.S.7a</b>	Space between HVT_P and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>HVT_P.S.7b</b>	Space between HVT_P and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>HVT_P.S.8</b>	Space between HVT_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>HVT_P.S.8a</b>	Space between HVT_P and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>HVT_P.S.9a</b>	Space between HVT_P and GATE (when channel length= 0.016/0.018/0.02um) respectively in S/D direction (GATE CUT HVT_P is not allowed), except GT_P96 region	≥	0.082/0.081/0.08	um
<b>HVT_P.S.9b</b>	Space between HVT_P and GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT HVT_P is not allowed)	≥	0.088/0.087/0.086/0.085/0.084	um
<b>HVT_P.S.10</b>	Space between HVT_P vertical edge (edge length ≤ 0.238um between two concave corners with both sides length ≥ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>HVT_P.S.11</b>	Space between HVT_P and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space ≤ 0.04um (HVT_P vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>HVT_P.EX.1</b>	HVT_P extension outside of ALL_AA (vertical edge abut AA edge is allowed)	≥	0.045	um
<b>HVT_P.EX.2</b>	HVT_P extension outside of ALL_AA in GATE poly direction	≥	0.048	um
<b>HVT_P.EX.3</b>	HVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs ≤ 0.004um	≥	0.024	um
<b>HVT_P.EX.4</b>	HVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>HVT_P.EX.5</b>	HVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um

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Rule number	Description	Opt.	Design Value	Unit
<b>HVT_P.EX.6</b>	HVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>HVT_P.EX.7</b>	HVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>HVT_P.EX.8</b>	HVT_P outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	≥	0.082/0.081/0.08	um
<b>HVT_P.EX.9</b>	HVT_P extension outside of GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction	≥	0.088/0.087/0.086/0.085/0.084	um
<b>HVT_P.EX.10</b>	HVT_P (line-end vertical width ≤ 0.238um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>HVT_P.EX.11</b>	HVT_P extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure ≤ 0.04um by HVT_P vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>HVT_P.EX.12</b>	(ALL_GT NOT P2) extension outside of HVT_P, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and HVT_P vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut HVT_P vertical edge)	≥	0.083	um
<b>HVT_P.O.1</b>	Overlap of (ALL_GT NOT P2) and HVT_P, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and HVT_P vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut HVT_P vertical edge)	≥	0.083	um
<b>HVT_P.A.1</b>	HVT_P area	≥	0.085	um <sup>2</sup>
<b>HVT_P.A.2</b>	HVT_P enclosed area	≥	0.085	um <sup>2</sup>
<b>HVT_P.A.3</b>	Area of ((ALL_GT NOT P2) AND HVT_P)	≥	0.00158	um <sup>2</sup>
<b>HVT_P.R.1</b>	(ALL_AA interact GT (width ≥ 0.032um)) CUT HVT_P is not allowed			
<b>HVT_P.R.2</b>	HVT_P overlap with N+AA, SVT_N, SVT_P, HVT_N, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude			

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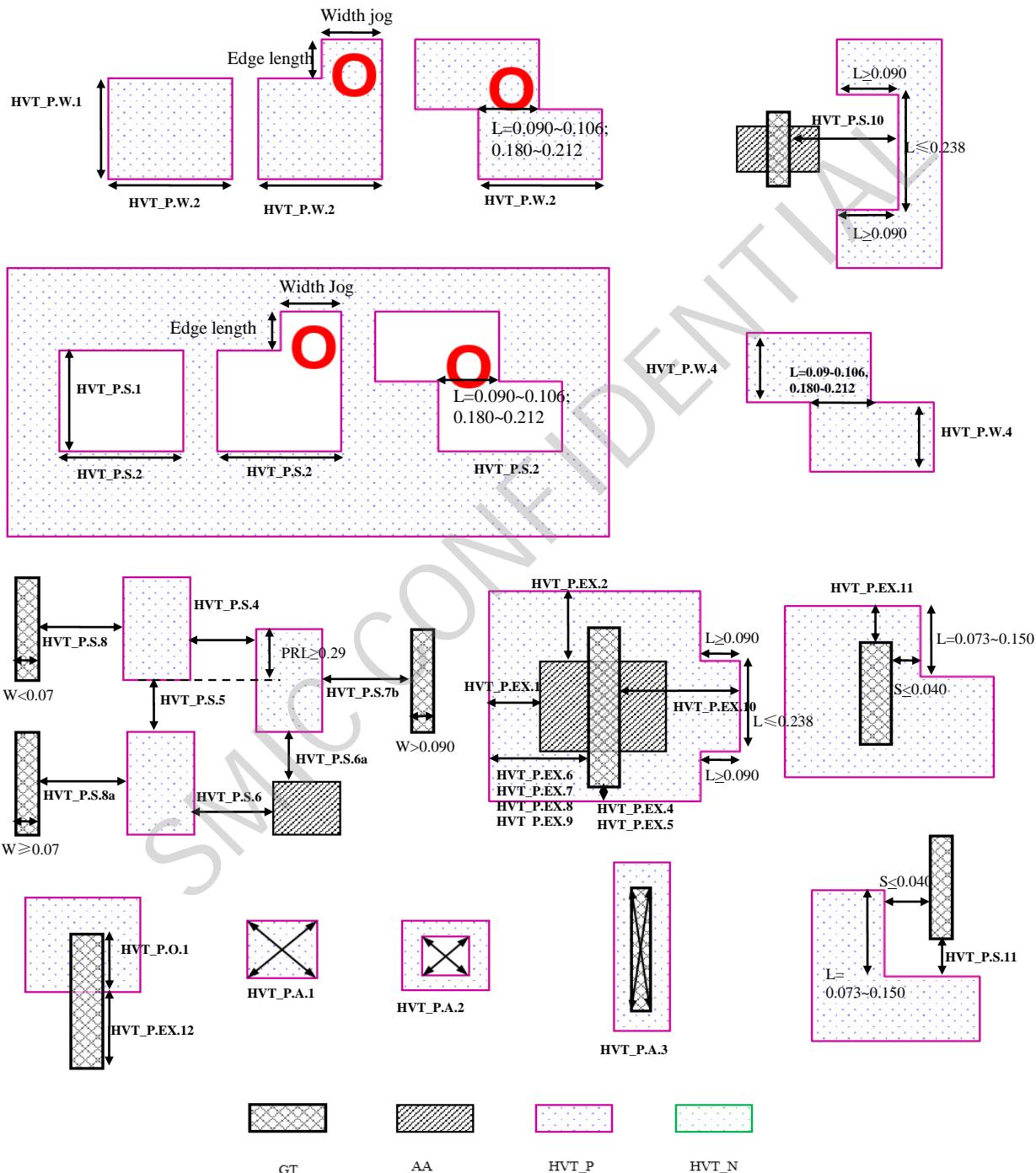
Rule number	Description	Opt.	Design Value	Unit
	OCCD region.			
<b>HVT_P.R.3</b>	(ALL_AA NOT AR) straddle on HVT_P horizontal edge is not allowed.			

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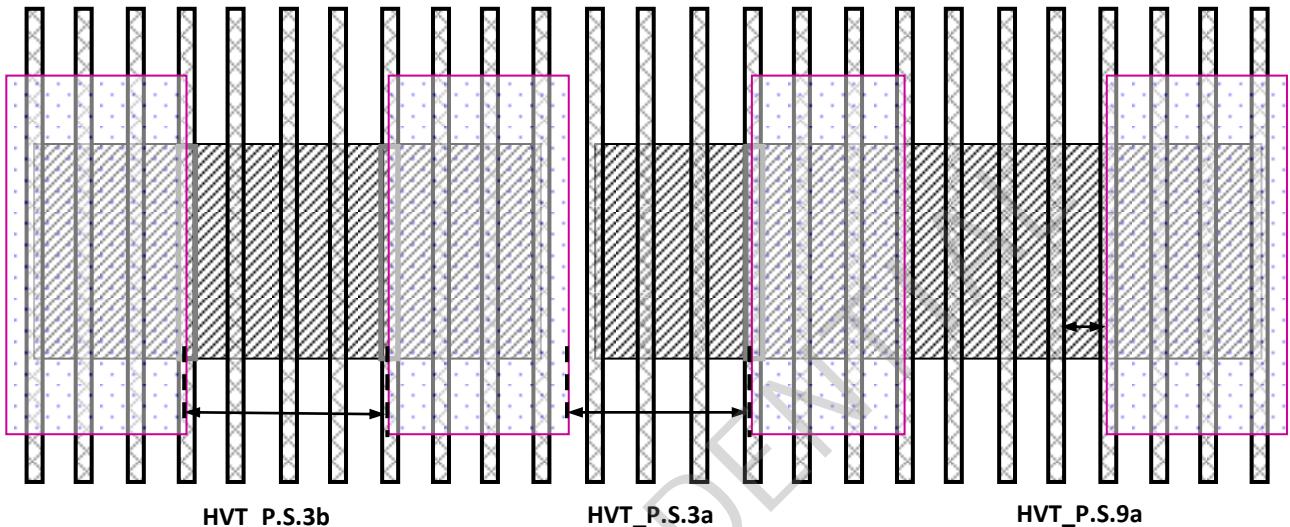


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### 7.2.11 LVT\_N design rules

A drawn LVT\_N layer is needed to define N-type low Vt MOS devices. LVT\_N is for 0.8V core N-type low Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
LVT_N.W.1	<p>LVT_N width, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ol style="list-style-type: none"> <li>1) LVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ol>	$\geq$	0.192	um
LVT_N.W.2	<p>LVT_N width in S/D direction, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ol style="list-style-type: none"> <li>1) LVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ol>	$\geq$	0.27	um
LVT_N.W.3a	<p>LVT_N width in S/D direction when just one LVT_N vertical edge CUT (GTMK1 OR AR), and ABUT SVT_N or HVT_N</p> <p>DRC waive:</p> <ol style="list-style-type: none"> <li>1) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ol>	$\geq$	0.315	um
LVT_N.W.3b	<p>LVT_N width in S/D direction when both two LVT_N's vertical edges CUT (GTMK1 OR AR) and ABUT SVT_N or HVT_N</p> <p>DRC waive:</p> <ol style="list-style-type: none"> <li>1) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in</li> </ol>	$\geq$	0.36	um

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Rule number	Description	Opt.	Design Value	Unit
	S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
LVT_N.W.4	LVT_N width in GATE poly direction when LVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	≥	0.238	um
LVT_N.S.1	Space between LVT_N, single-point-interaction is allowed. DRC waive: 1) LVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.192	um
LVT_N.S.2	Space between LVT_N in S/D direction, single-point-interaction is allowed. DRC waive: 1) LVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.27	um
LVT_N.S.3a	Space between LVT_N when just one vertical edge CUT (GTMK1 OR AR), and ABUT ULVT_N in S/D direction. DRC waive: 1) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.315	

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Rule number	Description	Opt.	Design Value	Unit
LVT_N.S.3b	Space between LVT_N when both LVT_N's vertical edge CUT (GTMK1 OR AR) and ABUT ULVT_N in S/D direction.  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.36	
LVT_N.S.4	Space between LVT_N when PRL $\geq$ 0.29um	$\geq$	0.248	um
LVT_N.S.5	LVT_N space in GATE poly direction when LVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
LVT_N.S.6	Space between LVT_N and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
LVT_N.S.6a	Space between LVT_N and ALL_AA in GATE poly direction	$\geq$	0.048	um
LVT_N.S.7	Space between LVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs $\leq$ 0.004um	$\geq$	0.024	um
LVT_N.S.7a	Space between LVT_N and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
LVT_N.S.7b	Space between LVT_N and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
LVT_N.S.8	Space between LVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
LVT_N.S.8a	Space between LVT_N and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
LVT_N.S.9a	Space between LVT_N and GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction (GATE CUT LVT_N is not allowed), except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
LVT_N.S.9b	Space between LVT_N and GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT LVT_N is not allowed)	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um

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Rule number	Description	Opt.	Design Value	Unit
LVT_N.S.10	Space between LVT_N vertical edge (edge length $\leq$ 0.238um between two concave corners with both sides length $\geq$ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
LVT_N.S.11	Space between LVT_N and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space $\leq$ 0.04um (LVT_N vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree coners)	$\geq$	0.054	um
LVT_N.EX.1	LVT_N extension outside of ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
LVT_N.EX.2	LVT_N extension outside of ALL_AA in GATE poly direction	$\geq$	0.048	um
LVT_N.EX.3	LVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width $<$ 0.07um), except small ALL_GT jog $\leq$ 0.004um	$\geq$	0.024	um
LVT_N.EX.4	LVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
LVT_N.EX.5	LVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width $>$ 0.09um)	$\geq$	0.058	um
LVT_N.EX.6	LVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width $<$ 0.07um) in S/D direction	$\geq$	0.035	um
LVT_N.EX.7	LVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
LVT_N.EX.8	LVT_N extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	$\geq$	0.082/0.081/0.08	um
LVT_N.EX.9	LVT_N extension outside GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction	$\geq$	0.088/0.087/0.086/0.085/0.084	um
LVT_N.EX.10	LVT_N (line-end vertical width $\leq$ 0.238um between two consecutive 90-90 degree corners with both sides length $\geq$ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
LVT_N.EX.11	LVT_N extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure $\leq$ 0.04um by LVT_N vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	$\geq$	0.054	um

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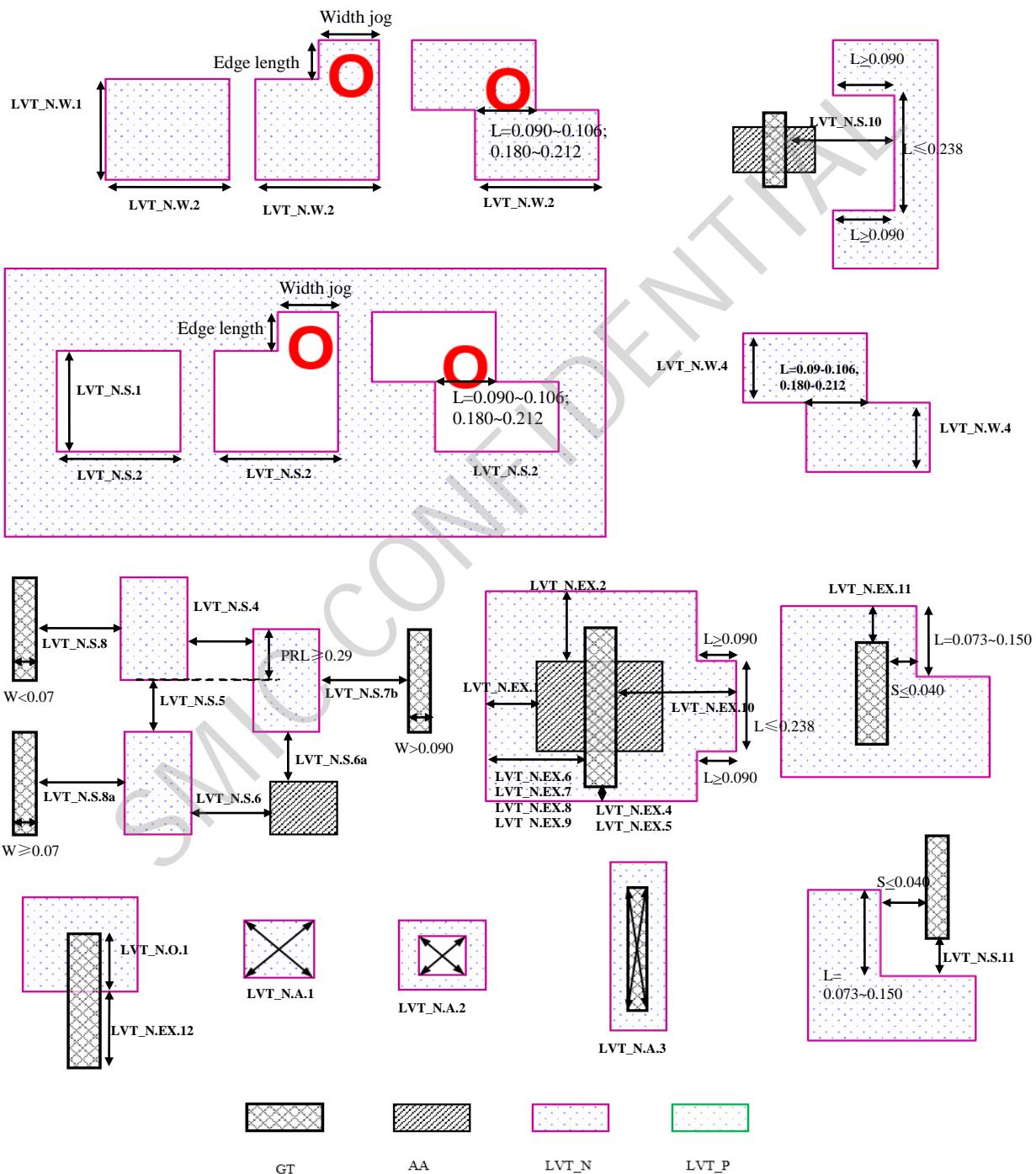


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Rule number	Description	Opt.	Design Value	Unit
LVT_N.EX.12	(ALL_GT NOT P2) extension outside of LVT_N, except small ALL_GT jogs $\leq 0.004\text{um}$ , Dummy_Cell_WO_IMP, and LVT_N vertical edge CUT (GTMK1 OR AR) (Channel length $\leq 0.024\text{um}$ , centerline abut LVT_N vertical edge)	$\geq$	0.083	um
LVT_N.O.1	Overlap of (ALL_GT NOT P2) and LVT_N, except small ALL_GT jogs $\leq 0.004\text{um}$ , Dummy_Cell_WO_IMP, and LVT_N vertical edge CUT (GTMK1 OR AR) (Channel length $\leq 0.024\text{um}$ , centerline abut LVT_N vertical edge)	$\geq$	0.083	um
LVT_N.A.1	LVT_N area	$\geq$	0.085	$\text{um}^2$
LVT_N.A.2	LVT_N enclosed area	$\geq$	0.085	$\text{um}^2$
LVT_N.A.3	Area of ((ALL_GT NOT P2) AND LVT_N)	$\geq$	0.00158	$\text{um}^2$
LVT_N.R.1	(ALL_AA interact GT (width $\geq 0.032\text{um}$ )) CUT LVT_N is not allowed			
LVT_N.R.2	LVT_N overlap with P+AA, SVT_N, SVT_P, HVT_N, HVT_P, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
LVT_N.R.3	(ALL_AA NOT AR) straddle on LVT_P horizontal edge is not allowed.			

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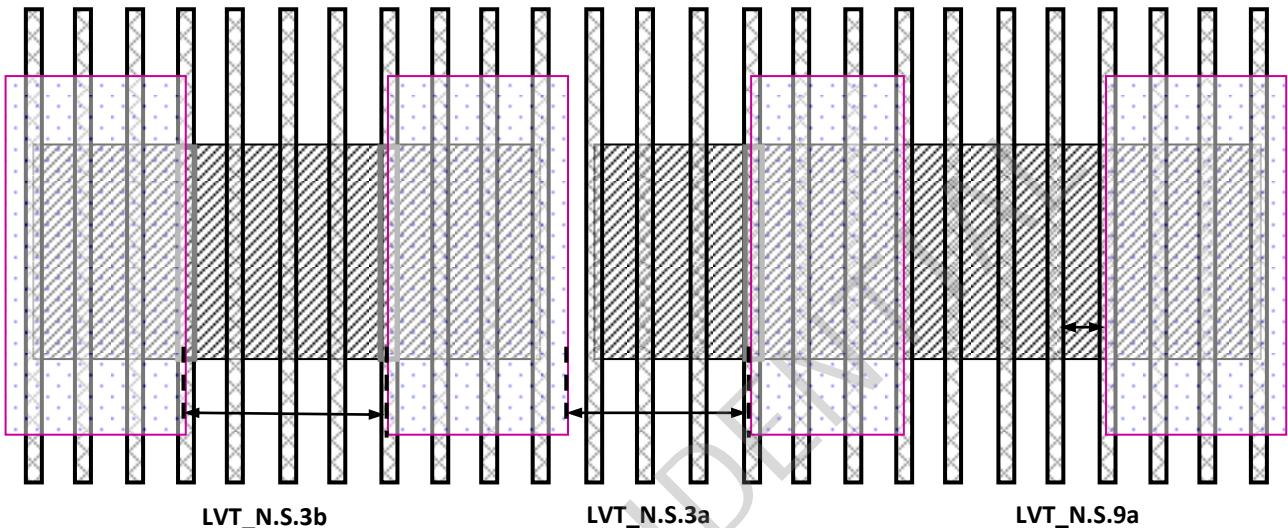


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### 7.2.12 LVT\_P design rules

A drawn LVT\_P layer is needed to define P-type low Vt MOS devices. LVT\_P is for 0.8V core P-type low Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
LVT_P.W.1	<p>LVT_P width, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) LVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.192	um
LVT_P.W.2	<p>LVT_P width in S/D direction, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) LVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.27	um
LVT_P.W.3	<p>LVT_P width in S/D direction when just one LVT_P vertical edge CUT (GTMK1 OR AR) and ABUT SVT_P or HVT_P</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.315	um
LVT_P.W.3a	<p>LVT_P width in S/D direction when both LVT_P vertical edge CUT (GTMK1 OR AR) and ABUT SVT_P or HVT_P</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in</li> </ul>	$\geq$	0.36	um

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Rule number	Description	Opt.	Design Value	Unit
	S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
LVT_P.W.4	LVT_P width in GATE poly direction when LVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	≥	0.238	um
LVT_P.S.1	Space between LVT_P, single-point-interaction is allowed. DRC waive: 1) LVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.192	um
LVT_P.S.2	Space between LVT_P in S/D direction, single-point-interaction is allowed. DRC waive: 1) LVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.27	um
LVT_P.S.3a	Space between LVT_P in S/D direction when just one LVT_P vertical edge CUT (GTMK1 OR AR), ABUT ULVT_P. DRC waive: 1) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.315	um

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Rule number	Description	Opt.	Design Value	Unit
LVT_P.S.3b	Space between LVT_P in S/D direction when both LVT_P vertical edge CUT (GTMK1 OR AR), ABUT ULVT_P.  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction  2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.36	um
LVT_P.S.4	Space between LVT_P when PRL $\geq$ 0.29um	$\geq$	0.248	um
LVT_P.S.5	LVT_P space in GATE poly direction when LVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
LVT_P.S.6	Space between LVT_P and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
LVT_P.S.6a	Space between LVT_P and ALL_AA in GATE poly direction	$\geq$	0.048	um
LVT_P.S.7	Space between LVT_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs $\leq$ 0.004um	$\geq$	0.024	um
LVT_P.S.7a	Space between LVT_P and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
LVT_P.S.7b	Space between LVT_P and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
LVT_P.S.8	Space between LVT_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
LVT_P.S.8a	Space between LVT_P and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
LVT_P.S.9a	Space between LVT_P and GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction. (GATE CUT LVT_P is not allowed), except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
LVT_P.S.9b	Space between LVT_P and to GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT LVT_P is not allowed)	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um

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Rule number	Description	Opt.	Design Value	Unit
LVT_P.S.10	Space between LVT_P vertical edge (edge length $\leq$ 0.238um between two concave corners with both sides length $\geq$ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
LVT_P.S.11	Space between LVT_P and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space $\leq$ 0.04um (LVT_P vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree coners)	$\geq$	0.054	um
LVT_P.EX.1	LVT_P extension outside of ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
LVT_P.EX.2	LVT_P extension outside of ALL_AA in GATE poly direction	$\geq$	0.048	um
LVT_P.EX.3	LVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jog $\leq$ 0.004um.	$\geq$	0.024	um
LVT_P.EX.4	LVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
LVT_P.EX.5	LVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
LVT_P.EX.6	LVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
LVT_P.EX.7	LVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
LVT_P.EX.8	LVT_P extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
LVT_P.EX.9	LVT_P extension outside of GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
LVT_P.EX.10	LVT_P (line-end vertical width $\leq$ 0.238um between two consecutive 90-90 degree corners with both sides length $\geq$ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
LVT_P.EX.11	LVT_P extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent enclosure $\leq$ 0.04um by LVT_P vertical edge (edge length = 0.073~0.15um, between two consecutive	$\geq$	0.054	um

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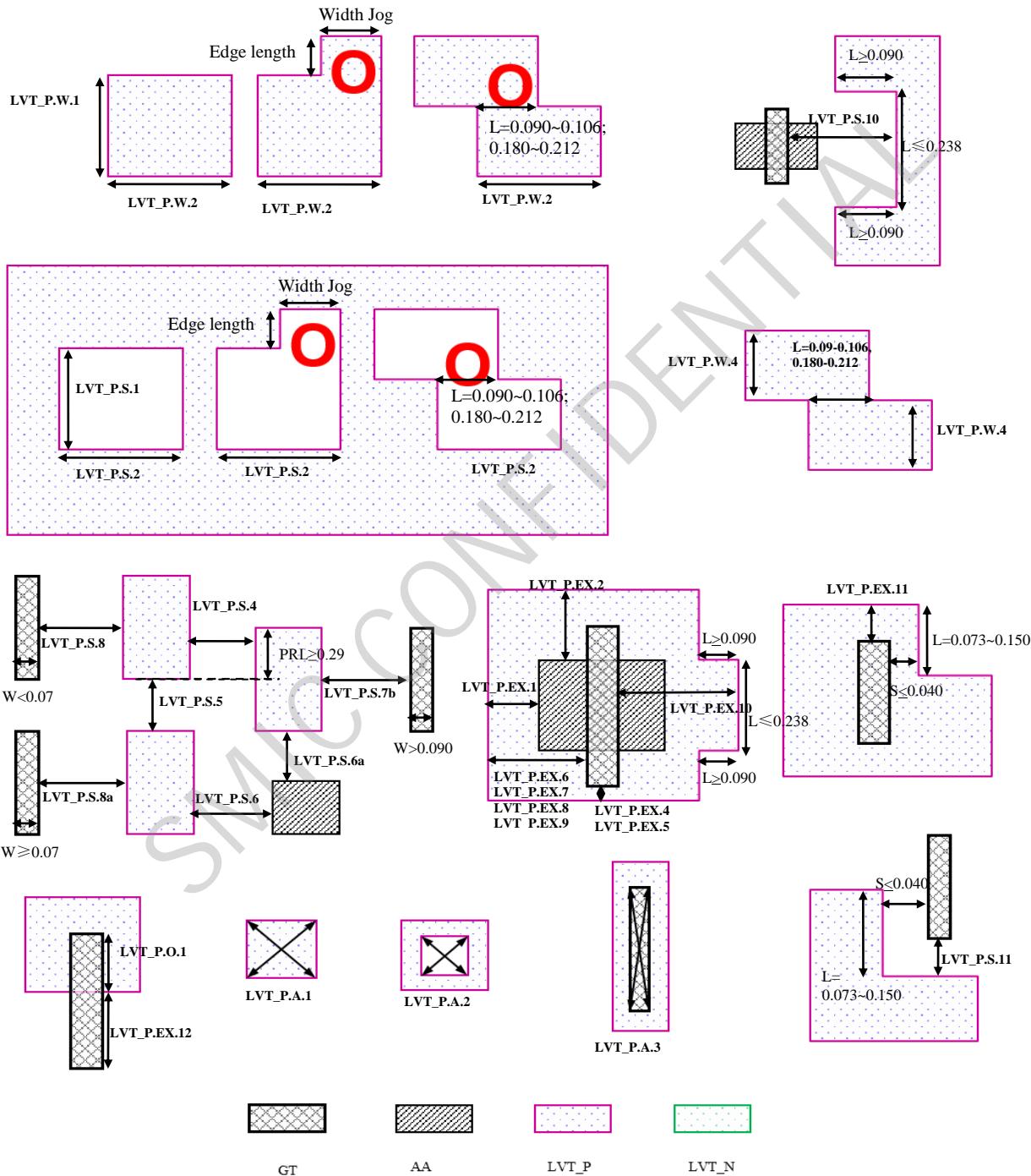


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Rule number	Description	Opt.	Design Value	Unit
	90-270 degree corners)			
LVT_P.EX.12	(ALL_GT NOT P2) extension outside of LVT_P, except small ALL_GT jogs $\leq 0.004\text{um}$ , Dummy_Cell_WO_IMP, and LVT_P vertical edge CUT (GTMK1 OR AR) (Channel length $\leq 0.024\text{um}$ , centerline abut LVT_P vertical edge)	$\geq$	0.083	um
LVT_P.O.1	Overlap of (ALL_GT NOT P2) and LVT_P, except small ALL_GT jogs $\leq 0.004\text{um}$ , Dummy_Cell_WO_IMP, and LVT_P vertical edge CUT (GTMK1 OR AR) (Channel length $\leq 0.024\text{um}$ , centerline abut LVT_P vertical edge)	$\geq$	0.083	um
LVT_P.A.1	LVT_P area	$\geq$	0.085	$\text{um}^2$
LVT_P.A.2	LVT_P enclosed area	$\geq$	0.085	$\text{um}^2$
LVT_P.A.3	Area of ((ALL_GT NOT P2) AND LVT_P)	$\geq$	0.00158	$\text{um}^2$
LVT_P.R.1	(ALL_AA interact GT (width $\geq 0.032\text{um}$ )) CUT LVT_P is not allowed.			
LVT_P.R.2	LVT_P overlap with N+AA, SVT_N, SVT_P, HVT_N, HVT_P, LVT_N, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
LVT_P.R.3	(ALL_AA NOT AR) straddle on LVT_P horizontal edge is not allowed.			

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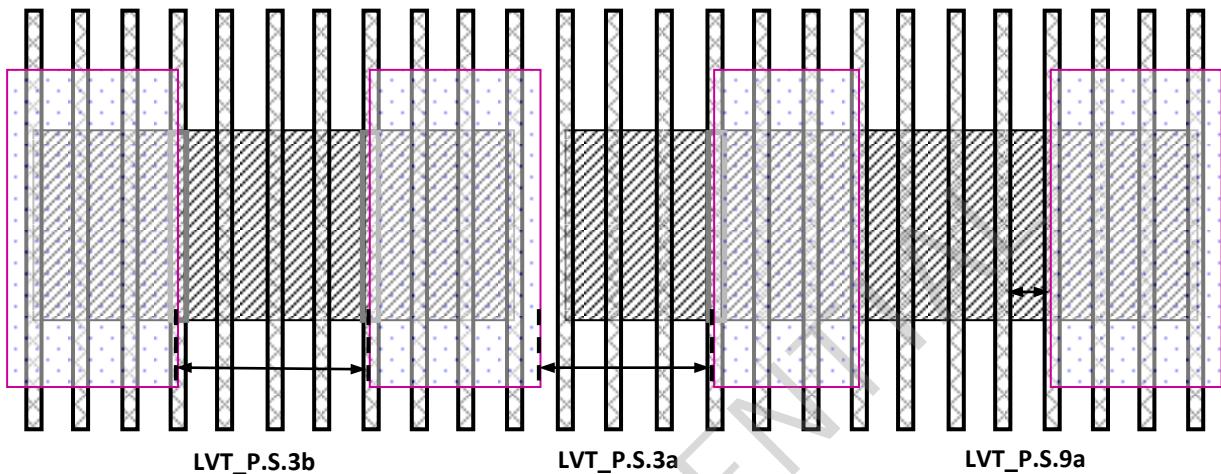


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### 7.2.13 ULVT\_N design rules

A drawn ULVT\_N layer is needed to define N-type ultra low Vt MOS devices. ULVT\_N is for 0.8V core N-type ultra low Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
ULVT_N.W.1	<p>ULVT_N width, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) ULVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.192	um
ULVT_N.W.2	<p>ULVT_N width in S/D direction, single-point-interaction is allowed.</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) ULVT_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um</li> <li>2) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.27	um
ULVT_N.W.3a	<p>ULVT_N width when just one vertical edge CUT (GTMK1 OR AR) in S/D direction</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction</li> <li>2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction</li> </ul>	$\geq$	0.315	um
ULVT_N.W.3b	<p>ULVT_N width when both vertical ULVT_N edges CUT (GTMK1 OR AR) in S/D direction</p> <p>DRC waive:</p> <ul style="list-style-type: none"> <li>1) Jog width adjacent to edge (length <math>\leq</math> 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um</li> </ul>	$\geq$	0.360	um

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Rule number	Description	Opt.	Design Value	Unit
	in S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
<b>ULVT_N.W.4</b>	ULVT_N width in GATE poly direction when ULVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	$\geq$	0.238	um
<b>ULVT_N.S.1</b>	Space between ULVT_N, single-point-interaction is allowed. DRC waive: 1) ULVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.192	um
<b>ULVT_N.S.2</b>	Space between ULVT_N in S/D direction, single-point-interaction is allowed. DRC waive: 1) ULVT_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
<b>ULVT_N.S.4</b>	Space between ULVT_N when PRL $\geq$ 0.29um	$\geq$	0.248	um
<b>ULVT_N.S.5</b>	Space between ULVT_N in GATE poly direction when ULVT_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
<b>ULVT_N.S.6</b>	Space between ULVT_N and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
<b>ULVT_N.S.6a</b>	Space between ULVT_N and ALL_AA in GATE poly direction	$\geq$	0.048	um

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Rule number	Description	Opt.	Design Value	Unit
<b>ULVT_N.S.7</b>	Space between ULVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jog ≤ 0.004um.	≥	0.024	um
<b>ULVT_N.S.7a</b>	Space between ULVT_N and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>ULVT_N.S.7b</b>	Space between ULVT_N and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>ULVT_N.S.8</b>	Space between ULVT_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>ULVT_N.S.8a</b>	Space between ULVT_N and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>ULVT_N.S.9a</b>	Space between ULVT_N and GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region (GATE CUT ULVT_N is not allowed)	≥	0.082/ 0.081/ 0.08	um
<b>ULVT_N.S.9b</b>	Space between ULVT_N and GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT ULVT_N is not allowed)	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>ULVT_N.S.10</b>	Space between ULVT_N vertical edge (edge length ≤ 0.238um between two concave corners with both sides length ≥ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>ULVT_N.S.11</b>	Space between ULVT_N and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space ≤ 0.040um (ULVT_N vertical edge edge length = 0.073~0.15um, between two consecutive 90-270 degree coners)	≥	0.054	um
<b>ULVT_N.EX.1</b>	ULVT_N extension outside of ALL_AA (vertical edge abut AA edge is allowed)	≥	0.045	um
<b>ULVT_N.EX.2</b>	ULVT_N extension outside of ALL_AA in GATE poly direction	≥	0.048	um
<b>ULVT_N.EX.3</b>	ULVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jog ≤ 0.004um.	≥	0.024	um
<b>ULVT_N.EX.4</b>	ULVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um

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Rule number	Description	Opt.	Design Value	Unit
<b>ULVT_N.EX.5</b>	ULVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>ULVT_N.EX.6</b>	Extension of ULVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>ULVT_N.EX.7</b>	ULVT_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>ULVT_N.EX.8</b>	ULVT_N extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>ULVT_N.EX.9</b>	ULVT_N extension outside of GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>ULVT_N.EX.10</b>	ULVT_N (line-end vertical width ≤ 0.238um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>ULVT_N.EX.11</b>	ULVT_N extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure ≤ 0.04um by ULVT_N vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>ULVT_N.EX.12</b>	(ALL_GT NOT P2) extension outside of ULVT_N, except small ALL_GT jog ≤ 0.004um, Dummy_Cell_WO_IMP, and ULVT_N vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut ULVT_N vertical edge)	≥	0.083	um
<b>ULVT_N.O.1</b>	Overlap of (ALL_GT NOT P2) and ULVT_N (Except small ALL_GT jog ≤ 0.004um, Dummy_Cell_WO_IMP, and ULVT_N vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut ULVT_N vertical edge))	≥	0.083	um
<b>ULVT_N.A.1</b>	ULVT_N area	≥	0.085	um <sup>2</sup>
<b>ULVT_N.A.2</b>	ULVT_N enclosed area	≥	0.085	um <sup>2</sup>
<b>ULVT_N.A.3</b>	Area of ((ALL_GT NOT P2) AND ULVT_N)	≥	0.00158	um <sup>2</sup>
<b>ULVT_N.R.1</b>	(ALL_AA interact GT (width ≥ 0.032um)) CUT ULVT_N is not			

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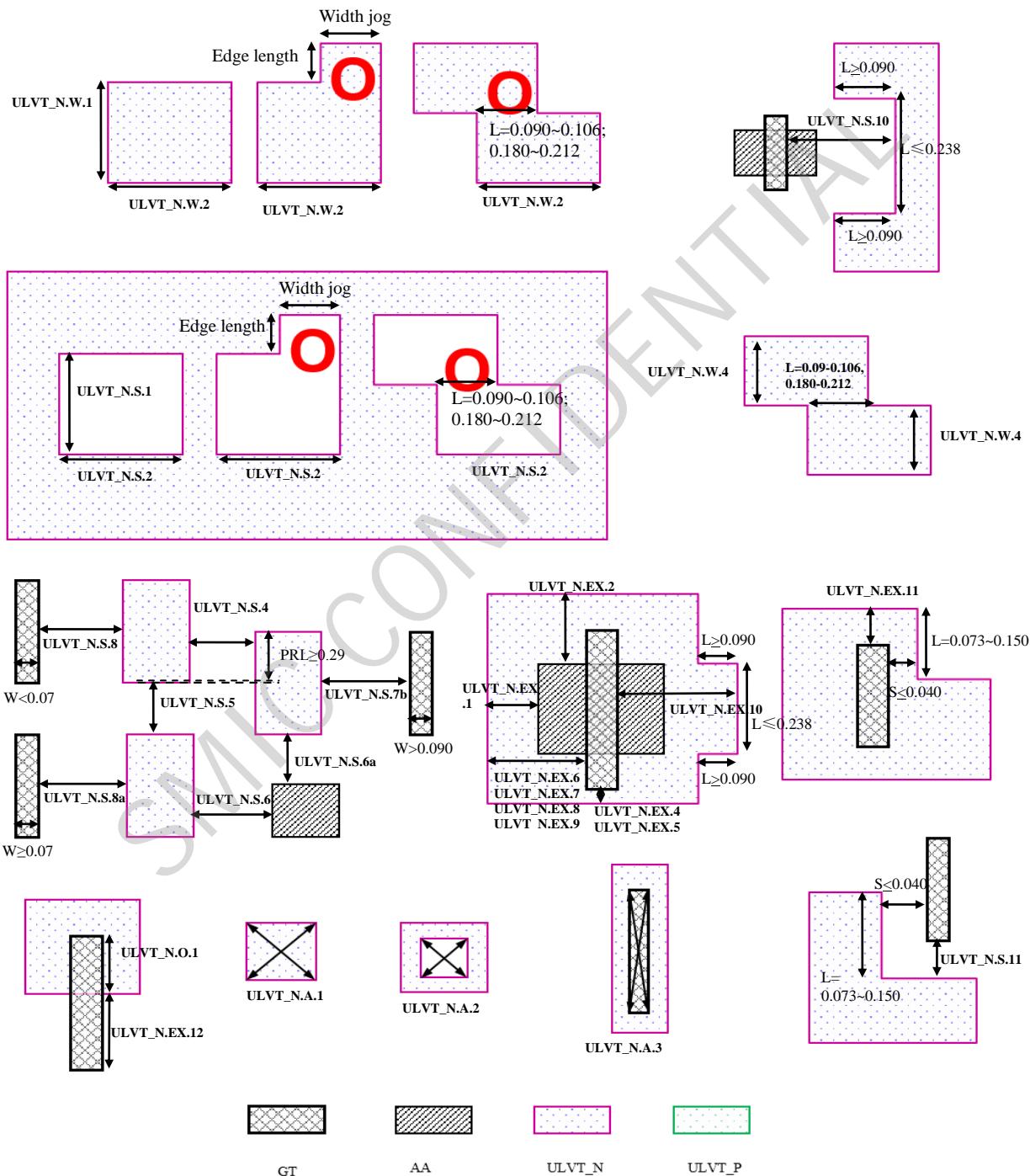
Rule number	Description	Opt.	Design Value	Unit
	allowed			
<b>ULVT_N.R.2</b>	ULVT_N overlap with P+AA, SVT_N, SVT_P, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_P, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
<b>ULVT_N.R.3</b>	(ALL_AA NOT AR) straddle on ULVT_N horizontal edge is not allowed.			

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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:2

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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:2

2017-11-02

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### 7.2.14 ULVT\_P design rules

A drawn ULVT\_P layer is needed to define P-type ultra low Vt MOS devices. ULVT\_P is for 0.8V core P-type ultra low Vt devices only.

Rule number	Description	Opt.	Design Value	Unit
<b>ULVT_P.W.1</b>	ULVT_P width, single-point-interaction is allowed. DRC waive: 1) ULVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.192	um
<b>ULVT_P.W.2</b>	ULVT_P width in S/D direction, single-point-interaction is allowed. DRC waive: 1) ULVT_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
<b>ULVT_P.W.3a</b>	ULVT_P width when just one vertical edge CUT (GTMK1 OR AR) in S/D direction DRC waive: 1) Jog width adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.315	um
<b>ULVT_P.W.3b</b>	ULVT_P width when both vertical ULVT_P edge CUT (GTMK1 OR AR) in S/D direction DRC waive: 1) Jog width adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in	$\geq$	0.36	um

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Rule number	Description	Opt.	Design Value	Unit
	S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
<b>ULVT_P.W.4</b>	ULVT_P width in GATE poly direction when ULVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	$\geq$	0.238	um
<b>ULVT_P.S.1</b>	Space between ULVT_P, single-point-interaction is allowed. DRC waive: 1) ULVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.192	um
<b>ULVT_P.S.2</b>	Space between ULVT_P in S/D direction, single-point-interaction is allowed. DRC waive: 1) ULVT_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
<b>ULVT_P.S.4</b>	Space between ULVT_P when PRL $\geq$ 0.29um	$\geq$	0.248	um
<b>ULVT_P.S.5</b>	Space between ULVT_P in GATE poly direction when ULVT_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
<b>ULVT_P.S.6</b>	Space between ULVT_P and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
<b>ULVT_P.S.6a</b>	Space between ULVT_P and ALL_AA in GATE poly direction	$\geq$	0.048	um

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Rule number	Description	Opt.	Design Value	Unit
<b>ULVT_P.S.7</b>	Space between ULVT_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jog ≤ 0.004um.	≥	0.024	um
<b>ULVT_P.S.7a</b>	Space between ULVT_P and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>ULVT_P.S.7b</b>	Space between ULVT_P and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>ULVT_P.S.8</b>	Space between ULVT_P and (ALL_GT NOT P2 ) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>ULVT_P.S.8a</b>	Space between ULVT_P and (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>ULVT_P.S.9a</b>	Space between ULVT_P and GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction (GATE CUT ULVT_P is not allowed), except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>ULVT_P.S.9b</b>	Space between ULVT_P and GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT ULVT_P is not allowed)	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>ULVT_P.S.10</b>	Space between ULVT_P vertical edge (edge length ≤ 0.238um between two concave corners with both sides length ≥ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>ULVT_P.S.11</b>	Space between ULVT_P and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space ≤ 0.04um (ULVT_P vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree coners)	≥	0.054	um
<b>ULVT_P.EX.1</b>	ULVT_P extension outside of ALL_AA (vertical edge abut AA edge is allowed)	≥	0.045	um
<b>ULVT_P.EX.2</b>	ULVT_P extension outside of ALL_AA in GATE poly direction	≥	0.048	um
<b>ULVT_P.EX.3</b>	ULVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) (Except small ALL_GT jogs ≤ 0.004um)	≥	0.024	um
<b>ULVT_P.EX.4</b>	ULVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>ULVT_P.EX.5</b>	ULVT_P extension outside of (ALL_GT NOT P2) (ALL_GT	≥	0.058	um

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Rule number	Description	Opt.	Design Value	Unit
	width > 0.09um)			
<b>ULVT_P.EX.6</b>	ULVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>ULVT_P.EX.7</b>	ULVT_P extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>ULVT_P.EX.8</b>	ULVT_P extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>ULVT_P.EX.9</b>	ULVT extension outside GATE (channel length = 0.016/0.018/0.020/0.022/0.024um, INSIDE GT_P96) in S/D direction	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>ULVT_P.EX.10</b>	ULVT_P (line-end vertical width ≤ 0.238um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>ULVT_P.EX.11</b>	ULVT_P extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure ≤ 0.04um by ULVT_P vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>ULVT_P.EX.12</b>	(ALL_GT NOT P2) extension outside of ULVT_P (Except small ALL_GT jog ≤ 0.004um), Dummy_Cell_WO_IMP, and ULVT_P vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut ULVT_P vertical edge))	≥	0.083	um
<b>ULVT_P.O.1</b>	Overlap of (ALL_GT NOT P2) and ULVT_P (Except small ALL_GT jog ≤ 0.004um), Dummy_Cell_WO_IMP, and ULVT_P vertical edge CUT (GTMK1 OR AR) (Channel length ≤ 0.024um, centerline abut ULVT_P vertical edge))	≥	0.083	um
<b>ULVT_P.A.1</b>	ULVT_P area	≥	0.085	um <sup>2</sup>
<b>ULVT_P.A.2</b>	ULVT_P enclosed area	≥	0.085	um <sup>2</sup>
<b>ULVT_P.A.3</b>	Area of ((ALL_GT NOT P2) AND ULVT_P)	≥	0.00158	um <sup>2</sup>
<b>ULVT_P.R.1</b>	(ALL_AA interact GT (width ≥ 0.032um)) CUT ULVT_P is not allowed.			

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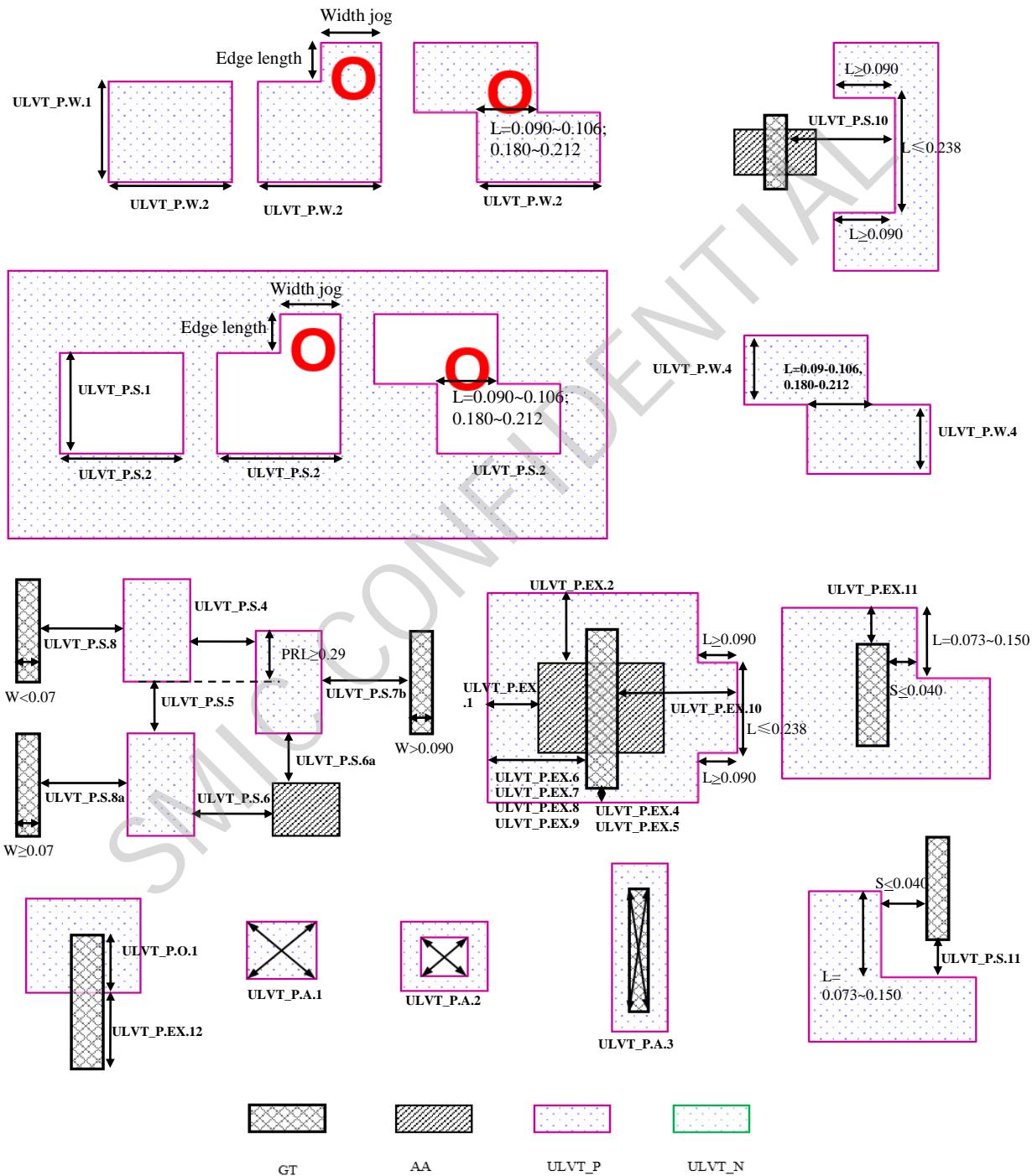
Rule number	Description	Opt.	Design Value	Unit
<b>ULVT_P.R.2</b>	ULVT_P overlap with N+AA, SVT_N, SVT_P, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_N, LFN_N, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
<b>ULVT_P.R.3</b>	(ALL_AA NOT AR) straddle on ULVT_P horizontal edge is not allowed.			

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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:2

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### 7.2.15 LFN\_N design rules

A drawn LFN\_N layer is needed to define core N-type LFN MOS device.

Rule number	Description	Opt.	Design Value	Unit
LFN_N.W.1	LFN_N width, single-point-interaction is allowed. DRC waive: 1) LFN_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.192	um
LFN_N.W.2	LFN_N width in S/D direction, single-point-interaction is allowed. DRC waive: 1) LFN_N one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.27	um
LFN_N.W.3	LFN_N width in S/D direction, when one LFN_N vertical edge CUT (GTMK1 OR AR) and ABUT HVT_N DRC waive: 1) Jog width adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.315	um
LFN_N.W.4	LFN_N width in GATE poly direction when LFN_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	≥	0.238	um
LFN_N.S.1	Space between LFN_N, single-point-interaction is allowed.	≥	0.192	um

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Rule number	Description	Opt.	Design Value	Unit
	DRC waive: 1) LFN_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
LFN_N.S.2	Space between LFN_N in S/D direction, single-point-interaction is allowed.  DRC waive: 1) LFN_N one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.27	um
LFN_N.S.3a	Space between LFN_N in S/D direction, when just one LFN_N vertical edge CUT (GTMK1 OR AR) and abut LVT_N or ULVT_N  DRC waive: 1) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	≥	0.315	um
LFN_N.S.3b	Space between LFN_N in S/D direction, when both LFN_N vertical edge CUT (GTMK1 OR AR) and abut LVT_N or ULVT_N  DRC waive: 1) Jog space adjacent to edge (length ≤ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction 2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D	≥	0.36	um

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Rule number	Description	Opt.	Design Value	Unit
	direction			
<b>LFN_N.S.4</b>	Space between LFN_N when PRL $\geq$ 0.29um	$\geq$	0.248	um
<b>LFN_N.S.5</b>	Space between LFN_N in GATE poly direction when LFN_N point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
<b>LFN_N.S.6</b>	Space between LFN_N and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
<b>LFN_N.S.6a</b>	Space between LFN_N and ALL_AA in GATE poly direction	$\geq$	0.048	um
<b>LFN_N.S.7</b>	Space between LFN_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs $\leq$ 0.004um	$\geq$	0.024	um
<b>LFN_N.S.7a</b>	Space between LFN_N and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
<b>LFN_N.S.7b</b>	Space between LFN_N and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
<b>LFN_N.S.8</b>	Space between LFN_N and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
<b>LFN_N.S.8a</b>	Space between LFN_N and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
<b>LFN_N.S.9a</b>	Space between LFN_N and GATE (when channel length= 0.016/0.018/0.02um) respectively in S/D direction, (GATE CUT LFN_N is not allowed), except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
<b>LFN_N.S.9b</b>	Space between LFN_N and GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT LFN_N is not allowed)	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>LFN_N.S.10</b>	Space between LFN_N vertical edge (edge length $\leq$ 0.238um between two concave corners with both sides length $\geq$ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
<b>LFN_N.S.11</b>	Space between LFN_N and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space to (ALL_GT NOT P2) $\leq$ 0.04um (LFN_N vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree coners)	$\geq$	0.054	um

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Rule number	Description	Opt.	Design Value	Unit
<b>LFN_N.EX.1</b>	LFN_N extension outside of ALL_AA (vertical edge abut AA edge is allowed)	≥	0.045	um
<b>LFN_N.EX.2</b>	LFN_N extension outside of ALL_AA in GATE poly direction	≥	0.048	um
<b>LFN_N.EX.3</b>	LFN_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jog ≤ 0.004um.	≥	0.024	um
<b>LFN_N.EX.4</b>	LFN_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um)	≥	0.034	um
<b>LFN_N.EX.5</b>	LFN_N extension outside of (ALL_GT NOT P2) (ALL_GT width > 0.09um)	≥	0.058	um
<b>LFN_N.EX.6</b>	LFN_N extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	≥	0.035	um
<b>LFN_N.EX.7</b>	LFN_N extension outside of (ALL_GT NOT P2) (ALL_GT width ≥ 0.07um) in S/D direction	≥	0.058	um
<b>LFN_N.EX.8</b>	LFN_N extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	≥	0.082/ 0.081/ 0.08	um
<b>LFN_N.EX.9</b>	LFN_N extension outside of GATE (when channel length = 0.016/0.018/0.02/0.022/0.024 um) respectively INSIDE GT_P96 in S/D direction.	≥	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>LFN_N.EX.10</b>	LFN_N (line-end vertical width ≤ 0.238um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	≥	0.079	um
<b>LFN_N.EX.11</b>	LFN_N extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure ≤ 0.04um by LFN_N vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	≥	0.054	um
<b>LFN_N.EX.12</b>	(ALL_GT NOT P2) extension outside of LFN_N, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and LFN_N vertical edge CUT (GTMK1 OR AR) (channel length ≤ 0.024um, centerline abut LFN_N vertical edge)	≥	0.083	um
<b>LFN_N.O.1</b>	Overlap of (ALL_GT NOT P2) and LFN_N, except small ALL_GT jogs ≤ 0.004um, Dummy_Cell_WO_IMP, and LFN_N	≥	0.083	um

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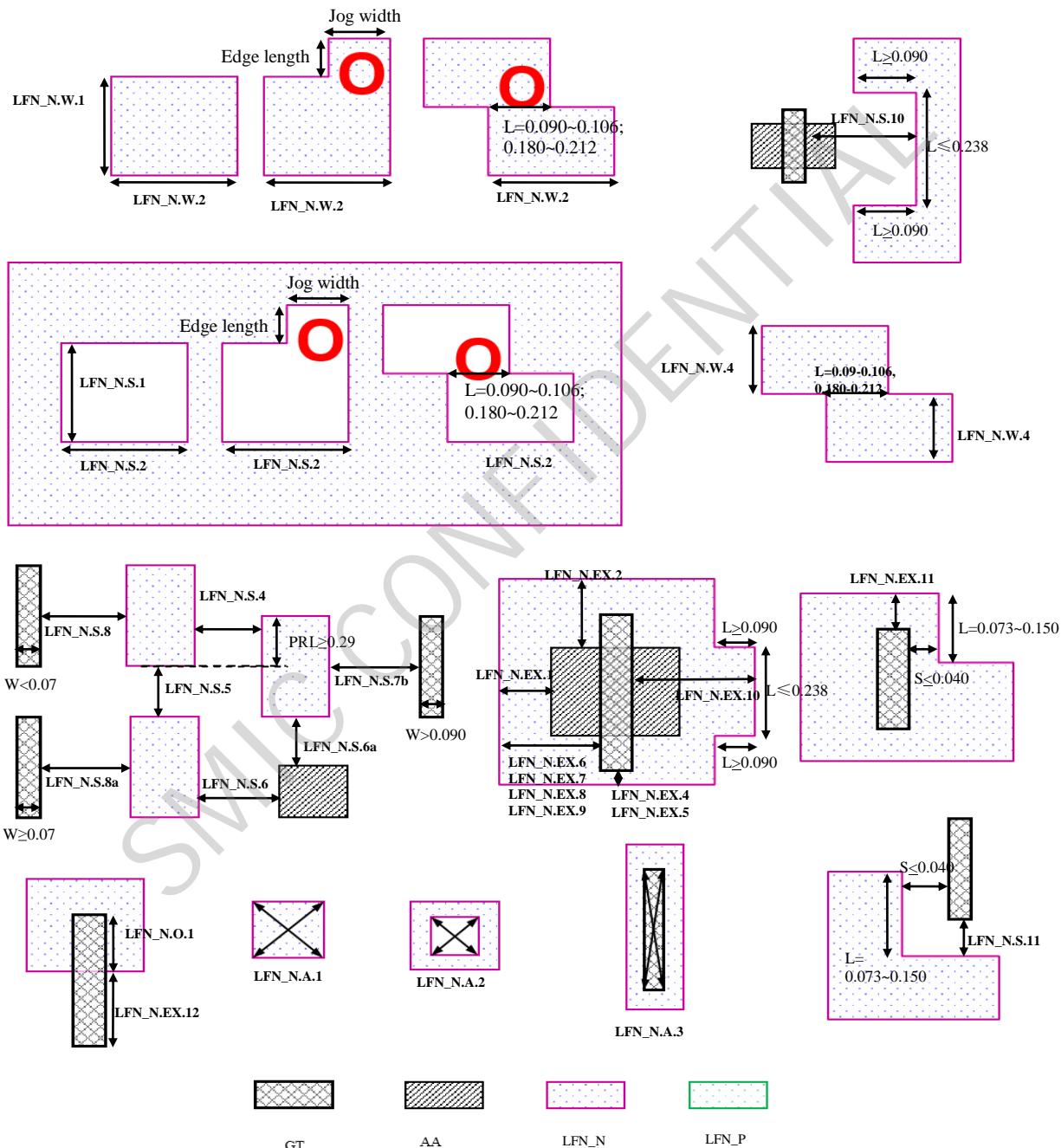
Rule number	Description	Opt.	Design Value	Unit
	vertical edge CUT (GTMK1 OR AR) (channel length $\leq$ 0.024um, centerline abut LFN_N vertical edge)			
<b>LFN_N.A.1</b>	LFN_N area	$\geq$	0.085	um <sup>2</sup>
<b>LFN_N.A.2</b>	LFN_N enclosed area	$\geq$	0.085	um <sup>2</sup>
<b>LFN_N.A.3</b>	Area of ((ALL_GT NOT P2) AND LFN_N)	$\geq$	0.00158	um <sup>2</sup>
<b>LFN_N.R.1</b>	(ALL_AA interact GT (width $\geq$ 0.032um)) CUT LFN_N is not allowed			
<b>LFN_N.R.2</b>	LFN_N overlap with P+AA, SVT_N, SVT_P, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_P, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
<b>LFN_N.R.3</b>	(ALL_AA NOT AR) straddle on LFN_N horizontal edge is not allowed.			

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2017-11-02

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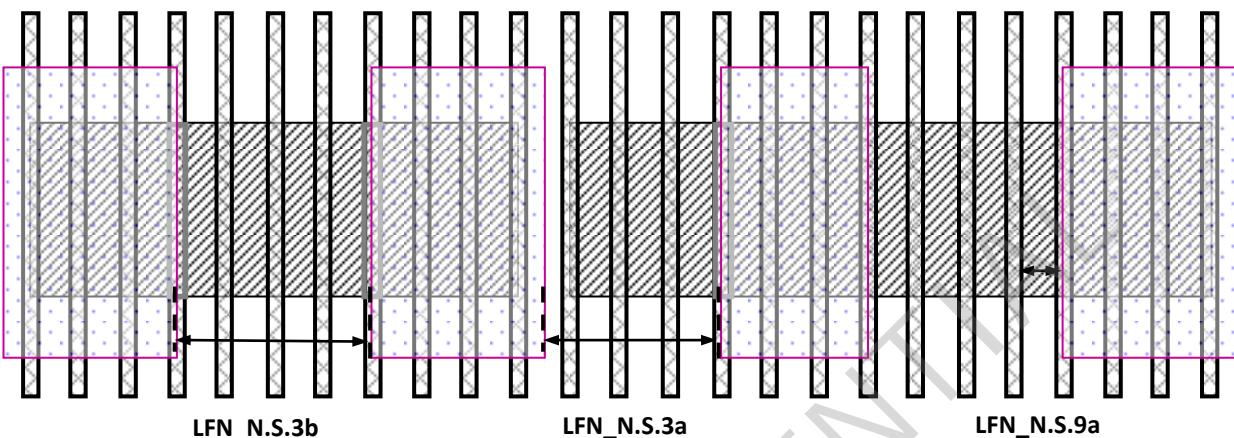


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2017-11-02

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### 7.2.16 LFN\_P design rules

A drawn LFN\_P layer is needed to define core P-type LFN MOS device.

Rule number	Description	Opt.	Design Value	Unit
<b>LFN_P.W.1</b>	LFN_P width, single-point-interaction is allowed. DRC waive: 1) LFN_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction 3) Jog width adjacent to edge (length = 0.002um , between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.192	um
<b>LFN_P.W.2</b>	LFN_P width in S/D direction, single-point-interaction is allowed. DRC waive: 1) LFN_P one-track width within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um 2) Jog width adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 3) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
<b>LFN_P.W.3</b>	LFN_P width in S/D direction, when LFN_P vertical edge CUT (GTMK1 OR AR) and ABUT HVT_P DRC waive: 1) Jog width adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18/0.192/0.225/0.24um in S/D direction 2) Jog width adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.315	um
<b>LFN_P.W.4</b>	LFN_P width in GATE poly direction when LFN_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction (except L-shape/T-shape concave corner)	$\geq$	0.238	um
<b>LFN_P.S.1</b>	Space between LFN_P, single-point-interaction is allowed. DRC waive:	$\geq$	0.192	um

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Rule number	Description	Opt.	Design Value	Unit
	1) LFN_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um  2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.18um in S/D direction  3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction			
LFN_P.S.2	Space between LFN_P in S/D direction, single-point-interaction is allowed.  DRC waive: 1) LFN_P one-track space within the range of 0.09~0.106um, 0.18~0.212um when PRL = 0um  2) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction  3) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.27	um
LFN_P.S.3a	Space between LFN_P in S/D direction, when just one LFN_P vertical edge CUT (GTMK1 OR AR) and abut LVT_P or ULVT_P.  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction  2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.315	um
LFN_P.S.3b	Space between LFN_P in S/D direction, when both LFN_P's vertical edges CUT (GTMK1 OR AR) and abut LVT_P or ULVT_P.  DRC waive: 1) Jog space adjacent to edge (length $\leq$ 0.048um, between two consecutive 90-270 degree corners) = 0.180/0.192/0.225/0.24um in S/D direction  2) Jog space adjacent to edge (length = 0.002um, between two consecutive 90-270 degree corners) = 0.135/0.144um in S/D direction	$\geq$	0.36	um

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Rule number	Description	Opt.	Design Value	Unit
<b>LFN_P.S.4</b>	Space between LFN_P when PRL $\geq$ 0.29um	$\geq$	0.248	um
<b>LFN_P.S.5</b>	Space between LFN_P in GATE poly direction when LFN_P point touch or horizontal width in the range of 0.09~0.106um, 0.18~0.212um while PRL = 0um in GATE poly direction	$\geq$	0.238	um
<b>LFN_P.S.6</b>	Space between LFN_P and ALL_AA (vertical edge abut AA edge is allowed)	$\geq$	0.045	um
<b>LFN_P.S.6a</b>	Space between LFN_P and ALL_AA in GATE poly direction	$\geq$	0.048	um
<b>LFN_P.S.7</b>	Space between LFN_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um), except small ALL_GT jogs $\leq$ 0.004um)	$\geq$	0.024	um
<b>LFN_P.S.7a</b>	Space between LFN_P and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
<b>LFN_P.S.7b</b>	Space between LFN_P and (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
<b>LFN_P.S.8</b>	Space between LFN_P and (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
<b>LFN_P.S.8a</b>	Space between LFN_P and (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
<b>LFN_P.S.9a</b>	Space between LFN_P and GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, (GATE CUT LFN_P is not allowed), except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
<b>LFN_P.S.9b</b>	Space between LFN_P and GATE (when channel length=0.016/0.018/0.02//0.022/0.024um, INSIDE GT_P96) in S/D direction (GATE CUT LFN_P is not allowed)	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>LFN_P.S.10</b>	Space between LFN_P vertical edge (edge length $\leq$ 0.238um between two concave corners with both sides length $\geq$ 0.09um) and ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
<b>LFN_P.S.11</b>	Space between LFN_P and (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal space $\leq$ 0.04um (LFN_P vertical edge length = 0.073~0.15um, between two consecutive 90-270 degree coners)	$\geq$	0.054	um
<b>LFN_P.EX.1</b>	LFN_P extension outside of ALL_AA (vertical edge abut AA edge)	$\geq$	0.045	um

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Rule number	Description	Opt.	Design Value	Unit
	is allowed)			
<b>LFN_P.EX.2</b>	LFN_P extension outside of ALL_AA in GATE poly direction	$\geq$	0.048	um
<b>LFN_P.EX.3</b>	LFN_P extension outside of (ALL_GT width < 0.07um) (ALL_GT NOT P2), except small ALL_GT jog $\leq$ 0.004um.	$\geq$	0.024	um
<b>LFN_P.EX.4</b>	LFN_P extension outside of (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um)	$\geq$	0.034	um
<b>LFN_P.EX.5</b>	LFN_P extension outside of (ALL_GT NOT P2) (ALL_GT width > 0.09um)	$\geq$	0.058	um
<b>LFN_P.EX.6</b>	LFN_P extension outside of (ALL_GT NOT P2) (ALL_GT width < 0.07um) in S/D direction	$\geq$	0.035	um
<b>LFN_P.EX.7</b>	LFN_P extension outside of (ALL_GT NOT P2) (ALL_GT width $\geq$ 0.07um) in S/D direction	$\geq$	0.058	um
<b>LFN_P.EX.8</b>	LFN_P extension outside of GATE (when channel length = 0.016/0.018/0.02um) respectively in S/D direction, except GT_P96 region	$\geq$	0.082/ 0.081/ 0.08	um
<b>LFN_P.EX.9</b>	LFN_P extension outside of GATE (when channel length = 0.016/0.018/0.02/0.022/0.024um, INSIDE GT_P96) in S/D direction	$\geq$	0.088/ 0.087/ 0.086/ 0.085/ 0.084	um
<b>LFN_P.EX.10</b>	LFN_P (line-end vertical width $\leq$ 0.238um between two consecutive 90-90 degree corners with both sides length $\geq$ 0.09um) enclosure of ((GT AND GTMK1) OR GATE) in S/D direction	$\geq$	0.079	um
<b>LFN_P.EX.11</b>	LFN_P extension outside of (ALL_GT NOT P2) in GATE poly direction with adjacent horizontal enclosure $\leq$ 0.04um by LFN_P vertical edge (edge length = 0.073~0.15um, between two consecutive 90-270 degree corners)	$\geq$	0.054	um
<b>LFN_P.EX.12</b>	(ALL_GT NOT P2) extension outside of LFN_P, except small ALL_GT jogs $\leq$ 0.004um, Dummy_Cell_WO_IMP, and LFN_P vertical edge CUT (GTMK1 OR AR) (Channel length $\leq$ 0.024um, centerline abut LFN_P vertical edge)	$\geq$	0.083	um
<b>LFN_P.O.1</b>	Overlap of (ALL_GT NOT P2) and LFN_P, except small ALL_GT jogs $\leq$ 0.004um, Dummy_Cell_WO_IMP, and LFN_P vertical edge CUT (GTMK1 OR AR) (Channel length $\leq$ 0.024um,	$\geq$	0.083	um

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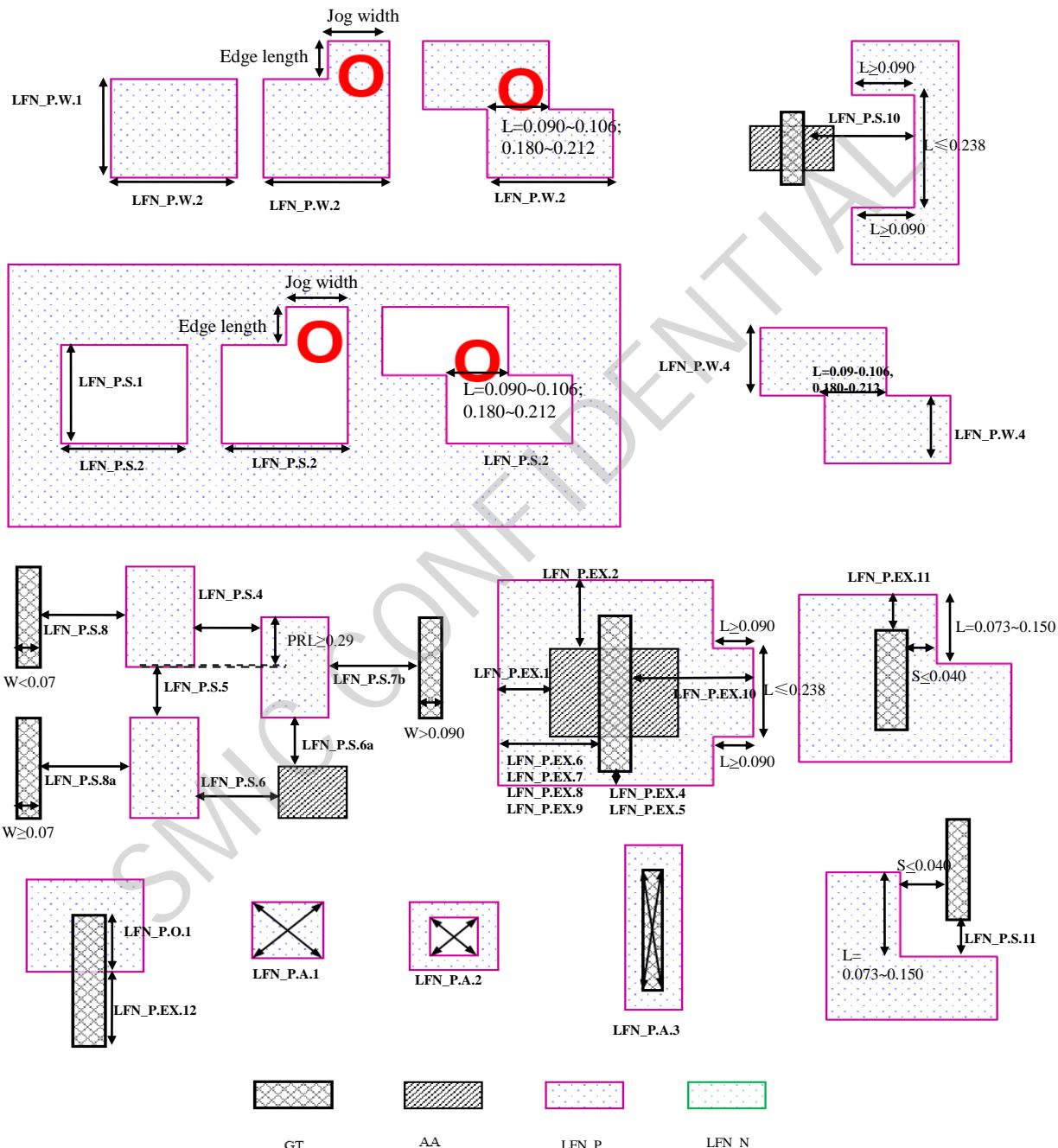
Rule number	Description	Opt.	Design Value	Unit
	centerline abut LFN_P vertical edge)			
<b>LFN_P.A.1</b>	LFN_P area	$\geq$	0.085	um <sup>2</sup>
<b>LFN_P.A.2</b>	LFN_P enclosed area	$\geq$	0.085	um <sup>2</sup>
<b>LFN_P.A.3</b>	Area of ((ALL_GT NOT P2) AND LFN_P)	$\geq$	0.00158	um <sup>2</sup>
<b>LFN_P.R.1</b>	(ALL_AA interact GT (width $\geq$ 0.032um)) CUT LFN_P is not allowed.			
<b>LFN_P.R.2</b>	LFN_P overlap with N+AA, SVT_N, SVT_P, HVT_N, HVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, DG, PSUB, INST, RESNW, VARMOS, DMPNP, MARKS is not allowed, exclude OCCD region.			
<b>LFN_P.R.3</b>	(ALL_AA NOT AR) straddle on LFN_P horizontal edge is not allowed.			

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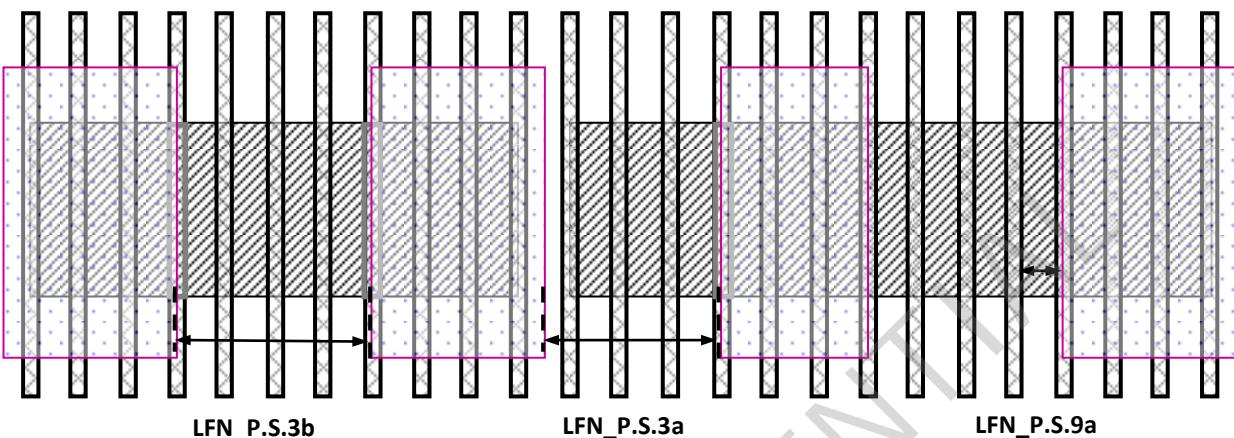


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### 7.2.17 DG design rules

Rule number	Description	Opt.	Design Value	Unit
<b>DG.W.1</b>	DG width	$\geq$	0.286	um
<b>DG.S.1</b>	Space between two DGs	$\geq$	0.286	um
<b>DG.S.2a</b>	Space between DG and GATE along the S/D direction	$\geq$	0.313	um
<b>DG.S.2b</b>	Space between DG and AA (AA cut DG is not allowed), except pick-up AA	$\geq$	0.098	um
<b>DG.S.2c</b>	Space between DG and AA (AA vertical edge extend 1/2 GT width) in S/D direction (AA cut DG is not allowed), except pick-up AA	$\geq$	0.116	um
<b>DG.S.2d</b>	Space between DG and DUM_AA (DUM_AA cut DG is not allowed)	$\geq$	0.053	um
<b>DG.S.2e</b>	Space between DG and DUM_AA (AA vertical edge extend 1/2 GT width) in S/D direction (DUM_AA cut DG is not allowed)	$\geq$	0.07	um
<b>DG.S.3</b>	Space between DG and NW (space = 0 is allowed)	$\geq$	0.238	um
<b>DG.EN.1a</b>	DG enclosure of GATE along the S/D direction	$\geq$	0.313	um
<b>DG.EN.1b</b>	DG enclosure of AA, except pick-up AA	$\geq$	0.098	um
<b>DG.EN.1c</b>	DG enclosure of AA (AA vertical edge extend 1/2 GT width) in S/D direction, except pick-up AA.	$\geq$	0.116	um
<b>DG.EN.1d</b>	DG enclosure of DUM_AA	$\geq$	0.053	um
<b>DG.EN.1e</b>	DG enclosure of DUM_AA (AA vertical edge extend 1/2 GT width) in S/D direction	$\geq$	0.07	um
<b>DG.EN.2a</b>	DG extension outside of NW (extension = 0um is allowed)	$\geq$	0.238	um
<b>DG.EN.2b</b>	DG enclosure by NW (enclosure = 0um is allowed)	$\geq$	0.238	um
<b>DG.O.1</b>	DG overlap of NW (abut is allowed)	$\geq$	0.238	um
<b>DG.A.1</b>	DG area	$\geq$	0.32	um <sup>2</sup>
<b>DG.A.2</b>	DG enclosed area	$\geq$	0.32	um <sup>2</sup>
<b>DG.R.1</b>	1.8V, 1.2V and 1.5V GATE cannot inside the same NW.			
<b>DG.R.2</b>	(GATE AND DGUD), (GATE AND DGV) must inside DG			

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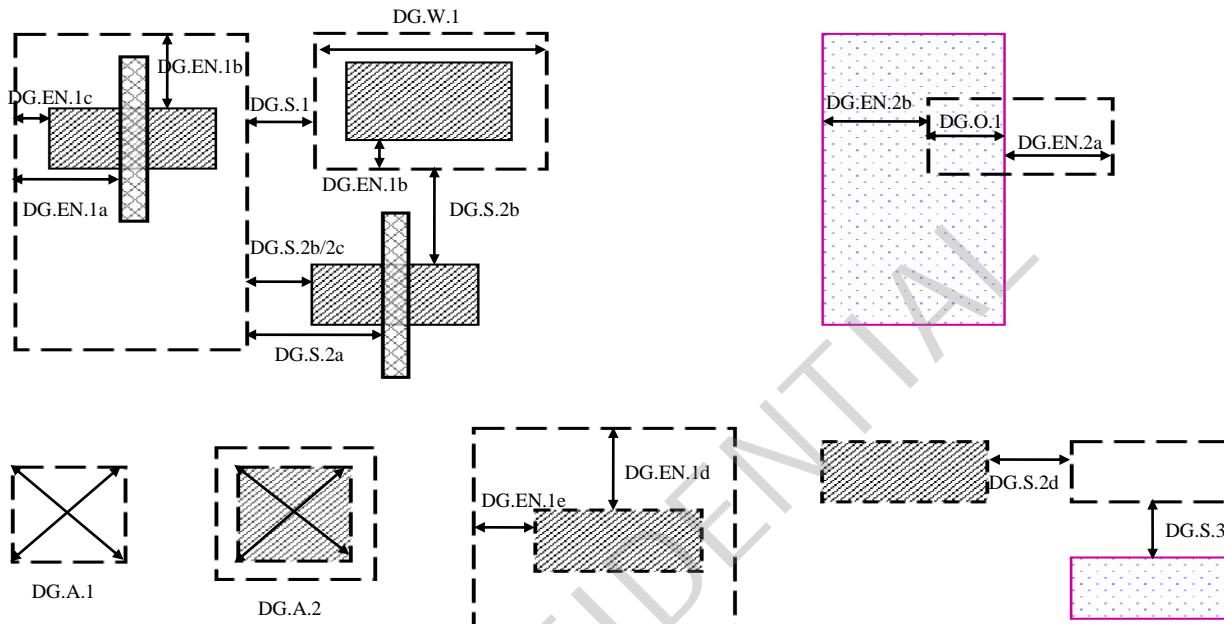
Rule number	Description	Opt.	Design Value	Unit
DG.R.3	GATE cut DG, DGUD or DGV is not allowed.			
DG.R.4	AOP_GT CUT DGV is not allowed.			
DG.R.5	DGUD overlap DGV is not allowed.			
DG.R.6	(DGV or DGUD) overlap VARMOS is not allowed.			

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### 7.2.18 GT design rules

Rule number	Description	Opt.	Design Value	Unit
<b>GT.W.1</b>	ALL_GT Width	$\geq$	0.016	um
<b>GT.W.2</b>	ALL_GT width, except DMCMK1, LDBK, MARKS, OCOVL and LOGO regions	$\leq$	0.242	um
<b>GT.W.3</b>	ALL_GT width in core region, except GT_P96, INST, MARKS, OCOVL and LOGO regions	$=$	0.016/0.018/ 0.02, 0.032, 0.07~0.242	um
<b>GT.W.3a</b>	(GT OR GTDMP) width in core region INSIDE GT_P96	$=$	0.016/0.018/ 0.02/0.022/ 0.024	um
<b>GT.W.4</b>	(AOP_GT INTERACT DG) width, except DGV region	$\geq$	0.086	um
<b>GT.W.4a</b>	(AOP_GT INTERACT DG) width in DGV region	$\geq$	0.08	um
<b>GT.W.5</b>	Channel length for core NMOS/PMOS transistor, except ESDIO2, GT_P96, VARMOS, INST and PSUB regions	$=$	0.016/0.018/ 0.02, 0.032, 0.07~0.242	um
<b>GT.W.5a</b>	Channel length for core NMOS/PMOS transistor INSIDE GT_P96	$=$	0.016/0.018/ 0.02/0.022/ 0.024	um
<b>GT.W.6</b>	Channel length of 1.8V MOS underdrive to 1.5V I/O NMOS/PMOS transistor (GATE AND DGUD)	$=$	0.086~0.242	um
<b>GT.W.7</b>	Channel length of 1.8V MOS underdrive to 1.2V I/O NMOS/PMOS transistor (GATE AND DGV)	$=$	0.08~0.242	um
<b>GT.W.8</b>	Channel length of 1.8V I/O NMOS /PMOS transistor, except DGUD, DGV, VARMOS, LDBK regions	$=$	0.134~0.242	um
<b>GT.W.9</b>	Channel length for core NMOS/PMOS transistor for HVT device	$\leq$	0.032	um
<b>GT.W.10b</b>	Width of AOP_GT neighboring to AOP_GT (width = 0.016/0.018um, space to AOP_GT < 0.117um), except ESDIO1, ESDIO2 regions	$=$	0.016/0.018/ 0.02	um
<b>GT.W.10d</b>	Width of AOP_GT neighboring to AOP_GT (width = 0.02um, space to AOP_GT < 0.117um), except INST, ESDIO1 and ESDIO2 regions	$=$	0.016/0.018/ 0.02/0.022/0. 024/0.032	um

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Rule number	Description	Opt.	Design Value	Unit
<b>GT.W.10e</b>	Width of AOP_GT neighboring to AOP_GT (width = 0.022/0.024um, space to ALL_GT < 0.117um), except ESDIO1 and ESDIO2 regions	=	0.02/0.022/ 0.024/0.032	um
<b>GT.W.10f</b>	Width of AOP_GT neighboring to AOP_GT (width = 0.032um, space to ALL_GT < 0.117um), except INST, ESDIO1 and ESDIO2 regions	=	0.02/0.022/ 0.024/0.032	um
<b>GT.W.11a</b>	Width of AOP_GT neighboring to GATE (channel length ≤ 0.02um, AOP_GT to neighboring GATE space < 0.117um), except INST, ESDIO1 and ESDIO2 regions	=	0.016/0.018/ 0.02	um
<b>GT.W.11b</b>	Width of AOP_GT neighboring to GATE (channel length = 0.022/0.024um, AOP_GT to neighboring GATE space < 0.117um), except ESDIO1, ESDIO2 regions	=	0.02/0.022/ 0.024	um
<b>GT.W.11c</b>	Width of AOP_GT neighboring to GATE (channel length = 0.032um, AOP_GT to neighboring GATE space < 0.117um), AOP_GT should be same to neighboring GATE, except ESDIO1, ESDIO2 regions	=	0.032	um
<b>GT.W.11d</b>	Width of AOP_GT neighboring to GATE (channel length ≥ 0.07um, AOP_GT to neighboring GATE space = 0.117~0.118um), except ESDIO1, ESDIO2 and L-shape AA region	≥	0.07	um
<b>GT.W.12a</b>	Width of AOP_GT neighboring to GATE (INSIDE DG, AOP_GT to neighboring GATE space = 0.117~0.118um), except DGV, ESDIO1, ESDIO2 and L-shape AA region	≥	0.086	um
<b>GT.W.12b</b>	Width of AOP_GT neighboring to GATE (INSIDE DGV, AOP_GT to neighboring GATE space = 0.117~0.118um), except ESDIO1, ESDIO2 and L-shape AA region	≥	0.08	um
<b>GT.S.1</b>	GT space, except LOGO and OCOVL region	≥	0.07	um
<b>GT.S.2</b>	Space between AOP_GT centerline (both AOP_GT width ≤ 0.02um) in S/D direction, except centerline space > 0.1um case and GT_P96 region	=	0.09	um
<b>GT.S.3a</b>	Space between AOP_GT centerline (both AOP_GT width ≤ 0.024um, INSIDE GT_P96) in S/D direction except centerline space > 0.1um	=	0.096	um
<b>GT.S.3b</b>	Space between AOP_GT centerline (both AOP_GT width = 0.032um) in S/D direction	≥	0.106	um

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Rule number	Description	Opt.	Design Value	Unit
<b>GT.S.4</b>	Space between two AOP_GT when either AOP_GT width $\geq$ 0.07um, except LOGO and OCOVL region	$\geq$	0.117	um
<b>GT.S.5</b>	Space between (AOP_GT NOT OUTSIDE DG) and AOP_GT	$\geq$	0.117	um
<b>GT.S.6</b>	Space between AOP_GT (INTERACT the same ALL_AA) in S/D direction, except ESDIO1 and ESDIO2 regions	$\leq$	0.12	um
<b>GT.S.7</b>	Space between the short side of AOP_GT (width $\leq$ 0.032um) and AOP_GT when PRL > -0.07um	$\geq$	0.108	um
<b>GT.S.8</b>	Space between the long side of ALL_GT (width $\leq$ 0.024um) and AOP_GT when PRL > -0.108um	$\geq$	0.07	um
<b>GT.S.8a</b>	Space between the long side of ALL_GT (width = 0.032um) and AOP_GT when PRL > -0.108um	$\geq$	0.072	um
<b>GT.S.9</b>	Space between AOP_GT (width $\geq$ 0.07um) and AOP_GT when PRL > -0.117um, except LOGO and OCOVL region	$\geq$	0.117	um
<b>GT.S.10</b>	Space between AOP_GT to AOP_AA	$\geq$	0.046	um
<b>GT.S.11</b>	Space between field (AOP_GT NOT P2) and AOP_AA (maximum delta V > 3.63V) (3.3V+10%)	$\geq$	0.108	um
<b>GT.S.12</b>	Space between field (AOP_GT NOT P2) and AOP_AA (AA vertical edge extend 1/2 GT width) (maximum delta V > 3.63V) (3.3V+10%) in S/D direction	$\geq$	0.117	um
<b>GT.S.13</b>	Space between (ALL_GT NOT ALL_P2), except (NODMF su 1um), (MARKS su 1um), RESP1, LOGO, OCOVL regions.  This rule is a local density related rule.  DRC flags (((Chip NOT (ALL_GT NOT ALL_P2)) sd 0.625um) su 0.625um) region greater than 1.25*1.25um	$\leq$	1.25	um
<b>GT.S.14</b>	Space between (ALL_GT NOT ALL_P2) INSIDE RESP1 region.  This rule is a local density related rule.  DRC flags (((((Chip AND RESP1) NOT (ALL_GT NOT ALL_P2)) sd 1.05um) su 1.05um) region greater than 2.1*2.1um	$\leq$	2.1	um

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Rule number	Description	Opt.	Design Value	Unit
<b>GT.S.15b</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.016um) and neighboring AOP_GT for core NMOS/PMOS, except ESDIO1, ESDIO2 and GT_P96 regions	=	0.072~0.074	um
<b>GT.S.15c</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.018um) and neighboring AOP_GT for core NMOS/PMOS, except ESDIO1, ESDIO2 and GT_P96 regions	=	0.071~0.073	um
<b>GT.S.15d</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.02um) and neighboring AOP_GT for core NMOS/PMOS, except ESDIO1, ESDIO2 and GT_P96 regions	=	0.070~0.072	um
<b>GT.S.15e</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.032um) and neighboring AOP_GT for core NMOS/PMOS , except ESDIO1, ESDIO2 regions	=	0.074	um
<b>GT.S.15f</b>	Space between ((GATE SIZING 0.042um) AND GT) (channel length $\geq$ 0.07um) and neighboring AOP_GT for core NMOS/PMOS, except ESDIO1, ESDIO2 regions	=	0.118, 0.119	um
<b>GT.S.15g</b>	Space between ((GATE SIZING 0.042um) AND GT) and neighboring AOP_GT for I/O device, except ESDIO1, ESDIO2, LDBK regions	=	0.118, 0.119	um
<b>GT.S.15i</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.016um) and neighboring AOP_GT for core NMOS/PMOS in GT_P96 region.	=	0.078~ 0.08	um
<b>GT.S.15j</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.018um) and neighboring AOP_GT for core NMOS/PMOS in GT_P96 region.	=	0.077~ 0.079	um
<b>GT.S.15k</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.02um) and neighboring AOP_GT for core NMOS/PMOS in GT_P96 region.	=	0.076~ 0.078	um
<b>GT.S.15l</b>	Space between ((GATE SIZING 0.02um) AND GT) (channel length = 0.022/0.024um) and neighboring AOP_GT for core NMOS/PMOS in GT_P96 region.	=	0.072~0.075	um
<b>GT.S.16a</b>	Space between GATE (channel length $\leq$ 0.032um) and neighboring second AOP_GT in S/D direction for core	$\leq$	0.18	um

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Rule number	Description	Opt.	Design Value	Unit
	MOS device. The second AOP_GT is required to be placed second neighboring the GATE, except INST, ESDIO1 and ESDIO2 regions			
<b>GT.S.16b</b>	Space between GATE (channel length $\geq$ 0.07um) and neighboring second AOP_GT in S/D direction for core MOS device. The second AOP_GT is required to be placed second neighboring the GATE, except ESDIO1 and ESDIO2 region	$\leq$	0.481	um
<b>GT.S.17b</b>	Space between AOP_GT (width = 0.016um and one side poly space $\geq$ 0.081um) and AOP_GT, except GT_P96 region	=	0.072~0.074	um
<b>GT.S.17c</b>	Space between AOP_GT (width = 0.018um and one side poly space $\geq$ 0.081um) and AOP_GT, except GT_P96 region	=	0.071~0.073	um
<b>GT.S.17d</b>	Space between AOP_GT (width = 0.02um and one side poly space $\geq$ 0.081um) and AOP_GT, except GT_P96 region	=	0.070~0.072	um
<b>GT.S.17e</b>	Space between AOP_GT (width = 0.032um and one side poly space $\geq$ 0.081um) and AOP_GT , except INST region	=	0.074	um
<b>GT.S.17f</b>	Space between ALL_GT (0.07um $\leq$ width $\leq$ 0.16um and one side poly space $\geq$ 0.118um) and ALL_GT, except ESDIO1, ESDIO2 and OCOVL regions	=	0.118,0.119	um
<b>GT.S.17h</b>	Space between AOP_GT (width = 0.016um and one side poly space $\geq$ 0.081um) and AOP_GT, inside GT_P96 region	=	0.078~0.08	um
<b>GT.S.17i</b>	Space between AOP_GT (width = 0.018um and one side poly space $\geq$ 0.081um) and AOP_GT, inside GT_P96 region	=	0.077~0.079	um
<b>GT.S.17j</b>	Space between AOP_GT (width = 0.02um and one side poly space $\geq$ 0.081um) and AOP_GT, inside GT_P96 region	=	0.074, 0.076~0.078	um
<b>GT.S.17k</b>	Space between AOP_GT (width = 0.022/0.024um and one side poly space $\geq$ 0.081um) and AOP_GT, inside GT_P96 region	=	0.072~0.075	um
<b>GT.S.18b</b>	Forbidden space between AOP_GT (width = 0.016um) and AOP_GT DRC don't check:	=	0.070~0.071, 0.075~0.079,	um

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Rule number	Description	Opt.	Design Value	Unit
	<p>1) AOP_GT (INSIDE P2) with PRL <math>\leq</math> 0.012um                      2) Space to one AOP_GT group = 0.207~0.342um.                      AOP_GT group definition: number of (AOP_GT width <math>\leq</math> 0.032um and space <math>\leq</math> 0.074um) <math>\geq</math> 7                      3) GT_P96 region</p>		0.1~0.342	
GT.S.18c	<p>Forbidden space between AOP_GT (width = 0.018um) and AOP_GT                      DRC don't check:                      1) AOP_GT (INSIDE P2) with PRL <math>\leq</math> 0.012um                      2) Space to one AOP_GT group = 0.207~0.342um.                      AOP_GT group definition: number of (AOP_GT width <math>\leq</math> 0.032um and space <math>\leq</math> 0.074um) <math>\geq</math> 7                      3) GT_P96 region</p>	=	0.07, 0.074~0.079, 0.1~0.342	um
GT.S.18d	<p>Forbidden space between AOP_GT (width = 0.02um) and AOP_GT                      DRC don't check:                      1) AOP_GT (INSIDE P2) with PRL <math>\leq</math> 0.012um                      2) Space to one AOP_GT group = 0.207~0.342um.                      AOP_GT group definition: number of (AOP_GT width <math>\leq</math> 0.032um and space <math>\leq</math> 0.074um) <math>\geq</math> 7                      3) GT_P96 and INST regions</p>	=	0.073~0.079, 0.1~0.342	um
GT.S.18f	<p>Forbidden space between AOP_GT (width = 0.016um, INSIDE GT_P96) and AOP_GT                      DRC don't check:                      1) AOP_GT (INSIDE P2) with PRL <math>\leq</math> 0.012um</p>	=	0.07~0.077, 0.1~0.342	um
GT.S.18g	<p>Forbidden space between AOP_GT (width = 0.018um, INSIDE GT_P96) and AOP_GT                      DRC don't check:                      1) AOP_GT (INSIDE P2) with PRL <math>\leq</math> 0.012um</p>	=	0.07~0.076, 0.1~0.342	um
GT.S.18h	<p>Forbidden space between AOP_GT (width = 0.02um, INSIDE GT_P96) and AOP_GT (except 0.032um AOP_GT)                      DRC don't check:                      1) AOP_GT (INSIDE P2) with PRL <math>\leq</math> 0.012um</p>	=	0.071~0.073, 0.079, 0.1~0.342	um
GT.S.18i	<p>Forbidden space between AOP_GT (width = 0.024um, INSIDE GT_P96) and AOP_GT                      DRC don't check:</p>	=	0.07~0.071, 0.075~0.079, 0.1~0.342	um

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Rule number	Description	Opt.	Design Value	Unit
	1) AOP_GT (INSIDE P2) with PRL $\leq$ 0.012um			
GT.S.18j	Forbidden space between AOP_GT (width = 0.022um, INSIDE GT_P96) and AOP_GT DRC don't check: 1) AOP_GT (INSIDE P2) with PRL $\leq$ 0.012um	=	0.07~0.072, 0.076~0.079, 0.1~0.342	um
GT.S.18k	Forbidden space between AOP_GT (width = 0.02um, INSIDE GT_P96) and AOP_GT (width = 0.032) DRC don't check: 1) AOP_GT (INSIDE P2) with PRL $\leq$ 0.012um	=	0.073~0.075, 0.081, 0.1~0.342	um
GT.S.19	Space between AOP_GT jog (width $\leq$ 0.004um) and GATE in GATE poly direction when PRL > -0.096um	$\geq$	0.048	um
GT.EX.1	AOP_GT jog (width $\leq$ 0.004um) extension outside of GATE in GATE poly direction when PRL > -0.1um	$\geq$	0.048	um
GT.EX.2	AOP_GT extension outside of AA in GATE poly direction (extension < 0 is not allowed), except AOP_GT jog $\leq$ 0.004um and MARKS region	$\geq$	0.041	um
GT.L.1	Maximum (GT NOT P2) (GT width $\leq$ 0.032um) length between two M0Gs, as well as the length from any point inside GATE to the nearest M0G when the GT width $\leq$ 0.032um, except ESDMK1, ESDIO1 and ESDIO2 regions.	$\leq$	10.5	um
GT.L.2	AOP_GT length (width < 0.07um), except DMCMK1 region	$\geq$	0.246	um
GT.L.3	AOP_GT length (width $\geq$ 0.07um), except DMCMK1 region	$\geq$	0.225	um
GT.L.4	AOP_GT jog length (jog width $\leq$ 0.004um)	$\geq$	0.24	um
GT.L.6	Length of ((ALL_GT NOT P2) INTERACT ALL_AA), except DMPNP, VARMOS region	$\leq$	10.5	um
GT.L.7	Length of ((ALL_GT (width $\geq$ 0.032um) NOT ALL_P2) INTERACT ALL_AA), except DMPNP, VARMOS, LDBK and DMC1 regions.	$\leq$	1.6	um
GT.A.1	GT area	$\geq$	0.00416	um <sup>2</sup>
GT.A.2	(ALL_GT NOT ALL_P2) area DRC don't check: 1) BJT region (DMPNP) and OCOVL region	$\leq$	2.45	um <sup>2</sup>

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Rule number	Description	Opt.	Design Value	Unit
	2) (AOP_GT NOT ALL_P2) (width $\leq$ 0.032um) enclosed in 10 um*10 um window with GT density $\leq$ 50% 3) (ALL_GT NOT ALL_P2) (width = 0.1um ~ 0.242um, length $\leq$ 30um) enclosed in 10 um*10 um window with poly density $\leq$ 50%			
<b>GT.A.3</b>	(ALL_GT NOT ALL_P2) area INSIDE DMPNP region	$\leq$	4.1	um <sup>2</sup>
<b>GT.A.4</b>	When (ALL_GT NOT ALL_P2) space $\geq$ 1.21um, the PRL must be $\leq$ 17um, except (NODMF OR MARKS), DIR, DIRDMP, OCOVL regions			
<b>GT.A.4a</b>	When (ALL_GT NOT ALL_P2)) space $\geq$ 0.91um, the PRL must be $\leq$ 5.5um, except (NODMF OR MARKS), RESNW, DIR, DIRDMP, DMPNP, LOGO, OCOVL regions.			
<b>GT.A.5</b>	When (ALL_GT NOT ALL_P2) space $\geq$ 0.55um in ((INST SIZING 1um) NOT INST), the PRL must be $\leq$ 10um, except BORDER enclosure INST $\leq$ 0.16um in cell level			
<b>GT.D.1</b>	(ALL_GT NOT ALL_P2) full chip density	$\geq$	14%	
<b>GT.D.2</b>	(ALL_GT NOT ALL_P2) full chip density	$\leq$	40%	
<b>GT.D.3</b>	(ALL_GT NOT ALL_P2) density, except (NODMF su 1um), OCOVL, DIR, DIRDMP regions (window 10um*10um, stepping 5um)	$\geq$	10%	
<b>GT.D.4</b>	(ALL_GT NOT ALL_P2) density for RESP1 region. (window 10um*10um, stepping 5um)	$\geq$	6%	
<b>GT.D.5</b>	(ALL_GT NOT ALL_P2) density for core device region. (window 10um*10um, stepping 5um)	$\leq$	50%	
<b>GT.D.5a</b>	(ALL_GT NOT ALL_P2) density for I/O device region (window 10um*10um, stepping 5um)	$\leq$	60%	
<b>GT.D.6</b>	(ALL_GT NOT ALL_P2) density (window 140um*140um, stepping 70um)	$\leq$	50%	
<b>GT.D.7</b>	(ALL_GT NOT ALL_P2) density difference between any two neighboring checking window (window 20um*20um, stepping 10um)	$\leq$	35%	
<b>GT.R.1</b>	ALL_GT (width $\geq$ 0.032um) must be a rectangle orthogonal			

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Rule number	Description	Opt.	Design Value	Unit
	to grid, except MARKS and LOGO regions..			
<b>GT.R.2</b>	ALL_GT (width < 0.032um) must be a rectangle orthogonal to grid, except small jog $\leq 0.004\text{um}$			
<b>GT.R.3</b>	O-shape GT is not allowed, except LOGO region			
<b>GT.R.4</b>	AOP_GT (width < 0.032um) interact AOP_GT (width $\geq 0.032\text{um}$ ) is not allowed.			
<b>GT.R.5</b>	Different jog width on the same ALL_GT is not allowed, except LOGO region			
<b>GT.R.6</b>	Different ALL_GT jog height inside the same P2 is not allowed.			
<b>GT.R.7</b>	Different jog height on the same ALL_GT and Z-shape GT jog are not allowed, except LOGO region			
<b>GT.R.8</b>	ALL_GT jog height must be the same when interact the same AA. DRC check the region of the AA horizontal edge sizing 0.1um.			
<b>GT.R.9</b>	ALL_GT must be vertical direction, except DMCMK1, LOGO and MARKS regions.			
<b>GT.R.10</b>	((ALL_GT NOT P2) NOT (DUM_GT INSIDE DMCB1)) CUT (DG OR ((DMPNP OR DSTR) OR VARMOS)) is not allowed.			
<b>GT.R.11</b>	The number of AOP_GT in one group 1) AA with only one or two GATE (width $\leq 0.024\text{um}$ ) 2) AOP_GT space $\leq 0.08\text{um}$ 3) AOP_GT has same PRL as ((GATE su 0.035um) AND GT)	$\geq$	7	
<b>GT.R.12</b>	The number of AOP_GT inside P96_Group Definition of P96_Group: (((AOP_GT INSIDE GT_P96) with width $\leq 0.024\text{um}$ ) su 0.04um) sd 0.04um DRC flags width of P96_Group $\leq 0.504\text{um}$ in S/D direction.	$\geq$	7	
<b>GT.R.13</b>	Floating GATE is not allowed if the effective S/D are not			

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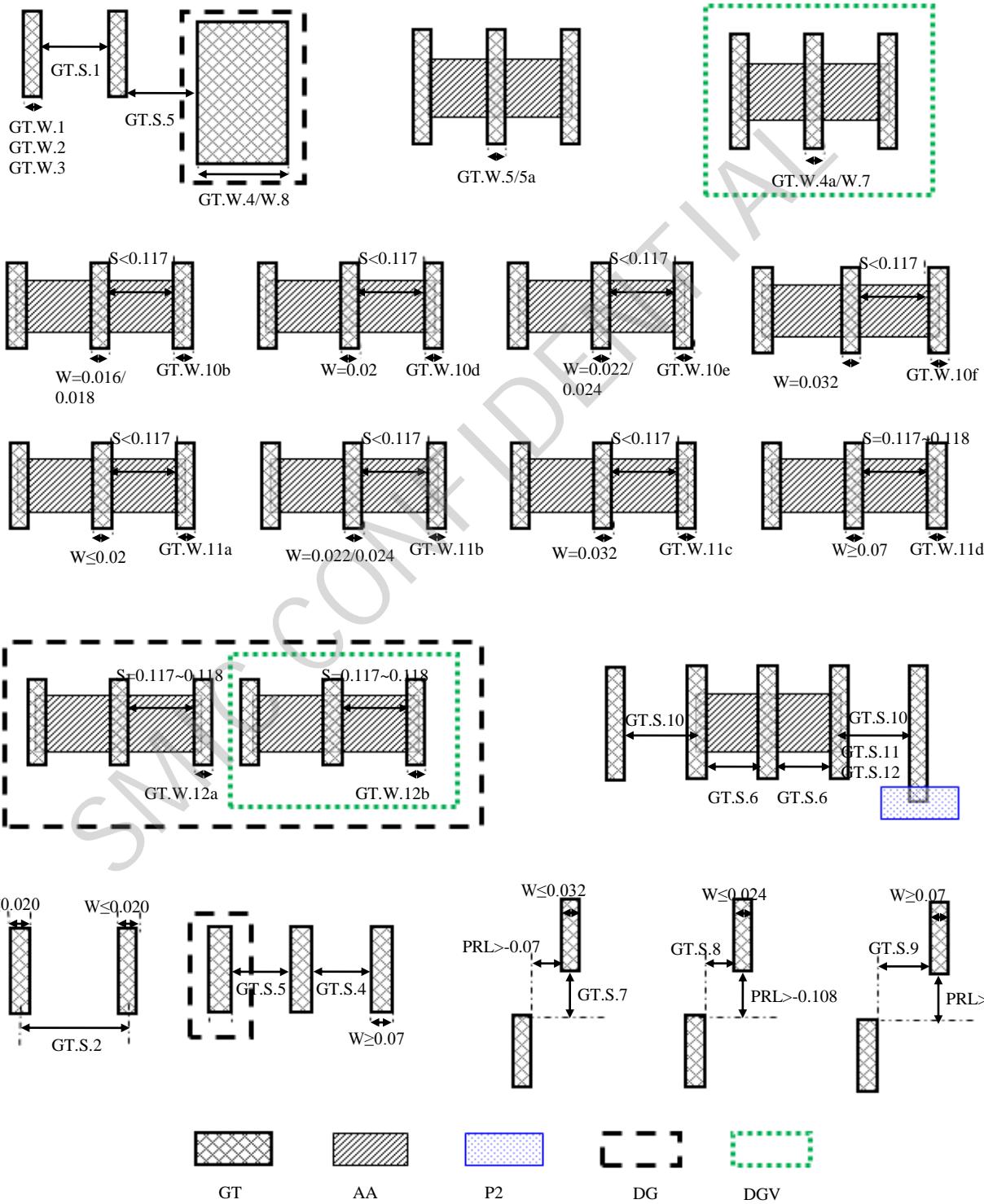


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Rule number	Description	Opt.	Design Value	Unit
	connected together, for chip level purpose. Floating GATE definition: (1) GATE not connected to M0G (2) GATE connected to M0G but not connected to MOS AA, pick-up or MD. (3) It is not a floating GATE if the GATE is connected to AA by M0G in SRAM bit cell. (4) HR resistor is treated as a conductor between the two HR terminal. DRC check methodology for effective S/D: (1) S/D is connected to different (MOS AA NOT GT), pick-up, Gate, or MD.			
<b>GT.R.14</b>	ALL_GT must be fully covered by (SN OR SP), except DMCMK1, RESNW, MRAKS and OCOVL regions			
<b>GT.R.15</b>	AOP_GT extension outside of AOP_AA in S/D direction equal to the half width of the same AOP_GT, except AOP_GT both side space to neighboring AOP_GT on the same AOP_AA, INST, and LDBK region. DRC flags the vertical edge of AOP_AA (INTERACT AOP_GT) NOT fully abut the centerline of AOP_GT			
<b>GT.R.17</b>	Space between P90_Group (AOP_GT number < 7, width < 0.556um in S/D direction) to AOP_GT (width $\geq$ 0.032um, PRL > -0.03um) $\leq$ 0.079um in S/D direction at both sides is not allowed, except GT_P96 region. Definition of P90_Group: ((AOP_GT (width $\leq$ 0.02um) su 0.037um) sd 0.037um)			
<b>GT.R.18</b>	GT fully cover AA is not allowed.			
<b>GT.R.19</b>	Maximum delta V $\geq$ 5.6V is not allowed, when space between (AOP_GT NOT P2) < 0.770um			

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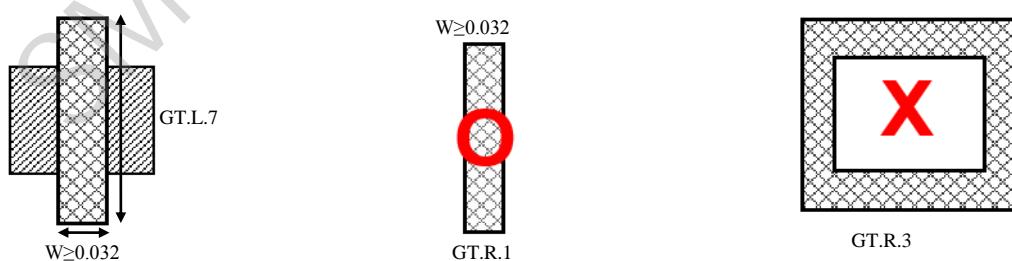
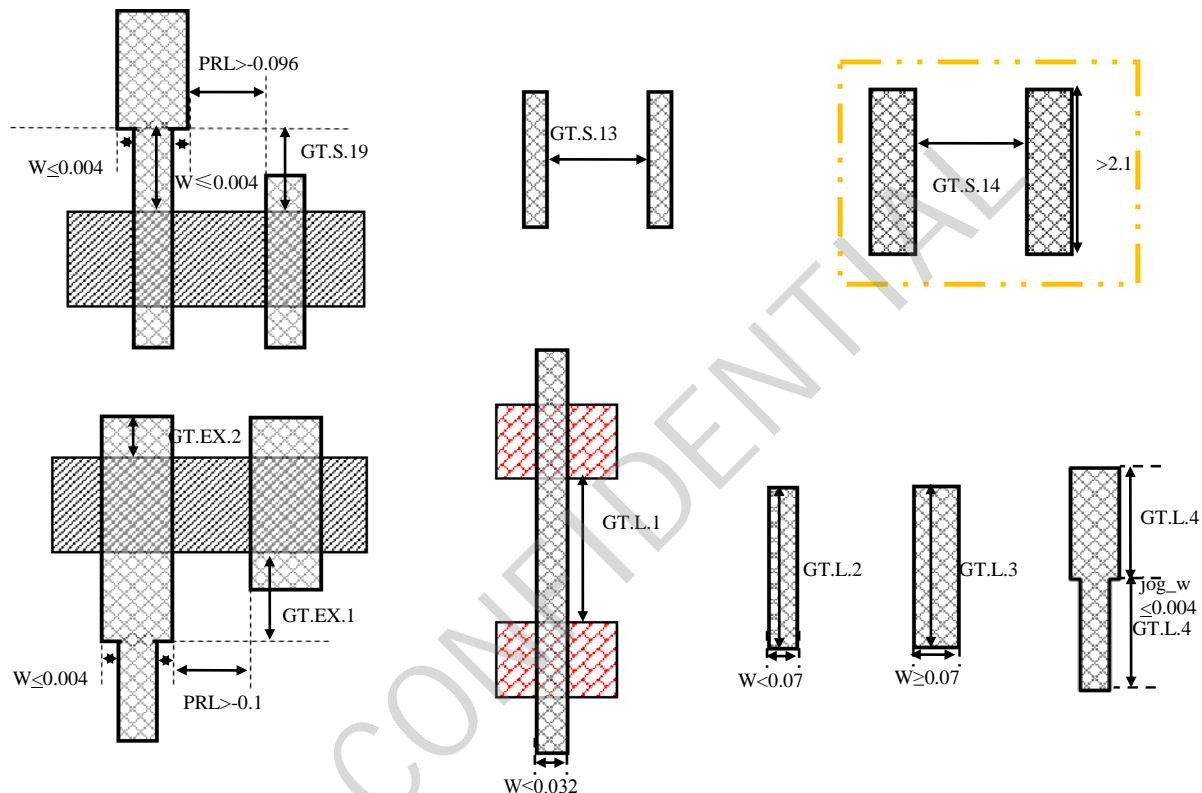


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### 7.2.19 EGATE design rules

GTMK1 is the marker layer to define edge GATE interact with AA vertical edge for 3 terminal MOS DIO on AA edge and 4-terminal turn off transistor after cell abutment, 4-terminal GTMK1 transistor GATE must be turned off.

GTMK2 is used to define the transistor when GATE abut GTMK1.

Rule number	Description	Opt.	Design Value	Unit
<b>EGATE.R.1</b>	GTMK1 must be fully covered by AOP_GT.			
<b>EGATE.R.2</b>	GTMK2 both two vertical edges must fully abut GT vertical edge.			
<b>EGATE.R.3</b>	GTMK1 and GTMK2 must be rectangles and orthogonal to grid.			
<b>EGATE.R.4</b>	(GTMK2 AND AA) must be rectangles and orthogonal to grid			
<b>EGATE.R.5</b>	GTMK2 both two horizontal edges must abut AA horizontal edges			
<b>EGATE.R.6</b>	GTMK2 at least one horizontal edge must abut GTMK1 horizontal edge			
<b>EGATE.R.7</b>	(GT AND GTMK1) width in S/D and outside AA direction must be the same as LAST GATE of 0.032um, when neighboring to LAST GATE (channel length = 0.032um, (GT AND GTMK1) to LAST GATE space = 0.074um)  LAST GATE definition: the closest GATE to AA edge in S/D direction (AA on LAST GATE extension $\leq$ 0.318um).			
<b>EGATE.R.8</b>	(GT AND GTMK1) width in S/D and outside AA direction must be the same as LAST GATE, or 0.072um, when neighboring to LAST GATE (channel length $\geq$ 0.07um, (GT AND GTMK1) to LAST GATE space = 0.118 or 0.119um), in core region.  LAST GATE definition: the closest GATE to AA edge in S/D direction (AA on LAST GATE extension $\leq$ 0.358um).			
<b>EGATE.R.9</b>	(GT AND GTMK1) width in S/D and outside AA direction must be the same as LAST GATE, or 0.086um, or 0.134um, when neighboring to LAST GATE ((GT AND GTMK1) to LAST GATE space = 0.118 or 0.119um) INSIDE DG, except DGV region.  LAST GATE definition: the closest GATE to AA edge in S/D direction (AA on LAST GATE extension $\leq$ 0.358um)			
<b>EGATE.R.10</b>	(GT AND GTMK1) width in S/D and outside AA direction must be the same as LAST GATE, or 0.08um, or 0.086um, or			

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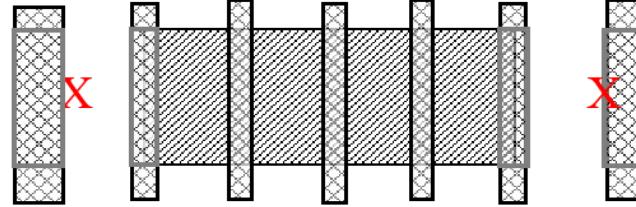
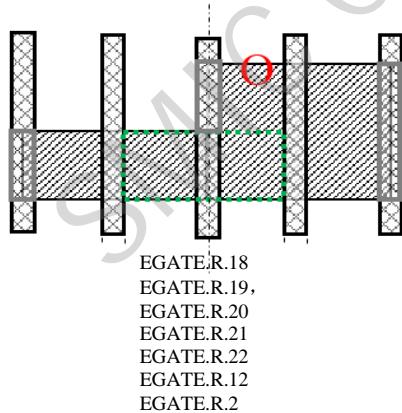
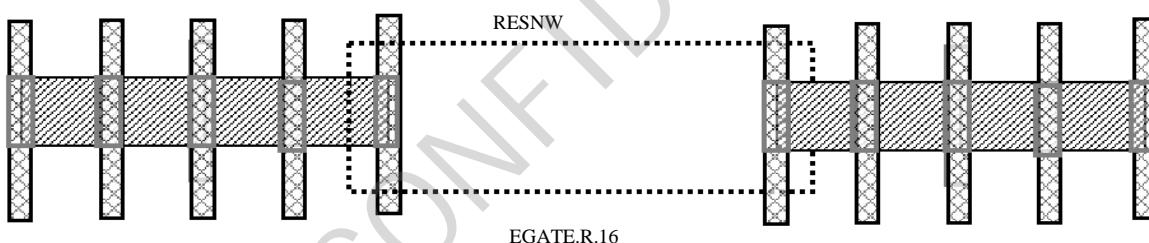
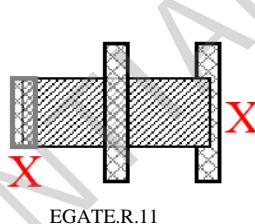
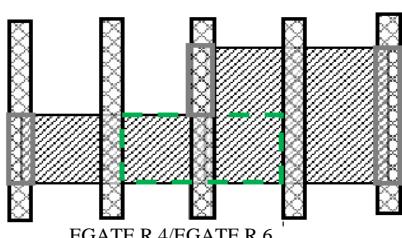
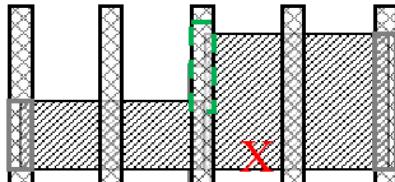
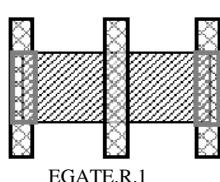


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Rule number	Description	Opt.	Design Value	Unit
	0.134um, when neighboring to LAST GATE ((GT AND GTMK1) to LAST GATE space = 0.118 or 0.119um), inside DGV region.  LAST GATE definition: the closest GATE to AA edge in S/D direction (AA on LAST GATE extension $\leq$ 0.358um)			
<b>EGATE.R.11</b>	AA vertical edge must align both GT and (GTMK1 or AR) centerline, except INST and MARKS regions.  The value of (GT AND GTMK1) width must be a even number.			
<b>EGATE.R.12</b>	GTMK2 overlap more than one GATE is not allowed.			
<b>EGATE.R.13</b>	((GT NOT P2) INTERACT (GTMK1 AND NW)) must connect to (N+ pick-up AA inside VARMOS).			
<b>EGATE.R.14</b>	Width of GATE (channel length $\leq$ 0.024 um) between two adjacent (GTMK1 OR AR) on the same AA must be the same.			
<b>EGATE.R.15</b>	GTMK2 interact the vertical edge (between 90-90 degree corners) of AA is not allowed.			
<b>EGATE.R.16</b>	The vertical edge of ((AA INTERACT RESNW) OR DOP_AA) must align with AOP_GT centerline			
<b>EGATE.R.17</b>	(AA AND GT) (INSIDE (pick-up NOT VARMOS), (DIOMK1 OR DIOMK2), DIR, DMPNP, or DSTR) must interact GTMK1, except INST region.			
<b>EGATE.R.18</b>	GTMK1 (width $>$ 0.032um in S/D direction) centerline must align (AA NOT INTERACT RESNW) vertical edge, except (pick-up NOT VARMOS), (DIOMK1 OR DIOMK2), DIR, DMPNP, and DSTR regions.			
<b>EGATE.R.19</b>	GTMK1 must be drawn identically to (GT AND AA (vertical edge extend 1/2 GT width) NOT GTMK2).			
<b>EGATE.R.20</b>	GTMK1 overlap GTMK2 is not allowed.			
<b>EGATE.R.21</b>	GTMK2 must be rectangle orthogonal to grid.			
<b>EGATE.R.22<sup>[NC]</sup></b>	4-terminal MOS with GTMK1 must be turned off and connect to metal pin test, except DSTR, DMPNP, (DIOMK1 OR DIOMK2), DIR and MARKS regions			

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### 7.2.20 GT\_P96 design rules

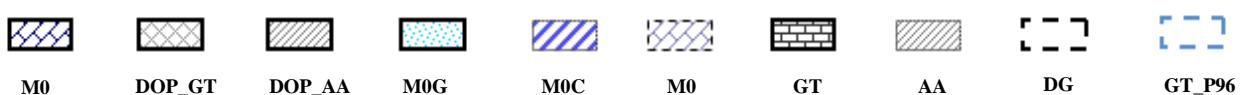
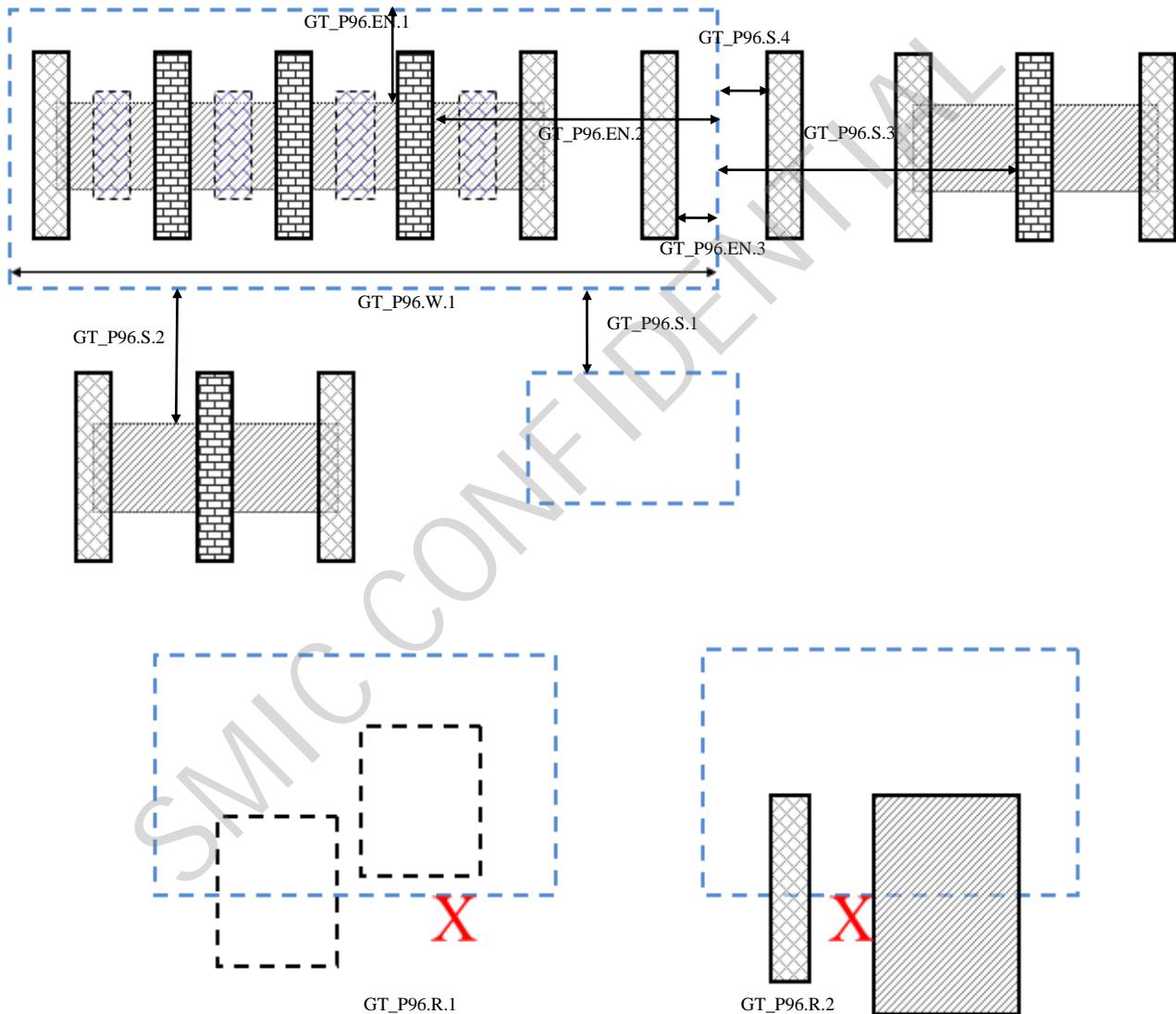
Rule number	Description	Opt.	Design Value	Unit
<b>GT_P96.W.1</b>	GT_P96 width in S/D direction	$\geq$	1.44	um
<b>GT_P96.S.1</b>	Space between two GT_P96	$\geq$	0.63	um
<b>GT_P96.S.2</b>	Space between GT_P96 and GATE	$\geq$	0.24	um
<b>GT_P96.S.3</b>	Space between GT_P96 and GATE in S/D direction	$\geq$	0.395	um
<b>GT_P96.S.4</b>	Space between GT_P96 and AOP_GT in S/D direction, except DMCMK1	$\geq$	0.035	um
<b>GT_P96.EN.1</b>	GT_P96 enclosure of GATE	$\geq$	0.048	um
<b>GT_P96.EN.2</b>	GT_P96 enclosure of GATE in S/D direction	$\geq$	0.313	um
<b>GT_P96.EN.3</b>	GT_P96 enclosure of AOP_GT in S/D direction, except DMCMK1	$\geq$	0.035	um
<b>GT_P96.R.1</b>	GT_P96 INTERACT DG is not allowed.			
<b>GT_P96.R.2</b>	AOP_AA or AOP_GT CUT GT_P96 is not allowed.			

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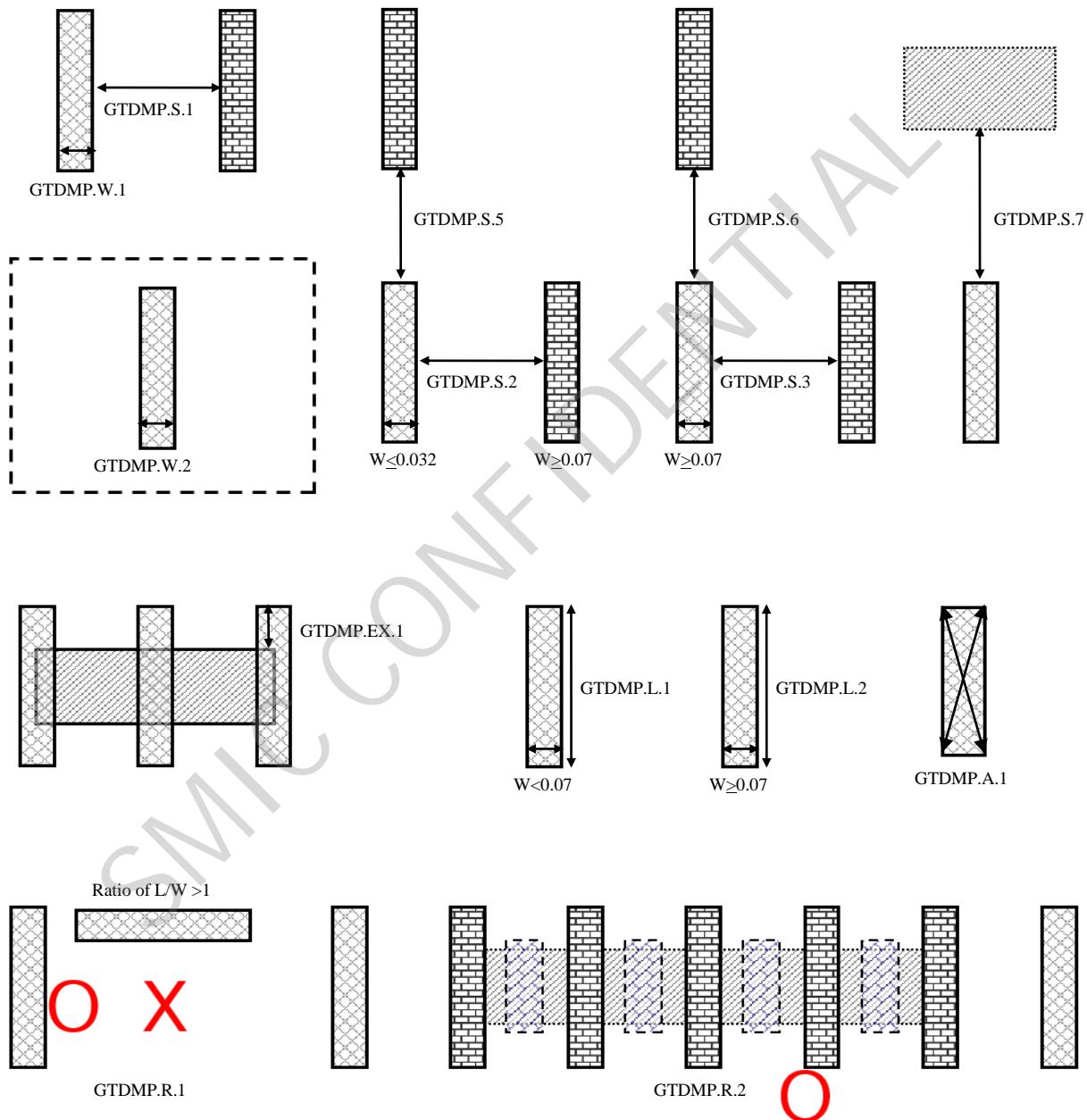
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### 7.2.21 GTDMP dummy rules (data type 8)

Rule number	Description	Opt.	Design Value	Unit
<b>GTDMP.W.1</b>	GTDMP width	=	0.016/0.018/ 0.02/0.022/ 0.024, 0.032, 0.07~0.242	um
<b>GTDMP.W.2</b>	GTDMP width when INTERACT DG, except DGV region.	=	0.086~0.242	um
<b>GTDMP.W.3</b>	GTDMP width INSIDE GT_P96, except dummy cell	=	0.016~0.024	um
<b>GTDMP.S.1</b>	Space between (GT OR GTDMP) (GTDMP overlap or abut GT is not allowed), except OCOVL region	≥	0.07	um
<b>GTDMP.S.2</b>	Space between GTDMP (width ≤ 0.032um) and AOP_GT (width ≥ 0.07um)	≥	0.117	um
<b>GTDMP.S.3</b>	Space between GTDMP (width ≥ 0.07um) and AOP_GT	≥	0.117	um
<b>GTDMP.S.5</b>	Space between GTDMP (width ≤ 0.032 um) and AOP_GT in GATE poly direction	≥	0.108	um
<b>GTDMP.S.6</b>	Space between GTDMP (width ≥ 0.07um) and AOP_GT in GATE poly direction	≥	0.117	um
<b>GTDMP.S.7</b>	Space between GTDMP and AOP_AA	≥	0.046	um
<b>GTDMP.EX.1</b>	GTDMP extension outside of DOP_AA in GATE poly direction (Extension < 0um is not allowed)	≥	0.041	um
<b>GTDMP.L.1</b>	GTDMP length (width < 0.07um)	≥	0.246	um
<b>GTDMP.L.2</b>	GTDMP length (width ≥ 0.07um)	≥	0.225	um
<b>GTDMP.A.1</b>	GTDMP area	≥	0.00416	um <sup>2</sup>
<b>GTDMP.R.1</b>	Rectangle GTDMP outside AA must be GATE poly direction and the same with the device channel width direction of core area in a chip (GTDMP length/width > 1 and width < 0.1um)			
<b>GTDMP.R.2</b>	GTDMP form device is not allowed. 1) Maximum two AOP_GTs must be placed beside AA edge (AA INTERACT GT). 2) M0 be placed between GTDMP and AA edge, and between two GTDMPS are not allowed, except MOMDMY, ESDIO1, ESDIO2 regions.			

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### 7.2.22 P2 (GT cut) design rules

Rule number	Description	Opt.	Design Value	Unit
<b>P2.W.1</b>	P2 width in GATE poly direction, except INST and OCOVL region	=	0.048, 0.068, 0.108	um
<b>P2.W.2</b>	Maximum width of ((ALL_GT INTERACT P2) NOT DG)	$\leq$	0.092	um
<b>P2.W.3</b>	Maximum width of ((ALL_GT INTERACT P2) NOT DG) when P2 width = 0.048um	<	0.07	um
<b>P2.L.1</b>	P2 edge length in S/D direction	$\geq$	0.09	um
<b>P2.L.2</b>	P2 edge length (width $\geq$ 0.108um) in S/D direction, except OCOVL region	$\geq$	0.166	um
<b>P2.S.1a</b>	Space between two P2s, except INST region	$\geq$	0.09	um
<b>P2.S.1b</b>	Space between two P2s when one or both P2 width $\geq$ 0.108um	$\geq$	0.178	um
<b>P2.S.1c</b>	Space between P2 (width = 0.048um) in GATE poly direction, except INST region	$\geq$	0.148	um
<b>P2.S.1d</b>	At least one side space between P2 in GATE poly direction when PRL > 0.312um, except OCOVLP2A mark region	$\geq$	0.178	um
<b>P2.S.1e</b>	At least one side space between P2 (width $\geq$ 0.108um) in GATE poly direction when PRL > 0.312um	$\geq$	0.218	um
<b>P2.S.2</b>	Space between P2 and AOP_GT, except INST region	$\geq$	0.035	um
<b>P2.S.3</b>	Space between P2 and M0G in GATE poly direction (overlap is not allowed) 1) DRC checks the M0G on nearest AOP_GT with distance from P2 jog $\leq$ 0.1um. 2) Space between P2 jog's vertical edge and GT is $\leq$ 0.04um	$\geq$	0.035	um
<b>P2.S.4a</b>	Space between P2 and AOP_AA in P2 width direction (overlap is not allowed), except P2 to pick-up space = 0.014um and INST region.	$>$	0.016	um
<b>P2.EX.1</b>	P2 extension outside of AOP_GT in P2 length direction	$\geq$	0.035	um
<b>P2.EX.2</b>	P2 extension outside of AOP_GT along S/D direction when one side poly space $\geq$ 0.08um and width $\leq$ 0.02um, except GT_P96 region.	=	0.036~ 0.052	um

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Rule number	Description	Opt.	Design Value	Unit
	DRC only flags the outermost AOP_GT along S/D direction			
<b>P2.EX.3</b>	P2 extension outside of AOP_GT along S/D direction when one side poly space > 0.08um and width $\leq$ 0.024um INSIDE GT_P96 region. DRC only flags the outermost AOP_GT along S/D direction	=	0.039~0.052	um
<b>P2.EX.4</b>	P2 extension outside of AOP_GT in GATE poly direction when PRL > -0.035um, except GT jog $\leq$ 0.004um and INST region	$\geq$	0.028	um
<b>P2.EX.5</b>	ALL_GT extension outside of P2 in P2 width direction	$\geq$	0.09	um
<b>P2.EX.6</b>	P2 extension outside of (M0G AND AOP_GT) in GATE poly direction (P2 cut (M0G AND AOP_GT)) is not allowed), except M0G (width/length = 0.06/0.095~0.096um) and INST region	$\geq$	0.034	um
<b>P2.O.1</b>	Overlap of AOP_GT and P2 in GATE poly direction, except AOP_GT jog $\leq$ 0.004um and INST region	$\geq$	0.04	um
<b>P2.A.1</b>	(ALL_GT NOT P2) area, except INST region	$\geq$	0.0024	um <sup>2</sup>
<b>P2.D.1a</b>	Full chip ALL_P2 density	$\leq$	15%	
<b>P2.D.1b</b>	Full chip ALL_P2 density	$\geq$	5%	
<b>P2.D.2</b>	Maximum ALL_P2 density (window 20um*20um, stepping 10um), except INST region	$\leq$	20%	
<b>P2.R.1</b>	P2 must be a rectangle, horizontal T- and crosstype-shape, square-wave-shape, L-shape, except OCOVL region. 1. Every segment of L-, T-, crosstype- or square-wave-shape P2 INTERACT at least two AOP_GT 2. L- or square-wave-shape P2 width must be combination of 0.048/0.068um and jog must = 0.02um 3. Horizontal T-shape, crosstype-shape P2 must be symmetric in GATE poly direction			
<b>P2.R.2</b>	Width of P2 (INTERACT the second AOP_GT neighboring of GATE) in S/D direction.	=	0.048, 0.068	um
<b>P2.R.3</b>	P2 INTERACT DG is not allowed.			
<b>P2.R.4</b>	ALL_GT line end (width $\leq$ 0.024um) must fully INTERACT P2			
<b>P2.R.5</b>	(P2 not INTERACT ALL_GT) is not allowed, except OCOVL			

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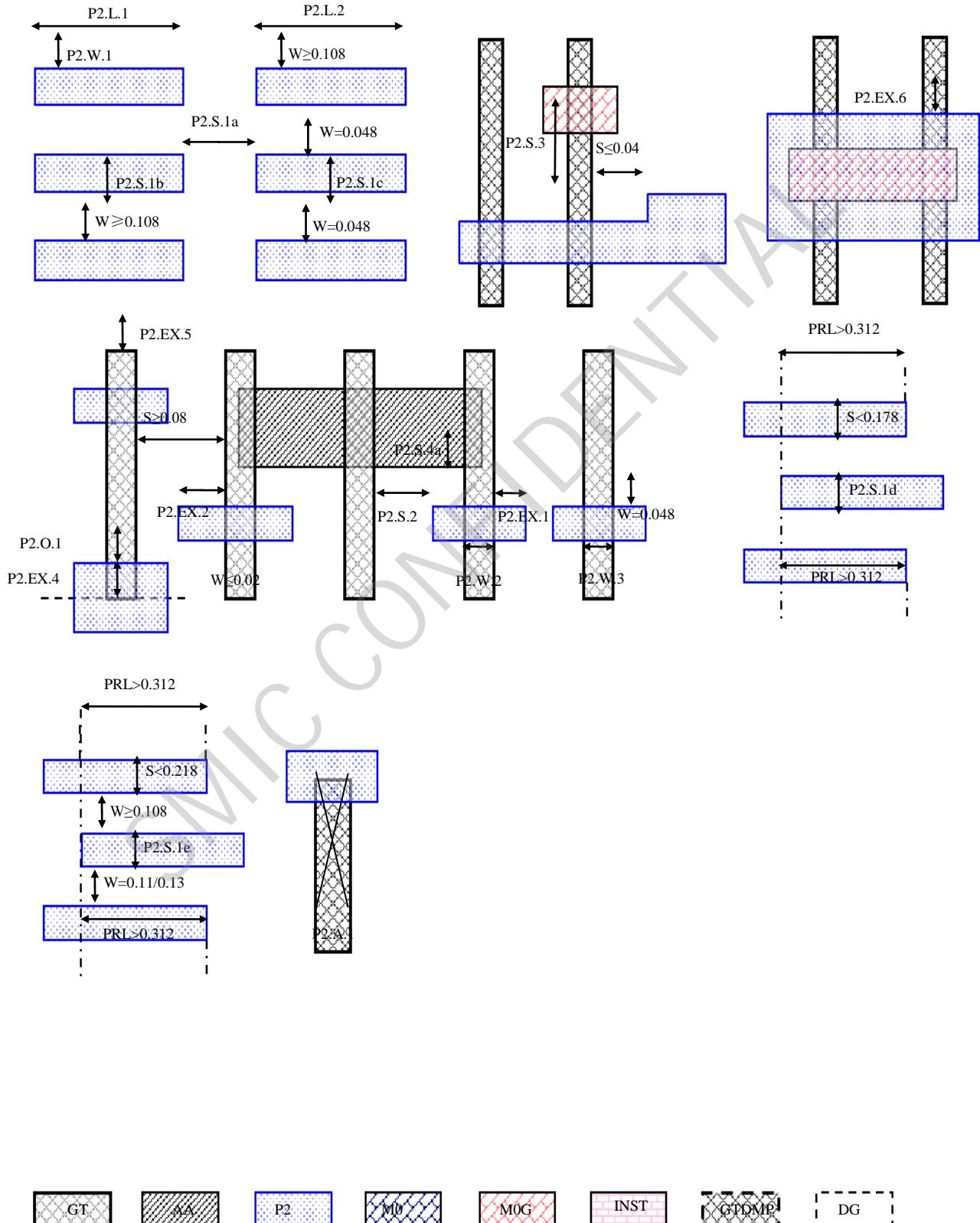
Rule number	Description	Opt.	Design Value	Unit
	region.			
<b>P2.R.6</b>	Any vertex of P2 INTERACT AOP_GT is not allowed.			
<b>P2.R.7</b>	Floating AOP_GT must be placed beside P2 edge if P2 length $\geq$ 3.1 um Floating AOP_GT definition: (AOP_GT NOT P2) NOT INTERACT M0G, except floating ((AOP_GT INTERACT M0G) INTERACT GTMK1))			

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### 7.2.23 SN design rules

Rule number	Description	Opt.	Design Value	Unit
<b>SN.W.1</b>	SN width, except INST region	$\geq$	0.192	um
<b>SN.S.1</b>	SN space, except INST region	$\geq$	0.192	um
<b>SN.S.2</b>	Space between SN in S/D direction when PRL $\geq$ 0.255um	$\geq$	0.248	um
<b>SN.S.3</b>	SN space on STI if PRL $\geq$ 0.352um, except: 1) SN space to ALL_AA < 0.082um in GATE poly direction 2) SN space to ALL_AA < 0.109um in S/D direction 3) GT_P96 and INST regions	$\geq$	0.224	um
<b>SN.S.4</b>	SN space on STI if PRL $\geq$ 0.386um INSIDE GT_P96 region, except: 1) SN space to ALL_AA < 0.082um in GATE poly direction 2) SN space to ALL_AA < 0.112um in S/D direction	$\geq$	0.224	um
<b>SN.S.5</b>	Space between SN and P+AA, except INST and DIOMK2 region	$\geq$	0.048	um
<b>SN.S.5a</b>	Space between SN and P+AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST and DIOMK2 region	$\geq$	0.065	um
<b>SN.S.6</b>	Space between SN and P+ pick-up AA, except INST and DIOMK2 region	$\geq$	0.048	um
<b>SN.S.6a</b>	Space between SN and P+ pick-up AA (AA vertical edge extend 1/2 GT width) in horizontal direction, except INST and DIOMK2 region	$\geq$	0.065	um
<b>SN.S.7</b>	Space between SN and DOP_AA (DOP_AA CUT SN is not allowed)	$\geq$	0.048	um
<b>SN.S.7a</b>	Space between SN and DOP_AA (AA vertical edge extend 1/2 GT width) in horizontal direction (DOP_AA CUT SN is not allowed)	$\geq$	0.065	um
<b>SN.S.8</b>	Space between SN and P+AA in GATE poly direction when space in S/D direction < 0.087um at each SN corner, except INST and DIOMK2 region	$\geq$	0.061	um
<b>SN.S.8a</b>	Space between SN and P+AA (AA vertical edge extend 1/2 GT width) in S/D direction when space in GATE poly direction < 0.061um at each SN corner, except INST and DIOMK2 region	$\geq$	0.079	um
<b>SN.S.9</b>	Space between SN vertical edge (edge length $\leq$ 0.296um between two concave corners with both sides length $\geq$ 0.09um) and AA (AA vertical edge extend 1/2 GT width) in S/D direction	$\geq$	0.079	um

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Rule number	Description	Opt.	Design Value	Unit
<b>SN.EN.5</b>	SN enclosure of N+AA, except MARKS and INST and DIOMK2 regions	≥	0.048	um
<b>SN.EN.5a</b>	SN enclosure of N+AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST and DIOMK2 region	≥	0.065	um
<b>SN.EN.6</b>	SN enclosure of N+ pick-up AA, except INST and DIOMK2 region	≥	0.048	um
<b>SN.EN.6a</b>	SN enclosure of N+ pick-up AA (AA vertical edge extend 1/2 GT width) in horizontal direction, except INST and DIOMK2 region	≥	0.065	um
<b>SN.EN.7</b>	SN enclosure of DOP_AA	≥	0.048	um
<b>SN.EN.7a</b>	SN enclosure of DOP_AA (AA vertical edge extend 1/2 GT width) in S/D direction, except LOGO region	≥	0.065	um
<b>SN.EN.8</b>	SN enclosure of N+AA in GATE poly direction when enclosure in S/D direction < 0.087um at each SN corner, except INST and DIOMK2 region	≥	0.061	um
<b>SN.EN.8a</b>	SN enclosure of N+AA (AA vertical edge extend 1/2 GT width) in S/D direction when enclosure in GATE poly direction < 0.061um at each SN corner, except INST and DIOMK2 region	≥	0.079	um
<b>SN.EN.9</b>	SN line-end (vertical width ≤ 0.296um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST region.	≥	0.079	um
<b>SN.EX.1</b>	SN extension outside of NMOS GATE for core region (Extension ≤ 0um is not allowed), except MARKS and INST regions	≥	0.048	um
<b>SN.EX.2</b>	SN extension outside of NMOS GATE for I/O region (Extension ≤ 0um is not allowed), except DIOMK2 region	≥	0.096	um
<b>SN.A.1a</b>	SN area, except INST region	≥	0.087	um <sup>2</sup>
<b>SN.A.1b</b>	SN area, ((((SN NOT DG) NOT (((NW OR PSUB) OR VARMOS) OR DMPNP)) su 0.095um) sd 0.19um) su 0.095um) ((((SN AND DG) NOT (((NW NOT PSUB) OR VARMOS) OR DMPNP)) su 0.095um) sd 0.19um) su 0.095um)	≥	0.087	um <sup>2</sup>
<b>SN.A.2a</b>	SN enclosed area, except INST region	≥	0.087	um <sup>2</sup>
<b>SN.A.2b</b>	SN enclosed area, except INST region	≥	0.087	um <sup>2</sup>

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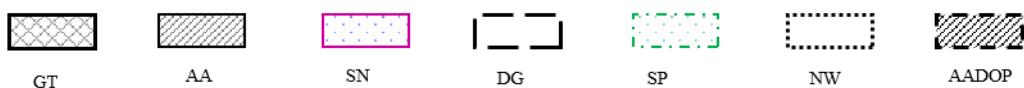
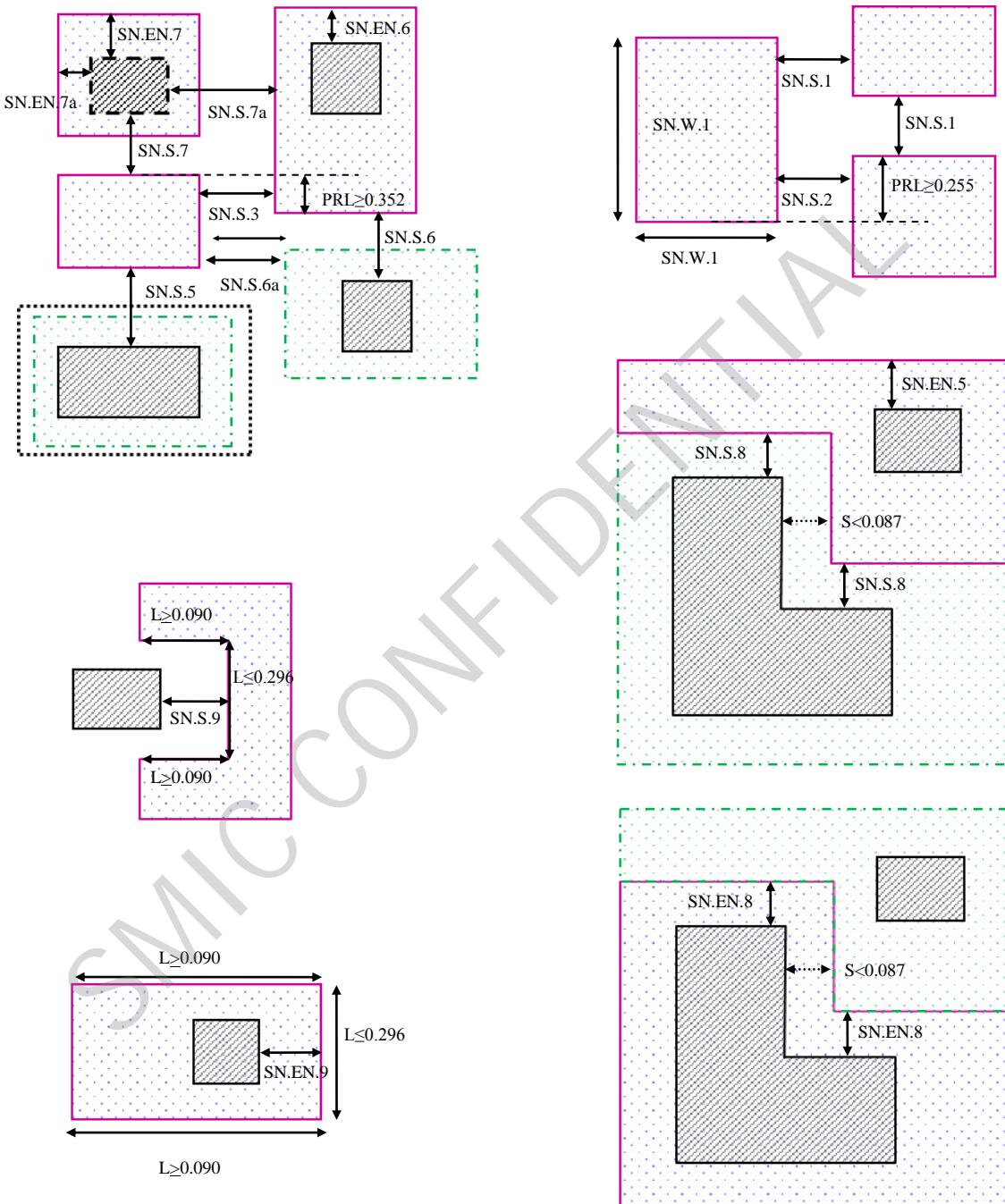
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<b>SN.R.1</b>	SP and SN interact the same ALL_AA is not allowed, except DIOMK2 region.			
<b>SN.R.2</b>	SN and SP overlap is not allowed.			

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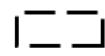
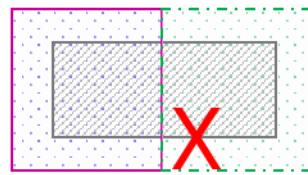
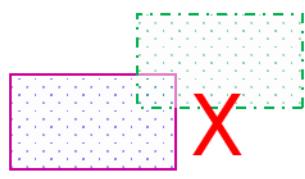
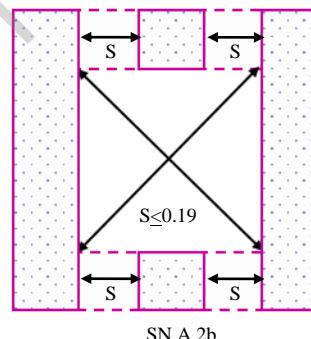
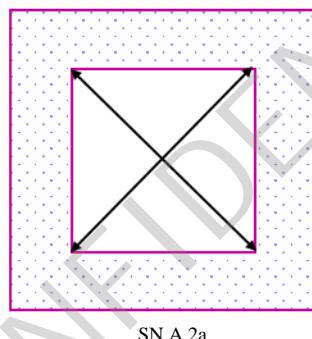
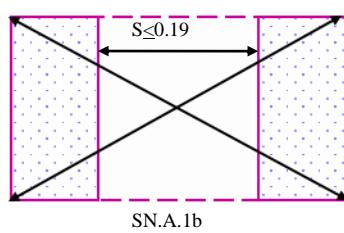
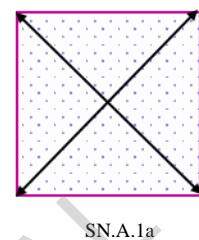
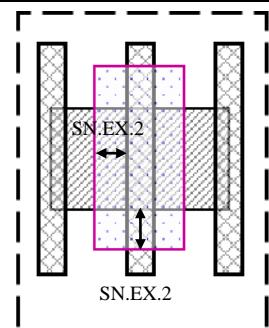
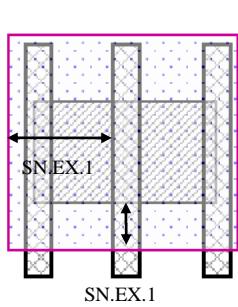


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### 7.2.24 SP design rules

Rule number	Description	Opt.	Design Value	Unit
SP.W.1	SP width, except INST region and 45-degree SP in MARKS region	≥	0.192	um
SP.S.1	SP space, except INST region	≥	0.192	um
SP.S.2	Space between SP in S/D direction when PRL ≥ 0.255um	≥	0.248	um
SP.S.3	SP space on STI if PRL ≥ 0.352um, except: 1) SP space to ALL_AA < 0.082um in GATE poly direction 2) SP space to ALL_AA < 0.109um in S/D direction 3) GT_P96 and INST regions	≥	0.224	um
SP.S.4	SP space on STI if PRL ≥ 0.386um in GT_P96 region, except: 1) SP space to ALL_AA < 0.082um in GATE poly direction 2) SP space to ALL_AA < 0.112um in S/D direction	≥	0.224	um
SP.S.5	Space between SP and N+AA, except INST and DIOMK2 region	≥	0.048	um
SP.S.5a	Space between SP and N+AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST and DIOMK2 region	≥	0.065	um
SP.S.6	Space between SP and N+ pick-up AA, except INST and DIOMK2 region	≥	0.048	um
SP.S.6a	Space between SP and N+ pick-up AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST and DIOMK2 region	≥	0.065	um
SP.S.7	Space between SP and DOP_AA (DOP_AA CUT SP is not allowed)	≥	0.048	um
SP.S.7a	Space between SP and DOP_AA (AA vertical edge extend 1/2 GT width) in S/D direction (DOP_AA CUT SP is not allowed)	≥	0.065	um
SP.S.8	Space between SP and N+AA in GATE poly direction when space in S/D direction < 0.087um at each SP corner, except INST and DIOMK2 region	≥	0.061	um
SP.S.8a	Space between SP and N+AA (AA vertical edge extend 1/2 GT width) in S/D direction when space in GATE poly direction < 0.061um at each SP corner, except INST and DIOMK2 region	≥	0.079	um
SP.S.9	Space between SP vertical edge (edge length ≤ 0.296um between two concave corners with both sides length ≥ 0.09um) and AA (AA vertical edge extend 1/2 GT width) in S/D direction	≥	0.079	um

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Rule number	Description	Opt.	Design Value	Unit
<b>SP.EN.5</b>	SP enclosure of P+AA, except INST and DIOMK2 region	≥	0.048	um
<b>SP.EN.5a</b>	SP enclosure of P+AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST and DIOMK2 region	≥	0.065	um
<b>SP.EN.6</b>	SP enclosure of P+ pick-up AA, except MARKS, INST and DIOMK2 regiond.	≥	0.048	um
<b>SP.EN.6a</b>	SP enclosure of P+ pick-up AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST and DIOMK2 region	≥	0.065	um
<b>SP.EN.7</b>	SP enclosure of DOP_AA	≥	0.048	um
<b>SP.EN.7a</b>	SP enclosure of DOP_AA (AA vertical edge extend 1/2 GT width) in S/D direction	≥	0.065	um
<b>SP.EN.8</b>	SP enclosure of P+AA in GATE poly direction when enclosure in S/D direction < 0.087um at each SP corner, except INST and DIOMK2 region	≥	0.061	um
<b>SP.EN.8a</b>	SP enclosure of P+AA (AA vertical edge extend 1/2 GT width) in S/D direction when enclosure in GATE poly direction < 0.061um at each SP corner, except INST and DIOMK2 region	≥	0.079	um
<b>SP.EN.9</b>	SP line-end (vertical width ≤ 0.296um between two consecutive 90-90 degree corners with both sides length ≥ 0.09um) enclosure of AA (AA vertical edge extend 1/2 GT width) in S/D direction, except INST region	≥	0.079	um
<b>SP.EX.1</b>	SP extension outside of PMOS GATE for core region (Extension ≤ 0um is not allowed), except MARKS and INST regions	≥	0.048	um
<b>SP.EX.2</b>	SP extension outside of PMOS GATE for I/O region (Extension ≤ 0um is not allowed), except DIOMK2 region	≥	0.096	um
<b>SP.A.1a</b>	SP area, except INST region	≥	0.087	um <sup>2</sup>
<b>SP.A.1b</b>	SP area, ((((SP NOT ((DG OR VARMOS) OR DMPNP)) AND NW) su 0.095um) sd 0.19um) su 0.095um), ((((((SP AND DG) AND NW) NOT (VARMOS OR DMPNP)) su 0.095um) sd 0.19um) su 0.095um)	≥	0.087	um <sup>2</sup>
<b>SP.A.2a</b>	SP enclosed area	≥	0.087	um <sup>2</sup>

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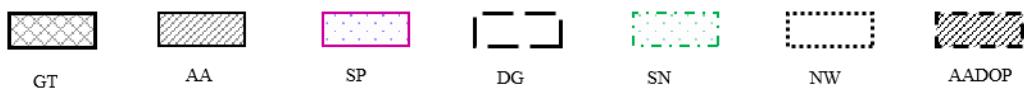
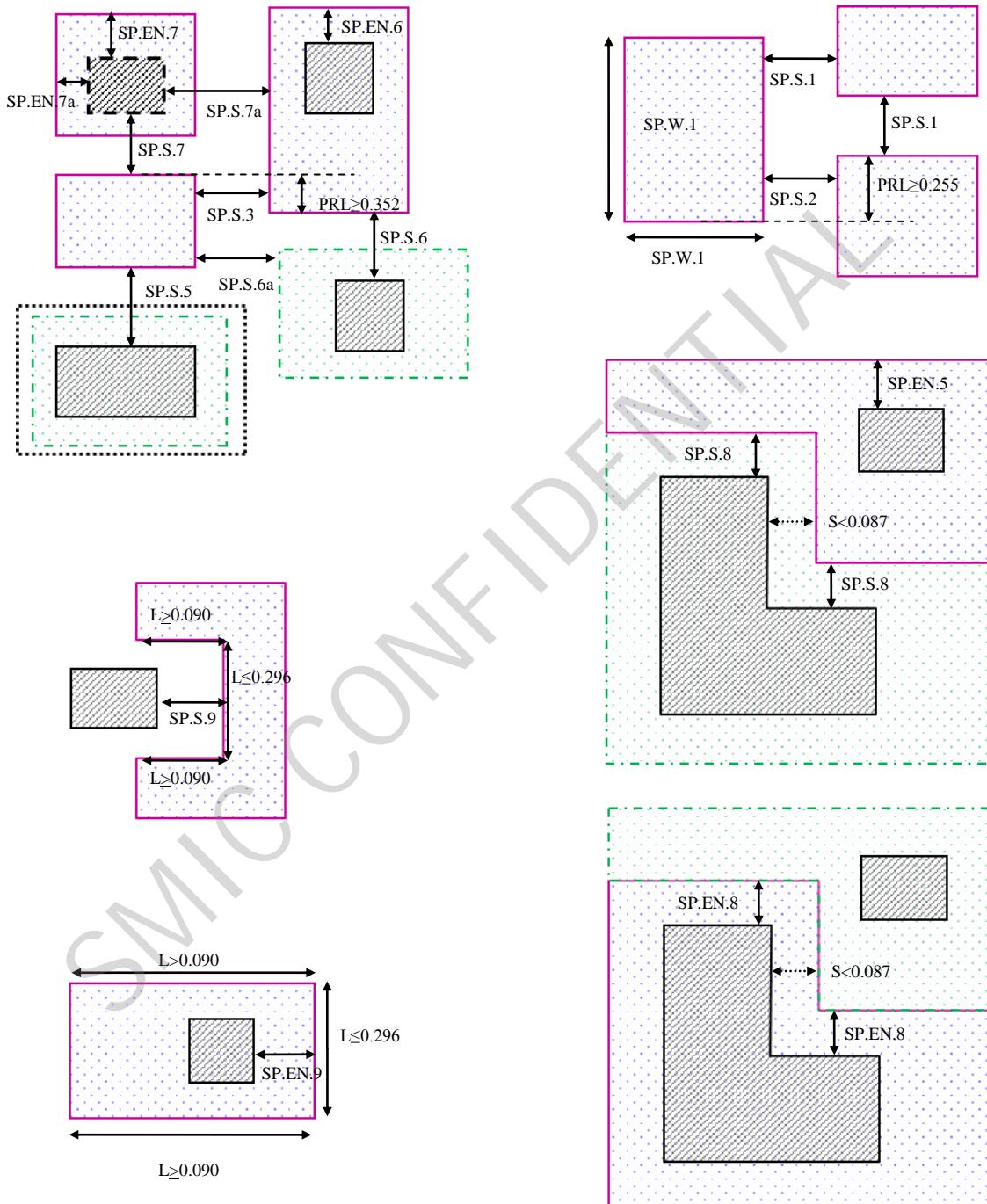
Rule number	Description	Opt.	Design Value	Unit
SP.A.2b	SP enclosed area, ((((SP NOT ((DG OR VARMOS) OR DMPNP)) AND NW) su 0.095um) sd 0.19um) su 0.095um), ((((((SP AND DG) AND NW) NOT (VARMOS OR DMPNP)) su 0.095um) sd 0.19um) su 0.095um)	≥	0.087	um <sup>2</sup>

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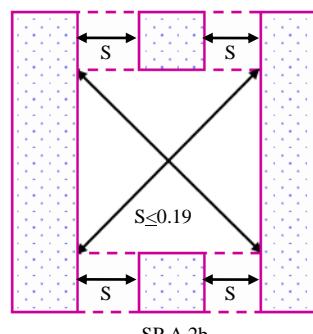
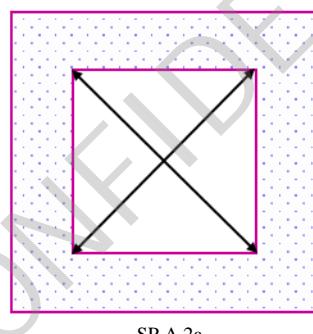
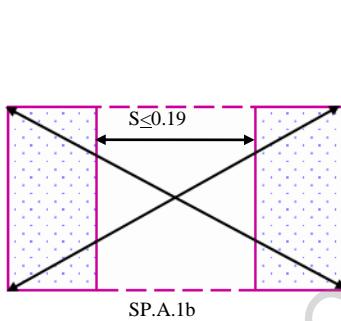
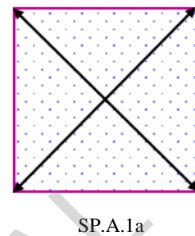
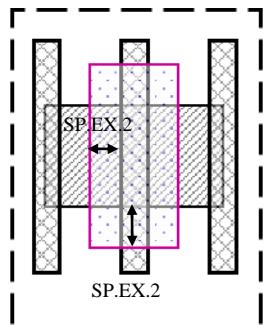
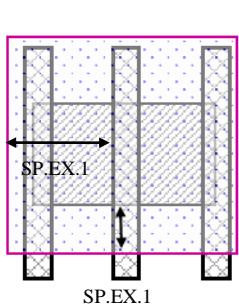
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### 7.2.25 Strained S/D design rules

Rule number	Description	Opt.	Design Value	Unit
<b>SSD.DN.1</b>	PSR open ratio should be as uniform as possible over the chip. PSR open ratio definition: $(((((SP - INST) - PSRBL) su 0.095) sd 0.19) su 0.095) + (((((SP * INST) - PSRBL) su 0.086) sd 0.172) su 0.086)) + SPDUM) * ALL_AA) - (ALL_GT))$ density across full chip	$\geq$	5.8%	
<b>SSD.DN.1a</b>	PSR open ratio should be as uniform as possible over the chip. PSR open ratio definition: $((((((SP - INST) - PSRBL) su 0.095) sd 0.19) su 0.095) + (((((SP * INST) - PSRBL) su 0.086) sd 0.172) su 0.086)) + SPDUM) * ALL_AA) - (ALL_GT))$ density across full chip	$\leq$	18%	
<b>SSD.DN.2</b>	NSR open ratio be as uniform as possible over the chip . NSR open ratio definition: $(((((((!SP) - RESNW) - NSRBL) - INST) su 0.095) sd 0.19) su 0.095) + ((((!SP) * INST) - NSRBL) su 0.086) sd 0.172) su 0.086)) - SPDUM) * ALL_AA) - (ALL_GT))$ density across full chip	$\geq$	5.8%	
<b>SSD.DN.2a</b>	NSR open ratio should be as uniform as possible over the chip . NSR open ratio definition: $(((((((!SP) - RESNW) - NSRBL) - INST) su 0.095) sd 0.19) su 0.095) + ((((!SP) * INST) - NSRBL) su 0.086) sd 0.172) su 0.086)) - SPDUM) * ALL_AA) - (ALL_GT))$ density across full chip	$\leq$	18%	

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### 7.2.26 M0 design rules

Rule number	Description	Opt.	Design Value	Unit
<b>M0.W.1</b>	M0 width, except MARKS and OCOVL regions	=	0.04, 0.042, 0.054	um
<b>M0.W.2</b>	M0 width in S/D direction when M0 INTERACT (AA INTERACT GT (width $\geq$ 0.07um)), except MARKS region	=	0.054	um
<b>M0.L.1</b>	M0 length (width = 0.04um), except (M0 interact TRCMK) and OCOVL region	$\geq$	0.114	um
<b>M0.L.1a</b>	M0 length (width = 0.042um), except OCOVL region	$\geq$	0.158	um
<b>M0.L.2</b>	M0 length (width = 0.054um)	$\geq$	0.158	um
<b>M0.L.3</b>	M0 length (width = 0.04um, space = 0.063/0.066 um)	$\geq$	0.158	um
<b>M0.L.4</b>	Length of (AOP_M0 NOT (M0C OR M0CDMP)) (AOP_M0 width = 0.04/0.042um), except INST region and ((AOP_M0 (width = 0.04/0.042um) NOT (M0C OR M0CDMP) (width = 0.052um)) NOT INTERACT ALL_AA), except RSPMK1 region	$\geq$	0.061	um
<b>M0.L.5</b>	Length of (AOP_M0 NOT AOP_M0C) (AOP_M0 width = 0.04/0.042um)	$\leq$	5.1	um
<b>M0.S.1</b>	Space between M0	$\geq$	0.05	um
<b>M0.S.2</b>	Space between M0 (width = 0.04um) and M0 (width = 0.042um)	$\geq$	0.192	um
<b>M0.S.3a</b>	Space between the short side of rectangular AOP_M0 (width = 0.054um) and AOP_M0 when PRL > -0.136um	$\geq$	0.119	um
<b>M0.S.3b</b>	Space between the long side of rectangular AOP_M0 (width = 0.054um) and AOP_M0 when PRL $\geq$ -0.119um	$\geq$	0.134	um
<b>M0.S.4</b>	Space between short side of AOP_M0 (width = 0.04/0.042um, PRL > -0.05um), except short side space $\geq$ 0.086um (length $\geq$ 0.229um, either one short side INTERACT M0C (width = 0.052um), short side (NOT INTERACT M0C) space to M0G $\geq$ 0.04um)	$\geq$	0.096	um
<b>M0.S.4a</b>	Space between the long side of rectangular AOP_M0 and AOP_M0 (width = 0.04um) when PRL > -0.09um	$\geq$	0.05	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M0.S.4b</b>	Space between the long side of rectangular AOP_M0 and AOP_M0 (width = 0.04um) when PRL > -0.096um INSIDE GT_P96 region	$\geq$	0.056	um
<b>M0.S.5b</b>	Space between the long side of rectangular AOP_M0 and AOP_M0 (width = 0.042um) when PRL > -0.096um inside GT_P96 region	$\geq$	0.054	um
<b>M0.S.6</b>	Forbidden zones $((W1+S1+W1)+S2+(W1+S1+W1)) = 0.342\text{um}$ when $W1 = 0.04\text{um}$ , $S1 = 0.066\text{um}$ , $S2 = 0.05\text{um}$ is not allowed. 1) $W1$ is AOP_M0 width; 2) $S1$ is horizontal space between two AOP_M0 (M0 line-end extend by 0.015um) with PRL > 0um; 3) $S2$ is space between two AOP_M0 P106 region.			
<b>M0.S.6a</b>	Space between AOP_M0 (width = 0.04um) and AOP_M0 in S/D direction when PRL > 0.01um, except GT_P96 and INST region.	=	0.05, 0.066, 0.14, 0.172, $\geq 0.23$	um
<b>M0.S.6c</b>	Space between AOP_M0 (width = 0.04um, line end extend 0.015um) and AOP_M0 in S/D direction inside GT_P96 region, except DMCB1 region.	=	0.056, 0.152, $\geq 0.248$	um
<b>M0.S.6d</b>	Space between AOP_M0 (width = 0.042um, line end extend 0.015um) and AOP_M0 in S/D direction (INSIDE GT_P96)	=	0.054, 0.15, $\geq 0.246$	um
<b>M0.S.7</b>	Space between (ALL_M0 NOT M0C) line-end and AOP_AA when PRL > -0.025um, except INST region	$\geq$	0.037	um
<b>M0.S.8</b>	Space between AOP_M0 (width = 0.04/0.042um) and AOP_GT (Overlap is not allowed)	$\geq$	0.015	um
<b>M0.S.8a</b>	Space between AOP_M0 (width = 0.04um) and AOP_GT (width = 0.016/0.032um)	$\geq$	0.017	um
<b>M0.S.8b</b>	Space between AOP_M0 (width = 0.04um) and AOP_GT (width = 0.018um)	$\geq$	0.016	um
<b>M0.S.8c</b>	Space between AOP_M0 (width = 0.04um) and AOP_GT (width = 0.02um)	$\geq$	0.015	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M0.S.9</b>	Space between AOP_M0 (width = 0.04/0.042um, INSIDE GT_P96) and AOP_GT (Overlap is not allowed) , except DMCB1 region.	$\geq$	0.016	um
<b>M0.S.9a</b>	Space between AOP_M0 (width = 0.04um, INSIDE GT_P96) and AOP_GT (width = 0.016um)	$\geq$	0.02	um
<b>M0.S.9b</b>	Space between AOP_M0 (width = 0.04um, INSIDE GT_P96) and AOP_GT (width = 0.018um)	$\geq$	0.019	um
<b>M0.S.9c</b>	Space between AOP_M0 (width = 0.04um, INSIDE GT_P96) and AOP_GT (width = 0.02um)	$\geq$	0.018	um
<b>M0.S.9d</b>	Space between AOP_M0 (width = 0.04um, INSIDE GT_P96) and AOP_GT (width = 0.022um)	$\geq$	0.017	um
<b>M0.S.9e</b>	Space between AOP_M0 (width = 0.04um, INSIDE GT_P96) and AOP_GT (width = 0.024um)	$\geq$	0.016	um
<b>M0.S.9f</b>	Space between AOP_M0 (width = 0.042um, INSIDE GT_P96) and AOP_GT (width = 0.016um)	$\geq$	0.019	um
<b>M0.S.9g</b>	Space between AOP_M0 (width = 0.042um, INSIDE GT_P96) and AOP_GT (width = 0.018um)	$\geq$	0.018	um
<b>M0.S.9h</b>	Space between AOP_M0 (width = 0.042um, INSIDE GT_P96) and AOP_GT (width = 0.02um)	$\geq$	0.017	um
<b>M0.S.9i</b>	Space between AOP_M0 (width = 0.042um, INSIDE GT_P96) and AOP_GT (width = 0.022um)	$\geq$	0.016	um
<b>M0.S.10</b>	Space between AOP_M0 and AOP_GT (width $\geq$ 0.07um)	$\geq$	0.032	um
<b>M0.S.10a</b>	Space between AOP_M0 (width = 0.054um) and AOP_GT (Overlap is not allowed)	$\geq$	0.032	um
<b>M0.S.10b</b>	Space between (AOP_M0 NOT AOP_M0C) and AOP_GT line-end, except small AOP_GT jog $\leq$ 0.004um and DMCMK1 region	$\geq$	0.046	um
<b>M0.S.11</b>	Space between M0 (width = 0.04um, OUTSIDE GT_P96) and AOP_GT (one side poly space $\geq$ 0.08um, width = 0.016/0.018/0.02um respectively)	$\geq$	0.031, 0.029, 0.027	um
<b>M0.S.11a</b>	Space between M0 (width = 0.04/0.042um, INSIDE GT_P96) and AOP_GT (one side poly space $>$ 0.08um, width =	$\geq$	0.034, 0.032,	um

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Rule number	Description	Opt.	Design Value	Unit
	0.016/0.018/0.02/0.022/0.024um respectively)		0.03, 0.028, 0.026	
<b>M0.S.12</b>	Space between M0 (width = 0.054um) and AOP_GT (one side poly space $\geq$ 0.118um, width = 0.016/0.018/0.02um respectively)	$\geq$	0.05, 0.048, 0.046	um
<b>M0.S.13</b>	Space between FIELD (AOP_GT NOT P2) and AOP_M0 (FIELD (AOP_GT NOT P2) width $<$ 0.096um, one side space to ((GT (INSIDE DG) SIZING 0.041um) AND GT) = 0.118~0.119um, the other side space to (AOP_GT NOT P2) $\geq$ 0.15um)	$\geq$	0.054	um
<b>M0.S.15</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and AOP_AA (AA vertical edge extend 1/2 GT width) (maximum delta V $>$ 1.05V, 0.95V+10%) in S/D direction.	$\geq$	0.032	um
<b>M0.S.16</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and AOP_AA (maximum delta V $>$ 1.98V, 1.8V+10%)	$\geq$	0.043	um
<b>M0.S.17</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and AOP_AA (AA vertical edge extend 1/2 GT width) (maximum delta V $>$ 1.98V, 1.8V+10%) in S/D direction.	$\geq$	0.061	um
<b>M0.S.18</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and AOP_AA (maximum delta V $>$ 3.63V, 3.3V+10%)	$\geq$	0.056	um
<b>M0.S.19</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and AOP_AA (AA vertical edge extend 1/2 GT width) (maximum delta V $>$ 3.63V, 3.3V+10%) in S/D direction.	$\geq$	0.074	um
<b>M0.S.20a</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and ((AOP_GT NOT P2) INTERACT (AA OR M0G)) (maximum delta V $>$ 1.05V, 0.95V+10%) Except (GTDMP INSIDE DG) case	$\geq$	0.032	um
<b>M0.S.20b</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and (AOP_GT NOT P2) (maximum delta V $>$ 1.98V, 1.8V+10%)	$\geq$	0.047	um
<b>M0.S.20c</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and (AOP_GT NOT P2) (maximum delta V $>$ 2.75V, 2.5V+10%)	$\geq$	0.053	um
<b>M0.S.20d</b>	Space between (AOP_M0 NOT (M0C OR M0CDMP)) and (AOP_GT NOT P2) (maximum delta V $>$ 3.63V, 3.3V+10%)	$\geq$	0.069	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M0.S.21</b>	Space between (M0 NOT M0C) (maximum delta V > 3.63V, 3.3V+10%)	≥	0.069	um
<b>M0.EX.1</b>	AA extention outside of the short side of M0 (Extension ≤ 0um is allowed), except INST region	≤	0.007	um
<b>M0.EX.2</b>	AA extension outside of the long side of M0 (Extension ≤ 0 um is not allowed)	≥	0.025	um
<b>M0.EX.3</b>	AA extension outside of M0 in S/D direction inside GT_P96 (Extention ≤ 0um is not allowed)	≥	0.028	um
<b>M0.EX.4</b>	AA (INTERACT ALL_GT (width ≥ 0.07um)) extension outside of the long side of M0 (Extension ≤ 0 um is not allowed)	≥	0.067	um
<b>M0.A.1</b>	M0 area, except (M0 interact TRCMK) region	≥	0.0046	um <sup>2</sup>
<b>M0.D.1</b>	ALL_M0 density (window 125um*125um, stepping 62.5um), except MARKS, RESP1, LOGO regions	≥	5%	
<b>M0.D.2</b>	ALL_M0 density (window 20um*20um, stepping 10um), except MARKS, LOGO, OCOVL, RESP1, (NODMF su 1um) regions	≥	1.2%	
<b>M0.D.3</b>	ALL_M0 density (window 20um*20um, stepping 10um), except INST, OCOVL regions	≤	40%	
<b>M0.R.1</b>	ALL_M0 must be rectangular and orthogonal to grid, except MARKS region.			
<b>M0.R.2</b>	ALL_M0 must be GATE poly direction and parallel to GT, except OCOVL region.			
<b>M0.R.3</b>	M0 (width = 0.04/0.042um) overlap with (DG OR NW resistor) is not allowed.			
<b>M0.R.4</b>	The number of ALL_M0 (width = 0.04/0.042um and at least one ALL_M0 length ≤ 0.148um) in one group ALL_M0 group definition: 1) ALL_M0 space ≤ 0.066um 2) ALL_M0 PRL ≥ 0.065um DRC flags ((ALL_M0 SIZING 0.043 um) SIZING -0.043um) in ALL_M0 short side direction	≥	5	
<b>M0.R.5</b>	Maximum delta V ≥ 5.6V is not allowed, when: 1. Space between (AOP_M0 NOT AOP_M0C) is < 0.7um			

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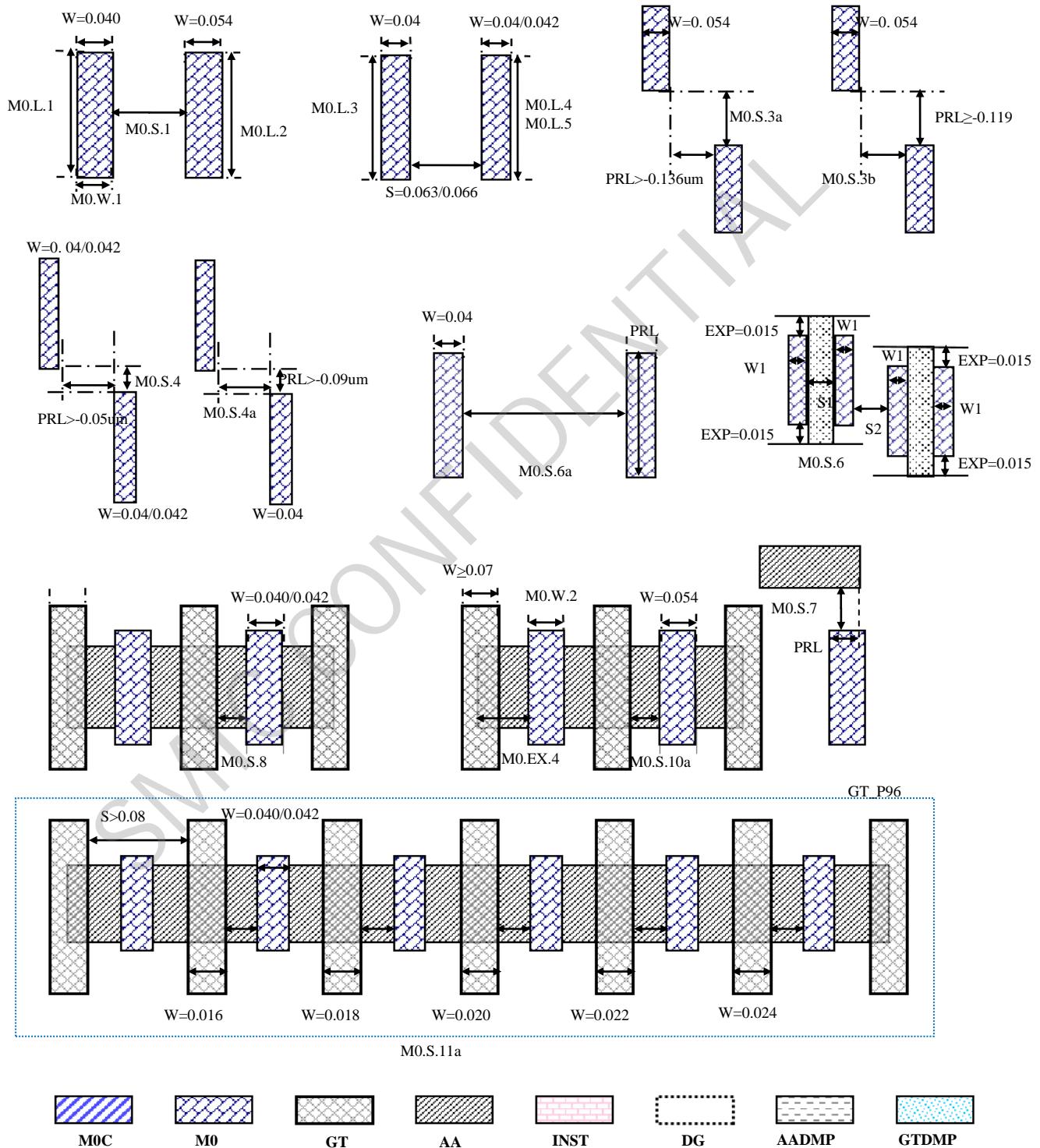
Rule number	Description	Opt.	Design Value	Unit
	2. Space between (AOP_M0 NOT AOP_M0C) and AOP_AA is < 0.77um 3. Space between (AOP_M0 NOT AOP_M0C) and (AOP_GT NOT P2) is < 0.72um			
<b>M0.R.6</b>	(AOP_M0 INTERACT AOP_GT) is not allowed.			
<b>M0.R.7</b>	((AA INTERACT GT) NOT GT) must INTERACT M0, except INST region			
<b>M0.R.8</b>	Only one M0 is allowed on single S/D region, except ESDIO1 and ESDIO2 regions.			
<b>M0.R.9</b>	M0 (width = 0.042um) must inside GT_P96			

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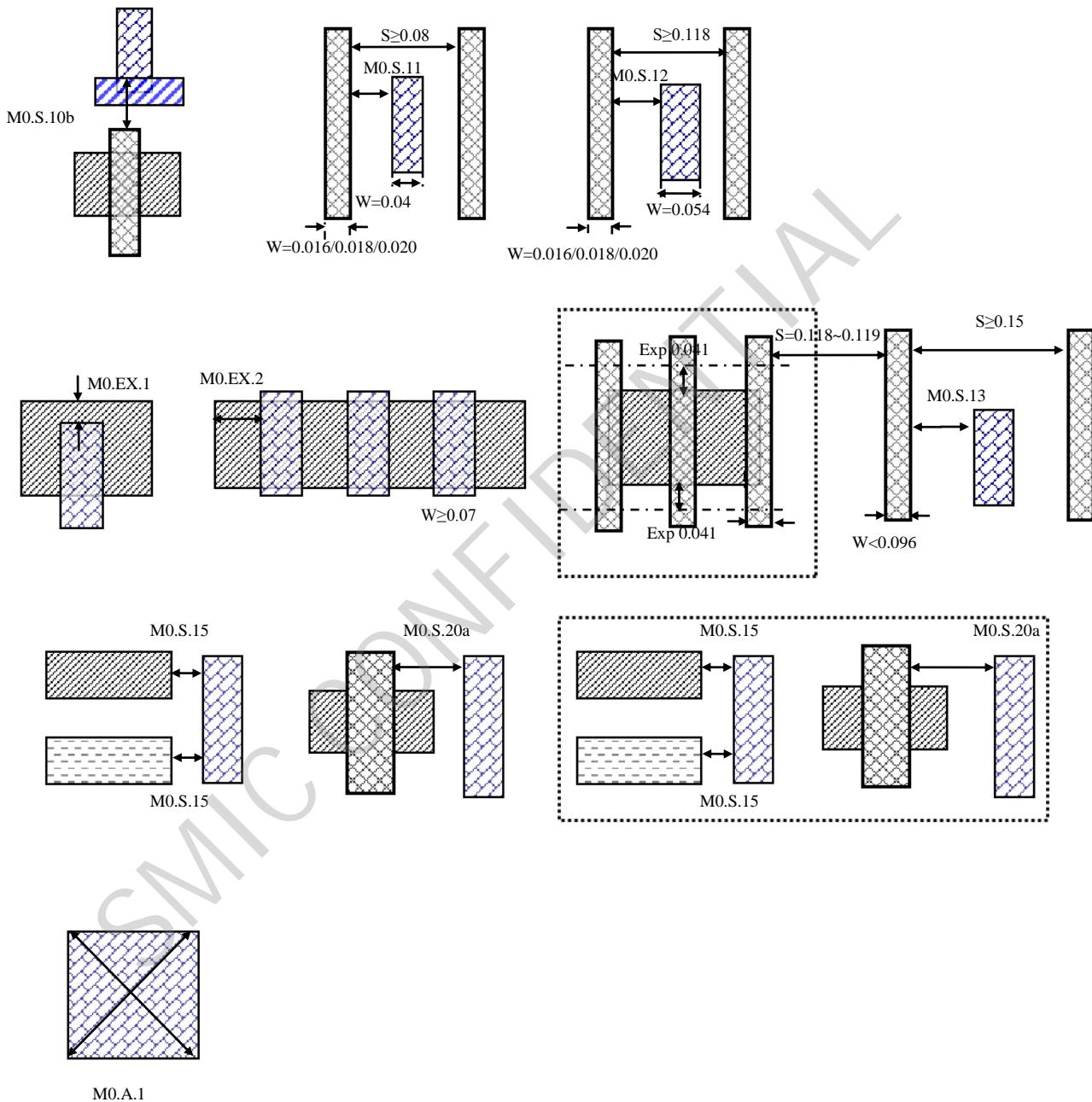


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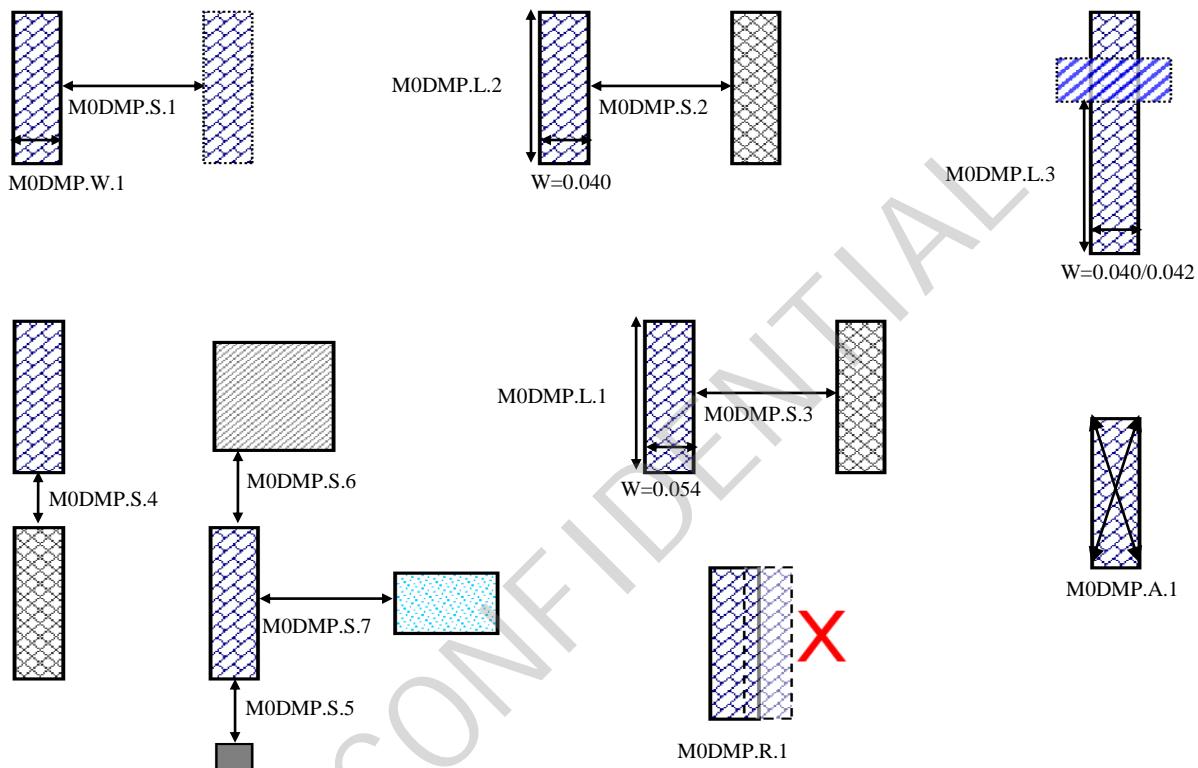
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### 7.2.27 M0DMP dummy rules (data type 8)

Rule number	Description	Opt.	Design Value	Unit
<b>M0DMP.W.1</b>	M0DMP width	=	0.04, 0.042, 0.054	um
<b>M0DMP.L.1</b>	M0DMP length (width = 0.054/0.042um)	≥	0.158	um
<b>M0DMP.L.2</b>	M0DMP length (width = 0.04um)	≥	0.114	um
<b>M0DMP.L.3</b>	Maximum length of (M0DMP (width= 0.04/0.042um) NOT M0CDMP )	≤	5.1	um
<b>M0DMP.S.1</b>	Space between M0DMP and AOP_M0 (Overlap with M0 is not allowed)	≥	0.05	um
<b>M0DMP.S.2</b>	Space between M0DMP and AOP_GT (M0DMP width = 0.04/0.042um) (Overlap is not allowed)	≥	0.015	um
<b>M0DMP.S.3</b>	Space between M0DMP and AOP_GT (M0DMP width = 0.054 um) (Overlap is not allowed)	≥	0.032	um
<b>M0DMP.S.4</b>	Space between (M0DMP NOT M0CDUM) line-end and AOP_GT (Except AOP_GT jogs $\leq 0.003\text{um}$ )	≥	0.046	um
<b>M0DMP.S.5</b>	Space between M0DMP and V0 (Overlap is not allowed)	≥	0.039	um
<b>M0DMP.S.6</b>	Space between (M0DMP NOT M0CDUM) and AOP_AA in GATE poly direction (Overlap with AA is not allowed)	≥	0.037	um
<b>M0DMP.S.7</b>	Space between M0DMP and AOP_M0G (Overlap with M0G is not allowed)	≥	0.039	um
<b>M0DMP.A.1</b>	M0DMP area	≥	0.0046	um
<b>M0DMP.R.1</b>	M0DMP INTERACT M0 is not allowed.			

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### 7.2.28 M0C design rules

M0C is a drawn layer and used for M0 cut,  $n \geq 0$  and n is an integer.

Rule number	Description	Opt.	Design Value	Unit
<b>M0C.W.1</b>	M0C width in GATE poly direction, except INST and OCOVL regions	=	0.048, 0.051, 0.052, 0.082, 0.108	um
<b>M0C.W.2</b>	AOP_M0C width in GATE poly direction when INTERACT ALL_M0 (width = 0.054um)	=	0.082, 0.108	um
<b>M0C.W.3</b>	DOP_M0C width in GATE poly direction	=	0.052, 0.082, 0.36	um
<b>M0C.W.4</b>	M0C width when M0C interact RSPMK1	=	0.051	um
<b>M0C.L.1</b>	AOP_M0C edge length in S/D direction	$\geq$	0.09	um
<b>M0C.L.2</b>	AOP_M0C (width = 0.048um) edge length in S/D direction, except INST region	$\geq$	0.36	um
<b>M0C.L.3</b>	AOP_M0C (width = 0.052um) edge length in S/D direction	$\geq$	0.18	um
<b>M0C.L.4</b>	AOP_M0C edge length in S/D direction (AOP_M0C width = 0.082/0.108um, INTERACT AOP_M0 (width = 0.054um))	$\geq$	0.36	um
<b>M0C.L.5</b>	M0C (width = 0.051um) length in S/D direction, except GT_P96 region	=	0.090*(n+1)	um
<b>M0C.L.5a</b>	AOP_M0C (width = 0.051um) length in S/D direction INSIDE GT_P96 region	=	0.096*(n+1)	um
<b>M0C.L.6</b>	DOP_M0C (width = 0.36um) edge length in S/D direction	=	0.18	um
<b>M0C.S.1</b>	Space between AOP_M0C, except RSPMK1, INST, M0C (width = 0.051um) and M0C (width = 0.052um) space = 0.043um in GATE poly direction when PRL = 0um) (overlap is not allowed)	$\geq$	0.044	um
<b>M0C.S.2</b>	Space between AOP_M0C in GATE poly direction when PRL > 0um, except M0C space = 0.014um in RSPMK1 region	$\geq$	0.054	um
<b>M0C.S.3</b>	Space between M0C and AOP_M0C (width = 0.048, 0.082, 0.108um) in GATE poly direction when PRL >	$\geq$	0.073	um

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Rule number	Description	Opt.	Design Value	Unit
	0um			
M0C.S.4	Space between AOP_M0C in S/D direction	$\geq$	0.09	um
M0C.S.5	Space between M0C and (M0C OR M0CDMP) (width = 0.048um) in S/D direction, except INST region	$\geq$	0.18	um
M0C.S.6	Space between M0C and (M0C OR M0CDMP) (width = 0.051um) in S/D direction, except GT_P96 region	$=$	0.09, 0.18, $\geq 0.27$	um
M0C.S.6a	Space between M0C and (M0C OR M0CDMP) (width = 0.051um) in S/D direction, INSIDE GT_P96 region	$=$	0.096, 0.192, $\geq 0.288$	um
M0C.S.6b	Space between DOP_M0C (width = 0.36um) in S/D direction when PRL > -0.36um	$\geq$	0.18	um
M0C.S.6c	Space between DOP_M0C (width = 0.36um) in GATE poly direction when PRL > -0.18um	$\geq$	0.36	um
M0C.S.6d	Space between DOP_M0C (width = 0.36um) and AOP_M0C (width = 0.052/0.082um) or M0CDUM	$\geq$	0.74	um
M0C.S.7	Space between AOP_M0C and ALL_M0	$\geq$	0.012	um
M0C.S.8	Space between AOP_M0C and ALL_M0 in S/D direction	$\geq$	0.025	um
M0C.S.8a	Space between AOP_M0C and AOP_M0 in S/D direction INSIDE GT_P96 region, except DMCB1 region	$\geq$	0.028	um
M0C.S.9	Space between AOP_M0C (width = 0.082/0.108um) and ALL_M0 (width = 0.054um) in S/D direction	$\geq$	0.067	um
M0C.S.10	Space between DOP_M0C (width = 0.36um) and ALL_M0 (overlap is not allowed)	$\geq$	0.148	um
M0C.S.11	Space between DOP_M0C (width = 0.36um) and ALL_M0G (overlap is not allowed)	$\geq$	0.148	um
M0C.S.12	Space between M0C concave corner and (M0 AND AA), except M0C jog $\leq 0.002\text{um}$	$\geq$	0.054	um
M0C.O.1	M0C (width = 0.048um) overlap ALL_M0 in GATE poly direction	$=$	0.024, 0.048	um
M0C.O.2	M0C (width = 0.051um) overlap ALL_M0 in GATE poly direction	$=$	0.026, 0.051	um
M0C.O.3	AOP_M0C (width = 0.052um) overlap ALL_M0 in	$=$	0.026, 0.052	um

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Rule number	Description	Opt.	Design Value	Unit
	GATE poly direction			
<b>M0C.O.4</b>	AOP_M0C (width = 0.082um) overlap ALL_M0 in GATE poly direction	=	0.041, 0.082	um
<b>M0C.O.5</b>	M0C (width = 0.108um) overlap ALL_M0 in GATE poly direction	=	0.054, 0.108	um
<b>M0C.O.6</b>	AOP_M0C overlap AOP_AA (INTERACT the same AOP_M0) in GATE poly direction	$\leq$	0.01	um
<b>M0C.EX.1</b>	AOP_M0C extension outside of AOP_M0 in S/D direction, except OCOVL region DRC only flags the outermost M0 along M0C length direction.	=	0.025~0.102	um
<b>M0C.EX.1a</b>	AOP_M0C extension outside of AOP_M0 in S/D direction inside GT_P96 region DRC only flags the outermost M0 along M0C length direction.	=	0.028~0.105	um
<b>M0C.EX.2</b>	AOP_M0C (width = 0.048um) extension outside of AOP_M0 in S/D direction, except INST region	$\geq$	0.049	um
<b>M0C.EX.3</b>	AOP_M0C (width = 0.082/0.108um) extension outside of AOP_M0 (width = 0.054um) in S/D direction	$\geq$	0.067	um
<b>M0C.EX.4</b>	AOP_M0C extension outside of AOP_M0 in GATE poly direction, except (M0C interact TRCMK), OCOVL region	$\geq$	0.024	um
<b>M0C.EX.5</b>	AOP_M0C extension outside of AOP_M0 (width = 0.054um) in GATE poly direction	$\geq$	0.041	um
<b>M0C.EX.6</b>	AOP_M0 extension outside of AOP_M0C in GATE poly direction, except OCOVL region	$\geq$	0.061	um
<b>M0C.EX.7</b>	M0 extension outside of AOP_M0C (width = 0.048um) in GATE poly direction, except INST region	$\geq$	0.113	um
<b>M0C.EX.8</b>	AOP_M0 extension outside of AOP_M0C (width $\geq$ 0.052um) in GATE poly direction, except INST and OCOVL regions	$\geq$	0.079	um
<b>M0C.A.1</b>	AOP_M0C area, except RSPMK1 and INST regions	$\geq$	0.0072	um <sup>2</sup>
<b>M0C.A.2</b>	AOP_M0C area when interact RSPMK1	$\geq$	0.004	um <sup>2</sup>

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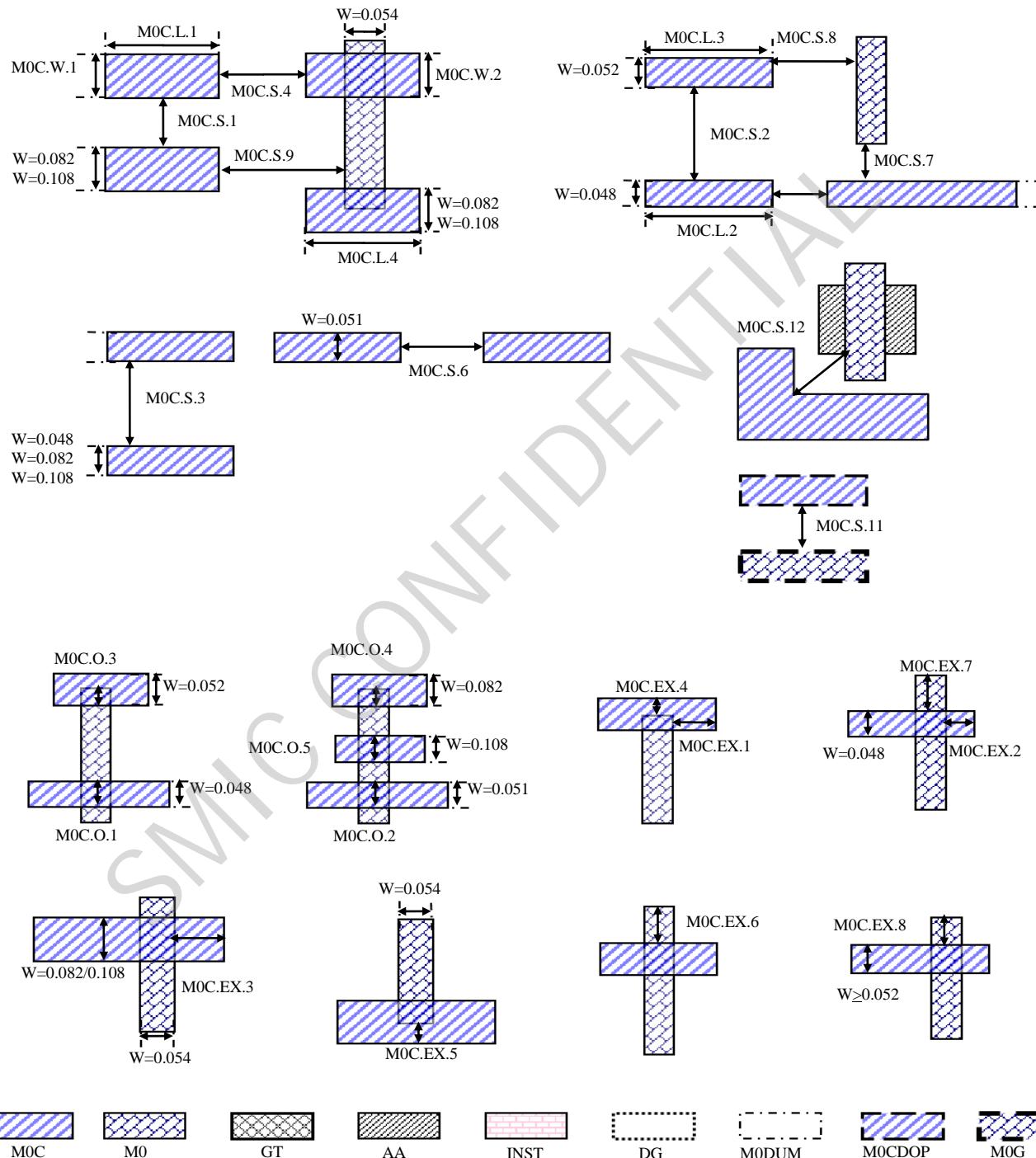
Rule number	Description	Opt.	Design Value	Unit
<b>M0C.D.1</b>	Full chip ALL_M0C density	$\geq$	5%	
<b>M0C.D.2</b>	ALL_M0C density (window 125 um*125um, stepping 62.5 um), except LOGO region	$\geq$	5%	
<b>M0C.D.3</b>	ALL_M0C density in window 125um*125 um, stepping 62.5um), except INST region	$\leq$	40%	
<b>M0C.R.1</b>	(ALL_M0 AND (All_AA (expanding horizontal edge by -0.01um))) overlap with ALL_M0C is not allowed, except INST region			
<b>M0C.R.2</b>	Any vertex of AOP_M0C inside ALL_M0 is not allowed, except OCOVL region			
<b>M0C.R.3</b>	ALL_M0C point touch is not allowed.			
<b>M0C.R.4</b>	ALL_M0C must be a rectangle orthogonal to grid or single L-, T-, U-, or combined L/T/U shape and at least two ALL_M0 INTERACT every segment of single L-, T-, U-, or combined L/T/U shape M0C. Single L-, T-, U-, or combined L/T/U shape M0C jog must = 0.056/0 um or 0.057/0.001um or 0.058/0.002 um for M0C width = 0.052/0.108um, except OCOVL region			
<b>M0C.R.5</b>	DUM_M0C must be a rectangle orthogonal to grid.			
<b>M0C.R.6</b>	AOP_M0 (width = 0.04/0.042um, length $\leq$ 0.17um) line-end must interact AOP_M0C, except INST region			
<b>M0C.R.7</b>	M0C (width = 0.051um) must interact RSPMK1.			
<b>M0C.R.8</b>	M0C must interact M0, floating M0C is not allowed, except OCOVL region			

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### 7.2.29 M0G design rules

Rule number	Description	Opt.	Design Value	Unit
<b>M0G.W.1</b>	M0G width, except OCOVL region	=	0.04, 0.05~0.055, 0.06, 0.088	um
<b>M0G.L.1</b>	AOP_M0G (width = 0.04um) length, except INST region	=	0.102~0.33	um
<b>M0G.L.2</b>	M0G (width = 0.05um) length in S/D direction, except GT_P96 region	=	0.05, 0.057~0.058	um
<b>M0G.L.2a</b>	M0G (width = 0.05um) length in S/D direction, inside GT_P96 region	=	0.05, 0.06~0.061	um
<b>M0G.L.2b</b>	AOP_M0G (width = 0.05um) length, except 0.05*(0.057~0.058)um and 0.05*(0.06~0.061)um M0G.	=	0.05	um
<b>M0G.L.3</b>	AOP_M0G (width = 0.06um) length, except length = 0.148~200um M0G inside RESP1	=	0.095~0.096, 0.198~200	um
<b>M0G.L.4</b>	M0G (width = 0.088um) length in S/D direction, except GT_P96 region	=	0.102~0.104	um
<b>M0G.L.5</b>	M0G (width = 0.088um) length in S/D direction, inside GT_P96 region	=	0.108~0.11	um
<b>M0G.L.6</b>	AOP_M0G (width = 0.051~0.055um) length in GATE poly direction	=	0.09~0.091	um
<b>M0G.S.1</b>	Space between AOP_M0G (except width = 0.05um) to AOP_M0G	≥	0.058	um
<b>M0G.S.1a</b>	Space between AOP_M0Gs (width = 0.04um)	≥	0.058	um
<b>M0G.S.1b</b>	Space between AOP_M0G (width = 0.04um) and AOP_M0G (width = 0.04um) when PRL ≥ -0.019um, except INST region.	≥	0.065	um
<b>M0G.S.1c</b>	Space between the short side of AOP_M0G (width = 0.04um) when PRL ≥ -0.019um	≥	0.076	um
<b>M0G.S.1d</b>	Space between the short side of M0G (width = 0.04um, and length = 0.121~0.161um or 0.223~0.249um, and PRL ≥ -0.02um) Except:	≥	0.082	um

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Rule number	Description	Opt.	Design Value	Unit
	Space between the short side of M0G (width = 0.04um, and length = 0.121~0.161um or 0.223~0.249um, and PRL $\geq$ -0.02um) to (M0 NOT M0C ) $\geq$ 0.03um			
<b>M0G.S.1e</b>	Space between AOP_M0G (width = 0.04um and length $\geq$ 0.12um) long side and AOP_M0G (width = 0.04um) when PRL $\geq$ -0.019um	$\geq$	0.084	um
<b>M0G.S.1f</b>	Space between AOP_M0G (width = 0.04um) and AOP_M0G (width = 0.05um), except M0G.S.1g	$\geq$	0.064	um
<b>M0G.S.1g</b>	Space between M0G (width = 0.04um) to M0G (width = 0.05um) when PRL < 0um	$\geq$	0.058	um
<b>M0G.S.1h</b>	Space between the short side of M0G (width = 0.04um) and AOP_M0G (width = 0.05um) when PRL $\geq$ -0.016um	$\geq$	0.068	um
<b>M0G.S.2</b>	Space between M0G (width = 0.05, length = 0.057~0.058um and AOP_M0G when PRL $\geq$ -0.074um	$\geq$	0.073	um
<b>M0G.S.3a</b>	Space between the center of AOP_M0G (width = 0.05um) and center of AOP_M0G (width = 0.05um) (Except M0G group in M0G.S.3c)	$\geq$	0.105	um
<b>M0G.S.3b</b>	Space between the center of M0G (width = 0.05um) and any one center of 3-neighboring M0G (width = 0.05um, center to center space $\leq$ 0.119um)	$\geq$	0.119	um
<b>M0G.S.3c</b>	Space between M0G group and AOP_M0G Definition of M0G group : 1) M0G width = 0.05um, and 2) M0G with PRL = 0.05um in vertical direction 3) 0.098um $\leq$ Center to center space $\leq$ 0.104um 4) The maximum M0G number in one group is 5	$\geq$	0.079	um
<b>M0G.S.3d</b>	Space between M0G group and AOP_M0G (width = 0.04um) in horizontal direction when PRL $\geq$ -0.079um Definition of M0G group follows M0G.S.3c.	$\geq$	0.114	um
<b>M0G.S.3e</b>	Space between M0G group and AOP_M0G (width = 0.04/0.05um) in vertical direction when PRL $\geq$ -0.079um Definition of M0G group follows M0G.S.3c	$\geq$	0.103	um
<b>M0G.S.4a</b>	Space between M0G (width = 0.06um) and M0G (Except M0G.S.4b, and the space between M0G (width = 0.06um) long side and M0G when -0.08 $\leq$ PRL < 0um), except	$\geq$	0.129	um

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Rule number	Description	Opt.	Design Value	Unit
	OCOVL region			
<b>M0G.S.4b</b>	Space between M0G (width = 0.06um) short side and M0G when PRL in width direction $\geq -0.08\text{um}$	$\geq$	0.101	um
<b>M0G.S.4c</b>	Space between DOP_M0G (width = 0.06um) to AOP_M0G	$\geq$	0.129	um
<b>M0G.S.4d</b>	Space between short side of M0G (width = 0.06um) and AOP_M0G (width = 0.05um) when PRL $\geq -0.075\text{um}$	$\geq$	0.106	um
<b>M0G.S.4e</b>	Space between AOP_M0G (width/length = 0.06/0.095~0.096um) and ALL_M0G	$\geq$	0.142	um
<b>M0G.S.5a</b>	Space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) and AOP_M0G (width = 0.05um) in vertical direction when PRL $\geq -0.015\text{um}$	$\geq$	0.069	um
<b>M0G.S.5b</b>	Space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) and AOP_M0G (width = 0.04um, PRL $\geq -0.015$ ) in vertical direction	$\geq$	0.065	um
<b>M0G.S.5c</b>	Space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) and AOP_M0G (width = 0.05/0.088um) in horizontal direction when PRL > 0um	$\geq$	0.077	um
<b>M0G.S.5d</b>	Space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) and AOP_M0G (width = 0.04um, PRL $\geq -0.015$ ) in horizontal direction	$\geq$	0.077	um
<b>M0G.S.5e</b>	Space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) in vertical direction when PRL > 0um	$\geq$	0.083	um
<b>M0G.S.5f</b>	Corner space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) and AOP_M0G (width = 0.04um, PRL $\leq -0.016\text{um}$ )	$\geq$	0.069	um
<b>M0G.S.5g</b>	Corner space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) when PRL $\leq 0\text{um}$	$\geq$	0.091	um
<b>M0G.S.6a</b>	Space between DOP_M0G and (AOP_M0G INSIDE DG)	$\geq$	0.046	um
<b>M0G.S.7a</b>	Space between AOP_M0G and AOP_AA (AA vertical)	$\geq$	0.029	um

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Rule number	Description	Opt.	Design Value	Unit
	edge extend 1/2 GT) (Overlap is not allowed, except (AOP_M0G AND AOP_AA) INTERACT M0), except (the space $\geq$ 0.013 in GATE poly direction) and INST region. DRC waive the space or overlap between DUM_M0G and DUM_AA.			
<b>M0G.S.7b</b>	Space between AOP_M0G and AOP_AA in GATE poly direction (Overlap is not allowed, except (AOP_M0G AND AOP_AA) INTERACT M0), except INST region. DRC waive the space or overlap between DUM_M0G and DUM_AA.	$\geq$	0.013	um
<b>M0G.S.8a</b>	Space between M0G (width = 0.06um) and AOP_AA (AA vertical edge extend 1/2 GT), except (the space $\geq$ 0.031 in GATE poly direction)	$\geq$	0.049	um
<b>M0G.S.8b</b>	Space between M0G (width = 0.06um) and AOP_AA in GATE poly direction	$\geq$	0.031	um
<b>M0G.S.9</b>	Space between M0G (width = 0.06um) and concave edge of L-shape AA edge (AA vertical edge extend 1/2GT) in S/D direction	$\geq$	0.069	um
<b>M0G.S.10a</b>	Space between AOP_M0G and AOP_GT, except AOP_GT jog $\leq$ 0.004um and OCOVL region	$\geq$	0.028	um
<b>M0G.S.10b</b>	Space between AOP_M0G and AOP_GT (width $\geq$ 0.07um)	$\geq$	0.038	um
<b>M0G.S.10c</b>	Space between AOP_M0G and AOP_GT line end	$\geq$	0.034	um
<b>M0G.S.11</b>	Space between M0G and ALL_GT (width $\leq$ 0.024um, the side space to ALL_GT $\geq$ 0.08um), except GT_P96 and small AOP_GT jog $\leq$ 0.004um.	$\geq$	0.049	um
<b>M0G.S.11a</b>	Space between M0G and ALL_GT (width = 0.032um, the side space to ALL_GT $\geq$ 0.08um), except GT_P96 and small AOP_GT jog $\leq$ 0.004um.	$\geq$	0.051	um
<b>M0G.S.12</b>	Space between AOP_M0G and (AOP_GT NOT P2) (width $\leq$ 0.09um, one side space to ((GATE (INSIDE DG) SIZING 0.041um) AND GT) = 0.118/0.119um, the other side space to (AOP_GT NOT P2) $\geq$ 0.15um) (Except the regions of only one M0G space to DOP_GT < 0.055um, and DOP_GT space to DOP_M0G)	$\geq$	0.054	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M0G.S.13</b>	Space between AOP_M0G (width = 0.06um) and AOP_GT, except small AOP_GT jog $\leq 0.004\text{um}$ and OCOVL region	$\geq$	0.031	um
<b>M0G.S.14</b>	Space between AOP_M0G (width = 0.06um) and AOP_GT line end	$\geq$	0.039	um
<b>M0G.S.15a</b>	Space between M0G and (M0 NOT M0C), except (M0G (width = 0.051~0.053/0.088um) AND GT) space to M0 = 0.025um, and INST region	$\geq$	0.026	um
<b>M0G.S.15b</b>	Space between M0G and (M0 NOT M0C) in S/D direction when PRL > -0.016um, except (M0G (width = 0.051~0.053/0.088um) AND GT) space to M0 = 0.025um and INST region.	$\geq$	0.026	um
<b>M0G.S.15c</b>	Space between M0G and (M0 NOT M0C) in S/D direction when PRL > -0.016 um, except poly center-to-center space = 0.09um design and INST region.	$\geq$	0.028	um
<b>M0G.S.16a</b>	Space between M0G (width = 0.06um) and (M0 NOT M0C)	$\geq$	0.028	um
<b>M0G.S.17a</b>	Space between M0G and short side of AOP_M0, except INST region 1. M0 width = 0.04/0.042um 2. M0 short side NOT INTERACT AOP_M0C 3. Space between AOP_M0 short side > 0.32um 4. PRL > 0	$\geq$	0.035	um
<b>M0G.S.17b</b>	Space between M0G and short side of AOP_M0, except INST region 1. M0 width = 0.04/0.042um 2. M0 short side NOT INTERACT AOP_M0C 3. Space between AOP_M0 short side > 0.41um 4. PRL > 0	$\geq$	0.049	um
<b>M0G.S.17c</b>	Corner space between M0G and short side of AOP_M0, except INST region 1. M0 width = 0.04/0.042um 2. M0 short side NOT INTERACT AOP_M0C	$\geq$	0.031	um

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Rule number	Description	Opt.	Design Value	Unit
	3. Space between AOP_M0 short side > 0.32um 4. PRL $\leq$ 0			
<b>M0G.S.18</b>	Space between M0G and short side of (M0 NOT M0C) (M0C width = 0.051um, M0 short side interact M0C)) in GATE poly direction when PRL $\geq$ 0um	$\geq$	0.039	um
<b>M0G.S.19</b>	Space between long side of M0G (width = 0.04um) and short side of (M0 NOT M0C) (M0 width = 0.04/0.042um) when PRL $\geq$ 0um, except INST region	$\geq$	0.028	um
<b>M0G.S.20</b>	Space between long side of M0G (width = 0.04/0.06um) and short side of (M0 NOT M0C) (M0 width = 0.054um) when PRL $\geq$ 0um	$\geq$	0.034	um
<b>M0G.S.21a</b>	Space between long side of M0G (width = 0.04/0.06/0.088um) and short side of M0 (short side NOT INTERACT M0C) when PRL $\geq$ -0.018um	$\geq$	0.031	um
<b>M0G.S.21b</b>	Space between long side of M0G (width = 0.04/0.06/0.088um) and short side of M0 (width = 0.054um, short side NOT INTERACT M0C) when PRL $\geq$ -0.018um	$\geq$	0.047	um
<b>M0G.S.22</b>	Space between long side of M0G (width = 0.06um) and long side of (M0 NOT M0C) when PRL > 0um and M0G and M0 are both in vertical direction	$\geq$	0.049	um
<b>M0G.S.23</b>	Space between short side of M0G (width = 0.06um) and short side of (M0 NOT M0C) when PRL $\geq$ 0um	$\geq$	0.049	um
<b>M0G.S.24</b>	Space between short side of M0G (width = 0.04/0.06um) and long side of (M0 NOT M0C) (M0 width = 0.054um) when PRL $\geq$ 0um	$\geq$	0.032	um
<b>M0G.S.25a</b>	Space between M0G (width = 0.05um) and the short side of M0 (short side NOT INTERACT M0C) when PRL > -0.018um	$\geq$	0.029	um
<b>M0G.S.25b</b>	Space between M0G (width = 0.05um) and the short side of (M0 NOT M0C) (M0 width = 0.04/0.042um) when PRL $\geq$ 0.02um, except INST region	$\geq$	0.049	um
<b>M0G.S.25c</b>	Space between M0G (width = 0.05um) and (M0 NOT M0C) (M0 width = 0.054um) when PRL $\geq$ 0um	$\geq$	0.049	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M0G.S.26</b>	Space between M0G (width/length = 0.051~0.053/0.09~0.091um, 0.054~0.055/0.09~0.091um) and long side of M0 in S/D direction when PRL > -0.025um DRC flags M0 line-end (NOT INTERACT M0C) inside the space region	$\geq$	0.032	um
<b>M0G.S.27</b>	Space between M0G (width = 0.051~0.053/0.054~0.055/0.088um) and (M0 NOT M0C) (M0 width = 0.04/0.042um) in GATE poly direction	$\geq$	0.029	um
<b>M0G.S.28</b>	Space between M0G (width = 0.06um) and (M0 NOT M0C) in S/D direction when PRL > -0.016um	$\geq$	0.029	um
<b>M0G.S.29</b>	Corner space between M0G and (M0 NOT M0C) when PRL < -0.014um, except INST region	$\geq$	0.028	um
<b>M0G.S.30</b>	Space between M0G and P2 in GATE poly direction when INTERACT the same GT (P2 (width = 0.048um, 0.068um) overlap (GT AND M0G) is not allowed), except M0G width/length = 0.06/0.095~0.096um, INST region.	$\geq$	0.016	um
<b>M0G.S.31a</b>	Space between the long side of M0G (width = 0.04/0.06um) and the short side of (M0 NOT M0C) when PRL $\geq$ 0um 1) M0C width = 0.048/0.052um, space to neighboring M0C (width = 0.048/0.052um) = 0.044um, PRL = 0um 2) M0 and M0G interact same M0C	$\geq$	0.033	um
<b>M0G.S.31b</b>	Space between the the short side of M0G (width = 0.051~0.053/0.054~0.055um) and the short side of M0 (short side not interact M0C) when PRL $\geq$ -0.018um	$\geq$	0.031	um
<b>M0G.S.31c</b>	Space between the short side of M0G (width = 0.051~0.053/0.054~0.055um) and the short side of M0 ( width = 0.054um, short side not interact M0C) when PRL $\geq$ -0.018um	$\geq$	0.047	um
<b>M0G.S.32a</b>	Space between AOP_M0G and AOP_AA (maximum delta V > 1.32V, 1.2V+10%) in GATE poly direction	$\geq$	0.028	um
<b>M0G.S.32b</b>	Space between AOP_M0G and AOP_AA (maximum delta V > 1.65V, 1.5V+10%) in GATE poly direction	$\geq$	0.03	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M0G.S.32c</b>	Space between AOP_M0G and AOP_AA (maximum delta V > 1.98V, 1.8V+10%) in GATE poly direction	$\geq$	0.033	um
<b>M0G.S.32d</b>	Space between AOP_M0G and AOP_AA (maximum delta V > 2.75V, 2.5V+10%) in GATE poly direction	$\geq$	0.043	um
<b>M0G.S.32e</b>	Space between AOP_M0G and AOP_AA (maximum delta V > 3.63V, 3.3V+10%) in GATE poly direction	$\geq$	0.055	um
<b>M0G.S.33a</b>	Space between AOP_M0G and ((AOP_GT NOT P2) INTERACT (AA OR M0G)) (maximum delta V > 0.935V)	$\geq$	0.031	um
<b>M0G.S.33b</b>	Space between AOP_M0G and (AOP_GT NOT P2) (maximum delta V > 1.32V, 1.2V+10%)	$\geq$	0.035	um
<b>M0G.S.33c</b>	Space between AOP_M0G and (AOP_GT NOT P2) (maximum delta V > 1.65V, 1.5V+10%)	$\geq$	0.037	um
<b>M0G.S.33d</b>	Space between AOP_M0G and (AOP_GT NOT P2) (maximum delta V > 1.98V, 1.8V+10%)	$\geq$	0.04	um
<b>M0G.S.33e</b>	Space between AOP_M0G and (AOP_GT NOT P2) (maximum delta V > 2.75V, 2.5V+10%)	$\geq$	0.05	um
<b>M0G.S.33f</b>	Space between AOP_M0G and (AOP_GT NOT P2) (maximum delta V > 3.63V, 3.3V+10%)	$\geq$	0.063	um
<b>M0G.S.34a</b>	Space between AOP_M0G and (AOP_M0 NOT AOP_M0C) (maximum delta V > 1.05V, 0.95V+10%)	$\geq$	0.03	um
<b>M0G.S.34b</b>	Space between AOP_M0G and (AOP_M0 NOT AOP_M0C) (maximum delta V > 1.32V, 1.2V+10%)	$\geq$	0.035	um
<b>M0G.S.34c</b>	Space between AOP_M0G and (AOP_M0 NOT AOP_M0C) (maximum delta V > 1.65V, 1.5V+10%)	$\geq$	0.037	um
<b>M0G.S.34d</b>	Space between AOP_M0G and (AOP_M0 NOT AOP_M0C) (maximum delta V > 1.98V, 1.8V+10%)	$\geq$	0.042	um
<b>M0G.S.34e</b>	Space between AOP_M0G and (AOP_M0 NOT AOP_M0C) (maximum delta V > 2.75V, 2.5V+10%)	$\geq$	0.05	um
<b>M0G.S.34f</b>	Space between AOP_M0G and (AOP_M0 NOT AOP_M0C) (maximum delta V > 3.63V, 3.3V+10%)	$\geq$	0.069	um
<b>M0G.S.35</b>	Space between M0G and AOP_M0G (maximum delta V >	$\geq$	0.067	um

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	3.63V, 3.3V+10%)			
<b>M0G.EX.1</b>	AOP_GT short side (width $\leq$ 0.032um, and short side not interact P2) extension outside of AOP_M0G (extension $\leq$ 0um is not allowed), except AOP_GT jog $\leq$ 0.004um	$\geq$	0.056	um
<b>M0G.EX.2</b>	AOP_GT short side (width $\geq$ 0.07um, and short side not interact P2) extension outside of AOP_M0G long side (width = 0.04/0.06um) (extension $\leq$ 0um is not allowed)	$\geq$	0.023	um
<b>M0G.EX.3</b>	M0G short side (width = 0.06um) extension outside of AOP_GT (extension $\leq$ 0um is not allowed), except OCOVL region	$\geq$	0.008	um
<b>M0G.EX.4</b>	M0 short side (width = 0.04/0.042um, and short side not interact M0C) extension outside of M0G (extension $\leq$ 0um is not allowed), except INST region	$\geq$	0.01	um
<b>M0G.EX.4a</b>	(M0 NOT M0C) short side (width = 0.04/0.042um) extension outside of M0G (extension $\leq$ 0um is not allowed), except INST region.	$\geq$	0.008	um
<b>M0G.EX.5</b>	(M0 NOT M0C) short side (width = 0.054um) extension outside of M0G (extension $\leq$ 0um is not allowed)	$\geq$	0.01	um
<b>M0G.EX.6</b>	M0G (width = 0.051~0.053/0.054~0.055/0.088um) extension outside of AA (horizontal edge extend -0.019um) in GATE poly direction, except INST region	$\geq$	0.007	um
<b>M0G.EX.7</b>	M0C (width/length = 0.108/0.09um) extension outside of M0G (width = 0.040/0.05) in GATE poly direction	=	0.034/0.029	um
<b>M0G.O.1</b>	M0G and (M0 NOT M0C) (width = 0.04/0.042um) overlap in S/D direction, except INST region	$\geq$	0.026	um
<b>M0G.O.1a</b>	M0G and ((M0 NOT M0C) AND AA) (M0 width = 0.04/0.042um) overlap in S/D direction (M0G cross M0 is not allowed), except (pick-up NOT VARMOS) and INST region.	=	0.026, 0.027	um
<b>M0G.O.2</b>	M0G and (M0 NOT M0C) (width = 0.054um) overlap in S/D direction, except M0G.O.2a	$\geq$	0.046	um
<b>M0G.O.2a</b>	M0G and ((M0 NOT M0C) AND AA) (M0 width = 0.054um) overlap in S/D direction (M0G cross M0 is not allowed), except (pick-up NOT VARMOS), and INST	=	0.04, 0.041	um

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Rule number	Description	Opt.	Design Value	Unit
	region.			
<b>M0G.O.3</b>	M0G and (M0 NOT M0C) overlap in length direction, M0G and M0 are both in vertical direction	$\geq$	0.059	um
<b>M0G.O.4a</b>	M0G (width = 0.04/0.05um) and (GT NOT P2) (GT width = 0.016um) overlap in S/D direction	$\geq$	0.014	um
<b>M0G.O.4b</b>	M0G (width = 0.04/0.05um) and (GT NOT P2) (GT width = 0.018um) overlap in S/D direction	$\geq$	0.015	um
<b>M0G.O.4c</b>	M0G (width = 0.04/0.05um) and (GT NOT P2) (GT width = 0.02um) overlap in S/D direction, except INST region	$\geq$	0.016	um
<b>M0G.O.4d</b>	M0G (width = 0.04/0.05um) overlap with (GT (width = 0.022um, INSIDE GT_P96) in S/D direction	$\geq$	0.017	um
<b>M0G.O.4e</b>	M0G (width = 0.04/0.05um) overlap with (GT (width = 0.024um, INSIDE GT_P96) in S/D direction	$\geq$	0.018	um
<b>M0G.O.4f</b>	M0G (width = 0.04/0.05um) and (GT NOT P2) (GT width = 0.032um) overlap in S/D direction	$\geq$	0.018	um
<b>M0G.O.4g</b>	M0G (width = 0.04um) and (GT NOT P2) (GT width $\geq$ 0.07um) overlap in S/D direction	$\geq$	0.07	um
<b>M0G.O.4h</b>	M0G (width = 0.05um) and (GT NOT P2) (GT width $\geq$ 0.07um) overlap in S/D direction	$\geq$	0.02	um
<b>M0G.O.5a</b>	M0G (width = 0.051~0.053/0.054~0.055/0.088um) and (GT NOT P2) (GT width = 0.016um) overlap in S/D direction	$\geq$	0.008	um
<b>M0G.O.5b</b>	M0G (width = 0.051~0.053/0.054~0.055/0.088um) and (GT NOT P2) (GT width = 0.018um) overlap in S/D direction	$\geq$	0.009	um
<b>M0G.O.5c</b>	M0G (width = 0.051~0.053/0.054~0.055/0.088um) and (GT NOT P2) (GT width = 0.02um) overlap in S/D direction	$\geq$	0.01	um
<b>M0G.O.5d</b>	M0G (width = 0.051~0.053/0.054~0.055/0.088um) and (GT NOT P2) (GT width = 0.022um) overlap in S/D direction	$\geq$	0.011	um
<b>M0G.O.5e</b>	M0G (width = 0.051~0.053/0.054~0.055/0.088um) and (GT NOT P2) (GT width = 0.024um) overlap in S/D	$\geq$	0.012	um

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Rule number	Description	Opt.	Design Value	Unit
	direction			
<b>M0G.O.6</b>	M0G (width/length = 0.06/0.095~0.096um) and (GT NOT P2) overlap in GATE poly direction	$\geq$	0.024	um
<b>M0G.D.1</b>	ALL_M0G density (window 125um*125um, stepping 62.5um), except 1. NODMF su 1um region. 2. MARKS su 1um region 3. LOGO, RESP1 region	$\geq$	1%	
<b>M0G.D.2</b>	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density (window 125um*125um, stepping 62.5um), except RESP1 and LOGO region	$\geq$	6%	
<b>M0G.D.3</b>	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density in RESP1 region (window 125um*125um, stepping 62.5um)	$\geq$	5%	
<b>M0G.D.4</b>	ALL_M0G density (window 20um x20um, stepping 10um), except OCOVL region	$\leq$	20%	
<b>M0G.D.5</b>	((ALL_M0 NOT ALL_M0C) OR ALL_M0G) density (window 20um*20um, stepping 10um) , except OCOVL region	$\leq$	45%	
<b>M0G.R.1</b>	ALL_M0G (width = 0.04um) must be horizontal.			
<b>M0G.R.2a</b>	M0G (width/length = 0.05/0.057~0.058, 0.05/0.06~0.061, 0.088/0.102~0.104, 0.088/0.108~0.11um) must be horizontal direction.			
<b>M0G.R.2b</b>	M0G (width/length = 0.051~0.053/0.09~0.091, 0.054~0.055/0.09~0.091, 0.06/0.095~0.096um) must be vertical direction.			
<b>M0G.R.3</b>	M0G interact with AA is not allowed, except M0G (INTERACT (M0 AND AA)) and INST region			
<b>M0G.R.3a</b>	M0G (width = 0.06um) interact with AA is not allowed, except pickup and VARMOS region.			
<b>M0G.R.4</b>	ALL_M0G must be rectangular, and orthogonal to grid.			
<b>M0G.R.5</b>	M0G (width/length = 0.05/0.057~0.058, 0.05/0.06~0.061um) and M0G (width/length = 0.051~0.053/0.09~0.091, 0.054~0.055/0.09~0.091um and INTERACT AA) must INTERACT both GT (width $\leq$			

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Rule number	Description	Opt.	Design Value	Unit
	0.024um) and (M0 NOT M0C) (M0 width = 0.04/0.042um)			
<b>M0G.R.6</b>	The maximum number of M0G (width/length = 0.05/0.057~0.058, 0.05/0.06~0.061um) within M0G su 0.0615um, except INST region	$\leq$	2	
<b>M0G.R.6.1</b>	The number of M0G (width/length = 0.06/0.095~0.096um) within M0G su 0.21um	$\geq$	2	
<b>M0G.R.7</b>	M0G (width = 0.05um) INTERACT GT (width $\geq$ 0.07um) is not allowed.			
<b>M0G.R.8</b>	M0G (width/length = 0.088/0.102~0.104, 0.088/0.108~0.11 um) must overlap AA.			
<b>M0G.R.9</b>	(M0G (width/length = 0.088/0.102~0.104, 0.088/0.108~0.11um) NOT M0) interact V0 is not allowed.			
<b>M0G.R.10</b>	M0G (width/length = 0.088/0.102~0.104, 0.088/0.108~0.11um) must INTERACT two (M0 NOT M0C) (M0 width = 0.04/0.042um)			
<b>M0G.R.11</b>	M0G (width = 0.06um) extension outside of (M0 NOT M0C) must be equal at both side of M0, when M0G and M0 are both in vertical direction.			
<b>M0G.R.12</b>	M0G (width/length = 0.06/0.095~0.096um) extension on (GT NOT P2) must be equal at both side of GT, when M0G and GT are both in vertical direction			
<b>M0G.R.13</b>	M0G (width = 0.04/0.06um) must INTERACT at least one of the following options, except OCOVL region: 1) two (GT NOT P2) 2) two (M0 NOT M0C) 3) one (M0 NOT M0C) and one (GT NOT P2) 4) one V0 and one (M0 NOT M0C) 5) one V0 and one (GT NOT P2) 6) two V0 <b>7) one rectangle V0 and DIR (width <math>\leq</math> 0.145um)</b>			
<b>M0G.R.14</b>	M0G INTERACT GATE is not allowed, except in pick-up, MARKG, MARKS, DSTR, DMPNP, DIOMK1, DIOMK2, VARMOS and M0G (width = 0.04 /0.051~0.055/0.088um).			

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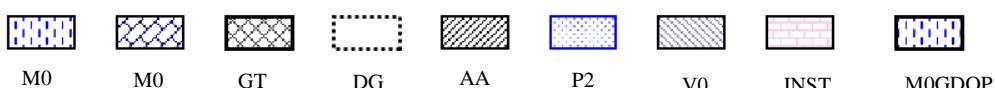
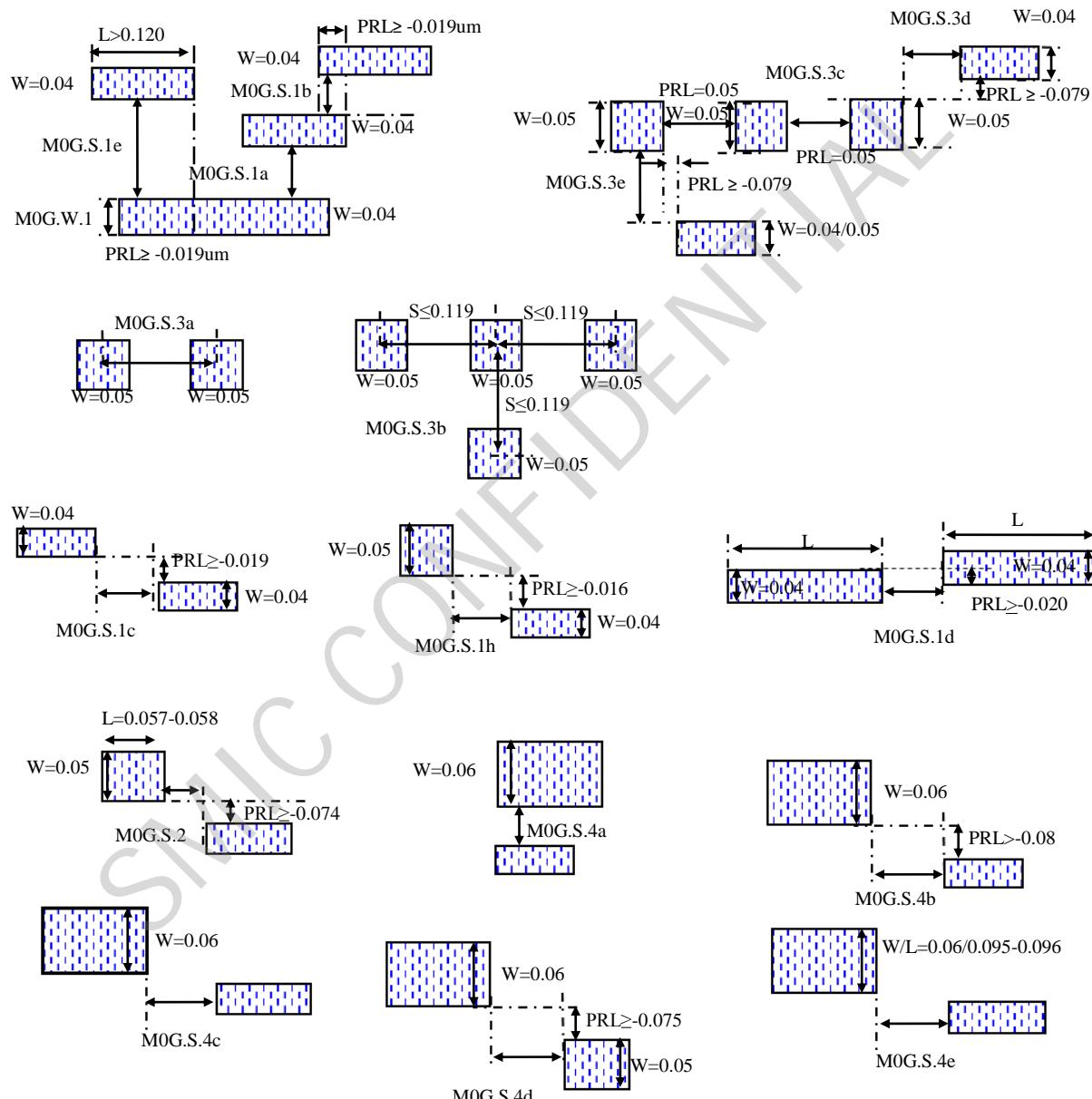
Rule number	Description	Opt.	Design Value	Unit
<b>M0G.R.15</b>	M0G interact with (DUM_GT NOT P2) is not allowed.			
<b>M0G.R.16</b>	It is not allowed maximum delta V $\geq$ 5.6V, when: 1. Space between AOP_M0G is < 0.7um 2. Space between AOP_M0G and AOP_AA is < 0.77um 3. Space between AOP_M0G and (AOP_GT NOT P2) is < 0.68um 4. Space between AOP_M0G and (AOP_M0 NOT AOP_M0C) is < 0.72um			
<b>M0G.R.17</b>	DOP_M0G overlap with M0G is not allowed			

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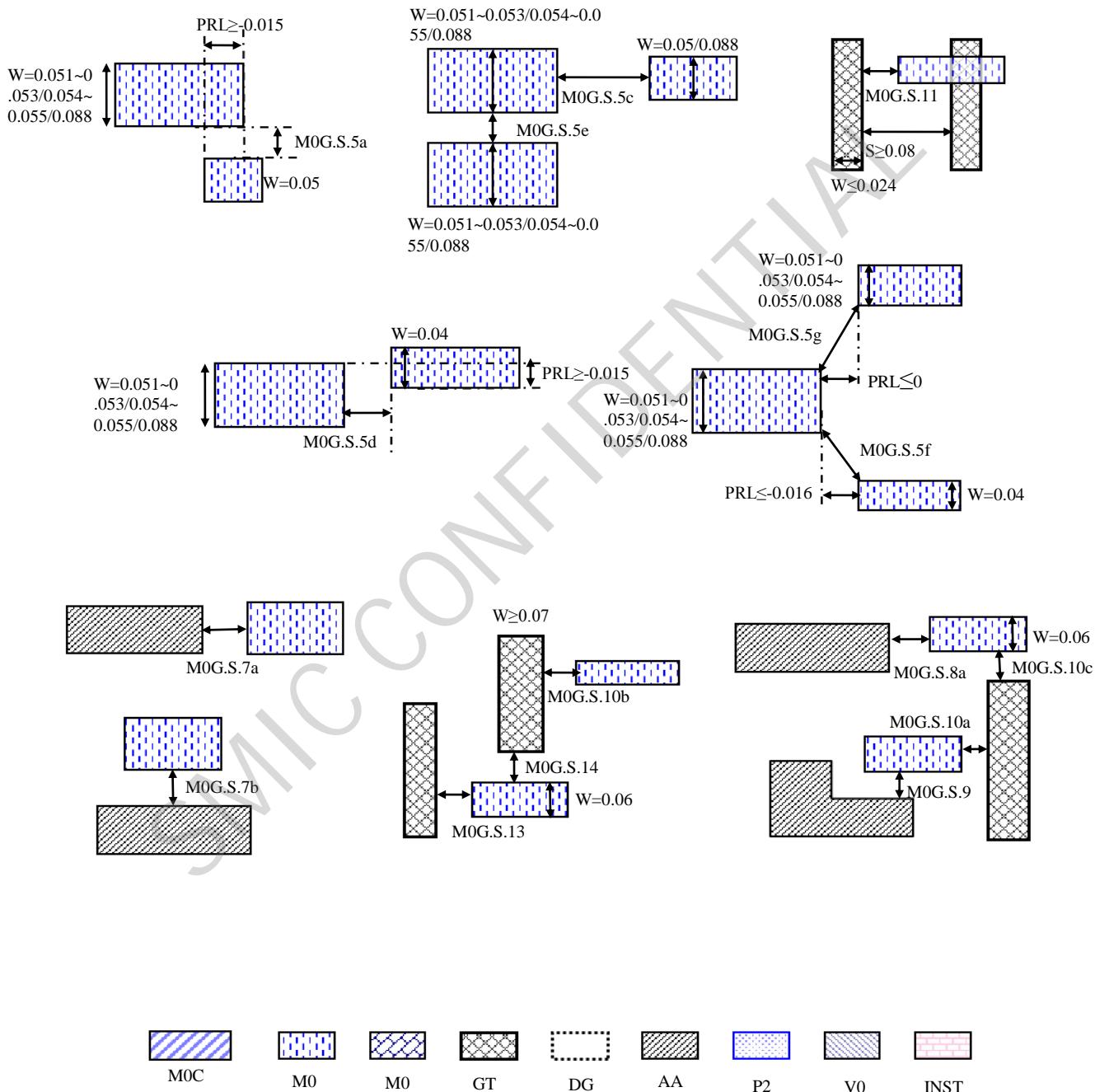
2017-11-02

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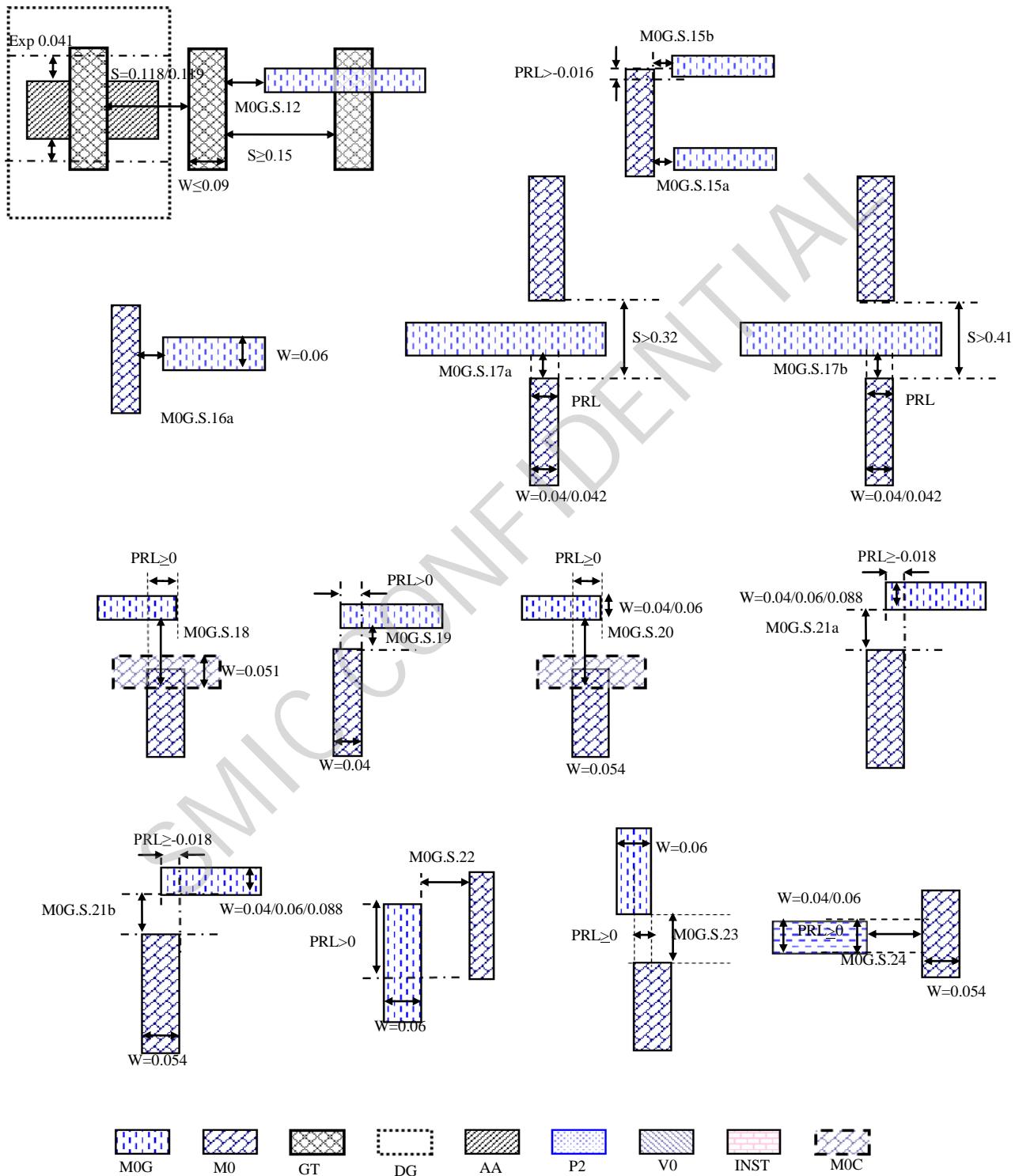
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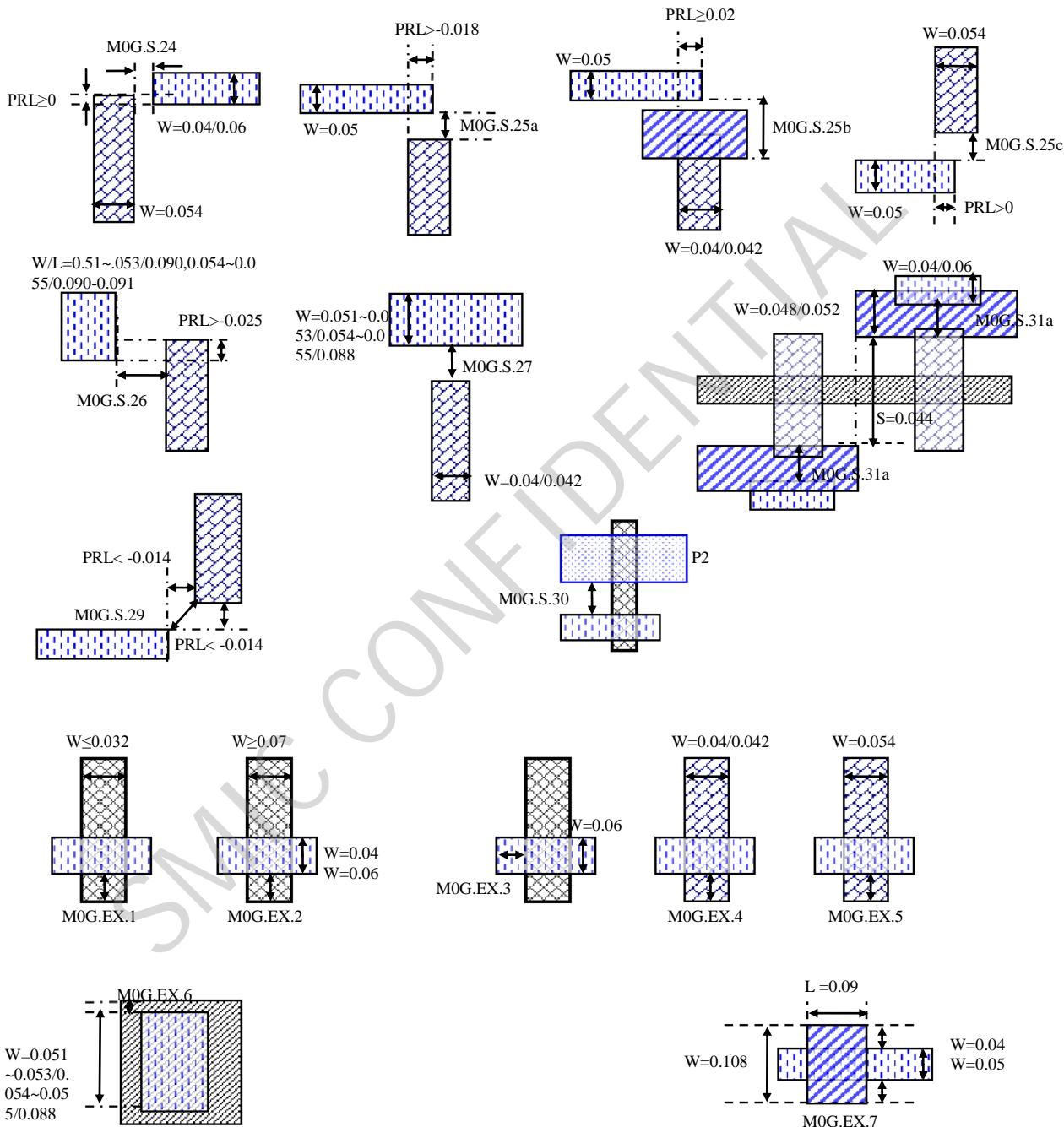


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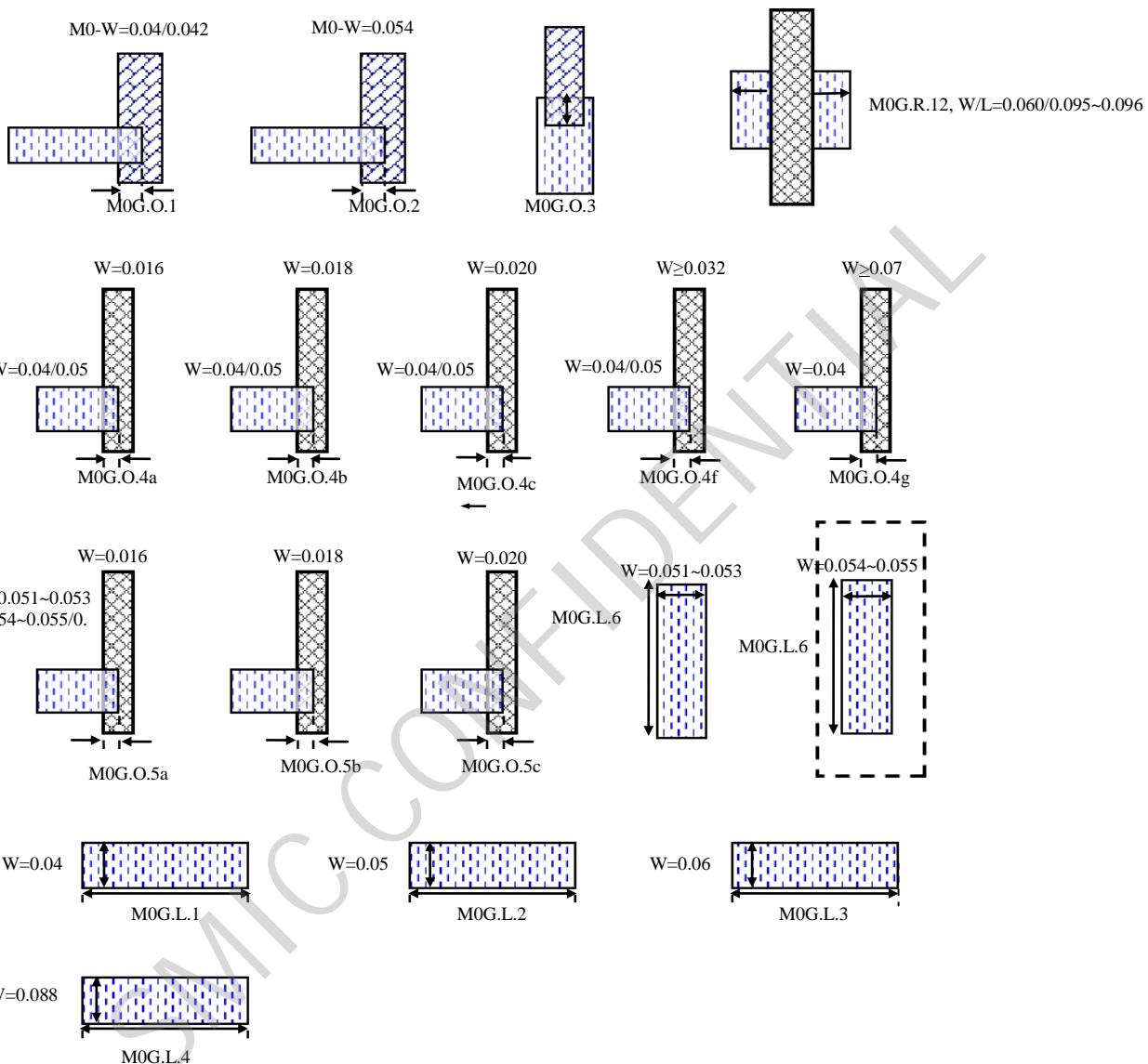
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### 7.2.30 M0GDMP dummy rules (data type 8)

Rule number	Description	Opt.	Design Value	Unit
M0GDMP.W.1	M0GDMP width	=	0.04/0.05/0.06	um
M0GDMP.S.1	Space between M0GDMP and (M0DMP NOT AOP_M0C) (Overlap with M0 is not allowed)	≥	0.049	um
M0GDMP.S.2	Space between M0GDMP and V0 (Overlap is not allowed)	≥	0.039	um
M0GDMP.S.3	Space between M0GDMP and M0G	≥	0.13	um
M0GDMP.S.4	Space between M0GDMP and AA	≥	0.07	um
M0GDMP.S.5	Space between M0GDMP and GT	≥	0.055	um
M0GDMP.S.6	Space between M0GDMP and M0	≥	0.05	um
M0GDMP.R.1	M0GDMP INTERACT M0G or P2 is not allowed.			
M0GDMP.R.2	M0GDMP INTERACT AA or GT is not allowed			

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### 7.2.31 V0 design rules

#### 7.2.31.1 Square V0 design rules

Rule number	Description	Opt.	Design Value	Unit
<b>V0.W.1</b>	V0 width and length, except 0.032*0.08 RV0, MARKS, MARKG, OCOVL and LOGO regions	=	0.032	um
<b>V0.W.2</b>	V0 bar width, and V0 bar is only allowed in MARKS, MARKG, INDMY and LOGO region. It allows 0.002um DRC checking tolerance in 45-degree region.	=	0.1	um
<b>V0.S.1</b>	Space between two V0s	$\geq$	0.04	um
<b>V0.S.2</b>	Space between two V0s when PRL $\geq$ -0.026um, except INST region, DRC only flag the point-to-point space when PRL $\leq$ 0.	$\geq$	0.051	um
<b>V0.S.3</b>	Space between V0 bar and V0 bar, square V0 or rectangular V0	$\geq$	0.59	um
<b>V0.S.4</b>	Space between V0 and M0G at different net	$\geq$	0.029	um
<b>V0.S.5</b>	Space between V0 and M0G at different net when PRL > -0.012um	$\geq$	0.032	um
<b>V0.S.7</b>	Space between V0 and (M0 NOT M0C) at different net in S/D direction when PRL > -0.016um	$\geq$	0.025	um
<b>V0.S.8</b>	Space between V0 and (M0 NOT M0C) at different net in S/D direction when PRL > -0.016um DRC only check space along M1 enclosure V0 > 0um in S/D direction.	$\geq$	0.027	um
<b>V0.S.9</b>	Space between V0 and (M0 NOT M0C) line-end at different net when PRL > 0.01um, except INST region	$\geq$	0.025	um
<b>V0.S.10</b>	(purposely blank)			
<b>V0.S.11</b>	Space between V0 (INTERACT M0 width = 0.04/0.042um) and M0C concave corner when V0 and M0C interact same M0	$\geq$	0.038	um
<b>V0.S.12</b>	Space between V0 (INTERACT M0 width = 0.054um) and M0C concave corner when V0 and M0C interact same M0	$\geq$	0.082	um
<b>V0.S.13</b>	Space between (V0 OR RV0) and (M0G OR (M0 NOT M0C)) (maximum delta V > 0.935V) (0.85V+10%)	$\geq$	0.035	um

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Rule number	Description	Opt.	Design Value	Unit
<b>V0.S.14</b>	Space between (V0 OR RV0) and (M0G OR (M0 NOT M0C)) (maximum delta V > 1.65V) (1.5V+10%)	≥	0.04	um
<b>V0.S.15</b>	Space between (V0 OR RV0) and (M0G OR (M0 NOT M0C)) (maximum delta V > 2.75V) (2.5V+10%)	≥	0.05	um
<b>V0.S.16</b>	Space between (V0 OR RV0) and (M0G OR (M0 NOT M0C)) (maximum delta V > 3.63V) (3.3V+10%)	≥	0.069	um
<b>V0.S.17</b>	Space between (V0 OR RV0) (maximum delta V > 1.05V) (0.95V+10%)	≥	0.051	um
<b>V0.S.18</b>	Space between (V0 OR RV0) (maximum delta V > 1.32V) (1.2V+10%)	≥	0.053	um
<b>V0.S.19</b>	Space between (V0 OR RV0) (maximum delta V > 1.65V) (1.5V+10%)	≥	0.059	um
<b>V0.S.20</b>	Space between (V0 OR RV0) (maximum delta V > 1.98V) (1.8V+10%)	≥	0.071	um
<b>V0.S.21</b>	Space between (V0 OR RV0) (maximum delta V > 2.75V) (2.5V+10%)	≥	0.077	um
<b>V0.S.22</b>	Space between (V0 OR RV0) (maximum delta V > 3.63V) (3.3V+10%)	≥	0.158	um
<b>V0.EN.1</b>	V0 must be fully covered by (M0 NOT M0C) or M0G, and must follow V0.EN.2, or V0.EN.2a, or V0.EN.3, or V0.EN.4, or (V0.EN.5a and V0.EN.5b), or V0.EN.6, or V0.EN.7 as below.  DRC waive the violation either V0/M0 or V0/M0G pass the enclosure rules when V0 INTERACT (M0 AND M0G).			
<b>V0.EN.2</b>	V0 enclosure by (M0 NOT M0C) (M0 width = 0.04um) for two opposite sides with other two sides = 0.004um, except INST region	≥	0.014	um
<b>V0.EN.2a</b>	V0 enclosure by (M0 NOT M0C) (M0 width = 0.042um) for two opposite sides with other two sides = 0.005um, except INST region	≥	0.014	um
<b>V0.EN.3</b>	V0 enclosure by (M0 NOT M0C) (M0 width = 0.054um) for two opposite sides with other two sides = 0.011um	≥	0.017	um

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Rule number	Description	Opt.	Design Value	Unit
<b>V0.EN.4</b>	V0 enclosure by M0G (width = 0.04um) for two opposite sides with other two sides = 0.004um, except INST region	$\geq$	0.011	um
<b>V0.EN.5a</b>	V0 enclosure by M0G (width = 0.05um) for two opposite sides with other two sides $\geq$ 0um	$\geq$	0.008	um
<b>V0.EN.5b</b>	V0 enclosure by M0G (width = 0.05um, length = 0.057~0.058/0.06~0.061um) for two opposite sides with other two sides $\geq$ 0.009um	$\geq$	0.011	um
<b>V0.EN.6</b>	V0 enclosure by M0G (width = 0.06um) for two opposite sides with other two sides $\geq$ 0.014um	$\geq$	0.029	um
<b>V0.EN.7</b>	V0 enclosure by M0G (width = 0.051~0.053/0.054~0.055um) for two opposite sides with the other two sides $\geq$ 0.009um	$\geq$	0.028	um
<b>V0.EN.8</b>	V0 must be fully covered by M1, and must follow V0.EN.9, or V0.EN.11, or V0.EN.12, or V0.EN.13, or V0.EN.14, or V0.EN.15, or V0.EN.16c, or (V0.EN.17a and V0.EN.17b), or V0.EN.18, or (V0.EN.19a and V0.EN.19b), or V0.EN.20, or (V0.EN.21a and V0.EN.21b), or V0.EN.22, or V0.EN.23 as below.			
<b>V0.EN.9</b>	V0 enclosure by M1 for all sides	$\geq$	0.015	um
<b>V0.EN.11</b>	Total V0 enclosure (E1+E2) by M1 (short side of M1 width = 0.032um, both two opposite sides (E1/E2) $\geq$ 0.035um) with the other two sides $\geq$ 0um, except INST region When meet either one of below conditions: 1. Space between V0 and metal in metal length direction $\leq$ 0.129um 2. Space between V0 and metal in metal width direction $\leq$ 0.089um	$\geq$	0.079	um
<b>V0.EN.12</b>	Total enclosure (E1+E2) by M1 (short side of M1 width = 0.032um, both two opposite sides (E1/E2) $\geq$ 0.03um) with the other two sides $\geq$ 0um for isolated V0 condition. Isolated V0 condition: Space between V0 and metal in metal length direction $>$ 0.129um and in metal width direction $>$ 0.089um.	$\geq$	0.069	um
<b>V0.EN.13</b>	V0 enclosure by M1 (short side of M1 width $>$ 0.032um and $\leq$ 0.046um) for opposite side $\geq$ 0.032um with the other two sides	$\geq$	0.047	um

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Rule number	Description	Opt.	Design Value	Unit
	$\geq 0.003\text{um}$			
<b>V0.EN.14</b>	V0 enclosure by M1 (short side of M1 width $> 0.032\text{um}$ and $\leq 0.046\text{um}$ ) for opposite side $\geq 0.036\text{um}$ with the other two sides $\geq 0\text{um}$	$\geq$	0.043	um
<b>V0.EN.15</b>	V0 enclosure by M1 (short side of M1 width $> 0.032\text{um}$ and $\leq 0.046\text{um}$ ) for two opposite sides with the other two sides $\geq 0\text{um}$	$\geq$	0.039	um
<b>V0.EN.16a</b>	V0 enclosure by M1 in adjacent S1 side, when 1. $0.032\text{um} < \text{short side of M1 width} \leq 0.046\text{um}$ 2. $0.058\text{um} \leq S1 < 0.063\text{um}$ , PRL $\geq 0.113\text{um}$	$\geq$	0.003	um
<b>V0.EN.16c</b>	V0 enclosure by M1 at least one side (short side of M1 width = $0.036\text{um}$ , space $< 0.058\text{um}$ or $\geq 0.063\text{um}$ ) for the opposite side $\geq 0.032\text{um}$ and the other two sides $\geq 0.002\text{um}$	$\geq$	0.047	um
<b>V0.EN.17a</b>	V0 enclosure by M1 (short side of M1 width $> 0.046\text{um}$ and $\leq 0.056\text{um}$ ) for two opposite sides with the other two sides $\geq 0.006\text{um}$ when V0 interact with M0G (width = $0.05\text{um}$ )	$\geq$	0.023	um
<b>V0.EN.17b</b>	V0 enclosure by M1 (short side of M1 width $> 0.046\text{um}$ and $\leq 0.056\text{um}$ ) for two opposite sides with the other two sides $\geq 0.009\text{um}$ , except V0 interact with M0G (width = $0.05\text{um}$ ) and INST region	$\geq$	0.024	um
<b>V0.EN.18</b>	V0 enclosure by M1 (short side of M1 width = $0.056\text{um}$ ) for two opposite sides with the other two sides = $0.012\text{um}$	$\geq$	0.023	um
<b>V0.EN.19a</b>	V0 enclosure by M1 (short side of M1 width $> 0.056\text{um}$ and $\leq 0.09\text{um}$ ) for two opposite sides with the other two sides $\geq 0.006\text{um}$ when V0 interact with M0G (width = $0.05\text{um}$ )	$\geq$	0.023	um
<b>V0.EN.19b</b>	V0 enclosure by M1 (short side of M1 width $> 0.056\text{um}$ and $\leq 0.09\text{um}$ ) for two opposite sides with the other two sides $\geq 0.009\text{um}$ , except V0 interact with M0G (width = $0.05\text{um}$ ), INST region	$\geq$	0.024	um
<b>V0.EN.20</b>	V0 enclosure by M1 (short side of M1 width = $0.084$ or $0.09\text{um}$ ) for two opposite sides, when 1. M1 space: $S < 0.058\text{um}$ or $> 0.062\text{um}$ and the adjacent side enclosure $0.005 \leq E \leq 0.008\text{um}$ , with PRL $> -0.015\text{um}$ . 2. At most one M1 polygon ( $0.058\text{um} \leq \text{M1 space} \leq 0.062\text{um}$ and the adjacent side enclosure $0.005 \leq E \leq 0.008\text{um}$ ,	$\geq$	0.059	um

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Rule number	Description	Opt.	Design Value	Unit
	-0.154um < PRL ≤ -0.015um)			
<b>V0.EN.21a</b>	V0 enclosure by M1 (short side of M1 width > 0.09um) for two opposite sides with the other two sides ≥ 0.015um when V0 interact with M0G (width = 0.05um)	≥	0.023	um
<b>V0.EN.21b</b>	V0 enclosure by M1 (short side of M1 width > 0.09um) for two opposite sides with the other two sides ≥ 0.014um, except V0 interact with M0G (width = 0.05um)	≥	0.024	um
<b>V0.EN.22</b>	V0 enclosure by M1 (short side of M1 width > 0.09um and ≤ 0.2um) for at least two adjacent edges with the other two sides ≥ 0.024um and ≥ 0.009um when V0 interact with M0G (width = 0.05um)	≥	0.059	um
<b>V0.EN.23</b>	V0 enclosure by M1 (short side of M1 width > 0.09um and ≤ 0.2um) for at least two adjacent edges with the other two sides ≥ 0.025um and ≥ 0.009um, except V0 interact with M0G (width = 0.05um)	≥	0.059	um
<b>V0.EN.24</b>	V0 enclosure by M1 for two opposite sides (projection space between V0 and M1 inner vertex = -0.007 ~ -0.026um, enclosure by M1 edge < 0.003um at opposite side of M1 inner vertex; the inner vertex with M1 width ≤ 0.046um and jog height > 0.014um)	≥	0.039	um
<b>V0.EN.25</b>	V0 enclosure by M1 for the long side edge (0.036um ≤ M1 width ≤ 0.041um, and the long side space ≥ 0.058um and < 0.063um, and the opposite long side space ≥ 0.068um, PRL > 0.136um)	≥	0.005	um
<b>V0.D.1<sup>[R]</sup></b>	(V0 OR RV0) density (window 5um*5um, stepping 2.5um)	<	7.7%	
<b>V0.R.1</b>	45-degree V0 and RV0 is not allowed, except V0 bar in MARKS/MARKG/INDMY/LOGO regions.			
<b>V0.R.2</b>	Single V0 is not allowed in "H-shape" M1, when: M1 has "H-shape" interacting with two metal holes: 1. Both two holes length ≤ 4.5um and area ≤ 4.05um <sup>2</sup> 2. The V0 overlaps the center metal bar of this "H-shape" M1. 3. The center metal bar length ≤ 0.9um and width ≤ 0.12um.			
<b>V0.R.3</b>	V0 and RV0 overlap with (DUM_AA OR DUM_GT) is not allowed.			

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Rule number	Description	Opt.	Design Value	Unit
<b>V0.R.4</b>	Maximum delta V $\geq 5.6V$ is not allowed, when space between V0 is $< 0.410\mu m$			
<b>V0.R.5</b>	It's not allowed (V0 OR RV0) overlap with the M1 resistor			
<b>V0.R.6<sup>[R]</sup></b>	Recommend space between a square V0 and another (V0 OR RV0 OR DUM_V0) $< 4\mu m$ to avoid single square V0			
<b>V0.OR<sup>[NC]</sup></b>	Odd ring conflict space definition: 1. Odd ring conflict space (ORCS): pitch space $< 0.108\mu m$ odd ring conflict line definition: 2. Odd ring conflict line (ORCL): The line between two VIAs with ORCS 3. ORCLs are independent to all other ones, even if they are overlapped or crossed 4. Including square V0 and rectangular V0 OR-AREA definition: 1. Odd ring line area (ORLA): The projection area between two edges with ORLS 2. Odd ring corner area (ORCA): The line between two corners with ORCS 3. ORLA or ORCA region are independent to all other ones, even if they are overlapped or crossed Loop: 1. A loop is formed when polygons of (V0 OR RV0) are connected in a cycle sequence with OR-AREA in between 2. A loop cannot contain any sub-loops which share one or more polygons with it Path: A path is formed when polygons of (V0 OR RV0) are connected one by one from one marker to another marker with OR-AREA in between			
<b>V0.OR.1</b>	ORCL cannot cross other ORCL or touch other ORCLs.			
<b>V0.OR.2</b>	ORCL count of the closed loop formed by original polygons and ORCLs cannot be odd number.			
<b>V0.OR.3</b>	V0DPMK must be drawn identically to V0 or RV0.			
<b>V0.OR.4</b>	(V0 INTERACT V0DPMK) cannot have ORCS with V0 (including square V0 and rectangular V0).			
<b>V0.OR.5</b>	(V0 INTERACT INST) INTERACT V0DPMK is not allowed (including square V0 and rectangular V0).			

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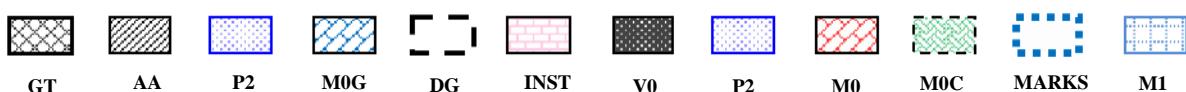
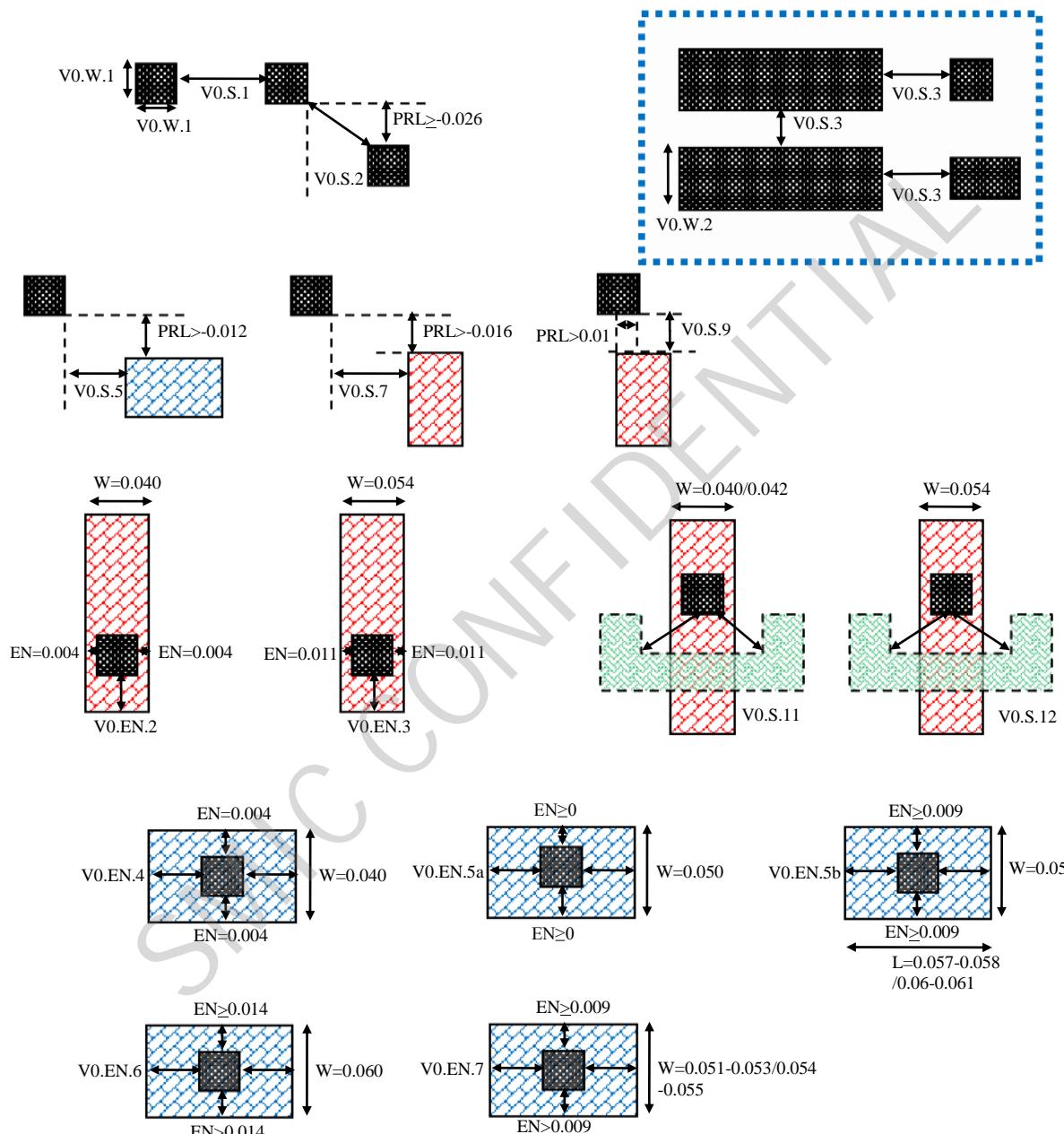


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Rule number	Description	Opt.	Design Value	Unit
<b>V0.OR.6</b>	Pre-coloring marker V0CA and V0CB must be drawn identically to (V0 OR RV0).			
<b>V0.OR.7</b>	V0CA INTERACT V0CB is not allowed.			
<b>V0.OR.8</b>	(V0 INTERACT INST) INTERACT (V0CA OR V0CB) is not allowed.			
<b>V0.OR.9</b>	(V0CA OR V0CB) INTERACT V0DPMK is not allowed.			
<b>V0.OR.10</b>	ORCA cross another ORCA or touch ORLA is not allowed.			
<b>V0.OR.11</b>	OR-AREA count of the close loop formed by original polygons and OR-AREA cannot be odd number.			
<b>V0.OR.12</b>	OR-AREA count of any path starting from V0CA and ending at V0CA must not be a odd number.			
<b>V0.OR.13</b>	OR-AREA count of any path starting from V0CB and ending at V0CB must not be a odd number.			
<b>V0.OR.14</b>	OR-AREA count of any path starting from V0CA and ending at V0CB must not be a even number.			
<b>V0.OR.15</b>	Maximum pre-coloring ratio of ((V0CA + V0CB + V0DPMK)/(V0 OR RV0)) before decomposition	<	16%	
<b>V0.ORCS.1</b>	(V0 OR RV0) Pitch space	≥	0.108	um

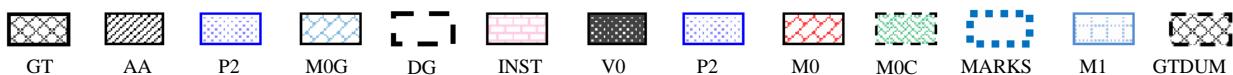
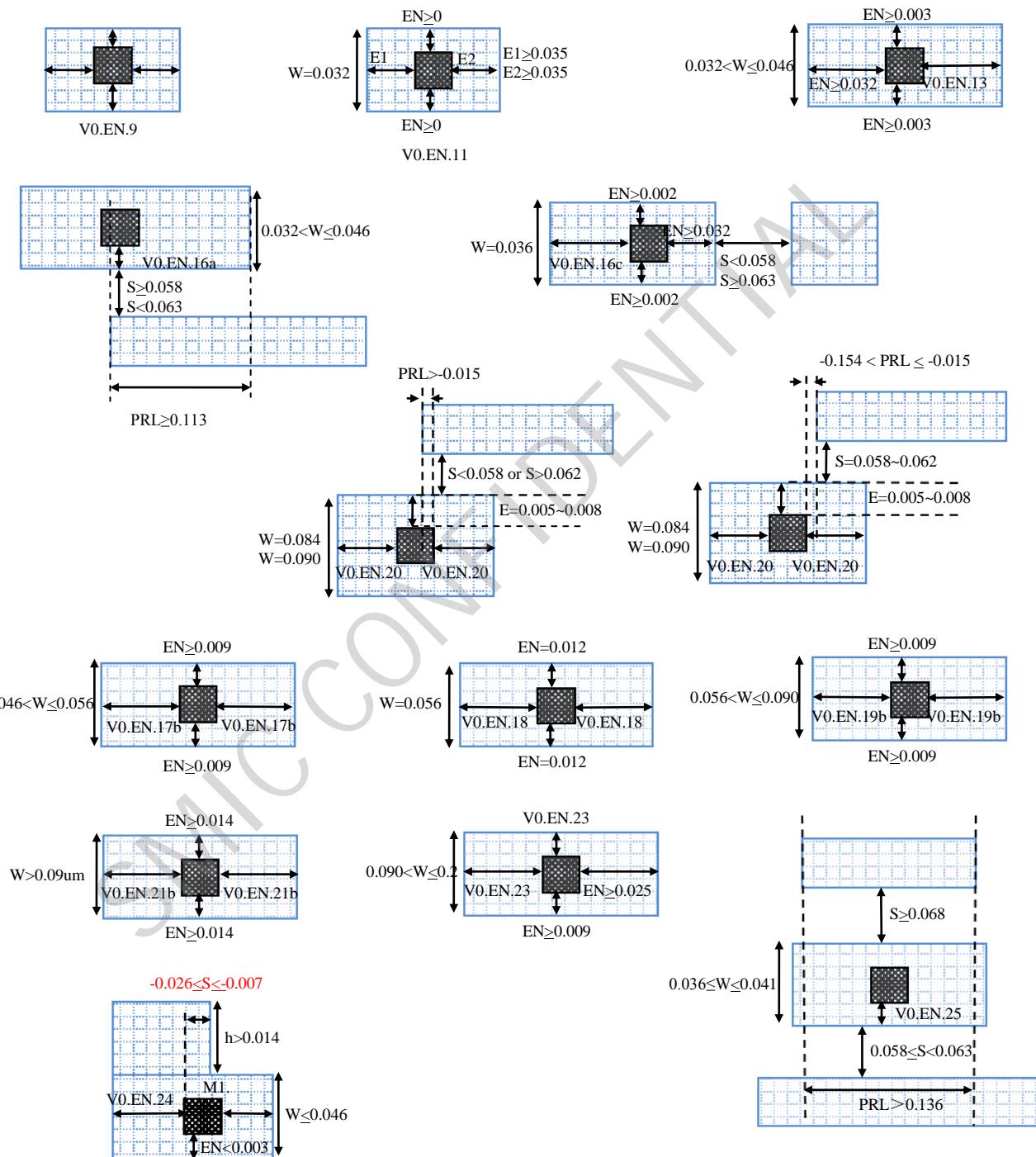
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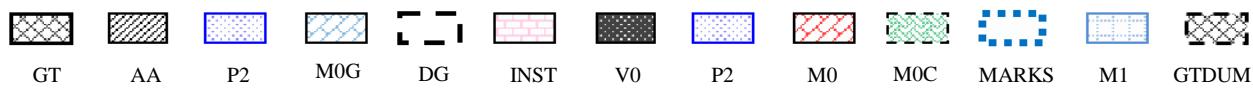
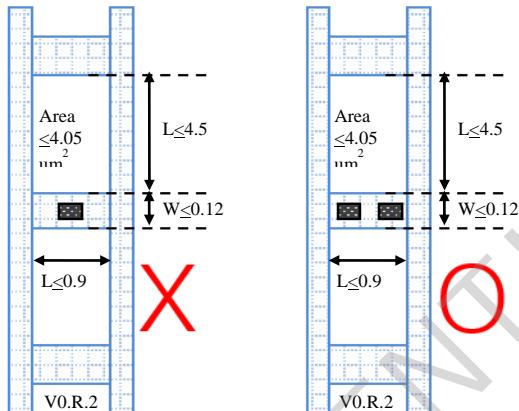
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V0.R.1



V0.R.1



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### 7.2.31.2 Rectangular V0 design rules

Rule number	Description	Opt.	Design Value	Unit
<b>RV0.W.1</b>	Rectangular V0 width, except OCOVL, MARKS and MARKG region	=	0.032	um
<b>RV0.L.1</b>	Rectangular V0 length, except OCOVL, MARKS and MARKG region	=	0.08	um
<b>RV0.L.2</b>	V0 bar length (width = 0.1um)	≥	0.35	um
<b>RV0.S.1</b>	Space between square V0 and rectangular V0	≥	0.049	um
<b>RV0.S.2</b>	Space between two rectangular V0s	≥	0.047	um
<b>RV0.S.3</b>	Space between rectangular V0 and square or rectangular V0 when PRL $\geq$ -0.026um, DRC only flag the point-to-point space when PRL $\leq$ 0.	≥	0.051	um
<b>RV0.S.4</b>	Space between rectangular V0 to square or rectangular V0 when PRL > -0.032um for the short side of rectangular V0	≥	0.074	um
<b>RV0.S.4a</b>	Space between short side of rectangular V0 when PRL > 0um	=	0.074~ 0.082, $\geq$ 0.1	um
<b>RV0.S.5</b>	Corner space between rectangular V0 and square or rectangular V0 when PRL $\leq$ -0.032um	≥	0.051	um
<b>RV0.S.6</b>	Space between the long side of RV0 when PRL > 0um and with one M1 between two RV0s	≥	0.115	um
<b>RV0.S.7</b>	Space between RV0 and M0G at different net	≥	0.029	um
<b>RV0.S.8</b>	Space between RV0 and M0G at different net when PRL > -0.012um	≥	0.032	um
<b>RV0.S.9</b>	Space between RV0 and (M0 NOT M0C) at different net in S/D direction when PRL > -0.016um	≥	0.025	um
<b>RV0.S.10</b>	Space between RV0 and (M0 NOT M0C) line-end at different net when PRL > 0.01um	≥	0.025	um
<b>RV0.S.11</b>	(purposely blank)			
<b>RV0.S.12</b>	Space between rectangular V0 (INTERACT M0 width = 0.04/0.042um) and M0C concave corner when rectangular	≥	0.038	um

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Rule number	Description	Opt.	Design Value	Unit
	V0 and M0C interact same M0			
<b>RV0.S.13</b>	Space between rectangular V0 (INTERACT M0 width = 0.054um) and M0C concave corner when rectangular V0 and M0C interact same M0	$\geq$	0.082	um
<b>RV0.EN.1</b>	RV0 must be fully covered by (M0 NOT M0C) or M0G, and must follow RV0.EN.2, or RV0.EN.2a, or RV0.EN.3, or RV0.EN.4, or RV0.EN.5 as below			
<b>RV0.EN.2</b>	RV0 enclosure by (M0 NOT M0C) (M0 width = 0.04um at least two opposite sides) for two opposite sides with other two sides = 0.004um	$\geq$	0.019	um
<b>RV0.EN.2a</b>	RV0 enclosure by (M0 NOT M0C) (M0 width = 0.042um at least two opposite sides) for two opposite sides with other two sides = 0.005um	$\geq$	0.019	um
<b>RV0.EN.3</b>	RV0 enclosure by (M0 NOT M0C) (M0 width = 0.054um at least two opposite sides) for two opposite sides with other two sides = 0.011um	$\geq$	0.019	um
<b>RV0.EN.4</b>	RV0 enclosure by M0G (width = 0.04um at least two opposite sides) for two opposite sides with other two sides = 0.004um	$\geq$	0.019	um
<b>RV0.EN.5</b>	RV0 enclosure by M0G (width = 0.06um at least two opposite sides) for two opposite sides with other two sides = 0.014um	$\geq$	0.029	um
<b>RV0.EN.6</b>	RV0 must be fully covered by M1, and must follow RV0.EN.7 or RV0.EN.8, or RV0.EN.9 as below, where M1 is the metal layer directly above rectangular V0.			
<b>RV0.EN.7</b>	RV0 enclosure by M1	$\geq$	0.015	um
<b>RV0.EN.8</b>	RV0 enclosure by M1 for two opposite sides with the other two sides $\geq$ 0.005um	$\geq$	0.019	um
<b>RV0.EN.9</b>	Short side of rectangular V0 enclosure by M1 with the other two sides $\geq$ 0um	$\geq$	0.024	um
<b>RV0.EN.10</b>	V0 bar must be fully covered by (M0 NOT M0C) or M0G.			
<b>RV0.R.1</b>	Redundant via requirement must be obeyed by one of following conditions for M1 connection (M1 plate with length and width $\geq$ 0.162um) (two square vias are equal to			

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Rule number	Description	Opt.	Design Value	Unit
	one rectangular via for below conditions) (Except VIA bar) 1) At least one rectangular via 2) At least two square vias with space $\leq 0.091\text{um}$ 3) At least four square vias with space $\leq 0.415\text{um}$			
RV0.R.2	Redundant via requirement must be obeyed by one of following conditions for M1 connection (M1 plate with length and width $\geq 0.272\text{um}$ ) (two square vias are equal to one rectangular via for below conditions) (Except VIA bar, OCCD region) 1) At least 4 square vias with space $\leq 0.091\text{um}$ 2) At least 9 square vias with space $\leq 0.545\text{um}$ 3) At least 5 rectangular vias with space $\leq 0.545\text{um}$			
RV0.R.3	There should be at least two square V0 or one rectangular V0 in the intersection area of bottom metal and upper metal, when either wide M1 width and length $\geq 0.162\text{um}$ , the space between either via and wide metal is $\leq 0.5\text{um}$ (S, S is the shortest running path length from Via to the wide metal). (except via bar). DRC doesn't check M0G or M0 region that with at least two square or one rectangular V0 at the boundary of wide metal and branch			
RV0.R.4	There should be at least two square V0 or one rectangular V0 in the intersection area of bottom metal and upper metal, when either wide metal M1 width and length $\geq 0.272\text{um}$ , the space between either via and wide metal is $\leq 1\text{um}$ (S, S is the shortest running path length from Via to the wide metal). (except via bar). DRC doesn't check M0G or M0 region that with at least two square or one rectangular V0 at the boundary of wide metal and branch			
RV0.R.5	There should be at least two square V0 or one rectangular V0 in the intersection area of bottom metal and upper metal, when either wide metal M1 width and length $\geq 0.542\text{um}$ , the space between either via and wide metal is $\leq 3\text{um}$ (S, S is the shortest running path length from Via to the wide metal). (except via bar). DRC doesn't check M0G or M0 region that with at least two square or one rectangular V0 at the boundary of wide metal and branch. s			

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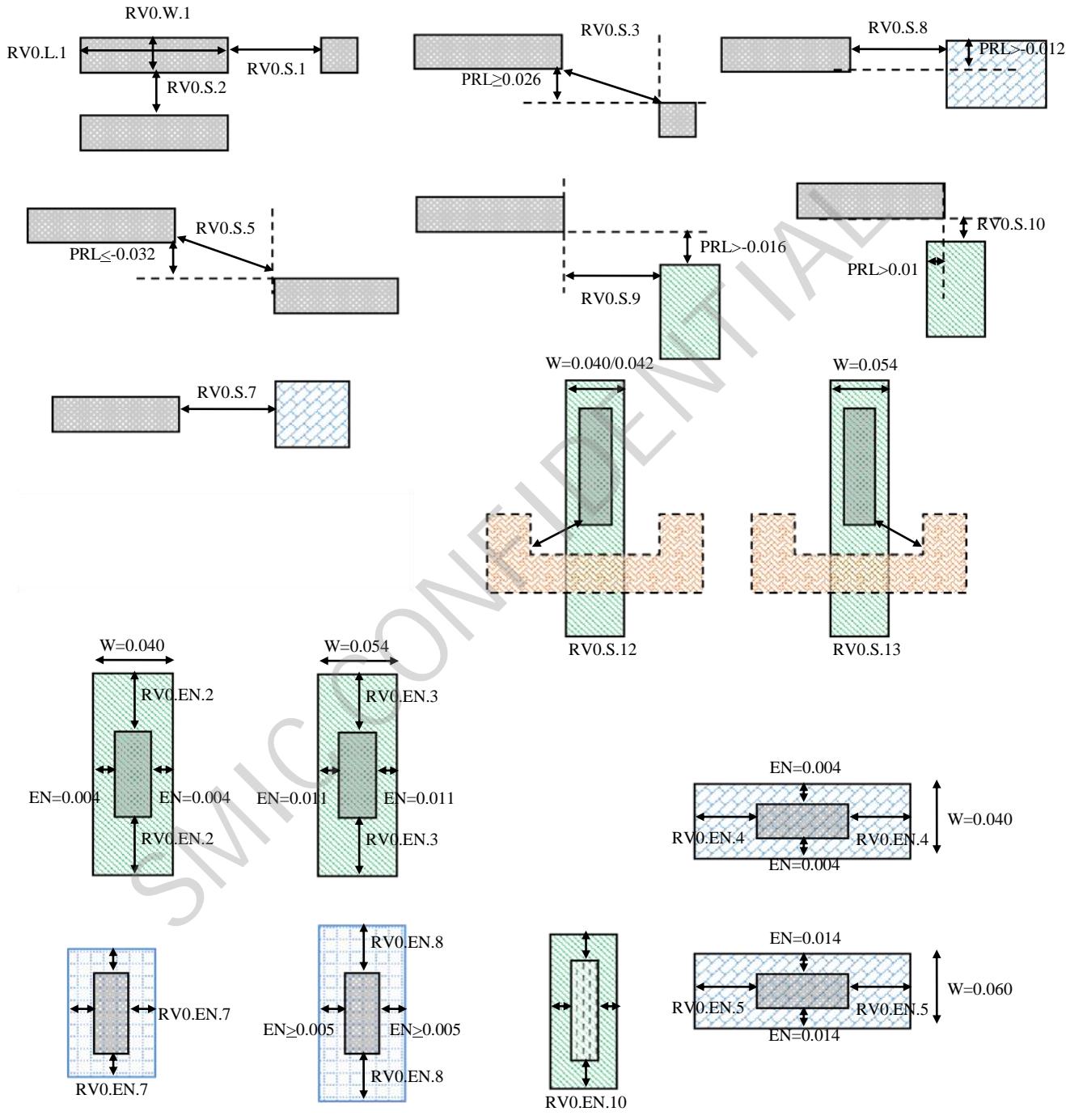
Rule number	Description	Opt.	Design Value	Unit
<b>RV0.R.6</b>	There should be at least two square V0 or one rectangular V0 in the intersection area of bottom metal and upper metal, when either wide metal M1 width and length $\geq 1.01\mu m$ , the space between either via and wide metal is $\leq 5\mu m$ (S, S is the shortest running path length from Via to the wide metal). (except via bar).  DRC doesn't check M0G or M0 region that with at least two square or one rectangular V0 at the boundary of wide metal and branch			
<b>RV0.R.7</b>	Maximum delta V $\geq 5.6V$ of (V0 OR RV0) is not allowed, when space between (V0 OR RV0) is $< 0.410\mu m$			
<b>RV0.R.8</b>	Rectangular V0 overlap with (M0G width = $0.05\mu m$ ) is not allowed.			

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Marks	M0C	M0G	M0	V0 bar	INST	RV0	M1

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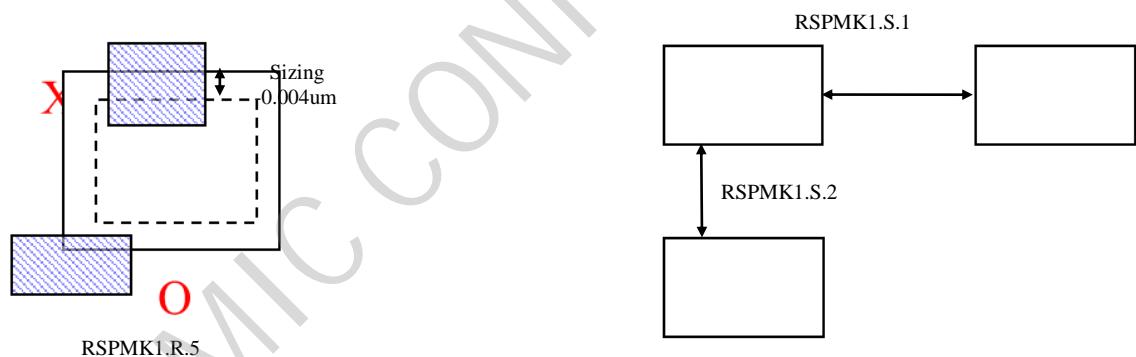
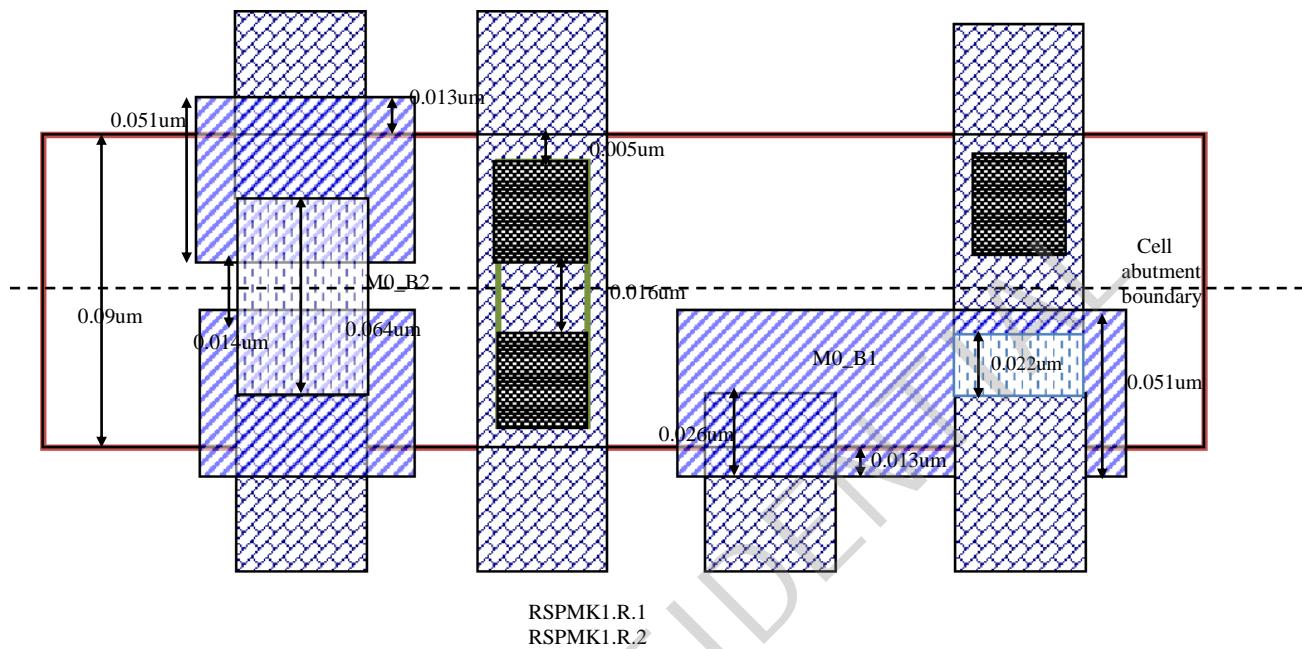
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### 7.2.32 Restricted special pattern design rules

RSPMK1 (CAD layer 131;153 ) is to define standard cell power rail marker layer 1

Rule number	Description	Opt.	Design Value	Unit
<b>RSPMK1.S.1</b>	RSPMK1 space	$\geq$	0.18	um
<b>RSPMK1.S.2</b>	RSPMK1 space in GATE poly direction	=	0.486, 0.39, $\geq 0.582$	um
<b>RSPMK1.EX.1</b>	M0C (width = 0.051um) extension on RSPMK1 in GATE poly direction	=	0.013	um
<b>RSPMK1.O.1</b>	M0C (width = 0.051um) overlap (AOP_M0 OR (M0_B1 OR M0_B2)) in GATE poly direction.	=	0.026/0. 051	um
<b>RSPMK1.R.1</b>	RSPMK1 must be a rectangle with width = 0.09um in GATE poly direction.			
<b>RSPMK1.R.2</b>	M0C (width = 0.051um) must interact RSPMK1.			
<b>RSPMK1.R.3</b>	RSPMK1 (length > 0.4um) must interact V0, and extension on either one side of V0 must be 0.005um in GATE poly direction			
<b>RSPMK1.R.4</b>	RSPMK1 overlap AOP_M0C (width = 0.048, 0.052, 0.082, 0.108um) or (AA NOT GTMK1) is not allowed			
<b>RSPMK1.R.5</b>	(RSPMK1 SIZING -0.004um) overlap M0G is not allowed.			
<b>RSPMK1.R.7</b>	RSPMK1 center line must align with any one of M1 center line in S/D direction.			

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2017-11-02

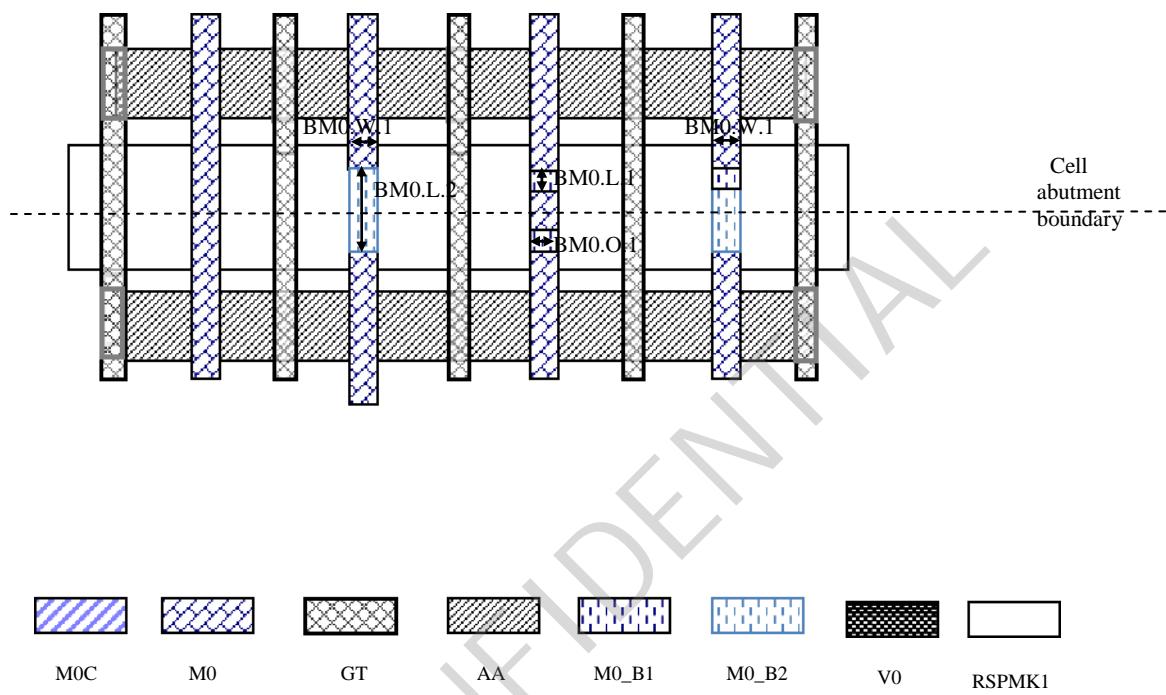
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### 7.2.33 Butted M0 design rules

M0\_B1 (59;13), M0\_B2 (59;14) are used to connect both M0 line-ends together (line-ends space = 0.022/0.064um) at cell boundary inside RSPMK1. Two M0s butted same M0\_B1 or M0\_B2 become one M0 when mask making process. M0\_B1 and M0\_B2 (with two butted M0s) will be treated as M0 and follow M0 rules in DRC.

Rule number	Description	Opt.	Design Value	Unit
<b>BM0.W.1</b>	M0_B1 or M0_B2 width in S/D direction	=	0.04	um
<b>BM0.L.1</b>	M0_B1 length in GATE poly direction	=	0.022	um
<b>BM0.L.2</b>	M0_B2 length in GATE poly direction	=	0.064	um
<b>BM0.O.1</b>	M0_B1 overlap M0 in GATE poly direction and S/D direction respectively.	=	0.022/0.04	um
<b>BM0.R.1</b>	M0_B1 or M0_B2 must be a rectangle and fully inside M0 or fully butted with M0 at either one horizontal side.			
<b>BM0.R.2</b>	(M0_B2 (INTERACT M0_B1) NOT M0_B1) must be one rectangle (width/length = 0.04/0.042um) and fully inside M0.			
<b>BM0.R.3</b>	M0_B2 (NOT INTERACT M0_B1) overlap M0 is not allowed.			
<b>BM0.R.4</b>	M0_B1 and M0_B2 must be inside RSPMK1.			
<b>BM0.R.5</b>	Horizontal edge of M0_B1/M0_B2 (horizontal edge fully butted with M0 at both sides) must be inside M0C.			
<b>BM0.R.6</b>	M0_B1 or M0_B2 interact (M0 (width = 0.054um) OR DOP_M0) is not allowed.			
<b>BM0.R.7</b>	M0_B2 interact two or three M0_B1 is not allowed.			

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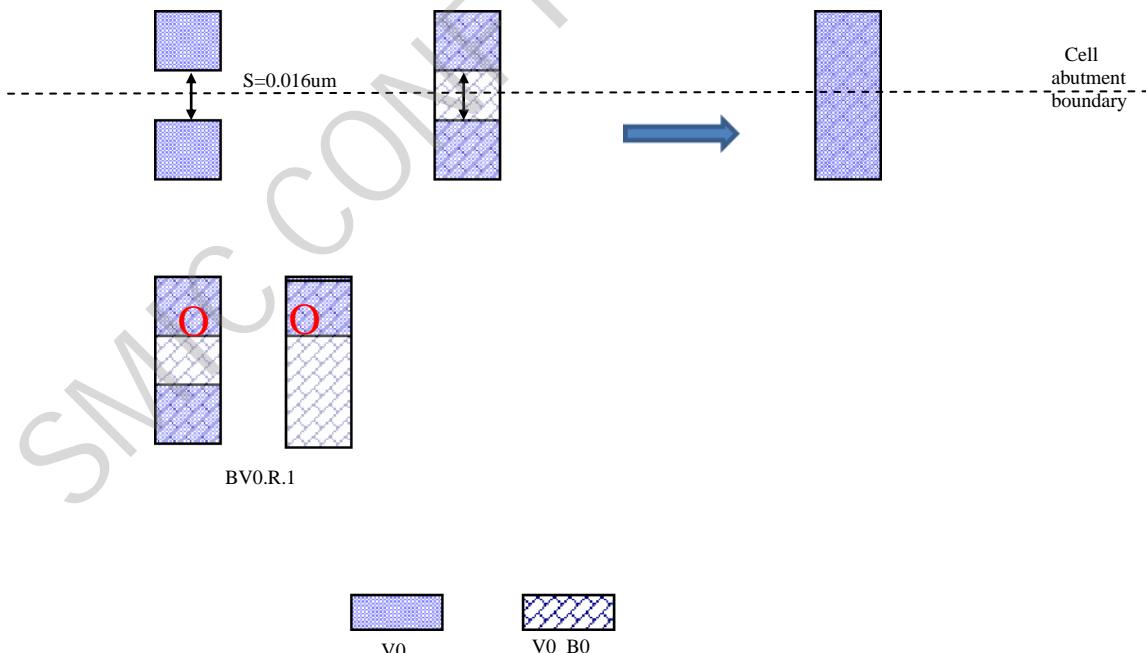
2017-11-02

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### 7.2.34 Butted V0 design rules

V0\_B0 (245;2) is used to replace two square V0 (space = 0.016um) with one square V0 or RV0 at cell boundary. Two square V0 touch same V0\_B0 become one rectangular V0 during mask making process. V0\_B0 which covers two square V0s will be treated as rectangular V0 and follow V0 rules in DRC.

Rule number	Description	Opt.	Design Value	Unit
<b>BV0.W.1</b>	V0_B0 width in S/D direction	=	0.032	um
<b>BV0.EN.1</b>	Square V0 enclosure by V0_B0 for three sides	=	0	um
<b>BV0.L.1</b>	Length of V0_B0	=	0.08	um
<b>BV0.R.1</b>	V0_B0 must overlap one or two square V0; V0_B0 overlap with RV0 is not allowed			



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### 7.2.35 M1 design rules

Rule number	Description	Opt.	Design Value	Unit
<b>M1.W.1</b>	M1 width	$\geq$	0.032	um
<b>M1.W.2</b>	M1 maximum width, except MARKS and LOGO regions	$\leq$	2.1	um
<b>M1.W.3</b>	M1 width when both side spaces are $\geq 0.058\text{um}$ and $\leq 0.062\text{um}$ , PRL of two spaces $\geq -0.099\text{um}$ and PRL of both side of metal $\leq 0.111\text{um}$ when metal A/B/C all in same color	$\geq$	0.036	um
<b>M1.W.4</b>	M1 branch width when connected to wide M1 (width $> 2\text{um}$ ) which enclosed inner hole ((M1 OR M1-hole) area $\geq 3050\text{um}^2$ ). DRC checks the M1 interact (((M1 OR M1-hole) sd 1um) su 1um) su 1um).	$\geq$	0.037	um
<b>M1.W.5</b>	M1 branch width when connected to wide M1 with both width and length $\geq 0.27\text{um}$	$\geq$	0.065	um
<b>M1.W.6</b>	Width of 45-degree bent M1	$\geq$	0.152	um
<b>M1.S.1</b>	Space between two M1s, except LOGO region	$\geq$	0.032	um
<b>M1.S.2</b>	Space between two M1s when one or both M1 enclosure of long side edge of RV0 $< 0.005\text{um}$ DRC flag the space between M1 and the long sides of RV0	$\geq$	0.035	um
<b>M1.S.3</b>	Space between two M1s when one or both M1 enclosure of long side edge of RV0 $< 0.003\text{um}$ DRC flag the space between M1 and the long sides of RV0	$\geq$	0.044	um
<b>M1.S.4</b>	(purposely blank)			
<b>M1.S.6</b>	45-degree bent M1 space to M1	$\geq$	0.152	um
<b>M1.S.7</b>	Space between M1 when one or both M1 width $\geq 0.091\text{um}$ when PRL $\geq 0.141\text{um}$	$=$	0.041~0.057, $\geq 0.072$	um
<b>M1.S.8</b>	Space between M1 when one or both M1 width $\geq 0.121\text{um}$ when PRL $\geq 0.141\text{um}$ , except OCOVL region	$=$	0.041~0.057, $\geq 0.106$	um
<b>M1.S.9</b>	Space between M1 when one or both M1 width $\geq 0.181\text{um}$ when PRL $\geq 0.189\text{um}$	$\geq$	0.125	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M1.S.10</b>	Space between M1 when one or both M1 width $\geq 0.271\text{um}$ when PRL $\geq 0.289\text{um}$	$\geq$	0.143	um
<b>M1.S.11</b>	Space between M1 when one or both M1 width $\geq 0.542\text{um}$ , except LOGO region	$\geq$	0.188	um
<b>M1.S.12</b>	Space between M1 when one or both M1 width $\geq 1.36\text{um}$ , except LOGO region	$\geq$	0.305	um
<b>M1.S.13</b>	Space between M1 and M1 line-end (width $< 0.046\text{um}$ ) when PRL $> -0.016\text{um}$	$\geq$	0.049	um
<b>M1.S.14</b>	Space between M1 line-end and line-end (width $< 0.046\text{um}$ ) when PRL $> -0.016\text{um}$ , except INST region	$\geq$	0.058	um
<b>M1.S.15</b>	Space between M1 and dense M1 line-end (width $< 0.046\text{um}$ , neighboring edge $\geq 0.048\text{um}$ ), when PRL $> -0.016\text{um}$ , except INST region  Dense M1 line end definition:  (W+S1) $< 0.09\text{um}$ , other metal must be in the region R, T and D is the extension from metal line end, T $< 0.016\text{um}$ , D $< 0.048\text{um}$ , S1 should be the space between separate metal. (Except small jog with edge length $< 0.032\text{um}$ )	$\geq$	0.069	um
<b>M1.S.16</b>	Space between M1 and M1 line-end space in metal array.  Metal array definition:  1) M1 width (W): $0.046\text{um} \leq W \leq 0.054\text{um}$ 2) M1 length (L) $\geq 0.135\text{um}$ 3) Searching distance (D) of M1 line-end edge: $0.048\text{um}$ 4) M1 space (S1) $0.058\text{um} \leq S1 \leq 0.076\text{um}$ for both long sides 5) M1 PRL $> 0\text{um}$ for short side (L1) 6) Line end space (S2) of both neighboring M1: $0.058\text{um} \leq S2 \leq 0.076\text{um}$ with PRL $> 0\text{um}$  DRC doesn't flag at least one $S1 \geq 0.058\text{um} \sim 0.063\text{um}$ with PRL $> 0.112\text{um}$ . And DRC flags forbidden space that has PRL $> 0\text{um}$ with both S2.	$\geq$	0.072	um
<b>M1.S.18</b>	M1 forbidden space when one M1 width $\geq 0.15\text{um}$ and PRL $> 0.135\text{um}$ , except M1 jog width $\leq 0.135\text{um}$ .  DRC searching range is from $0.106\text{um}$ to $0.729\text{um}$	=	0.058~0.062	um

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Rule number	Description	Opt.	Design Value	Unit
	DRC flags the forbidden space that totally inside the searching range along the space direction, and the PRL between forbidden space and the wide metal is $> 0.135\text{um}$			
M1.S.19	M1 forbidden space for single mask when M1 width $< 0.037\text{um}$ and PRL with neighboring M1 (W3) $> 0.117\text{um}$ DRC flags edge of $((W_1+S_1+W_2+S_2) \text{ or } (S_1+W_2+S_2+W_3)) = 0.141\text{~}0.159\text{um}$ . DRC waive when: (1) A/B or B/C are same polygons (2) A/C in different masks (3) INST region	=	0.141~0.159	um
M1.S.20	M1 forbidden space for single mask when 1. M1 width $< 0.034\text{um}$ and PRL with neighboring M1 (W2) $> 0.117\text{um}$ 2. M1 space: $0.032\text{um} \leq S_1 < 0.037\text{um}$ or $0.058\text{um} \leq S_1 < 0.068\text{um}$ , or $0.032\text{um} \leq S_3 < 0.037\text{um}$ or $0.058\text{um} \leq S_3 < 0.068\text{um}$ DRC flags edge of $((W_1+S_1+W_2+S_2) \text{ or } (S_1+W_2+S_2+W_3)) = 0.161\text{~}0.174$ DRC waive when: (1) A/B or B/C are same polygons (2) A/C in different masks (3) INST region	=	0.161~0.174	um
M1.S.21	Space between M1 and V0, RV0, V1, RV1 (maximum delta V $> 1.05\text{V}, 0.95\text{V}+10\%$ )	$\geq$	0.042	um
M1.S.22	Space between M1 and V0, RV0, V1, RV1 (maximum delta V $> 1.155\text{V}, 1.05\text{V}+10\%$ )	$\geq$	0.045	um
M1.S.23	Space between M1 and V0, RV0, V1, RV1 (maximum delta V $> 1.32\text{V}, 1.2\text{V}+10\%$ )	$\geq$	0.053	um
M1.S.24	Space between M1 and V0, RV0, V1, RV1 (maximum delta V $> 1.65\text{V}, 1.5\text{V}+10\%$ )	$\geq$	0.059	um
M1.S.25	Space between M1 and V0, RV0, V1, RV1 (maximum delta V $> 1.98\text{V}, 1.8\text{V}+10\%$ )	$\geq$	0.071	um
M1.S.26	Space between M1 and V0, RV0, V1, RV1 (maximum delta V $> 2.75\text{V}, 2.5\text{V}+10\%$ )	$\geq$	0.076	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M1.S.27</b>	Space between M1 and V0, RV0, V1, RV1 (maximum delta V > 3.63V, 3.3V+10%)	≥	0.159	um
<b>M1.S.28</b>	Space between M1 (maximum delta V > 1.05V, 0.95V+10%)	≥	0.04	um
<b>M1.S.29</b>	Space between M1 (maximum delta V > 1.155V, 1.05V+10%)	≥	0.042	um
<b>M1.S.30</b>	Space between M1 (maximum delta V > 1.32V, 1.2V+10%)	≥	0.045	um
<b>M1.S.31</b>	Space between M1 (maximum delta V > 1.65V, 1.5V+10%)	≥	0.050	um
<b>M1.S.32</b>	Space between M1 (maximum delta V > 2.75V, 2.5V+10%)	≥	0.068	um
<b>M1.S.33</b>	Space between M1 (maximum delta V > 3.63V, 3.3V+10%)	≥	0.104	um
<b>M1.S.34</b>	Space between M1 line end and M1 when PRL ≥ 0um (maximum delta V > 3.63V) (3.3V +10%) Definition of "M1 line end" M1edge with length < 0.046um(W) between two convex corners	≥	0.134	um
<b>M1.L.1</b>	M1 branch length when M1 branch width ≥ 0.065um and ≤ 0.269um, and connected to M1 plate with both width and length ≥ 0.27um  DRC waive the branch that can enclose at least one (0.005um*design value) orthogonal rectangle	≥	0.139	um
<b>M1.L.2</b>	M1 branch length when M1 branch width ≥ 0.065um and ≤ 0.269um, and connected to M1 plate with both width and length ≥ 0.542um  DRC waive the branch that can enclose at least one (0.005um* design value) orthogonal rectangle	≥	0.248	um
<b>M1.L.3</b>	M1 branch length when M1 branch width ≥ 0.065um and ≤ 0.269um, and connected to M1 plate with both width and length ≥ 1um  DRC waive the branch that can enclose at least one (0.005um* design value) orthogonal rectangle	≥	0.495	um
<b>M1.L.4</b>	M1 edge length with adjacent edge < 0.032um (these two edges formed by 3 consecutive 270-90-270degree inner angles; DRC don't flag if there is M1 within the area formed by 0.125um extension from these two edges and vertex)	≥	0.063	um

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Rule number	Description	Opt.	Design Value	Unit
M1.L.5	M1 edge length with adjacent edge $< 0.032\text{um}$ These two edges are formed by 3 consecutive 90-270-90 degree inner angles. DRC flags the edge which meets all the below conditions 1. Another adjacent edge is line-end (width $\leq 0.051\text{um}$ , 90-90 inner angles) 2. Enclosure of V0 by another adjacent edge $< 0.04\text{um}$	$\geq$	0.045	um
M1.L.6	M1 edge length with adjacent edge $< 0.032\text{um}$ These two edges are formed by 3 consecutive 90-270-90 degree inner angles. DRC flags the edge which meets all the below conditions 1. Another adjacent edge is line-end (width $\leq 0.051\text{um}$ , 90-90 inner angles) 2. Enclosure of V0 by another adjacent edge $< 0.04\text{um}$ 3. There is no M1 within the area formed by adjacent edge $< 0.032\text{um}$ expand edge $0.063\text{um}$ , extend $0.031\text{um}$	$\geq$	0.054	um
M1.L.7	Length of 45-degree bent M1, except MARKS region	$\geq$	0.445	um
M1.A.1	M1 area, except INST region	$\geq$	0.0061	um <sup>2</sup>
M1.A.2	M1 area (with all of edge lengths $< 0.203\text{um}$ , any edge length $\geq 0.117\text{um}$ ) Except: 1) The pattern can fill $0.045\text{um} \times 0.117\text{um}$ rectangular pattern 2) M1 edge of length $\geq 0.046\text{um}$ if this edge have another neighboring edge of length $< 0.032\text{um}$ 3) INST region	$\geq$	0.0072	um <sup>2</sup>
M1.A.3	M1 area when all of edge lengths $< 0.081\text{um}$ , except a M1 filling $0.077\text{um} \times 0.077\text{um}$ rectangular pattern, except INST region	$\geq$	0.0176	um <sup>2</sup>
M1.A.4	M1 enclosed area	$\geq$	0.16	um <sup>2</sup>
M1.D.1	M1 density (window $125\text{um} \times 125\text{um}$ , stepping $62.5\text{um}$ )	$\geq$	10%	
M1.D.2	M1 maximum density (window $125\text{um} \times 125\text{um}$ , stepping $62.5\text{um}$ )	$\leq$	85%	
M1.D.3	M1 density (window $50\text{um} \times 50\text{um}$ , stepping $25\text{um}$ ), except the window ( $15\% \leq \text{metal density} < 25\%$ ) not interact $3\text{um} \times 3\text{um}$ empty area, except OCOVL, (NODMF su 1um)	$\geq$	25%	

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Rule number	Description	Opt.	Design Value	Unit
	region			
<b>M1.D.4</b>	M1 maximum density (window 50um*50um, stepping 25um), except dummy metal	$\leq$	65%	
<b>M1.D.5</b>	M1 maximum density (window 50um*50um, stepping 25um)	$\leq$	75%	
<b>M1.D.6</b>	M1 density difference between any two neighboring checking windows (window 180 um*180um, stepping 180um).	$\leq$	40%	
<b>M1.D.7</b>	M1 maximum density ratio of ((M1 or dummy M1) INTERACT M1DPMK) to (M1 or dummy M1) (window 72um*72um, stepping 36um)	$\leq$	30%	
<b>M1.D.8</b>	M1 maximum density difference of ABS (((M1 OR M1DUM OR M1DOP) – (M1DP OR M1DPDUM OR M1DPDOP)) / ((M1 OR M1DUM OR M1DOP) + (M1DP OR M1DPDUM OR M1DPDOP))) This rule is applied post M1 layout decomposition	$\leq$	11%	
<b>M1.R.2</b>	Maximum delta V $\geq$ 5.6V is not allowed, when space between M1 and M1/V0/V1 is < 0.360um			
<b>M1.R.3<sup>[NC]</sup></b>	M1 line-end must be rectangular.			
<b>M1.R.4</b>	U-shape M1 pitch (W+S1) or (W+S2) must be $\geq$ 0.072um and V1 enclosure by M1 line-end (E) must be $\geq$ 0.032um, when: (1) Both PRL1 and PRL2 $\geq$ -0.015um; (2) Space (S) < 0.05um along length direction. (3) W < 0.04um. DRC waive if S1 or S2 > 0.04um This rule is not applied for INST region			
<b>M1.R.5</b>	U-shape M1 pitch (W+S1) or (W+S2) must be $\geq$ 0.072um, when: (1) Both PRL1 and PRL2 $\geq$ -0.015um; (2) Space (S) < 0.05um along length direction. (3) W < 0.04um. (4) M1 interact V0 and enclosure E < 0.032um. DRC waive if S1 or S2 > 0.04um			

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Rule number	Description	Opt.	Design Value	Unit
	This rule is not applied for INST region.			
M1.RSP.1	<p>Space between metal space segments with <math>S2 &lt; 0.072</math> and <math>L2 \leq 0.078\mu m</math>.</p> <p>Metal space segments definition:</p> <ol style="list-style-type: none"> <li>1) At least one metal line width <math>&gt; 0.09\mu m</math> (<math>W1</math>) and the parallel run length <math>&gt; 0.27\mu m</math> (<math>L1</math>) in metal space <math>&lt; 0.108\mu m</math> (<math>S1</math>) region;</li> <li>2) Metal space segments within metal space (<math>S1</math>) region and are generated by space cut line which is perpendicular with <math>L1</math> direction formed by all vertex in metal space region (<math>S1</math>);</li> <li>3) Metal space segments at least abut one metal with width <math>&gt; 0.09\mu m</math> (<math>W1</math>);</li> <li>4) <math>L2</math> is the width of metal space segments which is parallel with <math>L1</math> direction;</li> <li>5) <math>S2</math> is the width of metal space segments which is perpendicular with <math>L1</math> direction.</li> </ol>	$\geq$	0.298	$\mu m$
M1.RSP.2a	<p>Width (<math>S2</math>) of metal space segments with <math>L2 &gt; 0.078\mu m</math> (<math>0.058\mu m \leq S2A &lt; 0.072\mu m</math> is forbidden)</p> <p>Metal space segments definition:</p> <ol style="list-style-type: none"> <li>1) At least one metal line width <math>&gt; 0.09</math> (<math>W1</math>) and the parallel run length <math>&gt; 0.27\mu m</math> (<math>L1</math>) in metal space <math>&lt; 0.108\mu m</math> (<math>S1</math>) region;</li> <li>2) Metal space segments within metal space (<math>S1</math>) region and are generated by space cut line which is perpendicular with <math>L1</math> direction formed by all vertex in metal space region (<math>S1</math>);</li> <li>3) Metal space segments at least abut one metal with width <math>&gt; 0.09\mu m</math> (<math>W1</math>);</li> <li>4) <math>L2</math> is the width of metal space segments which is parallel with <math>L1</math> direction;</li> <li>5) <math>S2</math> is the width of metal space segments which is perpendicular with <math>L1</math> direction.</li> </ol>	$\geq$	0.041	$\mu m$
M1.RSP.2b	<p>Width (<math>S2</math>) of metal space segments with <math>L2 \leq 0.078\mu m</math></p> <p>Metal space segments definition:</p> <ol style="list-style-type: none"> <li>1) At least one metal line width <math>&gt; 0.09\mu m</math> (<math>W1</math>) and the parallel run length <math>&gt; 0.27\mu m</math> (<math>L1</math>) in metal space <math>&lt; 0.108\mu m</math> (<math>S1</math>) region;</li> <li>2) Metal space segments within metal space (<math>S1</math>) region and are generated by space cut line which is perpendicular with <math>L1</math> direction formed by all vertex in metal space region (<math>S1</math>);</li> <li>3) Metal space segments at least abut one metal with width <math>&gt; 0.09\mu m</math> (<math>W1</math>);</li> <li>4) <math>L2</math> is the width of metal space segments which is parallel</li> </ol>	$\geq$	0.032	$\mu m$

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Rule number	Description	Opt.	Design Value	Unit
	with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.RSP.3	Space between metal space segments with $S2 < 0.106\mu m$ and $L2 \leq 0.078\mu m$ . Metal space segments definition: 1) At least one metal line width $> 0.12\mu m$ (W1) and the parallel run length $> 0.27\mu m$ (L1) in metal space $< 0.126\mu m$ (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width $> 0.12\mu m$ (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	$\geq$	0.298	um
M1.RSP.4a	Width (S2) of metal space segments with $L2 > 0.078\mu m$ , ( $0.058\mu m \leq S < 0.106\mu m$ is forbidden), except OCOVL region Metal space segments definition: 1) At least one metal line width $> 0.12\mu m$ (W1) and the parallel run length $> 0.27\mu m$ (L1) in metal space $< 0.126\mu m$ (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width $> 0.12\mu m$ (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	$\geq$	0.041	um
M1.RSP.4b	Width (S2) of metal space segments with $L2 \leq 0.078\mu m$ ( $0.058\mu m \leq S < 0.072\mu m$ is forbidden) Metal space segments definition: 1) At least one metal line width $> 0.12\mu m$ (W1) and the parallel run length $> 0.27\mu m$ (L1) in metal space $< 0.126\mu m$ (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with	$\geq$	0.041	um

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Rule number	Description	Opt.	Design Value	Unit
	L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.12um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.RSP.5	Space between metal space segments with $S2 < 0.126\text{um}$ and $L2 \leq 0.078\text{um}$ . Metal space segments definition: 1) At least one metal line width $> 0.18\text{um}$ (W1) and the parallel run length $> 0.27\text{um}$ (L1) in metal space $< 0.144\text{um}$ (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width $> 0.18\text{um}$ (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	$\geq$	0.298	um
M1.RSP.6a	Width (S2) of metal space segments with $L2 > 0.078\text{um}$ Metal space segments definition: 1) At least one metal line width $> 0.180\text{um}$ (W1) and the parallel run length $> 0.27\text{um}$ (L1) in metal space $< 0.144\text{um}$ (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width $> 0.18\text{um}$ (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	$\geq$	0.125	um
M1.RSP.6b	Width (S2) of metal space segments with $L2 \leq 0.078\text{um}$ Metal space segments definition: 1) At least one metal line width $> 0.180\text{um}$ (W1) and the parallel run length $> 0.27\text{um}$ (L1) in metal space $< 0.144\text{um}$ (S1) region; 2) Metal space segments within metal space (S1) region and	$\geq$	0.107	um

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Rule number	Description	Opt.	Design Value	Unit
	are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.18um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.RSP.7	Space between metal space segments with $S2 < 0.144$ and $L2 \leq 0.078$ um. Metal space segments definition: 1) At least one metal line width > 0.270um (W1) and the parallel run length > 0.27um (L1) in metal space < 0.261um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.270 um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	$\geq$	0.298	um
M1.RSP.8a	Width (S2) of metal space segments with $L2 > 0.078$ um Metal space segments definition: 1) At least one metal line width > 0.270um (W1) and the parallel run length > 0.27um (L1) in metal space < 0.261um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.270 um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	$\geq$	0.142	um
M1.RSP.8b	Width (S2) of metal space segments with $L2 \leq 0.078$ um Metal space segments definition: 1) At least one metal line width > 0.27um (W1) and the parallel run length > 0.27um (L1) in metal space < 0.261um (S1) region;	$\geq$	0.125	um

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Rule number	Description	Opt.	Design Value	Unit
	2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.270 um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.OR.0 <sup>[NC]</sup>	Odd ring conflict space definition: OR Line Space (ORLS): polygons violate any one of the odd ring space rules from M1.ORCS.1 to M1.ORCS.3 OR Corner Space (ORCS): polygons violate any one of the odd ring space rule M1.ORCS.1a OR-AREA definition: 1. Odd ring line area (ORLA): The projection area between two edges with ORLS 2. Odd ring corner area (ORCA): The line between two corners with ORCS 3. ORLA or ORCA region are independent to all other ones, even if they are overlapped or crossed Loop: 1. A loop is formed when polygons of M1 are connected in a cycle sequence with OR-AREA in between 2. A loop cannot contain any sub-loops which share one or more polygons with it Path: A path is formed when polygons of M1 are connected one by one from one marker to another marker with OR-AREA in between			
M1.ORCS.1	Space between M1s when PRL > -0.015um	≥	0.058	um
M1.ORCS.1a	Corner space between M1s when PRL ≤ -0.015um	≥	0.058	um
M1.ORCS.2	Space between M1s when PRL > -0.015um Except the following conditions (these two conditions are only applied to different polygons) 1) M1 space perpendicular to width direction (M1 width ≥ 0.056um and PRL ≤ 0.112um) 2) M1 space parallel to width direction (M1 width ≥ 0.047um (both sides) and PRL ≤ 0.21um) 3) INST regions	≥	0.063	um

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Rule number	Description	Opt.	Design Value	Unit
<b>M1.ORCS.3</b>	Space between M1 line-end and M1 when PRL > -0.015um; M1 line-end definition: (width < 0.046um, 90-90 inner angles), except INST region	$\geq$	0.08	um
<b>M1.OR.1</b>	OR-AREA formed by single polygon is not allowed, except LOGO region			
<b>M1.OR.2</b>	ORCA cross another ORCA or touch ORLA is not allowed.			
<b>M1.OR.3</b>	OR-AREA count of the close loop formed by original polygons and OR-AREA cannot be odd number.			
<b>M1.OR.4</b>	M1DPMK must be drawn identically to M1.			
<b>M1.OR.5</b>	(M1 INTERACT M1DPMK) INTERACT ORLS or ORCS is not allowed.			
<b>M1.OR.6</b>	(M1 INTERACT INST) INTERACT M1DPMK is not allowed.			
<b>M1.OR.7</b>	Pre-coloring marker M1CA and M1CB must be drawn identically to M1.			
<b>M1.OR.8</b>	M1CA INTERACT M1CB is not allowed.			
<b>M1.OR.9</b>	(M1 INTERACT INST) INTERACT (M1CA OR M1CB) is not allowed.			
<b>M1.OR.10</b>	(M1CA OR M1CB) INTERACT M1DPMK is not allowed.			
<b>M1.OR.11</b>	OR-AREA count of any path starting from M1CA and ending at M1CA must not be a odd number.			
<b>M1.OR.12</b>	OR-AREA count of any path starting from M1CB and ending at M1CB must not be a odd number.			
<b>M1.OR.13</b>	OR-AREA count of any path starting from M1CA and ending at M1CB must not be a even number.			
<b>M1.OR.14</b>	Maximum pre-coloring ratio of ((M1CA + M1CB + M1DPMK)/M1) before decomposition	<	16%	

Note:

1. M1 is double patterning process. The rule like “M1.OR.\*” is for odd ring check rules, and the rule like “M1.ORCS.\*” is for odd ring conflict space check rules.

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2. V0 and V1 enclosure by M1 should be as large as the layout allows.
3. It is recommended that the lengths of metal lines are orthogonal to the lengths of metal lines on neighboring layers.

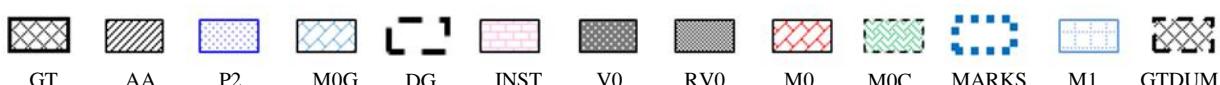
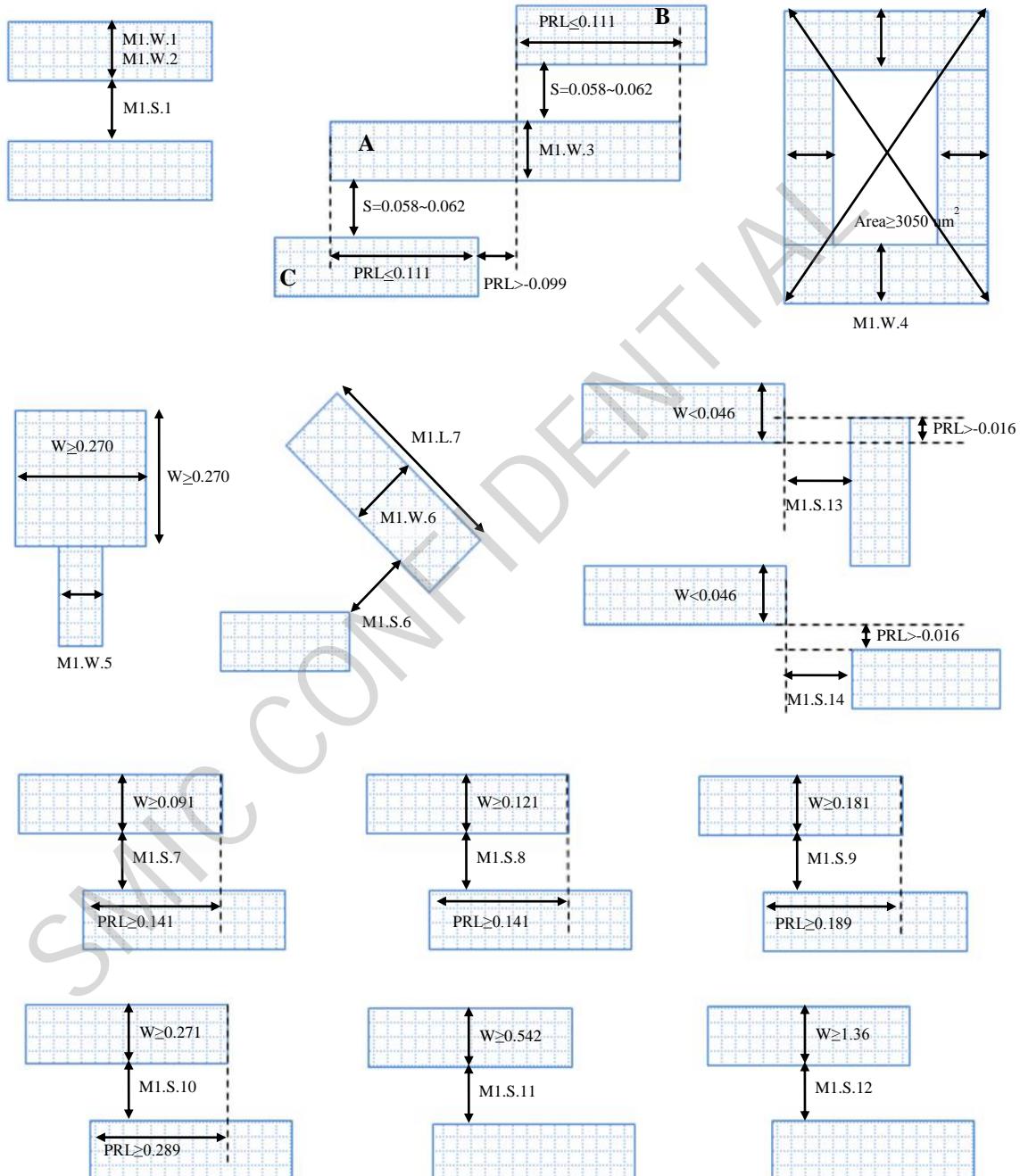
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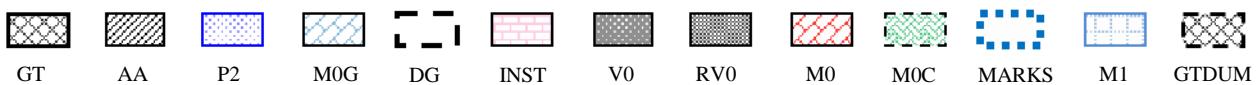
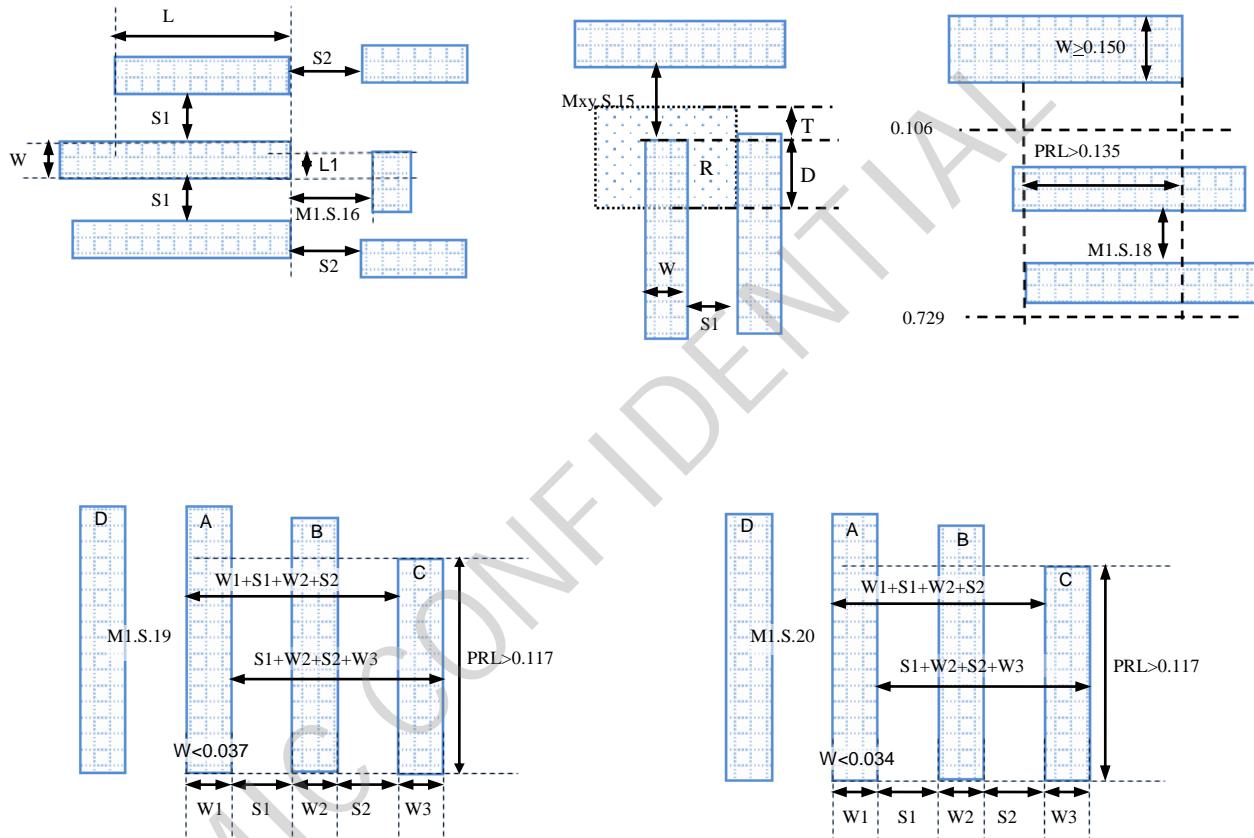
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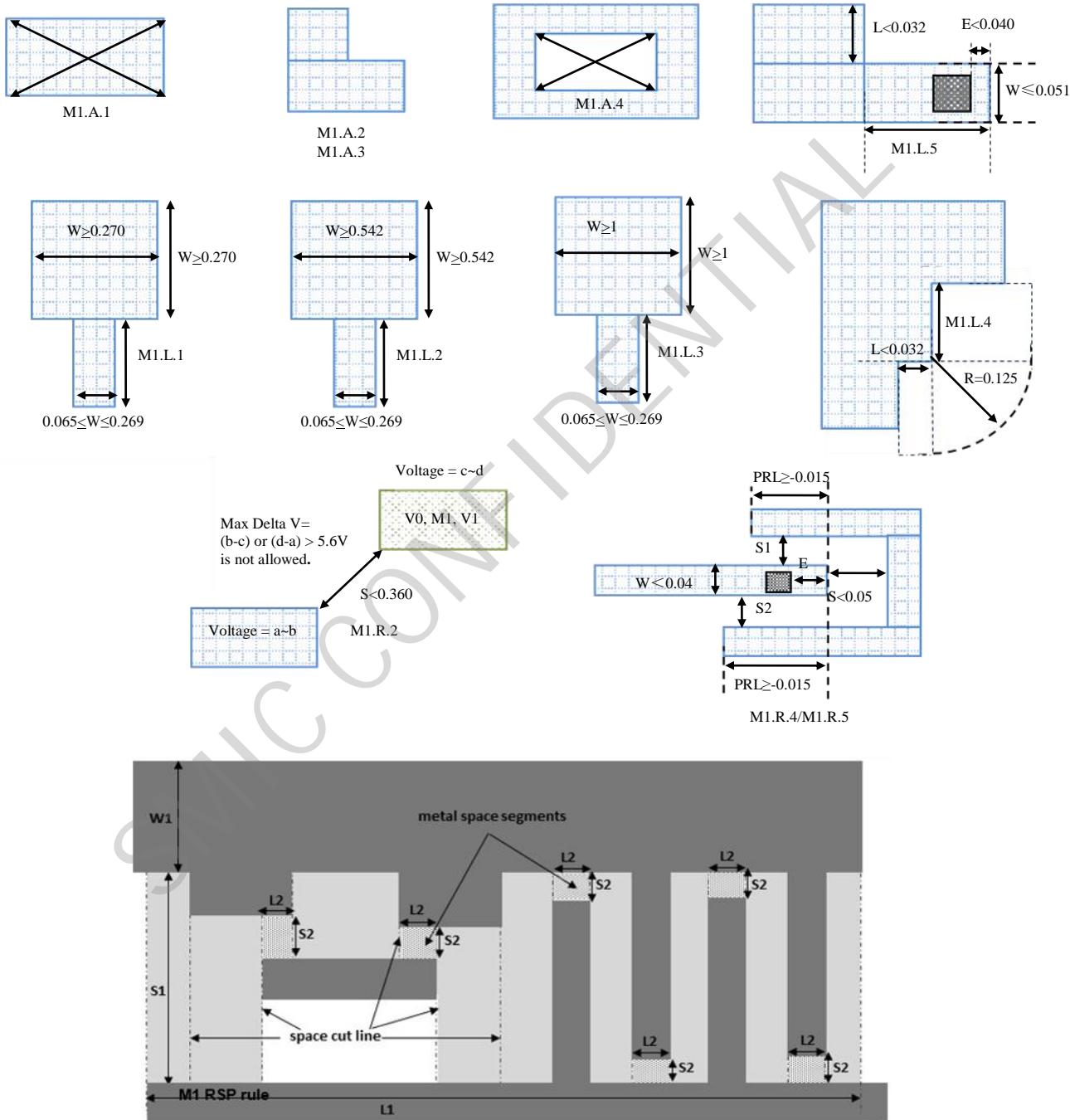


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GT AA P2 M0G DG INST V0/V1 RV0 M0 M0C MARKS M1 GTDUM

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## 7.2.36 Vy design rules

### 7.2.36.1 Square Vy design rules

Rule number	Description	Opt.	Design Value	Unit
<b>Vy.W.1</b>	Vy width and length (except 0.032*0.08um RVy, MARKS, MARKG, INDMY and LOGO region)	=	0.032	um
<b>Vy.W.2</b>	Vy bar width in MARKS and MARKG regions	=	0.1, 0.45	um
<b>Vy.S.1</b>	Space between two (Vy or RVy), except Vy.S.1a	≥	0.069	um
<b>Vy.S.1a</b>	Space between two (Vy or RVy) when under 1.25xMy	≥	0.066	um
<b>Vy.S.2</b>	Space between two Square Vy when PRL > -0.032um, except V1 in INST region, DRC only flag the point-to-point space when PRL ≤ 0.	≥	0.082	um
<b>Vy.S.3</b>	Space between square Vy and RVy	≥	0.082	um
<b>Vy.S.4</b>	Space between Vy and Vy-1 (including V0) at different net and PRL > 0um, when Mxy+1/1.25xMy enclosure of Vy > 0um	≥	0.038	um
<b>Vy.S.5</b>	Space between Vy and Mxy (including M1) at different net except V1 in INST region, when 1. Mxy (including M1) enclosure of Vy < 0.003um. 2. Mxy+1/1.25xMy width > 0.038um	≥	0.037	um
<b>Vy.S.6</b>	Projection space between Vy and the Mxy+1/1.25xMy concave corner, when 1. Mxy+1/1.25xMy width < 0.035um, form one edge of concave corner. 2. Vy enclosure by Mxy+1/1.25xMy ≤ 0.002um at opposite side of Mxy+1/1.25xMy concave corner. 3. The length of another edge of concave corner > 0.005um Via inside the cross region with vertex enclosure ≤ 0.001um is not allowed.	≥	0.029	um
<b>Vy.S.7</b>	Space between two square Vy with PRL ≥ -0.089um, and when 1) Vy enclosure by 1.25xMy ≤ 0.008um at opposite side. 2) Space between Vy and 1.25xMy ≤ 0.052um with PRL ≥	≥	0.099	um

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Rule number	Description	Opt.	Design Value	Unit
	-0.047um at opposite side. DRC doesn't flag space between Vy and $1.25 \times M_y \leq 0.052\text{um}$ with $PRL \geq -0.047\text{um}$ on both sides.			
Vy.S.8	Space between Vy bar (width = 0.1/0.45um) and (Vy or RVy)	$\geq$	0.34	um
Vy.S.9	Space between two Vy bar (width = 0.1/0.45um), DRC only check the space between parallel edge when the Vy bar is inside MARKS	$\geq$	0.55	um
Vy.EN.1	1X square Vy must be fully enclosed by M1 or Mxy where M1/Mxy is the metal layer directly underneath Vy, Vy enclosure by M1 or Mxy must follow either Vy.EN.2 or Vy.EN.3			
Vy.EN.2	Vy enclosure by M1 or Mxy when enclosure by M1 or Mxy on either perpendicular direction $\geq 0\text{um}$ , except V1 in INST region	$\geq$	0.024	um
Vy.EN.3	Vy enclosure by M1 or Mxy for all sides, except V1 in INST region	$\geq$	0.015	um
Vy.EN.4	Vy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath Vy, when 1. Mxy width W: $0.036\text{um} \leq W \leq 0.041\text{um}$ 2. Space: $0.058\text{um} \leq S_1 < 0.063\text{um}$ , $PRL \geq 0.083\text{um}$ . 3. The opposite space S2 $\geq 0.069\text{um}$	$\geq$	0.004	um
Vy.EN.4a	Vy enclosure by M1 in adjacent S1 side, where M1 is the metal layer directly underneath Vy, when 1. M1 width W: $0.036\text{um} \leq W \leq 0.041\text{um}$ 2. Space: $0.058\text{um} \leq S_1 < 0.063\text{um}$ , $PRL \geq 0.083\text{um}$ . 3. The opposite space S2 $\geq 0.069\text{um}$ DRC doesn't check V1 in INST region.	$\geq$	0.004	um
Vy.EN.4b	Vy enclosure by M1 in adjacent S1 side, where M1 is the metal layer directly underneath Vy, when 1. M1 width W: $0.042\text{um} \leq W \leq 0.05\text{um}$ 2. Space: $0.058\text{um} \leq S_1 \leq 0.067\text{um}$ , $PRL \geq 0.136\text{um}$ . DRC doesn't check V1 in INST region.	$\geq$	0.004	um

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Rule number	Description	Opt.	Design Value	Unit
Vy.EN.5	Vy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath Vy, when 1. Mxy width W: $0.042\text{um} < W \leq 0.05\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.067\text{um}$ , PRL $\geq 0.083\text{um}$ .	$\geq$	0.004	um
Vy.EN.6	Vy enclosure by M1 in adjacent S1 side, where M1 is the metal layer directly underneath Vy, when 1. M1 width W: $0.051\text{um} \leq W \leq 0.112\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.094\text{um}$ , PRL $\geq 0.136\text{um}$ . DRC doesn't check Vy: a) Two Vys with space $\leq 0.1\text{um}$ in M1 and $1.25 \times M_y/M_{xy}$ intersection region. b) One Vy and one rectangular Vy with space $\leq 0.1\text{um}$ in M1 and $1.25 \times M_y/M_{xy}$ intersection region.	$\geq$	0.004	um
Vy.EN.7	Vy enclosure by M1 in adjacent S1 side, where M1 is the metal layer directly underneath Vy, when 1. M1 width W: $0.061\text{um} \leq W \leq 0.09\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.079\text{um}$ , PRL $\geq 0.136\text{um}$ .	$\geq$	0.008	um
Vy.EN.8	Vy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath Vy, when 1. Mxy width W: $0.051\text{um} \leq W \leq 0.112\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.094\text{um}$ , PRL $\geq 0.083\text{um}$ . DRC doesn't check Vy: a) Two Vys with space $\leq 0.1\text{um}$ in Mxy and $1.25 \times M_y/M_{xy+1}$ intersection region. b) One Vy and one rectangular Vy with space $\leq 0.1\text{um}$ in Mxy and $1.25 \times M_y/M_{xy+1}$ intersection region.	$\geq$	0.004	um
Vy.EN.9	Vy enclosure by M1/Mxy in adjacent S1 side, where M1/Mxy is the metal layer directly underneath Vy, when 1. M1/Mxy dimension along enclosure direction: $0.113\text{um} \leq L \leq 0.201\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.094\text{um}$ , PRL $\geq 0.083\text{um}$ .	$\geq$	0.004	um
Vy.EN.10	Vy enclosure by M1/Mxy in adjacent S1 side, where M1/Mxy is the metal layer directly underneath Vy, when	$\geq$	0.014	um

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Rule number	Description	Opt.	Design Value	Unit
	1. M1/Mxy dimension along enclosure direction: $L \geq 0.202\mu m$ 2. Space: $0.058\mu m \leq S1 \leq 0.094\mu m$ , $PRL \geq 0.083\mu m$ .			
<b>Vy.EN.11</b>	Vy bar must fully enclosure by Mxy (including M1) where Mxy is the metal layer directly underneath Vy bar	$\geq$	0.2	um
<b>Vy.EN.12</b>	1X square Vy must be fully enclosure by $Mxy+1/1.25xMy$ where $Mxy+1/1.25xMy$ is the metal layer directly above Vy, Enclosure by $Mxy+1/1.25x My$ must follow one of Vy.EN.13 or Vy.EN.16a or Vy.EN.16b or Vy.EN.16c or Vy.EN.16d or Vy.EN.16e or Vy.EN.16f or Vy.EN.16g or Vy.EN.17 or Vy.EN.17a or Vy.EN.18, Vy.EN.18a or Vy.EN.19 or Vy.EN.20 or Vy.EN.21.			
<b>Vy.EN.13</b>	Vy enclosure by $Mxy+1$ for all sides	$\geq$	0.015	um
<b>Vy.EN.16a</b>	Vy enclosurere by $Mxy+1$ ( $0.032\mu m < \text{short side of } Mxy+1$ width $\leq 0.046\mu m$ ) for opposite side $\geq 0.032\mu m$ with the two sides $\geq 0.003\mu m$ , except V1 in INST region	$\geq$	0.047	um
<b>Vy.EN.16b</b>	Vy enclosurere by $Mxy+1$ for two opposite sides with the other two sides $\geq 0.008\mu m$ ( $0.046\mu m < \text{short side of } Mxy+1$ width $\leq 0.09\mu m$ ), except V1 in INST region	$\geq$	0.024	um
<b>Vy.EN.16c</b>	Vy enclosure by $Mxy+1$ for two opposite sides with the other two sides $\geq 0.014\mu m$ ( $0.09\mu m < \text{short side of } Mxy+1$ width $\leq 0.2\mu m$ ), except V1 in INST region	$\geq$	0.024	um
<b>Vy.EN.16d</b>	Vy enclosure by $Mxy+1$ for at least two adjacent edges with the other two sides $\geq 0.024\mu m$ and $\geq 0.009\mu m$ ( $0.09\mu m < \text{short side of } Mxy+1$ width $\leq 0.2\mu m$ ), except V1 in INST region	$\geq$	0.058	um
<b>Vy.EN.16e</b>	Vy enclosure by $Mxy+1$ for two opposite sides with the other two sides $\geq 0.014\mu m$ (short side of $Mxy+1$ width $> 0.2\mu m$ )	$\geq$	0.024	um
<b>Vy.EN.16f</b>	Total Vy enclosure by $Mxy+1$ ( $Mxy+1$ width = $0.032\mu m$ , both two opposite sides (EN1A/EN2A) $\geq 0.036\mu m$ ) with the other two sides $\geq 0\mu m$	$\geq$	0.079	um
<b>Vy.EN.16g</b>	Total Vy enclosure by $Mxy+1$ ( $Mxy+1$ width = $0.032\mu m$ , both two opposite side EN $\geq 0.03\mu m$ ) with the other two sides (EN1A/EN2A) $\geq 0\mu m$ ) (for iso Vy condition only).  Iso Vy condition definition:	$\geq$	0.069	um

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Rule number	Description	Opt.	Design Value	Unit
	S1 > 0.13um and S2 > 0.09um, where S1 is via space to metal in length direction and S2 is via space to metal in width direction)			
Vy.EN.17	Vy enclosure by 1.25xMy (width = 0.04um) for two opposite sides with the other two sides $\geq 0.004\text{um}$	$\geq$	0.034	um
Vy.EN.17a	Vy enclosure by 1.25xMy (width = 0.042um) for two opposite sides with the other two sides $\geq 0.005\text{um}$	$\geq$	0.034	um
Vy.EN.18	Vy enclosure by 1.25xMy (width = 0.044um) for two opposite sides with the other two sides $\geq 0.006\text{um}$	$\geq$	0.034	um
Vy.EN.18a	Vy enclosure by 1.25xMy (width = 0.046um) for two opposite sides with the other two sides $\geq 0.007\text{um}$	$\geq$	0.034	um
Vy.EN.19	Vy enclosure by 1.25xMy ( $0.06\text{um} \leq \text{width} < 0.08\text{um}$ ) for two opposite sides with the other two sides $\geq 0.014\text{um}$	$\geq$	0.034	um
Vy.EN.20	Vy enclosure by 1.25xMy (width = 0.08um) for all sides	$\geq$	0.024	um
Vy.EN.21	Vy enclosure by 1.25xMy (width $> 0.08\text{um}$ ) for two opposite sides with the other two sides $\geq 0.024\text{um}$	$\geq$	0.03	um
Vy.EN.22	Vy enclosure by Mxy+1 in adjacent S1 side, where Mxy+1 is the metal layer directly above Vy, when 1. Mxy+1 width W: $0.036\text{um} \leq W \leq 0.041\text{um}$ 2. $0.058\text{um} \leq S1 < 0.063\text{um}$ , PRL $\geq 0.083\text{um}$ . 3. The opposite space S2 $\geq 0.069\text{um}$	$\geq$	0.004	um
Vy.EN.23	Vy enclosure by 1.25xMy edge (between two consecutive 90-270 degree corners, length $< 0.16\text{ um}$ ), when PRL $> 0$	$\geq$	0.029	um
Vy.EN.24	Vy enclosure by 1.25xMy for two opposite sides (PRL $> 0$ ) with the other side enclosure $< 0.04\text{um}$ (corresponding edge length $< 0.16\text{um}$ between two consecutive 90-270 degree corners)	$\geq$	0.04	um
Vy.EN.25	Vy bar must fully enclosure by Mxy+1/1.25xMy where Mxy+1/1.25xMy is the metal layer directly above Vy bar	$\geq$	0.2	um
Vy.D.1 <sup>[R]</sup>	(Vy OR RVy) density (window 5um*5um, stepping 2.5um)	$<$	7.7%	
Vy.R.1	45-degree (Vy OR RVy) is not allowed.			

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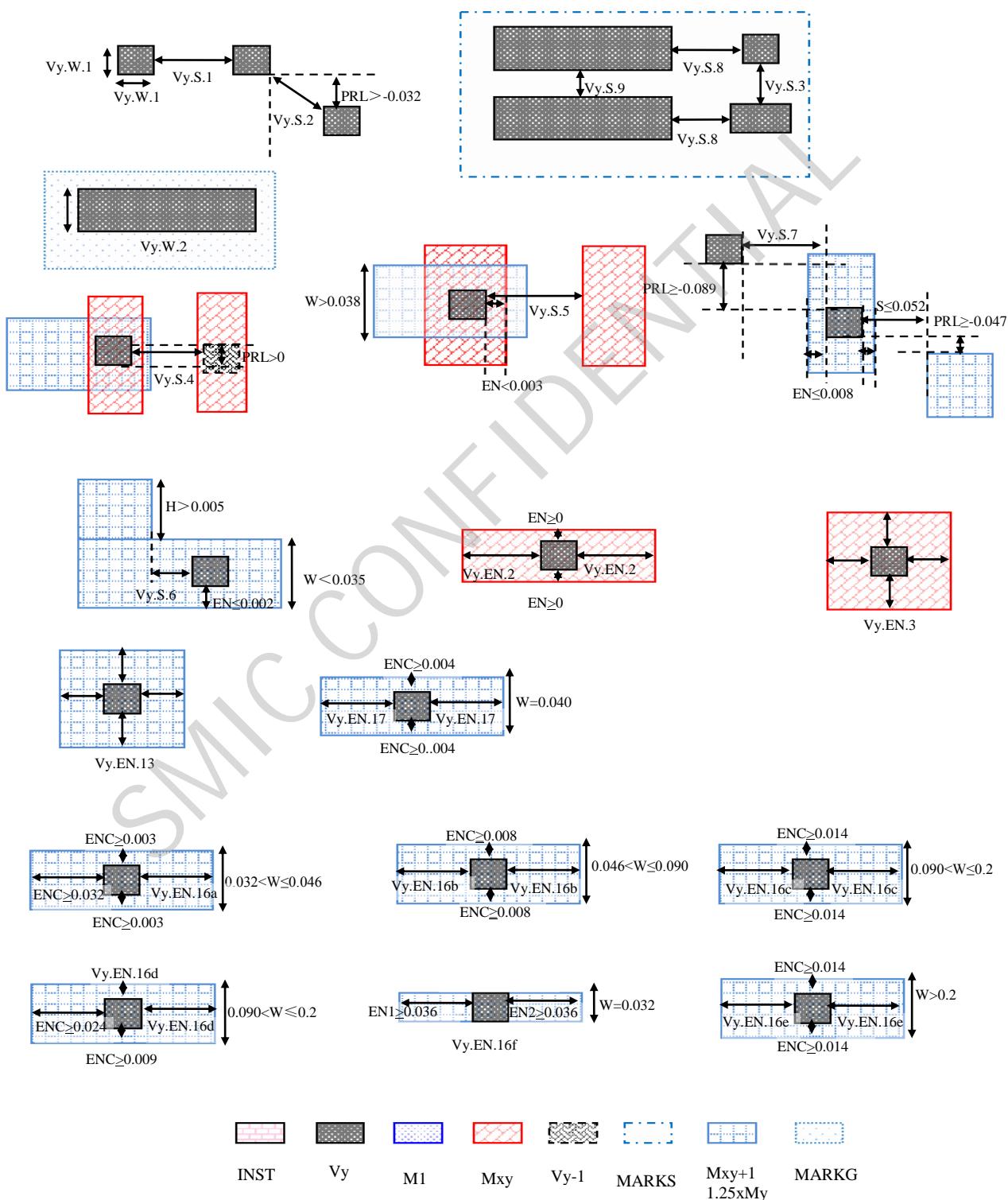


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Rule number	Description	Opt.	Design Value	Unit
Vy.R.2	Single Vy is not allowed in "H-shape" M <sub>xy+1/1.25x</sub> My, when: 1. The M <sub>xy+1/1.25x</sub> My has "H-shape" interacting with two metal holes: both two metal holes length $\leq 4.5\text{um}$ and two metal hole area $\leq 4.05\text{um}^2$ 2. The Vy overlaps on the center metal bar of this "H-shape" M <sub>xy+1/1.25x</sub> My. 3. The center metal bar length $\leq 0.9\text{um}$ and the metal bar width $\leq 0.12\text{um}$ .			
Vy.R.3	The numbers of neighboring square Vy to each edge of Vy (space $\leq 0.077\text{um}$ ) when Vy under 1.25xMy	<	2	
Vy.R.4	The numbers of neighboring square Vy in one group (space $\leq 0.077\text{um}$ ) when Vy under 1.25xMy.	$\leq$	3	
Vy.R.5	Maximum delta V $\geq 5.6\text{V}$ is not allowed, when space between Vy is $< 0.410\text{um}$			
Vy.R.7	(Vy OR RVy) overlap MTFUSE is not allowed, except V3			
Vy.R.8 <sup>[NC]</sup>	Vy pattern must be drawn on data type 40.			
Vy.R.9	It's not allowed Vy overlap with the metal resistor directly underneath and above the Vy			
Vy.R.10 <sup>[R]</sup>	Recommend space between a square Vy and another (Vy OR RVy OR DUM_Vy) $< 4\text{um}$ to avoid single square Vy			

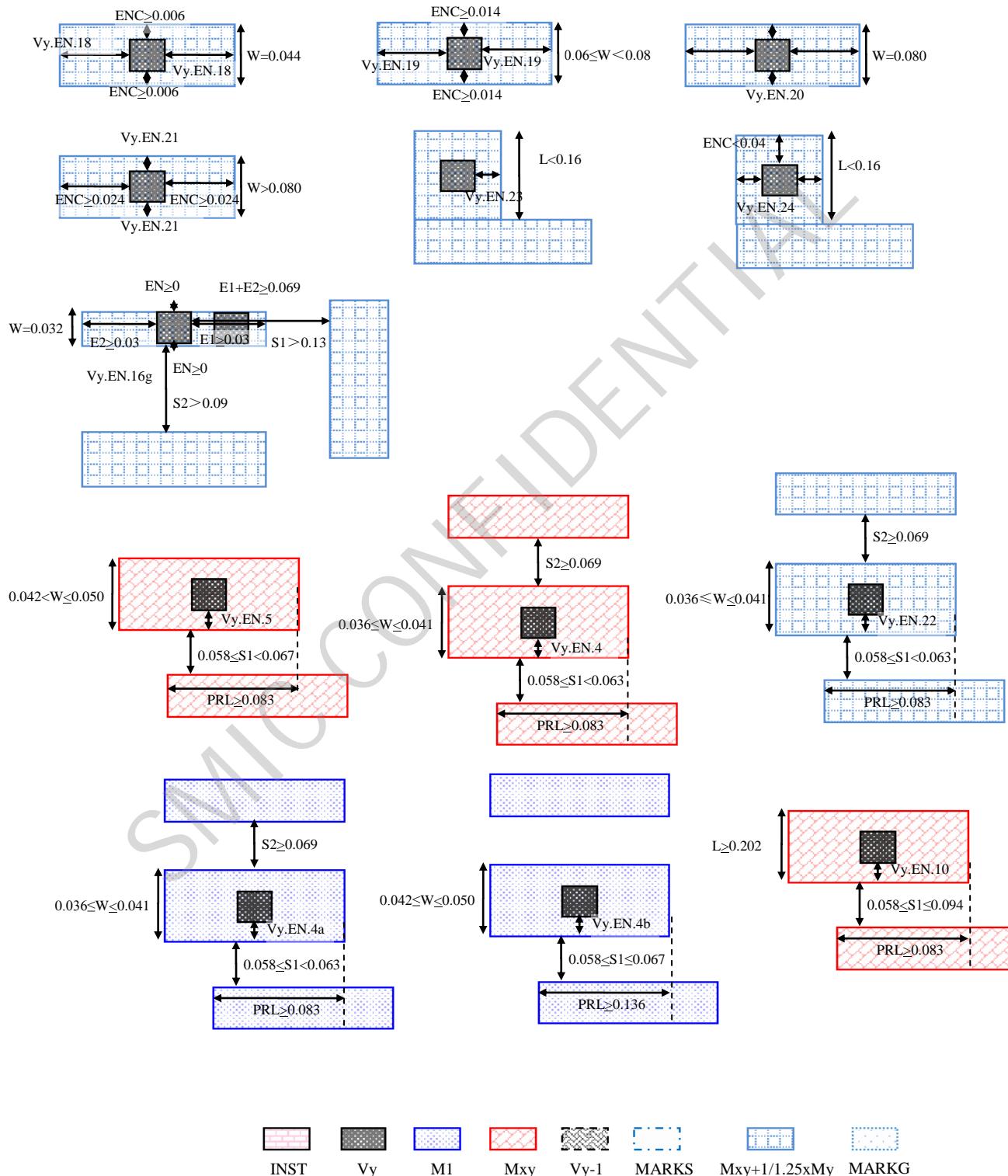
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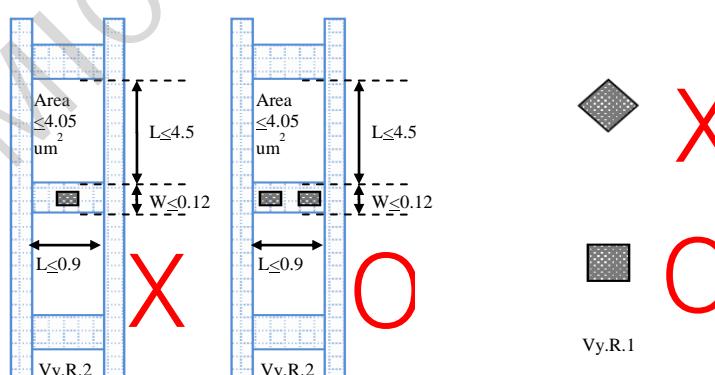
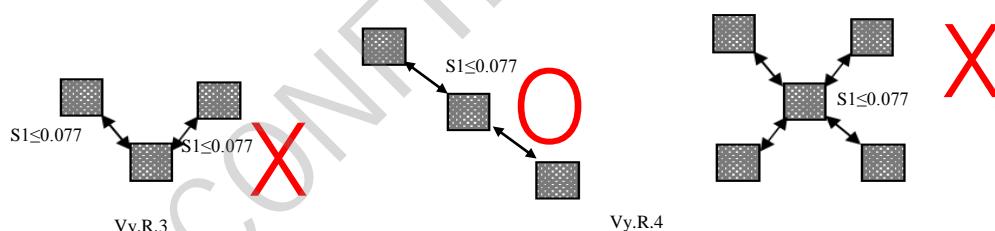
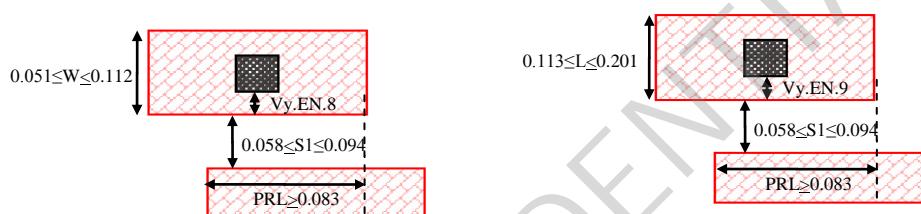
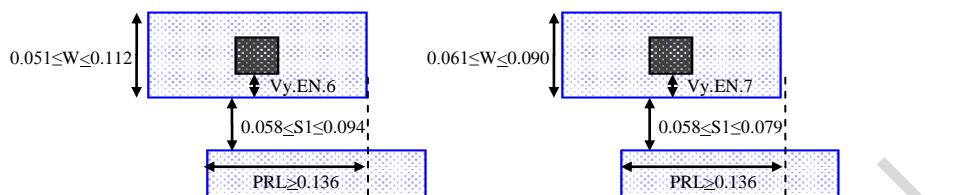


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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:2

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### 7.2.36.2 Rectangular Vy design rules

Rule number	Description	Opt.	Design Value	Unit
<b>RVy.W.1</b>	Rectangular Vy (RVy) width, except square Vy, MARKS, MARKG, INDMY, LOGO regions	=	0.032	um
<b>RVy.L.1</b>	Length of RVy (width = 0.032um)	=	0.08	um
<b>RVy.L.2</b>	Length of Vy bar (width = 0.1/0.45um)	≥	0.9	um
<b>RVy.S.1</b>	Space between RVy and (Vy-1 or RVy-1) (including V0 and RV0) at different net and PRL > 0um, when Mxy+1/1.25xMy enclosure of RVy > 0um.	≥	0.037	um
<b>RVy.S.1a</b>	Space between RVy	≥	0.082	um
<b>RVy.S.2</b>	Space between RVy and Mxy (including M1) at different net, when 1. Mxy (including M1) enclosure of RVy < 0.003um 2. Mxy+1/1.25xMy width > 0.038um	≥	0.037	um
<b>RVy.S.3</b>	Space between two RVy with PRL > -0.09um, and when 1. RVy enclosure by 1.25xMy < 0.01um at opposite side. 2. Space between RVy and 1.25xMy ≤ 0.052um with PRL ≥ -0.046um at opposite side. DRC doesn't flag space between RVy and 1.25xMy ≤ 0.052um with PRL ≥ -0.046um on both sides.	≥	0.099	um
<b>RVy.S.4</b>	Space between the short side of RVy and Vy when PRL > -0.032um	≥	0.108	um
<b>RVy.S.5</b>	Space between the long side of RVy (PRL > 0um, with one Mxy+1/1.25xMy in between)	≥	0.115	um
<b>RVy.EN.1</b>	RVy must be fully enclosed by M1/Mxy where M1/Mxy is the metal layer directly underneath RVy. Enclosure by M1/Mxy must follow either RVy.EN.2, RVy.EN.2a or RVy.EN.3			
<b>RVy.EN.2</b>	RVy enclosure by M1 or Mxy when enclosure on either perpendicular direction ≥ 0um	≥	0.024	um
<b>RVy.EN.2a</b>	RVy enclosure by M1 or Mxy for all sides	≥	0.015	um
<b>RVy.EN.3</b>	RVy enclosure by M1 or Mxy for two opposite sides with the other two sides ≥ 0.007um	≥	0.019	um

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Rule number	Description	Opt.	Design Value	Unit
<b>RVy.EN.4</b>	RVy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath RVy, when 1. Mxy width W: $0.036\text{um} \leq W \leq 0.041\text{um}$ 2. Space: $0.058\text{um} \leq S1 < 0.063\text{um}$ , PRL $\geq 0.083\text{um}$ . 3. The opposite space S2 $\geq 0.069\text{um}$	$\geq$	0.004	um
<b>RVy.EN.4a</b>	RVy enclosure by M1 in adjacent S1 side, where M1 is the metal layer directly underneath RVy, when 1. M1 width W: $0.036\text{um} \leq W \leq 0.041\text{um}$ 2. Space: $0.058\text{um} \leq S1 < 0.063\text{um}$ , PRL $\geq 0.083\text{um}$ 3. The opposite space S2 $\geq 0.069\text{um}$	$\geq$	0.004	um
<b>RVy.EN.4b</b>	RVy enclosure by M1 in adjacent S1 side, where M1 is the metal layer directly underneath RVy, when 1. M1 width W: $0.042\text{um} \leq W \leq 0.05\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.067\text{um}$ , PRL $\geq 0.136\text{um}$	$\geq$	0.004	um
<b>RVy.EN.5</b>	RVy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath RVy, when 1. Mxy width W: $0.042\text{um} \leq W \leq 0.05\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.067\text{um}$ , PRL $\geq 0.083\text{um}$	$\geq$	0.004	um
<b>RVy.EN.6</b>	RVy enclosure by M1 in adjacent S1 side, where M1 is the metal layer directly underneath RVy, when 1. M1 width W: $0.051\text{um} \leq W \leq 0.112\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.094\text{um}$ , PRL $\geq 0.136\text{um}$ DRC doesn't check RVy: a) Two RVys with space $\leq 0.1\text{um}$ in M1 and $1.25 \times \text{My/Mxy}$ intersection region. b) One Vy and one RVy with space $\leq 0.1\text{um}$ in M1 and $1.25 \times \text{My/Mxy}$ intersection region.	$\geq$	0.004	um
<b>RVy.EN.6a</b>	RVy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath RVy, when 1. Mxy width W: $0.051\text{um} \leq W \leq 0.112\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.094\text{um}$ , PRL $\geq 0.083\text{um}$ DRC doesn't check RVy: a) Two RVys with space $\leq 0.1\text{um}$ in M1 and $1.25 \times \text{My/Mxy}$	$\geq$	0.004	um

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Rule number	Description	Opt.	Design Value	Unit
	intersection region. b) One Vy and one RVy with space $\leq 0.1\text{um}$ in M1 and $1.25x\text{My}/\text{Mxy}$ intersection region.			
<b>RVy.EN.7</b>	RVy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath RVy, when 1. Mxy dimension along enclosure direction: $0.113\text{um} \leq L \leq 0.201\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.094\text{um}$ , PRL $\geq 0.083\text{um}$	$\geq$	0.004	um
<b>RVy.EN.8</b>	RVy enclosure by Mxy in adjacent S1 side, where Mxy is the metal layer directly underneath RVy, when 1. Mxy dimension along enclosure direction: $L \geq 0.202\text{um}$ 2. Space: $0.058\text{um} \leq S1 \leq 0.094\text{um}$ , PRL $\geq 0.083\text{um}$	$\geq$	0.014	um
<b>RVy.EN.9</b>	RVy must be fully enclosed by Mxy+1/1.25xMy where Mxy+1/1.25xMy is the metal layer directly above rectangular Vy. Enclosure by Mxy+1/1.25xMy must follow one of RVy.EN.9.1, RVy.EN.9.2, RVy.EN.9.3, RVy.EN.10, RVy.EN.10a, RVy.EN.10a1, RVy.EN.10a2, RVy.EN.10b or RVy.EN.11 or RVy.EN.12			
<b>RVy.EN.9.1</b>	RVy enclosure by Mxy+1 for all sides	$\geq$	0.015	um
<b>RVy.EN.9.2</b>	Enclosure of short side of RVy by Mxy+1 when enclosure by Mxy+1 on either perpendicular direction $\geq 0\text{um}$	$\geq$	0.024	um
<b>RVy.EN.9.3</b>	RVy enclosurere by Mxy+1 for two opposite sides with the other two sides $\geq 0.007\text{um}$	$\geq$	0.019	um
<b>RVy.EN.9.4</b>	RVy enclosure by Mxy+1 ( $0.036\text{um} \leq \text{Mxy+1 width} \leq 0.041\text{um}$ $0.058\text{um} \leq \text{space} < 0.063\text{um}$ and the opposite space $\geq 0.069\text{um}$ , PRL $\geq 0.083\text{um}$ )	$\geq$	0.004	um
<b>RVy.EN.10</b>	Enclosure of short side of RVy by 1.25xMy (width = $0.04\text{um}$ ) with the other two sides $\geq 0.004\text{um}$	$\geq$	0.038	um
<b>RVy.EN.10a1</b>	Enclosure of short side of RVy by 1.25xMy (width = $0.042\text{um}$ ) with the other two sides $\geq 0.005\text{um}$	$\geq$	0.038	um
<b>RVy.EN.10a</b>	Enclosure of short side of RVy by 1.25xMy (width = $0.044\text{um}$ ) with the other two sides $\geq 0.006\text{um}$	$\geq$	0.038	um
<b>RVy.EN.10a2</b>	Enclosure of short side of RVy by 1.25xMy (width = $0.046\text{um}$ )	$\geq$	0.038	um

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Rule number	Description	Opt.	Design Value	Unit
	with the other two sides $\geq 0.007\text{um}$			
<b>RVy.EN.10b</b>	Enclosure of short side of RVy by $1.25xMy$ ( $0.06\text{um} \leq \text{width} < 0.08\text{um}$ ) with the other two sides $\geq 0.014\text{um}$	$\geq$	0.038	um
<b>RVy.EN.11</b>	Enclosure of short side of RVy by $1.25xMy$ ( $\text{width} = 0.08\text{um}$ ) with the other two sides $\geq 0.024\text{um}$	$\geq$	0.019	um
<b>RVy.EN.12</b>	Enclosure of short side of RVy by $1.25xMy$ ( $\text{width} > 0.08\text{um}$ ) with the other two sides $\geq 0.03/0.024\text{um}$	$\geq$	0.019/0.029	um
<b>RVy.EN.13</b>	RVy enclosure by $1.25xMy$ edge (between two consecutive 90-270 degree corners, length $< 0.16\text{um}$ ), when $PRL > 0$	$\geq$	0.029	um
<b>RVy.EN.14</b>	RVy enclosure by $1.25xMy$ for two opposite sides ( $PRL > 0$ ) with the other side enclosure $< 0.04\text{ um}$ (corresponding edge length $< 0.16\text{ um}$ between two consecutive 90-270 degree corners)	$\geq$	0.040	um
<b>RVy.R.1</b>	Single RVy is not allowed in "H-shape" $M_{xy+1}/1.25x My$ , when: <ol style="list-style-type: none"><li>1. The <math>M_{xy+1}/1.25x My</math> has "H-shape" interacting with two metal holes: both two metal holes length <math>\leq 4.5\text{um}</math> and two metal hole area <math>\leq 4.05\text{um}^2</math></li><li>2. The Vy overlaps on the center metal bar of this "H-shape" <math>M_{xy+1}/1.25x My</math>.</li><li>3. The center metal bar length <math>\leq 0.9\text{um}</math> and the metal bar width <math>\leq 0.12\text{um}</math>.</li></ol>			
<b>RVy.R.2</b>	Redundant via requirement must be obeyed by one of following conditions of Vy numbers and space for $M_{xy}$ and $1.25xMy$ connection (One of $M_{xy}$ or $1.25xMy$ has width and length $\geq 0.162\text{um}$ ) (Except VIA bar) <ol style="list-style-type: none"><li>1. At least one rectangular Vy</li><li>2. At least two square Vy with space <math>\leq 0.091\text{um}</math></li><li>3. At least four square Vy with space <math>\leq 0.415\text{um}</math></li></ol>			
<b>RVy.R.3</b>	Redundant via requirement must be obeyed by one of following conditions of Vy numbers and space for $M_{xy}$ and $1.25xMy$ connection (One of $M_{xy}$ or $1.25xMy$ has width and length $\geq 0.272\text{um}$ , two square vias are equal to one rectangular via for below conditions) (Except VIA bar, MARKS and OCCD region): <ol style="list-style-type: none"><li>1. At least four square Vy with space <math>\leq 0.091\text{um}</math></li></ol>			

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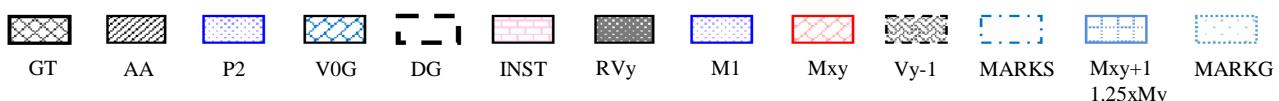
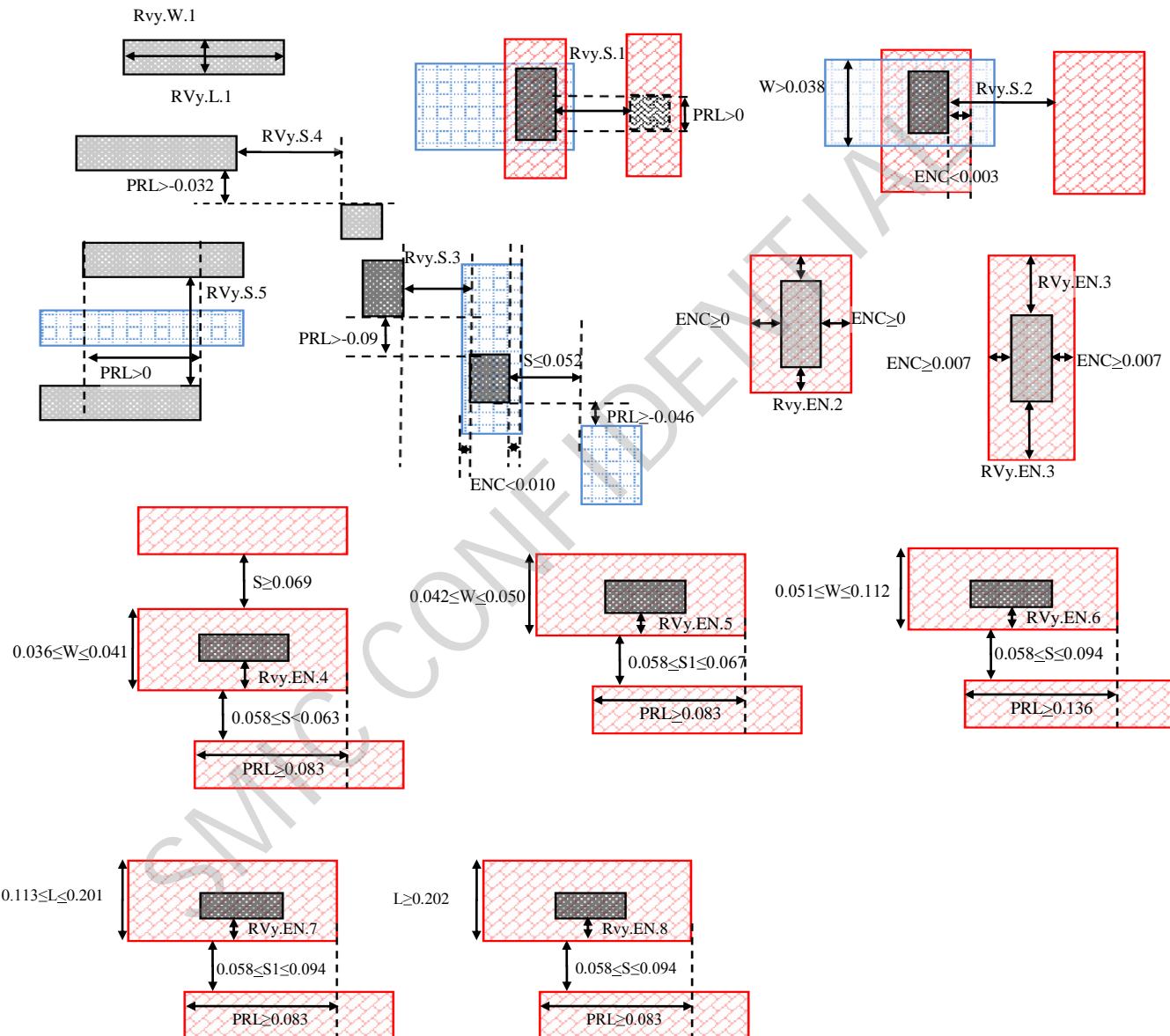


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Rule number	Description	Opt.	Design Value	Unit
	2. At least nine square Vy with space $\leq 0.545\mu m$ 3. At least two rectangular Vy with space $\leq 0.202\mu m$ 4. At least five rectangular Vy with space $\leq 0.545\mu m$			
<b>RVy.R.4</b>	There should be at least two square Vy or one rectangular Vy in the intersection area of bottom metal and upper metal, when either wide metal $M_{xy}$ or $1.25 \times M_y$ length $\geq 0.162\mu m$ and width $\geq 0.162\mu m$ , the space between either via and wide metal is $\leq 0.5\mu m$ ( $S$ , $S$ is the shortest running path length from Via to the wide metal). (except via bar).			
<b>RVy.R.5</b>	There should be at least two square Vy or one rectangular Vy in the intersection area of bottom metal and upper metal, when either wide metal $M_{xy}$ or $1.25 \times M_y$ length $\geq 0.272\mu m$ and width $\geq 0.272\mu m$ , the space between either via and wide metal is $\leq 1\mu m$ ( $S$ , $S$ is the shortest running path length from Via to the wide metal). (except via bar).			
<b>RVy.R.6</b>	There should be at least two square Vy or one rectangular Vy in the intersection area of bottom metal and upper metal, when either wide metal $M_{xy}$ or $1.25 \times M_y$ width and length $\geq 0.542\mu m$ , the space between either via and wide metal is $\leq 3\mu m$ ( $S$ , $S$ is the shortest running path length from Via to the wide metal). (except via bar).			
<b>RVy.R.7</b>	There should be at least two square Vy or one rectangular Vy in the intersection area of bottom metal and upper metal, when either wide metal $M_{xy}$ or $1.25 \times M_y$ width and length $\geq 1.01\mu m$ , the space between either via and wide metal is $\leq 5\mu m$ ( $S$ , $S$ is the shortest running path length from Via to the wide metal). (except via bar).			
<b>RVy.R.8</b>	Maximum delta V $\geq 5.6V$ is not allowed, when space between Vy and RVy is $< 0.410\mu m$			

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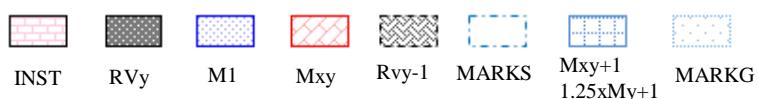
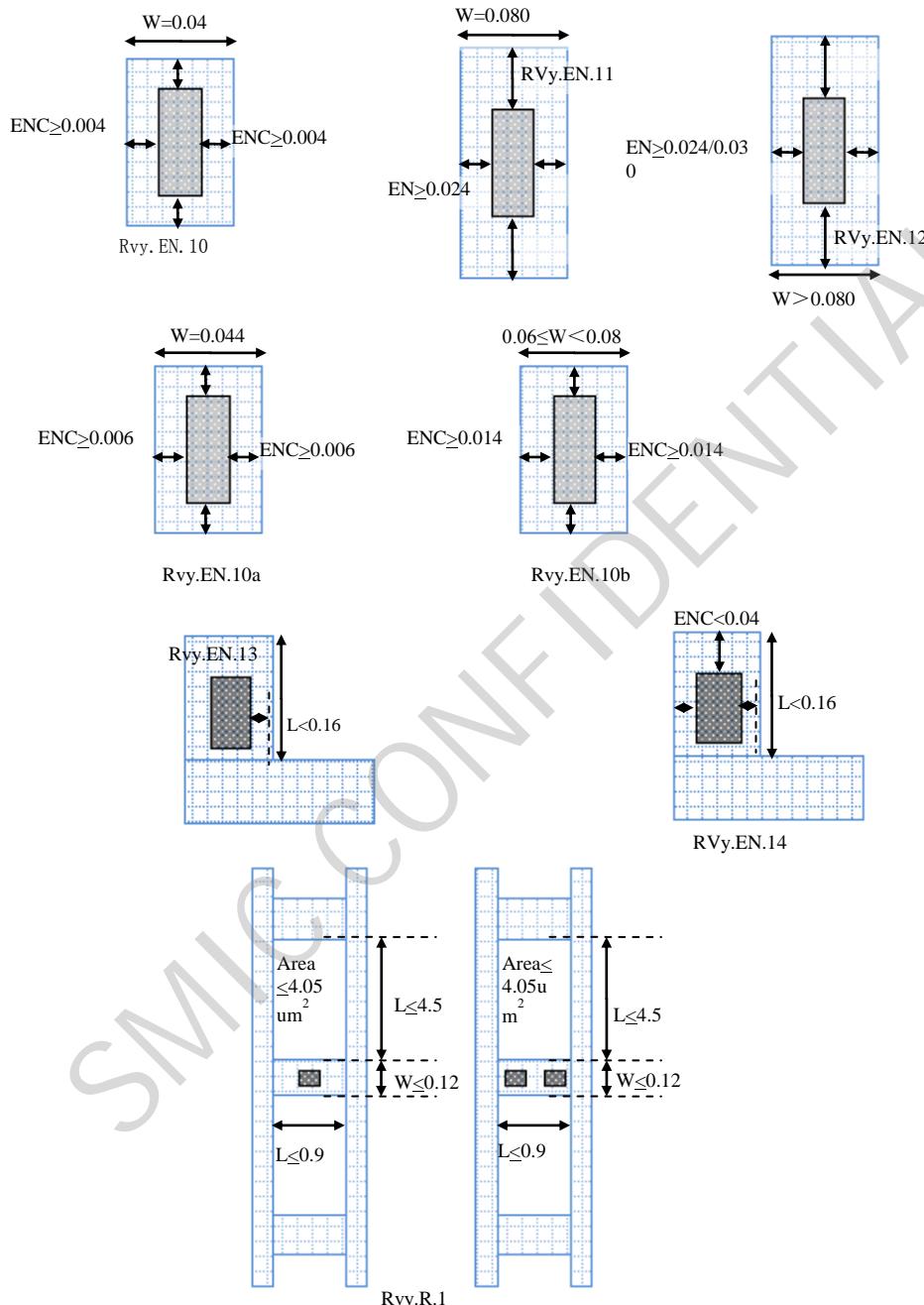


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### 7.2.37 Mxy design rules

Rule number	Description	Opt.	Design Value	Unit
<b>Mxy.W.1</b>	Mxy width	$\geq$	0.032	um
<b>Mxy.W.2</b>	Mxy width, except MARKS, and LOGO regions	$\leq$	2.1	um
<b>Mxy.W.3</b>	Metal branch width when connected to wide metal with both width and length $\geq 0.27\text{um}$	$\geq$	0.065	um
<b>Mxy.W.4</b>	Mxy branch width when connected to wide Mxy (width $> 2\text{um}$ ) which enclosed inner hole ((Mxy OR Mxy-hole) area $\geq 3050\text{um}^2$ ). DRC checks the Mxy interact (((Mxy OR Mxy-hole) sd 1um) su 1um) su 1um).	$\geq$	0.037	um
<b>Mxy.W.5</b>	Width of 45-degree bent Mxy	$\geq$	0.152	um
<b>Mxy.S.1</b>	Space between two Mxy, except LOGO region	$\geq$	0.032	um
<b>Mxy.S.2</b>	Space between Mxy when one or both Mxy width $\geq 0.071\text{um}$ and the PRL $\geq 0.14\text{um}$	$=$	0.041~0.062, $\geq 0.072$	um
<b>Mxy.S.3</b>	Space between Mxy when one or both width $\geq 0.09\text{um}$ and PRL $\geq 0.14\text{um}$	$=$	0.041~0.062, $\geq 0.081$	um
<b>Mxy.S.4</b>	Space between Mxy when one or both width $\geq 0.114\text{um}$ and PRL $\geq 0.14\text{um}$ , except LOGO region	$=$	0.041~0.062, $\geq 0.106$	um
<b>Mxy.S.5</b>	Space between Mxy when one or both width $\geq 0.181\text{um}$ and PRL $\geq 0.19\text{um}$	$\geq$	0.125	um
<b>Mxy.S.6</b>	Space between Mxy when one or both width $\geq 0.272\text{um}$ and PRL $\geq 0.288\text{um}$	$\geq$	0.143	um
<b>Mxy.S.7</b>	Space between Mxy when one or both width $\geq 0.542\text{um}$ , except LOGO region	$\geq$	0.188	um
<b>Mxy.S.8</b>	Space between Mxy when one or both width $\geq 1.352\text{um}$ , except LOGO region	$\geq$	0.304	um
<b>Mxy.S.9</b>	Space between Mxy line and line-end ( $W \leq 0.051\text{um}$ ) when PRL $\geq -0.021\text{um}$	$\geq$	0.049	um
<b>Mxy.S.10</b>	Space between Mxy line-end ( $0.032\text{um} \leq \text{width} \leq 0.051\text{um}$ ) and line-end ( $0.032\text{um} \leq \text{width} \leq 0.047\text{um}$ ) when PRL $\geq -0.021\text{um}$	$\geq$	0.058	um

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Rule number	Description	Opt.	Design Value	Unit
Mxy.S.11	Space between Mxy line-end ( $0.032\text{um} \leq \text{width} \leq 0.051\text{um}$ ) and line-end ( $0.048\text{um} \leq \text{width} \leq 0.051\text{um}$ ) when $\text{PRL} \geq -0.021\text{um}$	$\geq$	0.055	um
Mxy.S.12	Space between Mxy and dense Mxy line-end ( $0.032\text{um} \leq W \leq 0.047\text{um}$ ), when $\text{PRL} > -0.022\text{um}$ . Dense Mxy line end definition: $(W+S1) < 0.09\text{um}$ , other metal must be in the region R, T and D is the extension from metal line end, $T \leq 0.021\text{um}$ , $D \leq 0.051\text{um}$ , S1 should be the space between separate metal. (Except small jog with edge length $\leq 0.031\text{um}$ )	$\geq$	0.07	um
Mxy.S.13	Space between Mxy and dense Mxy line-end ( $0.048\text{um} \leq W \leq 0.051\text{um}$ ), when $\text{PRL} > -0.022\text{um}$ . Dense Mxy line end definition: $(W+S1) < 0.09\text{um}$ , other metal must be in the region R, T and D is the extension from metal line end, $T \leq 0.021\text{um}$ , $D \leq 0.051\text{um}$ , S1 should be the space between separate metal. (Except small jog with edge length $\leq 0.031\text{um}$ )	$\geq$	0.056	um
Mxy.S.14	Mxy line-end space in metal array. Metal array definition: 1. Mxy width (W): $0.046\text{um} \leq W \leq 0.054\text{um}$ 2. Mxy length (L) $\geq 0.134\text{um}$ 3. Searching distance (D) of Mxy line-end edge: $0.048\text{um}$ 4. Mxy space (S1) $0.058\text{um} \leq S1 \leq 0.076\text{um}$ for both long sides 5. Mxy PRL $> 0\text{um}$ for short side (L1) 6. Line end space (S2) of both neighboring Mxy: $0.058\text{um} \leq S2 \leq 0.076\text{um}$ with $\text{PRL} > 0\text{um}$ DRC doesn't flag at least one $S1 \geq 0.058 \sim \leq 0.063\text{um}$ with $\text{PRL} > 0.112\text{um}$ . And DRC flags forbidden space that has $\text{PRL} > 0\text{um}$ with both S2	$\geq$	0.072	um
Mxy.S.15	Space between two Mxy when one or both Mxy enclosure of long side edge of RVy-1 is $< 0.007\text{um}$ , Mxy is the metal layer directly above RVy-1 DRC flag the space between Mxy and the long sides of RVy-1.	$\geq$	0.035	um
Mxy.S.16	Space between two Mxy when one or both Mxy enclosure of long side edge of RVy-1 are $< 0.003\text{um}$ , Mxy is the metal layer	$\geq$	0.044	um

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Rule number	Description	Opt.	Design Value	Unit
	directly above RVy-1 DRC flag the space between Mxy and the long sides of RVy-1.			
<b>Mxy.S.17</b>	Space between Mxy and 45-degree bent Mxy, DRC check 45-degree direction	$\geq$	0.152	um
<b>Mxy.S.18</b>	Space between Mxy and INST, space = 0 is allowed	$\geq$	0.08	um
<b>Mxy.S.20</b>	Space between Mxy and Vy-1 or Vy where Mxy is the metal layer directly above Vy-1 and underneath Vy (Maximum delta V > 1.05V, 0.95V+10%)	$\geq$	0.042	um
<b>Mxy.S.21</b>	Space between Mxy and Vy-1 or Vy where Mxy is the metal layer directly above Vy-1 and underneath Vy (Maximum delta V > 1.155V, 1.05V+10%)	$\geq$	0.045	um
<b>Mxy.S.22</b>	Space between Mxy and Vy-1 or Vy where Mxy is the metal layer directly above Vy-1 and underneath Vy (Maximum delta V > 1.32V, 1.2V+10%)	$\geq$	0.053	um
<b>Mxy.S.23</b>	Space between Mxy and Vy-1 or Vy where Mxy is the metal layer directly above Vy-1 and underneath Vy (Maximum delta V > 1.65V, 1.5V+10%)	$\geq$	0.059	um
<b>Mxy.S.24</b>	Space between Mxy and Vy-1 or Vy where Mxy is the metal layer directly above Vy-1 and underneath Vy (Maximum delta V > 1.98V, 1.8V+10%)	$\geq$	0.071	um
<b>Mxy.S.25</b>	Space between Mxy and Vy-1 or Vy where Mxy is the metal layer directly above Vy-1 and underneath Vy (Maximum delta V > 2.75V, 2.5V+10%)	$\geq$	0.077	um
<b>Mxy.S.26</b>	Space between Mxy and Vy-1 or Vy where Mxy is the metal layer directly above Vy-1 and underneath Vy (Maximum delta V > 3.63V, 3.3V+10%)	$\geq$	0.159	um
<b>Mxy.S.27</b>	Space between Mxy (maximum delta V > 1.05V, 0.95V+10%), except M2 interact MTFUSE	$\geq$	0.04	um
<b>Mxy.S.28</b>	Space between Mxy (maximum delta V > 1.155V, 1.05V+10%), except M2 interact MTFUSE	$\geq$	0.042	um
<b>Mxy.S.29</b>	Space between Mxy (maximum delta V > 1.32V, 1.2V+10%) except M2 interact MTFUSE	$\geq$	0.045	um
<b>Mxy.S.30</b>	Space between Mxy (maximum delta V > 1.65V, 1.5V+10%),	$\geq$	0.05	um

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Rule number	Description	Opt.	Design Value	Unit
	except M2 interact MTFUSE			
<b>Mxy.S.31</b>	Space between Mxy (maximum delta V > 2.75V, 2.5V+10%)	$\geq$	0.068	um
<b>Mxy.S.32</b>	Space between Mxy (maximum delta V > 3.63V, 3.3V+10%)	$\geq$	0.135	um
<b>Mxy.L.1</b>	Mxy edge length with adjacent edge < 0.032um (these two edges formed by three consecutive 270-90-270 degree corner) DRC doesn't flag if there is Mxy in the region which is formed by 0.125um extension from these two edges and the 90-degree outer vertex.	$\geq$	0.064	um
<b>Mxy.L.2</b>	Mxy edge length with adjacent edge < 0.032um (these two edges formed by three consecutive 90-270-90 degree corners), except EFUSE region	$\geq$	0.064	um
<b>Mxy.L.3</b>	Mxy branch length when Mxy branch width $\leq$ 0.269um, and connected to wide metal with both width and length $\geq$ 0.27um DRC waive if the branch region can fill at least one (0.005um* design value) rectangle.	$\geq$	0.139	um
<b>Mxy.L.4</b>	Mxy branch length when Mxy branch width $\leq$ 0.269um, and connected to wide metal with both width and length $\geq$ 0.542um DRC waive if the branch region can fill at least one (0.005um* design value) rectangle.	$\geq$	0.248	um
<b>Mxy.L.5</b>	Length of Mxy branch when Mxy branch width $\leq$ 0.269um, and connected to wide metal with both width and length $\geq$ 1um DRC waive if the branch region can fill at least one (0.005um* design value) rectangle.	$\geq$	0.495	um
<b>Mxy.L.6</b>	Length of 45-degree bent metal, except MARKS region	$\geq$	0.44	um
<b>Mxy.D.1</b>	Mxy density (window 50um*50um, stepping 25um), except the window ( $15\% \leq$ metal density $<$ 25%) not interact 3um*3um empty area, except OCOVL region, (NODMF su 1um)	$\geq$	25%	
<b>Mxy.D.2</b>	Mxy maximum density (window 50um*50um, stepping 25um), except dummy metal	$\leq$	65%	
<b>Mxy.D.3</b>	Mxy maximum density (window 50um*50um, stepping 25um)	$\leq$	75%	
<b>Mxy.D.4</b>	Mxy density difference between any two neighboring checking	$\leq$	40%	

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Rule number	Description	Opt.	Design Value	Unit
	windows (window 180 um*180um, stepping 90um)			
Mxy.D.6	<p>It is not allowed to have local density of all three consecutive metal (Mxy, Mxy+1, Mxy+2) over any 30um*30um (stepping 15um), except NODMF su 0.4um region.</p> <p>The metal layers of Mxy+1 and Mxy+2 include Mxy, 1.25xMy, 1.25xMn, and relevant dummy metals.</p>	$\leq$	5%	
Mxy.D.7	Mxy density ratio of ((Mxy or dummy Mxy) INTERACT ((MxyDPMK OR MxyCA) OR MxyCB)) to (Mxy or dummy Mxy) in window 72um*72um, step size: 36um, except OCOVL region	$\leq$	30%	
Mxy.D.8	Mxy density difference of ABS (((Mxy OR MxyDUM OR MxyDOP) - (MxyDP OR MxyDPDUM OR MxyDPDOP)) / ((Mxy OR MxyDUM OR MxyDOP) + (MxyDP OR MxyDPDUM OR MxyDPDOP))) This rule is applied post Mxy layout decomposition	$\leq$	10%	
Mxy.A.1	M2 area	$\geq$	0.0061	um <sup>2</sup>
Mxy.A.2	M3 area	$\geq$	0.0072	um <sup>2</sup>
Mxy.A.3	<p>M2 Area (with all of edge length &lt; 0.204um, any edge length <math>\geq</math> 0.117um)</p> <p>Except:</p> <p>1.The patterns filling 0.046um*0.117um rectangular pattern</p> <p>2.M2 edge of length <math>\geq</math> 0.046um if this edge have another adjacent edge of length &lt; 1.0 *minimum width</p>	$\geq$	0.0072	um <sup>2</sup>
Mxy.A.4	Mxy area (with all of edge lengths < 0.082um) (Except a pattern filling 0.078um*0.078um rectangular pattern)	$\geq$	0.0178	um <sup>2</sup>
Mxy.A.5	Mxy enclosed area	$\geq$	0.161	um <sup>2</sup>
Mxy.R.1	<p>Mxy forbidden space (Mxy width <math>\geq</math> 0.15um and PRL &gt; 0.135um), except Mxy jog width <math>\leq</math> 0.135um</p> <p>DRC searching range is from 0.106um to 0.729um.</p> <p>DRC flags the forbidden space that totally inside the searching range along the space direction, and the PRL between forbidden space and the wide metal is &gt; 0.135um.</p>	=	0.058~0.062	um
Mxy.R.2	Mxy forbidden space for single mask when Mxy width < 0.037um and PRL with neighboring Mxy (W2) > 0.117um, for M2	=	0.141~0.175	um

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Rule number	Description	Opt.	Design Value	Unit
	DRC flags edge of ((W1+S1+W2+S2) or (S1+W2+S2+W3)) = 0.141~0.175um. DRC waive when: (1) A/B or B/C are same polygons (2) A/C in different masks DRC flags edge of forbidden zone.			
Mxy.R.3	Mxy forbidden space for single mask when Mxy width < 0.037um, except M2. DRC flags edge of ((W1+S1+W2+S2) or (S1+W2+S2+W3)) = 0.141~0.175um. DRC waive when: (1) A/B or B/C are same polygons (2) A/C in different masks DRC flags edge of forbidden zone.	=	0.141~0.175	um
Mxy.R.4	Mxy overlap of MTFUSE is not allowed.			
Mxy.R.5	Maximum delta V $\geq$ 5.6V is not allowed, when space between Mxy and Mxy/above via/bottom via < 0.360um			
Mxy.R.6 <sup>[NC]</sup>	Mxy pattern must be drawn on data type 0.			
Mxy.R.7	U-shape metal pitch (W+S1) or (W+S2) must be $\geq$ 0.072um and Vy enclosure by Mxy line-end (E) must be $\geq$ 0.032um, (Mxy is the metal underneath Vy, except M2 in INST region) when : (1) Both PRL1 and PRL2 $\geq$ -0.015um; (2) Space (S) < 0.070um along length direction. (3) W < 0.046um. DRC waive if S1 or S2 > 0.04um			
Mxy.R.8	U-shape metal pitch (W+S1) or (W+S2) must be $\geq$ 0.072um except M2 in INST region, when: (1) Both PRL1 and PRL2 $\geq$ -0.015um; (2) Space (S) < 0.070um along length direction. (3) W < 0.046um. (4) Mxy interact Vy-1 and enclosure E < 0.05um.(Mxy is the metal above Vy-1) DRC waive if S1 or S2 > 0.04um			
Mxy.RSP.1	Space between metal space segments with S2 < 0.072 and L2 $\leq$ 0.082um. Metal space segments definition: 1) At least one metal line width > 0.07um (W1) and PRL >	$\geq$	0.298	um

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Rule number	Description	Opt.	Design Value	Unit
	0.27um (L1) in metal space < 0.09um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.07um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
Mxy.RSP.2a	Width (S2) of metal space segments with L2 > 0.082um (0.063 ≤ S < 0.072 is forbidden) Metal space segments definition: 1) At least one metal line width > 0.07um (W1) and PRL > 0.27um (L1) in metal space < 0.09um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.07um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.041	um
Mxy.RSP.2b	Width (S2) of metal space segments with L2 ≤ 0.082um Metal space segments definition: 1) At least one metal line width > 0.07um (W1) and PRL > 0.27um (L1) in metal space < 0.09um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.070um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.032	um
Mxy.RSP.3	Space between metal space segments with S2 < 0.081 and L2 ≤ 0.082um. Metal space segments definition: 1) At least one metal line width > 0.088um (W1) and PRL > 0.27um (L1) in metal space < 0.108um (S1) region;	≥	0.298	um

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Rule number	Description	Opt.	Design Value	Unit
	2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.088um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
Mxy.RSP.4a	Width (S2) of metal space segments with L2 > 0.082um (0.063um ≤ S < 0.081um is forbidden) Metal space segments definition: 1) At least one metal line width > 0.088um (W1) and PRL > 0.27um (L1) in metal space < 0.108um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.088um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.041	um
Mxy.RSP.4b	Width (S2) of metal space segments with L2 ≤ 0.082um (0.063um ≤ S < 0.072um is forbidden) Metal space segments definition: 1) At least one metal line width > 0.088um (W1) and PRL > 0.270um (L1) in metal space < 0.108um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.088um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.041	um
Mxy.RSP.5	Space between metal space segments with S2 < 0.106um and L2 ≤ 0.082um. Metal space segments definition: 1) At least one metal line width > 0.112um (W1) and PRL > 0.270um (L1) in metal space < 0.126um (S1) region;	≥	0.298	um

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Rule number	Description	Opt.	Design Value	Unit
	2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.112um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
Mxy.RSP.6a	Width (S2) of metal space segments with L2 > 0.082um (0.063um ≤ S < 0.106um is forbidden) Metal space segments definition: 1) At least one metal line width > 0.112um (W1) and PRL > 0.27um (L1) in metal space < 0.126um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.112um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.041	um
Mxy.RSP.6b	Width (S2) of metal space segments with L2 ≤ 0.082um (0.063um ≤ S < 0.081um is forbidden) Metal space segments definition: 1) At least one metal line width > 0.112um (W1) and PRL > 0.27um (L1) in metal space < 0.126um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.112um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.041	um
Mxy.RSP.7	Space between metal space segments with S2 < 0.126 and L2 ≤ 0.082um. Metal space segments definition: 1) At least one metal line width > 0.180um (W1) and PRL > 0.27um (L1) in metal space < 0.144um (S1) region;	≥	0.298	um

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Rule number	Description	Opt.	Design Value	Unit
	2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.18um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
Mxy.RSP.8a	Width (S2) of metal space segments with L2 > 0.082um Metal space segments definition: 1) At least one metal line width > 0.18um (W1) and PRL > 0.27um (L1) in metal space < 0.144um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.18um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.125	um
Mxy.RSP.8b	Width (S2) of metal space segments with L2 ≤ 0.082um Metal space segments definition: 1) At least one metal line width > 0.18um (W1) and PRL > 0.27um (L1) in metal space < 0.144um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.18um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.107	um
Mxy.RSP.9	Space between metal space segments with S2 < 0.144 and L2 ≤ 0.082um. Metal space segments definition: 1) At least one metal line width > 0.27um (W1) and PRL > 0.27um (L1) in metal space < 0.261um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1	≥	0.298	um

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Rule number	Description	Opt.	Design Value	Unit
	direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.27um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.			
Mxy.RSP.10a	Width (S2) of metal space segments with L2 > 0.082um Metal space segments definition: 1) At least one metal line width > 0.27um (W1) and PRL > 0.27um (L1) in metal space < 0.261um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.27um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.142	um
Mxy.RSP.10b	Width (S2) of metal space segments with L2 ≤ 0.082um Metal space segments definition: 1) At least one metal line width > 0.27um (W1) and PRL > 0.27um (L1) in metal space < 0.261um (S1) region; 2) Metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3) Metal space segments at least abut one metal with width > 0.27um (W1); 4) L2 is the width of metal space segments which is parallel with L1 direction; 5) S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.125	um
Mxy.OR.0 <sup>[NC]</sup>	Odd ring conflict space definition: OR Line Space (ORLS): polygons violate any one of the odd ring space rules from Mxy.ORCS.1 and Mxy.ORCS.2 OR Corner Space (ORCS): polygons violate any one of the odd ring space rule Mxy.ORCS.3 OR-AREA definition: 1. Odd ring line area (ORLA): The projection area between two edges with ORLS 2. Odd ring corner area (ORCA): The line between two corners			

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Rule number	Description	Opt.	Design Value	Unit
	with ORCS 3. ORLA or ORCA region are independent to all other ones, even if they are overlapped or crossed Loop: 1. A loop is formed when polygons of Mxy are connected in a cycle sequence with OR-AREA in between 2. A loop cannot contain any sub-loops which share one or more polygons with it Path: A path is formed when polygons of Mxy are connected one by one from one marker to another marker with OR-AREA in between			
<b>Mxy.OR.1</b>	OR-AREA formed by single polygon is not allowed.			
<b>Mxy.OR.2</b>	ORCA cross another ORCA or touch ORLA is not allowed.			
<b>Mxy.OR.3</b>	OR-AREA count of the close loop formed by original polygons and OR-AREA cannot be odd number.			
<b>Mxy.OR.4</b>	MxyDPMK must be drawn identically to Mxy.			
<b>Mxy.OR.5</b>	(Mxy INTERACT MxyDPMK) INTERACT ORLS or ORCS is not allowed.			
<b>Mxy.OR.6</b>	(Mxy INTERACT INST) INTERACT MxyDPMK is not allowed.			
<b>Mxy.OR.7</b>	Pre-coloring marker MxyCA and MxyCB must be drawn identically to Mxy.			
<b>Mxy.OR.8</b>	MxyCA INTERACT MxyCB is not allowed.			
<b>Mxy.OR.9</b>	(Mxy INTERACT INST) INTERACT (MxyCA OR MxyCB) is not allowed.			
<b>Mxy.OR.10</b>	(MxyCA OR MxyCB) INTERACT MxyDPMK is not allowed.			
<b>Mxy.OR.11</b>	OR-AREA count of any path starting from MxyCA and ending at MxyCA must not be an odd number.			
<b>Mxy.OR.12</b>	OR-AREA count of any path starting from MxyCB and ending at MxyCB must not be an odd number.			
<b>Mxy.OR.13</b>	OR-AREA count of any path starting from MxyCA and ending at MxyCB must not be an even number.			

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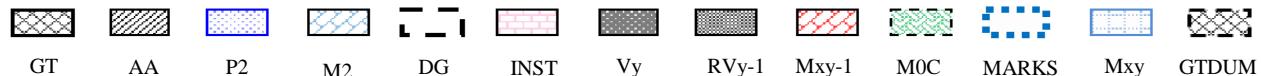
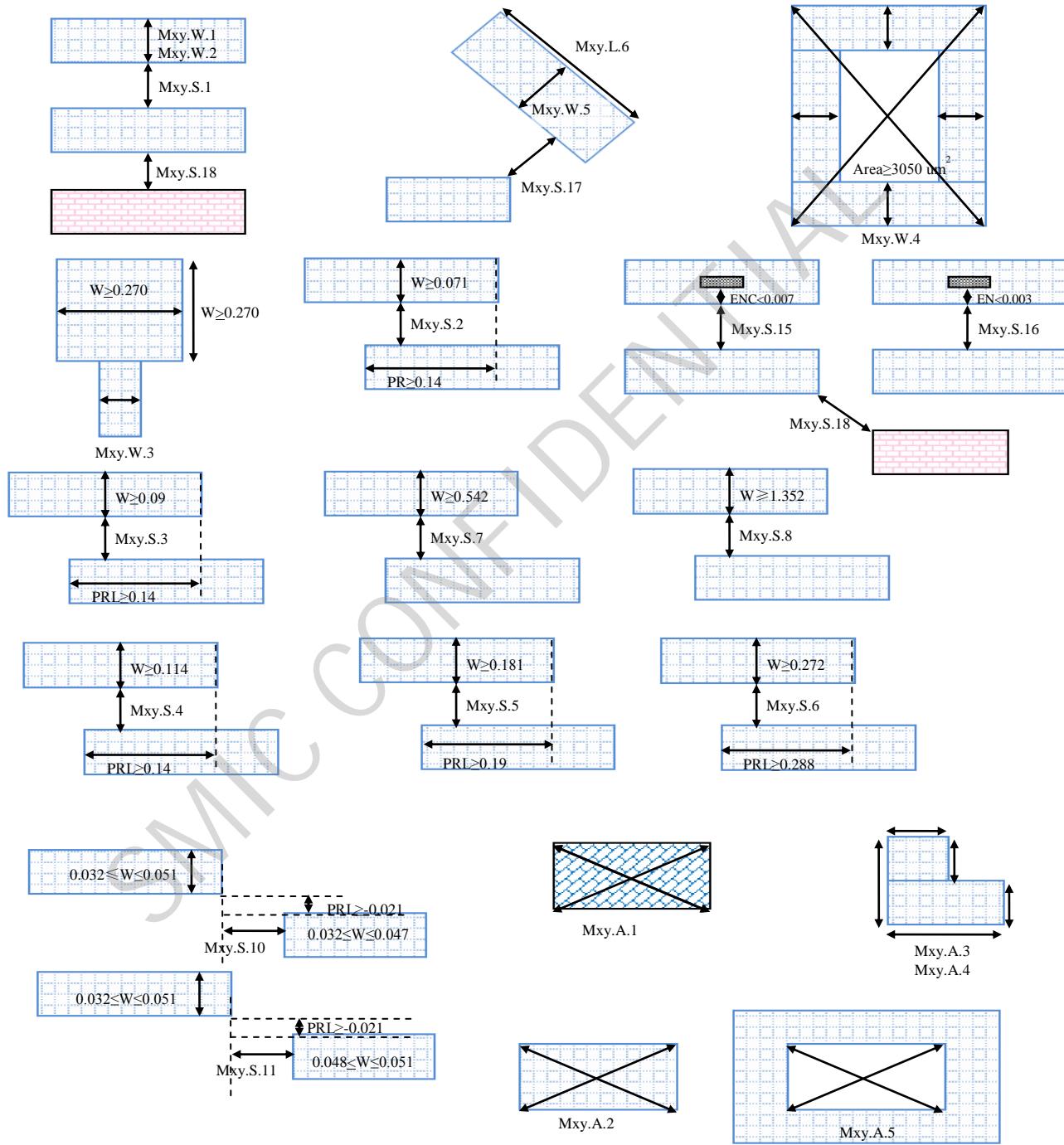
Rule number	Description	Opt.	Design Value	Unit
<b>Mxy.OR.14</b>	Maximum pre-coloring ratio of ((MxyCA + MxyCB + MxyDPMK)/Mxy) before decomposition	<	16%	
<b>Mxy.ORCS.1</b>	Space between Mxy to Mxy when PRL > -0.015um	$\geq$	0.063	um
<b>Mxy.ORCS.2</b>	Space between Mxy line-end (width < 0.046um) and Mxy when PRL > -0.015um	$\geq$	0.08	um
<b>Mxy.ORCS.3</b>	Corner space between Mxy when PRL $\leq$ -0.015um region	$\geq$	0.058	um

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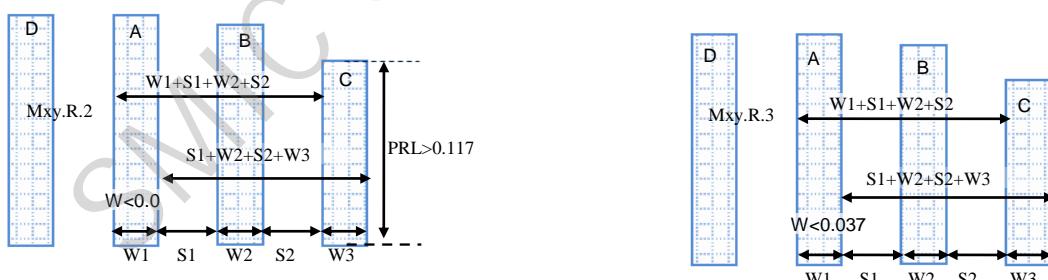
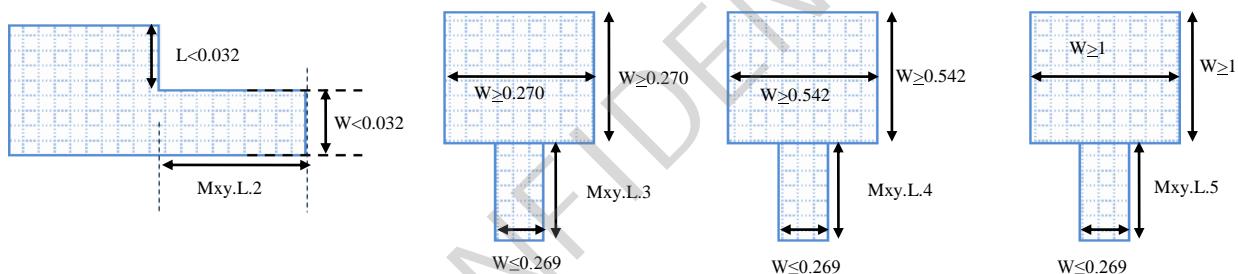
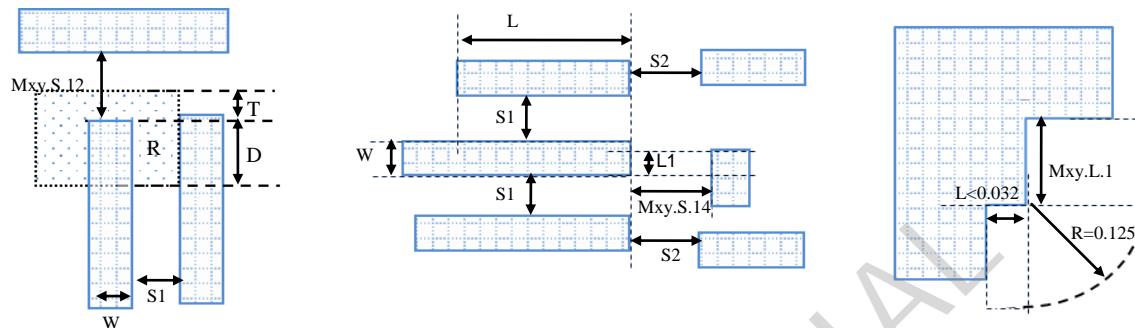


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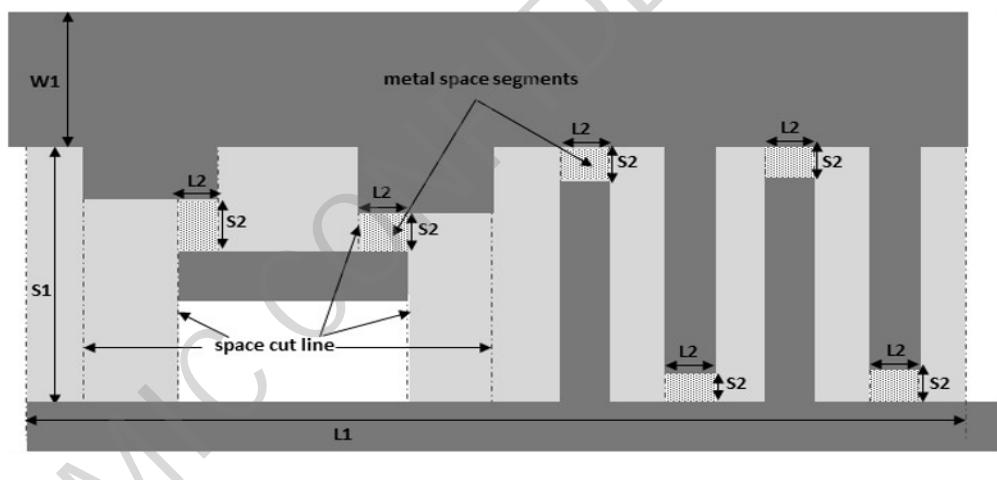
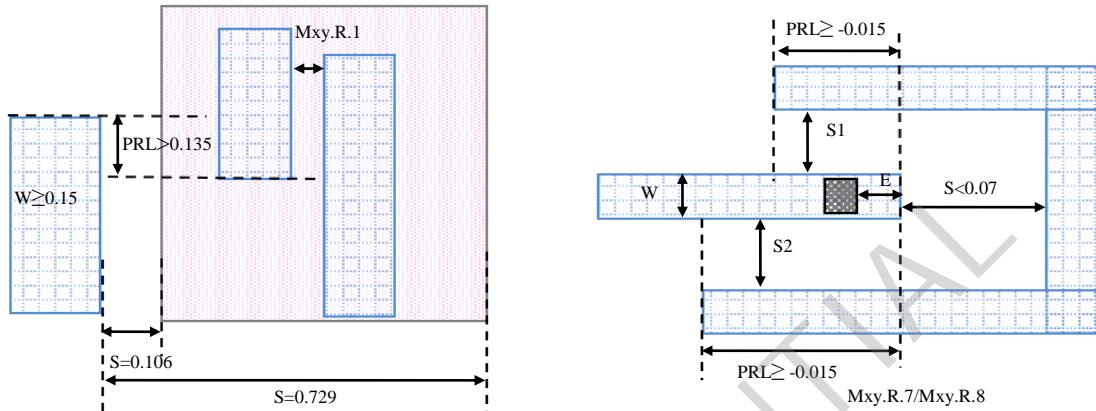
$V_y$      
  $M_{xy}$

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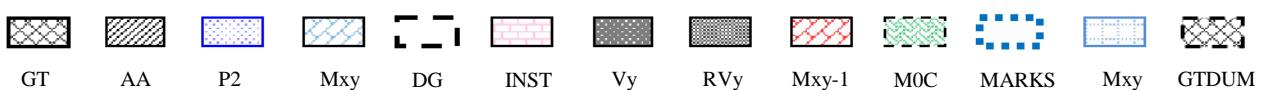
According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:2

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Mxy.R.4



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### 7.2.38 1.25xMy design rules

Rule number	Description	Opt.	Design Value	Unit
<b>1.25xMy.W.1</b>	1.25xMy width	$\geq$	0.04	um
<b>1.25xMy.W.1a</b>	1.25xMy width in CP direction  The width should be even value when $\leq 0.046\text{um}$ CP direction definition: Critical-Pitch direction along the minimum pitch (80nm) of 1.25xMy	$=$	0.04~0.046, $\geq 0.06$	um
<b>1.25xMy.W.1b</b>	1.25xMy width in NCP direction  NCP direction definition: Non-Critical-Pitch direction perpendicular to CP direction	$=$	0.08, $\geq 0.12$	um
<b>1.25xMy.W.2</b>	Maximum 1.25xMy width, except MARKS and LOGO regions	$\leq$	2.1	um
<b>1.25xMy.W.3</b>	Width of 45-degree bent 1.25xMy	$\geq$	0.396	um
<b>1.25xMy.W.4</b>	1.25xMy branch width when connected to wide metal with both width and length $\geq 0.401\text{um}$	$\geq$	0.08	um
<b>1.25xMy.W.5</b>	1.25xMy width when PRL < 0	$\geq$	0.08	um
<b>1.25xMy.S.1</b>	1.25xMy space	$\geq$	0.04	um
<b>1.25xMy.S.2</b>	Space between 1.25xMy when one or both 1.25xMy width $\geq 0.201\text{um}$ when PRL $\geq -0.139\text{um}$	$\geq$	0.139	um
<b>1.25xMy.S.3</b>	Space between 1.25xMy when one or both 1.25xMy width $\geq 0.282\text{um}$ when PRL $> 0.16\text{um}$	$\geq$	0.199	um
<b>1.25xMy.S.4</b>	Space between 1.25xMy when one or both 1.25xMy width $> 0.5\text{um}$ when PRL $\geq -0.199\text{um}$	$\geq$	0.199	um
<b>1.25xMy.S.5</b>	Space between 1.25xMy when one or both 1.25xMy width $> 1.35\text{um}$ when PRL $> 1.35\text{um}$	$\geq$	0.448	um
<b>1.25xMy.S.6</b>	Space between 1.25xMy in CP direction when one or both 1.25xMy width = 0.04um	$=$	0.04, $\geq 0.07$	um
<b>1.25xMy.S.6a</b>	Space between 1.25xMy in CP direction when one or both 1.25xMy width = 0.042um	$=$	0.048, $\geq 0.07$	um
<b>1.25xMy.S.7</b>	Space between 1.25xMy in CP direction when one or both 1.25xMy width = 0.044um	$=$	0.046, $\geq 0.07$	um
<b>1.25xMy.S.7a</b>	Space between 1.25xMy in CP direction when one or both	$=$	0.046, $\geq$	um

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Rule number	Description	Opt.	Design Value	Unit
	1.25xMy width = 0.046um		0.07	
<b>1.25xMy.S.8</b>	Space between 1.25xMy in CP direction when one or both 1.25xMy width = 0.06um)	=	0.04, 0.046, $\geq 0.06$	um
<b>1.25xMy.S.8a</b>	Space between 1.25xMy in CP direction when one or both 1.25xMy width $> 0.06\text{um}$ when PRL $> 0.08\text{um}$	$\geq$	0.06	um
<b>1.25xMy.S.9</b>	Space between 1.25xMy in CP direction, when one or both width = 0.06um, and the other side space $< 0.06\text{um}$	$\geq$	0.079	um
<b>1.25xMy.S.10</b>	Space between 1.25xMy in CP direction when one or both 1.25xMy width $\geq 0.08\text{um}$ , except Z-shape corner. Z-shape corner definition: edge length $> 0.04\text{um}$ between two consecutive 90-270 degree corners, corresponding width = 0.08um in NCP direction between two opposite edge length $> 0.04\text{um}$	$\geq$	0.079	um
<b>1.25xMy.S.11</b>	Space between 1.25xMy in CP direction when one or both width $\geq 0.121\text{um}$ , PRL $> 0.08\text{um}$	$\geq$	0.099	um
<b>1.25xMy.S.12</b>	Space between 1.25xMy (CP direction width $> 0.16\text{um}$ and NCP direction width $> 0.08\text{um}$ ) and 1.25xMy edge (edge length $> 0.08 \text{ um}$ in NCP direction) in CP direction	$\geq$	0.119	um
<b>1.25xMy.S.13</b>	Space between 1.25xMy in CP direction when one or both width $\geq 0.201\text{um}$ , PRL $\geq 0.121\text{um}$	$\geq$	0.144	um
<b>1.25xMy.S.14</b>	Space between 1.25xMy in CP direction when one or both width $\geq 0.231\text{um}$ , PRL $\geq 0.121\text{um}$	$\geq$	0.159	um
<b>1.25xMy.S.15</b>	Space between 1.25xMy and 1.25xMy line-end (width = 0.08um) in CP direction when PRL $> -0.08\text{um}$	$\geq$	0.099	um
<b>1.25xMy.S.16</b>	Space between 1.25xMy in NCP direction when one or both width = 0.08, 0.12um	$\geq$	0.08	um
<b>1.25xMy.S.17</b>	Space between 1.25xMy ( $0.16\text{um} \leq \text{NCP direction width} < 0.2\text{um}$ and CP direction width $> 0.08\text{um}$ ) and 1.25xMy edge (edge length $> 0.08\text{um}$ in CP direction) in NCP direction	$\geq$	0.099	um
<b>1.25xMy.S.18</b>	Space between 1.25xMy in NCP direction when one or both width $> 0.12\text{um}$ , PRL $\geq 0.121\text{um}$	$\geq$	0.119	um
<b>1.25xMy.S.19</b>	Space between 1.25xMy (NCP direction width $\geq 0.2\text{um}$ and CP direction width $> 0.08\text{um}$ ) and 1.25xMy edge (edge length $>$	$\geq$	0.139	um

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Rule number	Description	Opt.	Design Value	Unit
	0.08um in CP direction) in NCP direction			
<b>1.25xMy.S.20</b>	Space between 1.25xMy in NCP direction when one or both width > 0.16um, PRL > 0.2um	≥	0.159	um
<b>1.25xMy.S.21</b>	Space between 1.25xMy and 1.25xMy line-end (width = 0.04/0.042um) in NCP direction when PRL > -0.04um	≥	0.089	um
<b>1.25xMy.S.21a</b>	Space between 1.25xMy and 1.25xMy line-end (width = 0.044/0.046/0.06um) in NCP direction when PRL > -0.04um	≥	0.08	um
<b>1.25xMy.S.22</b>	Space between 1.25xMy and 1.25xMy line-end (0.06um < width ≤ 0.08um) in NCP direction when PRL > -0.08um	≥	0.08	um
<b>1.25xMy.S.23</b>	Space between 1.25xMy line-end (width < 0.08um) and U-shape inner edge (edge length ≤ 0.149um between two concave corners) in NCP direction	≥	0.149	um
<b>1.25xMy.S.24a</b>	Space between 1.25xMy_Group_80 and 1.25xMy_Group_90 in CP direction when PRL > -0.08um 1.25xMy_Group_80 definition: (((1.25xMy (width = 0.04um) su 0.02um) sd -0.04um) su 0.02um) 1.25xMy_Group_90 definition: 1) (((1.25xMy (width = 0.044um) su 0.023um) sd -0.046um) su 0.023um) 2) (((1.25xMy (width = 0.042um) su 0.024um) sd -0.048um) su 0.024um)	≥	0.199	um
<b>1.25xMy.S.24b</b>	Space between 1.25xMy line-end of 1.25xMy_Group_80 and 1.25xMy line-end of 1.25xMy_Group_90 in NCP direction when PRL > -0.199um	≥	0.149	um
<b>1.25xMy.S.25</b>	Corner projected space between 1.25xMy when -0.08um < PRL ≤ 0um, except line end-to-end space (width ≤ 0.06um) and space to Z-shape corner (edge length > 0.04um between two consecutive 90-270 degree corners, corresponding width = 0.08um in NCP direction between two opposite edge length > 0.04um, not including T-shape)	≥	0.08	um
<b>1.25xMy.S.25a</b>	Corner space between 1.25xMy in NCP direction when -0.04um < PRL ≤ 0um	≥	0.08	um
<b>1.25xMy.S.26</b>	At least one space between 1.25xMy edge (any adjacent edge of concave corner) and 1.25xMy, except either condition as below 1. Edge length between two concave corners < 0.12um.	≥	0.119	um

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Rule number	Description	Opt.	Design Value	Unit
	2. Side edge length of concave corner < 0.042um			
1.25xMy.S.27	Space between 1.25xMy concave corner (both side edge length > 0.08um) and 1.25xMy line-end (width < 0.08um)	≥	0.154	um
1.25xMy.S.28	Fobidden space between 1.25xMy (width = 0.04~0.046um and one side space = 0.04um) and 1.25xMy (width < 0.08um) in CP direction, except both side space of 1.25xMy (width < 0.08um) to 1.25xMy ≥ 0.1um	=	0.061~ 0.098, 0.131~ 0.178	um
1.25xMy.S.29	Fobidden space between 1.25xMy (width = 0.06~0.07um and one side space = 0.04um) and 1.25xMy (width < 0.08um) in CP direction, except both side space of 1.25xMy (width < 0.08um) to 1.25xMy ≥ 0.1um.	=	0.11~ 0.158	um
1.25xMy.S.30	Space between 1.25xMy and 45-degree bent 1.25xMy, DRC check 45-degree direction	≥	0.396	um
1.25xMy.S.31	Space between 1.25xMy and Vy or 1.25xVn (maximum delta V > 1.155V) (1.05V + 10%)	≥	0.046	um
1.25xMy.S.32	Space between 1.25xMy and Vy or 1.25xVn (maximum delta V > 1.32V) (1.2V + 10%)	≥	0.059	um
1.25xMy.S.33	Space between 1.25xMy and Vy or 1.25xVn (maximum delta V > 1.98V) (1.8V + 10%)	≥	0.079	um
1.25xMy.S.34	Space between 1.25xMy and Vy or 1.25xVn (maximum delta V > 3.63V) (3.3V + 10%)	≥	0.159	um
1.25xMy.S.35	Space between two 1.25xMy (maximum delta V > 1.98V) (1.8V + 10%)	≥	0.046	um
1.25xMy.S.36	Space between two 1.25xMy (maximum delta V > 2.75V) (2.5V + 10%)	≥	0.079	um
1.25xMy.S.37	Space between two 1.25xMy (maximum delta V > 3.63V) (3.3V + 10%)	≥	0.104	um
1.25xMy.S.37a	Space between 1.25xMy line-end (width < 0.08um) and 1.25xMy (Maximum delta V > 3.63V) (3.3V + 10%) when PRL ≥ 0um	≥	0.135	um
1.25xMy.L.1	Length of 45-degree bent 1.25xMy, except MARKS	≥	0.905	um
1.25xMy.L.2	1.25xMy edge length when the adjacent edge length ≤ 0.089um, except two 0.08um edges form a convex corner.	≥	0.099	um

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Rule number	Description	Opt.	Design Value	Unit
<b>1.25xMy.L.3</b>	1.25xMy edge length when the adjacent edge length < 0.04um	≥	0.119	um
<b>1.25xMy.L.4</b>	1.25xMy edge length when the adjacent line-end width < 0.06um	≥	0.159	um
<b>1.25xMy.L.5</b>	1.25xMy edge length when the adjacent line-end width < 0.08um	≥	0.109	um
<b>1.25xMy.L.6</b>	1.25xMy edge length between two consecutive 90-270 degree corners	≥	0.019	um
<b>1.25xMy.L.7</b>	1.25xMy edge length between two consecutive 90-270 degree corners with one adjacent line end width < 0.08um and the other adjacent edge length > 0.07um	≥	0.238	um
<b>1.25xMy.L.8</b>	1.25xMy U-shape inner edge length between two consecutive 270-270 degree corners	≥	0.08	um
<b>1.25xMy.L.9</b>	Length of 1.25xMy metal branch (width ≤ 0.269um), when 1) Metal branch is connected to wide metal with width and length ≥ 0.398um 2) One square Vy-1/1.25xVn in metal branch, and space to wide metal ≤ 1um  DRC flags branch that can't enclose a 0.08*1um orthogonal rectangle.	≥	1	um
<b>1.25xMy.L.10</b>	Length of 1.25xMy metal branch (width ≤ 0.269um), when 1) Metal branch is connected to wide metal with width and length ≥ 0.542um 2) One square Vy-1/1.25xVn in metal branch, and space to wide metal ≤ 3um  DRC flags branch that can't enclose a 0.08*3um orthogonal rectangle.	≥	3	um
<b>1.25xMy.L.11</b>	Length of 1.25xMy metal branch (width ≤ 0.269um), when 1) Metal branch is connected to wide metal with width and length > 1um 2) One square Vy-1/1.25xVn in metal branch, and space to wide metal ≤ 5um  DRC flags branch that can't enclose a 0.08*5um rectangle.	≥	5	um
<b>1.25xMy.A.1</b>	1.25xMy area	≥	0.0148	um <sup>2</sup>

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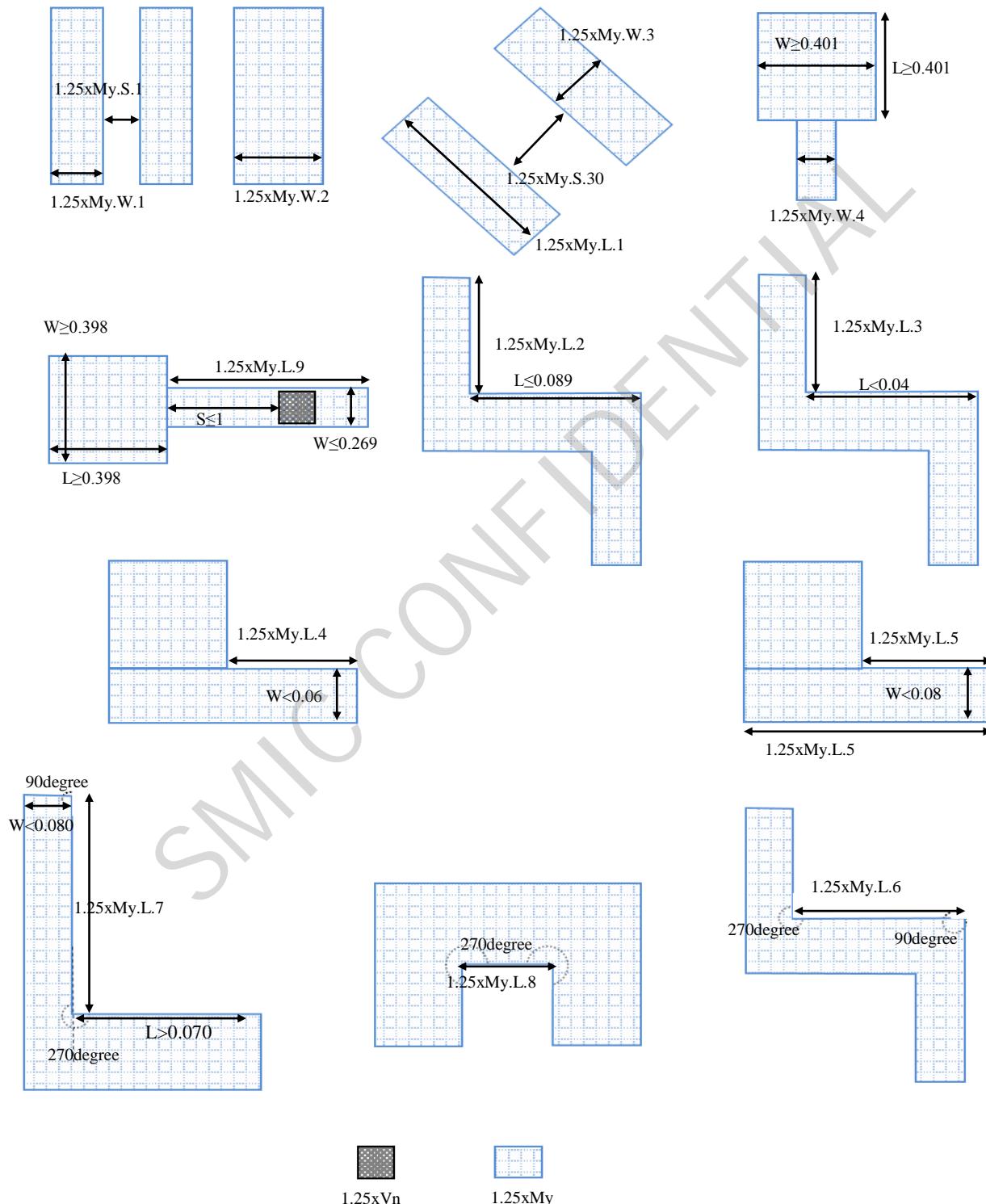
Rule number	Description	Opt.	Design Value	Unit
<b>1.25xMy.A.2</b>	1.25xMy area when all of edge length $\leq 0.115\mu m$ , except can fill 0.05*0.13um rectangle	$\geq$	0.039	$\mu m^2$
<b>1.25xMy.A.3</b>	1.25xMy enclosed area	$\geq$	0.181	$\mu m^2$
<b>1.25xMy.DN.1</b>	1.25xMy Density (window 50um*50um, stepping 25um), except LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	$\geq$	10%	
<b>1.25xMy.DN.1a</b>	1.25xMy Density (window 50um*50um, stepping 25um), except the window not interact 3um*3um empty area, LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	$\geq$	25%	
<b>1.25xMy.DN.2<sup>[R]</sup></b>	1.25xMy maximum density (window 50um*50um, stepping 25um), except dummy metal	$\leq$	65%	
<b>1.25xMy.DN.3</b>	1.25xMy maximum density (window 50um*50um, stepping 25um)	$\leq$	75%	
<b>1.25xMy.DN.4</b>	1.25xMy density difference between two neighboring checking windows (window 180um*180um, stepping 180um), except (NODMF su 0.4um) region.	$\leq$	50%	
<b>1.25xMy.DN.5</b>	It is not allowed to have local density $< 5\%$ of all 3 consecutive metal layers over any 30um*30um window (stepping 15um), except (NODMF su 0.4um) region.			
<b>1.25xMy.R.1<sup>[NC]</sup></b>	1.25xMy pattern must be drawn on data type 40.			
<b>1.25xMy.R.2</b>	It is not allowed for Maximum delta V $\geq 5.6V$ , when pace between 1.25xMy and 1.25xMy/above via/bottom via is $< 0.36\mu m$			

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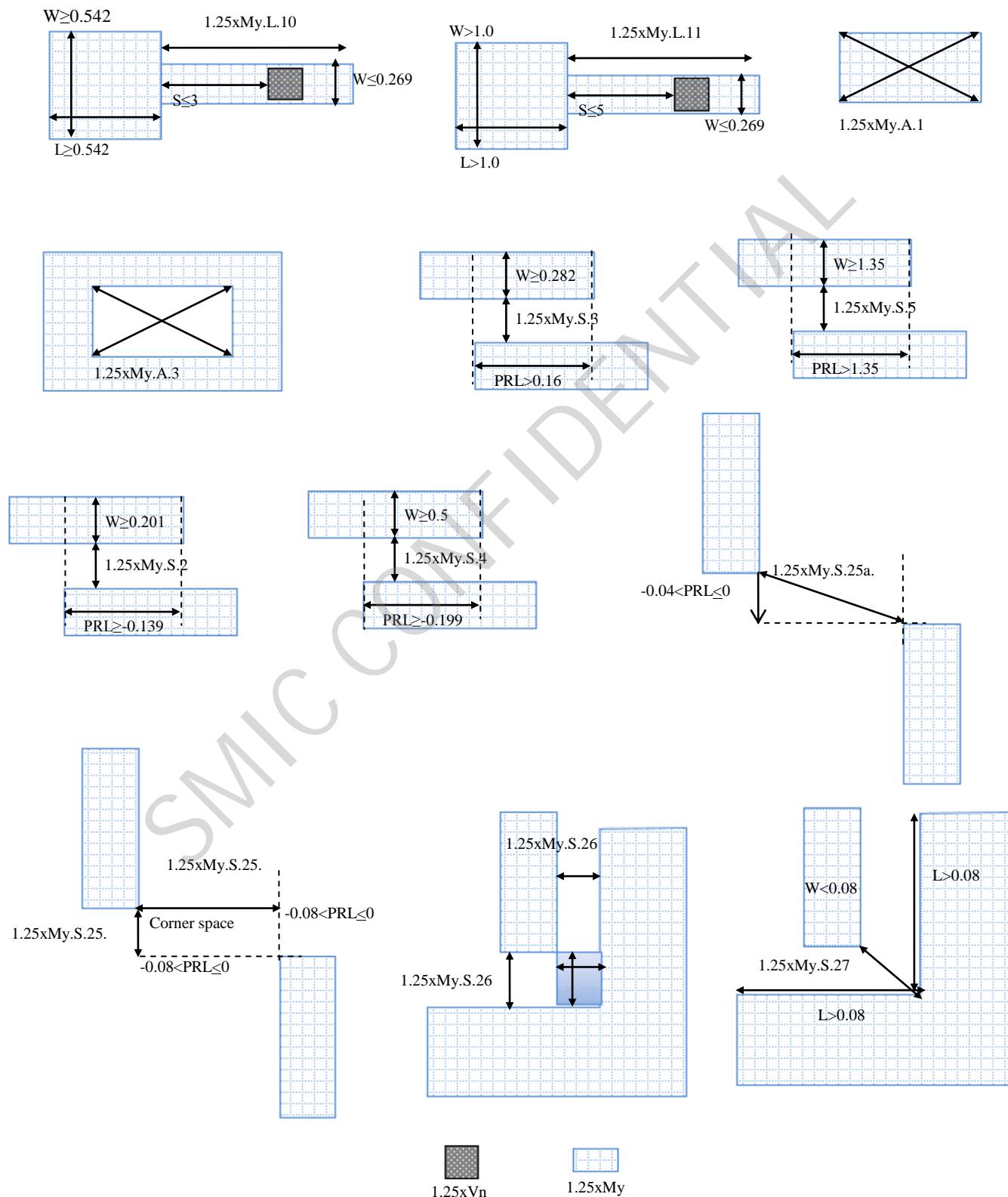


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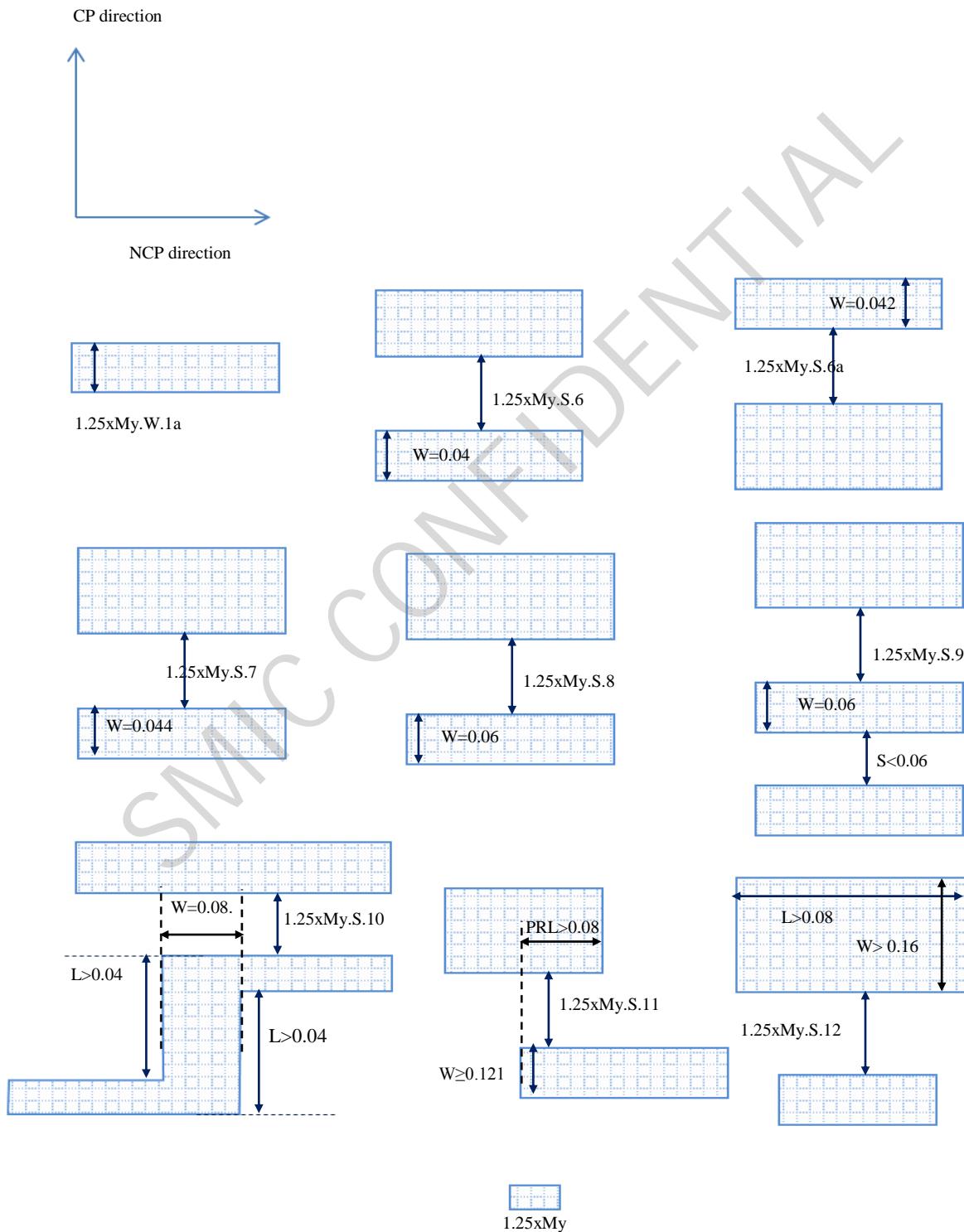


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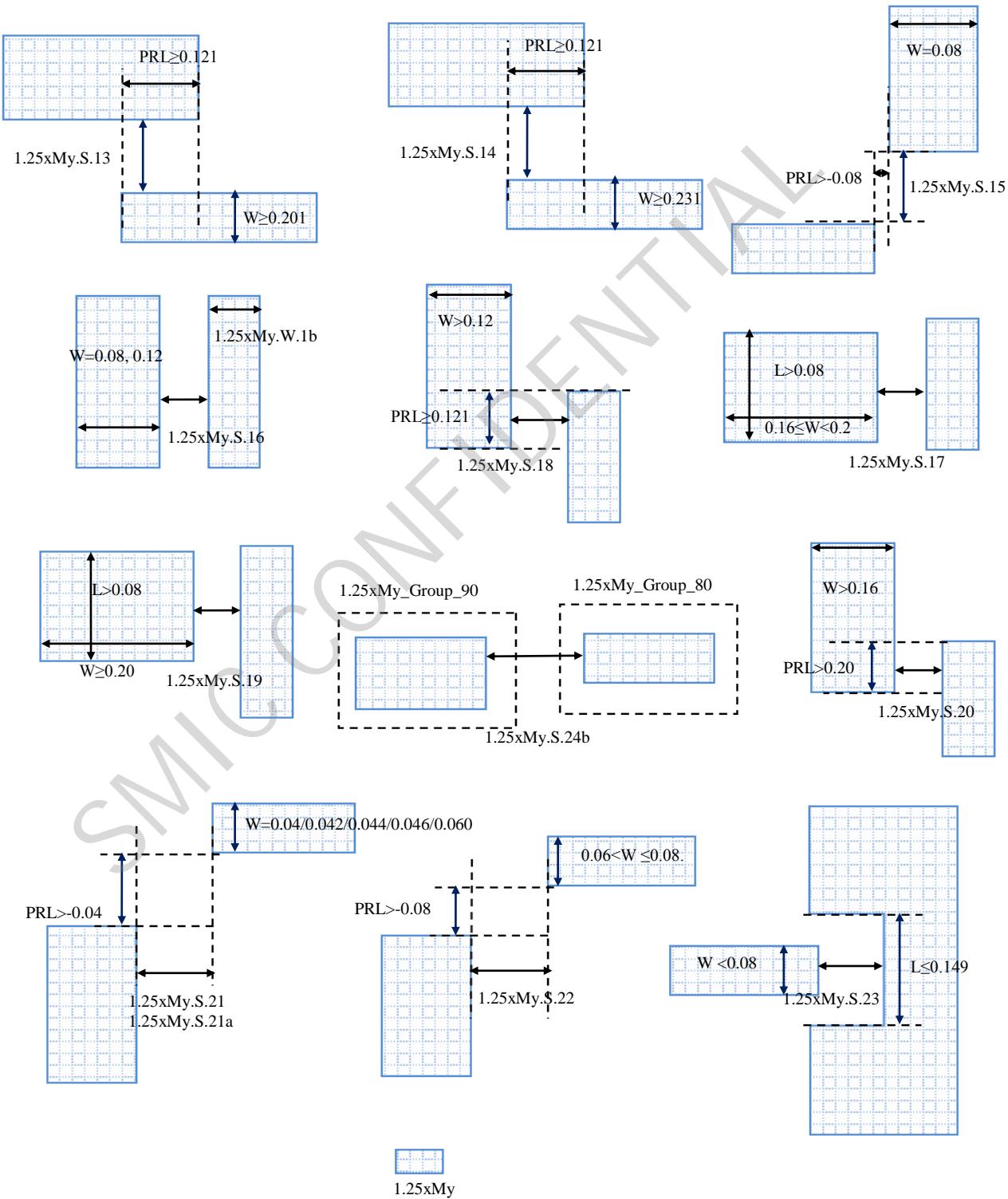


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## 7.2.39 1.25xVn design rules

### 7.2.39.1 Square 1.25xVn design rules

Rule number	Description	Opt.	Design Value	Unit
<b>1.25xVn.W.1</b>	1.25xVn width and length, except 0.04*0.1um 1.25xVn, MARKS, MARKG and LOGO regions	=	0.04	um
<b>1.25xVn.W.2</b>	1.25xVn bar width in MARKG/MARKS regions	=	0.1, 0.45	um
<b>1.25xVn.S.1</b>	Space between two 1.25xVn	$\geq$	0.056	um
<b>1.25xVn.S.2</b>	Space between two 1.25xVn when PRL > -0.04um	$\geq$	0.074	um
<b>1.25xVn.S.3</b>	Space between 1.25xVn (1.25xVn enclosure by upper metal > 0um) and Vy/1.25xVn-1 at different net and PRL > 0um	$\geq$	0.055	um
<b>1.25xVn.S.4</b>	Space between two square 1.25xVn with PRL > -0.119um, when 1) 1.25xVn enclosure by 1.25xMy/1.25xMn/1.25xMn+1 < 0.01um at opposite side. 2) Space between 1.25xVn and 1.25xMy/1.25xMn/1.25xMn+1 $\leq$ 0.052um with PRL $\geq$ -0.046um at opposite side. DRC doesn't flag space between 1.25xVn and 1.25xMy/1.25xMn/1.25xMn+1 $\leq$ 0.052um with PRL $\geq$ -0.046um on both sides.	$\geq$	0.119	um
<b>1.25xVn.S.5</b>	Space between 1.25xVn bar (width = 0.1/0.45um) and (1.25xVn or 1.25xRVn)	$\geq$	0.34	um
<b>1.25xVn.S.6</b>	Space between 1.25xVn bar (width = 0.1/0.45um), DRC only check the space between parallel edge when the 1.25xVn bar is inside MARKS	$\geq$	0.55	um
<b>1.25xVn.EN.1</b>	1.25xVn must be fully enclosed by 1.25xMy or 1.25xMn where 1.25xMy or 1.25xMn is the metal layer direct underneath 1.25xVn. Enclosure by 1.25xMy or 1.25xMn must follow one of 1.25xVn.EN.2 or 1.25xVn.EN.2a or 1.25xVn.EN.3 or 1.25xVn.EN.3a or 1.25xVn.EN.4 or 1.25xVn.EN.5 or 1.25xVn.EN.6 or 1.25xVn.EN.7			
<b>1.25xVn.EN.2</b>	1.25xVn enclosure by 1.25xMy or 1.25xMn (width = 0.04um) for two opposite sides with the other two sides $\geq$ 0 um	$\geq$	0.049	um

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Rule number	Description	Opt.	Design Value	Unit
<b>1.25xVn.EN.2a</b>	1.25xVn enclosure by 1.25xMy or 1.25xMn (width = 0.042um) for two opposite sides with the other two sides $\geq$ 0.001 um	$\geq$	0.049	um
<b>1.25xVn.EN.3</b>	1.25xVn enclosure by 1.25xMy or 1.25xMn (width = 0.044um) for two opposite sides with the other two sides $\geq$ 0.002 um	$\geq$	0.049	um
<b>1.25xVn.EN.4</b>	1.25xVn enclosure by 1.25xMy or 1.25xMn (width = 0.046um) for two opposite sides with the other two sides $\geq$ 0.003 um	$\geq$	0.049	um
<b>1.25xVn.EN.5</b>	1.25xVn enclosure by 1.25xMy or 1.25xMn (0.06 $\leq$ width < 0.08um) for two opposite sides with the other two sides $\geq$ 0.01 um	$\geq$	0.049	um
<b>1.25xVn.EN.6</b>	1.25xVn enclosure by 1.25xMy or 1.25xMn (width = 0.08um) for all sides	$\geq$	0.02	um
<b>1.25xVn.EN.7</b>	1.25xVn enclosure by 1.25xMy or 1.25xMn (width > 0.08um) for two opposite sides with the other two sides $\geq$ 0.02um	$\geq$	0.029	um
<b>1.25xVn.EN.8</b>	1.25xVn bar enclosure by 1.25xMy or 1.25xMn	$\geq$	0.098	um
<b>1.25xVn.EN.9</b>	1.25xVn must be fully enclosed by 1.25xMn+1 where 1.25xMn+1 is the metal layer directly above 1.25xVn. Enclosure by 1.25xMn+1 must follow one of 1.25xVn.EN.10 or 1.25xVn.EN.11 or 1.25xVn.EN.12 or 1.25xVn.EN.13 or 1.25xVn.EN.14			
<b>1.25xVn.EN.10</b>	1.25xVn enclosure by 1.25xMn+1 (width = 0.04um) for two opposite sides with the other two sides $\geq$ 0 um	$\geq$	0.049	um
<b>1.25xVn.EN.10a</b>	1.25xVn enclosure by 1.25xMn+1 (width = 0.042um) for two opposite sides with the other two sides $\geq$ 0.001 um	$\geq$	0.049	um
<b>1.25xVn.EN.11</b>	1.25xVn enclosure by 1.25xMn+1 (width = 0.044um) for two opposite sides with the other two sides $\geq$ 0.002 um	$\geq$	0.049	um
<b>1.25xVn.EN.11a</b>	1.25xVn enclosure by 1.25xMn+1 (width = 0.046um) for two opposite sides with the other two sides $\geq$ 0.003 um	$\geq$	0.049	
<b>1.25xVn.EN.12</b>	1.25xVn enclosure by 1.25xMn+1 (0.06 $\leq$ width < 0.08um) for two opposite sides with the other two sides $\geq$ 0.01um	$\geq$	0.049	um
<b>1.25xVn.EN.13</b>	1.25xVn enclosure by 1.25xMn+1 (width = 0.08um) for all sides	$\geq$	0.02	um

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Rule number	Description	Opt.	Design Value	Unit
<b>1.25xVn.EN.14</b>	1.25xVn enclosure by 1.25xMn+1 (width > 0.08um) for two opposite sides with the other two sides $\geq$ 0.02um	$\geq$	0.029	um
<b>1.25xVn.EN.15</b>	1.25xVn enclosure by 1.25xMn+1 edge (between two consecutive 90-270 degree corners, length < 0.16 um), when PRL > 0	$\geq$	0.029	um
<b>1.25xVn.EN.16</b>	1.25xVn enclosure by 1.25xMn+1 for two opposite sides (PRL > 0) with the other side enclosure < 0.04um (corresponding edge length < 0.16um between two consecutive 90-270 degree corners)	$\geq$	0.040	um
<b>1.25xVn.EN.17</b>	1.25xVn bar fully enclosure by 1.25xMn+1.	$\geq$	0.2	um
<b>1.25xVn.D.1<sup>[R]</sup></b>	(1.25xVn OR 1.25xRVn) density (window 5um*5um, stepping 2.5um)	<	12%	
<b>1.25xVn.R.1</b>	45-degree 1.25xVn is not allowed.			
<b>1.25xVn.R.2</b>	It is not allowed to have single 1.25xVn in "H-shape" 1.25xMn+1 when all of the following conditions come into existence: 1. The 1.25xMn+1 has "H-shape" interact two metal holes: both two metal hole length $L \leq 4.5\mu m$ and two metal hole area $\leq 4.05\mu m^2$ 2. The 1.25xVn overlaps on the center metal bar of this "H-shape" 1.25xMn+1 3. The center metal bar length $\leq 0.9\mu m$ and the metal bar width $\leq 0.162\mu m$			
<b>1.25xVn.R.3</b>	The numbers of neighboring square 1.25xVn to each edge of 1.25xVn $\leq 0.065\mu m$ is not allowed	<	2	
<b>1.25xVn.R.4</b>	The numbers of neighboring square 1.25xVn in one group (space $\leq 0.065\mu m$ )	$\leq$	3	
<b>1.25xVn.R.5</b>	Maximum delta V $\geq 5.6V$ is not allowed, when space between 1.25xVn is $< 0.410\mu m$			
<b>1.25xVn.R.8<sup>[NC]</sup></b>	1.25xVn pattern must be drawn on data type 50.			
<b>1.25xVn.R.9</b>	It's not allowed 1.25xVn overlap with the metal resistor directly underneath and above the 1.25xVn			
<b>1.25xVn.R.10<sup>[R]</sup></b>	Recommend space between a square 1.25xVn and another (1.25xVn OR 1.25xRVn OR DUM_1.25xVn) $< 4\mu m$ to avoid			

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Rule number	Description	Opt.	Design Value	Unit
	single square 1.25xVn			

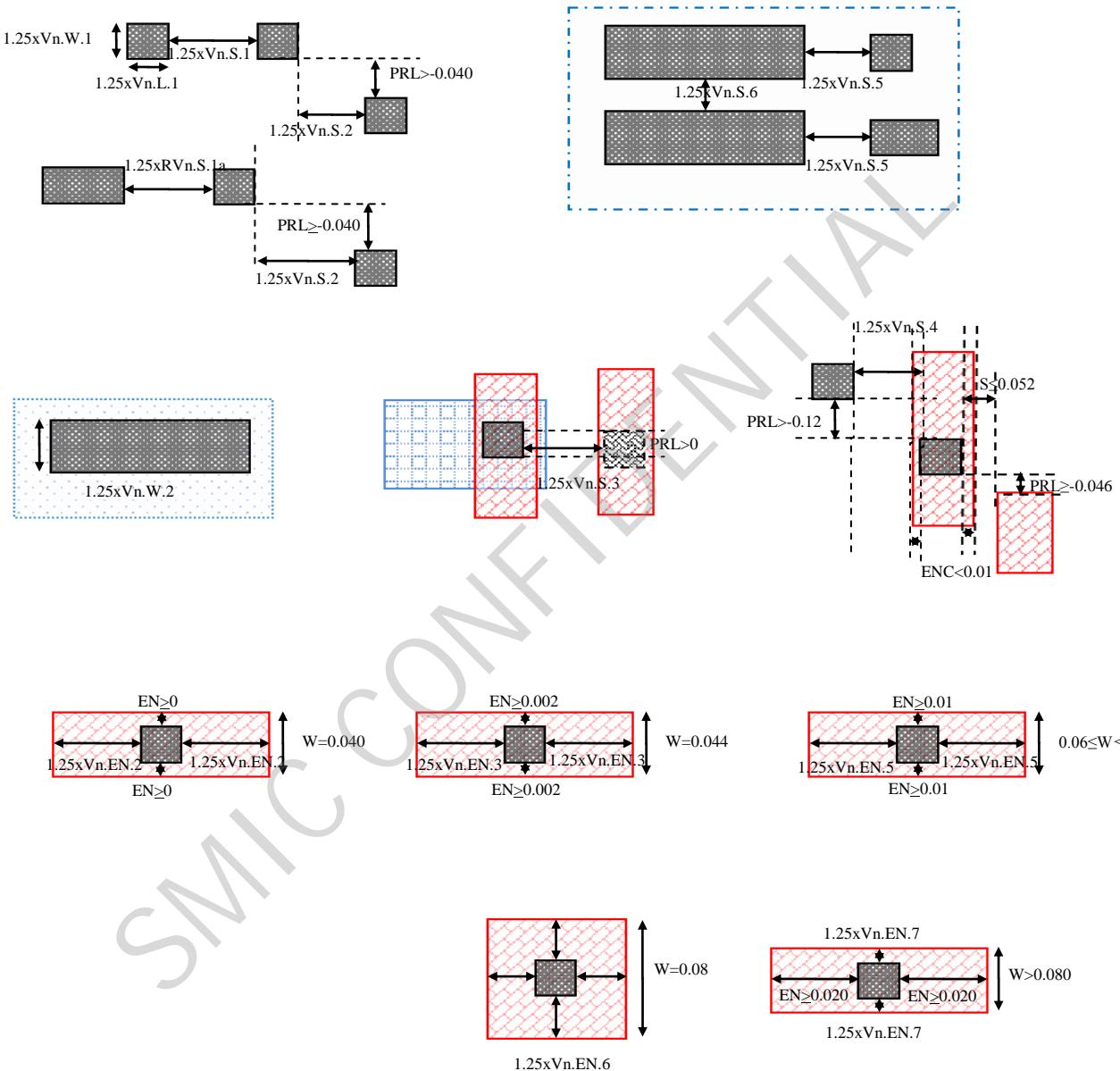
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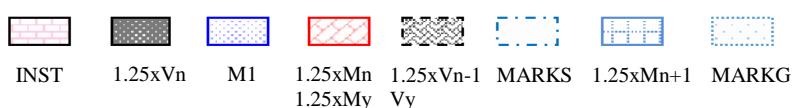
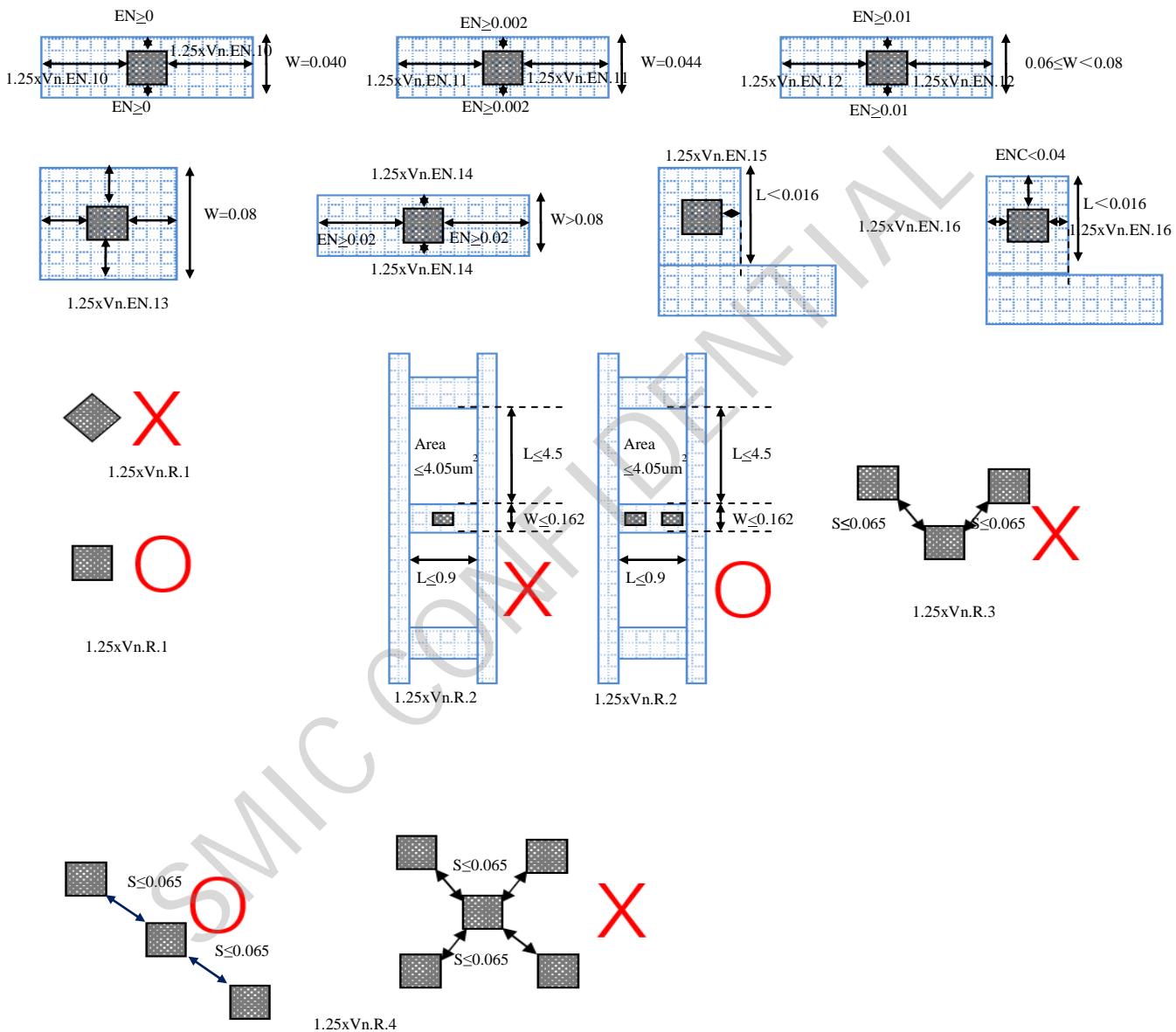
INST	$1.25xVn$	M1	$1.25xMn$	$1.25xVn-1$	MARKS	$1.25xMn+1$	MARKG
				$1.25xMy$			

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### 7.2.39.2 Rectangular 1.25xVn design rules

Rule number	Description	Opt.	Design Value	Unit
<b>1.25xRVn.W.1</b>	1.25xRVn width, except MARKS, MARKG and LOGO regions	=	0.04	um
<b>1.25xRVn.L.1</b>	Length of 1.25xRVn (width = 0.04um)	=	0.1	um
<b>1.25xRVn.S.1a</b>	Space between (1.25xVn or 1.25xRVn) and 1.25xRVn	≥	0.074	um
<b>1.25xRVn.S.1b</b>	Space between (1.25xVn or 1.25xRVn) and 1.25xRVn when PRL > -0.04um	≥	0.079	um
<b>1.25xRVn.S.1c</b>	Space between the short side of 1.25xRVn and (1.25xVn or 1.25xRVn) when PRL > -0.04um	≥	0.089	um
<b>1.25xRVn.S.2</b>	Space between 1.25xRVn and (Vy or RVy) at different net and PRL > 0um, when 1.25xMn+1 enclosure of 1.25xRVn > 0um	≥	0.055	um
<b>1.25xRVn.S.3</b>	Space between 1.25xRVn and (1.25xRVn-1 or 1.25xVn-1) at different net and PRL > 0um, when 1.25xMn+1 enclosure of 1.25xRVn > 0um	≥	0.055	um
<b>1.25xRVn.S.4</b>	Space between 1.25xRVn when PRL ≥ -0.119um, when 1) 1.25xRVn enclosure by 1.25xMy/1.25xMn/1.25xMn+1 < 0.01um at opposite side. 2) Space between 1.25xRVn and 1.25xMy/1.25xMn/1.25xMn+1 ≤ 0.052um with PRL ≥ -0.046um at opposite side. DRC doesn't flag space between 1.25xRVn and 1.25xMy/1.25xMn/1.25xMn+1 ≤ 0.052um with PRL ≥ -0.046um on both sides.	≥	0.119	um
<b>1.25xRVn.EN.1</b>	1.25xRVn must be fully enclosed by 1.25xMy or 1.25xMn where 1.25xMy or 1.25xMn is the metal layer directly underneath 1.25xRVn. Enclosure by 1.25xMy or 1.25xMn must follow one of 1.25xRVn.EN.2 or 1.25xRVn.EN.2a or 1.25xRVn.EN.3 or 1.25xRVn.EN.3a or 1.25xRVn.EN.4 or 1.25xRVn.EN.5 or 1.25xRVn.EN.6 or 1.25xRVn.EN.7 or 1.25xRVn.EN.8			
<b>1.25xRVn.EN.2</b>	1.25xRVn enclosure by 1.25xMy or 1.25xMn (width = 0.04um) for two opposite sides with the other two sides ≥ 0 um	≥	0.049	um
<b>1.25xRVn.EN.2a</b>	1.25xRVn enclosure by 1.25xMy or 1.25xMn (width = 0.042um)	≥	0.049	um

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Rule number	Description	Opt.	Design Value	Unit
	for two opposite sides with the other two sides $\geq 0.001 \mu m$			
<b>1.25xRVn.EN.3</b>	1.25xRVn enclosure by 1.25xMy or 1.25xMn (width = 0.044um) for two opposite sides with the other two sides $\geq 0.002 \mu m$	$\geq$	0.049	um
<b>1.25xRVn.EN.3a</b>	1.25xRVn enclosure by 1.25xMy or 1.25xMn (width = 0.046um) for two opposite sides with the other two sides $\geq 0.003 \mu m$	$\geq$	0.049	um
<b>1.25xRVn.EN.4</b>	1.25xRVn enclosure by 1.25xMy or 1.25xMn ( $0.06\mu m \leq \text{width} < 0.08\mu m$ ) for two opposite sides with the other two sides $\geq 0.01\mu m$	$\geq$	0.049	um
<b>1.25xRVn.EN.5</b>	1.25xRVn enclosure by 1.25xMy or 1.25xMn (width = 0.08um) for all sides	$\geq$	0.02	um
<b>1.25xRVn.EN.6</b>	1.25xRVn enclosure by 1.25xMy or 1.25xMn (width > 0.08um) for two opposite sides with the other two sides $\geq 0.02\mu m$ (except rectangular 1.25xRVn array)	$\geq$	0.029	um
<b>1.25xRVn.EN.7</b>	1.25xRVn enclosure by short side of 1.25xMy or 1.25xMn (width > 0.08um) with long side enclosure $\geq 0.039\mu m$ (except rectangular 1.25xRVn array)	$\geq$	0.01	um
<b>1.25xRVn.EN.8</b>	1.25xRVn array enclosed by 1.25xMn/1.25xMy for two opposite sides with the other two sides (rectangular 1.25xVn array edge length = 0.1um) $\geq 0.02\mu m$ Definition of 1.25xRVn array: 1.25xVn long side space = 0.08 um (PRL = 0.1um)	$\geq$	0.01	um
<b>1.25xRVn.EN.9</b>	1.25xRVn must be fully enclosed by 1.25xMn+1 where 1.25xMn+1 is the metal layer directly above 1.25xRVn. Enclosures by 1.25xMn+1 must follow one of 1.25xRVn.EN.10, 1.25xRVy.EN.10a, 1.25xRVn.EN.10b or 1.25xRVn.EN.11 or 1.25xRVn.EN.12 or 1.25xRVn.EN.13, RVy.EN.13a or 1.25xRVn.EN.14.			
<b>1.25xRVn.EN.10</b>	1.25xRVn enclosure by 1.25xMn+1 (width = 0.04um) for two opposite sides with the other two sides $\geq 0\mu m$	$\geq$	0.039	um
<b>1.25xRVn.EN.10a</b>	1.25xRVn enclosure by 1.25xMn+1 (width = 0.042um) for two opposite sides with the other two sides $\geq 0.001\mu m$	$\geq$	0.039	um
<b>1.25xRVn.EN.10b</b>	1.25xRVn enclosure by 1.25xMn+1 (width = 0.044um) for two opposite sides with the other two sides $\geq 0.002\mu m$	$\geq$	0.039	um
<b>1.25xRVn.EN.10c</b>	1.25xRVn enclosure by 1.25xMn+1 (width = 0.046um) for two	$\geq$	0.039	um

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Rule number	Description	Opt.	Design Value	Unit
	opposite sides with the other two sides $\geq 0.003\mu m$			
<b>1.25xRVn.EN.10d</b>	1.25xRVn enclosure by 1.25xMn+1 (width $\geq 0.06 < 0.08\mu m$ ) for two opposite sides with the other two sides $\geq 0.01\mu m$	$\geq$	0.039	um
<b>1.25xRVn.EN.11</b>	1.25xRVn enclosure by 1.25xMn+1 (width = $0.08\mu m$ ) for all sides	$\geq$	0.02	um
<b>1.25xRVn.EN.12</b>	1.25xRVn enclosure by 1.25xMn+1 (width $> 0.080\mu m$ ) for two opposite sides with the other two sides $\geq 0.02\mu m$ (except rectangular 1.25xVn array)	$\geq$	0.029	um
<b>1.25xRVn.EN.13</b>	1.25xRVn short side enclosed by 1.25xMn+1, 1.25xMn+1 (width $\geq 0.12\mu m$ ) with long sides enclosure $\geq 0.039\mu m$ (except rectangular 1.25xVn array)	$\geq$	0.01	um
<b>1.25xRVn.EN.13a</b>	1.25xRVn enclosure by 1.25xMn+1 (width $\geq 0.12\mu m$ ) for two opposite sides with the other two sides $\geq 0.02\mu m$ (except rectangle 1.25xVn array)	$\geq$	0.029	um
<b>1.25xRVn.EN.14</b>	1.25xRVn array enclosed by 1.25xMn+1 for two opposite sides with the other two sides (rectangular 1.25xVn array edge length = $0.1\mu m$ ) $\geq 0.02\mu m$ Definition of rectangular 1.25xVn array: 1.25xVn long side space = $0.08\mu m$ (PRL = $0.1\mu m$ )	$\geq$	0.01	um
<b>1.25xRVn.EN.15</b>	1.25xRVn enclosure by 1.25xMn+1 edge (between two consecutive 90-270 degree corners, length $< 0.16\mu m$ ), when PRL > 0	$\geq$	0.029	um
<b>1.25xRVn.EN.16</b>	1.25xRVn enclosure by 1.25xMn+1 for two opposite sides (PRL > 0) with the other side enclosure $< 0.04\mu m$ (corresponding edge length $< 0.16\mu m$ between two consecutive 90-270 degree corners)	$\geq$	0.040	um
<b>1.25xRVn.R.1</b>	Single 1.25xRVn is not allowed in "H-shape" 1.25xMn+1, when: 1. The 1.25xMn+1 has "H-shape" interacting with two metal holes: both two metal holes length $\leq 4.5\mu m$ and two metal hole area $\leq 4.05\mu m^2$ 2. The 1.25xRVn overlaps on the center metal bar of this "H-shape" 1.25xMn+1. 3. The center metal bar length $\leq 0.9\mu m$ and the metal bar width $\leq 0.162\mu m$ . DRC doesn't check when one or more square 1.25xRVn is also			

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Rule number	Description	Opt.	Design Value	Unit
	on H-shape 1.25xMn+1 region.			
<b>1.25xRVn.R.2</b>	Redundant via requirement must be obeyed by one of following conditions of via numbers and space for 1.25xMy/1.25xMn, 1.25xMn+1 connection (one of 1.25xMy/1.25xMn or 1.25xMn+1 have width and length $\geq 0.164\mu m$ , two square vias are equal to one rectangular via for below conditions) (Except VIA bar) 1) At least one rectangular 1.25xVn 2) At least two square 1.25xVn with space $\leq 0.091\mu m$ 3) At least four square 1.25xVn with space $\leq 0.59\mu m$			
<b>1.25xRVn.R.3</b>	Redundant via requirement must be obeyed by one of following conditions of 1.25xVn numbers and space for 1.25xMy/1.25xMn and 1.25xMn+1 connection (one of 1.25xMy/1.25xMn or 1.25xMn+1 have width and length $\geq 0.398\mu m$ , two square vias are equal to one rectangular via for below conditions), except VIA bar, OCCD region 1) At least 4 square 1.25xVn with space $\leq 0.091\mu m$ 2) At least two square 1.25xVn and 1 rectangular 1.25xVn with space $\leq 0.118\mu m$ 3) At least 9 square 1.25xVn with space $\leq 0.77\mu m$ For condition 2) and 3), two square 1.25xVn can be replaced by 1 rectangular 1.25xVn.			
<b>1.25xRVn.R.4</b>	There should be at least two square 1.25xVn or one rectangular 1.25xVn in the intersection area of bottom metal and upper metal, when either wide metal 1.25xMy/1.25xMn or 1.25xMn+1 length $\geq 0.162\mu m$ and width $\geq 0.162\mu m$ , the space between either via and wide metal is $\leq 1.48\mu m$ (S, S is the shortest running path length from Via to the wide metal). (except via bar). DRC flags each intersecting area ({bottom metal AND upper metal}) with single square Via within the branch check region			
<b>1.25xRVn.R.5</b>	There should be at least two square 1.25xVn or one rectangular 1.25xVn in the intersection area of bottom metal and upper metal, when either wide metal 1.25xMy/1.25xMn or 1.25xMn+1 length $\geq 0.91\mu m$ and width $\geq 0.91\mu m$ , the space between either via and wide metal is $\leq 3.59\mu m$ (S, S is the shortest running path length from Via to the wide metal). (except via bar).			

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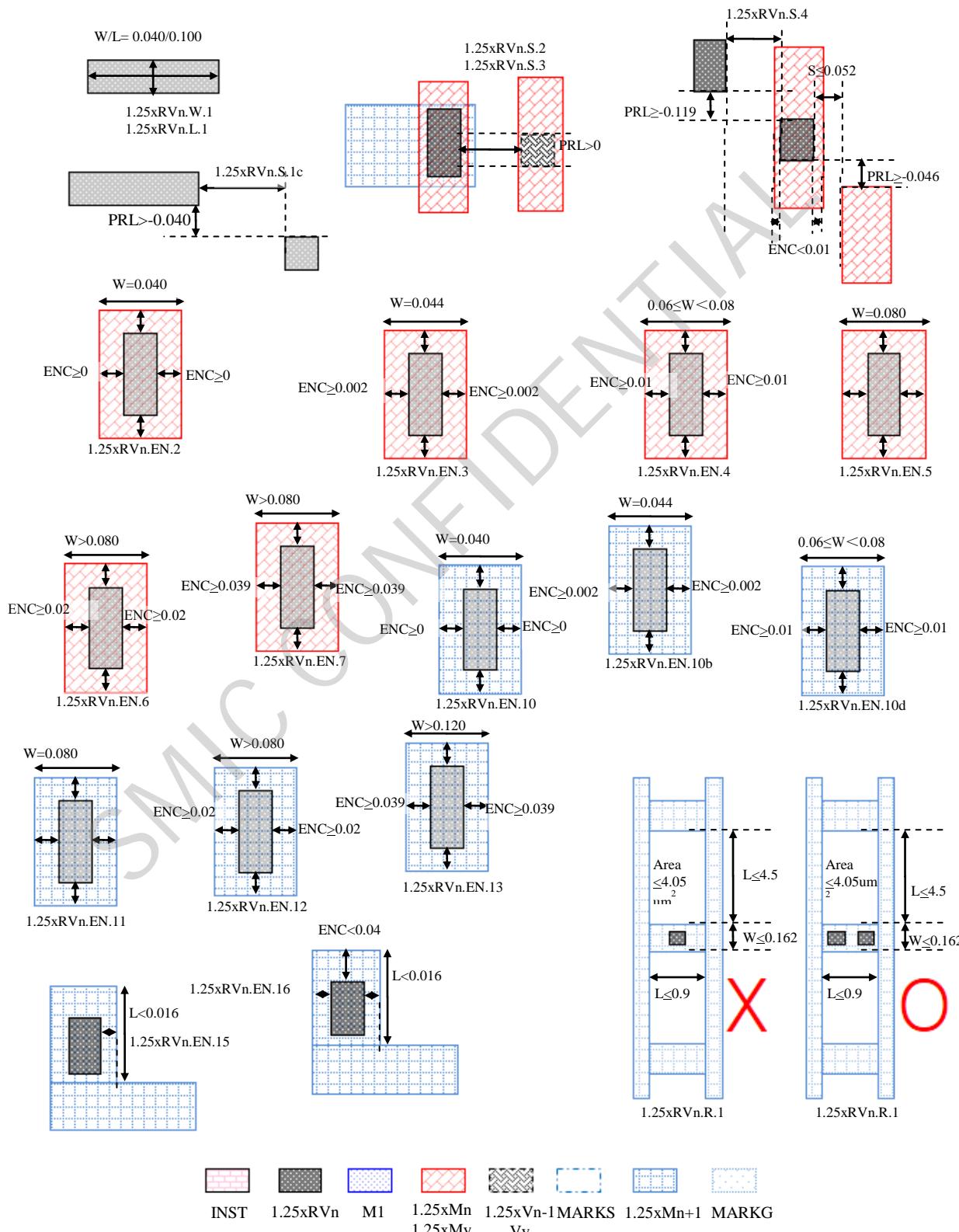
Rule number	Description	Opt.	Design Value	Unit
<b>1.25xRVn.R.6</b>	There should be at least two square 1.25xVn or one rectangular 1.25xVn in the intersection area of bottom metal and upper metal, when either wide metal 1.25xMy/1.25xMn or 1.25xMn+1 length $\geq$ 1.36um and width $\geq$ 1.36um, the space between either via and wide metal is $\leq$ 9um (S, S is the shortest running path length from Via to the wide metal). (except via bar).			
<b>1.25xRVn.R.7</b>	45-degree 1.25xRVn is not allowed.			
<b>1.25xRVn.R.8</b>	Maximum delta V $\geq$ 5.6V is not allowed, when space between 1.25xRVn is $<$ 0.410um			

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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:2

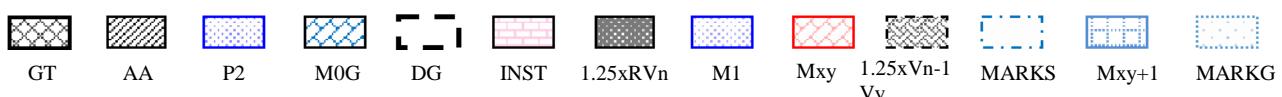
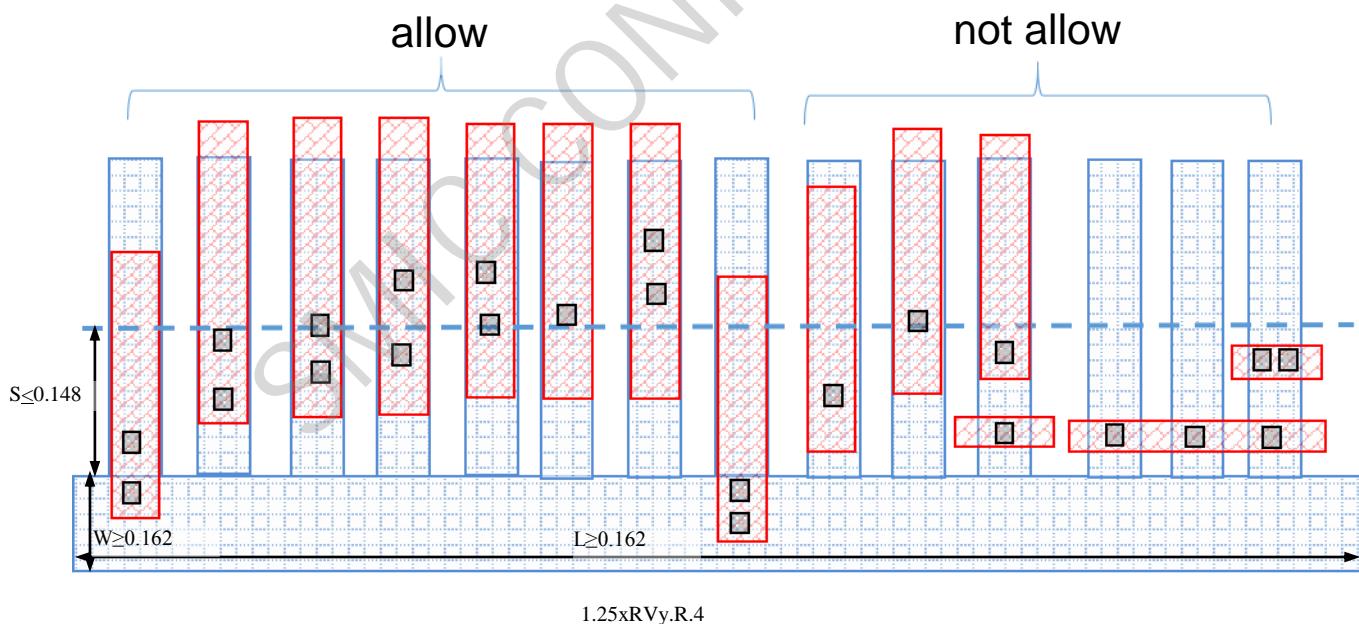
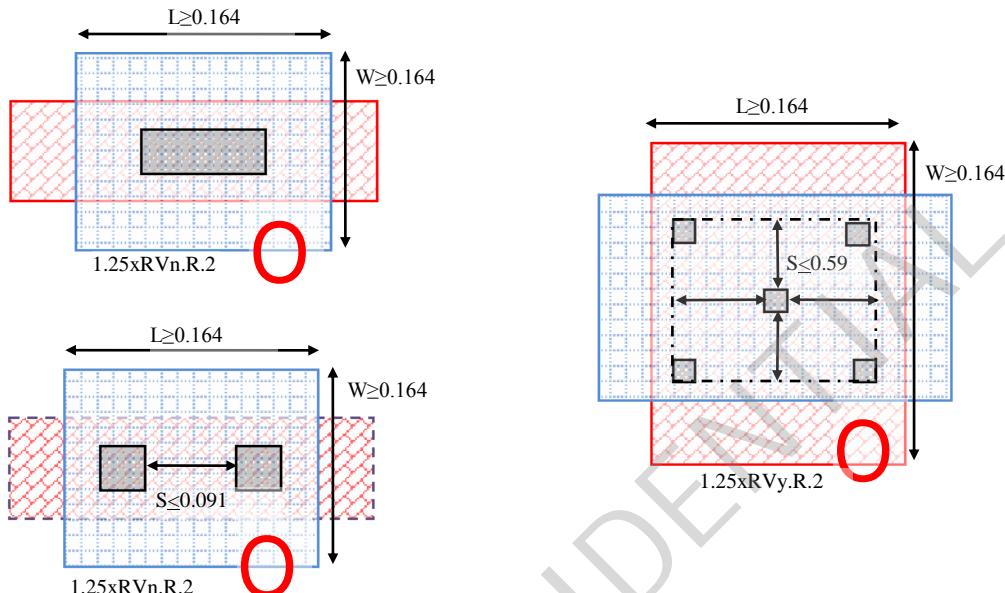
2017-11-02

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#### 7.2.40 1.25xMn design rules

Rule number	Description	Opt.	Design Value	Unit
<b>1.25xMn.W.1</b>	1.25xMn width	$\geq$	0.04	um
<b>1.25xMn.W.1a</b>	1.25xMn width in CP direction  The width should be even value when $\leq 0.046\text{um}$ CP direction definition: Critical-Pitch direction along the minimum pitch (80nm) of 1.25xMn	$=$	0.04~0.046, $\geq 0.06$	um
<b>1.25xMn.W.1b</b>	1.25xMn width in NCP direction  NCP direction definition: Non-Critical-Pitch direction which is perpendicular to CP direction	$=$	0.08, $\geq 0.12$	um
<b>1.25xMn.W.2</b>	Maximum 1.25xMn width, except MARKS, and LOGO regions. DRC doesn't flag (1.25xMn AND DUPMK1) region when the 1.25xMn layer is used as TM-1.	$\leq$	2.1	um
<b>1.25xMn.W.3</b>	1.25xMn width of 45-degree bent metal	$\geq$	0.396	um
<b>1.25xMn.W.4</b>	1.25xMn width of metal branch connected to wide metal width and length $\geq 0.401\text{um}$	$\geq$	0.08	um
<b>1.25xMn.W.5</b>	1.25xMn width when PRL $< 0$	$\geq$	0.08	um
<b>1.25xMn.S.1</b>	1.25xMn space	$\geq$	0.04	um
<b>1.25xMn.S.2</b>	Space between 1.25xMn when one or both width $\geq 0.201\text{um}$ when PRL $\geq -0.139\text{um}$	$\geq$	0.139	um
<b>1.25xMn.S.3</b>	Space between 1.25xMn when one or both width $\geq 0.282\text{um}$ when PRL $> 0.16\text{um}$	$\geq$	0.199	um
<b>1.25xMn.S.4</b>	Space between 1.25xMn when one or both width $> 0.5\text{um}$ when PRL $\geq -0.199\text{um}$	$\geq$	0.199	um
<b>1.25xMn.S.5</b>	Space between 1.25xMn when one or both width $> 1.35\text{um}$ when PRL $> 1.35\text{um}$	$\geq$	0.448	um
<b>1.25xMn.S.6</b>	Space between 1.25xMn in CP direction when one or both width = $0.04\text{um}$ .	$=$	0.04, $\geq 0.07$	um
<b>1.25xMn.S.6a</b>	Space between 1.25xMn in CP direction when one or both width = $0.042\text{um}$ .	$=$	0.048, $\geq 0.07$	um
<b>1.25xMn.S.7</b>	Space between 1.25xMn in CP direction when one or both width = $0.044\text{um}$	$=$	0.046, $\geq 0.07$	um

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Rule number	Description	Opt.	Design Value	Unit
<b>1.25xMn.S.7a</b>	Space between 1.25xMn in CP direction when one or both width = 0.046um	=	0.046, $\geq$ 0.07	um
<b>1.25xMn.S.8</b>	Space between 1.25xMn in CP direction when one or both width = 0.06um.	=	0.04, 0.046, $\geq$ 0.06	um
<b>1.25xMn.S.8a</b>	Space between 1.25xMn in CP direction when one or both width $>$ 0.06um when PRL $>$ 0.08um	$\geq$	0.06	um
<b>1.25xMn.S.9</b>	Space between 1.25xMn in CP direction, when one or both width = 0.06um, and the other side space $<$ 0.06um	$\geq$	0.079	um
<b>1.25xMn.S.10</b>	Space between 1.25xMn in CP direction when one or both width $\geq$ 0.08um, except Z shape and flag shape. (1) Z-shape definition: edge length $>$ 0.04um between two consecutive 90-270 degree corners, corresponding width = 0.08 um in NCP direction between two opposite edge length $>$ 0.04um, not including T-shape (2) Flag-shape definition: edge length $>$ 0.04um between two consecutive 90-270 degree corners, the opposite edge length $>$ 0.08um between two consecutive 90-90 degree corners, corresponding width = 0.08um in NCP direction between these two opposite edge, and the other corresponding width $>$ 0.04um in CP direction	$\geq$	0.079	um
<b>1.25xMn.S.11</b>	Space between 1.25xMn in CP direction when one or both width $\geq$ 0.121um, PRL $>$ 0.08um	$\geq$	0.099	um
<b>1.25xMn.S.12</b>	Space between 1.25xMn (CP direction width $>$ 0.16um and NCP direction width $>$ 0.08um) and 1.25xMn edge (edge length $>$ 0.08 um in NCP direction) in CP direction	$\geq$	0.119	um
<b>1.25xMn.S.13</b>	Space between 1.25xMn in CP direction when one or both width $\geq$ 0.201um, PRL $\geq$ 0.121um	$\geq$	0.144	um
<b>1.25xMn.S.14</b>	Space between 1.25xMn in CP direction when one or both width $\geq$ 0.231um, PRL $\geq$ 0.121um	$\geq$	0.159	um
<b>1.25xMn.S.15</b>	Space between 1.25xMn and 1.25xMn line-end (width = 0.08um and both adjacent edge length $>$ 0.09um) in CP direction when PRL $>$ -0.08um	$\geq$	0.099	um
<b>1.25xMn.S.16</b>	Space between 1.25xMn in NCP direction when one or both width = 0.08um, 0.12um	$\geq$	0.08	um

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Rule number	Description	Opt.	Design Value	Unit
<b>1.25xMn.S.17</b>	Space between 1.25xMn (0.16um $\leq$ NCP direction width $<$ 0.2um and CP direction width $>$ 0.08um) and 1.25xMn edge (edge length $>$ 0.08um in CP direction) in NCP direction	$\geq$	0.099	um
<b>1.25xMn.S.18</b>	Space between 1.25xMn in NCP direction when one or both width $>$ 0.12um, PRL $\geq$ 0.121um	$\geq$	0.119	um
<b>1.25xMn.S.19</b>	Space between 1.25xMn (NCP direction width $\geq$ 0.2um and CP direction width $>$ 0.08um) and 1.25xMn edge (edge length $>$ 0.08um in CP direction) in NCP direction	$\geq$	0.139	um
<b>1.25xMn.S.20</b>	Space between 1.25xMn in NCP direction when one or both width $>$ 0.16um when PRL $>$ 0.2um	$\geq$	0.159	um
<b>1.25xMn.S.21</b>	Space between 1.25xMn and 1.25xMn line-end (width = 0.04/0.042um ) in NCP direction when PRL $>$ -0.04um	$\geq$	0.099	um
<b>1.25xMn.S.21a</b>	Space between 1.25xMn and 1.25xMn line-end (width = 0.044/0.046/0.06um) in NCP direction when PRL $>$ -0.04um	$\geq$	0.08	um
<b>1.25xMn.S.22</b>	Space between 1.25xMn and 1.25xMn line-end (0.06um $<$ width $\leq$ 0.08um) in NCP direction when PRL $>$ -0.08um	$\geq$	0.08	um
<b>1.25xMn.S.23</b>	Space between 1.25xMn line-end (width $<$ 0.08um) and U-shape inner edge (edge length $\leq$ 0.149um between two concave corners) in NCP direction	$\geq$	0.149	um
<b>1.25xMn.S.24a</b>	Space between 1.25xMn_Group_80 and 1.25xMn_Group_90 in CP direction when PRL $>$ -0.08um 1.25xMy_Group_80 definition: (((1.25xMy (width = 0.04um) su 0.02um) sd -0.04um) su 0.02um) 1.25xMy_Group_90 definition: 1) (((1.25xMy (width = 0.044um) su 0.023um) sd -0.046um) su 0.023um) 2) (((1.25xMy (width = 0.042um) su 0.024um) sd -0.048um) su 0.024um)	$\geq$	0.199	um
<b>1.25xMn.S.24b</b>	Space between 1.25xMn line-end inside 1.25xMn_Group_80 and 1.25xMy line-end of 1.25xMn_Group_90 in NCP direction when PRL $>$ - 0.199um	$\geq$	0.149	um
<b>1.25xMn.S.25</b>	Corner projected space between 1.25xMn when -0.08um $<$ PRL $\leq$ 0um, except line end-to-end (width $\leq$ 0.06um), Z-shape, and flag-shape. 1) Z-shape: edge length $>$ 0.04um between two consecutive	$\geq$	0.08	um

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Rule number	Description	Opt.	Design Value	Unit
	90-270 degree corners, corresponding width = 0.08um in NCP direction between two opposite edge length > 0.04um, not including T-shape)  2) Flag-shape: edge length > 0.04um between two consecutive 90-270 degree corners, the opposite edge length > 0.08um between two consecutive 90-90 degree corners, corresponding width = 0.08 um in NCP direction between these two opposite edge, and the other corresponding width > 0.04um in CP direction			
<b>1.25xMn.S.25a</b>	Corner space between two 1.25xMn in NCP direction when -0.04um < PRL ≤ 0um	≥	0.08	um
<b>1.25xMn.S.26</b>	At least one space between 1.25xMn edge (any adjacent edge of concave corner) and 1.25xMn, except either condition as below 1. Edge length between two concave corners < 0.12um. 2. Side edge length of concave corner < 0.042um	≥	0.119	um
<b>1.25xMn.S.27</b>	Space between 1.25xMy concave corner (both side edge length > 0.08um) and 1.25xMy line-end (width < 0.08um)	≥	0.154	um
<b>1.25xMn.S.28</b>	Forbidden the space between 1.25xMn (width = 0.04~0.046um and one side space = 0.04um) and 1.25xMn (width < 0.08um (W1)) in CP direction, except both side space of 1.25xMy (width < 0.08um) to 1.25xMy ≥ 0.1um	=	0.061~0.098, 0.131~0.178	um
<b>1.25xMn.S.29</b>	Forbidden space between 1.25xMy (width = 0.06~0.07um and one side space = 0.04um) and 1.25xMy (width < 0.08um) in CP direction, except both side space of 1.25xMy (width < 0.08um) to 1.25xMy ≥ 0.1um.	=	0.11~ 0.158	um
<b>1.25xMn.S.30</b>	Space between 1.25xMn and 45-degree bent 1.25xMn, DRC check 45-degree direction	≥	0.396	um
<b>1.25xMn.S.31</b>	Space between 1.25xMn and 1.25xVn-1 or 1.25xVn/10xTVn (maximum delta V > 1.155V) (1.05V + 10%)	≥	0.046	um
<b>1.25xMn.S.32</b>	Space between 1.25xMn and 1.25xVn-1 or 1.25xVn/10xTVn (maximum delta V > 1.32V) (1.2V + 10%)	≥	0.059	um
<b>1.25xMn.S.33</b>	Space between 1.25xMn and 1.25xVn-1 or 1.25xVn/10xTVn (maximum delta V > 1.98V) (1.8V + 10%)	≥	0.079	um
<b>1.25xMn.S.34</b>	Space between 1.25xMn and 1.25xVn-1 or 1.25xVn/10xTVn (maximum delta V > 3.63V) (3.3V + 10%)	≥	0.159	um

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Rule number	Description	Opt.	Design Value	Unit
<b>1.25xMn.S.35</b>	Space between two 1.25xMn (maximum delta V > 1.98V) (1.8V + 10%)	≥	0.046	um
<b>1.25xMn.S.36</b>	Space between two 1.25xMn (maximum delta V > 2.75V) (2.5V + 10%)	≥	0.079	um
<b>1.25xMn.S.37</b>	Space between two 1.25xMn (maximum delta V > 3.63V) (3.3V + 10%)	≥	0.104	um
<b>1.25xMn.S.37a</b>	Space between 1.25xMn line-end (width < 0.08um) and 1.25xMn (Maximum delta V > 3.63V) (3.3V + 10%) when PRL ≥ 0um	≥	0.135	um
<b>1.25xMn.L.1</b>	Length of 45-degree bent 1.25xMn, except MARKS	≥	0.905	um
<b>1.25xMn.L.2</b>	1.25xMn edge length when the adjacent edge length ≤ 0.089um, except two 0.08um edges form a convex corner.	≥	0.099	um
<b>1.25xMn.L.3</b>	1.25xMn edge length when the adjacent edge length < 0.04um	≥	0.119	um
<b>1.25xMn.L.4</b>	1.25xMn edge length when the adjacent line-end width < 0.06um	≥	0.159	um
<b>1.25xMn.L.5</b>	1.25xMn edge length when the adjacent line-end width < 0.08um	≥	0.109	um
<b>1.25xMn.L.6</b>	1.25xMn edge length between two consecutive 90-270 degree corners	≥	0.019	um
<b>1.25xMn.L.7</b>	1.25xMn edge length between two consecutive 90-270 degree corners with one adjacent line end edge width < 0.08um and the other adjacent edge > 0.07um	≥	0.238	um
<b>1.25xMn.L.8</b>	1.25xMn U-shape inner edge length between two consecutive 270-270 degree corners	≥	0.08	um
<b>1.25xMn.L.9</b>	Length of 1.25xMn metal branch (width ≤ 0.269um), when 1.Metal branch is connected to wide metal with width and length ≥ 0.398um 2.One square 1.25xVn -1/1.25xVn in metal branch, and space to wide metal ≤ 1.5um DRC flags branch that can't enclose a 0.08 um*1.5um orthogonal rectangle.	≥	1.5	um
<b>1.25xMn.L.10</b>	Length of 1.25xMn metal branch (width ≤ 0.269um), when	≥	3.6	um

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Rule number	Description	Opt.	Design Value	Unit
	1.Metal branch is connected to wide metal with width and length > 0.9um 2.one square 1.25xVn -1/1.25xVn in metal branch, and space to wide metal ≤ 3.6um DRC flags branch that can't enclose a 0.08 um*3.6um orthogonal rectangle.			
<b>1.25xMn.L.11</b>	Length of 1.25xMn metal branch (width ≤ 0.269um), when 1.Metal branch is connected to wide metal with width and length > 1.35um 2.one square 1.25xVn-1/1.25xVn in metal branch, and space to wide metal ≤ 9um DRC flags branch that can't enclose a 0.08 um*9um orthogonal rectangle.	≥	9	um
<b>1.25xMn.A.1</b>	1.25xMn area	≥	0.0148	um <sup>2</sup>
<b>1.25xMn.A.2</b>	1.25xMn area when all of edge lengths < 0.115um, except can fill a 0.05 um*0.13 um rectangle	≥	0.039	um <sup>2</sup>
<b>1.25xMn.A.3</b>	1.25xMn enclosed area	≥	0.181	um <sup>2</sup>
<b>1.25xMn.DN.1</b>	1.25xMn Density (window 50um*50um, stepping 25um), except LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions.	≥	10%	
<b>1.25xMn.DN.1a</b>	1.25xMn Density (window 50um*50um, stepping 25um), except the window not interact 3um*3um empty area, LOGO, MARKS, (OCOVL AND MnDUB), (NODMF su 1um) regions	≥	25%	
<b>1.25xMn.DN.2<sup>[R]</sup></b>	1.25xMn maximum density (window 50um*50um, stepping 25um), except dummy metal. DRC doesn't check (1.25xMn AND DUPMK1) region when the 1.25xMn layer is used as TM-1.	≤	65%	
<b>1.25xMn.DN.3</b>	Maximum 1.25xMn density (window 50um*50um, stepping 25um). DRC doesn't check (1.25xMn AND DUPMK1) region when the 1.25xMn layer is used as TM-1.	≤	75%	
<b>1.25xMn.DN.4</b>	1.25xMn density difference between two neighboring checking windows (window 180um*180um, stepping 180um), except (NODMF) su 0.4um region	≤	50%	
<b>1.25xMn.DN.6</b>	It is not allowed to have local density < 5% of all 3 consecutive metal layers over any 30um*30um window (stepping 15um),			

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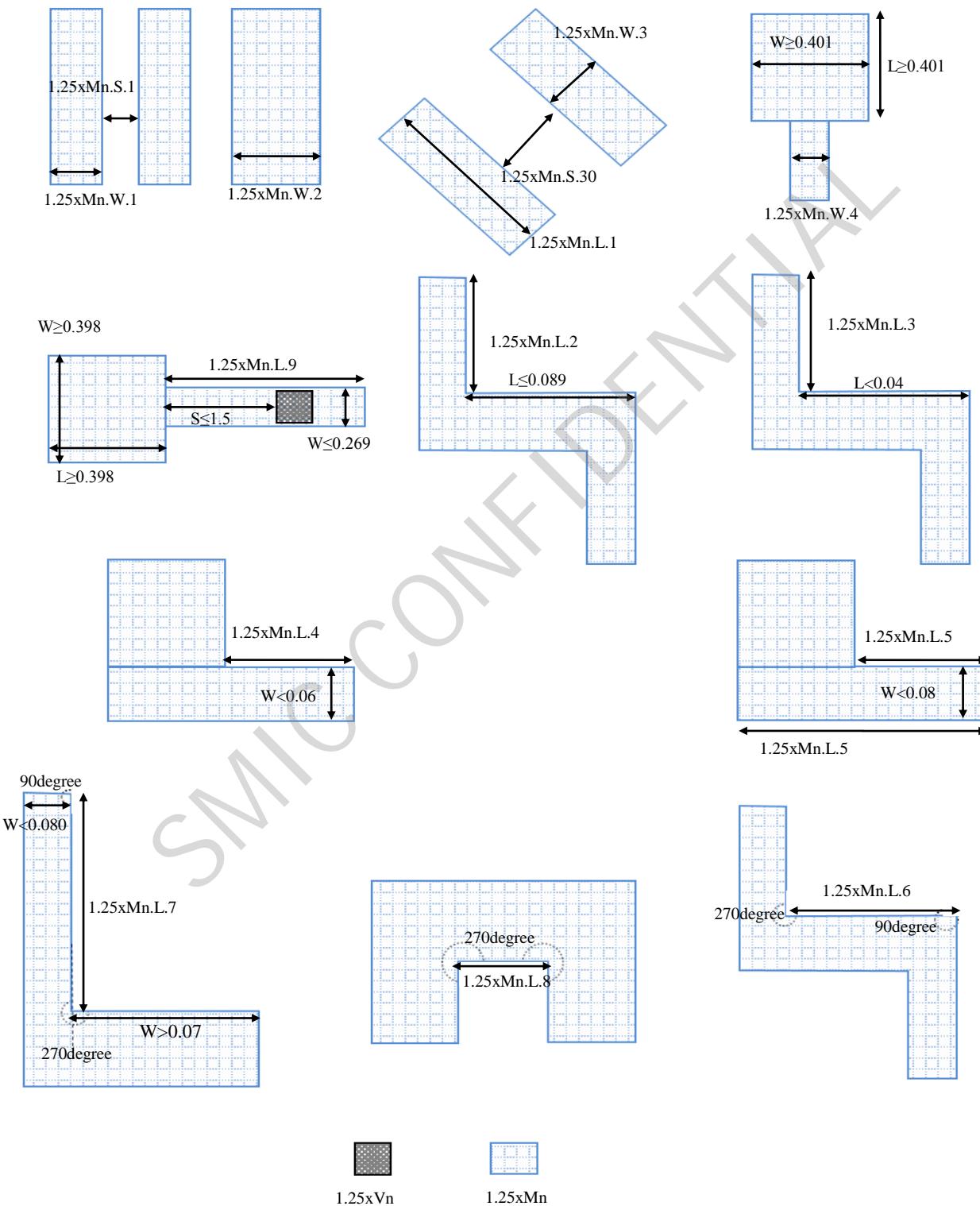
Rule number	Description	Opt.	Design Value	Unit
	except (NODMF) su 0.4um region			
<b>1.25xMn.R.1<sup>[NC]</sup></b>	1.25xMn pattern must drawn on data type 50 or 55.			
<b>1.25xMn.R.2<sup>[NC]</sup></b>	It is not allowed for data type 50 and 55 exist on the same metal layer at the same time.			
<b>1.25xMn.R.3<sup>[NC]</sup></b>	M5/M7 must be drawn on data type 55, M6/M8 must be drawn on data type 50, 1.25xMn and 1.25xMn-1 using same data type is not allowed.			
<b>1.25xMn.R.4</b>	It is not allowed for maximum delta V $\geq 5.6V$ , when space between 1.25xMn and 1.25xMn/1.25xVn-1/1.25xVn is < 0.36um			

Note:

1. CP direction means the direction along the minimum pitch (80nm) of 1.25xMn; NCP direction means the direction vertical to CP direction.
2. Data Type 40 is used for the direction of the minimum pitch of 1.25xMy parallel to Poly direction of core device.
3. Data Type 45 is used for the direction of the minimum pitch of 1.25xMy vertical to Poly direction of core device.
4. Data Type 50 is used for the direction of the minimum pitch of 1.25xMn parallel to Poly direction of core device.
5. Data Type 55 is used for the direction of the minimum pitch of 1.25xMn vertical to Poly direction of core device.
6. Line end width means edge length between two consecutive 90-90 degree corners of 1.25xMn.
7. Via enclosure by 1.25xMn should be as large as the layout allows.

It is recommended that the lengths of metal lines are orthogonal to the lengths of metal lines on neighboring layers.

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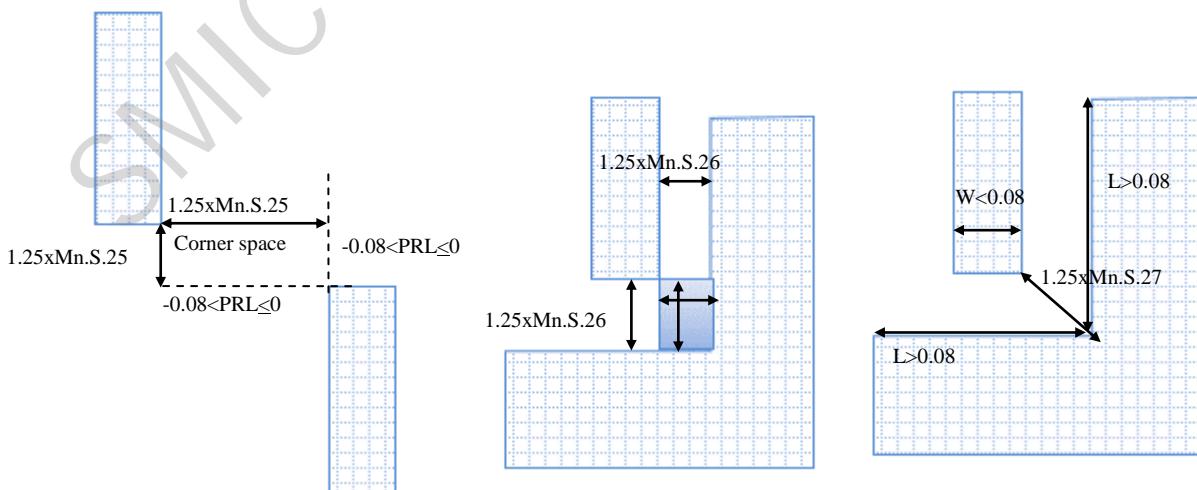
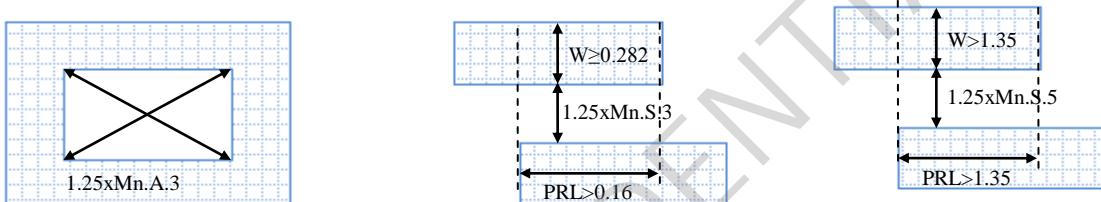
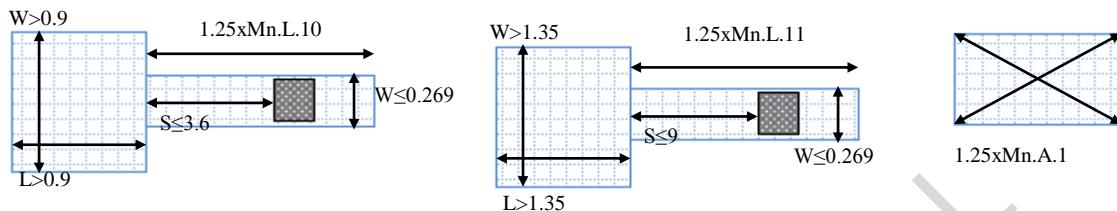


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$1.25 \times \text{Vn}$      
  $1.25 \times \text{Mn}$

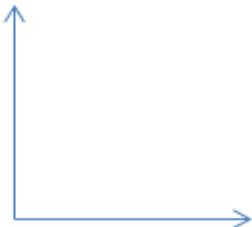
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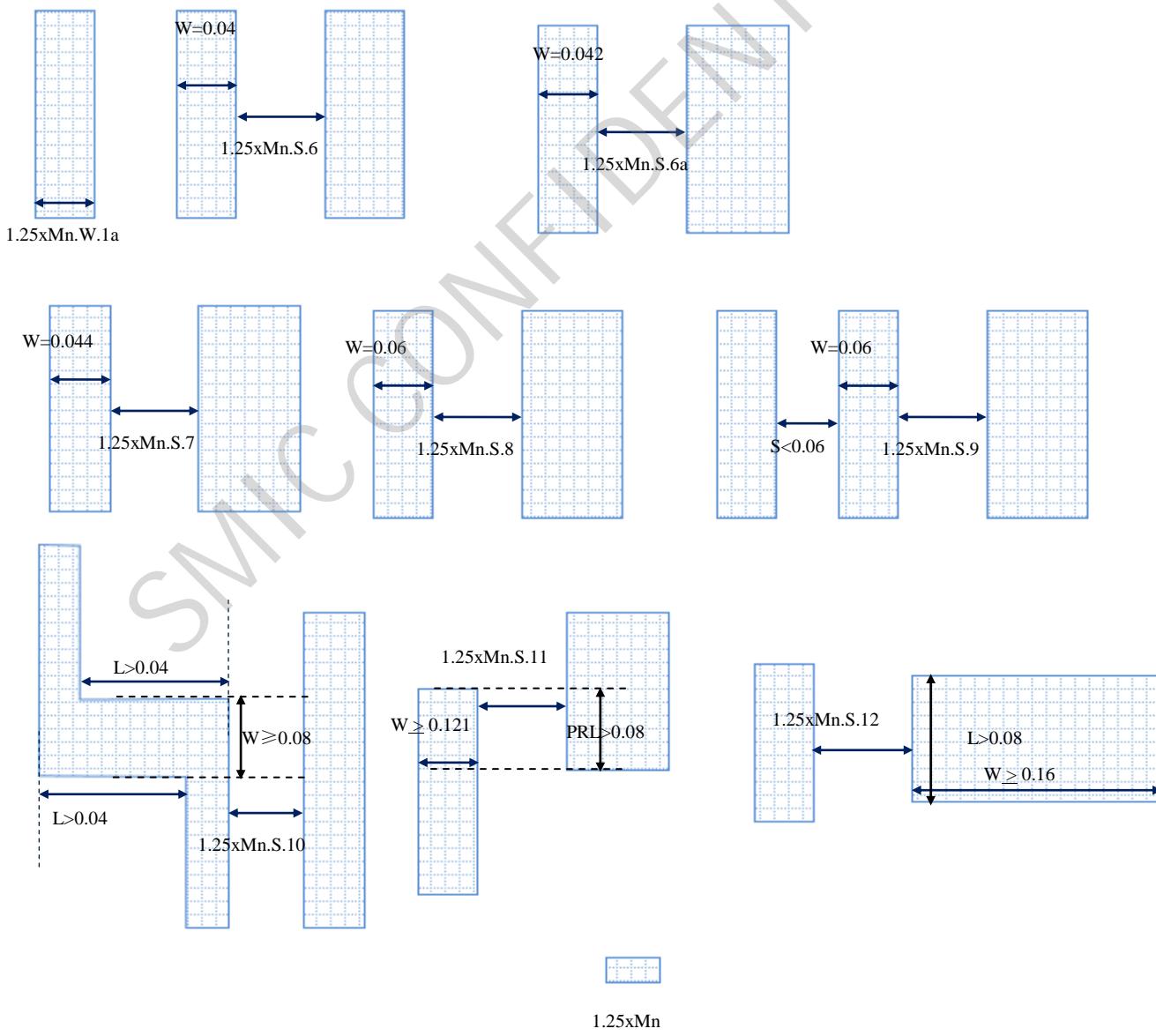
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NCP direction



CP direction

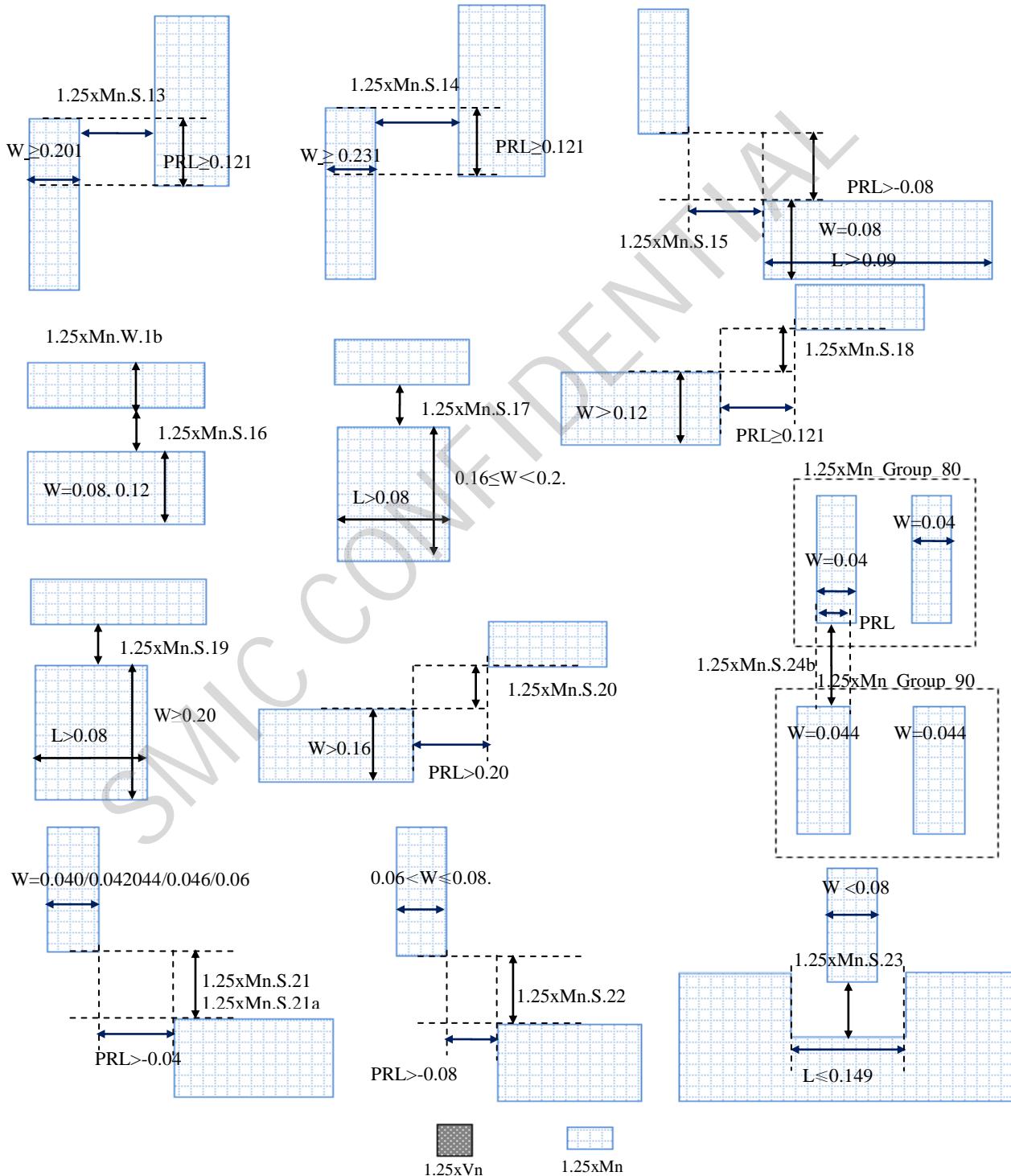


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#### 7.2.41 2xVn (BV1/BV2) design rules

Rule number	Description	Opt.	Design Value	Unit
<b>2xVn.W.1</b>	Square 2xVn size, except MARKS, MARKG, INDMY and LOGO regions	=	0.062	um
<b>2xVn.W.2</b>	2xVn bar width in MARKG and MARKS regions	=	0.1, 0.45	um
<b>2xVn.S.1</b>	2xVn space, except the space between 2xVn bar inside MARKS	≥	0.064	um
<b>2xVn.S.2</b>	Space between 2xVn when (maximum delta V > 3.63V) (3.3V + 10%)	≥	0.178	um
<b>2xVn.S.3</b>	Space between 2xVn and its neighboring 2xVn (T). The definition of neighboring 2xVn (T) : 1) 2xVn (T) is in a 2xVn group 2) The number of this 2xVn group is ≥ 4, there are at least 3 2xVn s neighboring to 2xVn (T) 3) The space between 2xVn (T) to other 2xVn s in this group < 0.09um	≥	0.081	um
<b>2xVn.S.4</b>	2xVn space at different net	≥	0.081	um
<b>2xVn.S.5</b>	2xVn space at different net when PRL > 0um	≥	0.098	um
<b>2xVn.S.6</b>	Space between 2xVn bar and 2xVn, except the space between 2xVn bar inside MARKS	≥	0.34	um
<b>2xVn.S.7</b>	Space between 2xVn bars, DRC only check the space between parallel edges when the 2xVn bar is inside MARKS	≥	0.55	um
<b>2xVn.EN.1</b>	2xVn must be fully covered by 1.25xMn or 2xMn where 1.25xMn/2xMn is the metal layer directly underneath 2xVn; Enclosure by 1.25Mn/2xMn is defined by 2xVn.EN.3 or 2xVn.EN.4, enclosure by 1.25xMn is defined by 2xVn.EN.5			
<b>2xVn.EN.2</b>	2xVn bar enclosure by 1.25xMn/2xMn	≥	0.098	um
<b>2xVn.EN.3</b>	2xVn enclosure by 2x Mn when enclosure by 2x Mn on either perpendicular direction ≥ 0um	≥	0.026	um
<b>2xVn.EN.4</b>	2xVn enclosure by 2x Mn when enclosure by 2x Mn on either perpendicular direction ≥ 0.009um	≥	0.017	um
<b>2xVn.EN.5</b>	2xVn enclosure by 1.25x Mn when enclosure by 1.25x Mn on either perpendicular direction ≥ 0.02um	≥	0.026	um

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Rule number	Description	Opt.	Design Value	Unit
<b>2xVn.EN.6</b>	2xVn bar enclosure by 2xMn+1, where 2xMn+1 is the metal layer directly above 2xVn bar	$\geq$	0.098	um
<b>2xVn.EN.7</b>	2xVn must be fully covered by 2xMn+1, where 2xMn+1 is the metal layer directly above 2xVn; Enclosure by 2xMn+1 is defined by either 2xVn.EN.8 or 2xVn.EN.9			
<b>2xVn.EN.8</b>	2xVn enclosure by 2x Mn+1 when enclosure by 2x Mn+1 on either perpendicular direction $\geq 0$ um, except MARKS region	$\geq$	0.026	um
<b>2xVn.EN.9</b>	2xVn enclosure by 2x Mn+1 when enclosure by 2x Mn+1 on either perpendicular direction $\geq 0.009$ um, except MARKS region.	$\geq$	0.017	um
<b>2xVn.R.1</b>	45-degree rotated 2xVn is not allowed.			
<b>2xVn.R.2</b>	Single 2xVn is not allowed in "H-shape" 2xMn+1 when: 1. The 2xMn+1 has "H-shape" interact with two metal holes: both two metal holes length $\leq 4.5$ um (L2) and two metal hole area $\leq 4.05$ um <sup>2</sup> . 2. The 2xVn overlaps on the center metal bar of this "H-shape" 2xMn+1. 3. The center metal bar width $\leq 0.18$ um and length $\leq 0.9$ um (L).			
<b>2xVn.R.3</b>	At least two 2xVn with space $\leq 0.127$ um (S1), or at least four 2xVn with space $\leq 0.57$ um (S1') be used to connect 1.25xMn/2xMn and 2xMn+1 when one of these two metals has width and length $> 0.19$ um (W1), except VIA bar, OCCD region			
<b>2xVn.R.4</b>	At least four 2xVn with space $\leq 0.127$ um (S2), or at least nine 2xVn with space $\leq 0.75$ um (S2') be used to connect intersection region of 1.25xMn/2xMn and 2xMn+1 when one of these two metals has width and length $> 0.5$ um (W1), except VIA bar, OCCD region.			
<b>2xVn.R.5</b>	At least two 2xVns when either wide metal of 1.25xMn, 2xMn or 2xMn+1 with both width W and length L $> 0.19$ um, and the distance D $\leq 1$ um away from this wide metal. DRC flags each intersecting area (bottom metal AND upper metal) with single square Via within the branch check region			
<b>2xVn.R.6</b>	At least two 2xVns when either wide metal of 1.25xMn, 2xMn or 2xMn+1 with both width W and length L $> 1.27$ um, and the distance D $\leq 2.5$ um away from this wide metal. DRC flags each intersecting area (bottom metal AND upper metal) with single square Via within the branch check region			

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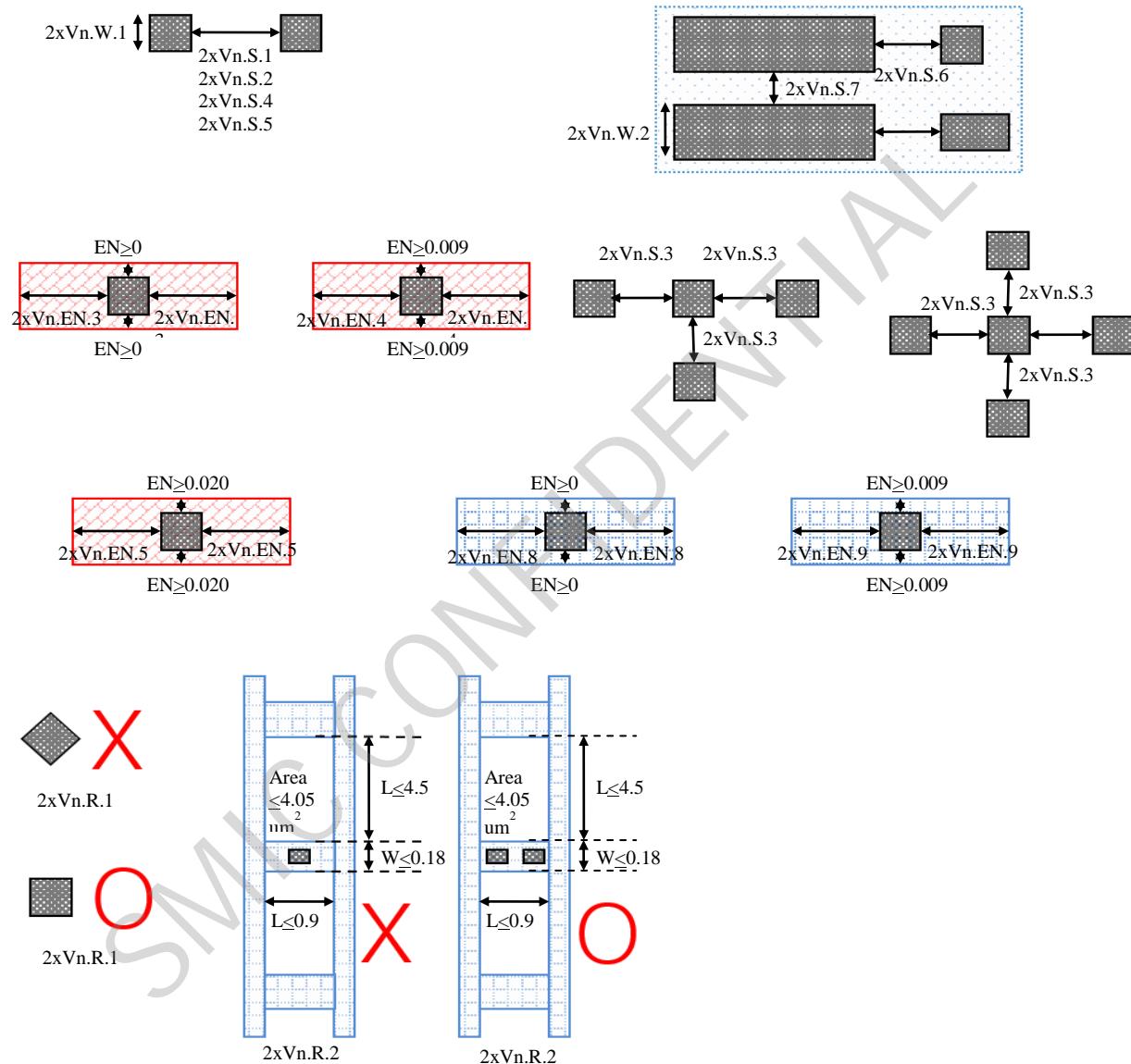
Rule number	Description	Opt.	Design Value	Unit
<b>2xVn.R.7</b>	At least two 2xVns when either wide metal of 1.25xMn, 2xMn or 2xMn+1 with both length L > 6.33um and width W > 1.9um, and the distance D $\leq$ 6.35um away from this wide metal. DRC flags each intersecting area (bottom metal AND upper metal) with single square Via within the branch check region			
<b>2xVn.R.8</b>	Maximum delta V $\geq$ 5.6V is not allowed, when space between 2xVn is < 0.410um			
<b>2xVn.R.9</b>	Vn connected to 2xMnDUM, 2xMn+1 Dummy is not allowed, except LOGO region.			
<b>2xVn.R.10</b>	It's not allowed 2xVn overlap with the metal resistor directly underneath and above the 2xVn			

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#### 7.2.42 2xMn (B1/B2) design rules

Rule number	Description	Opt.	Design Value	Unit
<b>2xMn.W.1</b>	2xMn width	$\geq$	0.062	um
<b>2xMn.W.2</b>	2xMn width, except MARKS and LOGO regions	$\leq$	4.1	um
<b>2xMn.W.3</b>	45-degree 2xMn width	$\geq$	0.152	um
<b>2xMn.S.1</b>	Space between 2xMn	$\geq$	0.064	um
<b>2xMn.S.2</b>	Space between 2xMn (maximum delta V > 3.63V) (3.3V + 10%)	$\geq$	0.08	um
<b>2xMn.S.3</b>	Space between 2xMn, when both metal width is > 0.198um and PRL > 0.27um	$\geq$	0.089	um
<b>2xMn.S.5</b>	Space between 2xMn, when one or both metal width is > 0.63um and PRL > 0.54um	$\geq$	0.108	um
<b>2xMn.S.6</b>	Space between 2xMn when one metal width is > 0.198um and other metal width is > 0.63um, and PRL > 0.54um	$\geq$	0.126	um
<b>2xMn.S.7</b>	Space between 2xMn when one or both metal width is > 1.35um and PRL > 1.35um	$\geq$	0.27	um
<b>2xMn.S.8</b>	Space between 2xMn and 2xMn line-end (width < 0.09um), except extrusion F < 0.063um  The space can be line end head or to other 2xMn or line end side to other 2xMn. Rule check: S $\geq$ (Dh or Ds). E1 = 0.027um, K1= 0.0855um, Dh = Ds = 0.089um in the illustration.	$\geq$	0.089	um
<b>2xMn.S.9</b>	Space between 2xVn and 2xMn (B) (except extrusion F < 0.063um), when: 1. 2xVn enclosure by 2xMn (A) line end: E < 0.045um, W < 0.09um 2. PRL between 2xMn (A) and 2xMn (B): $\geq$ -0.027um 3. Space Ss between 2xMn (A) and the neighboring parallel metal line < 0.072um (Ds) 4. Any one edge distance from the corner of the two edges of 2xMn (A): < 0.0855um (K1) Rule check: Ss < Ds, E1 = 0.027, K1 = 0.0855um, Dh = 0.152um, Ds = 0.072um in the illustration. At least one 2xVn in the 2xMn(A) and 2xMn-1 intersection meet this rule is ok.	$\geq$	0.152	um
<b>2xMn.S.10</b>	Space between 45-degree 2xMn and parallel 2xMn when PRL > 0	$\geq$	0.152	um

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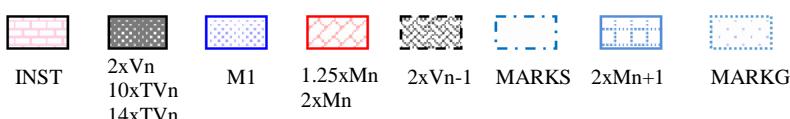
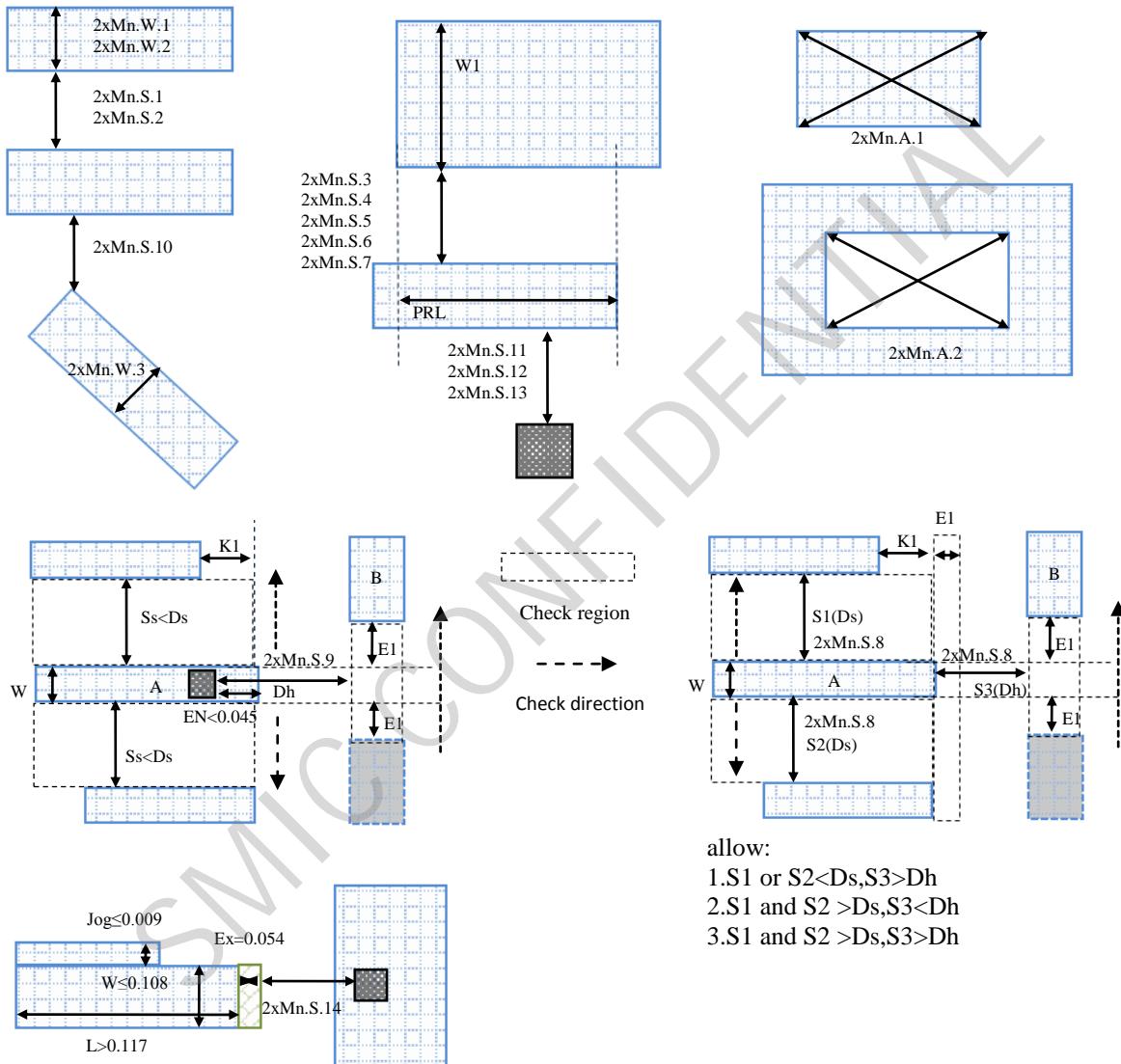
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Rule number	Description	Opt.	Design Value	Unit
	um			
<b>2xMn.S.11</b>	Space between 2xMn and 2xVn+1 or 2xVn/10xVn/14xVn (maximum delta V > 1.65V) (1.5V+10%)	≥	0.071	um
<b>2xMn.S.12</b>	Space between 2xMn and 2xVn+1 or 2xVn/10xVn/14xVn (maximum delta V > 1.98V) (1.8V+10%)	≥	0.089	um
<b>2xMn.S.13</b>	Space between 2xMn and 2xVn+1 or 2xVn/10xVn/14xVn (maximum delta V > 3.63V) (3.3V+10%)	≥	0.161	um
<b>2xMn.S.14</b>	Space between 2xMn line-end (width ≤ 0.108um and two adjacent edge length ≥ 0.117um) extend 0.054um and 2xVn (maximum delta V > 3.63V) (3.3V+10%), except small jog ≤ 0.009um	≥	0.134	um
<b>2xMn.A.1</b>	2xMn area	≥	0.0196	um <sup>2</sup>
<b>2xMn.A.2</b>	2xMn enclosed area	≥	0.161	um <sup>2</sup>
<b>2xMn.DN.1</b>	2xMn density (window 112um*112um, stepping 56um), except INDMY, LOGO regions	≥	10%	
<b>2xMn.DN.2</b>	2xMn density (window 112um*112um, stepping 56um), except INDMY region	≤	85%	
<b>2xMn.DN.3a</b>	2xMn density (window 760um*760um, stepping 380um)	≤	70%	
<b>2xMn.DN.3b</b>	Full chip 2xMn density	≥	20%	
<b>2xMn.DN.4</b>	2xMn density (window 72um*72um, stepping 36um), except (NODMF) su 0.4um region	≥	1%	
<b>2xMn.DN.5</b>	2xMn density difference (window 180um*180um, stepping 180um), except (NODMF) su 0.4um region	≤	50%	
<b>2xMn.DN.6</b>	It is not allowed to have local density < 5% of all 3 consecutive metal (1.25xMy/1.25Mn, 2xMn, 2xMn+1) over any window 30*30um (stepping 15um). The metal layers include M1/Mn and dummy metals, except (NODMF) su 0.4um region			
<b>2xMn.R.1<sup>[NC]</sup></b>	2xMn line-end must be rectangular.			

<b>2xMn.R.2</b>	Maximum delta V ≥ 5.6V is not allowed, when space between 2xM1 and 2xM1/2xVn-1/2xVn is < 3.6um			
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### 7.2.43 10xTVn (TV1/TV2) Via design rules

Rule number	Description	Opt.	Design Value	Unit
<b>10xTVn.W.1</b>	Square 10xTVn size, except MARKS and MARKG regions	=	0.324	um
<b>10xTVn.S.1</b>	Space between 10x TVns.	$\geq$	0.306	um
<b>10xTVn.S.2</b>	Space between 10x TVn and its neighboring 10xTVn (T). The definition of neighboring 10x TVn (T) : 1) 10xTVn (T) is in a 10x TVn group 2) The number of 10x TVn group is $\geq 4$ , there are at least 3 10x TVn s neighboring to 10xTVn (T) 3) The space between 10x TVn (T) to other 10x TVn s in this group < 0.504um	$\geq$	0.484	um
<b>10xTVn.EN.1</b>	10xTVn must be fully enclosed by 1.25xMn, 2xMn, 10xTMn-1, MIM, or CTOP, and must follow 10xTVn.EN.2a 10xTVn. EN.2b, MIM.3 or CTOP.5, where 1.25xMn, 2xMn, 10xTMn-1, MIM, or CTOP is the metal layer directly underneath 10xTVn.			
<b>10xTVn.EN.2a</b>	10x TVn must be fully enclosed by 1.25xMn, 2xMn, 10xTMn-1	$\geq$	0.018	um
<b>10xTVn.EN.2b</b>	10xTVn enclosure by 1.25xMn, 2xMn, 10xTMn-1 for two opposite sides with the other two sides $\geq 0.018\text{um}$	$\geq$	0.071	um
<b>10xTVn.EN.3</b>	10xTVn must be fully enclosed by 10xTMn and must follow 10xTVn.EN.4a, 10xTVn.EN.4b as below; 10xTMn is the metal layer directly above 10xTVn.			
<b>10xTVn.EN.4a</b>	10x TVn fully enclosure by 10x TMn	$\geq$	0.018	um
<b>10xTVn.EN.4b</b>	10xTVn enclosure by 10x TMn for two opposite sides with the other two sides $\geq 0.018\text{um}$	$\geq$	0.071	um
<b>10xTVn.R.1</b>	10x TVn and 14xTVn can't be used on same chip.			
<b>10xTVn.R.2</b>	45-degree rotated 10xTVn is not allowed.			
<b>10xTVn.R.3</b>	There should be at least two 10x TVns with space $\leq 1.54\text{um}$ (S1) in 1.25xMn, 2xMn, 10xTMn-1 and 10xTMn intersection area, when either 1.25xMn, 2xMn, 10xTMn-1 and 10xTMn width and length (W1) $> 1.63\text{um}$ .			
<b>10xTVn.R.4</b>	There should be at least two 10x TVns in the intersection area of 1.25xMn, 2xMn, 10xTMn-1 and 10xTMn, when either wide metal of 1.25xMn, 2xMn, 10xTMn-1 and 10xTMn with both width W $> 2.75\text{um}$ and length L $> 9.1\text{um}$ , the space between either via and wide metal is $\leq 5.4\text{um}$ (D3, D3 is the shortest running path length)			

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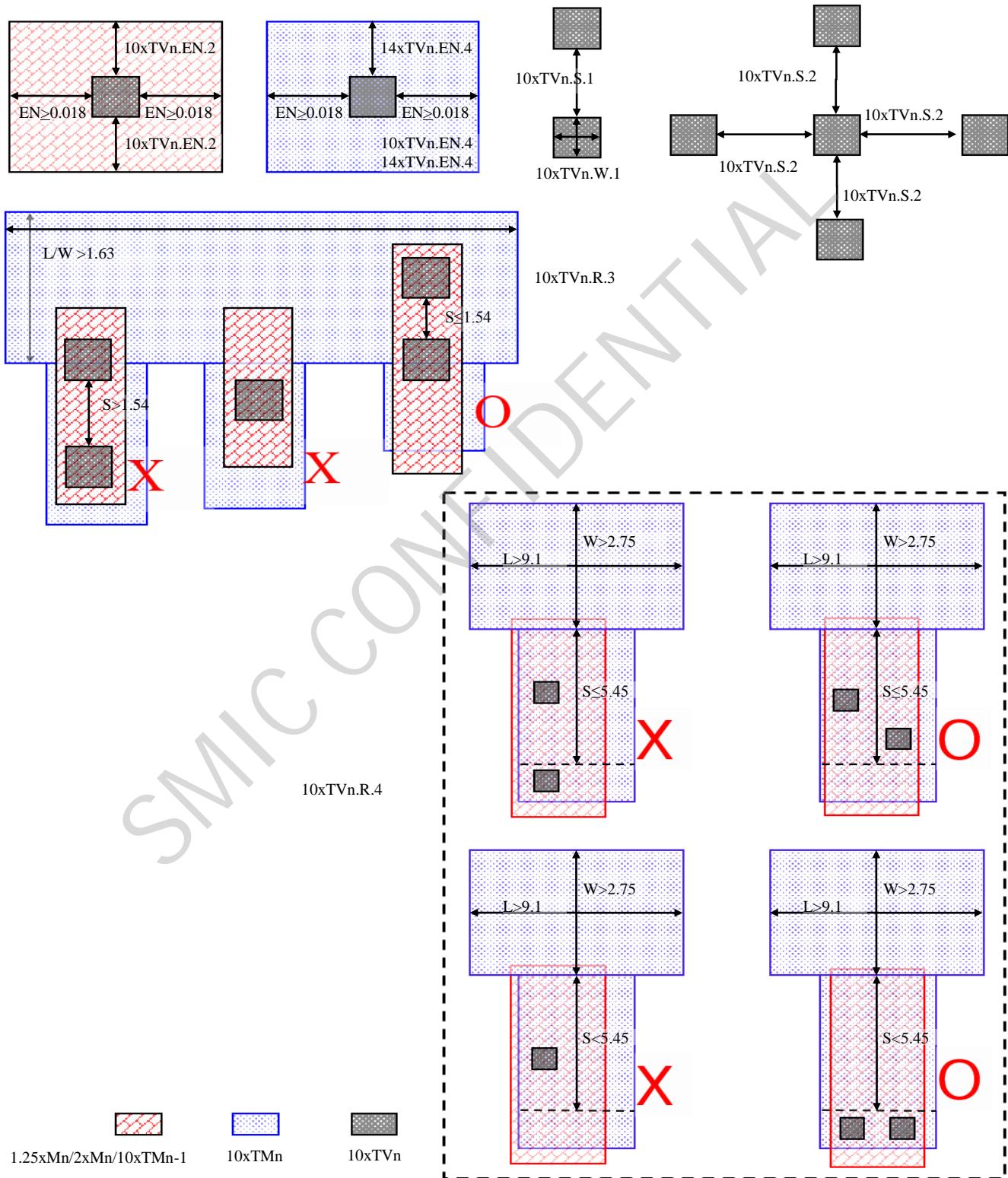
Rule number	Description	Opt.	Design Value	Unit
	from 10xTVn to the wide metal). DRC flags each intersecting area ((bottom metal AND upper metal)) with single square Via within the branch check region			
<b>10xTVn.R.5</b>	It is not allowed for maximum delta V $\geq$ 5.6V, when space between 10xTVn is < 0.410um			
<b>10xTVn.R.6</b>	10xTVn must be drawn on data type of 0.			
<b>10xTVn.R.7</b>	It's not allowed 10x TVn overlap with the metal resistor directly underneath and above the 10x TVn			
<b>10xTVn.R.8<sup>[NC]</sup></b>	Recommend to use redundant vias to avoid high Rc wherever layout allows.			

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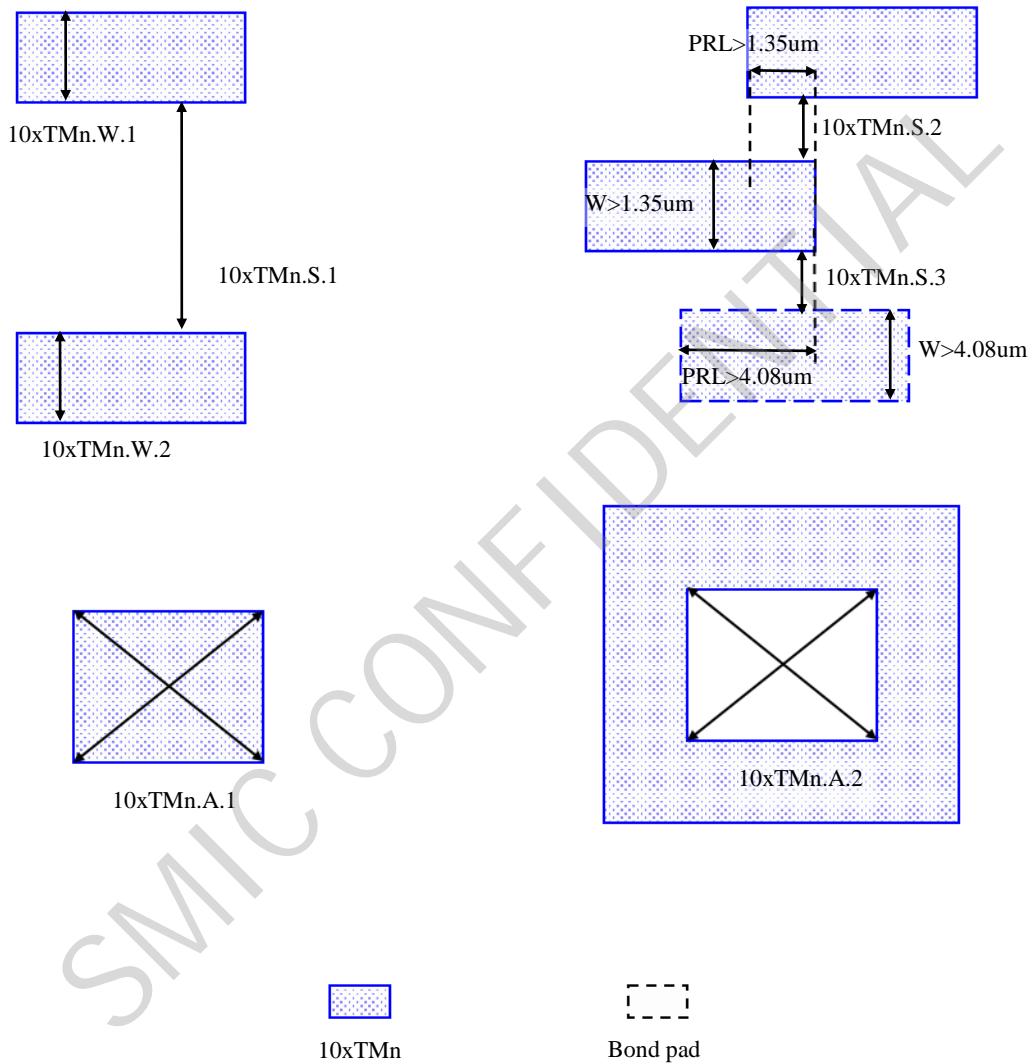
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#### 7.2.44 10xTMn (TM1/TM2) design rules

Rule number	Description	Opt.	Design Value	Unit
<b>10xTMn.W.1</b>	10xTMn width.	$\geq$	0.36	um
<b>10xTMn.W.2</b>	10xTMn width, except AL pad, DUPMK1 and INDMY regions	$\leq$	11	um
<b>10xTMn.S.1</b>	Space between 10xTMns, except LOGO region	$\geq$	0.36	um
<b>10xTMn.S.2</b>	Space between two 10x TMNs when one or both 10x TMn widths are > 1.35um and PRL > 1.35um.	$\geq$	0.448	um
<b>10xTMn.S.3</b>	Space between two 10x TMNs when one or both 10x TMn widths is > 4.08um and PRL > 4.08um	$\geq$	1.33	um
<b>10xTMn.A.1</b>	10xTMn area	$\geq$	0.453	um <sup>2</sup>
<b>10xTMn.A.2</b>	10xTMn enclosed area	$\geq$	0.463	um <sup>2</sup>
<b>10xTMn.DN.1</b>	10xTMn density (window 112um*112um, stepping 56um), except DUPMK1, PAD, INDMY, LOGO regions	$\geq$	10%	
<b>10xTMn.DN.2</b>	10xTMn density (window 112um*112um, stepping 56um), except DUPMK, PAD, LOGO regions	$\leq$	85%	
<b>10xTMn.DN.3</b>	10xTMn density difference between any two neighboring checking windows (window 180um*180um, stepping 180um), except NODMF su 0.4um region.	$\leq$	50%	
<b>10xTMn.DN.4</b>	10xTMn full chip density	$\geq$	20%	
<b>10xTMn.R.1</b>	10xTMn must be drawn on data type of 0.			
<b>10xTMn.R.2</b>	10x TMn and 14xTMn can't be used on same chip.			
<b>10xTMn.R.3</b>	Maximum delta V $\geq$ 5.6V is not allowed, when space between 10xTMn and 10xTMn/10xTVn-1/10xTVn is < 3.6um			
<b>10xTMn.R.4<sup>[NC]</sup></b>	10xMn line-end must be rectangular.			
<b>10xTMn.R.5</b>	10xTM1 exist in a chip without (10xTM2 OR UTM) is not allowed.			

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### 7.2.45 14xTVn (TV1/TV2) design rules

Rule number	Description	Opt.	Design Value	Unit
<b>14xTVn.W.1</b>	Square 14xTVn size, except MARKS and MARKG regions	=	0.414	um
<b>14xTVn.S.1</b>	Space between single 14xTVns.	≥	0.396	um
<b>14xTVn.S.2</b>	Space between 14xTVn and its neighboring 14xTVn (T). The definition of neighboring 14x TVn (T) : 1) 14xTVn (T) is in a 14x TVn group 2) The number of this 14x TVn group is ≥ 4, there are at least 3 14x TVn s neighboring to 14x TVn (T) 3) The space between 14x TVn (T) to other 14x TVn s in this group ≤ 0.592um	≥	0.592	um
<b>14xTVn.S.3</b>	Space between 14x TVns in 2x2 14x TVns array at the same net. Two vias whose space ≤ 0.592um are considered to be in the same array. DRC check method: identify 2x2 14x TVns array at the same net, then check space.	≥	0.484	um
<b>14xTVn.EN.1</b>	14xTVn must be fully covered by 1.25xMn, 2xMn, 10xTMn or 14xTMn-1, MIM, or CTOP where 1.25xMn, 2xMn, 10xTMn or 14xTMn-1, MIM, or CTOP is the metal layer directly underneath 14xTVn. Enclosure by 1.25xMn, 2xMn, 10xTMn or 14xTMn-1, MIM, or CTOP must follow 14xTVn.EN.2, 14xTVn.EN.2a, MIM.3 or CTOP.5			
<b>14xTVn.EN.2a</b>	14xTVn enclosure by 1.25xMn, 2xMn, 10xTMn or 14xTMn-1, where 1.25xMn, 2xMn, 10xTMn or 14xTMn-1 is the metal layer directly underneath 14x TVn. 14x TVn must be fully covered by 1.25xMn, 2xMn, 10xTMn or 14xTMn-1	≥	0.018	um
<b>14xTVn.EN.2</b>	14xTVn enclosure by 1.25xMn, 2xMn, 10xTMn or 14xTMn-1 when enclosure by 1.25xMn, 2xMn, 10xTMn or 14xTMn-1 on either perpendicular direction ≥ 0.018um, and 1.25xMn, 2xMn, 10xTMn or 14xTMn-1 is the metal layer directly underneath 14x TVn.	≥	0.071	um
<b>14xTVn.EN.3</b>	14xTVn must be fully covered by 14xTMn, where 14xTMn is the metal layer directly above 14xTVn. Enclosure by 14xTMn must follow 14xTVn.EN.4 as below			
<b>14xTVn.EN.4a</b>	14xTVn enclosure by 14x TMn, where 14x TMn is the metal layer directly above 14x TVn. 14x TVn must be fully enclosed by 14x TMn	≥	0.018	um

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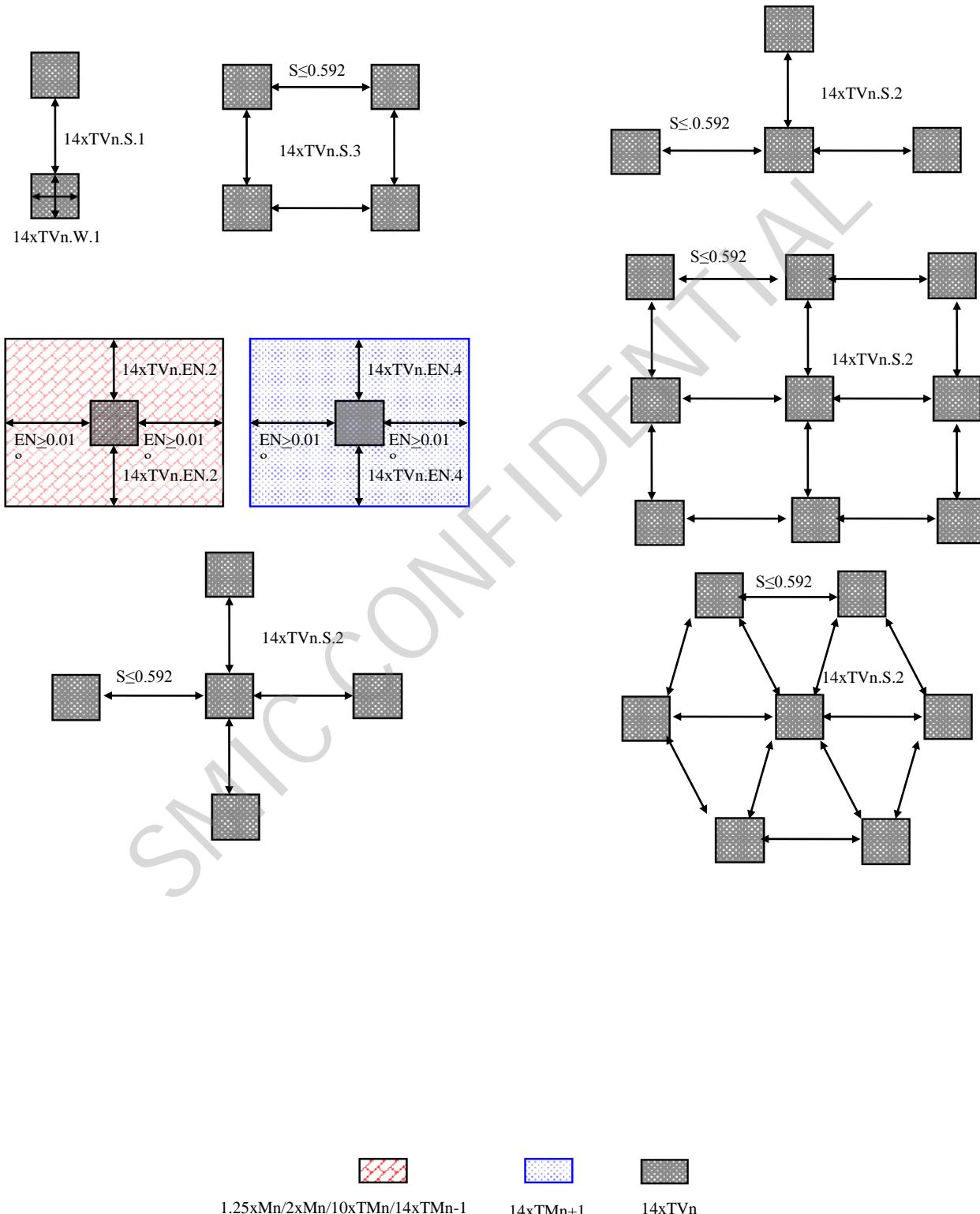


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Rule number	Description	Opt.	Design Value	Unit
<b>14xTVn.EN.4</b>	14xTVn enclosure by 14x TMn when enclosure by 14x TMn on either perpendicular direction $\geq 0.018\text{um}$ , and 14x TMn is the metal layer directly above 14xTVn.	$\geq$	0.071	um
<b>14xTVn.R.1</b>	14xTVn pattern must be drawn on data type 40.			
<b>14xTVn.R.2</b>	45-degree rotated 14xTVn is not allowed.			
<b>14xTVn.R.3</b>	At least two 14xTVns with space $\leq 1.54\text{um}$ (S1) in 1.25xMn, 2xMn/10xTMn or 14xTMn-1 and 14xTMn intersection area, when either 1.25xMn, 2xMn/10xTMn/14xTMn-1 and 14xTMn width and length (W1) $> 1.63\text{um}$ .			
<b>14xTVn.R.4</b>	There should be at least two 14xTVn in the intersection area of 1.25xMn, 2xMn/10xTMn or 14xTMn-1 and 14xTMn, when either wide metal of 1.25xMn, 2xMn/10xTMn /14xTMn-1 and 14xTMn with both length L $> 9.1\text{um}$ and width W $> 2.75\text{um}$ , the space between either via and wide metal is $\leq 5.4\text{um}$ (D3, D3 is the distance 5.4um away from this wide metal).  DRC flags each intersecting area ((bottom metal AND upper metal)) with single square Via within the branch check region			
<b>14xTVn.R.5</b>	It is not allowed for maximum delta V $\geq 5.6\text{V}$ , when space between 14xTVn is $< 0.410\text{um}$			
<b>14xTVn.R.6</b>	It's not allowed 14x TVn overlap with the metal resistor directly underneath and above the 14x TVn.			
<b>14xTVn.R.7<sup>[NC]</sup></b>	Recommend to use redundant vias to avoid high Rc wherever layout allows.			

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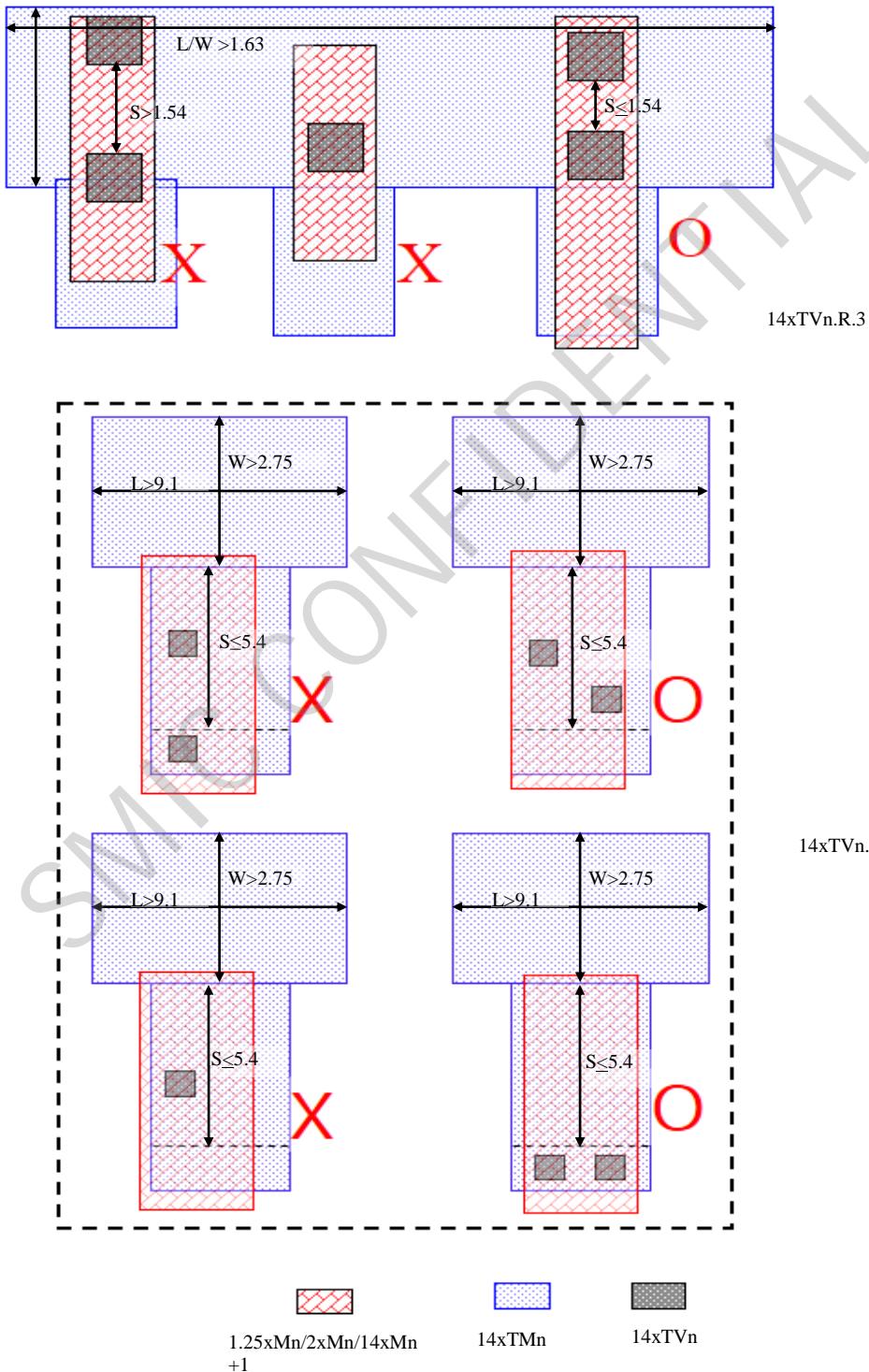


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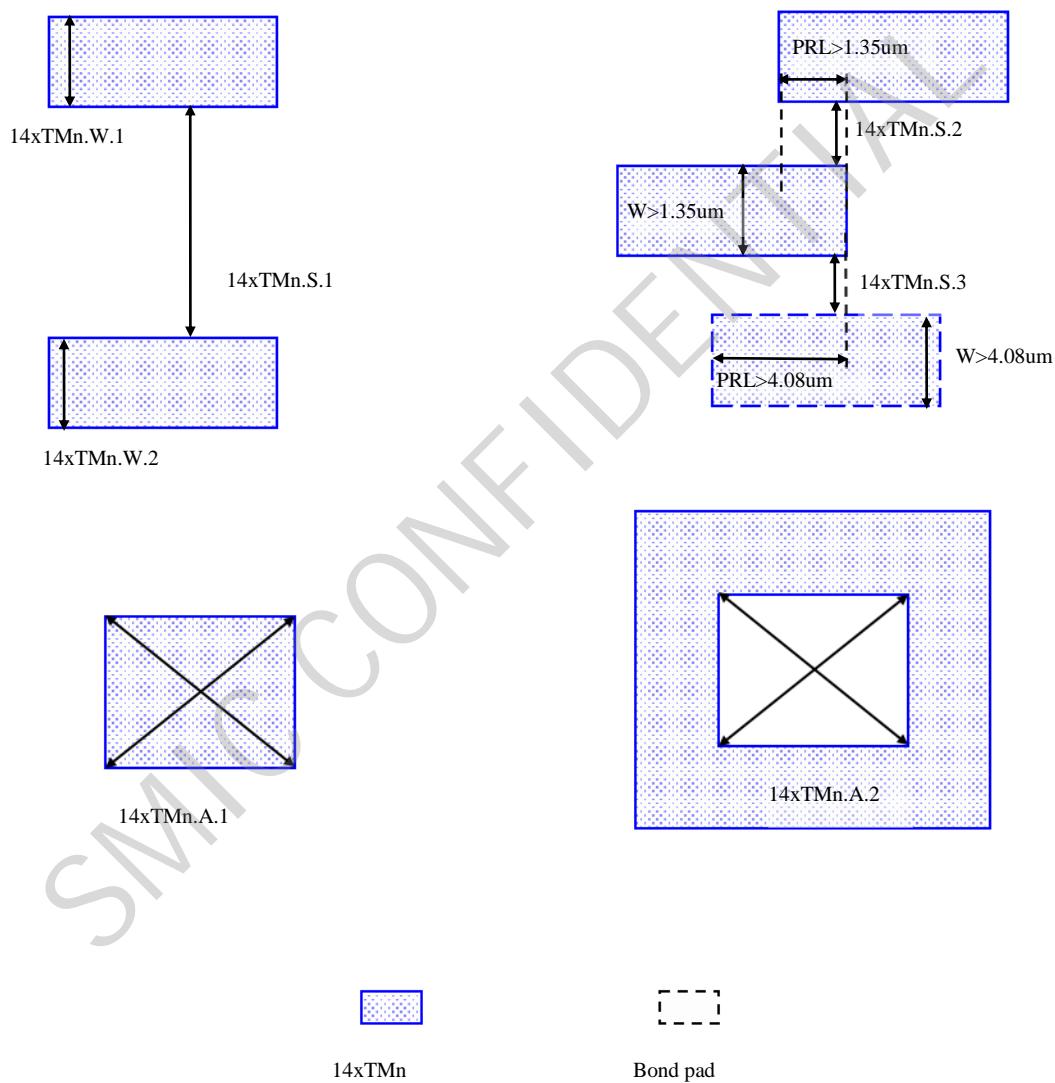
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#### 7.2.46 14xTMn (TM1/TM2) design rules

Rule number	Description	Opt.	Design Value	Unit
<b>14xTMn.W.1</b>	14xTMn width.	$\geq$	0.45	um
<b>14xTMn.W.2</b>	14xTMn width, except AL pad, DUPMK1 and INDMY regions.	$\leq$	11	um
<b>14xTMn.S.1</b>	Space between 14xTMns.	$\geq$	0.45	um
<b>14xTMn.S.2</b>	Space between 14xTMns when one or both 14x TMn width is > 1.35um and PRL > 1.35um.	$\geq$	0.584	um
<b>14xTMn.S.3</b>	Space between 14xTMns when one or both 14x TMn width is > 4.08um and PRL > 4.08um.	$\geq$	1.33	um
<b>14xTMn.A.1</b>	14xTMn area	$\geq$	0.8	um <sup>2</sup>
<b>14xTMn.A.2</b>	14xTMn enclosed area	$\geq$	2	um <sup>2</sup>
<b>14xTMn.DN.1</b>	14xTMn density (window 112um*112um, stepping 56um), except DUPMK1, PAD and INDMY, LOGO regions	$\geq$	10%	
<b>14xTMn.DN.2</b>	14xTMn density (window 112um*112um, stepping 56um), except DUPMK1, PAD and INDMY, LOGO regions	$\leq$	85%	
<b>14xTMn.DN.3</b>	14xTMn density difference between any two neighboring checking windows (window 180um*180um, stepping 180um), except NODMF su 0.4um region.	$\leq$	50%	
<b>14xTMn.DN.4</b>	14xTMn full chip density	$\geq$	20%	
<b>14xTMn.R.1</b>	14xTMn pattern must be drawn on data type of 40.			
<b>14xTMn.R.2</b>	It is not allowed for maximum delta V $\geq$ 5.6V, when space between 14xTMn and 14xTMn/14xTVn-1/14xTVn is < 4.5um			
<b>14xTMn.R.3<sup>[NC]</sup></b>	14xTMn line-end must be rectangular.			
<b>14xTMn.R.4</b>	14x TM1 exist in a chip without 14x TM2 is not allowed.			

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#### 7.2.47 Ultra Thick Via (UTV) design rules

Rule number	Description	Opt.	Design Value	Unit
UTV.W.1	UTV width and length, except MARKS and MARKG regions	=	0.324	um
UTV.S.1	Space between single UTVs	$\geq$	0.306	um
UTV.S.2	Space between UTV and its neighboring UTV (T). The definition of neighboring UTV (T): 1) UTV (T) is in a UTV group 2) The number of this UTV group is $\geq 4$ , there are at least 3 UTV s neighboring to UTV (T) 3) The space between UTV (T) to other UTV s in this group $< 0.504\text{um}$	$\geq$	0.484	um
UTV.EN.1	UTV must be fully covered by 1.25xMn, 10xTMn, MIM, or CTOP; where 1.25xMn, 10xTMn, MIM, or CTOP is the metal layer directly underneath UTV. Enclosure by 10xTMn must follow UTV.EN.2, MIM.3 or CTOP.5.			
UTV.EN.2	UTV must be fully covered by 1.25xMn, 10xTMn, where 1.25xMn, 10xTMn is the metal layer directly underneath UTV, UTV enclosure by 1.25xMn, 10xTMn, except MARKS region	$\geq$	0.071	um
UTV.EN.3	UTV must be fully covered by UTM, where UTM is the metal layer directly above UTV. Enclosure by UTM must follow UTV.EN.4 as below			
UTV.EN.4	UTV enclosure by UTM. UTV must be fully covered by UTM	$\geq$	0.45	um
UTV.R.1	UTV must be drawn on data type of 0.			
UTV.R.2	45-degree rotated UTV is not allowed.			
UTV.R.3	There should be at least two UTVs with space $\leq 1.54\text{um}$ (S1) in 10xTMn and UTM intersection area, when either 10xTMn or UTM width and length (W1) $> 1.63\text{um}$ , except MARKS.			
UTV.R.4	There should be at least two UTVs in the intersection area of (1.25xMn or 10xTMn) and UTM, when either wide metal of (1.25xMn or 10xTMn) or UTM with both length L $> 9.1\text{um}$ and width W $> 2.75\text{um}$ , the space between either via and wide metal is $\leq 5.4\text{um}$ (D3, D3 is the shortest running path length from Via to the wide metal).			
UTV.R.5	It is not allowed for maximum delta V $\geq 5.6\text{V}$ , when space between UTV is $< 0.410\text{um}$			
UTV.R.6	It's not allowed UTV overlap with the metal resistor directly underneath			

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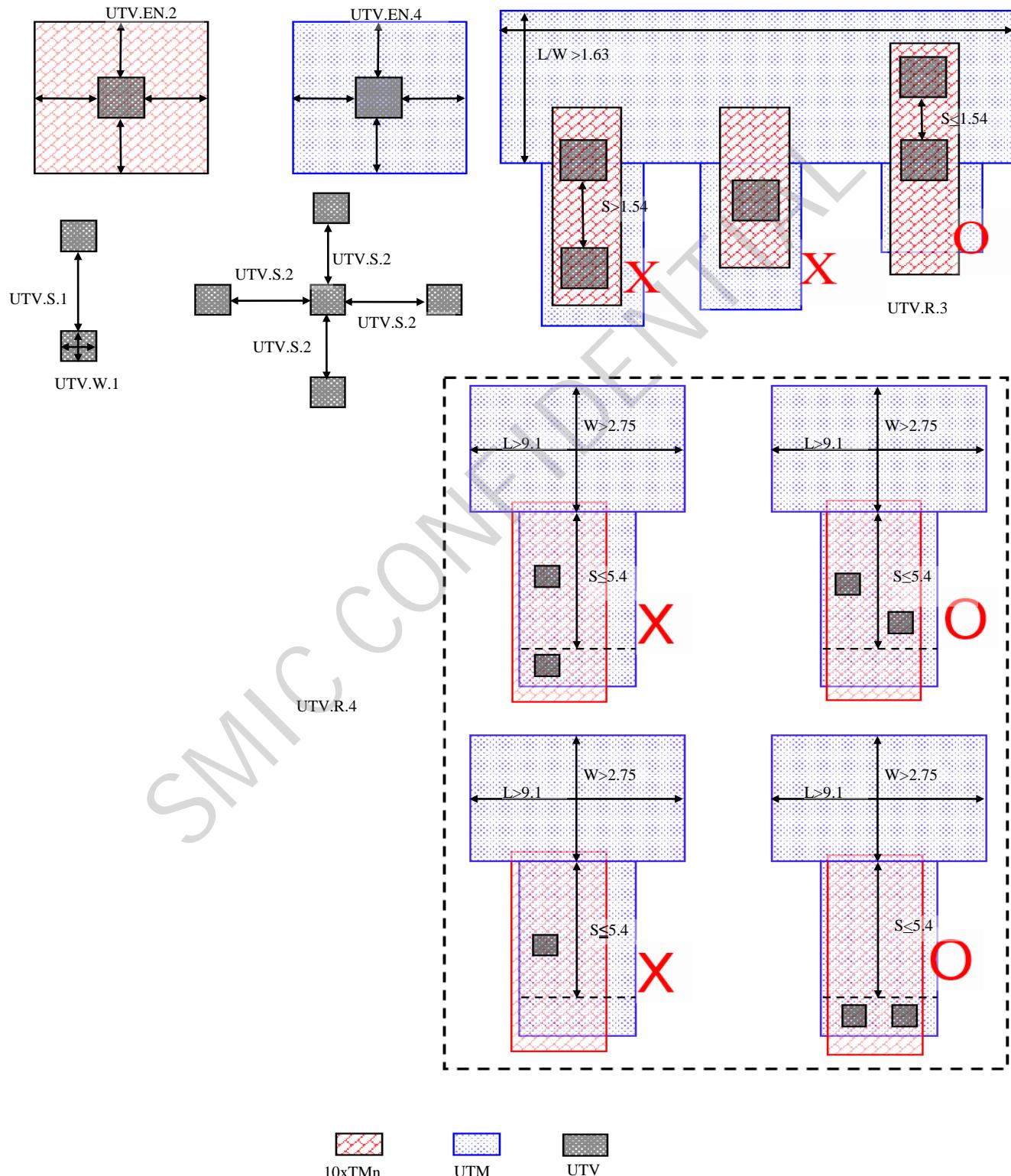
Rule number	Description	Opt.	Design Value	Unit
	and above the UTV.			
UTV.R.7 <sup>[NC]</sup>	Recommend to use redundant vias to avoid high Rc wherever layout allows.			

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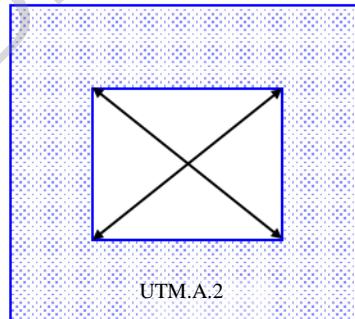
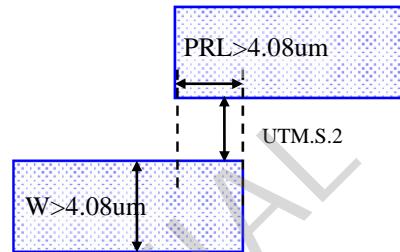
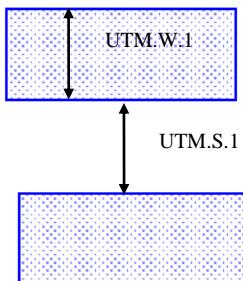
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### 7.2.48 Ultra Thick Metal (UTM) design rules

UTM design rules are only used for ultra-thick top metal (3.35um)

Rule number	Description	Opt.	Design Value	Unit
<b>UTM.W.1</b>	UTM width	$\geq$	1.8	um
<b>UTM.W.2</b>	UTM width, except MD, DUPMK1, PAD and INDMY regions	$\leq$	11	um
<b>UTM.S.1</b>	Space between two UTM	$\geq$	0.9	um
<b>UTM.S.2</b>	Space between two UTM when one or both UTM width is > 4.08um and PRL > 4.08um	$\geq$	1.33	um
<b>UTM.A.1</b>	UTM area	$\geq$	7.25	um <sup>2</sup>
<b>UTM.A.2</b>	UTM enclosed area	$\geq$	7.25	um <sup>2</sup>
<b>UTM.DN.1</b>	UTM full chip density	$\geq$	20%	
<b>UTM.DN.2</b>	UTM full chip density	$\leq$	50%	
<b>UTM.DN.3</b>	UTM density (window 112um*112um, stepping 56um), except DUPMK1, PAD, NODMF, MARKS, LOGO and INDMY regions	$\geq$	10%	
<b>UTM.DN.4</b>	UTM density (window 112um*112um, stepping 56um), except DUPMK1, PAD, NODMF, MARKS, LOGO regions	$\leq$	85%	
<b>UTM.R.1</b>	It is not allowed for UTM above 14xTMn.			
<b>UTM.R.2<sup>[NC]</sup></b>	UTM line-end must be rectangular.			
<b>UTM.R.3</b>	Maximum delta V $\geq$ 5.6V is not allowed, when space between UTM and UTM/UTV is < 5um			

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UTM



Pad

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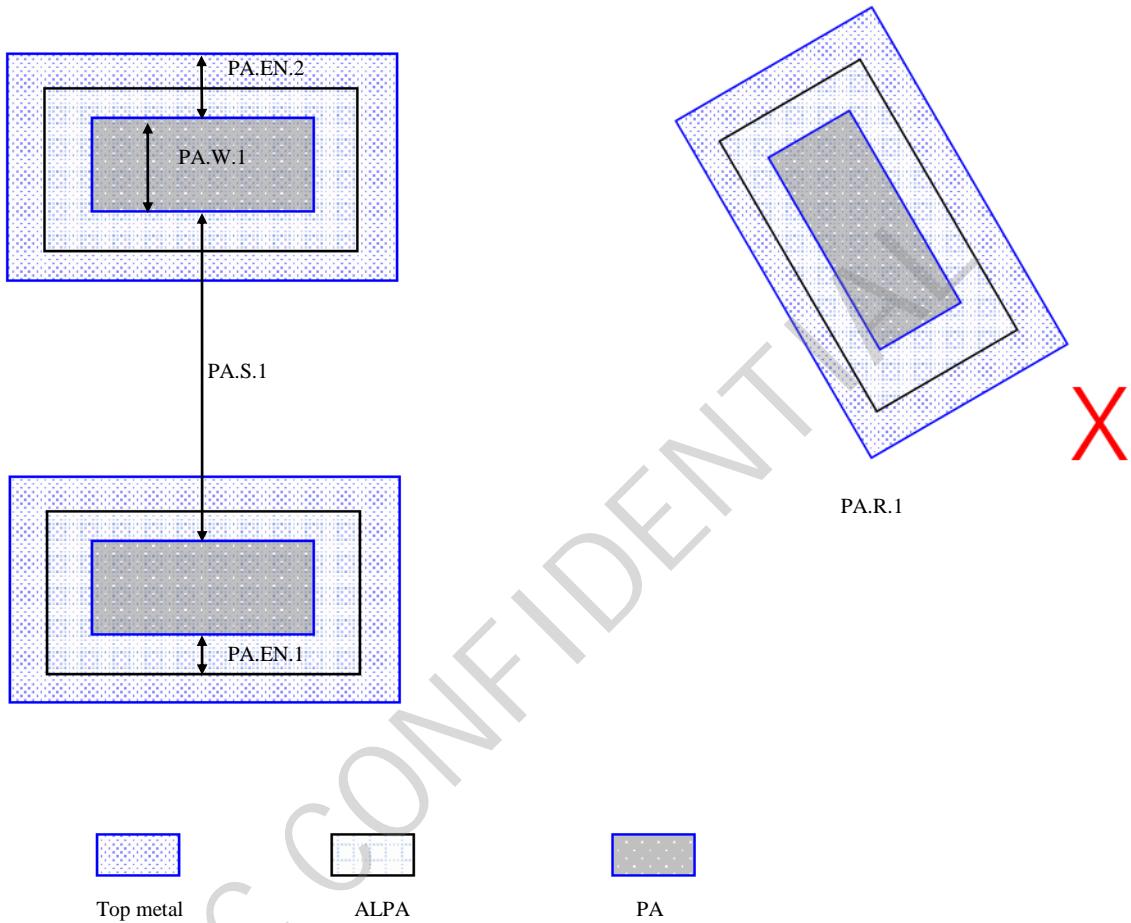
### 7.2.49 PA design rules

Passivation 1 can be used for pad opening and AL RDL Via opening

Rule number	Description	Opt.	Design Value	Unit
PA.W.1	PA width and length if PA not overlap with MD, except MARKS and LOGO regions	=	1.8, 2.7	um
PA.W.2	PA width if PA overlap with MD, except MARKS and LOGO regions	≥	30.6	um
PA.S.1	Space between two PA, except LOGO region	≥	1.8	um
PA.EN.1	PA fully enclosure by ALPA if PA not overlap with MD, except LOGO region It allows 0.009um DRC checking tolerance in INDMY region.	≥	0.45	um
PA.EN.1a	PA fully enclosure by ALPA if PA overlap with MD, except LOGO region It allows 0.009um DRC checking tolerance in INDMY region.	≥	0.9	um
PA.EN.2	PA fully enclosure by UTM/14xTMn/10xTMn, except LOGO region It allows 0.009um DRC checking tolerance in INDMY region.	≥	0.45	um
PA.R.1	45-degree rotated PA is not allowed, except INDMY region.			

Note: Pad design please consult to relative package house.

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### 7.2.50 ALPA rules

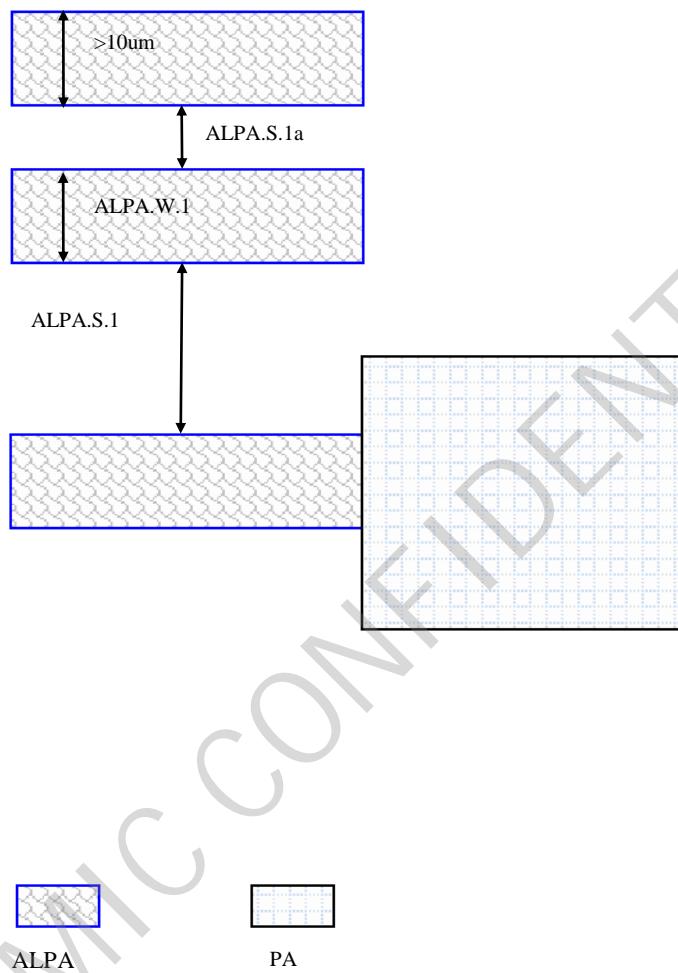
ALPA patterns include Al pads generated by PA logic generation patterns and drawn AL pad or AL redistribution patterns (ALRDL). Please check below rules after logic operation.

ALRDL: ALPA layer width smaller than 35um

ALPA pad: ALPA layer width equal or larger than 35um.

Rule number	Description	Opt.	Design Value	Unit
<b>ALPA.W.1</b>	ALPA width, except LOGO region It allows 0.009um DRC checking tolerance in INDMY region	$\geq$	1.8	um
<b>ALPA.S.1</b>	ALPA space, except LOGO region DRC waive space in same polygon. It allows 0.009um DRC checking tolerance in INDMY region	$\geq$	1.8	um
<b>ALPA.S.1a</b>	Space between ALPA when one or both ALPA width larger than 10um, except ALPA.S.2.	$\geq$	2.69	um
<b>ALPA.S.2</b>	Space between (ALPA AND (MD sizing up 3um)) and (ALPA AND (MD sizing up 3um)) or ALRDL. DRC waive space in same polygon. It allows 0.009um DRC checking tolerance in INDMY region.	$\geq$	2.25	um
<b>ALPA.S.3</b>	Space between ALPA pad and Fuse window edge	$\geq$	44.5	um
<b>ALPA.DN.1</b>	ALPA full chip density	$\geq$	10%	
<b>ALPA.DN.2</b>	ALPA full chip density	$\leq$	70%	
<b>ALPA.R.1<sup>[NC]</sup></b>	ALPA includes ALPA Pad and ALRDL. ALRDL is defined as ALPA layer width smaller than 35um. ALPA pad is defined as ALPA layer width equal or larger than 35um.			
<b>ALPA.R.2</b>	ALPA is must drawn layer.			

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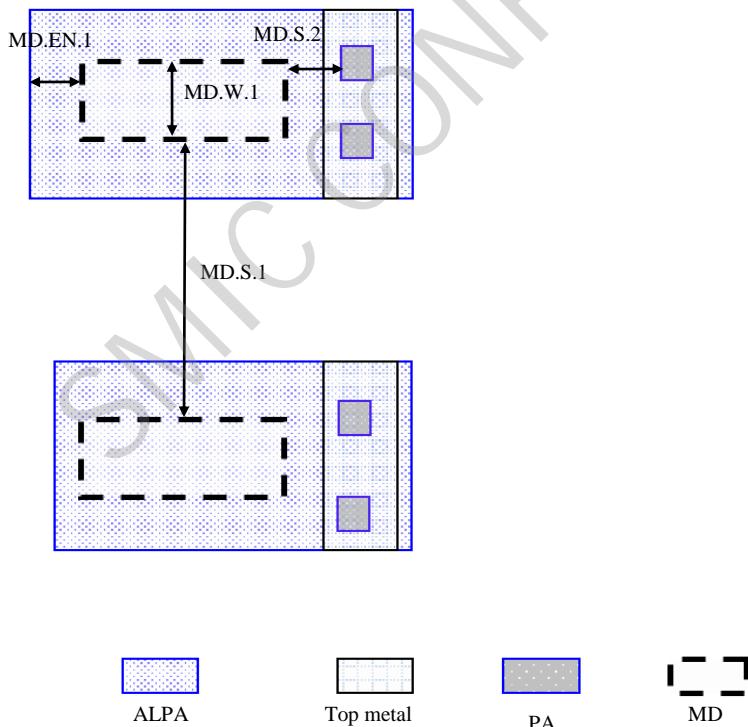
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### 7.2.51 MD (PA2) design rules

Rule number	Description	Opt.	Design Value	Unit
<b>MD.W.1</b>	MD width, except LOGO region	$\geq$	12.5	um
<b>MD.S.1</b>	MD space, except LOGO region	$\geq$	4.49	um
<b>MD.S.2</b>	Space between MD and PA (space = 0 is allowed), except LOGO region	$\geq$	1.52	um
<b>MD.EN.1</b>	MD fully enclosure by ALPA, except LOGO region	$\geq$	0.9	um
<b>MD.R.1</b>	MD must be a drawn layer.			
<b>MD.R.2</b>	MD interact PA (PA size $\leq$ 2.7um) is not allowed, except LOGO region			
<b>MD.R.3</b>	Inductor under MD wire-bond pad opening is not allowed.			



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