



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev. Rev: 1.10.1
---------------------------	---	------------	-----------------------

Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

Level 1 - Manual Level 2 – Procedure/SPEC/Report Level 3 - Operation Instruction

Security Level:

Security 1 - SMIC Confidential Security 2 - SMIC Restricted Security 3 - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
1	1.10	2015-01-15	Jenny Pang	<p>1. 7.1.3: exclude OCCDB in DGR.1;update DGR4 for INDMY checking.</p> <p>2. 7.1.5: add density check DRC check guideline.</p> <p>3. 7.1.6: add explanation for metal option table.</p> <p>4. 7.1.8: Add LUWMK1,M1B,M2B,M3B,M4B,M5B,M6B, M7B,M8B,TM1B,TM2B,B1B,B2B,STM1B,STM2B, MTT2B,ALPAB, PRBOUN,ERCMK1, RFDN5T layer; modify DUMBMB layer definition; add sequence No.</p> <p>5. 7.1.9 Mask layer mapping table: add MVN,NDRN, ULVN,ULVP layer, and adjust layer sequence based on process sequence.</p> <p>6. 7.1.10: add ESD device notes, update TG from “0” to “*” for resistor device to align DG.</p> <p>7. 7.1.12: add LDMOS drain definition.</p> <p>8. 7.1.15: add DRC Connectivity Definition.</p> <p>9. 7.2.2: AA.6: change rule value to 0.13; change 5um to 0.09um for AA.27a/b; AA.23: optimize non-DRC check condition.</p> <p>10. 7.2.3/10: downgrade AADMP.18/GTDMP.18 to DFM priority3 rule and exclude OCOVL; add max rule for AADMP.1; add AADMP.9/GTDMP.8; add min rule for AADMP.17; change AADMP.13 value to 0.08um; change GTDMP.24 to main rule.</p> <p>11. 7.2.6: add P+AA for LVT_N.11 and add N+AA for LVT_P.11.</p> <p>12. 7.2.7/7.2.8: add DG.16/17,TG.15/16.</p> <p>13. 7.2.9:GT.5/36: exclude OCOVL; GT.6a/7a: exclude VARMOS; GT.8d: exclude FUSEMK1, delete EFUSE in non-DRC check condition; GT.22: optimize non-DRC check condition; GT.27: exclude INDMY; GT.30a/30a[R]: change LDBK to LDMOS drain site; GT.35: change channel length to >0.06um; GT.36[R]: change to main rule; GT.31/55: optimize description; GT.28/56: optimize voltage.</p> <p>14. 7.2.13/14: add SN.15b/SP.15b, change SN.15/SP.15 rule No to SN.15a/SP.15a.</p> <p>15. 7.2.15: SAB.5/12: exclude INDMY.</p> <p>16. 7.2.16: add it for process concern.</p> <p>17. 7.2.17: CT.6/6a/6b/6c//6a[R]/6b[R]: exclude OCOVL. CT.9/9a/9b/9c: exclude OCCD; CT.12: exclude INDMY.</p> <p>18. 7.2.18:M1.7[R]: exclude INDMY; M1.11c: change runlength to -0.12; M1.12-15: add non-DRC check condition; M1.17b/17c: update non-DRC check condition; add M1.30; delete Note4.</p> <p>19. 7.2.19 1xMn.1:update non-DRC check condition; 1xMn.6[R]/1xMn.24: exclude INDMY; 1xMn.10-13: add non-DRC</p>



Semiconductor Manufacturing International Corporation

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev. Rev: 1.10.1
---------------------------	---	------------	-----------------------

			<p>check condition;1xMn.15b: update non-DRC check condition;delete Note4.</p> <p>20. 7.2.20 1xRVn.7:delete item2 condition c),update condition a);1xRVn.8:exclude INST.</p> <p>21. 7.2.21: 2xMn.1: add non-DRC check condition.</p> <p>22. 7.2.24 8xTMn.2c: change rule value to 1.5; 8xTMn.5/.5[R] : update non-DRC check condition.</p> <p>23. 7.2.26: 10xTMn.5/.6[R]: update non-DRC check condition.</p> <p>24. 7.2.27: LT.4/6:optimize description and change LT.6 value to 0.3.</p> <p>25. 7.2.28: MTT2.5:update description, change rule value to 1.5; delete INDMY in MTT2.8/9.</p> <p>26. 7.2.29:PA.4: optimize description.</p> <p>27. 7.2.32 DUP: add 8xTV in DUP.5,update Notes.</p> <p>28. 7.2.35/37: RESAA.5[G]/RESP1.5[G]: change rule value from 0.19 to 0.1; add RESAA.13[G]/RESP1.14[G].</p> <p>29. 7.2.38: EFU.6: add 0.1um in rule value; EFU.8:change rule value to 0.022um.</p> <p>30. 7.2.43: ANT.GT9a/9b/11:change 14K to 14.5K.</p> <p>31. 7.3.3: overall update inductor rule based on inductor design.</p> <p>32. 7.3.4: new define LDMOS rule.</p> <p>33. 7.3.5 seal ring section:update Table1;separate table2 SR.2[G]/3[G]/4[G]/5[G] to two rules at straight direction and at 45 degree angle area; and change SR.6[G]/7[G] ruel value, update SR.14[G] description;delete [G] for SR.11-14.7.3.5:</p> <p>34. 7.3.6: add DRC check metod, update LU.1/2/3/6 description, exclude OCCD in LU.4.</p> <p>35. 7.3.7: ESD.5[G]/6[G] :delete; ESD.8[G]: Change rule value to 0.6.</p> <p>36. 7.3.8: update it based on latest utility.</p> <p>37. 7.3.10:add Bn and STMn related layer.</p> <p>38. 7.4: DUMC.GT.07: change rule value to 0.0138; delete DUMC.GT.22;update DUMC.Mn.00, DUMC.P2.05, DUMC.M1.06-07, DUMC.Mn.05-07.</p> <p>39. 7.5.2 DFM: define 2xMn.6[R]/13[R];delete MD.6[R]/ALPA.4[R];change AA.1b[R]/ AA.21f[R]/ M1.7[R]/ 1xMn.6[R]/2xMn.6[R]/ 8xTMn .2d[R]/ 10xTMn .2d[R] to pri 3;add IND.26[G][R] and LD.13[G][R] ;8xTMn.5/.5[R]/10xTMn.5/.6[R]: update non-DRC check condition.</p> <p>40. Update seal ring GDS: change 8xTM/TV size, and add 10xTMn/TVn/LT design.</p>
2	1.10.1	2016-09-09	Minna Xu
			1. Update 8 attachment: in order to solve the DRC violation of seal ring, PIE updated the GDS sample 2. Add "Note: Any DRC violation please confirm with SMIC" in item 8.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 1/306
---------------------------	---	------------	----------------------	-----------------

**SEMICONDUCTOR MANUFACTURING INTERNATIONAL
CORPORATION**

28nm Logic Low Power(Poly/SION) 1.05V/1.8V/2.5V Design Rules

Version **1.10.1**

SMIC Confidential – Do Not Copy

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 2/306
---------------------------	---	------------	----------------------	-----------------

CONTENTS

1. Title:	4
2. Purpose:	4
3. Scope:	4
4. Nomenclature:	4
5. Reference:	4
6. Responsibility:	4
7. Subject content:	4
7.1 USER GUIDELINE	4
<i>7.1.1 Introduction.....</i>	<i>4</i>
<i>7.1.2 Grid size</i>	<i>4</i>
<i>7.1.3 Design requirements.....</i>	<i>4</i>
<i>7.1.4 Non-DRC check guideline</i>	<i>6</i>
<i>7.1.5 DRC check guideline.....</i>	<i>6</i>
<i>7.1.6 Metallization Options</i>	<i>7</i>
<i>7.1.7 SMIC Drawn layer Mapping Table.....</i>	<i>11</i>
<i>7.1.8 SMIC CAD layer Mapping Table.....</i>	<i>15</i>
<i>7.1.9 SMIC Mask layer Mapping Table.....</i>	<i>22</i>
<i>7.1.10 Device Layout Truth Table.....</i>	<i>25</i>
<i>7.1.11 Device table for dummy insertion</i>	<i>33</i>
<i>7.1.12 Design Rules Nomenclatures and Abbreviations</i>	<i>34</i>
<i>7.1.13 Definition of terminology used in these design rules.....</i>	<i>36</i>
<i>7.1.14 Design Check Flow for Tape out</i>	<i>48</i>
<i>7.1.15 DRC Connectivity Definition.....</i>	<i>50</i>
7.2 LAYOUT RULE DESCRIPTION.....	51
<i>7.2.1 DNW: Deep N-Well design rules.....</i>	<i>51</i>
<i>7.2.2 AA: Active Area design rules</i>	<i>53</i>
<i>7.2.3 AADMP: AA dummy design rules</i>	<i>63</i>
<i>7.2.4 NW: N-Well design rules.....</i>	<i>66</i>
<i>7.2.5 PSUB: Native device design rules.....</i>	<i>68</i>
<i>7.2.6 Low Vt design rules</i>	<i>70</i>
<i>7.2.7 DG: Dual GATE design rules to define 1.8V device</i>	<i>74</i>
<i>7.2.8 TG: Dual GATE design rules to define 2.5V IO device</i>	<i>76</i>
<i>7.2.9 GT: Poly design rules</i>	<i>78</i>
<i>7.2.10 GTDMP: GT dummy desing rules.....</i>	<i>94</i>
<i>7.2.11 GTMK2: Core Horizontal GATE design rules</i>	<i>98</i>
<i>7.2.12 P2: Poly cut design rules.....</i>	<i>100</i>
<i>7.2.13 SN: N+ source/drain implantation design rules.....</i>	<i>104</i>
<i>7.2.14 SP : P+ source/drain implantation design rules.....</i>	<i>108</i>
<i>7.2.15 SAB: Salicide Block design rules</i>	<i>113</i>
<i>7.2.16 Strained Source/Drain (PSR) design rules.....</i>	<i>116</i>
<i>7.2.17 CT: Contact design rules</i>	<i>117</i>
<i>7.2.18 Metal 1 design rules</i>	<i>123</i>
<i>7.2.19 1x Mn(n=2-8): 1x Metal design rules</i>	<i>136</i>
<i>7.2.20 1x Vn(n=1-7): IX Via design rules</i>	<i>149</i>
<i>7.2.21 2x Mn: 2x Metal design rules</i>	<i>163</i>
<i>7.2.22 2x Vn: 2x Via design rules</i>	<i>166</i>
<i>7.2.23 8x TVn: 8x Via(TV1/TV2) design rules</i>	<i>170</i>
<i>7.2.24 8x TMn : 8x Metal (TM1 /TM2) design rules</i>	<i>173</i>
<i>7.2.25 10x TVn: 10x Via(TV1/TV2) design rules</i>	<i>176</i>
<i>7.2.26 10xTMn : 10x Metal (TM1 /TM2) design rules</i>	<i>179</i>

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 3/306
---------------------------	---	------------	----------------------	-----------------

7.2.27 8x UTV: 8x UTV(LT) design rules	181
7.2.28 MTT2 design rules (ultra-thick metal)	184
7.2.29 PA: Passivation 1 design rules	186
7.2.30 ALPA design rules	188
7.2.31 MD(Passivation 2) design rules	190
7.2.32 DUP(Device Under Pad) design rules	191
7.2.33 Chip corner design rules	193
7.2.34 BORDER(Chip edge) layer design rule	194
7.2.35 AA resistor design rules	195
7.2.36 N-Well resistor design rules	198
7.2.37 Poly resistor design rules	202
7.2.38 Poly E-Fuse design rules	205
7.2.39 Diode design rules	207
7.2.40 MOM design rules	209
7.2.41 LOGO design rules	211
7.2.42 Metal low density design rules	212
7.2.43 Antenna Ratio Effect rules	214
7.2.44 SRAM marking layer design rules	219
7.3 LAYOUT GUIDELINE.....	222
7.3.1 Varactor layout guidelines	222
7.3.2 BIPOLA layout guidelines	225
7.3.3 Inductor design guidelines	226
7.3.4 LDMOS layout guideline	230
7.3.5 Seal ring layout guideline	233
7.3.6 ESD design rules and guideline	244
7.3.7 Latch-Up prevention layout guidelines	264
7.3.8 Redundant Via insertion guidelines	271
7.3.9 AA/GT/Metal/Via/ALPA Dummy insertion method selection guideline	272
7.3.10 Mask Re-tooling Guidelines Related with Dummy Insertion	273
7.3.11 Inline OCCD and OCOVL monitor cell guidelines	276
7.4 DUMMY CHECK RULE.....	279
7.5 DESIGN FOR MANUFACTURABILITY (DFM) RULES	287
7.5.1 Introduction	288
7.5.2 DFM Rules	288
7.6 CURRENT DENSITY GUIDELINES	300
7.6.1 Metal line/CT/Vn/PA Current Density	300
7.6.2 Metal line Irms definition	302
7.6.3 Temperature coefficient	303
8. ATTACHMENT:	304

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 4/306
---------------------------	---	------------	----------------------	-----------------

1. Title:

28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules

2. Purpose:

Patterns Design Rules and Guideline for 28nm Logic Low Power (Poly/SION) Process

3. Scope:

SMIC TD

4. Nomenclature:

NA

5. Reference:

NA

6. Responsibility:

Technology Development Center

7. Subject content:**7.1 User Guideline****7.1.1 Introduction**

This document provides 32nm layout dimension, 28nm logic poly/SION product is 90% liner shrinkage from this 32nm layout dimension, and layout 90% shrinkage is implemented in SMIC after product tape-out.

7.1.2 Grid size

1. Layout grid size is 0.001um.

2. Design geometry grid size:

0.005um OUTSIDE (INST OR FUSEMK1) region;

0.001um NOT OUTSIDE (INST OR FUSEMK1) region.

7.1.3 Design requirements

Designers should follow design requirement guidelines in this section in order to reduce the OPC loading and then enhance the OPC efficiency.

Guidelines number	Description
DGR.1	All the geometry design must be an integer multiple of 0.005um OUTSIDE (INST OR FUSEMK1) region. DRC check DNW, AA, AADMP, NW, PSUB, LVT_N, LVT_P, DG, TG, GT, GTDMP, GTMK2, P2, SN, SP, SAB, CT, M1, 1xMn, 1xVn, 2xMn, 2xVn, 8xTVn, 8xTMn, 10xTVn, 10xTMn, LT, MTT2, PA, NODMF, BORDER layers.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 5/306
---------------------------	---	------------	----------------------	-----------------

Guidelines number	Description
	DRC doesn't check INDMY and OCCDB region.
DGR.2^[NC]	All the geometry design must be an integer multiple is 0.001um NOT OUSTSIDE (INST OR FUSEMK1) region.
DGR.3^[NC]	Design geometry shape must be polygons
DGR.4	Only shapes of geometry that are orthogonal or 45-degree angle are allowed, DRC doesn't check MARKS and MD region. It allows 0.5-degree checking tolerance for 45-degree design in INDMY region.
DGR.5^[NC]	Only unidirectional, straight transistor channels are allowed
DGR.6^[NC]	Recommended to design simple rectangular shape geometry as possible, avoid L, U, H, or O shapes.
DGR.7^[NC]	All line-end are must be rectangular
DGR.8^[NC]	Self-intersecting shape are not allowed
DGR.9^[NC]	All the text or labels in the chip must be covered by the marker layer LOGO (26;0)
DGR.10^[NC]	Make sure the designs are DRC clean
DGR.11^[NC]	Recommended to avoid small jogs ($\leq 0.005\text{um}$) of geometry.
DGR.12^[NC]	The layout of designs should have the well organized hierarchical structures.
DGR.13^[NC]	The layout of auto dummy insertion designs should be put in a separate hierarchy from the main designs, and try to avoid the flattened dummy insertion designs.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 6/306
---------------------------	---	------------	----------------------	-----------------

7.1.4 Non-DRC check guideline

1. No DRC for the design rules with the superscript of [NC]
2. No DRC for Notes.

7.1.5 DRC check guideline

1. The rules with the superscript of [R] are recommended rules which require performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow recommended rules which purpose is to ensure better performance for process and device. Customers can waive violations based on their own judgment, and please consult with integration engineers if customers feel the need.

2. The rules with the superscript of [G] are layout guidelines which require performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow layout guidelines which purpose is to ensure better performance for process and device. Customers can waive violations based on their own judgment, and please consult with integration engineers if customers feel the need.

SMIC spice model and PDK is based on SMIC design rule guidelines. And SMIC don't provide spice model and PDK if customers don't follow the layout guidelines.

3. The design rules in this document are not applicable for seal ring area (marked with MARKS layer) which exclude DUMC_AA.11,DUMC_AA.12,DUMC_GT.08,DUMC_GT.09,DUMC_M1.06,DUMC_M1.07,DUMC_Mn.06, DUMC_Mn.07,DUMC_Bn.05,DUMC_Bn.07,DUMC_TMn.5,DUMC_TMn.6,DUMC_STMn.05,DUMC_STMn.06, DUMC_V1.05,DUMC_1xVn.05,DUMC_MTT2.03,DUMC_MTT2.04,DUMC_ALPA.03,DUMC_ALPA.04. For seal ring constrains and dimensions, please refer to seal ring section.

4. Pls follow guidelines for DRC checking as below:

Category	Rules	DRC switch setting by default
Guideline (Rule number with superscript of [G])	Varactor	Turn-on
	BIPOLA	Turn-on
	Inductor	Turn-on
	Seal Ring	Turn-on
	ESD	Turn-off
	Latch Up	Turn-on
	Inline OCCD and OCOVL	Turn-on

5. For density design rules, DRC code firstly exclude the region which is defined in rule, then check the layer density.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 7/306
---------------------------	---	------------	----------------------	-----------------

7.1.6 Metallization Options

28 nm metal options definition scheme was denoted in this section for metal layer and dielectric type, and is limited only to those materials present in the stack.

The scheme uses the following naming: xPyM_zMa_nMb_mIc_pTMc_qSTMc_sMTTc_tALPA

Where:

P = poly layers,

M = total metal layers excluding AL pad/Al RDL,

Ma = 1x metal layers,

Mb = 2x metal layers,

Ic = Cu inter metal layers (included M1),

TMc = Cu 8x top metal layers,

STMc = Cu 10x top metal layers,

MTTc = Cu Ultra thick metal layers,

ALPA = AL pad/AL RDL layers,

x = number of poly layers,

y = number of total metal layers excluding AL pad/Al RDL, ($y = m+p+q+s$),

z = number of 1x metal layers (included M1)

n = number of 2x metal layers,

m = number of Cu inter metal layers (included M1, $m=z+n$),

p = number of 8x Cu top metal layers,

q = number of 10x Cu top metal layers,

s = number of Cu ultra thick metal layers.

t = number of AL pad/AL RDL layers

Metal thickness in metal option table is only reference for customer. Please contact with SMIC BEOL integration team if customer needs exact thickness.

All metal option are applicable for ALPA 14.5KA and 28KA process.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 8/306
---------------------------	---	------------	----------------------	-----------------

Table 1 8xTMn/TVn optional table:

Metal option		1x +2x +8x metal option																																								
		IP5M_4Ma_4lc_1TMC_ALPA	IP6M_4Ma_1Mb_5lc_1TMC_ALPA	IP7M_4Ma_2Mb_6lc_1TMC_ALPA	IP8M_4Ma_3Mb_7lc_1TMC_ALPA	IP9M_5Ma_1Mb_6lc_1TMC_ALPA	IP10M_6Ma_1Mb_7lc_1TMC_ALPA	IP11M_7Ma_2Mb_8lc_1TMC_ALPA	IP12M_8Ma_2Mb_9lc_1TMC_ALPA	IP13M_8Ma_3Mb_10lc_1TMC_ALPA	IP14M_8Ma_4Mb_11lc_1TMC_ALPA	IP15M_8Ma_5Mb_12lc_1TMC_ALPA	IP16M_8Ma_6Mb_13lc_1TMC_ALPA	IP17M_8Ma_7Mb_14lc_1TMC_ALPA	IP18M_8Ma_8Mb_15lc_1TMC_ALPA	IP19M_8Ma_9Mb_16lc_1TMC_ALPA	IP20M_8Ma_10Mb_17lc_1TMC_ALPA	IP21M_8Ma_11Mb_18lc_1TMC_ALPA	IP22M_8Ma_12Mb_19lc_1TMC_ALPA	IP23M_8Ma_13Mb_20lc_1TMC_ALPA	IP24M_8Ma_14Mb_21lc_1TMC_ALPA																					
Total metal layers(excluding ALPA)		5	6	7	6	7	8	6	7	8	7	8	7	8	9	7	8	9	8	9	10	8	9	10	9	10	11	9	10	11	10	11	12									
M1 wiring level in CVD ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um M1 typical thickness: 900A M1 typical Sheet Resistance: 0.48 ohm/sq	160 M1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X									
	178 V1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
1x (thin) wiring levels in ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um Mn typical thickness: 900A Mn typical Sheet Resistance: 0.48 ohm/sq	180 M2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
	179 V2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
	181 M3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
	177 V3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
	182 M4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
	176 V4																																									
	183 M5																																									
	175 V5																																									
	184 M6																																									
	174 V6																																									
	185 M7																																									
	173 V7																																									
	186 M8																																									
2x (thin) wiring levels in BDI dielectric metal minimum pitch W / S = 0.1um / 0.1um Mn typical thickness: 2250A Mn typical Sheet Resistance: 0.18 ohm/sq	270 W0																																									
	280 B1																																									
	271 W1	X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X						
	281 B2	X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X		X	X						
8x (thick) wiring levels in TEOS dielectric TMn minimum pitch W / S = 0.40um / 0.40um TMn typical thickness: 9000A TMn typical Sheet Resistance: 0.022 ohm/sq	142 TV1																																									
	141 TM1																																									
	144 TV2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X							
	143 TM2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X							

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	Tech Dev Rev: 1.10.1	Page No.:
TD-LO28-DR-2006			2		9/306

Table 2 10xTMn/TVn optional table:

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 10/306
---------------------------	---	------------	----------------------	------------------

Table 3 8xTMn/TVn + MTT2 optional table:

		1x +2x+ 8x + MTT2 metal option											
Metal option		1P5M_4Ma_4lc_1MTTc_ALPA 1P6M_5Ma_5lc_1MTTc_ALPA 1P7M_6Ma_6lc_1MTTc_ALPA 1P8M_7Ma_7lc_1MTTc_ALPA 1P9M_8Ma_8lc_1MTTc_ALPA 1P6M_4Ma_4lc_1ITMc_1MTTc_ALPA 1P7M_5Ma_5lc_1ITMc_1MTTc_ALPA 1P8M_6Ma_6lc_1ITMc_1MTTc_ALPA 1P9M_7Ma_7lc_1ITMc_1MTTc_ALPA 1P10M_8Ma_8lc_1ITMc_1MTTc_ALPA 1P8M_5Ma_1Mb_6lc_1ITMc_1MTTc_ALPA											
Total metal layers(excluding ALPA)		5	6	7	8	9	6	7	8	9	10	8	
M1 wiring level in CVD ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um M1 typical thickness: 900A M1 typical Sheet Resistance: 0.48 ohm/sq	160	M1	X	X	X	X	X	X	X	X	X	X	
	178	V1	X	X	X	X	X	X	X	X	X	X	
1x (thin) wiring levels in ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um Mn typical thickness: 900A Mn typical Sheet Resistance: 0.48 ohm/sq	180	M2	X	X	X	X	X	X	X	X	X	X	
	179	V2	X	X	X	X	X	X	X	X	X	X	
	181	M3	X	X	X	X	X	X	X	X	X	X	
	177	V3	X	X	X	X	X	X	X	X	X	X	
	182	M4	X	X	X	X	X	X	X	X	X	X	
	176	V4		X	X	X			X	X	X	X	
	183	M5		X	X	X			X	X	X	X	
	175	V5			X	X	X			X	X	X	
	184	M6			X	X	X			X	X	X	
	174	V6				X	X				X	X	
	185	M7					X	X			X	X	
	173	V7						X				X	
	186	M8						X				X	
	270	W0											
	280	B1											
	271	W1										X	
	281	B2										X	
8x (thick) wiring levels in TEOS dielectric TMn minimum pitch W / S = 0.40um / 0.40um TMn typical thickness: 9000A TMn typical Sheet Resistance: 0.022 ohm/sq	142	8X TV1						X	X	X	X	X	
	141	8X TM1						X	X	X	X	X	
	144	8X TV2											
	143	8X TM2											
MTT2 minimum pitch W / S = 2.00um / 1.00um MTT2 typical thickness: 35kA MTT2 typical Sheet Resistance: 5mhm/sq	240	LT	X	X	X	X	X	X	X	X	X	X	
	543	MTT2	X	X	X	X	X	X	X	X	X	X	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 11/306
TD-LO28-DR-2006					

7.1.7 SMIC Drawn layer Mapping Table

Sequence number	Design layer name	GDS layer No	GDSdata type	Layer Description
1	AA	10	0	Active Area/SDG
2	DNW	19	0	Deep N well imp for substrate noise suppression
3	NW	14	0	N-Well / N-Tub
4	DG	29	0	1.8V IO device
5	TG	125	0	2.5V IO device
6	SDOP	99	0	HV SD open (for LDMOS)/SRAM PG device block layer
7	GT	30	0	Poly
8	P2	31	0	Poly trim slot
9	SP	43	0	P+ S/D Implant
10	SN	40	0	N+ S/D Implant
11	SAB	48	0	Resist Protect Oxide / Salicide Block
12	CT	50	0	Contact Hole (Metal to Si/Poly)
13	M1	61	0	Metal-1
14	V1	70	0	Via-1 Hole
15	M2	62	0	Metal-2
16	V2	71	0	Via-2 Hole
17	M3	63	0	Metal-3
18	V3	72	0	Via-3 Hole
19	M4	64	0	Metal-4
20	V4	73	0	Via-4 Hole
21	M5	65	0	Metal-5
22	V5	74	0	Via-5 Hole
23	M6	66	0	Metal-6
24	V6	75	0	Via-6 Hole
25	M7	67	0	Metal-7
26	V7	76	0	Via-7 Hole
27	M8	68	0	Metal-8
28	W0	225	0	2x Via-1
29	B1	141	0	2x Metal-1
30	W1	226	0	2x Via-2
31	B2	142	0	2x Metal-2
32	TV1	121	0	8x top via1
33	TM1	120	0	8x top metall1
34	TV2	123	0	8x top via2
35	TM2	122	0	8x top metal2
36	STV1	243	0	10x top via1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 12/306
---------------------------	---	------------	----------------------	------------------

Sequence number	Design layer name	GDS layer No	GDSdata type	Layer Description
37	STM1	228	0	10x top metal1
38	STV2	244	0	10x top via2
39	STM2	229	0	10x top metal2
40	LT	200	0	8x UTV
41	MTT2	231	0	Second Ultra Thick Top Metal
42	PA	80	0	Passivation / Pad
43	ALPA	83	0	AL Bonding Pad
44	MD	130	0	Metal about topmetal for redistribution,Passivation 2
45	ESD1	41	0	ESD Implant
46	PSUB	85	0	Psub area(NN)
47	EFUSE	81	2	DRC marking layer for an electrical fuse
48	INST	60	0	SRAM bitcell ,edge cell, strap cell or instance outline; SRAM bitcell ,edge cell ,strap cell area block layer
49	2PSRAM	60	12	DRC/LVS marking layer to identify 2P240 SRAM cells
50	VARMOS	93	0	Block Layer to cover all MOS-type varactor
51	RESNW	95	0	Dummy Pattern for NWELL Resistor
52	RESP1	96	0	Dummy Pattern for Poly-1 Resistor
53	RESAA	97	0	Dummy Pattern for AA Resistor
54	BIPOLA	159	1	Marking layer for PNP and NPN bipolars
55	DSTR	138	0	Diode Marker (identifies a diode, for LVS only)
56	NLDB	12	150	Block layer for N+ LDD and pocket implant
57	PLDB	13	150	Block layer for P+ LDD and pocket implant
58	SPBL	13	239	Marking layer for blocking P+ S/D Implant
59	SNBL	12	138	Marking layer for blocking N+ S/D Implant
60	HRBL	34	239	Marking layer for blocking poly resistor implant and poly N+ doping
61	PSRBL	6	239	Block layer for non-SiGe PFET Si recess(GS)
62	PSRDUM	6	1	PSR Dummy Layer (For dummy PSR insertion)
63	PSRNDUM	6	11	PSR Dummy Layer (For dummy PSR insertion)
64	AADOP	10	7	AA Dummy pattern layer is referenced in OPC engineering
65	AADUM	10	1	[DATATYPE:1] AA Dummy Layer(For dummy AA insertion)
66	GTDOP	30	7	Poly Dummy pattern layer is referenced in OPC engineering
67	GTDUM	30	1	[DATATYPE:1] Poly Dummy Layer(For dummy poly insertion)
68	M1DOP	61	7	Metal 1 Dummy pattern layer is referenced in OPC engineering
69	M1DUM	61	1	[DATATYPE:1]Metal1 Dummy Layer(For dummy Metal insertion)

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 13/306
---------------------------	---	------------	----------------------	------------------

Sequence number	Design layer name	GDS layer No	GDSdata type	Layer Description
70	V1DUM	70	1	via-1 Dummy Layer (For dummy via insertion)
71	M2DOP	62	7	Metal 2 Dummy pattern layer is referenced in OPC engineering
72	M2DUM	62	1	[DATATYPE:1] Metal2 Dummy Layer(For dummy Metal insertion)
73	V2DUM	71	1	via-2 Dummy Layer(For dummy via insertion)
74	M3DOP	63	7	Metal 3 Dummy pattern layer is referenced in OPC engineering
75	M3DUM	63	1	[DATATYPE:1]Metal3 Dummy Layer(For dummy Metal insertion)
76	V3DUM	72	1	via-3 Dummy Layer(For dummy via insertion)
77	M4DOP	64	7	Metal 4 Dummy pattern layer is referenced in OPC engineering
78	M4DUM	64	1	[DATATYPE:1]Metal4 Dummy Layer(For dummy Metal insertion)
79	V4DUM	73	1	via-4 Dummy Layer(For dummy via insertion)
80	M5DOP	65	7	Metal 5 Dummy pattern layer is referenced in OPC engineering
81	M5DUM	65	1	[DATATYPE:1]Metal5 Dummy Layer(for dummy Metal insertion)
82	V5DUM	74	1	Via-5 Dummy Layer(For dummy via insertion)
83	M6DOP	66	7	Metal 6 Dummy pattern layer is referenced in OPC engineering
84	M6DUM	66	1	[DATATYPE:1]Metal6 Dummy Layer(For dummy Metal insertion)
85	V6DUM	75	1	via-6 Dummy Layer(For dummy via insertion)
86	M7DOP	67	7	Metal 7 Dummy pattern layer is referenced in OPC engineering
87	M7DUM	67	1	[DATATYPE:1]Metal7 Dummy Layer(For dummy Metal insertion)
88	V7DUM	76	1	via-7 Dummy Layer(For dummy via insertion)
89	M8DOP	68	7	Metal 8 Dummy pattern layer is referenced in OPC engineering
90	M8DUM	68	1	{DATATYPE:1}Metal8 Dummy Layer(For dummy Metal insertion)
91	B1DUM	141	1	2x Metal-1 Dummy Layer
92	B1DOP	141	7	2x Metal-1 Dummy pattern layer for OPC engineering
93	B2DUM	142	1	2x Metal-2 Dummy Layer
94	B2DOP	142	7	2x Metal-2 Dummy pattern layer for OPC engineering
95	TV1DUM	121	1	8x top via1 dummy
96	TM1DUM	120	1	8x top metal1 dummy
97	TV2DUM	123	1	8x top via2 dummy
98	TM2DUM	122	1	8x top metal2 dummy
99	STV1DM	243	1	10x top via1 dummy
100	STM1DM	228	1	10x top metal 1 dummy
101	STV2DM	244	1	10x top via2 dummy
102	STM2DM	229	1	10x top metal2 dummy

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 14/306
---------------------------	---	------------	----------------------	------------------

Sequence number	Design layer name	GDS layer No	GDSdata type	Layer Description
103	MTT2DM	231	1	MTT2 Dummy layer
104	ALDUM	83	11	ALPA Dummy layer
105	AADMP	10	8	Manually drawn AA dummy layer with OPC engineering
106	GTDMMP	30	8	Manually drawn poly dummy layer with OPC engineering
107	UDSRAM	60	3	Marking layer UDSRAM(60;3) for LR D240 read port
108	GTMK2	89	168	Marking layer for the core horizontal gate
109	P2DUM	31	1	P2 layer dummy(for dummy P2 insertion)
110	P2DOP	31	7	P2 dummy pattern layer for OPC engineering
111	E1	144	0	4x Metal-1
112	Y0	233	0	4x Via-1 hole
113	LVT_N	159	158	Marking layer for N-type low-Vt devices
114	LVT_P	159	168	Marking layer for P-type low-Vt devices
115	ULVT_N	159	159	Marker layer for N-type Ultra low Vth device
116	ULVT_P	159	169	Marker layer for P-type Ultra low Vth device

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 15/306
---------------------------	---	------------	----------------------	------------------

7.1.8 SMIC CAD layer Mapping Table

Sequence No	Layer name	GDS No	Data Type	Description
1	STSRAM	60	1	LVS marking layer to identify SP127 SRAM cells
2	DPSRAM	60	4	LVS marking layer to identify DP315 dualport SRAM cells;
3	LRSRAM	60	5	LVS marking layer to identify SP155 SRAM cells
4	6TMK	60	151	Marking layer to identify 6T SRAM transistor in 2P240 SRAM.
5	HPBL	60	150	Marking layer to identify low leakage SRAM.
6	LDBK	216	150	Marking layer to identify LDMOS function area.
7	NODMF	180	0	Area not to add AA/poly/Metal dummies
8	MOMDMY	211	1	MOM Dummy layer
9	JVARDUM	183	0	Junction Varactor recognition for DRC/LVS
10	DGOD	29	2	To block over drive poly
11	DGUD	29	3	To block under drive poly
12	MARKF	190	0	Fuse area mark for Fuse DRC check
13	MARKG	189	0	Guard ring mark for DRC check
14	MARKS	189	151	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage
15	INDMY	212	0	Dummy layer for MTT in Inductor
16	DTDMY	191	3	Marker layer for different net AA
17	DIFRES	97	3	LVS marking layer for AA Resistor
18	PLRES	96	3	LVS Marking layer for Poly resistor portion
19	RESP3T	96	1	Dummy layer for Poly-1 Resistor with 3 terminal
20	RFDEV	181	0	DRC/LVS mark layer for RF device
21	RFMOSD	182	0	DRC/LVS mark layer for RF mos drain terminal
22	JVARDUM	183	0	DRC/LVS mark layer for junction varactor
23	VARJUN	94	0	DRC/LVS mark layer for junction varactor
24	RF3T	183	2	DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM
25	SUBD	131	1	LVS substrate separation layer
26	MOSCKT	131	2	LVS dummy layer to distinguish bsim MOS and subckt MOS
27	RESCKT	131	3	LVS dummy layer for subckt resistor
28	PLDMK	131	4	LVS marking layer for device dummy poly
29	NFDMK	131	5	LVS marking layer for MOS multiple fingers
30	DNWTR	19	2	LVS six terminal DNW MOS
31	M1R	171	0	M1 resistor layer
32	M2R	172	0	M2 resistor layer
33	M3R	173	0	M3 resistor layer

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 16/306
---------------------------	---	------------	----------------------	------------------

Sequence No	Layer name	GDS No	Data Type	Description
34	M4R	174	0	M4 resistor layer
35	M5R	175	0	M5 resistor layer
36	M6R	176	0	M6 resistor layer
37	M7R	177	0	M7 resistor layer
38	M8R	178	0	M8 resistor layer
39	B1R	194	154	2xmetal 1 resistor layer
40	B2R	194	155	2xmetal 2 resistor layer
41	TM1R	201	0	8x top metal1 resistor layer
42	TM2R	202	0	8x top metal2 resistor layer
43	STM1R	194	150	10x top metal1 resistor layer
44	STM2R	194	151	10x top metal2 resistor layer
45	MTT2R	194	153	MTT2 resistor layer
46	ALPAR	83	1	ALPA resistor layer
47	DCTY	139	0	Area with no Extraction for LVS
48	RFSD	181	3	RF MOS of even finger with S/D permute for LVS
49	RFDN6T	181	4	6-terminal RF MOS in deep NWELL for LVS, the sixth terminal is Psub.
50	MOMTEM	211	2	LVS mark layer for MOM terminal
51	LOGO	26	0	LOGO
52	EXDFM	239	1	DFM error waive
53	EXLFD	239	2	LFD errors waive
54	BORDER	127	0	Marking layer for chip edge
55	DUPMK1	89	156	Marking layer for DUP(pad with device underneath)
56	ESDIO1	133	0	DRC marking layer for SMIC IO ESD protection devices and circuits identification.
57	ESDIO2	133	3	DRC marking layer for ESD protection devices and circuits identification.
58	ESDHV	133	1	DRC marking layer for HV tolerant ESD protection devices using cascoded NMOS.
59	M1V12	89	16	DRC and LVS marking layer for 1.2V M1
60	M1V15	89	17	DRC and LVS marking layer for 1.5V M1
61	M1V18	89	11	DRC and LVS marking layer for 1.8V M1
62	M1V25	89	12	DRC and LVS marking layer for 2.5V M1
63	M1V33	89	13	DRC and LVS marking layer for 3.3V M1
64	M1V50	89	15	DRC and LVS marking layer for 5V M1
65	M2V12	89	26	DRC and LVS marking layer for 1.2V M2
66	M2V15	89	27	DRC and LVS marking layer for 1.5V M2
67	M2V18	89	21	DRC and LVS marking layer for 1.8V M2
68	M2V25	89	22	DRC and LVS marking layer for 2.5V M2

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 17/306
---------------------------	---	------------	----------------------	------------------

Sequence No	Layer name	GDS No	Data Type	Description
69	M2V33	89	23	DRC and LVS marking layer for 3.3V M2
70	M2V50	89	25	DRC and LVS marking layer for 5V M2
71	M3V12	89	36	DRC and LVS marking layer for 1.2V M3
72	M3V15	89	37	DRC and LVS marking layer for 1.5V M3
73	M3V18	89	31	DRC and LVS marking layer for 1.8V M3
74	M3V25	89	32	DRC and LVS marking layer for 2.5V M3
75	M3V33	89	33	DRC and LVS marking layer for 3.3V M3
76	M3V50	89	35	DRC and LVS marking layer for 5V M3
77	M4V12	89	46	DRC and LVS marking layer for 1.2V M4
78	M4V15	89	47	DRC and LVS marking layer for 1.5V M4
79	M4V18	89	41	DRC and LVS marking layer for 1.8V M4
80	M4V25	89	42	DRC and LVS marking layer for 2.5V M4
81	M4V33	89	43	DRC and LVS marking layer for 3.3V M4
82	M4V50	89	45	DRC and LVS marking layer for 5V M4
83	M5V12	89	56	DRC and LVS marking layer for 1.2V M5
84	M5V15	89	57	DRC and LVS marking layer for 1.5V M5
85	M5V18	89	51	DRC and LVS marking layer for 1.8V M5
86	M5V25	89	52	DRC and LVS marking layer for 2.5V M5
87	M5V33	89	53	DRC and LVS marking layer for 3.3V M5
88	M5V50	89	55	DRC and LVS marking layer for 5V M5
89	M6V12	89	66	DRC and LVS marking layer for 1.2V M6
90	M6V15	89	67	DRC and LVS marking layer for 1.5V M6
91	M6V18	89	61	DRC and LVS marking layer for 1.8V M6
92	M6V25	89	62	DRC and LVS marking layer for 2.5V M6
93	M6V33	89	63	DRC and LVS marking layer for 3.3V M6
94	M6V50	89	65	DRC and LVS marking layer for 5V M6
95	M7V12	89	76	DRC and LVS marking layer for 1.2V M7
96	M7V15	89	77	DRC and LVS marking layer for 1.5V M7
97	M7V18	89	71	DRC and LVS marking layer for 1.8V M7
98	M7V25	89	72	DRC and LVS marking layer for 2.5V M7
99	M7V33	89	73	DRC and LVS marking layer for 3.3V M7
100	M7V50	89	75	DRC and LVS marking layer for 5V M7
101	M8V12	89	86	DRC and LVS marking layer for 1.2V M8
102	M8V15	89	87	DRC and LVS marking layer for 1.5V M8
103	M8V18	89	81	DRC and LVS marking layer for 1.8V M8
104	M8V25	89	82	DRC and LVS marking layer for 2.5V M8
105	M8V33	89	83	DRC and LVS marking layer for 3.3V M8

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 18/306
---------------------------	---	------------	----------------------	------------------

Sequence No	Layer name	GDS No	Data Type	Description
106	M8V50	89	85	DRC and LVS marking layer for 5V M8
107	B1V18	89	91	DRC and LVS marking layer for 1.8V 2x metal 1
108	B1V25	89	92	DRC and LVS marking layer for 2.5V 2x metal 1
109	B1V33	89	93	DRC and LVS marking layer for 3.3V 2x metal 1
110	B1V50	89	95	DRC and LVS marking layer for 5V 2x metal 1
111	B1V12	89	96	DRC and LVS marking layer for 1.2V 2x metal 1
112	B1V15	89	97	DRC and LVS marking layer for 1.5V 2x metal 1
113	B2V18	89	101	DRC and LVS marking layer for 1.8V 2x metal 2
114	B2V25	89	102	DRC and LVS marking layer for 2.5V 2x metal 2
115	B2V33	89	103	DRC and LVS marking layer for 3.3V 2x metal 2
116	B2V50	89	105	DRC and LVS marking layer for 5V 2x metal 2
117	B2V12	89	106	DRC and LVS marking layer for 1.2V 2x metal 2
118	B2V15	89	107	DRC and LVS marking layer for 1.5V 2x metal 2
119	M1TXT	61	250	Metal-1 Text Layer, label text
120	M2TXT	62	250	Metal-2 Text Layer, label text
121	M3TXT	63	250	Metal-3 Text Layer, label text
122	M4TXT	64	250	Metal-4 Text Layer, label text
123	M5TXT	65	250	Metal-5 Text Layer, label text
124	M6TXT	66	250	Metal-6 Text Layer, label text
125	M7TXT	67	250	Metal-7 Text Layer, label text
126	M8TXT	68	250	Metal-8 Text Layer, label text
127	B1TXT	141	250	2xmetal 1 text Layer , label text
128	B2TXT	142	250	2xmetal 2 text Layer , label text
129	TM1TXT	120	3	8x top metal 1 Text Layer, label text
130	TM2TXT	122	3	8x top metal 2 Text Layer, label text
131	STM1TXT	228	3	10x top metal 1 Text Layer, label text
132	STM2TXT	229	3	10x top metal 2 Text Layer, label text
133	MTT1TXT	230	3	MTT1 Text Layer, label text
134	MTT2TXT	231	3	MTT2 Text Layer, label text
135	ALPATXT	83	2	ALPA Text Layer, label text
136	SUBTXT	161	0	Substrate Pin Text Layer
137	WELTXT	162	0	Wells Pin Text Layer
138	DIFTXT	163	0	Diffusion Pin Text Layer
139	POLYTXT	164	0	Poly Pin Text Layer
140	TTXT	87	0	Text for Top Structure
141	BTXT	88	0	Text for Block
142	CTXT	89	0	Text for Cell

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 19/306
---------------------------	---	------------	----------------------	------------------

Sequence No	Layer name	GDS No	Data Type	Description
143	0M	1	0	Dummy layer for SMIC internal design switch layer
144	DUMBA	91	0	Block Layer for Dummy operation on AA
145	DUMBp	92	0	Block Layer for Dummy operation on poly
146	M1DUB	151	1	Metal-1 Dummy Block layer for M1 dummy fill
147	M2DUB	152	1	Metal-2 Dummy Block layer for M2 dummy fill
148	M3DUB	153	1	Metal-3 Dummy Block layer for M3 dummy fill
149	M4DUB	154	1	Metal-4 Dummy Block layer for M4 dummy fill
150	M5DUB	155	1	Metal-5 Dummy Block layer for M5 dummy fill
151	M6DUB	156	1	Metal-6 Dummy Block layer for M6 dummy fill
152	M7DUB	157	1	Metal-7 Dummy Block layer for M7 dummy fill
153	M8DUB	158	1	Metal-8 Dummy Block layer for M8 dummy fill
154	B1DUB	141	6	2x Metal-1 Dummy Block layer for 2x Metal-1 dummy fill
155	B2DUB	142	6	2x Metal-2 Dummy Block layer for 2x Metal-2 dummy fill
156	TM1DUB	193	1	8x top Metal 1 Dummy Block layer for TM1 dummy fill
157	TM2DUB	194	1	8x top Metal 2 Dummy Block layer for TM2 dummy fill
158	STM1DB	194	5	10x top Metal 1 Dummy Block layer for TM1 dummy fill
159	STM2DB	194	4	10x top Metal 2 Dummy Block layer for TM2 dummy fill
160	MTT2DB	194	2	MTT2 Dummy block layer for MTT2 dummy fill
161	ALDUB	83	6	ALPA Dummy block layer for ALPA dummy fill
162	DUMBM	90	0	Block Layer for all Metal layer dummy fill in RF device region
163	V1DUB	70	6	Via-1 Dummy Blockage.
164	V2DUB	71	6	Via-2 Dummy Blockage.
165	V3DUB	72	6	Via-3 Dummy Blockage.
166	V4DUB	73	6	Via-4 Dummy Blockage.
167	V5DUB	74	6	Via-5 Dummy Blockage.
168	V6DUB	75	6	Via-6 Dummy Blockage.
169	V7DUB	76	6	Via-7 Dummy Blockage.
170	V1RB	70	8	Via-1 blockage layer to skip redundant via insertion
171	V2RB	71	8	Via-2 blockage layer to skip redundant via insertion
172	V3RB	72	8	Via-3 blockage layer to skip redundant via insertion
173	V4RB	73	8	Via-4 blockage layer to skip redundant via insertion
174	V5RB	74	8	Via-5 blockage layer to skip redundant via insertion
175	V6RB	75	8	Via-6 blockage layer to skip redundant via insertion
176	V7RB	76	8	Via-7 blockage layer to skip redundant via insertion
177	W0RB	225	8	2xVia 1 blockage layer to skip redundant via insertion
178	W1RB	226	8	2xVia 2 blockage layer to skip redundant via insertion
179	TV1RB	121	8	8x top via1 blockage layer to skip redundant via insertion

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 20/306
---------------------------	---	------------	----------------------	------------------

Sequence No	Layer name	GDS No	Data Type	Description
180	TV2RB	123	8	8x top via1 blockage layer to skip redundant via insertion
181	STV1RB	243	8	10x top via1 blockage layer to skip redundant via insertion
182	STV2RB	244	8	10x top via1 blockage layer to skip redundant via insertion
183	V1RM	70	10	V1 mark layer to identify redundant via
184	V2RM	71	10	V2 mark layer to identify redundant via
185	V3RM	72	10	V3 mark layer to identify redundant via
186	V4RM	73	10	V4 mark layer to identify redundant via
187	V5RM	74	10	V5 mark layer to identify redundant via
188	V6RM	75	10	V6 mark layer to identify redundant via
189	V7RM	76	10	V7 mark layer to identify redundant via
190	W0RM	225	10	2xVia 1 mark layer to identify redundant via
191	W1RM	226	10	2xVia 2 mark layer to identify redundant via
192	TV1RM	121	10	8x top via1 mark layer to identify redundant via
193	TV2RM	123	10	8x top via1 mark layer to identify redundant via
194	STV1RM	243	10	10x top via1 mark layer to identify redundant via
195	STV2RM	244	10	10x top via1 mark layer to identify redundant via
196	M1B	151	0	Metal-1 Blockage Layer(For Place & Route use)
197	M2B	152	0	Metal-2 Blockage Layer(For Place & Route use)
198	M3B	153	0	Metal-3 Blockage Layer(For Place & Route use)
199	M4B	154	0	Metal-4 Blockage Layer(For Place & Route use)
200	M5B	155	0	Metal-5 Blockage Layer(For Place & Route use)
201	M6B	156	0	Metal-6 Blockage Layer(For Place & Route use)
202	M7B	157	0	Metal-7 Blockage Layer(For Place & Route use)
203	M8B	158	0	Metal-8 Blockage Layer(For Place & Route use)
204	B1B	181	150	B1 Blockage Layer(For Place & Route use)
205	B2B	181	151	B2 Blockage Layer(For Place & Route use)
206	TM1B	193	0	First 8x Top Metal Blockage Layer(For Place &Route use).
207	TM2B	194	0	Second 8x Top Metal Blockage Layer(For Place &Route use).
208	STM1B	181	152	STM1 Blockage Layer(For Place & Route use)
209	STM2B	181	153	STM2 Blockage Layer(For Place & Route use)
210	MTT2B	181	155	MTT2 Blockage Layer(For Place & Route use)
211	ALPAB	181	156	ALPA Blockage Layer(For Place & Route use)
212	VSIA	63	63	VSIA tagging layer(Text Only)
213	DMPNP	134	0	LVS mark layer for BJT
214	GTFUSE	81	1	LVS marking to identify the E-Fuse function area
215	PWMK1	89	165	Marking layer for EDA modeling
216	MOMP1	211	3	MOM capacitor mesh terminal one
217	MOMP2	211	4	MOM capacitor mesh terminal one

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 21/306
---------------------------	---	------------	----------------------	------------------

Sequence No	Layer name	GDS No	Data Type	Description
218	MOMMES	211	5	MOM capacitor mesh LVS marking layer
219	TGV	125	1	Marking layer for 2.5V under drive 1.8V IO device
220	OVERDR	125	3	Marking layer for 2.5V over drive 3.3V IO device
221	DGV	29	1	Marking layer for 1.8V under drive to 1.2V IO device
222	ZVT	159	6	Marking layer for core zero VT native device
223	FUSEMK1	81	152	Marking layer for fuse bitcell
224	RFMK1	181	6	Marking layer for RF device
225	DCTY	139	0	Marking layer for non-LVS check
226	P2DUB	31	6	P2 dummy blockage(for dummy P2 insertion) and exclude dummy insertion
227	RFMOM	211	6	LVS mark layer for RF MOM
228	INDR	212	1	LVS mark layer for inductor radius calculation
229	FUSEAD	81	4	Marking layer for fuse anode side
230	ESDCLP	41	2	Marking layer for ESD RC-triggered power clamp structures connected to a power supply pad
231	ESDPOB	41	8	Marking layer for Poly-bound ESD diode
232	CLPDMDY	87	2	Marking layer for STI ESD diode
233	LBESD	41	7	Marking layer used to identify input/output pads in ESD/latch up DRC decks
234	LDNMK1	131	170	Marking layer of metal low density area
235	OCCD	91	4	Marking layer of chip CD
236	OCOVL	91	5	Marking layer of chip OVL
237	OCCDFH	91	6	Marking layer of horizontal direction FEOL OCCD cell
238	OCCDFV	91	7	Marking layer of vertical direction FEOL OCCD cell
239	OCCDFDB	91	8	FEOL OCCD cell block layer
240	OCCDBDB	91	9	BEOL OCCD cell block layer
241	OCCDB	91	10	Marking layer of BEOL OCCD cell
242	VDDMK1	131	175	Marking layer for Power (Vdd) PAD for DRC use
243	VSSMK1	131	176	Marking layer for Power (Vss) PAD for DRC use
244	LUWMK1	131	177	Marking layer to waive latch up rules
245	PRBOUN	127	1	PR Boundary layer
246	ERCMK1	131	12	LVS ERC mark layer to waive floating gate violation
247	RFDN5T	181	7	LVS mark layer for 5-terminal RF MOS in deep NWELL, the fifth terminal is DNW.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 22/306
---------------------------	---	------------	----------------------	------------------

7.1.9 SMIC Mask layer Mapping Table

32nm POLY SION Top tier is LCMO28-V01

Mask ID	Process Name	Dig. Area Tone	Drawn	Description	Layers in Logic Operation Formula
120	AA	D	Generated	Active Area/SDG	AA,AADMP,AADUM,AADOP
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	DNW
192	NW	C	Drawn	N-Well / N-Tub	NW
191	PW	C	Generated	P-Well / P-Tub	NW,PSUB,INST,DG,TG
491	PWH	C	Generated	P well I/O	NW,PSUB,DG,TG,RESAA
492	NWH	C	Generated	N well I/O	NW,DG,TG,RESAA
296	MVN	C	Generated	Core NMOS Vt IMP	NW, PSUB, DG, TG, INST
146	SDOP	C	Drawn	HV SD open (for LDMOS)/SRAM PG device block layer	SDOP
131	DG	D	Generated	Dual Gate	DG,TG
412	HR	C	Generated	N+ poly Pre-doping	SN,INST,NW,EFUSE,HRBL,RESP1
413	HRP	C	Generated	P+ poly Pre-doping	SP,INST,RESP1,DG,TG,EFUSE, HRBL
130	GT	D	Generated	Poly	GT,GTDMP,GTDUM,GTDOP,SN, DG,TG
132	P2	C	Drawn	Poly trim slot	P2,P2DUM,P2DOP
193	NC	C	Generated	N-Cell Implant	SN,NW,INST,DPSRAM,NLDB,LVT_N
194	PC	C	Generated	P-Cell Implant/NFILED	SP,INST,NW,PLDB,LVT_P
322	NDRN	C	Generated	Core native device LDD	SN,NW, PSUB,DG,TG,LVT_N, INST, RESAA,RESNW,RESP1, VARMOS,NLDB,EFUSE,BIPOLA
596	LVN	C	Generated	Low VT NMOS/NMOS LDD Implant for LV	SN,NW,LVT_N,,RESAA,RESNW, RESP1,BIPOLA,VARMOS,NLDB
595	LVP	C	Generated	Low VT PMOS/PMOS LDD Implant for LV	SP,NW,LVT_P,RESAA,RESNW, RESP1,BIPOLA,VARMOS,PLDB
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	SN,NW,DG,TG,PSUB,LVT_N, INST,RESAA,RESNW,RESP1, VARMOS,NLDB,EFUSE,BIPOLA, DPSRAM
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	SP,NW,DG,TG,LVT_P,INST, RESAA,RESNW,RESP1,VARMOS, PLDB,EFUSE,BIPOLA
114	NLH	C	Generated	NMOS LDD Implant for High VDD	SN,NW,DG,TG,INST,RESAA,RES NW,RESP1,VARMOS, BIPOLA,NLDB
115	PLH	C	Generated	PMOS LDD Implant for High VDD	SP,NW,DG,TG,INST,RESAA, RESNW,RESP1,VARMOS, BIPOLA,PLDB

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 23/306
---------------------------	---	------------	----------------------	------------------

Mask ID	Process Name	Dig. Area Tone	Drawn	Description	Layers in Logic Operation Formula
594	ULVN	C	Generated	ULVT NMOS LDD IMP	SN,NW,ULVT_N,RESAA,REANW,RESP1,BIPOLA,VARMOS,NLDB
593	ULVP	C	Generated	ULVT NMOS LDD IMP	SP,NW,ULVT_P,RESAA,REANW,RESP1,BIPOLA,VARMOS,PLDB
201	PSR	C	Generated	PMOS recess/eSiGe PFET Si recess(GS)	SP,NW,DG,TG,RESAA,RESNW,BIPOLA,DSTR,RESP1,VARMOS,PSRBL,PSRDUM,AA
200	NSR	C	Generated	NMOS recess/N+ P1 Resistor2	SP,NW,DG,TG,RESAA,RESNW,BIPOLA,DSTR,RESP1,VARMOS,PSRBL,PSRDUM,AA
197	SP	C	Generated	P+ S/D Implant	SP,NW,INST,SPBLE,EFUSE
198	SN	C	Generated	N+ S/D Implant	SN,INST,SNBL,DPSRAM
298	NPCI	C	Generated	N+ contact implant	SN,INST,DPSRAM,NW,SNBL
110	ESD1	C	Drawn	ESD Implant	ESD1
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	SAB
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	CT
160	M1	C	Generated	Metal-1	M1,M1DUM,M1DOP
178	V1	C	Generated	Via-1 Hole	V1,V1DUM
180	M2	C	Generated	Metal-2	M2,M2DUM,M2DOP
179	V2	C	Generated	Via-2 Hole	V2,V2DUM
181	M3	C	Generated	Metal-3	M3,M3DUM,M3DOP
177	V3	C	Generated	Via-3 Hole	V3,V3DUM
182	M4	C	Generated	Metal-4	M4,M4DUM,M4DOP
176	V4	C	Generated	Via-4 Hole	V4,V4DUM
183	M5	C	Generated	Metal-5	M5,M5DUM,M5DOP
175	V5	C	Generated	Via-5 Hole	V5,V5DUM
184	M6	C	Generated	Metal-6	M6,M6DUM,M6DOP
174	V6	C	Generated	Via-6 Hole	V6,V6DUM
185	M7	C	Generated	Metal-7	M7,M7DUM,M7DOP
173	V7	C	Generated	Via-7 Hole	V7,V7DUM
186	M8	C	Generated	Metal-8	M8,M8DUM,M8DOP
270	W0	C	Generated	2xVia-1	W0
280	B1	C	Generated	2xMetal-1	B1, B1DUM
271	W1	C	Generated	2xVia-2	W1
281	B2	C	Generated	2xMetal-2	B2, B2DUM
142	TV1	C	Drawn	8x Top Via1	TV1
141	TM1	C	Generated	8x Top Metal	TM1,TM1DUM
144	TV2	C	Drawn	8x Top Top Via2	TV2

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 24/306
---------------------------	---	------------	----------------------	------------------

Mask ID	Process Name	Dig. Area Tone	Drawn	Description	Layers in Logic Operation Formula
143	TM2	C	Generated	8x Top Top Metal2	TM2,TM2DUM
442	STV1	C	Drawn	10x Top Via1	STV1
441	STM1	C	Generated	10x Top Metal	STM1,STM1DM
444	STV2	C	Drawn	10x Top Top Via2	STV2
443	STM2	C	Generated	10x Top Top Metal2	STM2,STM2DM
107	PA	C	Generated	Passivation / Pad	PA
108	ALPA	D	Generated	AL Bonding Pad	ALPA,PA,ALDUM
163	MD	C	Drawn	Metal about top metal for redistribution, Passivation 2	MD
240	LT	C	Drawn	8x UTV	LT
543	MTT2	C	Generated	Second Ultra Thick Top Metal	MTT2,MTT2DM

Note: Please refer DCC document **PM-DATA-02-2001** layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 25/306
---------------------------	---	------------	----------------------	------------------

7.1.10 Device Layout Truth Table

Drawing layer name																											
Drawing layer GDS No																											
Drawing layer GDS data type		Spice Model Name																									
Core	1.05V NMOS Regular VT	n105ll_ckt/n105ll_dnw_ckt	0	0	10	AA	0	0	19	DNW	NW	14	158	LVT_N	159	LVT_P	DG	29	DGUD	DGV	TG	OVERDR	TQV	GT	SP	SN	
	1.05V PMOS Regular VT	p105ll_ckt	1	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1.05V NMOS Low VT	nlvt105ll_ckt/nlvt105ll_dnw_ckt	1	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1.05V PMOS Low VT	plvt105ll_ckt	1	*	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
I/O 1.8V	1.8V NMOS Regular VT	n18ll_ckt/n18ll_dnw_ckt	1	*	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1.8V PMOS Regular VT	p18ll_ckt	1	*	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
I/O 1.5V(1.8V underdrv)	1.8V underdrive 1.5V NMOS	n18ud15ll_ckt/n18ud15ll_dnw_ckt	1	*	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1.8V underdrive 1.5V PMOS	p18ud15ll_ckt	1	*	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
I/O 1.2V(1.8V underdrv)	1.8V underdrive 1.2V NMOS	n18ud12ll_ckt/n18ud12ll_dnw_ckt	1	*	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	1.8V underdrive 1.2V PMOS	p18ud12ll_ckt	1	*	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
I/O 2.5V	2.5V NMOS Regular VT	n25ll_ckt/n25ll_dnw_ckt	1	*	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Semiconductor Manufacturing International Corporation

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 26/306
---------------------------	---	------------	----------------------	------------------

Drawing layer name				AA	DNW	NW	LVT_N	LVT_P	DG	DGUD	DGV	TG	TGVR	GT	SP	SN	PSUB	ZVT	SAB	CT	INST	STSRAM	LRSRAM	DPSRAM	2PSRAM	6TMK	UDSRAM	HPBL	RESP1	PLRES	RESNW	RESAA	DIFRES	VARMOS	DSTR	LDBK	GTFUSE	EFUSE	FUSEAD	INDMY	MOMDDMY	BIPOLA	SDOP
Drawing layer GDS No				0	10	0	19																																				
Drawing layer GDS data type		Spice Model Name		0	0	0	14																																				
2.5V PMOS Regular VT		p25ll_ckt		1	*	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									
I/O 3.3V(2.5V overdrv)	2.5V overdrive 3.3V NMOS	n25od33ll_ckt/n25od33ll_dnw_ckt		1	*	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
I/O 1.8V(2.5V underdrv)	2.5V overdrive 3.3V PMOS	p25od33ll_ckt		1	*	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
I/O 1.8V(2.5V underdrv)	2.5V underdrive 1.8V NMOS	n25ud18ll_ckt/n25ud18ll_dnw_ckt		1	*	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
I/O 1.8V(2.5V underdrv)	2.5V underdrive 1.8V PMOS	p25ud18ll_ckt		1	*	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
Native NMOS	1.05V NMOS ZVT	nzvt105ll_ckt		1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0										
	1.05V NMOS Native VT	nt105ll_ckt		1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0										
	1.8V NMOS Native VT	nt18ll_ckt		1	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0										
	2.5V NMOS Native VT	nt25ll_ckt		1	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0										
SRAM D127	Pull Up	stpl_ckt		1	*	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	*	0								
	Pull Down	stnpld_ckt		1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	*	0									
	Pass Gate	stnpg_ckt		1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	*	0									
SRAM D155	Pull Up	lrpl_ckt		1	*	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	*	0									
	Pull Down	lrnpld_ckt		1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	*	0									

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 27/306
---------------------------	---	------------	----------------------	------------------

Drawing layer name				AA	DNW	NW	LVT_N	LVT_P	DG	DGUD	DGV	TG	OVERDR	TGV	GT	SP	SN	PSUB	ZVT	SAB	CT	INST	STSRAM	LRSRAM	DPSRAM	2PSRAM	6TMK	UDSRAM	HPBL	RESP1	PLRES	RESNW	RESAA	DIFRES	VARMOS	DSTR	LDBK	GTIFUSE	EFUSE	FUSEAD	INDMY	MOMDDMY	BIPOLA	SDOP
Pass Gate	lrnpg_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	1
Pull Up	tplrpl_ckt	1	*	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0
Pull Down	tplrnpd_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0
Pass Gate1	tplrnpg_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	1	
Read Port	tplrnrdp_ckt,tplrnrg_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0
Pull Up	tplvpl_ckt	1	*	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0
Pull Down	tplvndp_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0	
Pass Gate1	tplvnpg_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	1		
Read Port	tplvnrdp_ckt,tplvnrg_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0	
Pull Up	dppl_ckt	1	*	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0	
Pull Down	dppnd_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0		
Pass Gate1	dppnga_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	1		
Pass Gate2	dppngb_ckt	1	*	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	1		
N+ Poly Silicided Resistor	rnpo_2t_ckt/rnpo_3t_ckt	0	*	*	0	0	*	0	0	*	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0			
N+ Poly Non-silicided Resistor	rnposab_2t_ckt/rnposab_3t_ckt	0	*	*	0	0	*	0	0	*	0	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0			
P+ Poly Silicided	rppo_2t_ckt/rppo_3t_ckt	0	*	*	0	0	*	0	0	*	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0				

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 28/306
---------------------------	---	------------	----------------------	------------------

Drawing layer name				AA	DNW	NW	LVT_N	LVT_P	DG	DGUD	DGV	TG	OVERDR	TGV	GT	SP	SN	PSUB	ZVT	SAB	CT	INST	STSRAM	LRSRAM	DPSRAM	2PSRAM	6TMK	UDSRAM	HPBL	RESP1	PLRES	RESNW	RESAA	DIFRES	VARMOS	DSTR	LDBK	GTFUSE	EFUSE	FUSEAD	INDMY	MOMDDMY	BIPOLA	SDOP
Resistor		Spice Model Name		0	0	19																																						
P+	Poly	rpposab_2t_ckt/rpposab_3t_ckt	0	*	*	0	0	*	0	0	*	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									
Non-silicided Resistor																																												
AA resistor portion	N+ Diffusion Silicided Resistor	rndif_2t_ckt/rndif_3t_ckt	1	*	0	0	0	*	0	0	*	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
	N+ Diffusion Non-silicided Resistor	rndifsab_2t_ckt/rndifsab_3t_ckt	1	*	0	0	0	*	0	0	*	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
	P+ Diffusion Silicided Resistor	rpdif_2t_ckt/rpdif_3t_ckt	1	*	1	0	0	*	0	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
	P+ Diffusion Non-silicided Resistor	rpdifsab_2t_ckt/rpdifsab_3t_ckt	1	*	1	0	0	*	0	0	*	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
N-Well resistor portion	NW Diffusion Resistor	rnwaa_2t_ckt/rnwaa_3t_ckt	1	0	1	0	0	*	0	0	*	0	0	0	0	*	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
	NW STI Resistor	rnwsti_2t_ckt/rnwsti_3t_ckt	0	0	1	0	0	*	0	0	*	0	0	0	0	*	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
BJT (Vertical BJT)	NPN (NPN105A4)	npn105a2d56ll_ckt npn105a4ll_ckt npn105a25ll_ckt npn105a100ll_ckt	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION)	Doc. Rev. 2	Tech Dev Rev: 1.10.1	Page No.: 29/306
TD-LO28-DR-2006	1.05V/1.8V/2.5V Design Rules				

Drawing layer name			AA	DNW	NW	LVT_N	LVT_P	DG	DGUD	DGV	TG	OVERDR	TGV	GT	SP	SN	PSUB	ZVT	SAB	CT	INST	STSRAM	LRSRAM	DPSRAM	2PSRAM	6TMK	UDSRAM	HPBL	RESP1	PLRES	RESNW	RESAA	DIFRES	VARMOS	EFuse	DSTR	FUSEAD	INDMY	MOMDDMY	BIPOLA	SDOP
Drawing layer GDS No			0	10	0	19																																			
Drawing layer GDS data type		Spice Model Name	0	1	0	158	159	168	159	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
NPN_IO (NPN18A4)		npn18a2d56ll_ckt npn18a4ll_ckt npn18a25ll_ckt npn18a100ll_ckt	1	1	1	0	0	0	1	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
NPN_IO (NPN25A4)		npn25a2d56ll_ckt npn25a4ll_ckt npn25a25ll_ckt npn25a100ll_ckt	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
PNP (PNP105A4)		pnp105a2d56ll_ckt pnp105a4ll_ckt pnp105a25ll_ckt pnp105a100ll_ckt	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
PNP_IO (PNP18A4)		pnp18a2d56ll_ckt pnp18a4ll_ckt pnp18a25ll_ckt pnp18a100ll_ckt	1	0	1	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
PNP_IO (PNP25A4)		pnp25a2d56ll_ckt pnp25a4ll_ckt pnp25a25ll_ckt pnp25a100ll_ckt	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Diode	P+/Nwell_Core (1.05V)	P+ Nwell	pdio105ll	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Semiconductor Manufacturing International Corporation

Doc.	No.:	Doc.	28nm Logic Low Power (Poly/SION)	Doc.Rev:	Tech Dev	Page No.:
TD-LO28-DR-2006		Title:	1.05V/1.8V/2.5V Design Rules	2	Rev: 1.10.1	30/306

Drawing layer name			AA	DNW	NW	LVT_N	LVT_P	DG	DGUD	DGV	TG	OVERDR	TGV	GT	SP	SN	PSUB	ZVT	SAB	CT	INST	STSRAM	LRSRAM	DPSRAM	2PSRAM	6TMK	UDSRAM	HPBL	RESP1	PLRES	RESNW	RESAA	DIFRES	VARMOS	DSTR	LDBK	GTIFUSE	EFUSE	FUSEAD	INDMY	MOMDDMY	BIPOLA	SDOP	
Drawing layer GDS No																																												
Drawing layer GDS data type		Spice Model Name																																										
LVT P+/Nwell_Core (1.05V)	P+	pdio105llvt	0	0	0	19	DNW																																					
	Nwell		1	0	1	0	158	159	LVT_N	LVT_P																																		
P+/Nwell_IO (1.8V)	P+	pdio18ll	1	0	1	0	0	168	159	DGUD	DGV	TG	OVERDR	TGV	GT	SP	SN	PSUB	ZVT	SAB	CT	INST	STSRAM	LRSRAM	DPSRAM	2PSRAM	6TMK	UDSRAM	HPBL	RESP1	PLRES	RESNW	RESAA	DIFRES	VARMOS	DSTR	LDBK	GTIFUSE	EFUSE	FUSEAD	INDMY	MOMDDMY	BIPOLA	SDOP
	Nwell		1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
P+/Nwell_IO (2.5V)	P+	pdio25ll	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
	Nwell		1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
N+/Pwell_Core (1.05V)	N+	ndio105ll	1	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
	Pwell		1	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
LVT N+/Pwell_Core (1.05V)	N+	ndio105llvt	1	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Pwell		1	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
N+/Pwell_IO (1.8V)	N+	ndio18ll	1	*	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Pwell		1	*	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
N+/Pwell_IO (2.5V)	N+	ndio25ll	1	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Pwell		1	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
ZVT Diode (1.05V)	N+	nzvtdio105ll	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
	Psub		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
Native Diode (1.05V)	N+	ntdio105ll	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Psub		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
Native Diode (1.8V)	N+	ntdio18ll	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
	Psub		1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
Native Diode (2.5V)	N+	ntdio25ll	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Semiconductor Manufacturing International Corporation

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	Tech Dev Rev: 1.10.1	Page No.: 31/306
TD-LO28-DR-2006			2		

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Semiconductor Manufacturing International Corporation

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 32/306
---------------------------	---	------------	----------------------	------------------

Notes:

1. For the ESD device, please refer to the ESD design guidelines.
2. The MOS device covered by ESDIO1 or ESDIO2 can have SAB layer as an option.
3. The “1” in device layout truth table is must drawn layer for device.
4. The “*” in device layout truth table is optional layer for device.
5. The “0” in device layout truth table is non-exist layer for device.

SMIC CONFIDENTIAL

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 33/306
---------------------------	---	------------	----------------------	------------------

7.1.11 Device table for dummy insertion

Designers can refer to below device table for dummy pattern insertion and need add dummy block layers to avoid dummy patterns insertion.

Dummy patterns device category	Marker Layer	GDS No.	AA Dummy	Poly Dummy	Inter Metal Dummy	Inter Via Dummy	Top Metal dummy	ALPA Dummy	Remark
LDMOS	LDBK	216; 150	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement.
SRAM	INST	60; 0	N	N	N	Y	Y	Y	M4 ~ M8, V3 ~ V7 dummy should be "Y" for INST.
	RFSRAM	60; 9	N	N	N	Y	Y	Y	M4 ~ M8, V3 ~ V7 dummy should be "Y" for RFSRAM.
AA Resistor	RESAA	97; 0	Y	N	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
NW Resistor	RESNW	95; 0	N	N	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
Poly Resistor	RESP1	96; 0	N	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
Diode	DSTR	138; 0	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
BJT	BIPOLA	159;1	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
MOS Varactor	VARMOS	93; 0	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
MOM	MOMDMY	211;1	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
Inductor	INDMY	212; 0	Y	Y	Y	N	Y	N	Designers can draw dummy block layer based on their requirement
e-fuse	GTFUSE	81;1	N	N	Y	Y	Y	Y	M1 ~ M2, V1 ~ V2 dummy should be "N" for GTFUSE.
Seal Ring	MARKS	189;151	N	N	N	N	N	N	
Guard Ring	MARKG	189; 0	N	N	N	N	N	N	

Y: do dummy filling by script automatically.

N: block dummy filling by marker layer of device, and will be defined in the dummy insertion rules to avoid dummy filling.

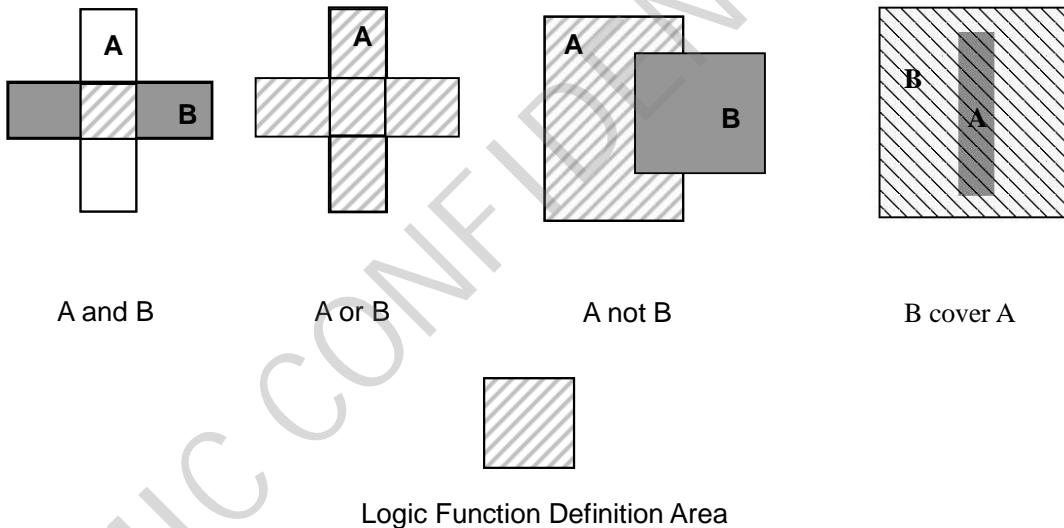
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 34/306
TD-LO28-DR-2006					

7.1.12 Design Rules Nomenclatures and Abbreviations

(A) Logic Function Definition

Logic Function	Definition
A and B	Define the intersection area of A and B.
A or B	Define the union area of A and B.
A not B	Define the area of A excluding the common area of A and B.
B cover A	Define the B area where there is A inside B.



Logic Function Definition Area

(B) Nomenclatures and Abbreviations

Name	Definitions
PW	(NOT (NW OR PSUB))
Poly	GT with GDS No (30;0)
GATE	GATE = AA AND poly
Channel Length	The dimension (from poly edge to poly edge) over AA.
Channel Width	The dimension (from AA edge to AA edge) over poly.
MOS AA	MOS AA refers to an AA that is part of a transistor active area. When a poly pattern is on top of an AA, the AA is treated as MOS AA. If there is no poly pattern on top of an AA, the AA is not a MOS AA. Dummy AA is not a MOS AA.
N+AA	((AA and SN) NOT NW)
P+AA	((AA and SP) AND NW)
N+ pick-up AA	((AA and SN) AND NW)
P+ pick-up AA	((AA and SP) NOT NW)

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	Tech Dev Rev:	Page No.:
TD-LO28-DR-2006			2	1.10.1	35/306

STI	Not (AA or AA dummy)
Share contact	Connects AA and poly, and the length is larger than the width, which is in INST/2PSRAM region.
Different or same net	Electrically based connectivity using all conducting layers (unless otherwise noted), including diffusion, poly, and all back-end-of-line (BEOL) metal and via layers in the stack (M1 through last metal). It also includes connectivity through the substrate, through n-wells and p-wells and between n-wells through the deep n-well (for triple-well designs).
Source/Drain	((AA INTERACT GATE) NOT (((poly OR GTDUM) OR GTDOP) OR GTDMP)) NOT Pick-up)
POLY_DMY	(GTDUM OR GTDOP) OR GTDMP)
AA_DMY	(AADUM OR AADOP) OR AADMP)
LDMOS drain	T

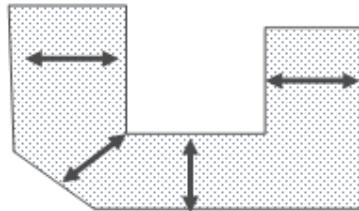
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 36/306
---------------------------	---	------------	----------------------	------------------

7.1.13 Definition of terminology used in these design rules

1. Width

- The distance of interior-facing sides of one layer edges.



2. Length

- Distance from one inside edge to a parallel inside edge within a same rectangular shape along the longer dimension of the shape.



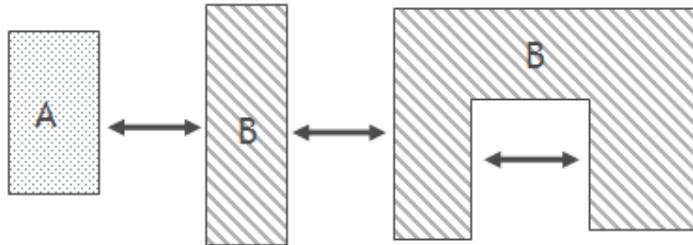
3. Line / Line-end

- (Poly or POLY_DMY) line: (Poly or POLY_DMY) edges with length > 0.1 um;
- (Poly or POLY_DMY) line-end: (Poly or POLY_DMY) edges with length ≤ 0.1 um



4. Space

- The distance of exterior-facing sides of one or two layer edges.

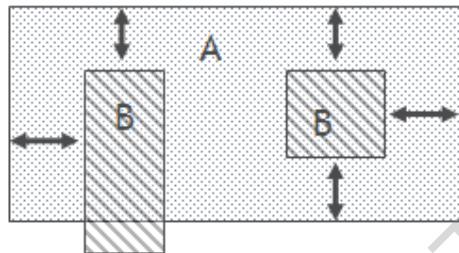


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

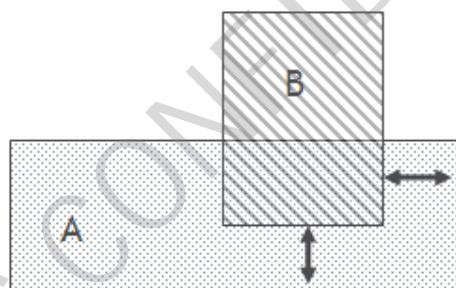
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 37/306
---------------------------	---	------------	----------------------	------------------

5. Enclosure

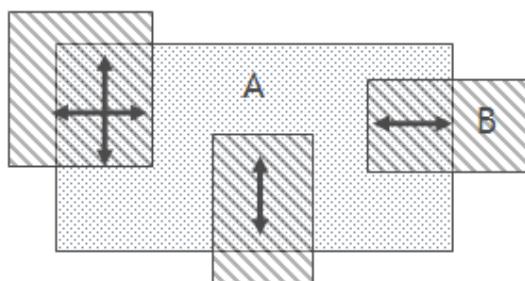
- The distance between the interior-facing sides of layer A edges and the exterior-facing sides of layer B edges.

**6. Extension**

- The distance between the interior-facing sides of layer A edges and the exterior-facing sides of layer B edges.

**7. Overlap**

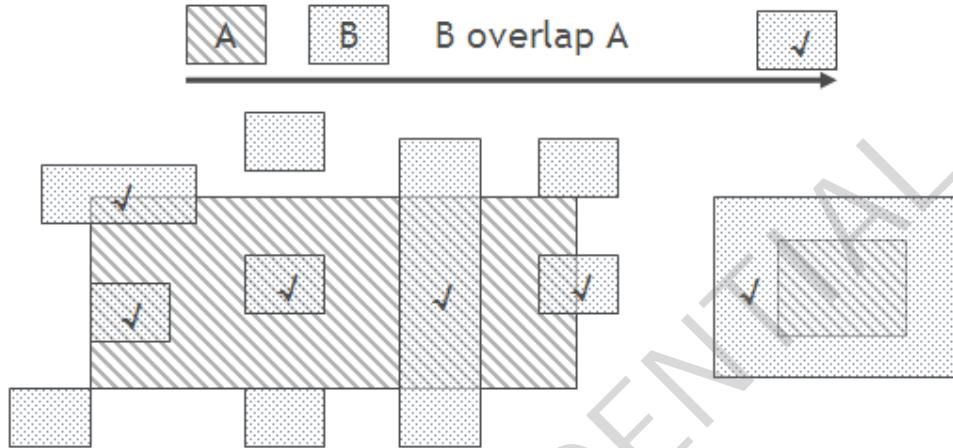
- For the overlap-required rule: The distance between the interior-facing sides of layer A edges and the interior-facing sides of layer B edges



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

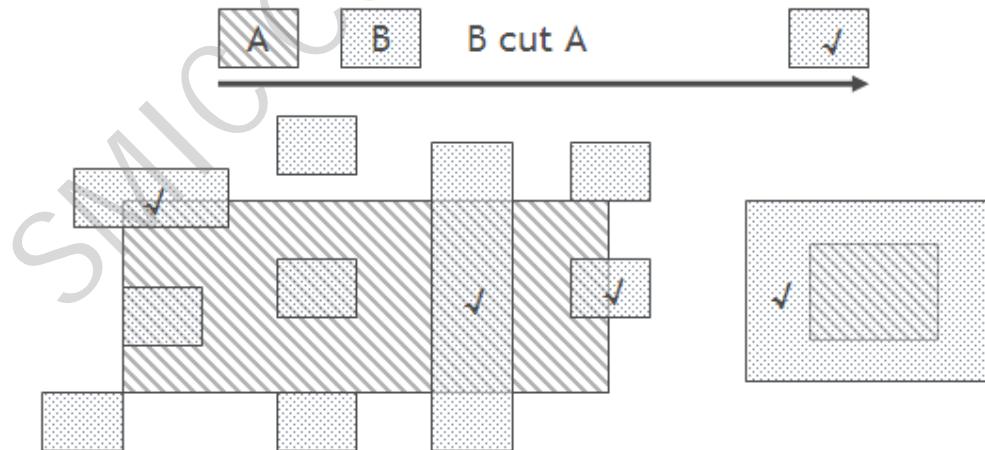
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 38/306
---------------------------	---	------------	----------------------	------------------

- For the non-overlap-required rule: Two layers share part (or all) of area.



8. Cut

- A cut B: A share part (not all) of area with B;
- B cut A: B share part (not all) of area with A.

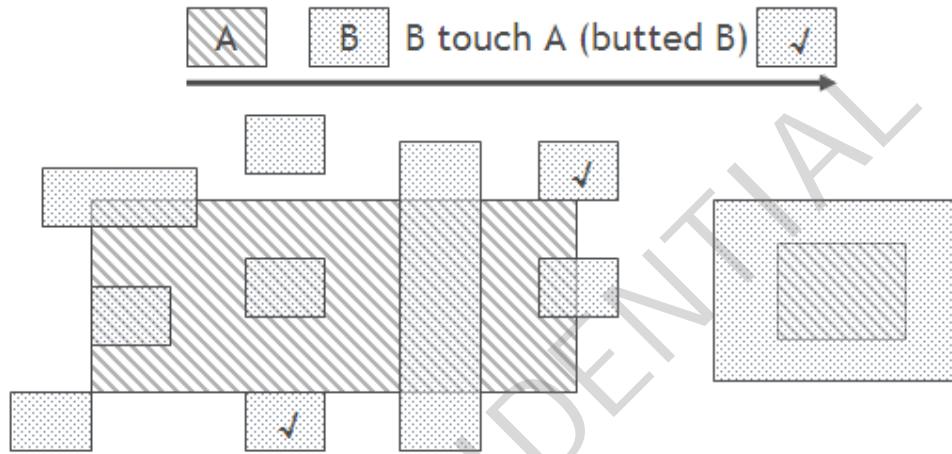


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

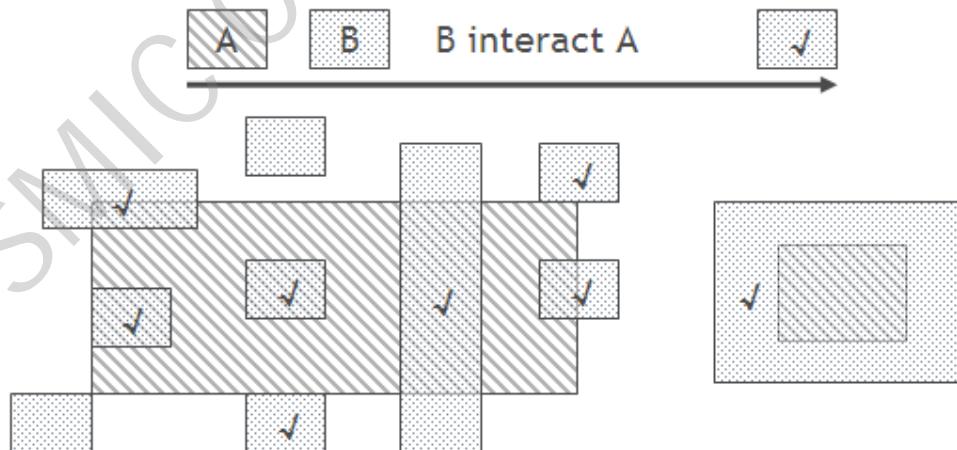
Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 39/306
-----------	-------------	--	------------	----------------------	------------------

9. Butted

- Butted A: A share at least one edge (or edge segment) with B from outside;
- Butted B: B share at least one edge (or edge segment) with A from outside;

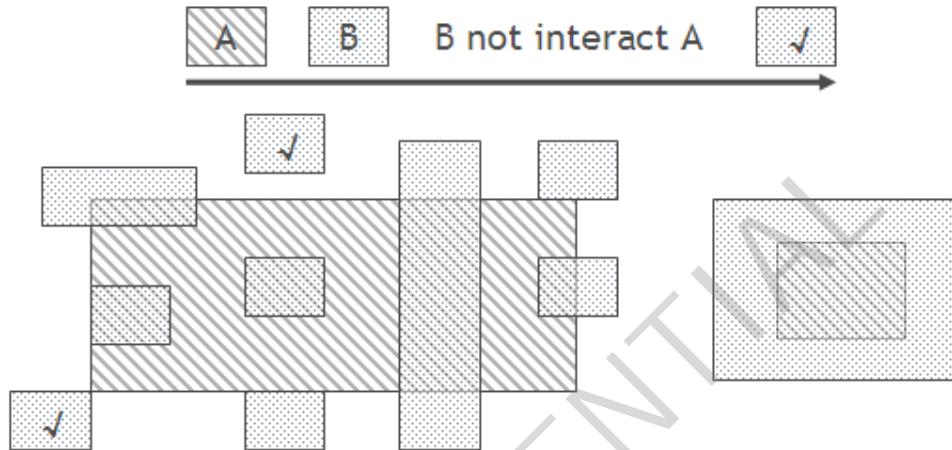
**10. Interact**

- A interact B: A touch or overlap B;
- B interact A: B touch or overlap A.

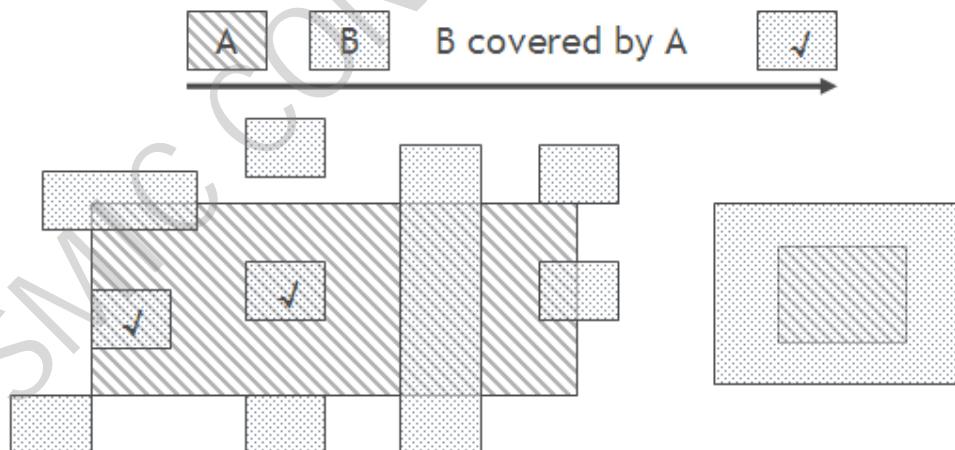


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 40/306
---------------------------	---	------------	----------------------	------------------

11. Not Interact**12. Cover**

- A covered by B: A share all area with B;
- B covered by A: B share all area with A;

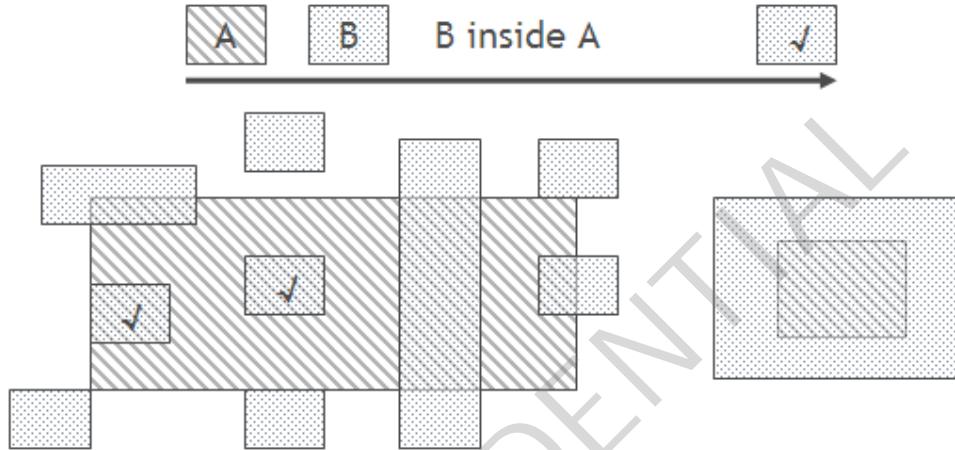
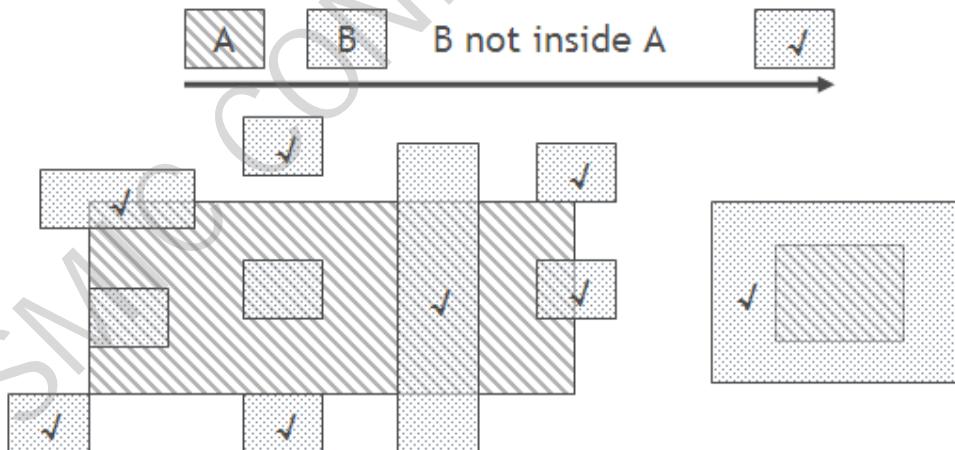


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 41/306
---------------------------	---	------------	----------------------	------------------

13. Inside

- A inside B (A covered by B): A share all area with B;
- B inside A (B covered by A): B share all area with A.

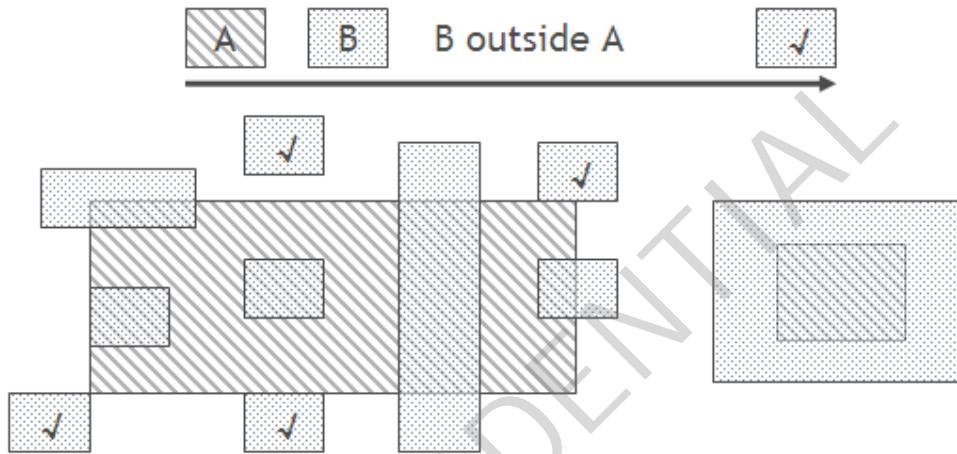
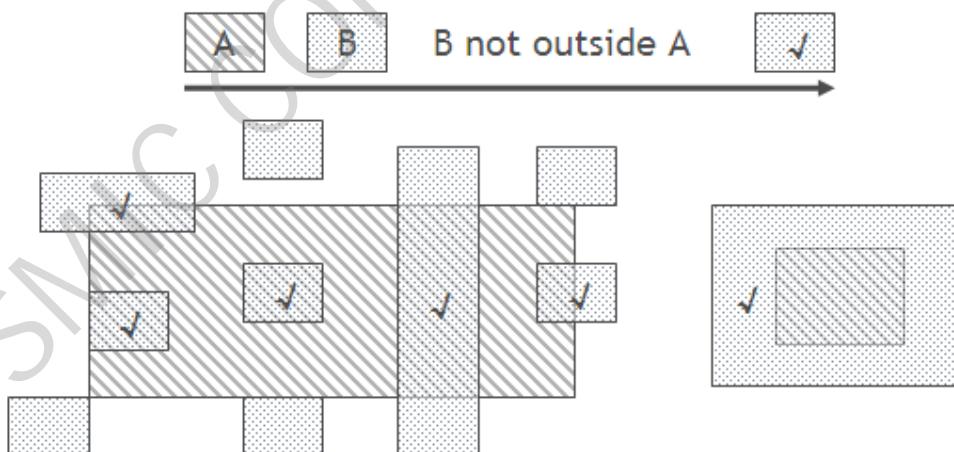
**14. Not Inside**

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 42/306
---------------------------	---	------------	----------------------	------------------

15. Outside

- A outside B: A doesn't share any area with B;
- B outside A: B doesn't share any area with A.

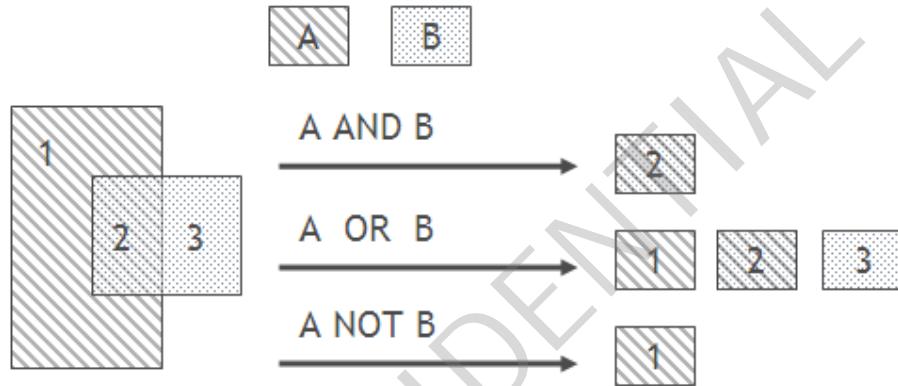
**16. Not Outside**

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

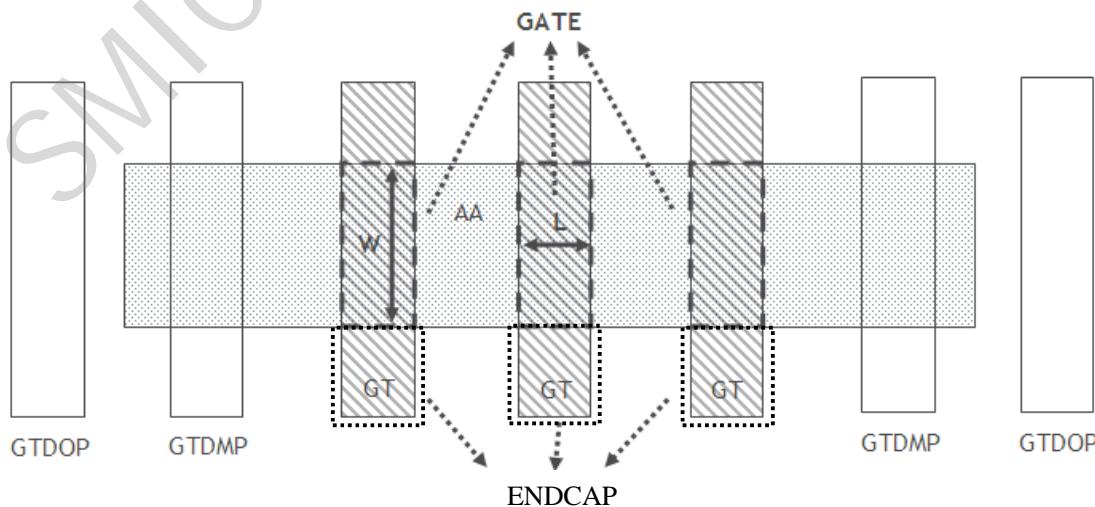
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 43/306
---------------------------	---	------------	----------------------	------------------

17. AND / OR / NOT

- A AND B: Output the shared area of A and B;
- A OR B: A and B merge as one layer;
- A NOT B: A exclude the shared area of A and B.

**18. GATE**

- GATE = AA AND poly;
- Channel Length (L in figure): The distance between interior-facing sides of poly edge segments inside AA;
- Channel Width (W in figure): The distance between interior-facing sides of AA edge segments inside poly;
- ENDCAP: poly extension outside GATE in the channel width direction.

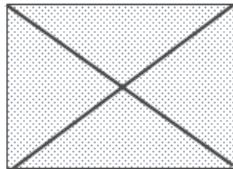


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

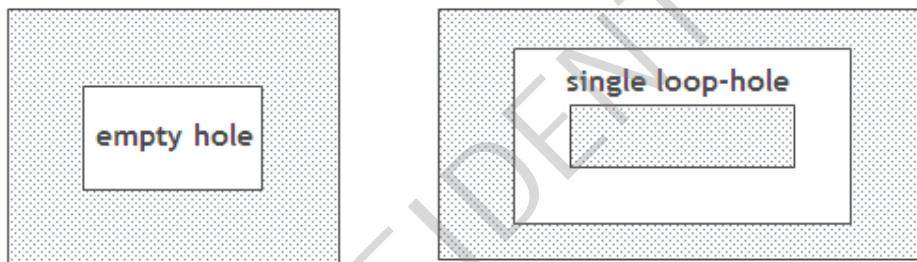
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 44/306
---------------------------	---	------------	----------------------	------------------

19. Area

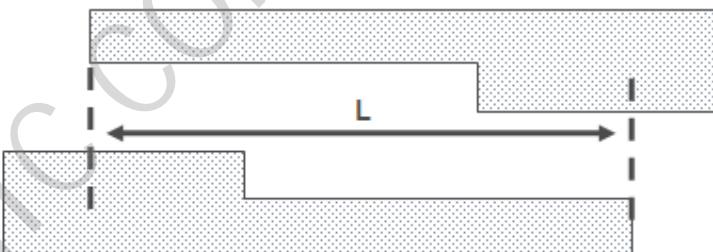
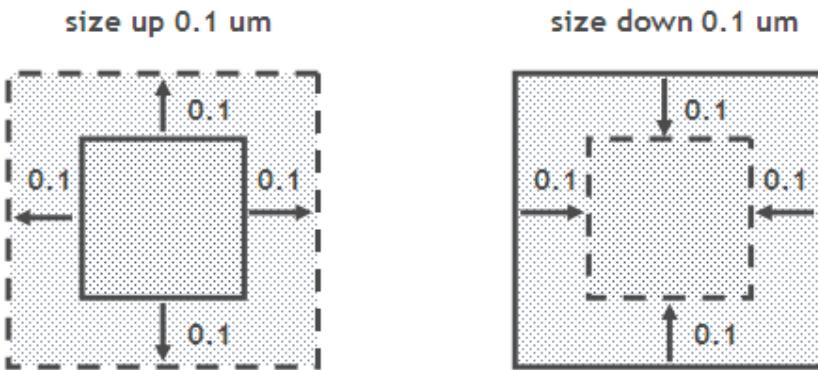
- The area of the polygon.

**20. Enclosed Area**

- The area of empty hole or single loop-hole.

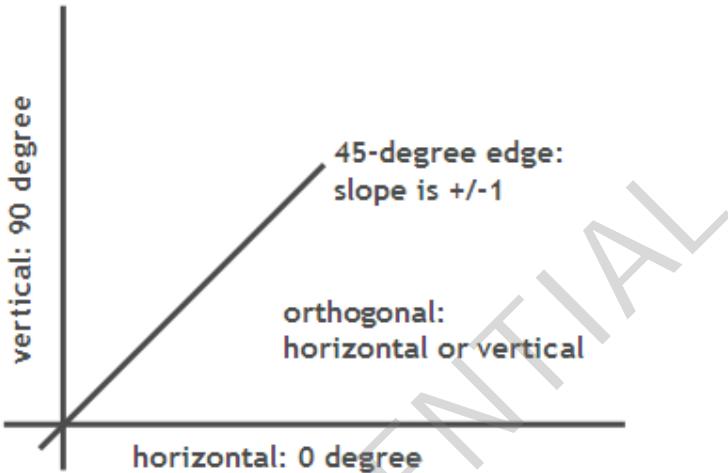
**21. Parallel Run Length**

- Projection length between two polygons.

**22. Size Up / Size Down**

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 45/306
---------------------------	---	------------	----------------------	------------------

23. Horizontal / Vertical / 45-degree / Orthogonal**24. Rectangle / Square**

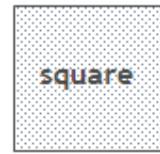
- Rectangle: Orthogonal polygon with 4 vertexes;
- Square: Rectangle with aspect ratio equal to 1.

rectangle: all edges are orthogonal, vertex = 4

rectangle with aspect ratio > 1



rectangle with aspect ratio = 1

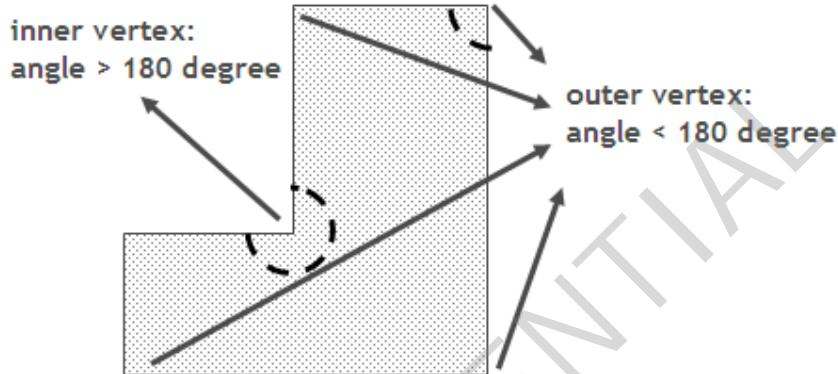
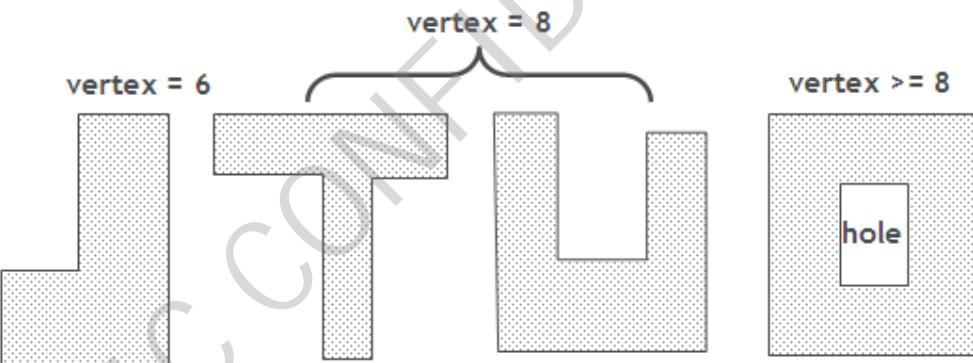


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

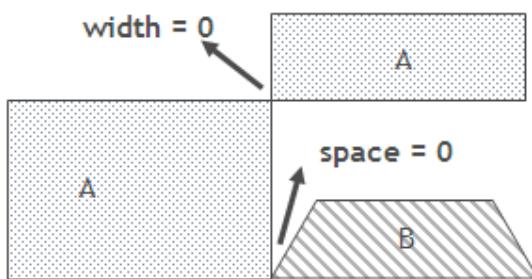
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 46/306
---------------------------	---	------------	----------------------	------------------

25. Vertex / Inner Vertex / Outer Vertex

- Inner Vertex (Concave Corner): angle > 180 degree measured inside polygon;
- Outer Vertex (Convex Corner): angle < 180 degree measured inside polygon.

**26. Single L/T/U-shape / O-shape****27. Single-Point-Interaction**

- One or two layers share one vertex from outside.

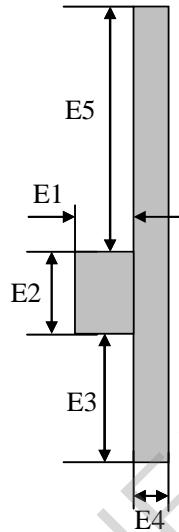


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 47/306
---------------------------	---	------------	----------------------	------------------

28. POLY_JOG

- The poly(30;0) jog with $0.03 \geq E1 \geq 0.005\mu m$, $0.09\mu m \geq E2 \geq 0.03\mu m$, $E3 \geq 0\mu m$, $E1+E4=0.06$, $E5 \geq 0.005\mu m$.

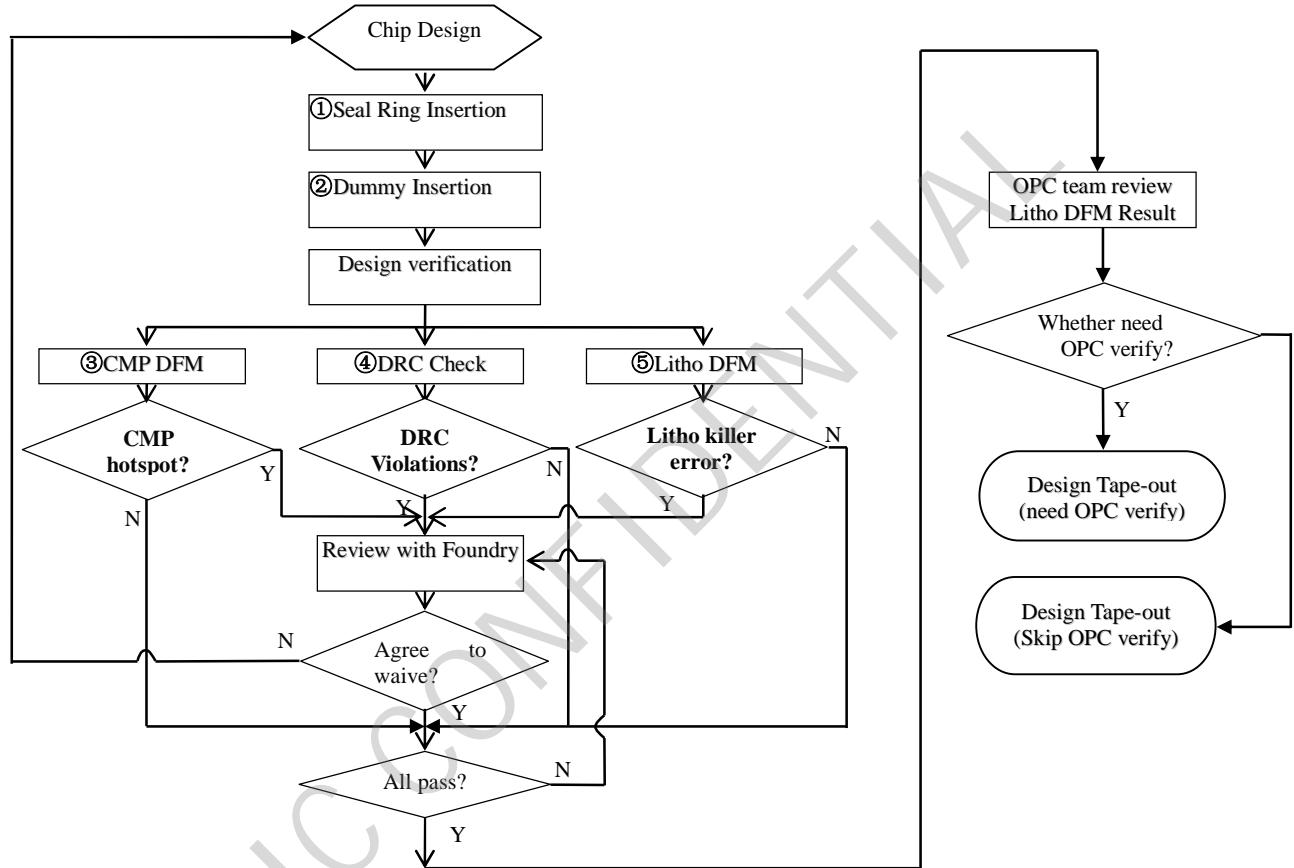


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	TD-LO28-DR-2006	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	2	Tech Dev Rev:	1.10.1	Page No.:	48/306
-----------	-----------------	-------------	--	----------	---	---------------	--------	-----------	--------

7.1.14 Design Check Flow for Tape out

7.1.14.1 Design Check Flow before Tape out



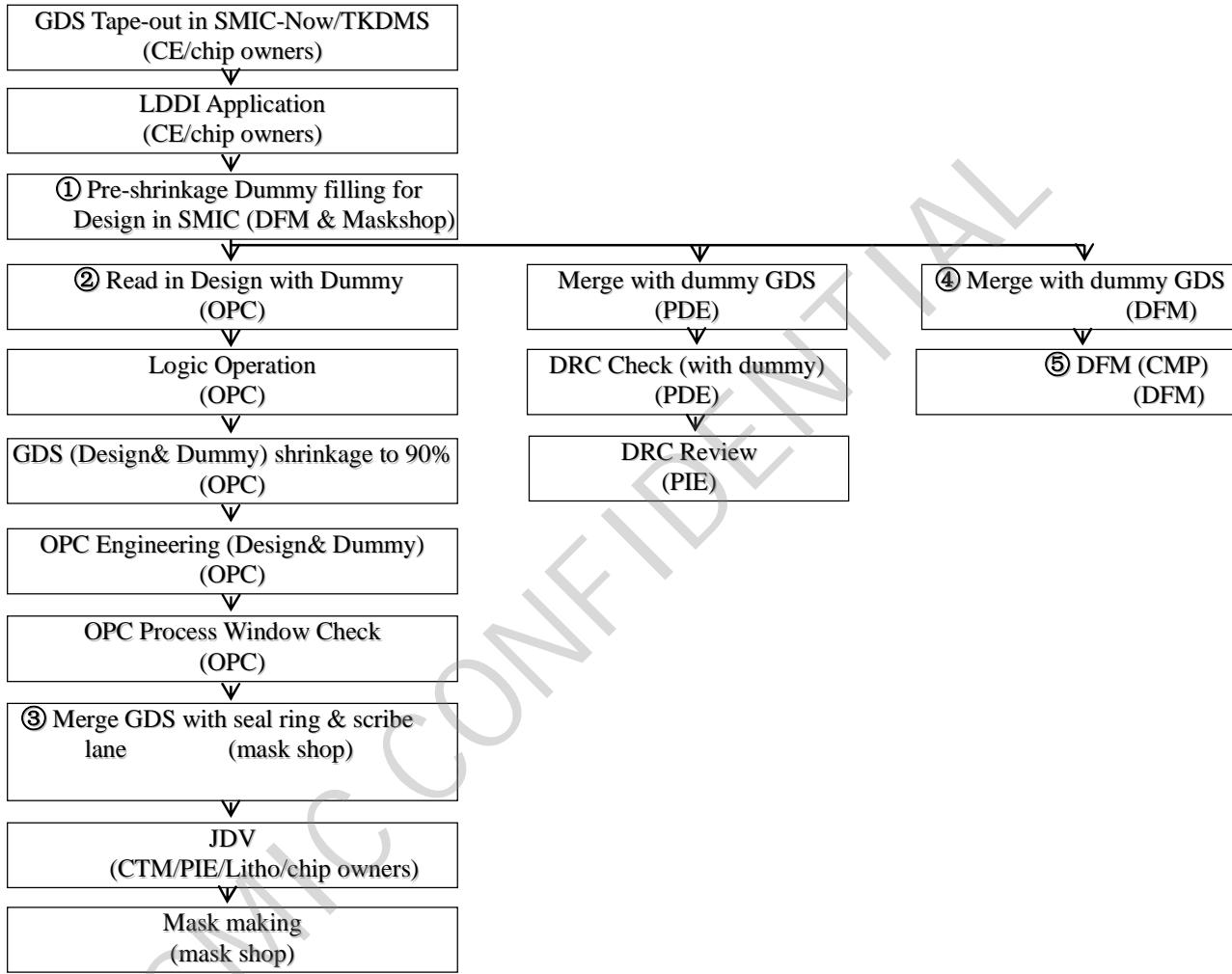
Notes:

1. Designer must clean DRC and DFM litho killer errors before tape-out. Non-cleans can not be waived unless SMIC does so after reviews.
2. Recommend designers to add seal ring (Step①) before DRC and DFM check following SMIC 32nm seal ring GDS sample.
3. Recommend designers to do dummy insertions (Step②) before DRC and DFM check. Without dummy inserted, design verification, CMP DFM, and DRC results related to dummy patterns will not be accurate.
4. Recommend designers to do the steps of ③, ④ and ⑤ by themselves. SMIC can help to do the work before tape out if designers have concerns or difficulties.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 49/306
---------------------------	---	------------	----------------------	------------------

7.1.14.2 Post-Tape out Working Flow



Notes:

1. If designers have inserted dummies and do not request SMIC to add dummy. Dummy patterns will be treated as design patterns. Steps of ① related with dummy will be skipped.
2. If designers revised GDS layout (mask re-tooling) for the layers which need dummy insertion, in the step ①, all layers' dummies of this GDS should be generated again by DFM team, and then DFM team will pass the new version dummy file to relative departments.
3. If designers have added seal ring before tape out, seal ring merge in the step of ③ will be skipped. The seal ring GDS in step ③ is post shrinkage design (28nm).
4. DRC violations and DFM litho killer errors must be clean before tape-out. Designers must pass the results to SMIC.
5. If designers have added dummy filling and performed DFM CMP simulation before tape-out, step ④ and ⑤ can be skipped.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	Tech Dev Rev: 1.10.1	Page No.: 50/306
TD-LO28-DR-2006			2		

7.1.15 DRC Connectivity Definition

1. Poly connectivity:
 - Interconnect non-resistor silicided poly, dummy poly is excluded
 - Interconnect poly = ((poly NOT P2) NOT SAB)
2. NW and DNW connectivity:
 - NW interact with DNW
3. Pickup connectivity:
 - N+ pickup interact with NW; P+ pickup interact with (NOT (NW OR PSUB)).
 - N+ pickup butted P+ silicided source/drain; P+ pickup butted N+ silicided source/drain.
4. BEOL connectivity:
 - Silicided source/drain, interconnect poly, pickup connected with M1 by CT.
 - BEOL metal, via are defined as conducting layers by default, metal dummy is excluded.
 - Metal resistors and inductors are treated as conducting metal.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 51/306
---------------------------	---	------------	----------------------	------------------

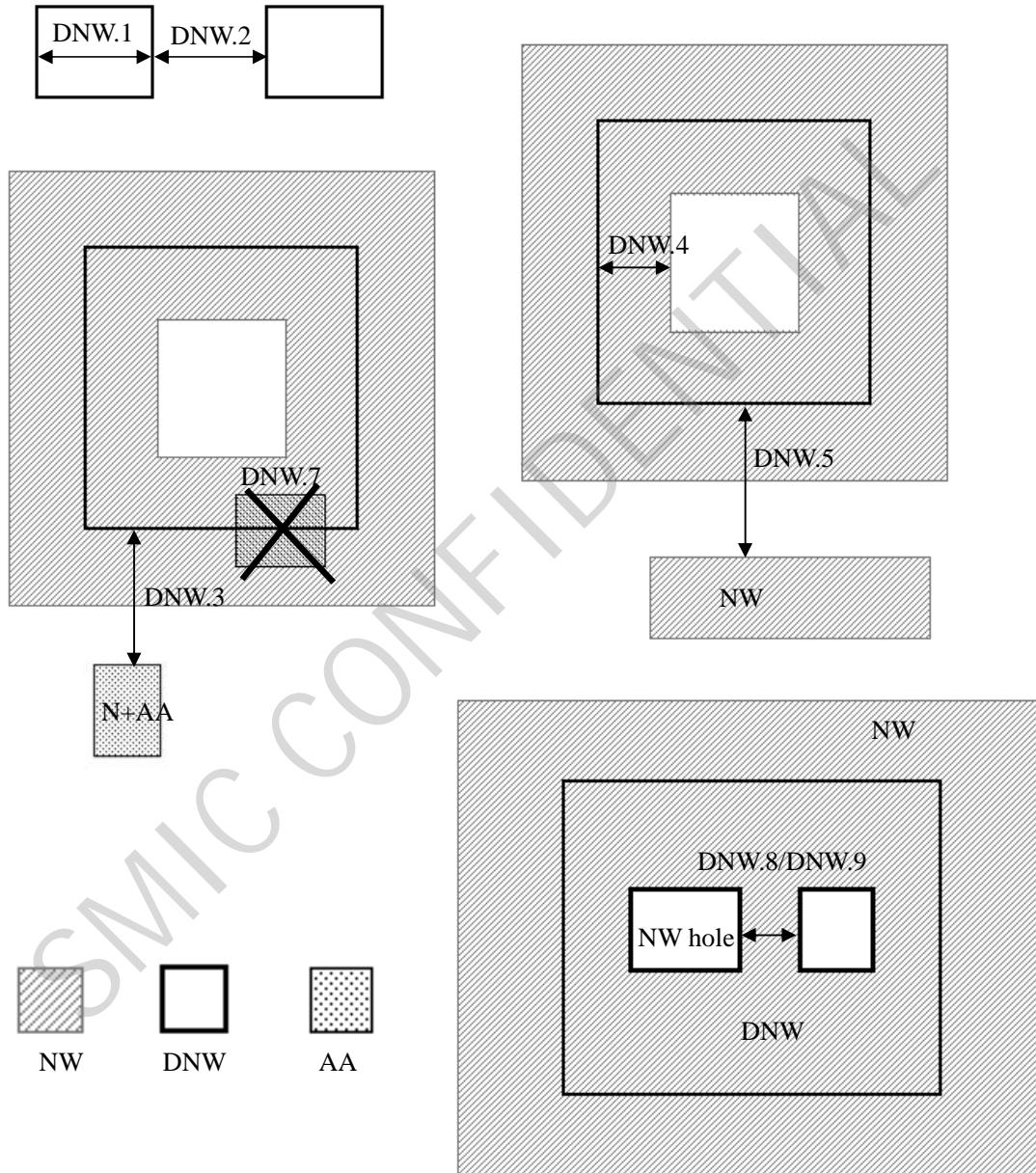
7.2 Layout Rule Description

7.2.1 DNW: Deep N-Well design rules

Rule number	Description	Operation	Design Value	Unit
DNW.1	DNW width	\geq	3	um
DNW.2	Space between DNWs	\geq	3.5	um
DNW.3	Space between DNW and N+AA (N+AA outside of DNW or NW)	\geq	1.65	um
DNW.4	Overlap of NW and DNW	\geq	0.4	um
DNW.5	Space between DNW and NW at different nets	\geq	2.5	um
DNW.6	N+AA enclosure by DNW	\geq	0.465	um
DNW.7	It is not allowed that N+AA CUT DNW			
DNW.8	Space between ((NW hole INSIDE DNW) NOT INTERACT (DG OR TG)) and ((NW hole INSIDE DNW) NOT INTERACT (DG OR TG)) or (PW NOT DNW) at different nets.	\geq	0.8	um
DNW.9	Space between ((NW hole INSIDE DNW) INTERACT (DG OR TG)) and (NW hole INSIDE DNW) or (PW NOT DNW) at different nets.	\geq	1	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev. 2	Tech Dev Rev: 1.10.1	Page No.: 52/306
TD-LO28-DR-2006					



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 53/306
---------------------------	---	------------	----------------------	------------------

7.2.2 AA: Active Area design rules

Rule number	Description	Operation	Design Value	Unit
AA.1	AA width DRC doesn't check INST region.	\geq	0.05	um
AA.1a ^[R]	Recommended AA width. DRC doesn't check INST region.	\geq	0.06	um
AA.1b ^[R]	Recommended AA width.	\leq	30	um
AA.2a	Channel width for core NMOS/PMOS transistors.	\geq	0.1	um
	This rule isn't applicable for PSUB, VARMOS, ESDIO1, ESDIO2,ESDCLP,ESDPOB,CLPDMY,INST region, and AA without CT.	\leq	3	um
AA.2b	Channel width for I/O NMOS/PMOS transistors. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region, and AA without CT.	\geq	0.27	um
AA.3	Width of 45-degree AA.	\geq	0.45	um
AA.4a	Space between two AAs. DRC doesn't check IND MY, INST region.	\geq	0.07	um
AA.4a ^[R]	Recommended space between two AAs to prevent AA bridge. DRC doesn't check IND MY, INST region.	\geq	0.075	um
AA.4b	Space between two AAs inside DG/TG. DRC doesn't check LDBK region.	\geq	0.15	um
AA.4c	Space between two AAs when one or both AA widths are >0.09um, and parallel run length of two AAs is >0. DRC doesn't check IND MY, INST region.	\geq	0.08	um
AA.4d	At least one side space between (AA or AA_DMY), when 1.Width of (AA or AA_DMY) W1 = 0.05um, the width is measured in parallel to space direction; 2.Width of two neighboring (AA or AA_DMY) W2 > 0.09um, the width is measured in parallel to space direction; 3. The parallel run length of (AA or AA_DMY) and W1 and W2 > 0um.	\geq	0.09	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 54/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
AA.4e	Space between two (AA or AA_DMY),when 1. Width of (AA or AA_DMY) W1 >0.09um; 2. Width of (AA or AA_DMY) W2 >0.05um and <0.07um; 3. The parallel run length > 0.3um.	\geq	0.1	um
AA.4f	Space between two (AA or AA_DMY),when 1. Width of (AA or AA_DMY) W1 >0.09um; 2. Width of (AA or AA_DMY) W2 <0.09um ,and \geq 0.07um; 3. The parallel run length > 0.3um. DRC doesn't check INST region.	\geq	0.09	um
AA.5	Space between 45-degree AA and AA DRC doesn't check INDMY region.	\geq	0.45	um
AA.6	Space between U-shape (or O-shape) AA inner edges.	\geq	0.13	um
AA.7	Space between U-shape (or O-shape) AA inner edges when the U-shape (or O-shape) AA interact with poly.	\geq	0.21	um
AA.9 ^[R]	Space between (AA or AA_DMY) DRC check maximum STI width. DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	\leq	10	um
AA.10	Space between AA and (AA INTERACT poly) along channel width direction, when channel width < 0.15um, AA area < 0.0465um ² , and the parallel runlength between AA and channel >0um. DRC doesn't check INST region.	\geq	0.09	um
AA.11	(Purposely blank)			
AA.12	(Purposely blank)			
AA.13	NW enclosure of N+ pickup AA. DRC doesn't check resistor NW region, LDBK and INST region.	\geq	0.065	um
AA.14	Space between NW and N+AA. DRC doesn't check resistor NW region, LDBK and INST region.	\geq	0.065	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 55/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
AA.15	Space between N+AA corner edge and NW corner edge. DRC follows below conditions to check: 1. The edge of E1 \leq 0.105um, the edge of E2 \leq 0.065um. 2. DRC only flags the opposite space between E1 and E2. 3. DRC flags the space between concave corner and convex corner. DRC doesn't check resistor NW region, INST and LDBK region.	\geq	0.105	um
AA.16	Space between NW and (N+AA INTERCACT (DG or TG)) DRC doesn't check resistor NW region and LDBK region.	\geq	0.18	um
AA.17	NW enclosure of P+AA. DRC doesn't check LDBK and INST region.	\geq	0.065	um
AA.18	NW corner edge enclosure of P+AA corner edge. DRC follows below conditions to check: 1. The edge of E1 \leq 0.105um, the edge of E2 \leq 0.065um 2. DRC only flag the opposite space between E1 and E2. 3. DRC flag the enclosure between concave corner and concave corner; or the enclosure between convex corner and convex corner. DRC doesn't check LDBK region.	\geq	0.105	um
AA.19	NW enclosure of (P+AA INTERACT (DG OR TG)). DRC doesn't check LDBK region.	\geq	0.18	um
AA.20	Space between NW and P+ pickup AA. DRC doesn't check LDBK and INST region.	\geq	0.065	um
AA.21a	(AA and AA_DMY) density. Density check window size: 50um*50um, step size: 25um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\geq	15%	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 56/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
AA.21b	(AA and AA_DMY) density. Density check window size: 150um*150um, step size: 75um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\geq	20%	
AA.21b ^[R]	(AA and AA_DMY) density. Density check window size: 20um*20um, step size: 10um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\geq	20%	
AA.21c	(AA and AA_DMY) density for non-IO region. Density check window size: 150um*150um, step size: 75um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\leq	80%	
AA.21d	(AA and AA_DMY) for IO region. Density check window size: 150um*150um, step size: 75um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\leq	90%	
AA.21e	(AA or AA_DMY) density in full chip	\geq	25%	
		\leq	75%	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 57/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
AA.21f ^[R]	(AA or AA_DMY) density inside of the dummy block area(DUMBA), Density check window size: 20um*20um, step size: 10um DRC need check the design if DUMBA width is >5um and <20um, where density ratio= AA area/DUMBA area.	\geq	20%	
AA.22	AA area. DRC doesn't check INST region.	\geq	0.018	um ²
AA.23a	AA area when AA any edge length<0.1um. DRC doesn't check INST region.	\geq	0.03	um ²
AA.23b	AA area when AA all of edge length <0.13um DRC doesn't check INST region and , and doesn't check the AA pattern which can fill 0.1um * 0.3um rectangular pattern	\geq	0.04	um ²
AA.24	AA enclosed area.	\geq	0.0288	um ²
AA.25	AA enclosed area when AA any of inner edge length <0.13um	\geq	0.04	um ²
AA.26	Area sum of ((AA AND SP) INTERACT poly) NOT ((poly or GTDMP) or GTDOP)) in the same AA for core PMOS device.	\leq	280	um
AA.27a	AA length between two CTs when AA width <0.1um. This rule doesn't check the region of (MOMDMY sizing up 0.9um).	\leq	18	um
AA.27b	AA length between one CT and this AA line-end when AA width <0.1um. AA line-end definition: AA edge <0.1um, and the AA edge is between two consecutive 90degree outer vertex. This rule doesn't check the region of (MOMDMY sizing up 0.9um).	\leq	18	um
AA.28	L-shape AA edge length (L1) (AA INTERACT poly) when L-shape AA width (W1) <0.18um in source/drain direction. L-shape AA edge definition: the edge is between consecutive 90degree outer vertex and 270 degree inner vertex.	\leq	0.275	um
AA.29	(Purposely blank)			
AA.30	45-degree AA edge length	\geq	0.45	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

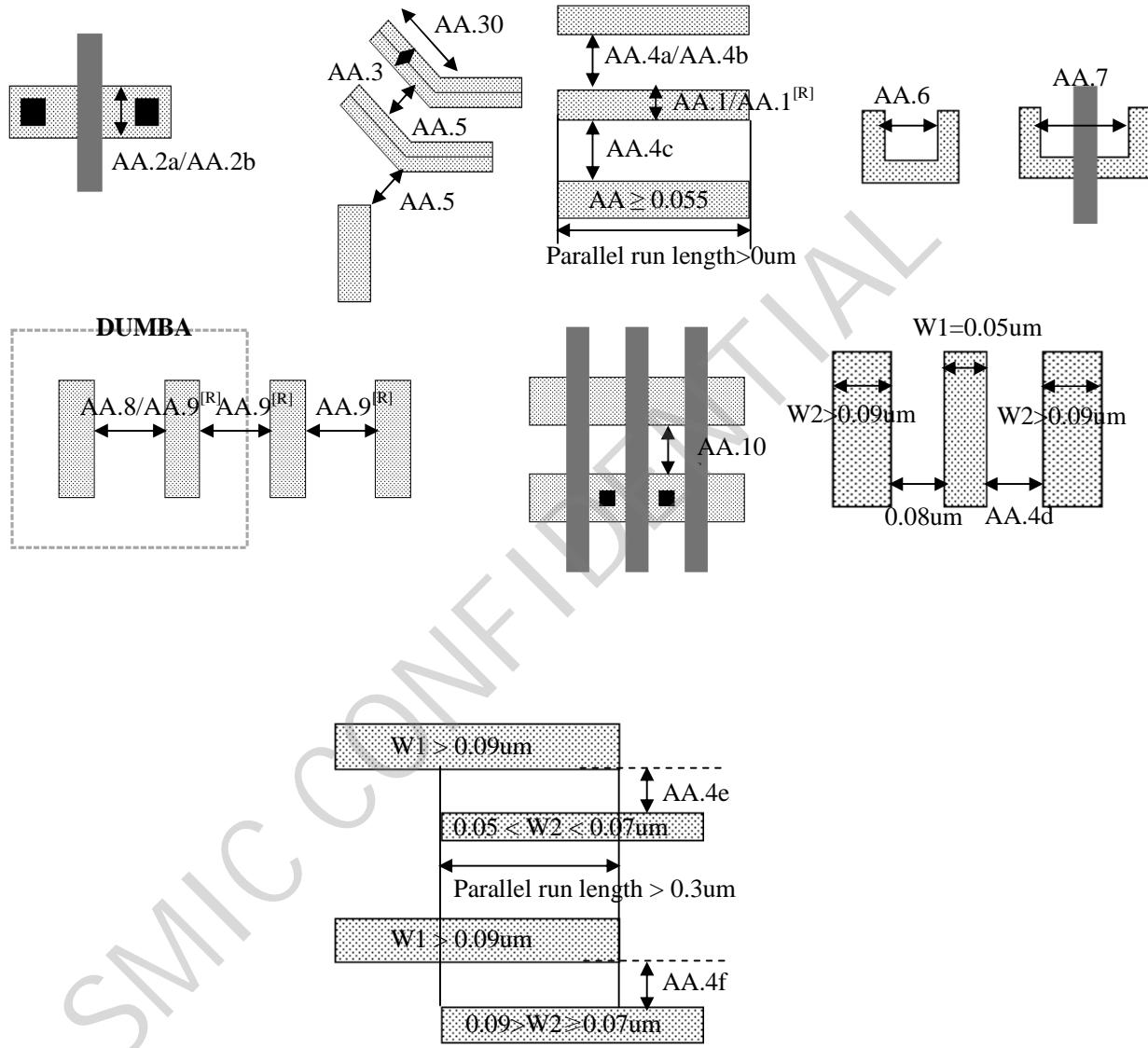


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 58/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
AA.31	Any edge length of (AA INTERACT poly) with another adjacent edge length <0.13um. DRC doesn't check INST region.	\geq	0.13	um
AA.32	(Purposely blank)			
AA.33	(Purposely blank)			
AA.34	AA must be fully covered by (SP or SN). DRC doesn't check AA_DMY , LOGO, OCCD, OCOVL and RESNW related region			
AA.35	(AA INTERACT poly) must be rectangular, single L-, T-, or U-shape and the GATE direction must be perpendicular to the edge E) of this T- or U-shape design. (45-degree edge is not allowed) DRC doesn't check INDMY, INST region and LOGO.			

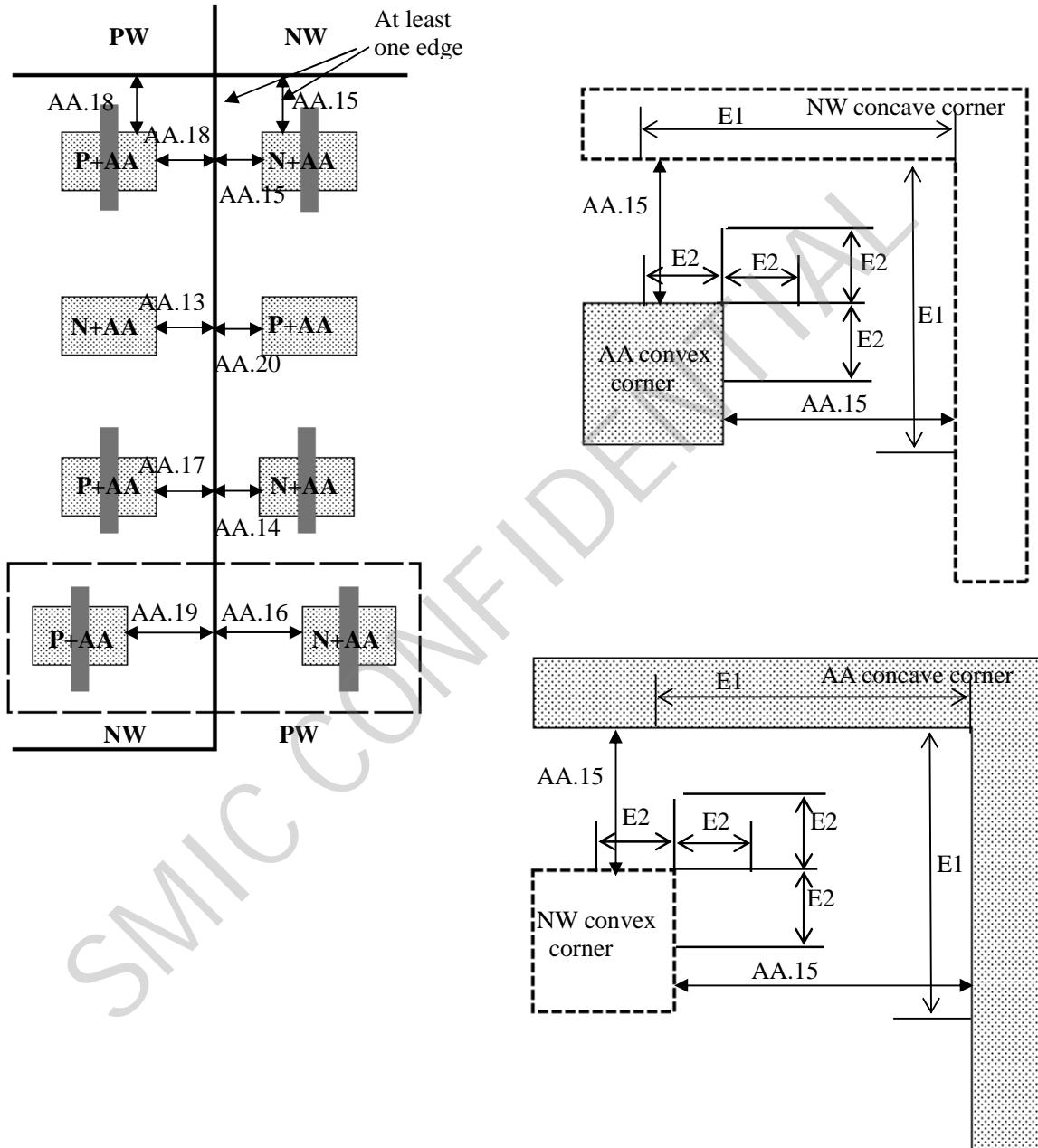
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 59/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

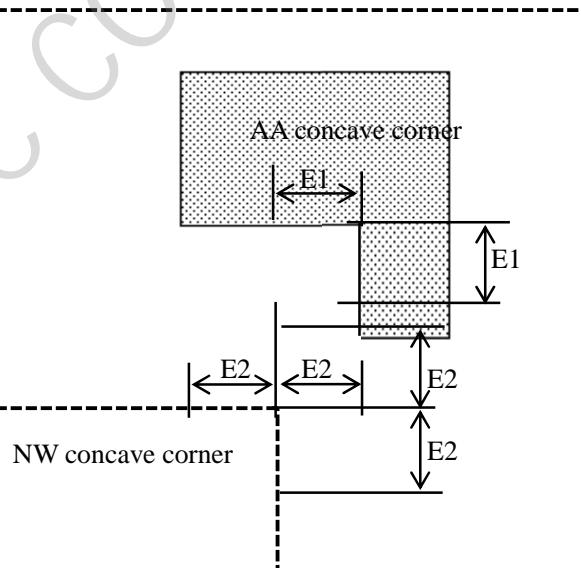
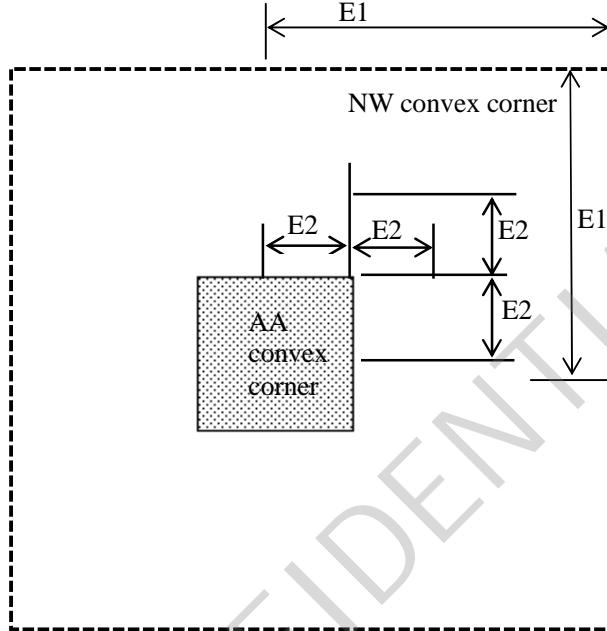
Doc. No.:	TD-LO28-DR-2006	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	2	Tech Dev Rev:	1.10.1	Page No.:	60/306
-----------	-----------------	-------------	--	----------	---	---------------	--------	-----------	--------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

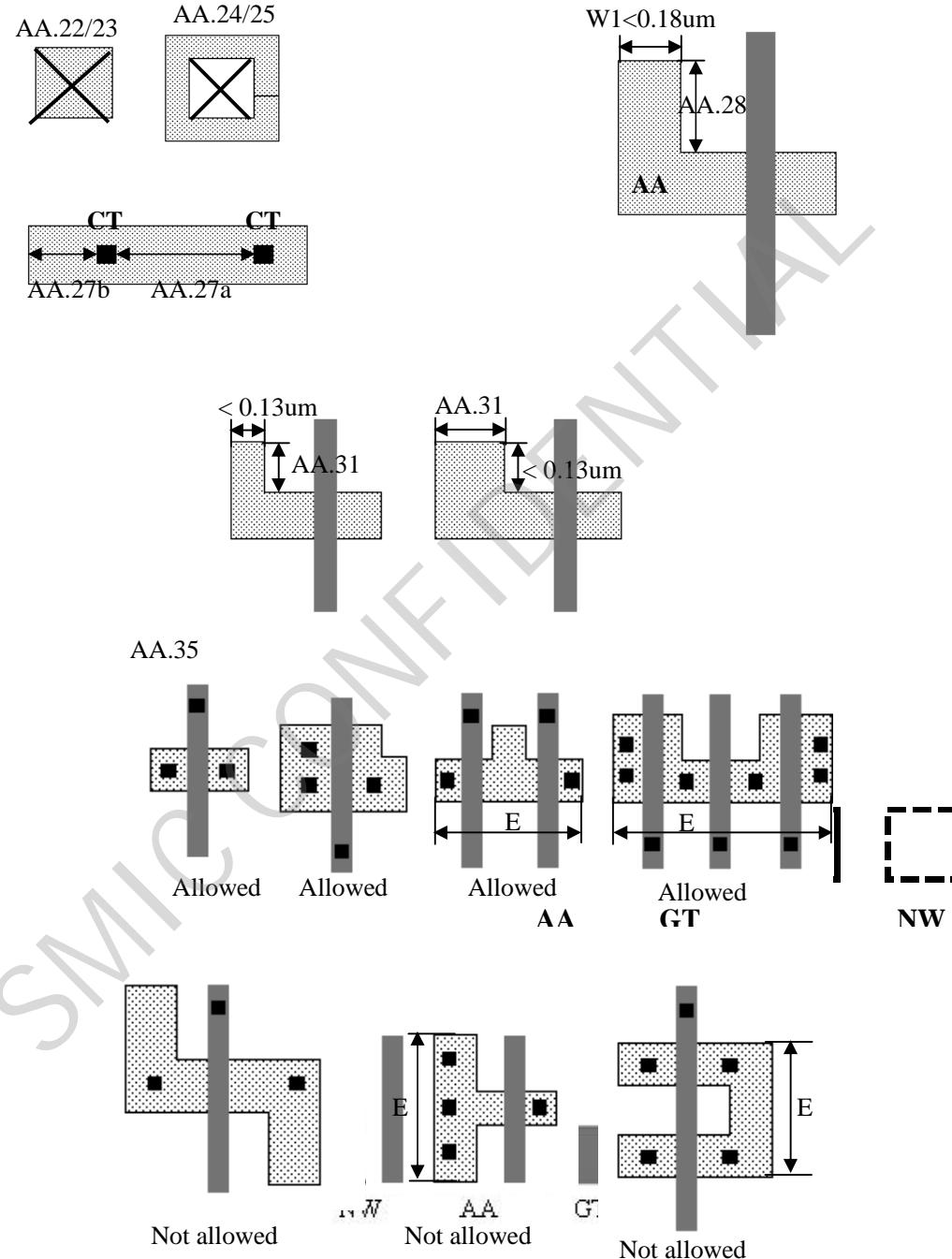
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 61/306
---------------------------	---	------------	----------------------	------------------

AA.18



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev. 2	Tech Dev Rev: 1.10.1	Page No.: 62/306
TD-LO28-DR-2006					



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 63/306
---------------------------	---	------------	----------------------	------------------

7.2.3 AADMP: AA dummy design rules

Rule number	Description	Operation	Design Value	Unit
AADMP.1	AADMP width	\geq	0.05	um
	DRC doesn't check MOMDMY region for maximum width check.	\leq	0.5	um
AADMP.2	AADMP width inside DG/TG	\geq	0.1	um
AADMP.3	Space between AADMP and (AA or AA_DMY). (AADMP and AA overlap is not allowed)	\geq	0.08	um
AADMP.4	Space between AADMP and (AA or AA_DMY) inside DG/TG. (overlap is not allowed)	\geq	0.15	um
AADMP.5	Space between AADMP and 45-degree AA	\geq	0.45	um
AADMP.6	Space between AADMP and (poly OR GTDOP OR GTDMP) (It's not allowed AADMP overlap with ((poly OR GTDUM) OR GTDOP))	\geq	0.025	um
AADMP.7	Space between AADMP and NW	\geq	0.08	um
AADMP.8	Space between AADMP and RESNW (overlap is not allowed)	\geq	0.7	um
AADMP.9	Space between AADMP and INDMY	\geq	1.2	um
AADMP.10	Space between AADMP and PSUB (overlap is not allowed if AA inside PSUB) DRC doesn't check MOMDMY region.	\geq	0.14	um
AADMP.11	Space between AADMP and DG/TG. It's not allowed AADMP CUT DG/TG.	\geq	0.08	um
AADMP.12	Space between AADMP and SP It's not allowed AADMP CUT SP.	\geq	0.065	um
AADMP.13	NW enclosure of AADMP	\geq	0.08	um
AADMP.14	DG/TG enclosure of AADMP	\geq	0.08	um
AADMP.15	SP enclosure of AADMP	\geq	0.065	um
AADMP.16	AADMP area	\geq	0.03	um ²

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

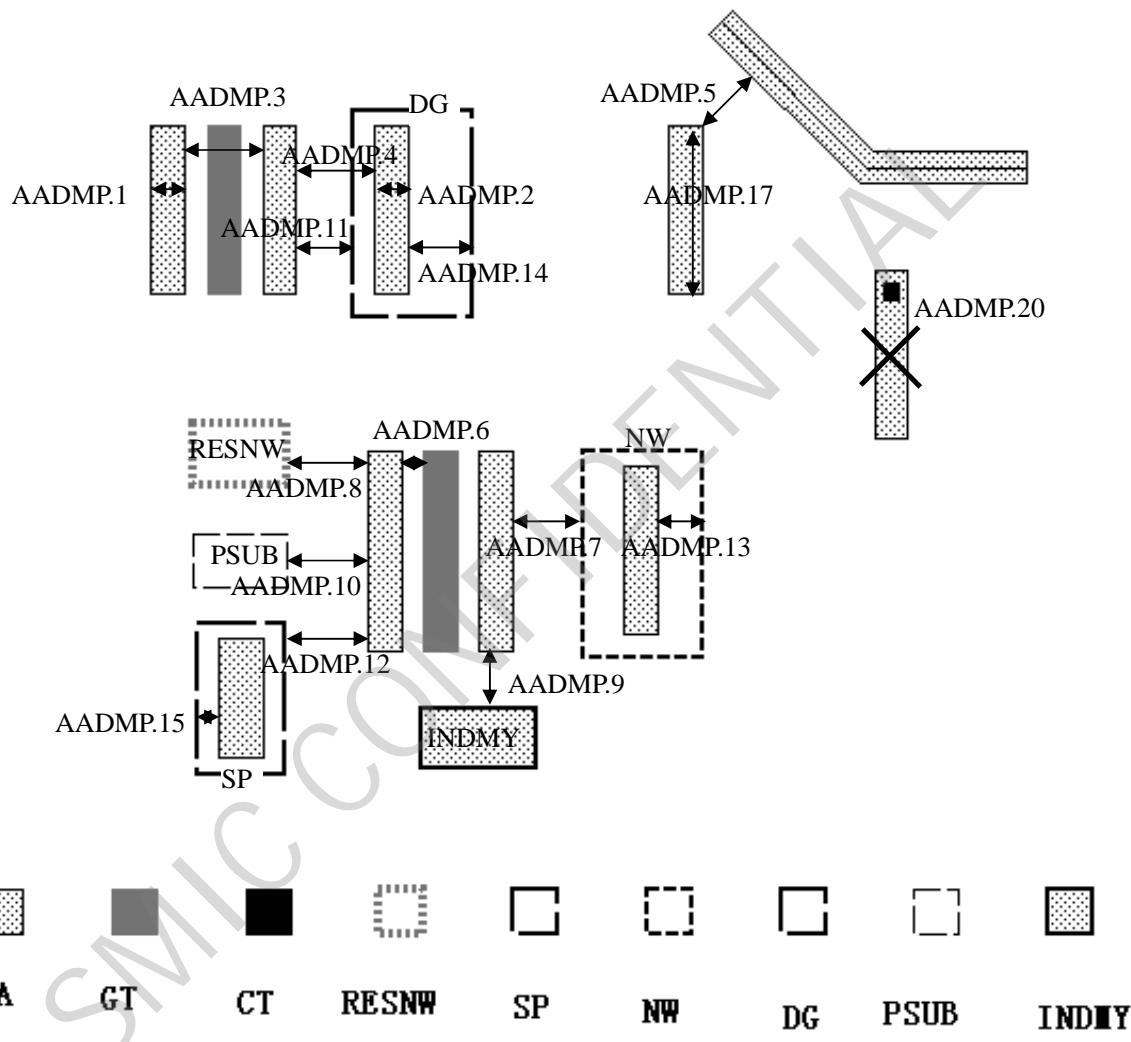


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 64/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
AADMP.17	AADMP length DRC doesn't check RESP1, RESAA and MOMDMY regions for the maximum length check.	\geq	0.6	um
		\leq	16	um
AADMP.18^[R]	(AA OR AA_DMY) density. DRC check window follow: ((AA OR poly) INTERACT GATE) sizing up 2um) NOT ((AA OR poly) sizing up 0.15um)) This rule doesn't check DG, TG, VARMOS, NODMF, INST, OCOVL and OCCD regions.	\geq	10%	
AADMP.19	It's not allowed 45-degree AADMP.			
AADMP.20	CT is not allowed to INTERACT with AADMP			
AADMP.21	AADMP must be rectangular.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	TD-LO28-DR-2006	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	2	Tech Dev Rev:	1.10.1	Page No.: 65/306
-----------	-----------------	-------------	--	----------	---	---------------	--------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



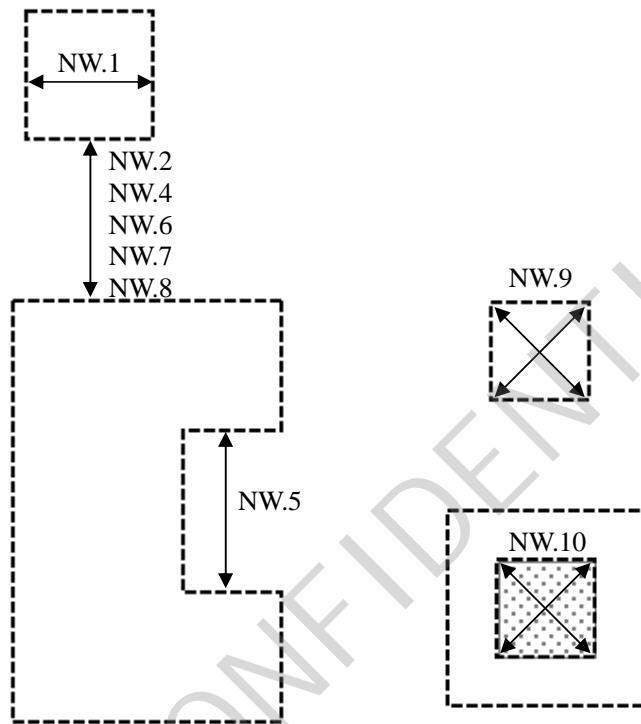
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 66/306
---------------------------	---	------------	----------------------	------------------

7.2.4 NW: N-Well design rules

Rule number	Description	Operation	Design Value	Unit
NW.1	NW width. DRC doesn't check INST region.	\geq	0.24	um
NW.2	NW space	\geq	0.24	um
NW.3 ^[R]	Space between NWs if at least one NW width<0.28um DRC doesn't check INST region.	\geq	0.28	um
NW.4	Space between NWs with parallel run length >0.5um, which NWs space is on STI (NOT INTERACT AA or AA_DMY)	\geq	0.3	um
NW.5	Space between NWs at same net	\geq	0.24	um
NW.6	Space between 1.05V NWs at different net. DRC doesn't check OCCD region.	\geq	0.8	um
NW.7	Space between 1.05V NW and 1.8V/2.5V NW at different net	\geq	1	um
NW.8	Space between 1.8V//2.5V NWs at different net	\geq	1	um
NW.9	NW area (um ²)	\geq	0.4	um ²
NW.10	NW enclosed area (um ²)	\geq	0.4	um ²
NW.11	Area of (NW NOT DG), (DG AND NW), (NW NOT TG), (TG AND NW)	\geq	0.35	um ²
NW.12	Enclosed area of (NW NOT DG), (DG AND NW), (NW NOT TG), (TG AND NW)	\geq	0.35	um ²

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 67/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 68/306
---------------------------	---	------------	----------------------	------------------

7.2.5 PSUB: Native device design rules

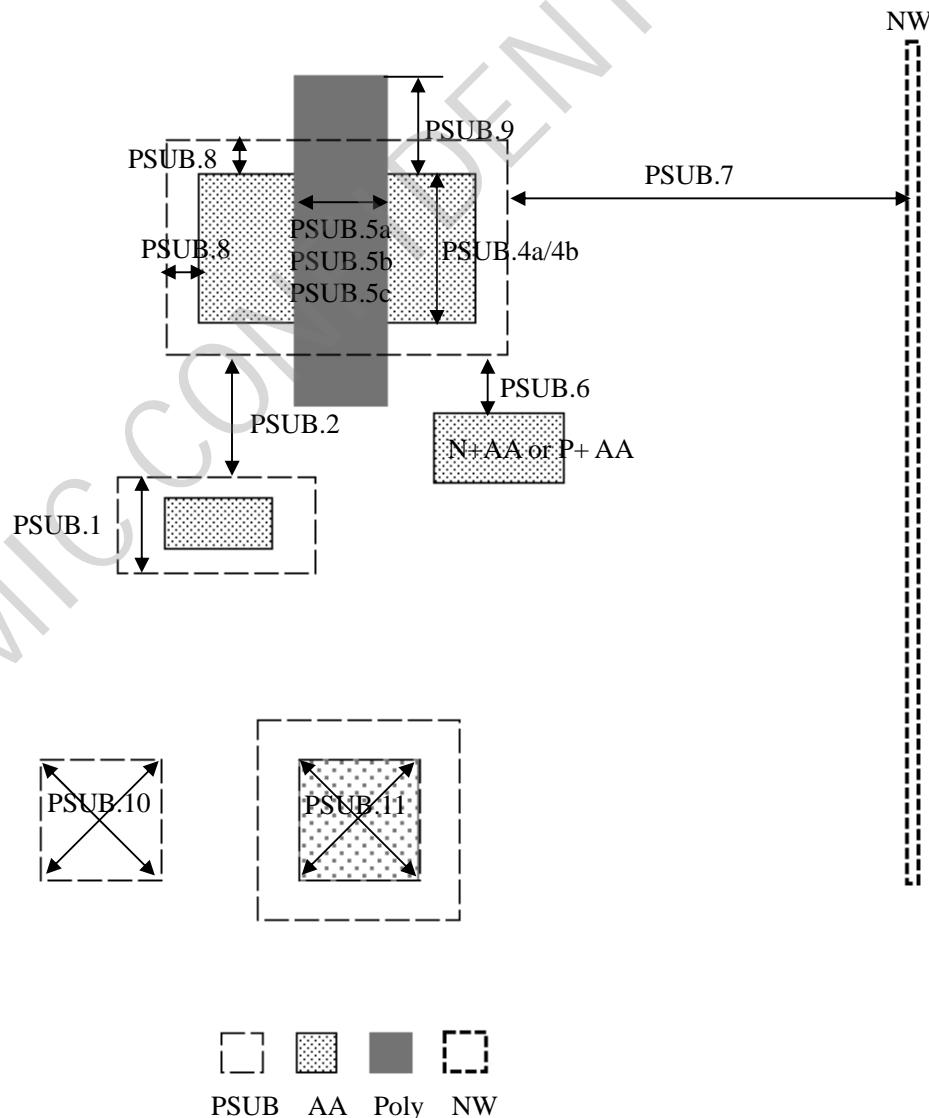
PSUB is to define the area for a native NMOS device on a P-substrate

Rule number	Description	Operation	Design Value	Unit
PSUB.1	PSUB width	\geq	0.24	um
PSUB.2	PSUB space	\geq	0.24	um
PSUB.3^[R]	Space of PSUBs if at least one PSUB width<0.28um	\geq	0.28	um
PSUB.4a	Channel width for core zero/native Vt NMOS DRC doesn't check IND MY region	\geq	0.5	um
		\leq	10	um
PSUB.4b	Channel width for IO native NMOS	\geq	0.5	um
PSUB.5a	Channel length for core zero Vt NMOS	\geq	0.2	um
		\leq	6	um
PSUB.5b	Channel length for core native Vt NMOS	\geq	0.3	um
		\leq	6	um
PSUB.5c	Channel length for 1.8V IO NMOS	\geq	0.8	um
		\leq	6	um
PSUB.5d	Channel length for 2.5V IO NMOS	\geq	1.2	um
		\leq	6	um
PSUB.6	Space between PSUB and N+AA or P+AA	\geq	0.38	um
PSUB.7	Space between PSUB and NW.	\geq	0.8	um
PSUB.8	MOS AA enclosure by PSUB. DRC doesn't check IND MY region.	=	0.16	um
PSUB.9	((Poly extension outside of AA) NOT OUTSIDE PSUB) along poly length direction DRC doesn't check IND MY region.	\geq	0.24	um
PSUB.10	PSUB area.	\geq	0.4	um ²
PSUB.11	PSUB enclosed area.	\geq	0.4	um ²
PSUB.12	PSUB must not overlap NW or DNW.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 69/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
PSUB.13	One AA shape per PSUB shape, except for NMOS capacitors, pickup region.			
PSUB.14	It's not allowed P+ GATE in PSUB. DRC doesn't check INDMDY region.			
PSUB.15	It's not allowed ZVT and TG on the same chip			



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 70/306
---------------------------	---	------------	----------------------	------------------

7.2.6 Low Vt design rules

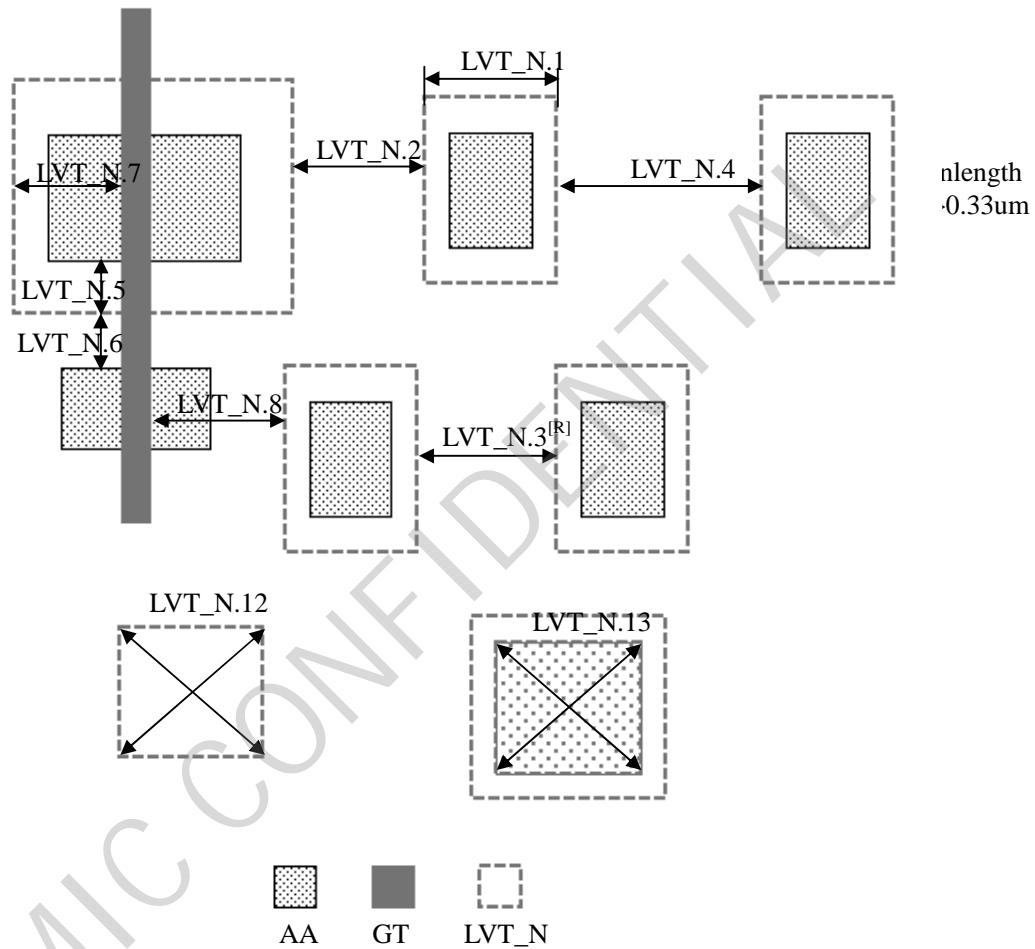
7.2.6.1 LVT_N : Low Vt NMOS design rules

A drawn LVT_N(159;158) layer is needed to define low Vt NMOS devices. LVT_N is for 1.05V N core low Vt devices only.

Rule number	Description	Operation	Design Value	Unit
LVT_N.1	LVT_N width. Single-point-interaction is allowed. DRC doesn't highlight the violation when LVT_N opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
LVT_N.2	Space between LVT_Ns. DRC doesn't highlight the violation when LVT_N opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
LVT_N.3 ^[R]	Space between LVT_Ns with parallel run length $>0.24\text{um}$, when one LVT_N width $>0.22\text{um}$.	\geq	0.18	um
LVT_N.4	Space between LVT_Ns with parallel run length $>0.33\text{um}$, and LVT_N space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
LVT_N.5	LVT_N extension outside of GATE along GATE poly direction.	\geq	0.065	um
LVT_N.6	Space between LVT_N and GATE along GATE poly direction.	\geq	0.065	um
LVT_N.7	LVT_N extension outside of GATE along source/drain direction.	\geq	0.115	um
LVT_N.8	Space between LVT_N and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT LVT_N) is not allowed.	\geq	0.115	um
LVT_N.9	Space between LVT_N and non-silicided AA/poly resistor	\geq	0.15	um
LVT_N.10	45-degree edge length	\geq	0.52	um
LVT_N.11	LVT_N overlap P+ AA, LVT_P, PSUB, DG, TG, RESAA, RESNW, RESP1, VARMOS, BIPOLA, LOGO is prohibited.			
LVT_N.12	LVT_N area.	\geq	0.1	um^2
LVT_N.13	LVT_N enclosed area	\geq	0.1	um^2

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 71/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 72/306
---------------------------	---	------------	----------------------	------------------

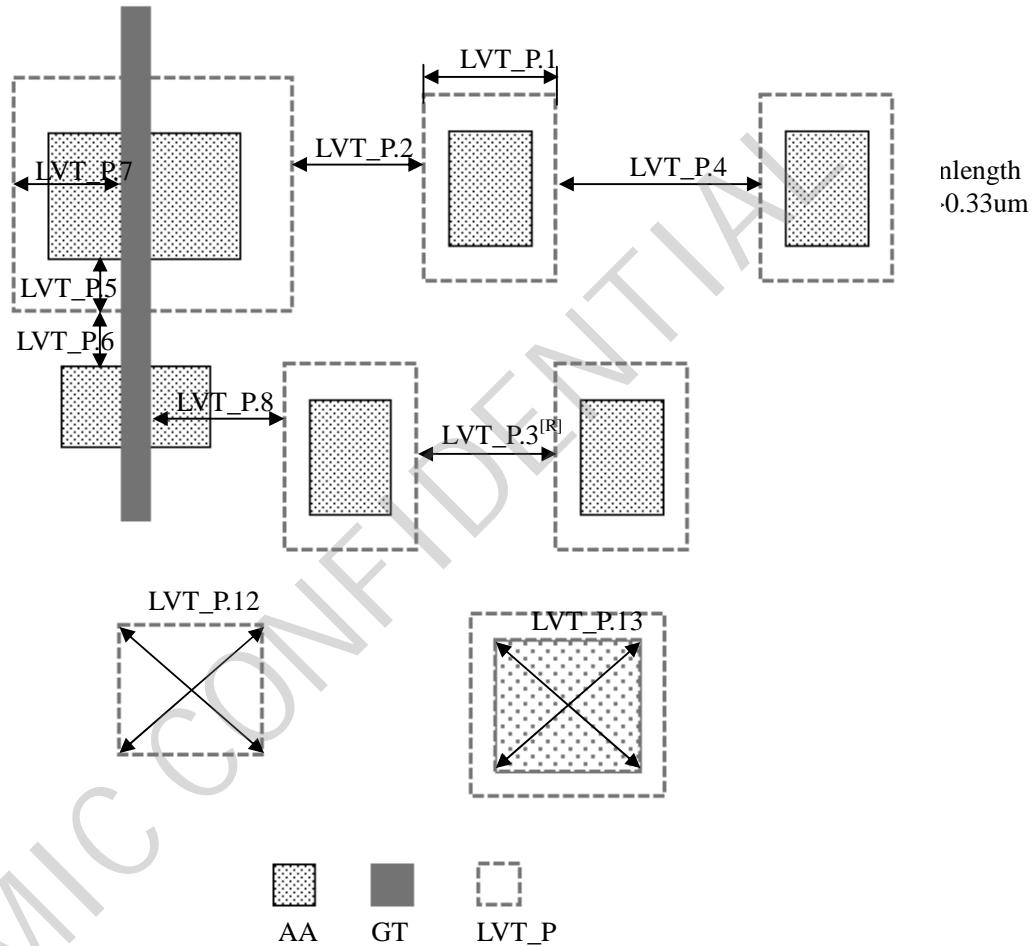
7.2.6.2 LVT_P : Low Vt PMOS design rules

A drawn LVT_P(159;168) layer is needed to define low Vt PMOS devices. LVT_P is for 1.05V P core low Vt devices only.

Rule number	Description	Operation	Design Value	Unit
LVT_P.1	LVT_P width. Single-point-interaction is allowed. DRC doesn't highlight the violation when LVT_P opposite side width $\geq 0.135\mu m$, and $< 0.16\mu m$.	\geq	0.16	um
LVT_P.2	Space between LVT_Ps. DRC doesn't highlight the violation when LVT_P opposite side width $\geq 0.135\mu m$, and $< 0.16\mu m$.	\geq	0.16	um
LVT_P.3 ^[R]	Space between LVT_Ps with parallel run length $> 0.24\mu m$, when one LVT_P width $> 0.22\mu m$.	\geq	0.18	um
LVT_P.4	Space between LVT_Ps with parallel run length $> 0.33\mu m$, and LVT_P space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
LVT_P.5	LVT_P extension outside of GATE along GATE poly direction.	\geq	0.065	um
LVT_P.6	Space between LVT_P and GATE along GATE poly direction.	\geq	0.065	um
LVT_P.7	LVT_P extension outside of GATE along source/drain direction.	\geq	0.115	um
LVT_P.8	Space between LVT_P and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT LVT_P) is not allowed.	\geq	0.115	um
LVT_P.9	Space between LVT_P and non-silicided AA/poly resistor	\geq	0.15	um
LVT_P.10	45-degree edge length	\geq	0.52	um
LVT_P.11	LVT_P overlap N+AA, LVP_N, PSUB, DG, TG, RESAA, RESNW, RESP1, VARMOS, BIPOLA, LOGO is prohibited.			
LVT_P.12	LVT_P area.	\geq	0.1	um ²
LVT_P.13	LVT_P enclosed area	\geq	0.1	um ²

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 73/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



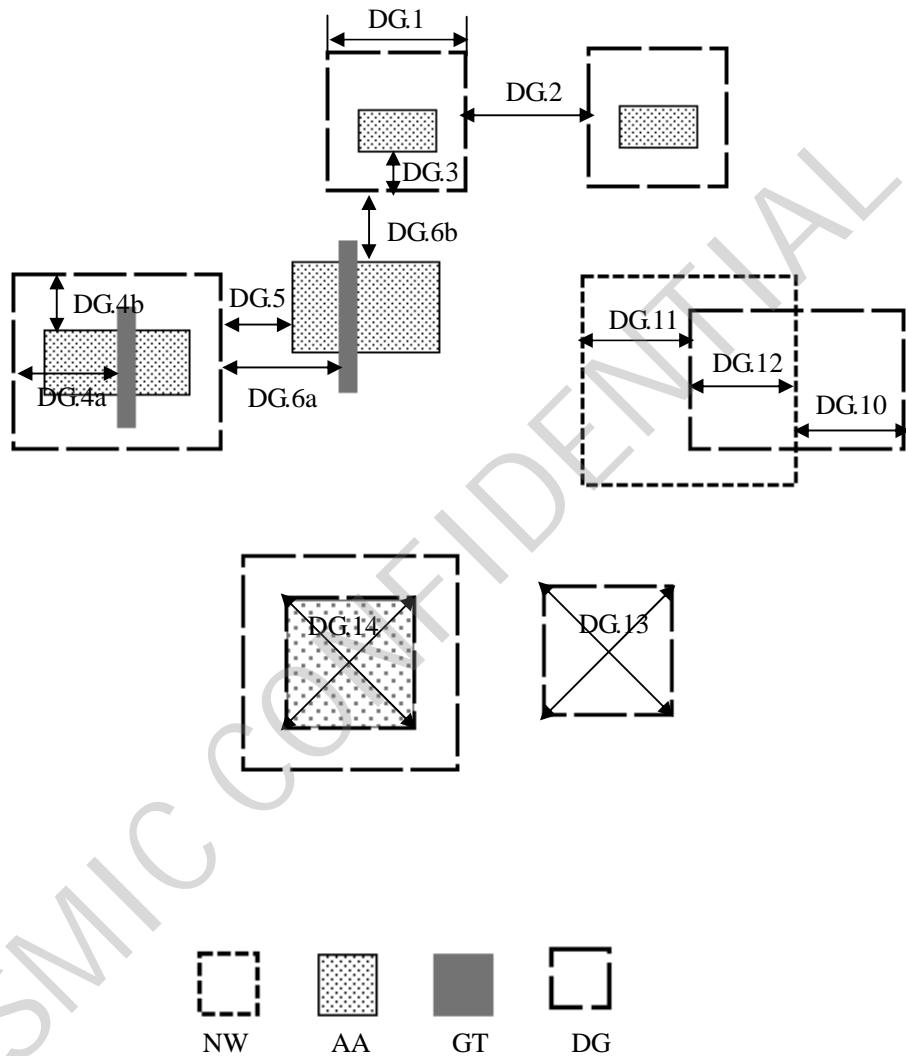
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 74/306
---------------------------	---	------------	----------------------	------------------

7.2.7 DG: Dual GATE design rules to define 1.8V device

Rule number	Description	Operation	Design Value	Unit
DG.1	DG width	\geq	0.32	um
DG.2	Space between two DGs.	\geq	0.32	um
DG.3	DG enclosure of AA. Pick-up AAs do not need to follow this rule.	\geq	0.13	um
DG.4a	DG enclosure of GATE along S/D direction.	\geq	0.24	um
DG.4b	DG enclosure of GATE along poly length direction.	\geq	0.13	um
DG.5	Space between DG and AA (except pickup AA). It is not allowed that AA CUT DG (except pickup AA).	\geq	0.13	um
DG.6a	Space between DG and GATE along S/D direction.	\geq	0.24	um
DG.6b	Space between DG and GATE along poly direction.	\geq	0.13	um
DG.7	Space between DG and NW. Space= 0um is allowed.	\geq	0.24	um
DG.8	Space between (NW NOT DG) and (NW NOT DG)	\geq	0.24	um
DG.9	Space between (DG AND NW) and (DG AND NW)	\geq	0.24	um
DG.10	DG extension outside of NW. Extension = 0um is allowed.	\geq	0.24	um
DG.11	NW extension outside of DG. Extension = 0um is allowed.	\geq	0.24	um
DG.12	DG overlap of NW. Overlap= 0um is allowed.	\geq	0.24	um
DG.13	DG area	\geq	0.4	um ²
DG.14	DG enclosed area	\geq	0.4	um ²
DG.15	DG and TG can't be used on same chip.			
DG.16	Width of (DG OR (NW OR PSUB)). DRC doesn't check INST region.	\geq	0.24	um
DG.17	Space between (DG NOT (NW OR PSUB)) and (DG NOT (NW OR PSUB))	\geq	0.24	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 75/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



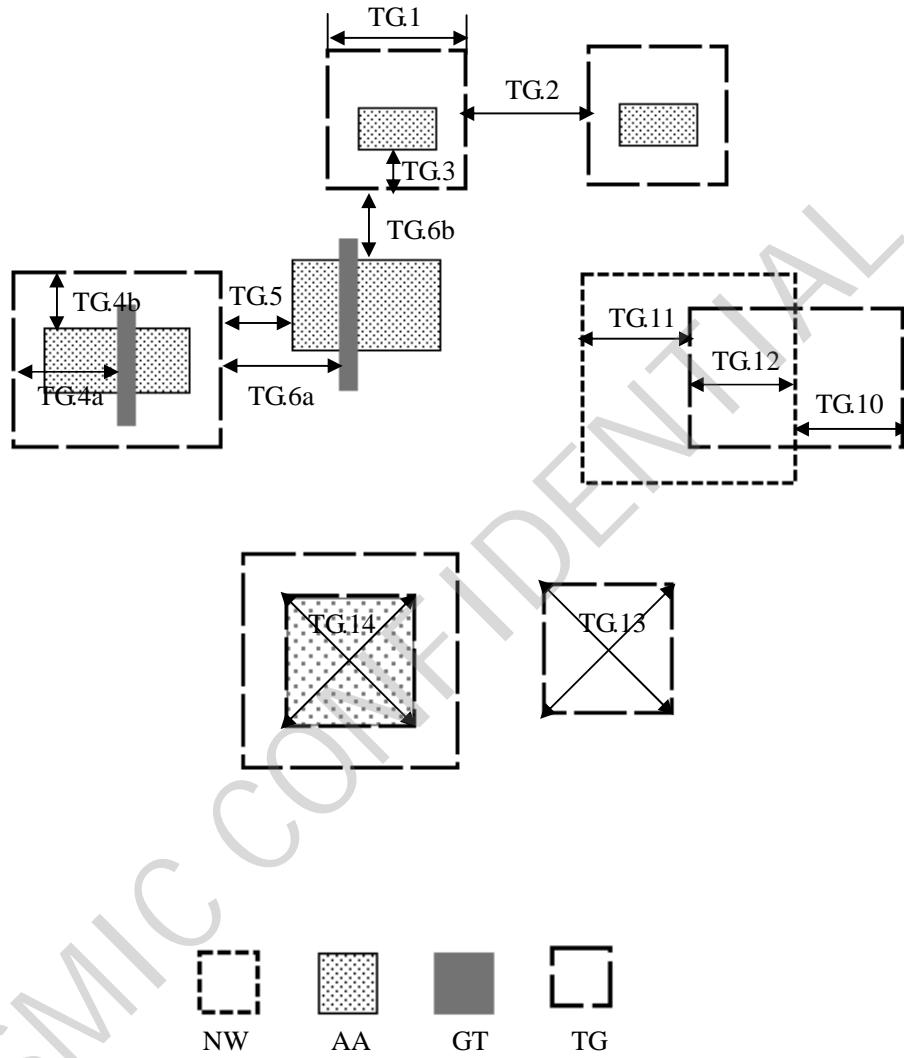
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 76/306
---------------------------	---	------------	----------------------	------------------

7.2.8 TG: Dual GATE design rules to define 2.5V IO device

Rule number	Description	Operation	Design Value	Unit
TG.1	TG width	\geq	0.32	um
TG.2	Space between two TGs.	\geq	0.32	um
TG.3	TG enclosure of AA. Pick-up AAs do not need to follow this rule.	\geq	0.13	um
TG.4a	TG enclosure of GATE along S/D direction.	\geq	0.24	um
TG.4b	TG enclosure of GATE along poly length direction.	\geq	0.13	um
TG.5	Space between TG and AA (except pickup AA). It is not allowed that AA CUT TG (except pickup AA).	\geq	0.13	um
TG.6a	Space between TG and GATE along S/D direction.	\geq	0.24	um
TG.6b	Space between TG and GATE along poly direction.	\geq	0.13	um
TG.7	Space between TG and NW. Space= 0um is allowed.	\geq	0.24	um
TG.8	Space between (NW NOT TG) and (NW NOT TG)	\geq	0.24	um
TG.9	Space between (TG AND NW) and (TG AND NW)	\geq	0.24	um
TG.10	TG extension outside of NW. Extension = 0um is allowed.	\geq	0.24	um
TG.11	NW extension outside of TG. Extension = 0um is allowed.	\geq	0.24	um
TG.12	TG overlap of NW. Overlap = 0um is allowed.	\geq	0.24	um
TG.13	TG area	\geq	0.4	um ²
TG.14	TG enclosed area	\geq	0.4	um ²
TG.15	Width of (TG OR (NW OR PSUB)). DRC doesn't check INST region.	\geq	0.24	um
TG.16	Space between (TG NOT (NW OR PSUB)) and (TG NOT (NW OR PSUB))	\geq	0.24	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 77/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 78/306
---------------------------	---	------------	----------------------	------------------

7.2.9 GT: Poly design rules

Rule number	Description	Operation	Design Value	Unit
GT.1	Width	\geq	0.03	um
GT.2	Width of horizontal poly. DRC only check opposite side.	\geq	0.04	um
GT.3	Width of horizontal poly. This rule doesn't check rectangle or L-shape poly, and poly covered by P2.	\geq	0.06	um
GT.4	Width of ((poly INTERACT CT) NOT OUTSIDE (DG OR TG)),when space between (poly INTERACT CT) and (AA INTERACT CT) <0.05um. DRC check poly width when the width is measured in parallel to space direction.	\geq	0.1	um
GT.5	Channel Length for core NMOS /PMOS transistor. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY VARMOS, PSUB, LOGO, OCOVL and INST region.	=	0.03/0.035/0.04/0.05/ 0.06/0.08/0.09-6	um
GT.6a	Channel Length for 1.8V I/O NMOS/PMOS transistor.	\geq	0.15	um
	This rule isn't applicable for DGUD, DGV, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, VARMOS region.	\leq	6	um
GT.6b	Channel Length for 1.8V I/O NMOS/PMOS transistor (for 1.5V under drive).	\geq	0.11	um
	This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\leq	6	um
GT.6c	Channel Length for 1.8V I/O NMOS/PMOS transistor (for 1.2V under drive).	\geq	0.11	um
	This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\leq	6	um
GT.7a	Channel Length for 2.5V I/O NMOS/PMOS transistor.	\geq	0.27	um
	This rule isn't applicable for TGV, ESDIO1,	\leq	6	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 79/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
	ESDIO2,ESDCLP,ESDPOB,CLPDMY,VARMOS region.			
GT.7b	Channel Length for 2.5V I/O NMOS/PMOS transistor (for 1.8V under drive).	\geq	0.25	um
	This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP,ESDPOB,CLPDMY region.	\leq	6	um
GT.7c	Channel Length for 2.5V I/O NMOS transistor (for 3.3V over drive).	\geq	0.55	um
	This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP,ESDPOB,CLPDMY region.	\leq	6	um
GT.7d	Channel Length for 2.5V I/O PMOS transistor (for 3.3V over drive).	\geq	0.44	um
	This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP,ESDPOB,CLPDMY region.	\leq	6	um
GT.8a	Width of 1st poly (or POLY_DMY) neighboring (GATE or (GTDMP AND (AA INTERACT poly))) (width = 0.03um) for core NMOS/PMOS. 1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE or (GTDMP AND (AA INTERACT poly)) <0.23um. The violation is allowed when the violation length is \leq 0.08um. This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP, ESDPOB, CLPDMY,OCCD and INST region.	=	0.03~0.04	um
GT.8b	Width of 1st poly (or POLY_DMY) neighboring (GATE or (GTDMP AND (AA INTERACT poly))) (width = 0.035um) for core NMOS/PMOS. 1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE or (GTDMP AND (AA INTERACT poly)) <0.23um. The violation is allowed when the violation length is \leq 0.08um. This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP, ESDPOB, CLPDMY and INST region.	=	0.03~0.05	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 80/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
GT.8c	<p>Width of 1st poly (or POLY_DMY) neighboring (GATE or (GTDMP AND (AA INTERACT poly))) (width = 0.04/0.045um) for core NMOS/PMOS.</p> <p>1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE or (GTDMP AND (AA INTERACT poly)) <0.23um.</p> <p>The violation is allowed when the violation length is ≤0.08um.</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY and INST region.</p>	=	0.03~0.06	um
GT.8d	<p>Width of 1st poly (or POLY_DMY) neighboring (GATE or (GTDMP AND (AA INTERACT poly))) (width ≥0.05um and ≤0.09 um) for core NMOS/PMOS.</p> <p>1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE or (GTDMP AND (AA INTERACT poly)) <0.23um, which excludes FUSEMK1 region.</p> <p>The violation is allowed when the violation length is ≤0.08um.</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, VARMOS and INST region.</p>	=	0.04~0.09	um
GT.9	(Purposely blank)			
GT.10	<p>Space</p> <p>This check doesn't check POLY_JOG, INDMY region.</p>	≥	0.08	um
GT.11	Space between poly inside DG/TG and poly	≥	0.18	um
GT.12a	<p>Space between poly and (poly or POLY_DMY) if at least one (poly or POLY_DMY) width ≥ 0.03um, and ≤0.09um, and the parallel run length >0.09um.</p> <p>DRC doesn't check INST region.</p>	≥	0.1	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 81/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
GT.12b	Space between poly and (poly or POLY_DMY) if at least one (poly or POLY_DMY) width >0.09um, and the parallel run length >0.09um. DRC doesn't check INST region	\geq	0.12	um
GT.13	At least one side space between (poly or POLY_DMY) and poly, when poly or POLY_DMY width <0.06um, and parallel run length of (poly or POLY_DMY) and two neighboring POLY_JOG >0um, or the parallel run length of (poly or POLY_DMY) and two neighboring poly line end >0um. DRC only check: 1. (poly or POLY_DMY) with width <0.06um is placed in between two neighboring POLY_JOG, the parallel run length of two POLY_JOG \geq 0um. 2. (poly or POLY_DMY) with width <0.06um is placed in between two neighboring poly line end(poly line end definition: poly width \leq 0.09um)	\geq	0.1	um
GT.14	Space between horizontal (poly NOT INTERACT GTMK2) when 1. at least one poly width>0.09um 2. poly parallel run length >0.09um. This rule doesn't check rectangular (poly INTERCACT AA) NOT AA).	\geq	0.15	um
GT.15	(Purposely blank)			
GT.16a	Space between ((GATE sizing up 0.06um) AND poly) (channel length = 0.03um) and (neighboring ((poly or POLY_DMY) NOT POLY_JOG)) for core NMOS/PMOS. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um. The POLY_JOG E2=0.08um.(Pls refer to POLY_JOG definition in 7.1.13). This rule isn't applicable for ESDIO1, ESDIO2,	=	0.1/0.105/0.11	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 82/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
	ESDCLP, ESDPOB, CLPDMY ,VARMOS,OCCD and INST region.			
GT.16b	<p>Space between ((GATE sizing up 0.06um) AND poly) (channel length = 0.035um) and (neighboring ((poly or POLY_DMY) NOT POLY_JOG)) for core NMOS/PMOS.</p> <p>Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um.</p> <p>The POLY_JOG E2=0.08um.(Pls refer to POLY_JOG definition in 7.1.13).</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY ,VARMOS and INST region.</p>	=	0.1/0.105	um
GT.16c	<p>Space between ((GATE sizing up 0.06um) AND poly) (0.04um ≤ channel length ≤ 0.09um) and (neighboring ((poly or POLY_DMY) NOT POLY_JOG)) for core NMOS/PMOS.</p> <p>Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um.</p> <p>The POLY_JOG E2=0.08um.(Pls refer to POLY_JOG definition in 7.1.13).</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, VARMOS, FUSEMK1 and INST region.</p>	=	0.1	um
GT.16d	<p>Space between ((GATE sizing up 0.06um) AND poly) (channel length > 0.09um) and neighboring (poly or POLY_DMY) for core NMOS/PMOS.</p> <p>Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um.</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY,VARMOS and INST region.</p>	=	0.12	um
GT.16e	Space between ((GATE sizing up 0.06um) AND poly) and neighboring (poly or POLY_DMY) for core device in ESDIO1, ESDIO2, ESDCLP,	≥	0.12	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 83/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
	ESDPOB, CLPDMY region. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um.			
GT.16f ^[R]	Space between ((GATE sizing up 0.06um) AND poly) and neighboring (poly or POLY_DMY) for I/O NMOS/PMOS. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.51um. This rule isn't applicable for GATE in ESDIO1, ESDIO2,ESDCLP, ESDPOB, CLPDMY, LDBK and VARMOS region.	=	0.18	um
GT.17	Space between 1st (poly or POLY_DMY) neighboring GATE (channel length = 0.03um/0.035um) and 2nd (poly or POLY_DMY) for core NMOS/PMOS. 2nd (poly or POLY_DMY) is must when the space between 2nd poly (or POLY_DMY) and neighboring GATE space =0.23um~0.28um. The violation is allowed when the violation parallel length is \leq 10% of neighboring GATE width. The violation is allowed when the violation length is \leq 0.08um. This rule isn't applicable for PSUB, VARMOS, ESDIO1, ESDIO2,ESDCLP, ESDPOB, CLPDMY, OCCD and INST region.	\geq	0.1	um
		\leq	0.15	um
GT.18	(Purposely blank)			
GT.19	(Purposely blank)			
GT.20	Space between AA and poly (or POLY_DMY) on STI. DRC doesn't check INST region.	\geq	0.025	um
GT.21a	Space between (((poly or POLY_DMY) NOT P2) INTERACT AA) and (((AA or AA_DMY) NOT INTERACT poly)) INTERACT CT), when width of (AA or AA_DMY) <0.07um, and the parallel	\geq	0.05	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 84/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
	run length > 0.09um			
GT.21b	Space between (poly or POLY_DMY) and (AA or AA_DMY), when width of (AA or AA_DMY) <0.07um, and the parallel run length >0um and ≤ 0.09um. DRC doesn't check INST region.	≥	0.05	um
GT.21c	Space between (poly or POLY_DMY) and AA, when 1. Space between two (poly or POLY_DMY) > 0.27um; 2. The parallel run length of (poly or POLY_DMY) and AA > 0.09um. This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP, ESDPOB, CLPDMY region.	≥	0.035	um
GT.21d	Space between poly and (AA or AA_DMY), when 1. Space between poly and (poly or POLY_DMY) > 0.27um; 2. The parallel run length of poly and (AA or AA_DMY) > 0.09um. This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP, ESDPOB, CLPDMY region.	≥	0.035	um
GT.22	Space between (AA INTERACT CT) and ((poly NOT P2) INTERCACT CT) , when 1. The parallel runlength >0um; 2. AA width ≥0.07um and <0.1um; 3. (Poly NOT P2) extension outside of CT <0.08um in opposite AA site; 3. AA and poly are at different net. DRC doesn't check: 1.INST region; 2.The edge L1 with length≤ 0.275um, which L1 is opposite to ((poly NOT P2) INTERCACT CT), and L1 and its adjencent edge formed one inner vertex 270 degree angle A, and AA width = 0.07um which formed by L1 and its opposite edge L2.	≥	0.04	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 85/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
	3. The space between poly line-end (poly edge length < 0.04um) and AA.			
GT.23a	Space between L-shape or U-shape poly and AA when poly and AA in the same MOS, when L shape poly length (L) \leq 0.03um. DRC doesn't check INST region.	\geq	0.035	um
GT.23b	Space between L-shape poly and AA when poly and AA in the same MOS, when L shape poly length (L) $> 0.03\text{um}$ and $\leq 0.07\text{um}$.	\geq	0.07	um
GT.24	Space between L-shape poly and (AA AND CT) when poly and AA in the same MOS, when L shape poly length (L) $\leq 0.03\text{um}$. DRC doesn't check INST region.	\geq	0.065	um
GT.25	Space between POLY_JOG. DRC only check the space is opposite to POLY_JOG E2 direction. (Pls refer to POLY_JOG definition in 7.1.13)	\geq	0.1	um
GT.26	Space between POLY_JOG and (poly or GTDMP or GTDOP)	\geq	0.07	um
GT.27	Space between (poly or POLY_DMY) and ((poly or POLY_DMY) AND SAB). DRC doesn't check INDMY region.	\geq	0.18	um
GT.28	Space between (poly NOT P2) and ((AA INTERACT CT) NOT INSIDE (DG OR TG)), which poly connects to (1.2V or 1.5V or 1.8V or 2.5V or 3.3V) net. DRC doesn't check EFUSE region. DRC check follows metal voltage marking layer for (1.2V or 1.5V or 1.8V or 2.5V or 3.3V) net.	\geq	0.065	um
GT.29a	Extension of AA outside of (poly or POLY_DMY) for core device with channel length $\leq 0.09\text{um}$. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, EFUSE, OCCD and INST region.	=	0.075/0.08/0.085	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 86/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
GT.29a ^[R]	Extension of AA outside of (poly INTERACT CT) for core device with channel length $\leq 0.09\mu m$. This rule isn't applicable for PSUB, VARMOS, ESDIO1, ESDIO2,ESDCLP, ESDPOB, CLPDMY, EFUSE,OCCD and INST region.	\geq	0.205	um
GT.29b	Extension of AA outside of (poly or POLY_DMY) for core device with channel length $> 0.09\mu m$. This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP,ESDPOB,CLPDMY, VARMOS,OCCD region.	=	0.095	um
GT.29c	Extension of AA outside of (poly or POLY_DMY) for core device in ESDIO1, ESDIO2,ESDCLP,ESDPOB,CLPDMY region.	\geq	0.095	um
GT.30a	Extension of AA outside of (poly or POLY_DMY) for I/O device region. This rule isn't applicable for LDMOS drain site region.	\geq	0.155	um
GT.30a ^[R]	Extension of AA outside of (poly or POLY_DMY) for I/O device region. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB,CLPDMY, VARMOS, LDMOS drain site region.	=	0.155	um
GT.30b	Extension of AA outside of (poly or POLY_DMY) for I/O device in ESDIO1, ESDIO2, ESDCLP, ESDPOB,CLPDMY region.	\geq	0.155	um
GT.31	Extension of poly outside of AA along channel width direction. This rule isn't applicable for INDMY, LOGO and INST region.	\geq	0.08	um
GT.32	(Purposely blank)			
GT.33	Extension of poly outside of AA when the poly to L-shape AA (in same MOS) space $< 0.1\mu m$. DRC doesn't check INST region.	\geq	0.095	um
GT.34	((Poly or POLY_DMY) NOT P2) density in full	\geq	15%	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 87/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
	chip	\leq	40%	
GT.35	((Poly or POLY_DMY) NOT P2) density. Density check window: Window size: 20um*20um, step size: 10um. For low density , DRC don't check: 1. RESAA, DSTR, and BIPOLA. 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer. For high density, DRC doesn't flag violation when all channel length>0.06um device in check window.	\geq	10%	
		\leq	65%	
GT.36	((Poly or POLY_DMY) NOT P2)) density inside of the dummy block area(DUMBP).Density check window size: 10um*10um, step size: 5um DRC need check the design if DUMBP width is >3um and <10um, where density ratio= ((poly or POLY_DMY) NOT P2) area/DUMBP area. This rule doesn't check MOMDMY and OCOVL region.	\geq	10%	
GT.37	Rectangular poly length	\geq	0.26	um
GT.38	(Purposely blank)			
GT.39a	(Poly NOT P2) length between two CTs(the two CTs on same poly), when poly width <0.06um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, RESP1 and (poly INTERACT MOMDMY) region.	\leq	18	um
GT.39b	The length from the any point inside poly GATE to (the nearest CT on GATE poly) (without P2 between GATE and CT), when poly width <0.06um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY and (poly INTERACT MOMDMY) region.	\leq	18	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 88/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
GT.40	Poly area. DRC doesn't check rectangle (poly INTERACT AA) with length \geq 0.32 um	\geq	0.0115	um ²
GT.41	Poly enclosed area	\geq	0.02	um ²
GT.42	Only axes of poly geometry at 0-degree (X), 90-degree (Y) are allowed, 45-degree poly is not allowed. This rule doesn't check NODMF, EFUSE, LOGO and INDMY region.			
GT.43^[R]	O-shape poly is not allowed, except the LOGO area. DRC doesn't check INST region.			
GT.44^[NC]	Poly line-end must be rectangular.			
GT.45^[R]	((Poly NOT P2) NOT INSIDE (DG OR TG)) must be rectangle. This rule doesn't check NODMF, EFUSE, LOGO and INST region.			
GT.46^[R]	(((Poly NOT P2) OUTSIDE (DG OR TG)) INTERACT AA)) must be rectangle. DRC doesn't check INST region.			
GT.47	Floating ((poly NOT P2) NOT INTERACT CT) must be a rectangle DRC doesn't check INST, EFUSE and LOGO region, and doesn't check the poly with width \geq 0.15um.			
GT.48	GATE of core device must be in vertical direction. This rule doesn't check VARMOS, LOGO, NODMF, GTMK2 region.			
GT.49^[R]	In core device region, rectangle (poly NOT INTERACT AA) must be vertical, which is same as GATE poly direction. This rule doesn't check BIPOLA, DSTR, LOGO, and square pattern.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 89/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
GT.50	(Poly or POLY_DMY) width on same AA must be same for core device region with channel length=0.03um. DRC doesn't check ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, OCCD and INST regions.			
GT.51 ^[R]	Recommended poly width on same AA must be same for core device with channel length \geq 0.15um. DRC doesn't check ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY and INST regions.			
GT.52	Space between ((poly and (poly or POLY_DMY)) on same AA must be same for channel length =0.03/0.035um core device. DRC doesn't check PSUB, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, INST, OCCD and VARMOS region.			
GT.53	Poly interacting AA must separate at least two AA diffusions. DRC doesn't check (poly INTERACT INST), LDBK, LOGO, OCOVL and INDMY region.			
GT.54	(Poly NOT P2) must be covered by SN or SP. DRC doesn't check INDMY, LOGO, OCCD, OCOVL, EFUSE and (Poly INTERACT MOMDMY) region.			
GT.55	Floating gate is prohibited if the effective source/drain are not connected together. Definition of floating GATE: (1) GATE without poly CT (2) GATE with poly CT but not connected to MOS AA, pickup AA or ALPA pad, which excludes GATE with poly CT connected to metal in IP level. Definition of the effective source/drain: Source/drain is connected to different (MOS AA NOT poly), pickup AA, GATE or ALPA pad. Resistor poly is considered as conduct poly. This rule doesn't check INST, LOGO, OCCD, OCOVL region.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

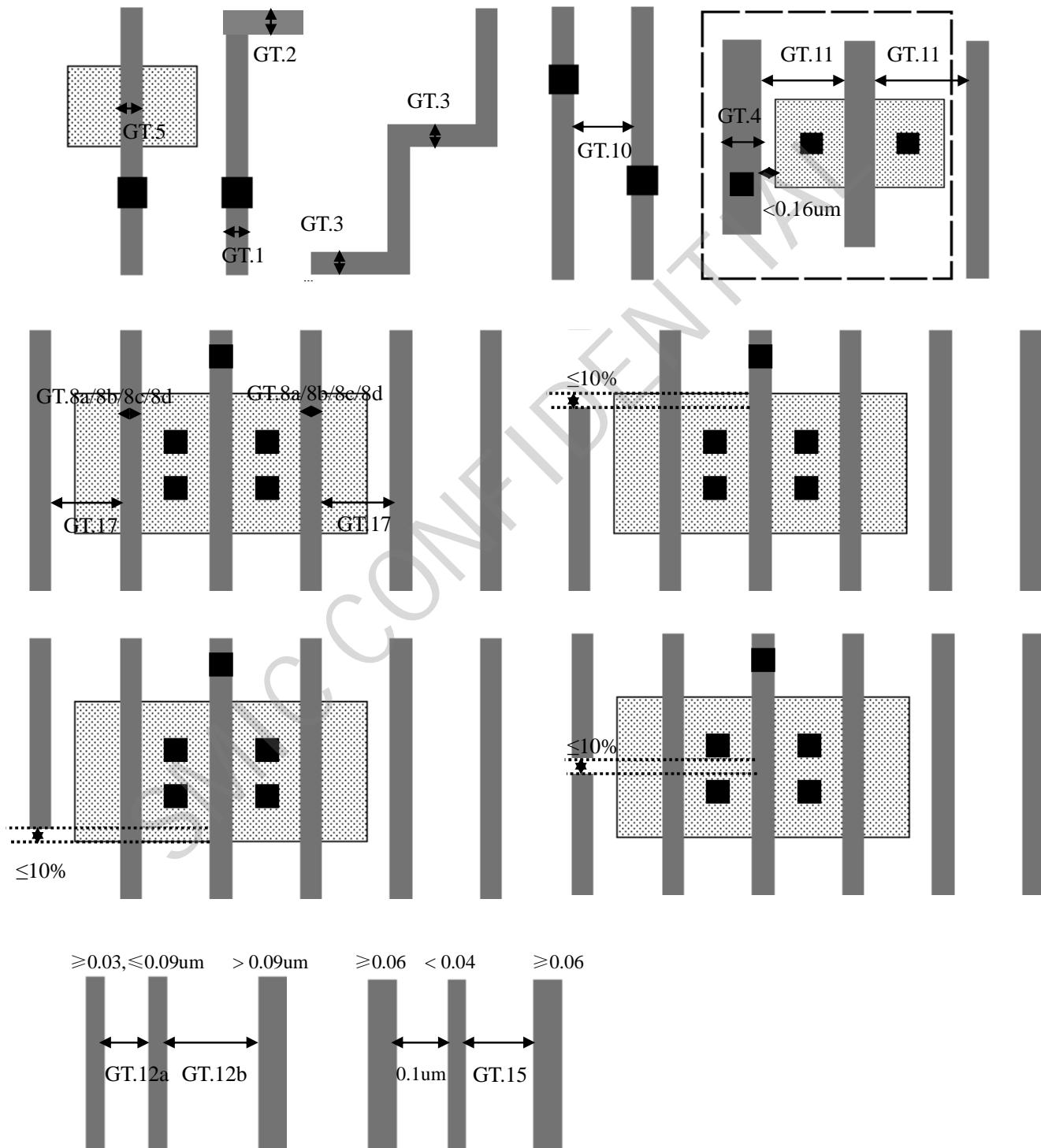


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 90/306
---------------------------	---	------------	----------------------	------------------

Rule number	Description	Operation	Design Value	Unit
	Set DRC switch for IP level and full chip, default open switch is for chip level check.			
GT.56	((poly OR GTDMP) OR GTDOP) NOT P2) NOT INSIDE (DG OR TG) can't apply the voltage > 3.3V.			
GT.57	L-shape (poly NOT P2) number, when (1) space between poly and AA <0.07um, (2) poly and AA are in the same MOS (3) L-shape poly length (L) ≤ 0.03um DRC doesn't check POLY_JOG with E3>0um(Pls refer to POLY_JOG definition in 7.1.13), and skip to check INST region.	<	2	

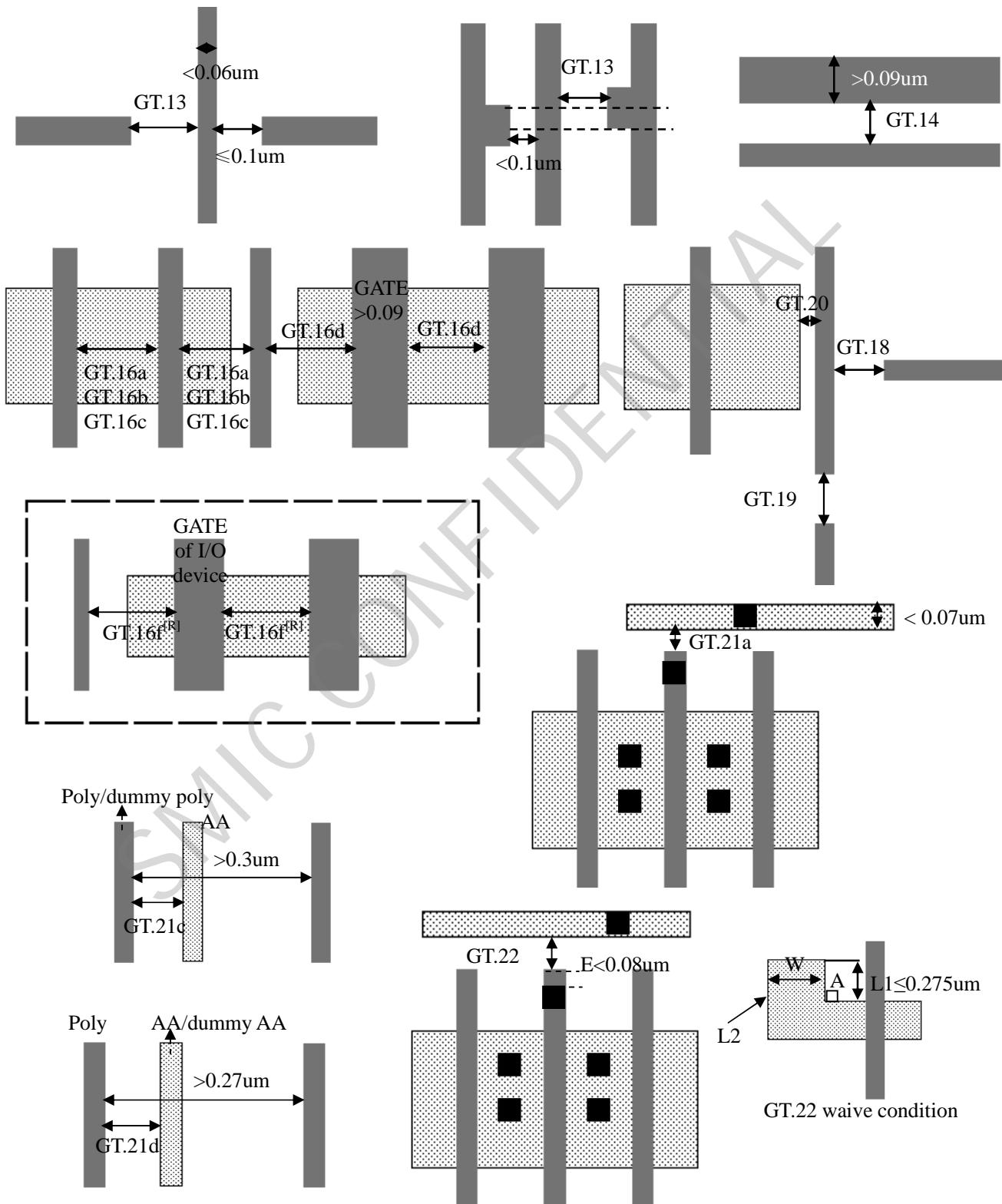
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 91/306
---------------------------	---	------------	----------------------	------------------



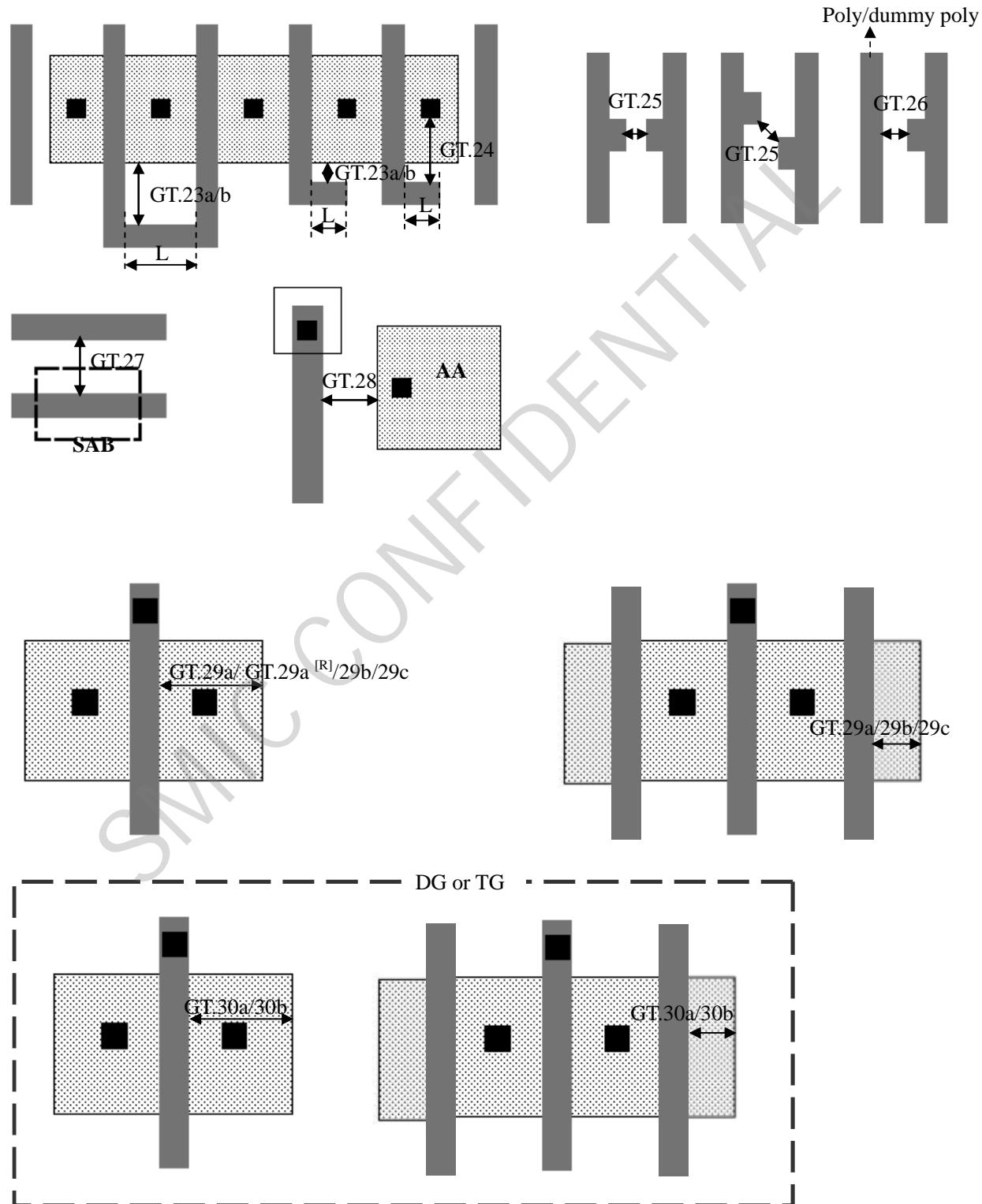
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 92/306
---------------------------	---	------------	----------------------	------------------



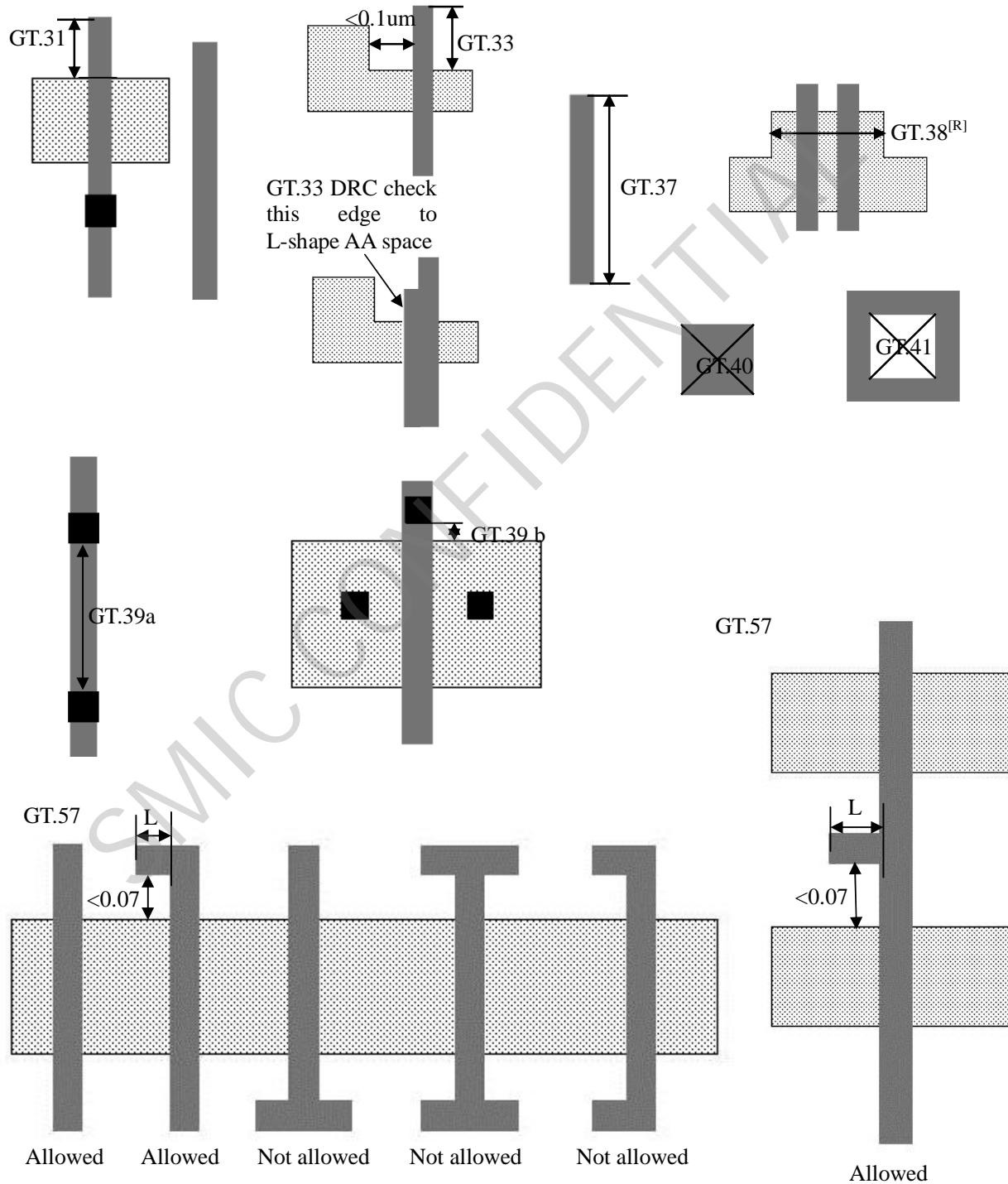
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 93/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 94/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 95/306
---------------------------	---	------------	----------------------	------------------

7.2.10 GTDMP: GT dummy desing rules

Rule number	Description	Operation	Design Value	Unit
GTDMP.1	Width	\geq	0.03	um
GTDMP.2	Width inside DG/TG	\geq	0.1	um
GTDMP.3	Space between two GTDMPs if at least one GTDMP width \geq 0.03um, and \leq 0.09um, and the parallel run length \geq 0.1um	\geq	0.1	um
GTDMP.4	Space between two GTDMPs if at least one GTDMP width $>$ 0.09um, and the GTDMP parallel run length \geq 0.1um	\geq	0.12	um
GTDMP.5	Space between GTDMP and ((poly or GTDMP) or GTDOP). It's not allowed ((GTDMP interact poly) outside P2). DRC doesn't check POLY_JOG.	\geq	0.08	um
GTDMP.6	Space between (GTDMP AND AA) and neighboring GATE or (GTDMP AND AA)	\geq	0.1	um
GTDMP.7	Space between two (GTDMP AND AA) inside DG/TG in the same AA	\geq	0.18	um
GTDMP.8	Space between GTDMP and INDMY	\geq	1.2	um
GTDMP.9	Space between (GTDMP AND AA) and SAB. ((GTDMP AND AA) and SAB overlap is not allowed). This rule isn't applicable for RESP1, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.38	um
GTDMP.10	Space between (GTDMP AND AA) and CT for core device when GTDMP width \leq 0.09um ((GTDMP AND AA) and CT overlap is not allowed)	\geq	0.03	um
GTDMP.11	Space between (GTDMP AND AA) and CT for core device when GTDMP width $>$ 0.09um. ((GTDMP AND AA) and CT overlap is not allowed)	\geq	0.04	um
GTDMP.12	Space between (GTDMP AND AA) and CT for IO device. ((GTDMP AND AA) and CT overlap is not allowed)	\geq	0.07	um
GTDMP.13	(Poly OR GTDMP) extension outside of AA DRC doesn't check INST region.	\geq	0.08	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

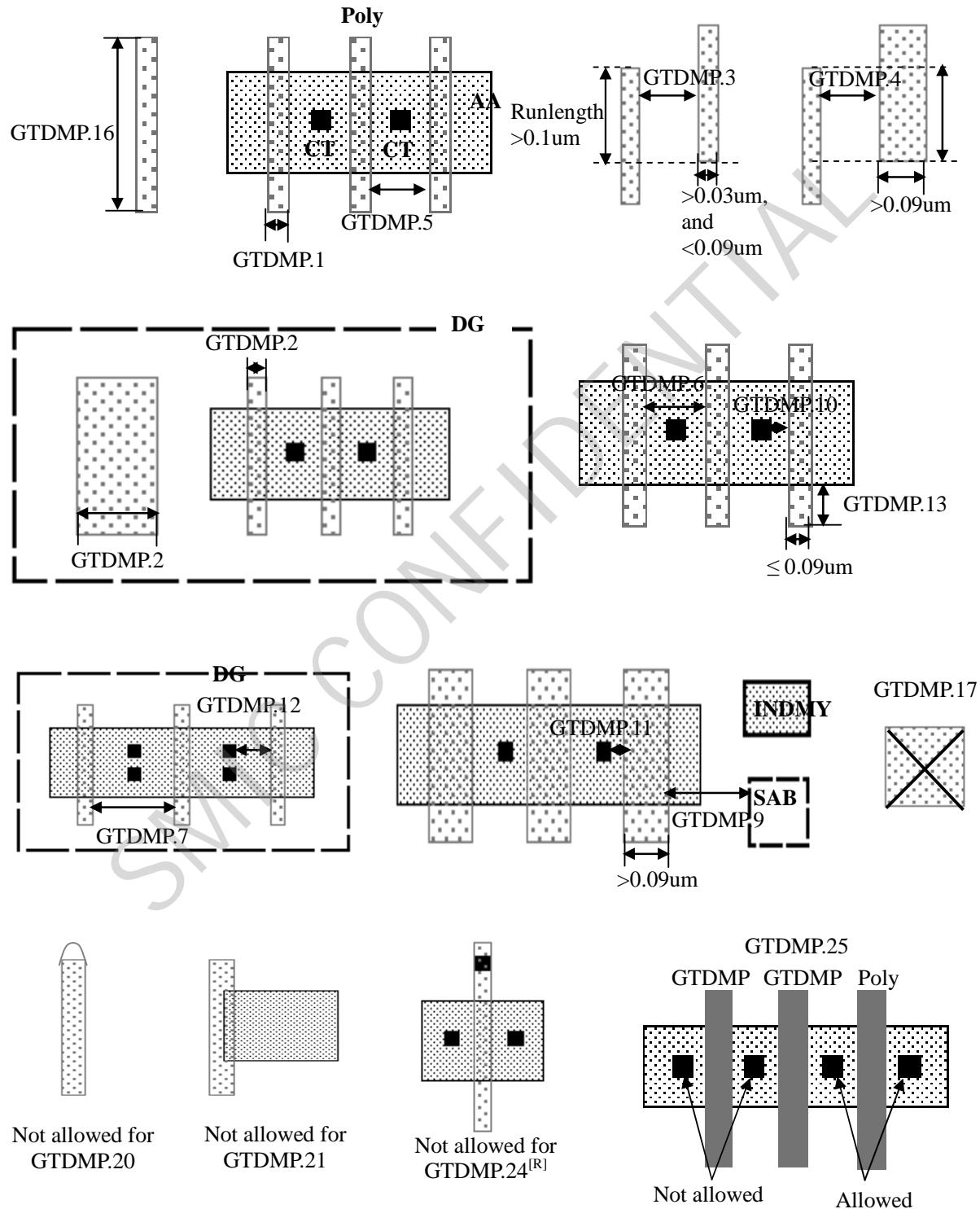


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 96/306
---------------------------	---	------------	----------------------	------------------

GTDM^P.14	GTDM ^P extension outside of AADMP	≥	0.08	um
GTDM^P.15	AADMP extension outside of GTDM ^P	≥	0.075	um
GTDM^P.16	Rectangular GTDM ^P length	≥	0.26	um
GTDM^P.17	GTDM ^P area. DRC doesn't check rectangle (GTDM ^P INTERACT AA) with length ≥ 0.32 um	≥	0.0115	um ²
GTDM^P.18^[R]	((Poly or POLY_DMY) NOT P2) density. DRC check region follow: (((AA OR poly) INTERACT GATE) sizing up 2um) NOT ((AA OR poly) sizing up 0.15um)) DRC doesn't check VARMOS, NODMF, INST, DG, TG, OCOVL and OCCD region.	≥	7%	
GTDM^P.19	GTDM ^P (NOT P2) must be rectangular.			
GTDM^P.20^[NC]	GTDM ^P line-end must be rectangular.			
GTDM^P.21	GTDM ^P interacting AA must separate at least two AA diffusions. DRC doesn't check MOMDMY region.			
GTDM^P.22	(GTDM ^P AND AA) of core device must be vertical direction. This rule isn't applicable for the regions covered by BIPOLA, DSTR, NODMF and LOGO.			
GTDM^P.23^[NC]	GTDM ^P (30;8) can not form device.			
GTDM^P.24	CT is not allowed to land on GTDM ^P			
GTDM^P.25	CT is not allowed to be placed between GTDM ^P and AA edge, or two GTDM ^P s.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 97/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



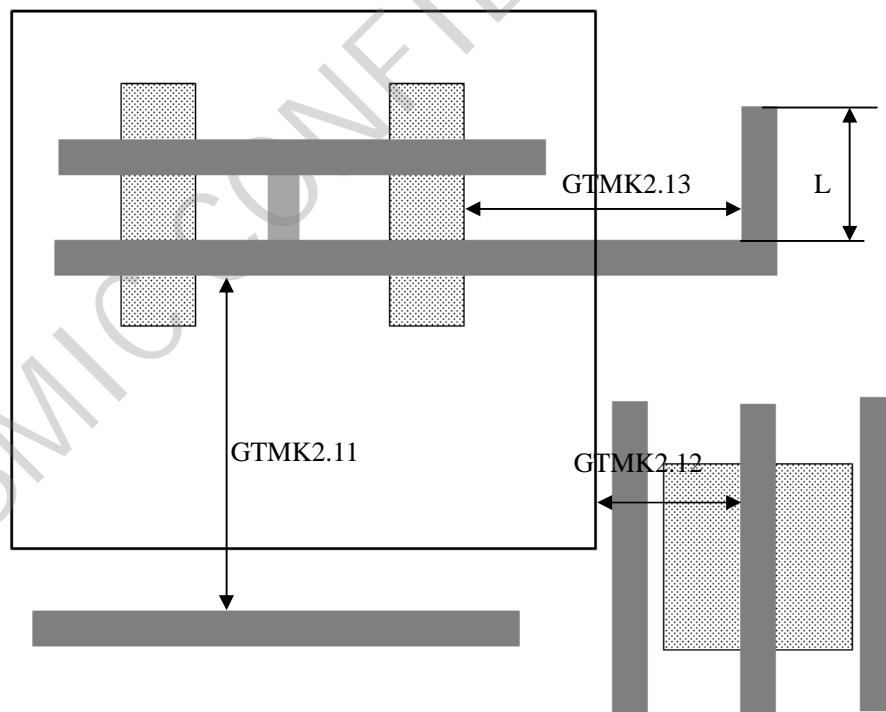
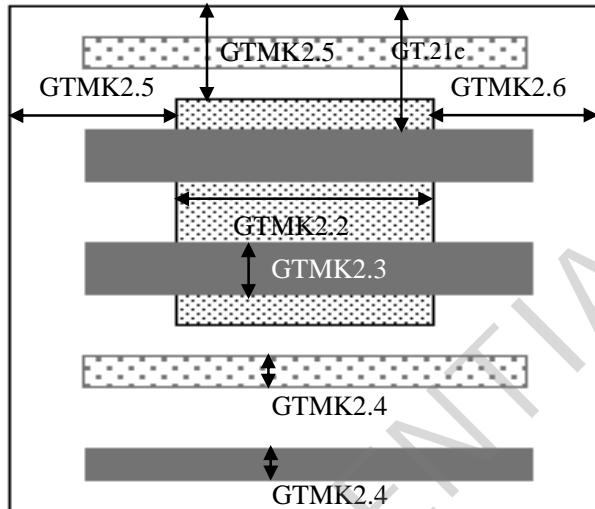
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 98/306
---------------------------	---	------------	----------------------	------------------

7.2.11 GTMK2: Core Horizontal GATE design rules

Rule number	Description	Operation	Design Value	Unit
GTMK2.1	GTMK2 is the marking layer for the horizontal gate in core region. GTMK2 must be drawn for the horizontal gate in core region.			
GTMK2.2	Channel width in GTMK2	\geq	0.3	um
		\leq	3	um
GTMK2.3	Channel length in GTMK2	\geq	0.1	um
		\leq	6	um
GTMK2.4	Width of (poly or GTDMP or GTDOP) in GTMK2	\geq	0.04	um
GTMK2.5	GTMK2 enclosure of N+ AA or P+ AA	\geq	0.04	um
GTMK2.6	GTMK2 must fully cover (GATE INTERACT GTMK2)	\geq	0.08	um
GTMK2.7	(AA INTERACT poly) inside GTMK2 must be rectangular.(45 degree edge is not allowed)			
GTMK2.8	GATE inside GTMK2 must be in horizontal direction.			
GTMK2.9	It's not allowed that horizontal GATE NOT INSIDE GTMK2 in core region			
GTMK2.10	It's not allowed GTMK2 overlap LVT_N, LVT_P, DG, TG, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, P2, NODMF, EFUSE, LOGO.			
GTMK2.11	Space between ((poly or GTDMP or GTDOP) INTERACT GTMK2) and ((poly or GTDMP or GTDOP)	\geq	0.12	um
GTMK2.12	Space between GTMK2 and (GATE OUTSIDE GTMK2)	\geq	0.08	um
GTMK2.13	Space between L shape poly and AA when poly and AA in same MOS, and L shape poly interact with GTMK2, and L shape length (L) \leq 0.08um.	\geq	0.16	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 99/306
---------------------------	---	------------	----------------------	------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 100/306
---------------------------	---	------------	----------------------	-------------------

7.2.12 P2: Poly cut design rules

Rule number	Description	Operation	Design Value	Unit
P2.1	P2 width DRC doesn't check INST region	=	0.08	um
P2.2	P2 length DRC doesn't check INST region	\geq	0.15	um
P2.3	Poly width which the poly is cut by P2. DRC only check P2 overlap poly region	\leq	0.5	um
P2.4	Space between P2 and P2	\geq	0.09	um
P2.5	Space between P2 and ((poly OR GTDMP) OR GTDOP) in P2 length direction.	\geq	0.04	um
P2.6	Space between P2 and ((poly OR GTDMP) OR GTDOP) excluding P2 length direction DRC doesn't check INST region	\geq	0.02	um
P2.7	Space between P2 and AA (overlap is not allowed). DRC doesn't check INST region.	\geq	0.035	um
P2.8	Space between P2 and GATE in P2 width direction when space between poly and L-shape AA in the same MOS < 0.1um (overlap is not allowed). DRC doesn't check INST region.	\geq	0.05	um
P2.9	Space between P2 and CT (overlap is not allowed) DRC doesn't check INST region.	\geq	0.02	um
P2.10	P2 extension outside of ((poly OR GTDMP) OR GTDOP) in P2 length direction	\geq	0.05	um
P2.11	P2 extension outside of ((poly OR GTDMP) OR GTDOP) in P2 width direction. DRC doesn't check INST region	=	0.03/0.035	um
P2.12	((Poly OR GTDMP) OR GTDOP) extension outside of P2. DRC doesn't check INST region.	\geq	0.1	um
P2.13	It's not allowed P2 overlap DG/TG/PSUB/AA/CT.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

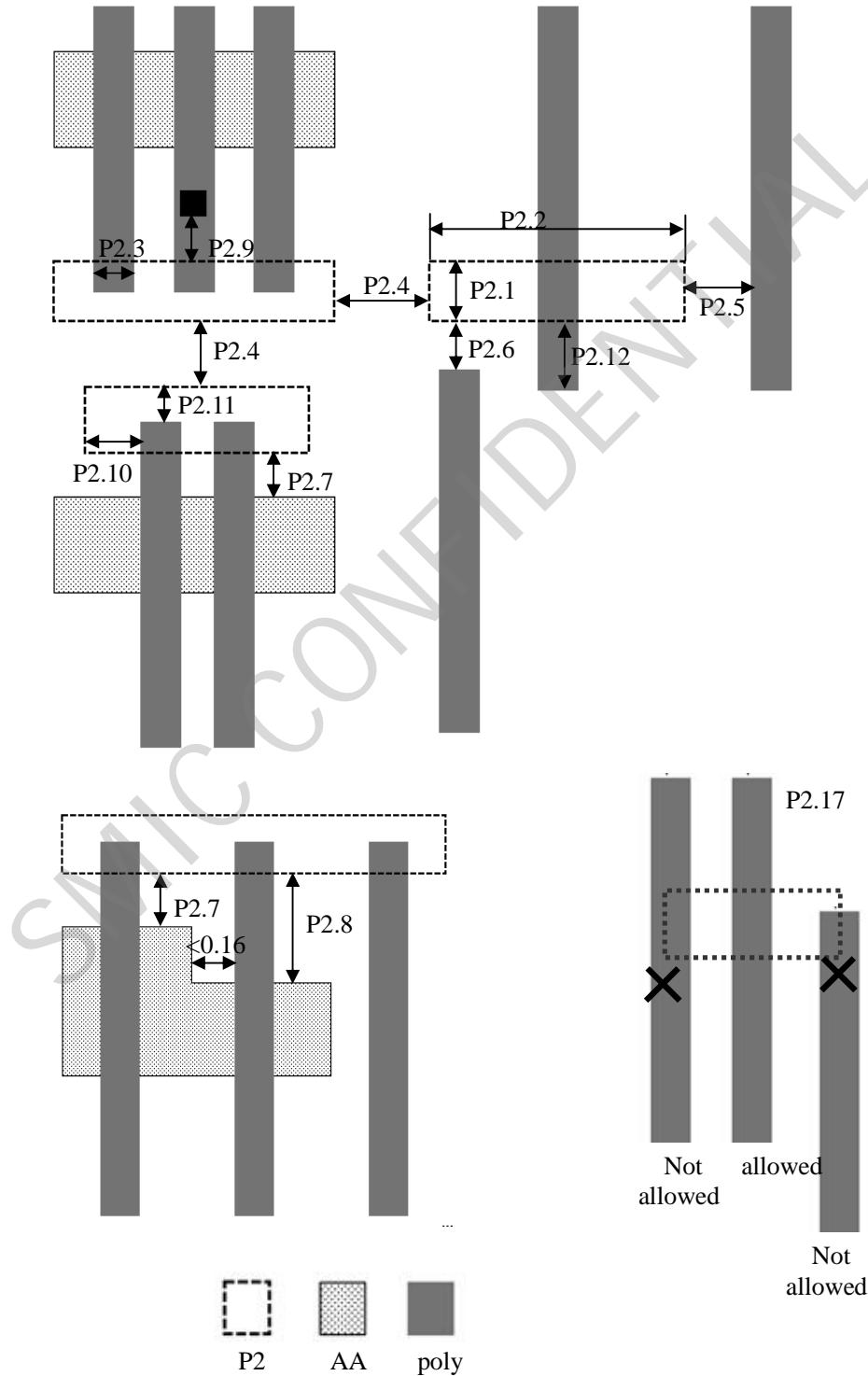


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 101/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check P2 overlap AA in INST region.			
P2.14	P2 must INTERACT ((poly OR GTDMP) OR GTDOP)			
P2.15	P2 must be in the horizontal direction which is perpendicular to the core GATE poly length direction in same chip.			
P2.16	P2 must be rectangular			
P2.17	It's not allowed (any vertex of P2) INTERACT ((poly OR GTDMP) OR GTDOP)			
P2.18	((Poly OR GTDMP) OR GTDOP) AND P2 must be rectangular except small jogs (jog \leq 0.005um)			
P2.19	Area of (((poly OR GTDMP) OR GTDOP) NOT P2). This rule doesn't check rectangle (((poly OR GTDMP) OR GTDOP) NOT P2) INTERACT AA) any edge \geq 0.23um.	\geq	0.009	um ²
P2.20	Overlap area of P2 and AA_DMY.	\leq	0.01	um ²
P2.21	The outermost ((Poly OR GTDMP) INTERACT P2) must be floating when P2 length \geq 18um. The floating definition is: (((Poly OR GTDMP) NOT P2) NOT INTERACT CT).			
P2.22 ^[R]	Recommended (P2 or P2DUM or P2DOP) density in full chip	\geq	5%	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 102/306
---------------------------	---	------------	----------------------	-------------------



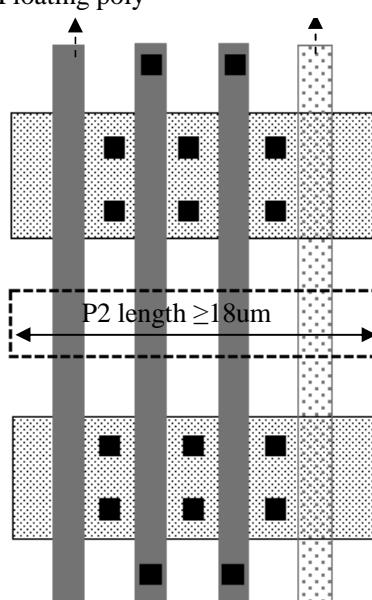
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 103/306
---------------------------	---	------------	----------------------	-------------------

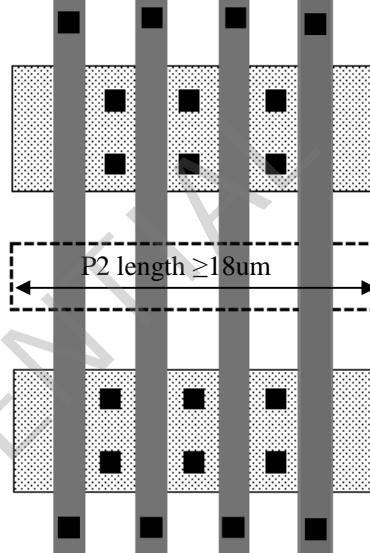
P2.21

Floating poly

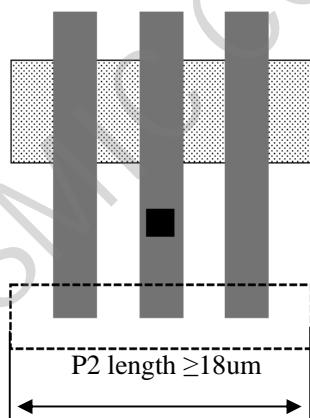
GTDMP



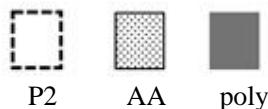
(a) Allowed



(b) Not allowed



(c) DRC skip to check



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 104/306
---------------------------	---	------------	----------------------	-------------------

7.2.13 SN: N+ source/drain implantation design rules

Rule number	Description	Operation	Design Value	Unit
SN.1	SN width. Single-point-interaction is allowed. DRC doesn't check INST region	\geq	0.16	um
SN.2	Space between SNs. Single-point-interaction is allowed.	\geq	0.16	um
SN.3 ^[R]	Space between SNs with parallel run length >0.24um, when one SN width >0.22um.	\geq	0.18	um
SN.4	Space between SNs, when one or both SNs width (W1) < 0.22um. DRC only check opposite sides.	\geq	0.22	um
SN.5	Space between SNs with parallel run length >0.33um and SN space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
SN.6	Space between SN and GATE along the source/drain direction. DRC doesn't check INST region.	\geq	0.14	um
SN.7	Space between SN and GATE along GATE poly direction. DRC doesn't check INST region.	\geq	0.065	um
SN.8	Space between SN and non-butted P+AA. DRC doesn't check INST region.	\geq	0.065	um
SN.9	Space between SN and non-butted P+ pick-up AA	\geq	0.02	um
SN.10 ^[NC]	Space between SN and butted P+ AA or P+ pick-up AA	=	0	um
SN.11	Space between butted N+ pick-up AA and PMOS GATE in the same AA.	\geq	0.165	um
SN.12	Space between butted N+ pick-up AA (in L shape AA) and PMOS GATE poly in the same AA, when this butted N+ pick-up AA extrusion: $0 < h < 0.08\text{um}$	\geq	0.165	um
SN.13	SN extension outside of GATE along the source/drain direction.	\geq	0.14	um
SN.14	SN extension outside of NMOS GATE along the source/drain direction where there is a butted P+ pick-up AA in the same AA	\geq	0.165	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



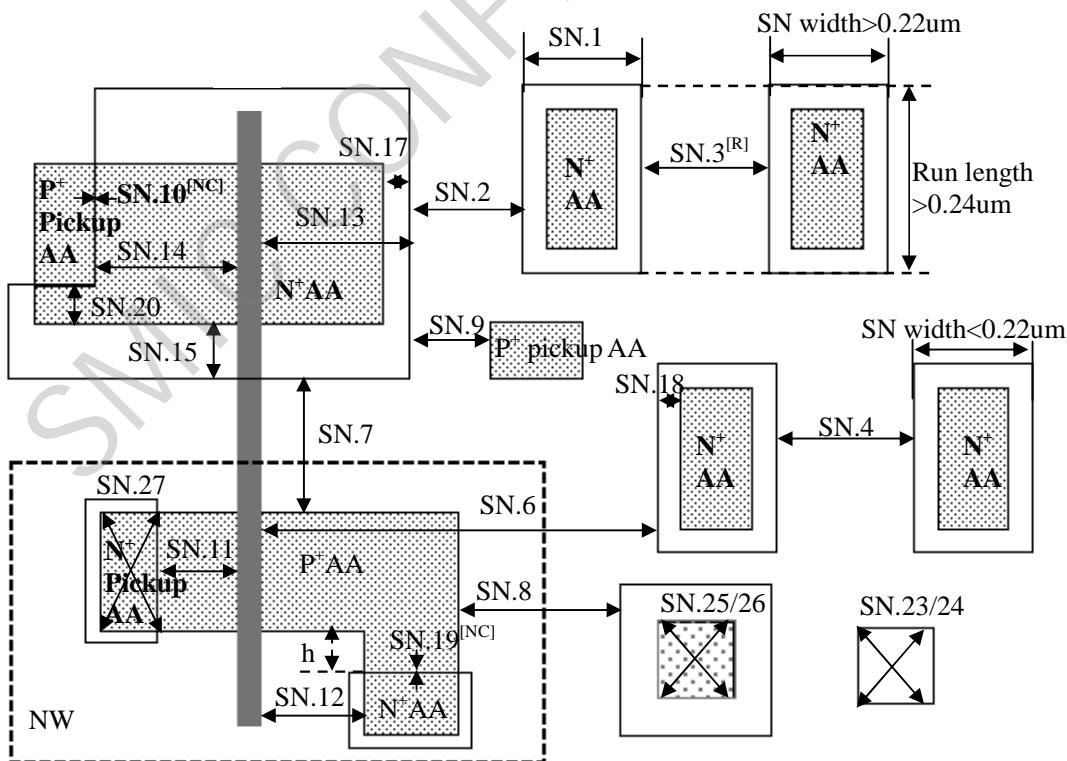
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 105/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check INST region.			
SN.15a	SN extension outside of GATE along the GATE poly direction for core device. DRC doesn't check INST region.	\geq	0.065	um
SN.15b	SN extension outside of GATE along the GATE poly direction for IO device. DRC doesn't check INST region.	\geq	0.13	um
SN.16	SN extension outside of NW/DG/TG. Extension=0um is allowed. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SN.17	Enclosure of N+ AA by SN. DRC doesn't check INST and (AA INTERACT RESNW) region.	\geq	0.065	um
SN.18	Enclosure of non-butted N+ pickup AA by SN.	\geq	0.02	um
SN.19^[NC]	Enclosure of butted N+ pickup AA by SN.	\geq	0	um
SN.20	SN and AA overlap	\geq	0.08	um
SN.21	SN and DG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SN.22	SN and TG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SN.23	Area of SN, while (((((SN NOT NW) INTERACT CT)sizing up 0.079um)sizing down 0.158um)sizing up 0.079um) DRC doesn't check INST region. DRC doesn't flag the rectangle pattern, when 1. Any one of the edge length =0.33um, 2. The space between any two outer vertexes =0.16um	\geq	0.1	um ²
SN.24	Area of SN.	\geq	0.07	um ²
SN.25	Enclosed area of SN, while (((((SN NOT NW) INTERACT CT)sizing up 0.079um)sizing down 0.158um)sizing up 0.079um)	\geq	0.1	um ²

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

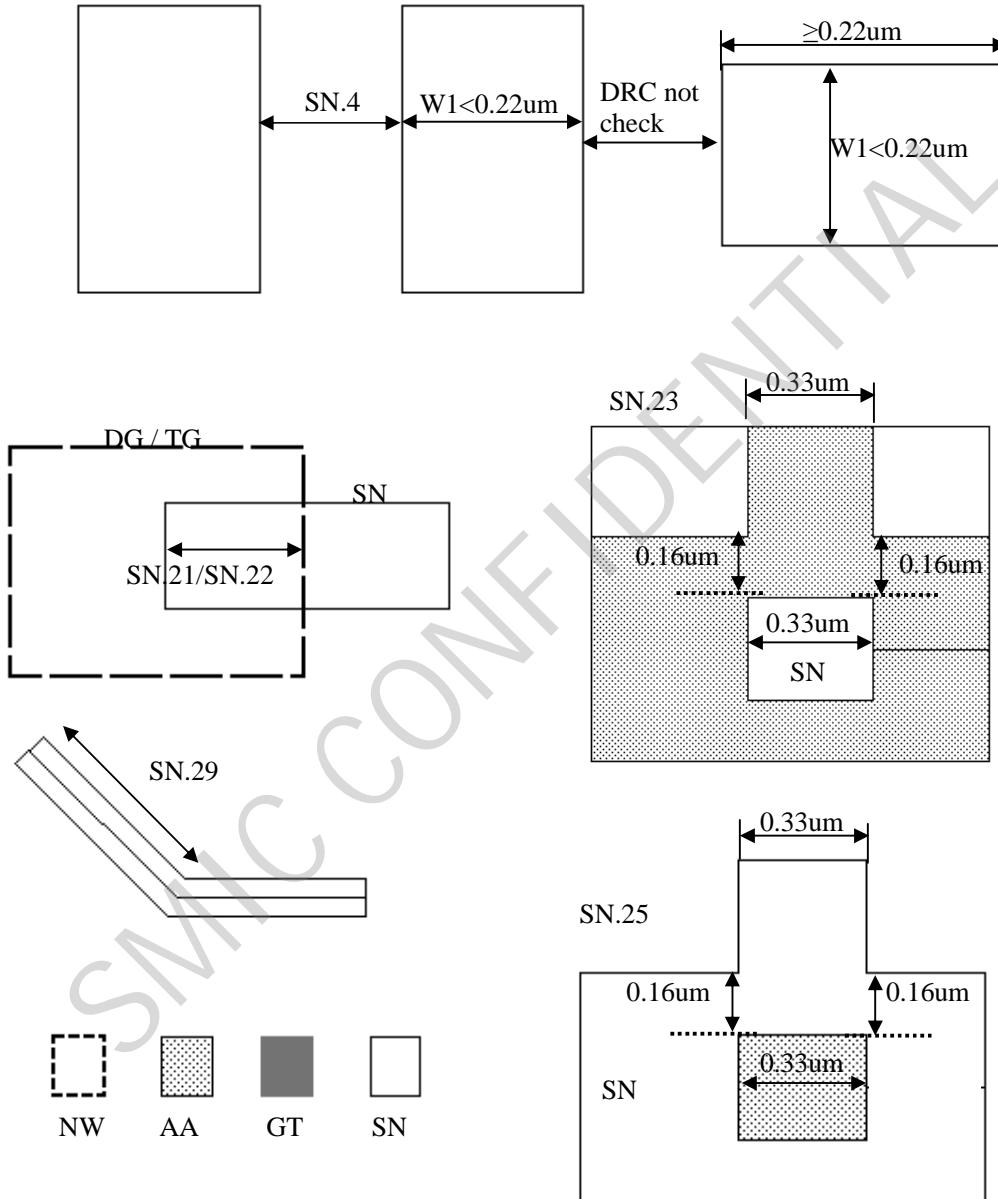
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 106/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check INST region. DRC doesn't flag the rectangle pattern, when 1. Any one of the edge length =0.33um, 2. The space between any two inner vertexes =0.16um			
SN.26	Enclosed area of SN.	\geq	0.07	μm^2
SN.27	N+ butted AA in NW area(the area interact with CT)	\geq	0.024	μm^2
SN.28	SN and SP overlap is forbidden			
SN.29	45-degree edge length	\geq	0.52	μm
SN.30	(SN AND (AA AND poly)) in NW is not allowed, except LDBK and VARMOS region.			



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev. 2	Tech Dev Rev: 1.10.1	Page No.: 107/306
TD-LO28-DR-2006					



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 108/306
---------------------------	---	------------	----------------------	-------------------

7.2.14 SP : P+ source/drain implantation design rules

Rule number	Description	Operation	Design Value	Unit
SP.1	SP width. Single-point-interaction is allowed.	\geq	0.16	um
SP.2	Space between SPs. Single-point-interaction is allowed. DRC doesn't check INST region.	\geq	0.16	um
SP.3 ^[R]	Space between SPs with parallel run length >0.24um, when one SP width >0.22um	\geq	0.18	um
SP.4	Space between SPs when one or both SPs width (W1) < 0.22um. DRC only check opposite sides.	\geq	0.22	um
SP.5	Space between SPs with parallel run length >0.33um and SP space on STI(not INTERACT AA OR AA_DMY)	\geq	0.25	um
SP.6	Space between SP and GATE along the source/drain direction.	\geq	0.14	um
SP.7	Space between SP and GATE along GATE poly direction. DRC doesn't check INST region.	\geq	0.065	um
SP.8	Space between SP and non-butted N+AA. DRC doesn't check INST region.	\geq	0.065	um
SP.9	Space between SP and non-butted N+ pickup AA	\geq	0.02	um
SP.10 ^[NC]	Space between SP and butted N+ AA or N+ pick-up AA	=	0	um
SP.11	Space between a butted P+ pick-up AA and NMOS GATE in the same AA. DRC doesn't check INST region.	\geq	0.165	um
SP.12	Space between a butted P+ pick-up AA (in L shape AA) and NMOS GATE poly in the same AA, when this butted P+ pick-up AA extrusion: $0 < h < 0.08\text{um}$	\geq	0.165	um
SP.13	SP extension outside of GATE along the source/drain direction. DRC doesn't check INST region.	\geq	0.14	um
SP.14	SP extension outside of PMOS GATE along the source/drain direction where there is a butted N+ pick-up AA in the same AA	\geq	0.165	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 109/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
SP.15a	SP extension outside of GATE along the GATE poly direction for core device. DRC doesn't check INST region.	\geq	0.065	um
SP.15b	SP extension outside of GATE along the GATE poly direction for IO device. DRC doesn't check INST region.	\geq	0.13	um
SP.16	SP extension outside of DG/TG. Extension=0um is allowed. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.17	Enclosure of P+ AA by SP. DRC doesn't check INST region.	\geq	0.065	um
SP.18	Enclosure of non-butted P+ pickup AA by SP	\geq	0.02	um
SP.19 ^[NC]	Enclosure of butted P+ pickup AA by SP	\geq	0	um
SP.20	SP and AA overlap	\geq	0.08	um
SP.21	SP and NW overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.22	SP and DG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.23	SP and TG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.24	Area of SP, while (((SP AND NW) INTERACT CT) sizing up 0.079um) sizing down 0.158um) sizing up 0.079um). DRC doesn't check INST region. DRC doesn't flag the rectangle pattern, when 1.Any one of the edge length =0.33um, 2.The space between any two outer vertexes =0.16um.	\geq	0.1	um ²
SP.25	Area of SP.	\geq	0.07	um ²
SP.26	Enclosed area of SP, while (((SP AND NW) INTERACT CT) sizing up 0.079um) sizing down 0.158um) sizing up 0.079um). DRC doesn't check INST region.	\geq	0.1	um ²

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

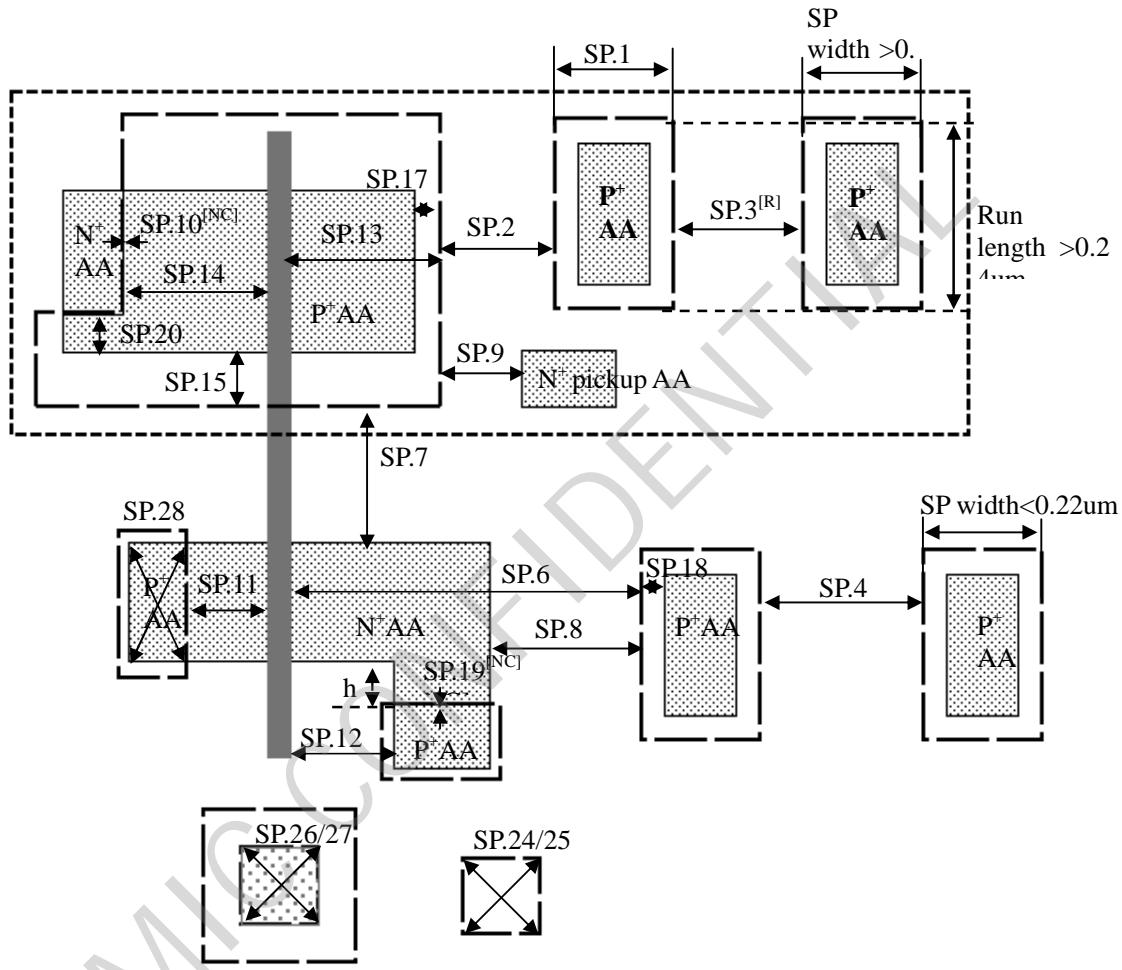


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 110/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC doesn't flag the rectangle pattern, when 1.Any one of the edge length =0.33um, 2.The space between any two inner vertexes =0.16um.			
SP.27	Enclosed area of SP.	\geq	0.07	um ²
SP.28	P+ butted AA in P-well area(the area interact with CT). DRC doesn't check INST region.	\geq	0.024	um ²
SP.29	45-degree edge length	\geq	0.52	um
SP.30	(SP AND (AA AND poly)) in PW is not allowed. DRC doesn't check LDBK, VARMOS and INST region.			

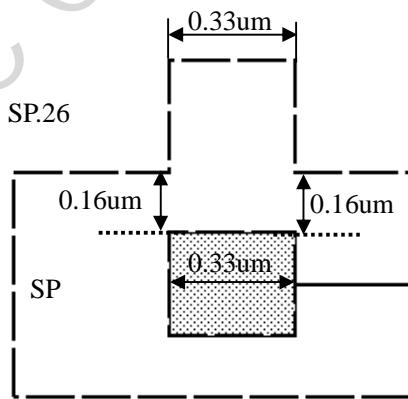
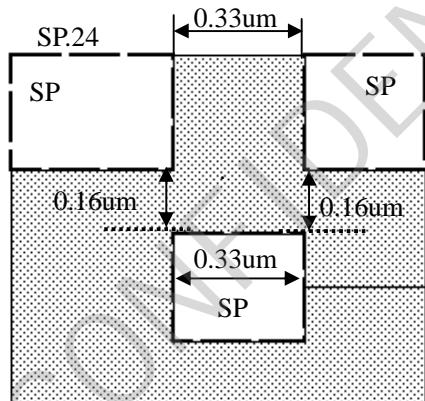
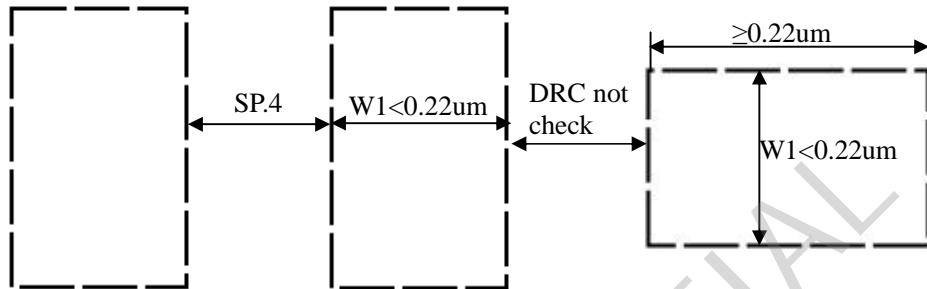
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 111/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 112/306
---------------------------	---	------------	----------------------	-------------------



NW AA GT SP

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 113/306
---------------------------	---	------------	----------------------	-------------------

7.2.15 SAB: Salicide Block design rules

Rule number	Description	Operation	Design Value	Unit
SAB.1	SAB width	\geq	0.32	um
SAB.2	Space between SABs	\geq	0.32	um
SAB.3	Extension of related AA outside of SAB	\geq	0.22	um
SAB.4	Space between SAB and AA	\geq	0.22	um
SAB.5	Space between SAB and GATE. Overlap of SAB and GATE is not allowed. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, OCOVL,INDMY region.	\geq	0.38	um
SAB.6a	Extension of SAB outside of unsilicided AA resistor or non-silicide poly resistor. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.22	um
SAB.6b	Extension of SAB outside of unsilicided AA resistor or non-silicide poly resistor when SAB width and length >10um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.3	um
SAB.6c	Extension of SAB outside of unsilicided AA resistor or non-silicide poly resistor when SAB width \leq 0.43um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.3	um
SAB.7	Space between SAB and CT	\geq	0.12	um
SAB.8	(Purposely blank)			
SAB.9	SAB area	\geq	0.9	um ²
SAB.10	SAB enclosed area	\geq	0.9	um ²
SAB.11	Space between SAB and (poly on STI).	\geq	0.3	um
SAB.12	SAB and poly must not overlap one another, except poly interact with RESP1, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, INDMY			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



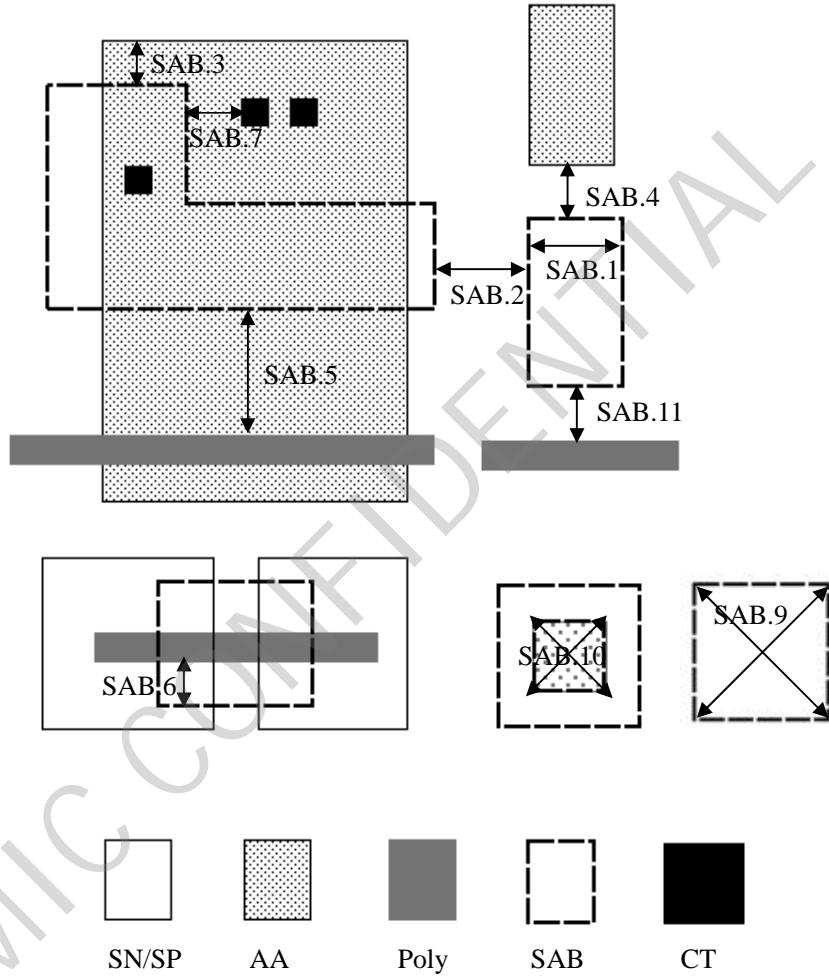
Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	Tech Dev Rev: 1.10.1	Page No.: 114/306
TD-LO28-DR-2006			2		

Rule number	Description	Operation	Design Value	Unit
	DRC ignore the violation poly without CT.			
SAB.13	AA_DMY extension outside of SAB	\geq	0.12	um

SMIC CONFIDENTIAL

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 115/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 116/306
---------------------------	---	------------	----------------------	-------------------

7.2.16 Strained Source/Drain (PSR) design rules

Rule Number	Description	Operation	Design Value	Unit
PSR.1	Strained source/drain open ratio. DRC checking method: (((((((((SP AND NW) NOT ((((((DG OR TG) OR RESAA) OR RESNW) OR BIPOLA) OR DSTR) OR RESP1) OR VARMOS) OR INST)) AND (((SP AND NW) AND AA) sizing up 0.065um)) NOT PSRBL) sizing up 0.079um) sizing down 0.079um) sizing down 0.089um) sizing up 0.089um)) OR ((SP AND NW) AND INST)) OR PSRDUM) AND (AA OR AA_DMY)) NOT (GT OR POLY_DMY)) full chip density.	\geq	5.8%	

Notes:

To avoid low strained source/drain open ratio, designer should:

1. Please control the device amount or area for decoupling capacitor and varactor in chip design.
2. Please avoid to draw SN layer on large STI region which excludes poly resistor device.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 117/306
---------------------------	---	------------	----------------------	-------------------

7.2.17 CT: Contact design rules

Below rules are only used for square CT region.

Rule number	Description	Operation	Design Value	Unit
CT.1	Fixed contact size (square shape) DRC don't check share CT in SRAM, CT in EFUSE region and OCOVL.	=	0.04	um
CT.2a	Space between contacts. DRC doesn't check INST region	\geq	0.07	um
CT.2b	Space between CT and its neighboring CT (T). The definition of neighboring CT (T) : 1.CT (T) is in a CT group 2.The number of this CT group is ≥ 4 , there are at least 3 CTs neighboring to CT (T) 3.The space between CT (T) to other CTs in this group $< 0.09\text{um}$ DRC doesn't check INST, EFUSE region.	\geq	0.085	um
CT.2c	Space between CT on different nets. DRC doesn't check INST region.	\geq	0.08	um
CT.3	Space between AA and contact on poly. DRC doesn't check INST region.	\geq	0.035	um
CT.4a	Space between GATE and contact on AA for core device when channel length of core device $\leq 0.09\text{um}$. DRC doesn't check INST region.	\geq	0.03	um
CT.4b	Space between GATE and contact on AA for core device when channel length of core device $> 0.09\text{um}$.	\geq	0.04	um
CT.4c	Space between GATE and contact on AA for IO device.	\geq	0.07	um
CT.4d	Space between (poly or GTDMP or GTDOP) and CT on AA in vertical direction. DRC doesn't check INST region.	\geq	0.04	um
CT.5	Space between (CT AND INST) and (CT NOT INST)	\geq	0.2	um
CT.6	CT must be fully covered by AA. AA Enclosure by AA must			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 118/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	follow (CT.6a and CT.6b) or CT.6d ^[R] or CT.6d ^[R] as below. DRC doesn't check OCOVL region.			
CT.6a	Enclosure by AA for a CT landed on AA. DRC doesn't check INST and OCOVL region	≥	0.005	um
CT.6a ^[R]	Enclosure by AA for a CT landed on AA when channel length>0.09um to avoid high RC. DRC doesn't check INST and OCOVL region	≥	0.015	um
CT.6b	Enclosure by AA for a CT landed on AA when enclosure by AA on either perpendicular direction ≥0.005um. DRC doesn't check INST and OCOVL region	≥	0.03	um
CT.6b ^[R]	Enclosure by AA for a CT landed on AA when enclosure by AA on either perpendicular direction ≥ 0.005um to avoid high RC. DRC doesn't check INST and OCOVL region	≥	0.04	um
CT.6c	Enclosure by AA, when 1. AA width W1: 0.07um ≤ W1≤ 0.09um, 2. Space between AA and ((AA OR Aadmp) OR Aadop) is 0.07um, and width of ((AA OR Aadmp) OR Aadop) is 0.05um DRC doesn't check INST and OCOVL region.	≥	0.01	um
CT.7	CT must be fully covered by ((poly sizing up 0.005um) NOT P2). Enclosure by (poly or GTDMP or GTDOP) must follow (CT.7a and CT.7c) or (CT.7b and CT.7d) or (CT.7b and CT.7e) or CT.7f or (CT.7g and CT.7h) as below.			
CT.7a	Enclosure by (poly or GTDMP or GTDOP) when (poly or GTDMP or GTDOP) width <0.04um.	≥	-0.005	um
CT.7b	Enclosure by (poly or GTDMP or GTDOP) when (poly or GTDMP or GTDOP) width ≥0.04um. This rule doesn't check poly jog region. The poly jog is defined as the rectangular with size 0.06 *0.08um.	≥	0	um
CT.7c	Enclosure by (poly or GTDMP or GTDOP) when enclosure by (poly or GTDMP or GTDOP) on either perpendicular direction ≥-0.005um, and (poly or GTDMP or GTDOP) width <0.04um.	≥	0.05	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 119/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
CT.7d	Enclosure by (poly or GTDMP or GTDOP) when enclosure by (poly or GTDMP or GTDOP) on either perpendicular direction $\geq 0\text{um}$, and (poly or GTDMP or GTDOP) width $\geq 0.04\text{um}$ and $\leq 0.09\text{um}$. DRC doesn't check EFUSE region.	\geq	0.05	um
CT.7e	Enclosure by (poly or GTDMP or GTDOP) when enclosure by (poly or GTDMP or GTDOP) on either perpendicular direction $\geq 0\text{um}$, and (poly or GTDMP or GTDOP) width $>0.09\text{um}$.	\geq	0.02	um
CT.7e ^[R]	Recommended enclosure by poly when enclosure by poly on either perpendicular direction $\geq 0\text{um}$, and poly width $>0.09\text{um}$.	\geq	0.03	um
CT.7f	Enclosure by poly in the four sides when the poly width $>0.09\text{um}$	\geq	0.015	um
CT. 7g	Enclosure by poly jog along poly width direction The poly jog is defined as the rectangular with size $0.06 * 0.08\text{um}$	\geq	-0.005	um
CT.7h	Enclosure by poly jog along poly length direction The poly jog is defined as the rectangular with size $0.06 * 0.08\text{um}$	\geq	0.02	um
CT.8a	CT enclosure by AA in IO region, when space between AA and poly $< 0.05\text{um}$ and the parallel run length between CT and S1 $>0\text{um}$	\geq	0.015	um
CT.8b	CT enclosure by poly in IO region with the parallel run length $>0\text{um}$, when space between poly and AA $< 0.05\text{um}$ and the parallel run length between CT and S1 $>0\text{um}$	\geq	0.015	um
CT.9	CT must be fully covered by M1. Enclosure by M1 must follow (CT.9a and CT.9b) or CT.9c, and CT.9d, and CT.9f as below. DRC doesn't check OCCD region.			
CT.9a	Enclosure by M1. DRC doesn't check INST, OCOVL and OCCD region.	\geq	0	um
CT.9b	Enclosure by M1 when enclosure by M1 on either perpendicular direction $\geq 0\text{um}$ and $< 0.015\text{um}$.	\geq	0.02	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 120/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check INST, OCOVL and OCCD region.			
CT.9c	Enclosure by M1 in the four sides. DRC doesn't check INST, OCOVL and OCCD region.	\geq	0.015	um
CT.9d	Enclosure by M1 in adjacent S1 side (M1 width \geq 0.08um, M1 and M1 space S1 < 0.06um, and the parallel run length > 0.18um) This rule doesn't check two CTs (when CTs space < 0.08um).	\geq	0.015	um
CT.9f	Enclosure by M1 (metal width > 0.7um) in the four sides. DRC violation is allowed if only one CT meets this rule for the redundant CTs pattern.	\geq	0.03	um
CT.9g	Enclosure by M1 when enclosure by M1 on either perpendicular direction \geq 0, and M1 area < 0.014um ² . DRC doesn't check INST region.	\geq	0.03	um
CT.9 ^[R]	CT must be fully covered by M1. Enclosure by M1 must follow (CT.9a ^[R] and CT.9b ^[R]) or CT.9c ^[R] , and CT.9d ^[R] , and CT.9e ^[R] as below.			
CT.9a ^[R]	Recommended enclosure by M1. DRC doesn't check INST region.	\geq	0.01	um
CT.9b ^[R]	Recommended enclosure by M1 when enclosure by M1 on either perpendicular direction \geq 0.01um and < 0.02um. DRC doesn't check INST region.	\geq	0.035	um
CT.9c ^[R]	Recommended enclosure by M1 in the four sides. DRC doesn't check INST region.	\geq	0.02	um
CT.9d ^[R]	Recommended enclosure by M1(M1 width \geq 0.08um, M1 and M1 space < 0.06um) This rule doesn't check two CTs (when CTs space < 0.08um)	\geq	0.015	um
CT.9e ^[R]	Enclosure by M1 (metal width \geq 0.33um and \leq 0.7um) when enclosure by M1 on either perpendicular direction \geq 0.015um. DRC violation is allowed if only one CT meets this rule for the redundant CTs pattern.	\geq	0.02	um
CT.10 ^[R]	Recommended inner vertex AA enclosure of CT. This rule doesn't check the N+/P+ pickup regions	\geq	0.04	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

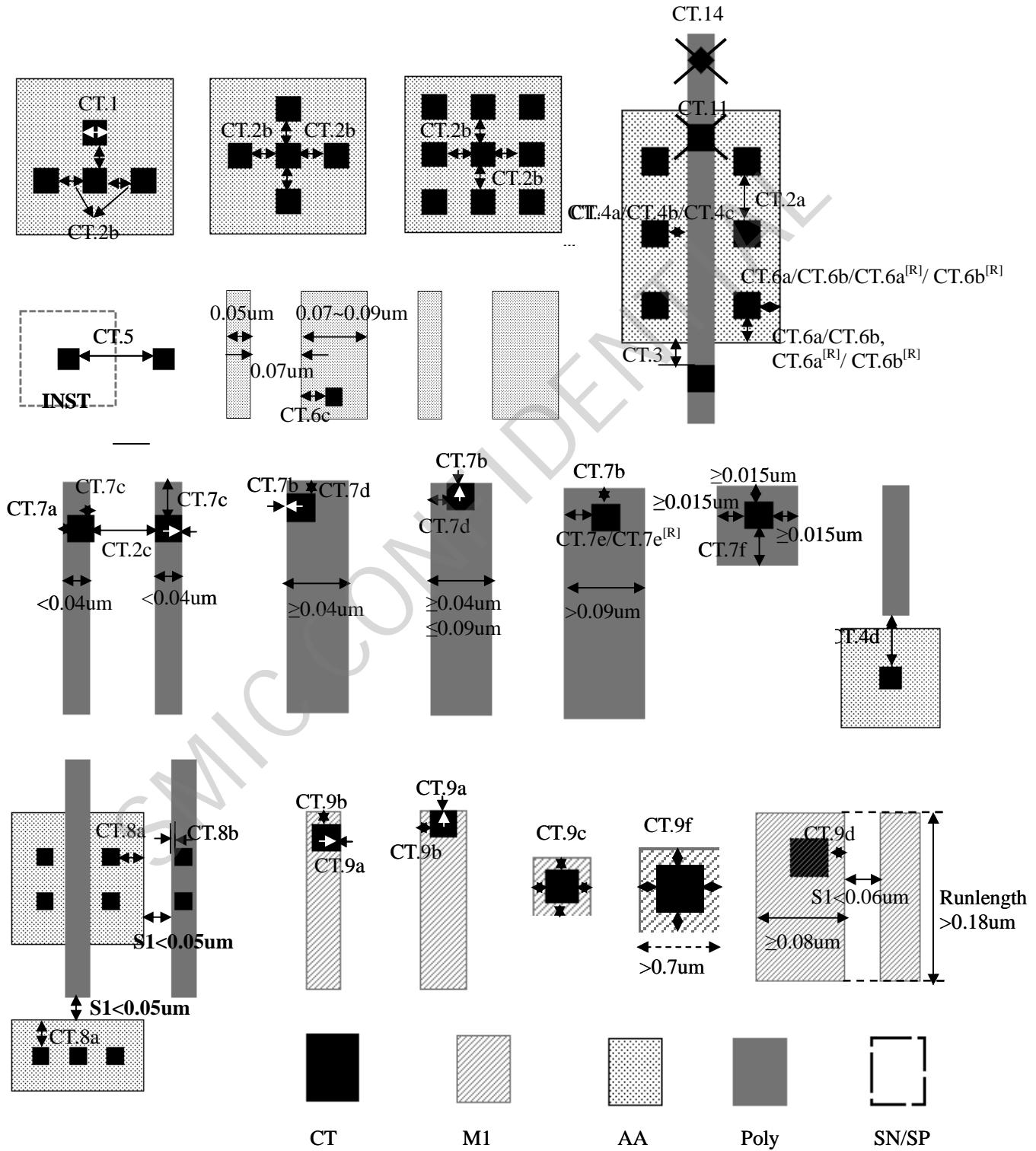


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 121/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
CT.11	CT is not allowed to land on GATE. DRC doesn't check INDMY and INST region.			
CT.12	CT is not allowed to land on SAB, and can't land on STI without Poly. This rule isn't applicable for SRAM, INDMY and OCOVL region.			
CT.13	CT enclosed by butted SN/SP edge on AA	\geq	0.035	um
CT.14	45-degree rotated CT is not allowed.			
CT.15	CT can't overlap with SN/SP boundary (for CTs on AA).			
CT.16^{[NC][R]}	Recommend put more CTs avoid high resistance wherever layout allows.			
CT.17	It's not allowed CT overlap with AA/poly silicided resistor. Pls refer the definition of AA/poly silicided resistor in AA/poly resistor section.			
CT.18	It's not allowed CT connects to $\geq 5V$ net outside DG/TG region.			

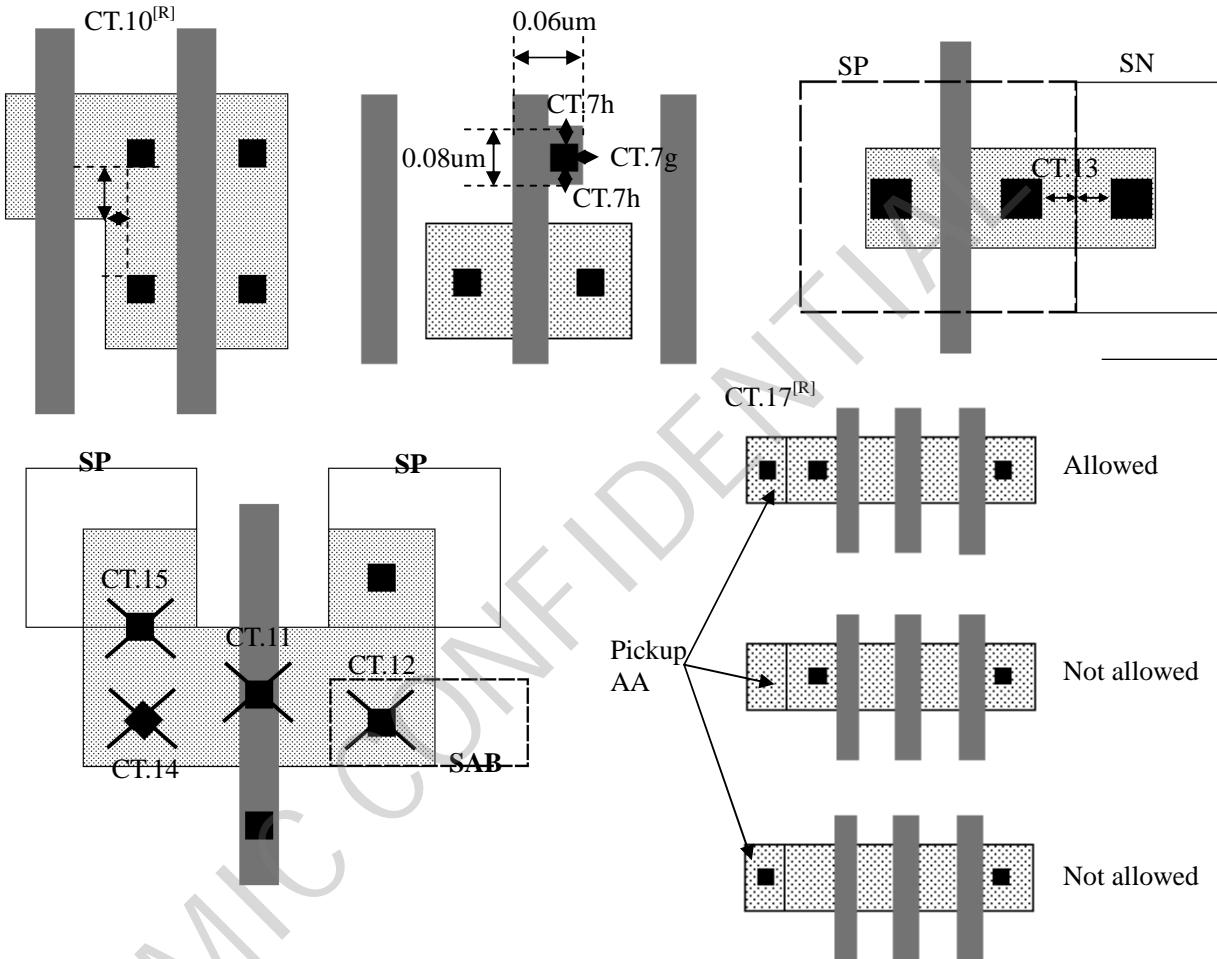
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	28nm Logic Low Power (Poly/SION)	Doc. Rev.:	Tech Dev	Page No.:
TD-LO28-DR-2006	Title: 1.05V/1.8V/2.5V Design Rules	2	Rev: 1.10.1	122/306



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 123/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 124/306
---------------------------	---	------------	----------------------	-------------------

7.2.18 Metal 1 design rules

Rule number	Description	Operation	Design Value	Unit
M1.1	M1 width	\geq	0.05	um
		\leq	4.5	um
M1.2a	Width of 45-degree M1. The vertex of 45-degree pattern should be on 0.005um grid. DRC doesn't check INDMY region for the vertex of 45-degree pattern grid.	\geq	0.17	um
M1.2b	Length of 45-degree M1	\geq	0.5	um
M1.3	M1 edge length when the adjacent edge $< 0.05\text{um}$, and these two edges formed by 3 consecutive 270 degree inner vertex-90 degree outer vertex-270 degree inner vertex. DRC doesn't flag if there is M1 in the region which is formed by 0.16um extension from these two edges and the 90-degree outer vertex. DRC doesn't check INST region.	\geq	0.065	um
M1.4^[R]	Recommended M1 width, when 1. Space between M1 and two side-wall M1 is 0.05 um, with parallel run length $> 0.16\text{um}$; 2. CT/V1 enclosure by this M1: $0.02\text{um} \leq E1 \leq 0.03\text{um}$; 3. Space between this M1 line end and M1: $0.07\text{um} \leq S \leq 0.08\text{um}$.	\geq	0.06	um
M1.5a	Space between two M1s. DRC doesn't check INST region.	\geq	0.05	um
M1.5b	Space between two M1s when one or both M1 widths are $> 0.1\text{um}$, and parallel run length of two M1s is $> 0.22\text{um}$.	\geq	0.06	um
M1.5c	Space between two M1s when one or both M1 widths are $> 0.18\text{um}$, and parallel run length of two M1s is $> 0.22\text{um}$.	\geq	0.1	um
M1.5d	Space between two M1s when one or both M1 widths are $> 0.47\text{um}$, and parallel run length of two M1s is $> 0.47\text{um}$.	\geq	0.13	um
M1.5e	Space between two M1s when one or both M1 widths are $> 0.63\text{um}$, and parallel run length of two M1s	\geq	0.15	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 125/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	is >0.63um.			
M1.5f	Space between two M1s when one or both M1 width are >1.5um, and parallel run length of two M1s is >1.5um.	\geq	0.5	um
M1.6a	Space between M1 and M1 line end, and the parallel run length is >-0.025um. M1 line-end definition: M1 edge with length < 0.07um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.05um. DRC doesn't check INST region.	\geq	0.06	um
M1.6b	Space between M1 and dense M1 line-end, when parallel run length >-0.025um. 1. M1 line-end definition: M1 edge with length < 0.07um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.05um; 2. Dense M1 line end definition: (W+S) < 0.12um, other metal must be in the region R, L1 and L2 is the extension from metal line end, L1 < 0.025um, L2 < 0.07um, S should be the space between separate metal. DRC doesn't check INST region.	\geq	0.07	um
M1.7^[R]	Space between (M1 or dummy M1). DRC check maximum width of (NOT (M1 or dummy M1)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um, LOGO and INDMY.	\leq	4.5	um
M1.8	(Purposly blank)			
M1.9	Space between 45-degree M1 and M1	\geq	0.17	um
M1.10	Space between two M1s when one or both of M1 connects to 3.3V net	\geq	0.07	um
M1.11a	Space between M1 line and line when one or both of M1 connects to 5V net, parallel run length >-0.11um. M1 line definition: M1 edge \geq 0.08um.	\geq	0.11	um
M1.11b	Space between M1 line and line end when one or both of M1 connects to 5V net, parallel run length >-0.14um. M1 line end definition: M1 edge < 0.08um between two	\geq	0.14	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 126/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	outer vertex. M1 line definition: NOT M1 line end.			
M1.11c	Space between M1 line end and line end when one or both of M1 connects to 5V net, parallel run length >-0.12um. M1 line end definition: M1 edge < 0.08um between two outer vertex.	\geq	0.12	um
M1.12	Space between M1 and neighboring V1 when either V1 or M1 connects to 1.5V net. DRC doesn't check M1 which the neighboring V1 is landed	\geq	0.06	um
M1.13	Space between M1 and neighboring V1 when either V1 or M1 connects to 1.8V and 2.5V net. DRC doesn't check M1 which the neighboring V1 is landed	\geq	0.08	um
M1.14	Space between M1 and neighboring V1 when either V1 or M1 connects to 3.3V net. DRC doesn't check M1 which the neighboring V1 is landed	\geq	0.087	um
M1.15	Space between M1 and neighboring V1 when either V1 or M1 connects to 5V net. DRC doesn't check M1 which the neighboring V1 is landed	\geq	0.165	um
M1.16	(Purposely blank)			
M1.17a	M1 area. DRC doesn't check INST region.	$>$	0.0115	um ²
M1.17a ^[R]	Recommended M1 area	\geq	0.023	um ²
M1.17b	M1 area when all of M1 edge length < 0.2um, any M1 edge length \geq 0.13um This rule doesn't check the patterns which can fill 0.05um * 0.2um rectangular pattern and doesn't check INST region.	\geq	0.014	um ²
M1.17c	M1 area when all of M1 edge length < 0.13um. This rule doesn't check the patterns which can fill 0.05um*0.13um rectangular pattern, and doesn't check INST region.	\geq	0.04	um ²
M1.18	Dielectric area enclosed by M1	\geq	0.2	um ²

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 127/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
M1.19	M1 density (including dummy). Density check window size: 125um*125um, step size: 62.5um.	\geq	10%	
		\leq	85%	
M1.20	The density difference between any two neighboring checking windows (window 200*200, stepping 200um). DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	\leq	50%	
M1.21^[R]	M1 density (including dummy) in DUMB/M1DUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMB/M1DUB width is >5um and <125um, where density ratio= M1 area/(DUMB/M1DUB) area.	\geq	10%	
		\leq	85%	
M1.22	M1 density (including dummy).Density check window size: 80um*80um, step size 40um DRC don't check: 1. Chip corner triangle region(NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1. DRC only check the region with width of (checking window NOT above excluding region) \geq 40um	\geq	1%.	
M1.23	Maximum M1 area of merged low density windows must follow item (1) and (2). The definition of low density window: window size 10um*10um, step size: 5um, density <1% (1) Maximum area of merged low density window \leq 6000um ² , except merged low density windows width \leq 30um. (2) Maximum area of merged low density window \leq 16000um ² . DRC don't check: 1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1. DRC only check the region with width of (checking window NOT above excluding region) \geq 5um			
M1.24^[NC]	M1 line-end must be rectangular.			
M1.25	Space of metal space segments with S2 < 0.08 and L2 \leq 0.22um.	\geq	0.3	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 128/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	Metal space segments definition: 1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.25um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.25a	Width (S2) of metal space segments with L2 > 0.22um Metal space segments definition: 1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.25um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.1	um
M1.25b	Width (S2) of metal space segments with L2 ≤ 0.22um Metal space segments definition: 1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.25um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.06	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 129/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	perpendicular with L1 direction.			
M1.25c	Space of metal space segments with $S2 < 0.1$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ ($W1$) and the parallel run length $> 0.3\mu m$ ($L1$) in metal space $< 0.19\mu m$ ($S1$) region; 2). metal space segments within metal space ($S1$) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region ($S1$); 3). metal space segments at least abut one metal with width $> 0.25\mu m$ ($W1$); 4). $L2$ is the width of metal space segments which is parallel with L1 direction; 5). $S2$ is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
M1.26	Space of metal space segments with $S2 < 0.13$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.47\mu m$ ($W1$) and the parallel run length $> 0.5\mu m$ ($L1$) in metal space $< 0.32\mu m$ ($S1$) region; 2). metal space segments within metal space ($S1$) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region ($S1$); 3). metal space segments at least abut one metal with width $> 0.47\mu m$ ($W1$); 4). $L2$ is the width of metal space segments which is parallel with L1 direction; 5). $S2$ is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
M1.26a	Width ($S2$) of metal space segments with $L2 > 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.47\mu m$ ($W1$) and the parallel run length $> 0.5\mu m$ ($L1$) in metal space $< 0.32\mu m$ ($S1$) region; 2). metal space segments within metal space ($S1$) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region ($S1$);	\geq	0.13	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 130/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	3). metal space segments at least abut one metal with width > 0.47um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.26b	Width (S2) of metal space segments with $L2 \leq 0.22\text{um}$ Metal space segments definition: 1). at least one metal line width > 0.47um (W1) and the parallel run length > 0.5um (L1) in metal space < 0.32um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.47um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
M1.27	Space of metal space segments with $S2 < 0.15$ and $L2 \leq 0.22\text{um}$. Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
M1.27a	Width (S2) of metal space segments with $L2 > 0.22\text{um}$ Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region;	\geq	0.15	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 131/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.27b	Width (S2) of metal space segments with $L2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
M1.28	Space of metal space segments with $S2 < 0.3$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width > 1.5um (W1) and the parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
M1.28a	Width (S2) of metal space segments with $L2 > 0.22\mu m$	\geq	0.3	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 132/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	Metal space segments definition: 1). at least one metal line width > 1.5um (W1) and the parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.28b	Width (S2) of metal space segments with $L2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width > 1.5um (W1) and the parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
M1.29	It is not allowed for M1 zone, and M1 Zone definition as below: 1), W1, W3 and W5 are same polygons, W2 and W4 are same polygons; 2), Width of M1 (W2,W3,W4) = 0.05um; 3), Space of M1 (S1,S2,S3,S4) = 0.05um; 4), Space of M1 line-end to opposite M1(S5) < 0.08um; 5), parallel run length of 5 M1 lines L1 <= 0.4um.			
M1.30	It's not allowed DUMBM(GDS No: 90;0) layer in design. DRC doesn't check (DUMBM INTERACT RFDEV) region.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	Tech Dev Rev: 1.10.1	Page No.: 133/306
TD-LO28-DR-2006			2		

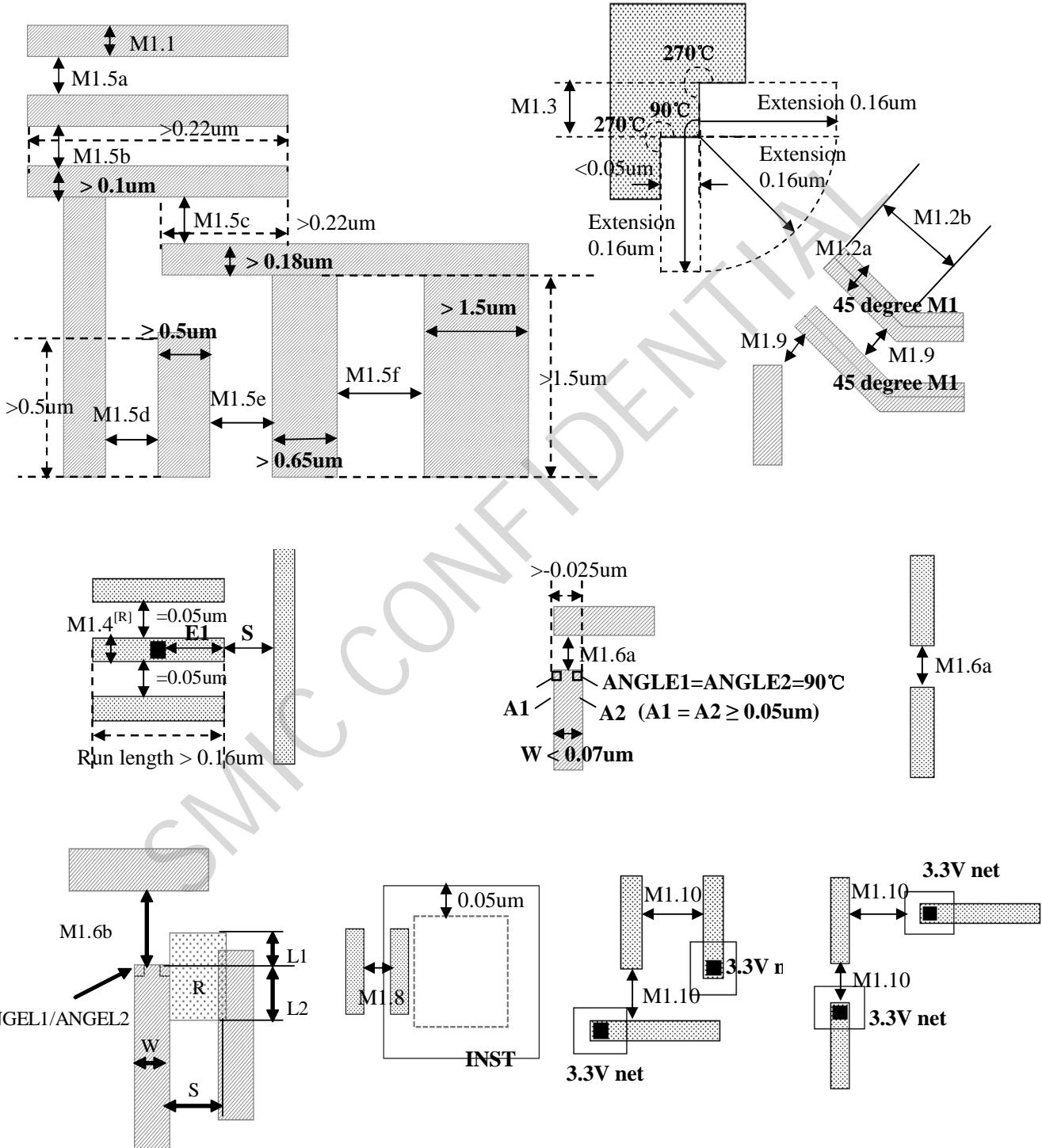
Note:

1. CT and via enclosure by M1 should be as large as the layout allows.
2. It is recommended that the lengths of metal lines are orthogonal to the lengths of metal lines on neighboring layers.
3. The marking layers have priority, higher voltage marking layer have higher priority. For example, the M1 will be identified as 2.5V M1 when there are two marking layer as M1V18 and M1V25.

SMIC CONFIDENTIAL

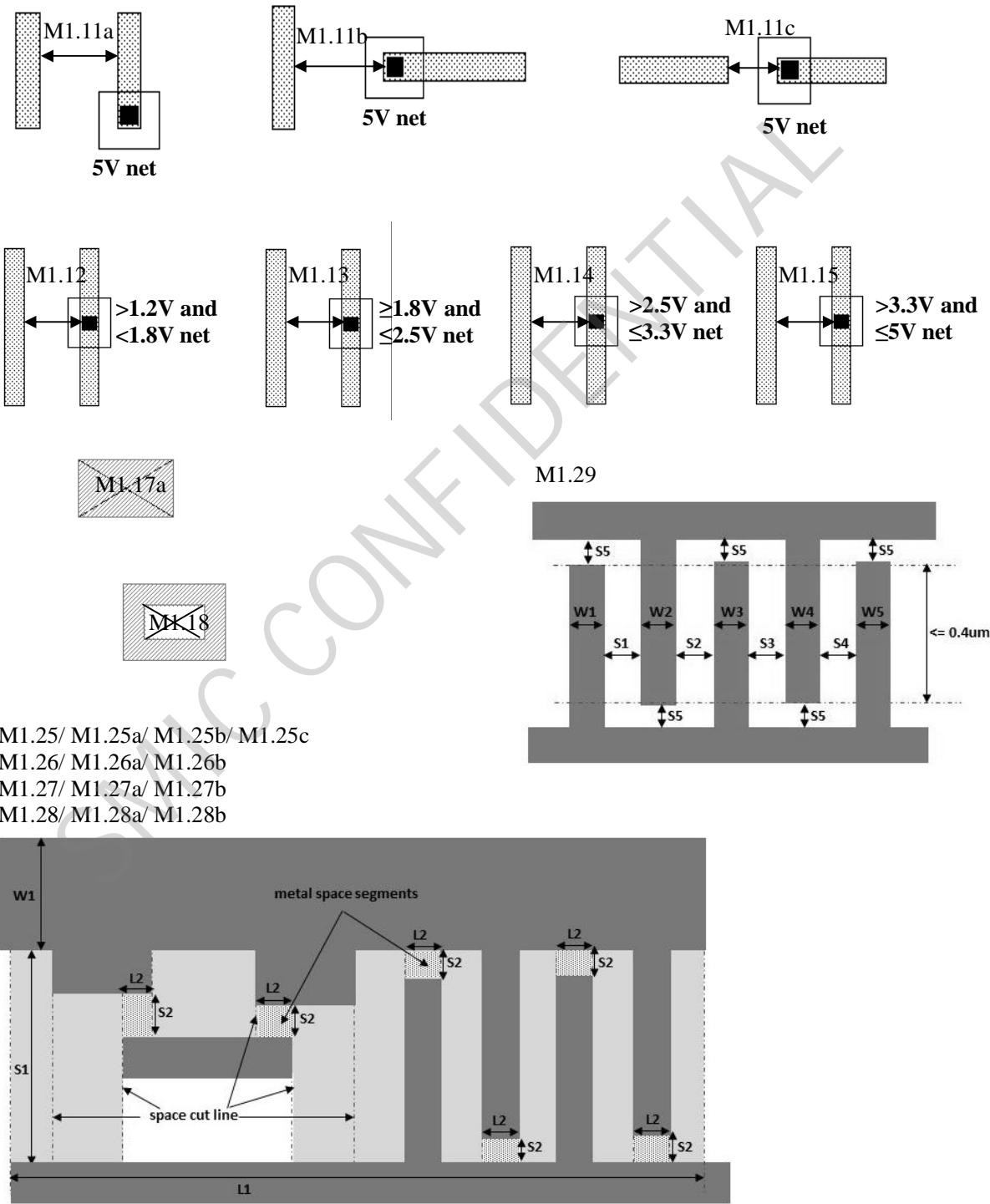
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 134/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 135/306
---------------------------	---	-------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 136/306
---------------------------	---	------------	----------------------	-------------------

7.2.19 1x Mn(n=2-8): 1x Metal design rules

Rule number	Description	Operation	Design Value	Unit
1xMn.1	1xMn width. DRC doesn't check INST region. For maximum rule, DRC doesn't check DUPMK1 region.	\geq	0.05	um
		\leq	4.5	um
1xMn.2a	Width of 45-degree 1xMn	\geq	0.17	um
1xMn.2b	Length of 45-degree 1xMn	\geq	0.5	um
1xMn.3	1xMn edge length when the adjacent edge < 0.05um, and these two edges formed by 3 consecutive 270 degree inner vertex-90 degree outer vertex-270 degree inner vertex. DRC doesn't flag if there is 1xMn in the region which is formed by 0.16um extension from these two edges and the 90-degree outer vertex.	\geq	0.065	um
1xMn.4a	Space between two 1xMns.	\geq	0.05	um
1xMn.4b	Space between two 1xMns when one or both 1xMn widths are >0.09um, and parallel run length of two 1xMns is >0.22um.	\geq	0.06	um
1xMn.4c	Space between two 1xMns when one or both 1xMn widths are >0.13um, and parallel run length of two 1xMns is >0.22um.	\geq	0.08	um
1xMn.4d	Space between two 1xMns when one or both 1xMn widths are >0.16um, and parallel run length of two 1xMns is >0.22um.	\geq	0.1	um
1xMn.4e	Space between two 1xMns when one or both 1xMn widths are >0.47um, and parallel run length of two 1xMns is >0.47um.	\geq	0.13	um
1xMn.4f	Space between two 1xMns when one or both 1xMns width are >0.63um, and parallel run length of two 1xMns is >0.63um.	\geq	0.15	um
1xMn.4g	Space between two 1xMns when one or both 1xMns width are >1.5um, and parallel run length of two 1xMns is >1.5um.	\geq	0.5	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 137/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
1xMn.5a	Space between 1xMn end to 1xMn, and the parallel run length is >-0.025um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 ≥ 0.05um. DRC doesn't check INST region.	≥	0.07	um
1xMn.5b	Space between 1xMn line end and end, and the parallel run length is >-0.025um. 1xMn line definition: 1xMn edge ≥ 0.07um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 ≥ 0.05um. DRC doesn't check INST region.	≥	0.08	um
1xMn.5c	Space between 1xMn line and dense 1xMn line-end with 1xVn-1/or 1xRVn-1(E ≤ 0.05um) (the parallel run length >-0.025um). 1xMn line definition: 1xMn edge ≥ 0.07um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 ≥ 0.05um Dense 1xMn line end definition: (W+S) <0.115um, other metal must be in the region R, L1 and L2 is the extension from metal line end, L1< 0.025um, L2 <0.07um, S should be the space between separate metal.	≥	0.08	um
1xMn.5d	Space between 1xMn line and 1xVn-1 or 1xRVn-1 (dense 1xMn line-end enclosure of 1xVn-1 or 1xRVn-1 E≤ 0.05um), the parallel run length of 1xMn line and dense 1xMn line-end >-0.025um. 1xMn line definition: 1xMn edge ≥ 0.07um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 ≥ 0.05um Dense 1xMn line end definition: (W+S) <0.115um, other metal must be in the region R, L1 and L2 is the extension from metal line end, L1< 0.025um, L2 <0.07um, S should be the space between separate metal.	≥	0.13	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 138/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
1xMn.6^[R]	Space between (1xMn or dummy 1xMn). DRC check maximum width of (NOT (1xMn or dummy 1xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um , LOGO and INDMY.	\leq	4.5	um
1xMn.7	Space between 45-degree 1xMn and 1xMn	\geq	0.17	um
1xMn.8	Space between two 1xMns when one or both of 1xMn connects to 3.3V net	\geq	0.07	um
1xMn.9a	Space between 1xMns line and line when one or both of 1xMn connects to 5V net, the parallel run length > -0.11um. 1xMns line definition: 1xMns edge with length \geq 0.08um	\geq	0.11	um
1xMn.9b	Space between 1xMns line and line end when one or both of 1xMn connects to 5V net, the parallel run length > -0.14um. 1xMns line-end definition: 1xMns edge with length < 0.08um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.05um. 1xMns line definition: 1xMns edge with length \geq 0.08um	\geq	0.14	um
1xMn.9c	Space between 1xMns line ends when one or both of 1xMn connects to 5V net, the parallel run length > -0.12um. 1xMns line-end definition: 1xMns edge with length < 0.08um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.05um.	\geq	0.12	um
1xMn.10	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 1.5V net. DRC doesn't check 1xMn which the neighboring (Vn or Vn-1) is landed	\geq	0.06	um
1xMn.11	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 1.8V and 2.5V net. DRC doesn't check 1xMn which the neighboring (Vn or Vn-1) is landed	\geq	0.08	um
1xMn.12	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 3.3V net.	\geq	0.087	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 139/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check 1xMn which the neighboring (Vn or Vn-1) is landed			
1xMn.13	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 5V net. DRC doesn't check 1xMn which the neighboring (Vn or Vn-1) is landed	\geq	0.165	um
1xMn.14	(Purposely blank)			
1xMn.15a	1xMn area (except M2) DRC doesn't check OCOVL region.	\geq	0.017	um ²
1xMn.15a^[R]	Recommended 1xMn area. DRC doesn't check INST region.	\geq	0.023	um ²
1xMn.15b	1xMn area when all of 1xMn edge length < 0.13um. DRC doesn't check INST, 2PSRAM and RFSRAM region, and this rule doesn't check the patterns which can fill 0.05um*0.13um rectangular pattern.	\geq	0.045	um ²
1xMn.16	M2 area. DRC doesn't check INST and OCOVL region.	\geq	0.014	um ²
1xMn.17	Dielectric area enclosed by 1xMn (um ²).	\geq	0.2	um ²
1xMn.18	1xMn density (including dummy). Density check window size: 125um*125um, step size: 62.5um.	\geq \leq	10% 85%	
1xMn.19	The density difference between any two neighboring checking windows (window 200*200, stepping 200um).	\leq	50%	
1xMn.20^[R]	1xMn density (including dummy) in DUMB/MnDUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMB/MnDUB width is >5um and <125um, where density ratio= 1xMn area/(DUMB/MnDUB) area.	\geq \leq	10% 85%	
1xMn.21	1xMn density (including dummy).Density check window size: 80um*80um, step size 40um	\geq	1%.	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 140/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC does't check: 1. Chip corner triangle region(NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1. DRC only check the region with width of (checking window NOT above excluding region) \geq 40um			
1xMn.22	Maximum 1x Mn area of merged low density windows must follow item (1) and (2). The definition of low density window: window size 10um*10um, step size: 5um, density <1% (1) Maximum area of merged low density window \leq 6000um ² , except merged low density windows width \leq 30um. (2) Maximum area of merged low density window \leq 16000um ² . DRC doesn't check: 1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1. DRC only check the region with width of (checking window NOT above excluding region) \geq 5um			
1xMn.23	It is not allowed to have local density $>$ 85% of all 3 consecutive metal (1xMn, 1xMn+1 and 1xMn+2) over any window size 60*60um (stepping size 30um). The metal layers include M1/1xMn and dummy metals. DRC doesn't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC, seal ring region.			
1xMn.24	It is not allowed to have local density $<$ 5% of all 3 consecutive metal (1xMn, 1xMn+1 and 1xMn+2) over any window 30*30um (stepping 15um).The metal layers include M1/1xMn and dummy metals. DRC does't check: 1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1 and INDMY. DRC only check the region with width of (checking window NOT above excluding region) \geq 15um			
1xMn.25 ^[NC]	1xMn line-end must be rectangular.			
1xMn.26	Space of metal space segments with S2 $<$ 0.08 and L2 \leq	\geq	0.3	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 141/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	<p>0.22um.</p> <p>Metal space segments definition:</p> <ol style="list-style-type: none">1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region;2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);3). metal space segments at least abut one metal with width > 0.25um (W1);4). L2 is the width of metal space segments which is parallel with L1 direction;5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.26a	<p>Width (S2) of metal space segments with L2 > 0.22um</p> <p>Metal space segments definition:</p> <ol style="list-style-type: none">1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region;2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);3). metal space segments at least abut one metal with width > 0.25um (W1);4). L2 is the width of metal space segments which is parallel with L1 direction;5). S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.1	um
1xMn.26b	<p>Width (S2) of metal space segments with L2 ≤ 0.22um</p> <p>Metal space segments definition:</p> <ol style="list-style-type: none">1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region;2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);3). metal space segments at least abut one metal with width > 0.25um (W1);4). L2 is the width of metal space segments which is parallel with L1 direction;	≥	0.06	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 142/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.26c	Space of metal space segments with $S2 < 0.1$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ (W1) and the parallel run length $> 0.3\mu m$ (L1) in metal space $< 0.19\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.25\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
1xMn.27	Space of metal space segments with $S2 < 0.13$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.47\mu m$ (W1) and the parallel run length $> 0.5\mu m$ (L1) in metal space $< 0.32\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.47\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
1xMn.27a	Width (S2) of metal space segments with $L2 > 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.47\mu m$ (W1) and the parallel run length $> 0.5\mu m$ (L1) in metal space $< 0.32\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space	\geq	0.13	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 143/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	region (S1); 3). metal space segments at least abut one metalwith width > 0.47um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.27b	Width (S2) of metal space segments with $L2 \leq 0.22\text{um}$ Metal space segments definition: 1). at least one metal line width > 0.47um (W1) and the parallel run length > 0.5um (L1) in metal space < 0.32um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metalwith width > 0.47um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
1xMn.28	Space of metal space segments with $S2 < 0.15$ and $L2 \leq 0.22\text{um}$. Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metalwith width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
1xMn.28a	Width (S2) of metal space segments with $L2 > 0.22\text{um}$ Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um	\geq	0.15	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 144/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	(S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.28b	Width (S2) of metal space segments with $L2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
1xMn.29	Space of metal space segments with $S2 < 0.3$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width > 1.5um (W1) and the parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 145/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
1xMn.29a	Width (S2) of metal space segments with $L2 > 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 1.5\mu m$ (W1) and the parallel run length $> 1.5\mu m$ (L1) in metal space $< 0.5\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 1.5\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
1xMn.29b	Width (S2) of metal space segments with $L2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 1.5\mu m$ (W1) and the parallel run length $> 1.5\mu m$ (L1) in metal space $< 0.5\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 1.5\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
1xMn.30	It is not allowed for 1xMn zone, and 1xMn Zone definition as below: 1), W1, W3 and W5 are same polygons, W2 and W4 are same polygons; 2), Width of 1xMn (W2,W3,W4) = $0.05\mu m$; 3), Space of 1xMn (S1,S2,S3,S4) = $0.05\mu m$; 4), Space of 1xMn line-end to opposite 1xMn (S5) $< 0.08\mu m$; 5), parallel run length of 5 1xMn lines L1 $\leq 0.4\mu m$.			

Note:

1. CT and via enclosure by 1X Mn should be as large as the layout allows.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 146/306
---------------------------	---	------------	----------------------	-------------------

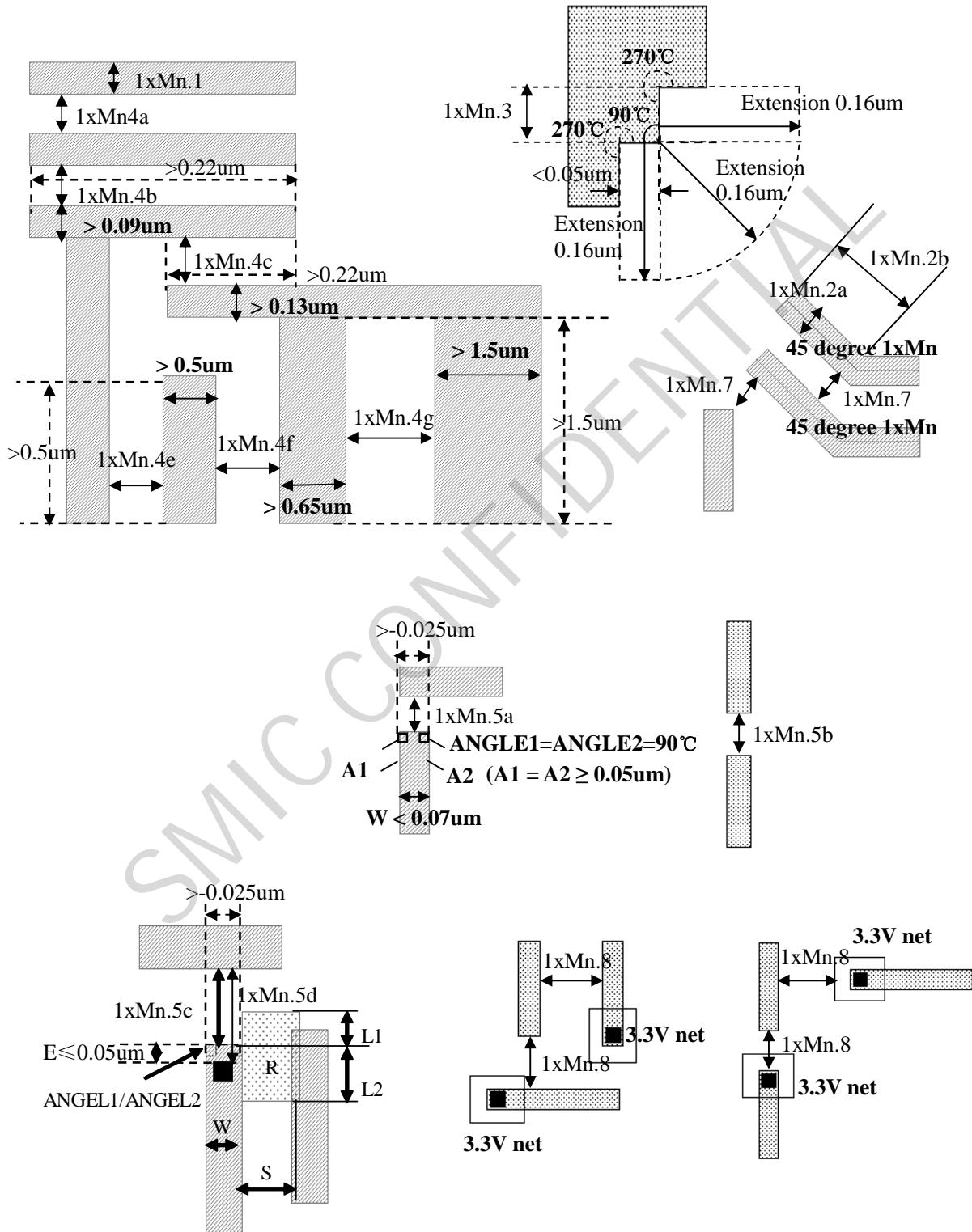
2. It is recommended that the lengths of metal lines are orthogonal to the lengths of metal lines on neighboring layers.

3. The marking layers have priority, higher voltage marking layer have higher priority. For example, the 1xMn will be identified as 2.5V 1xMn when there are two marking layer as MnV18 and MnV25 (n=2-8).

SMIC CONFIDENTIAL

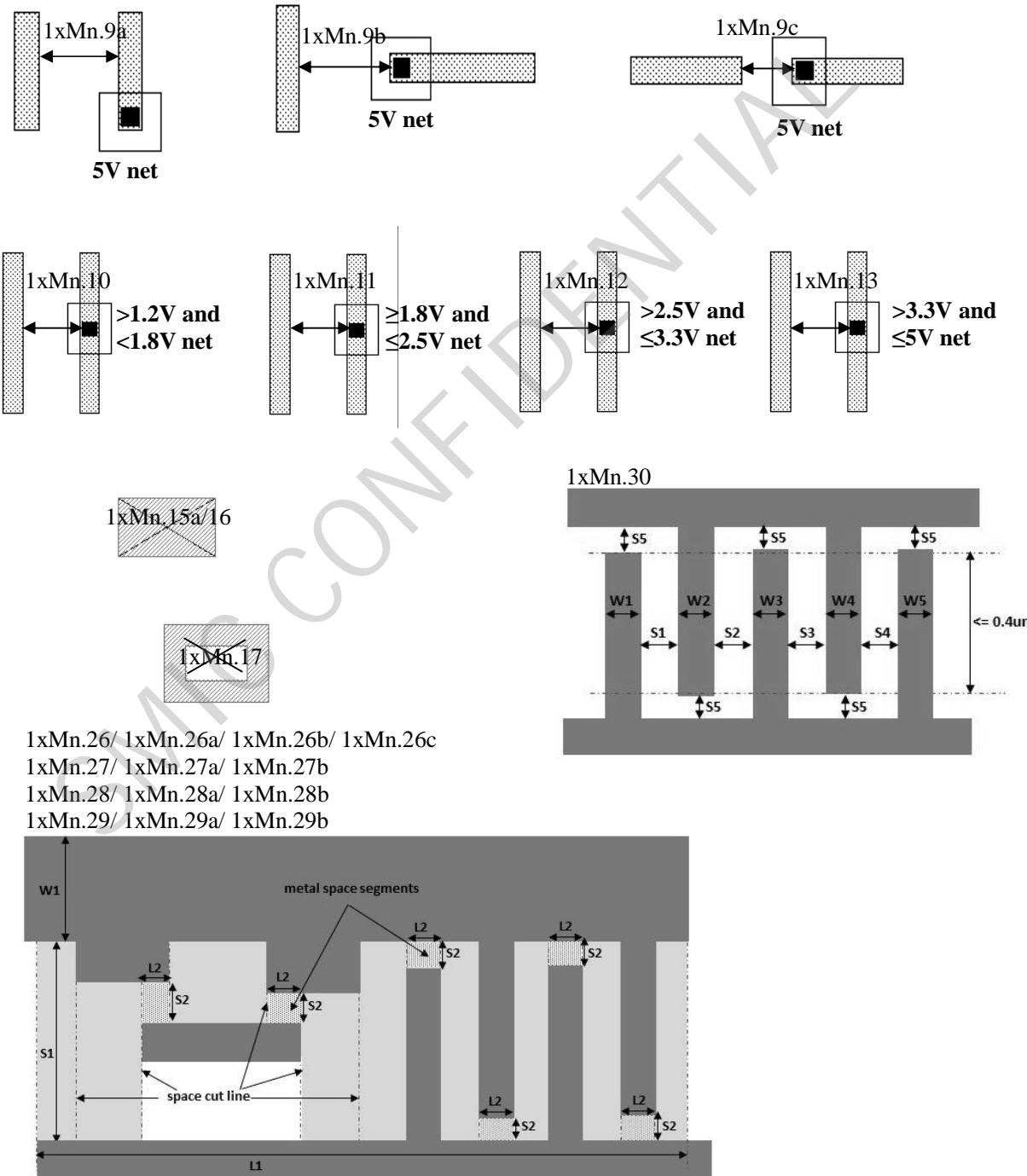
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 147/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 148/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 149/306
---------------------------	---	------------	----------------------	-------------------

7.2.20 1x Vn(n=1-7): 1X Via design rules

7.2.20.1 1x Vn: 1x square via design rules

Rule number	Description	Operation	Design Value	Unit
1xVn.1	Fixed 1x Vn size (square shape) DRC don't check rectangular 1xVn, MARKG (0.15um 1xVn ring in MARKG region).	=	0.05	um
1xVn.2a	Space between 1x Vns when the parallel run length $\leq -0.04\text{um}$.	\geq	0.07	um
1xVn.2b	Space between 1x Vns when the run length $>-0.04\text{um}$. DRC doesn't check INST and FUSEMK1 region.	\geq	0.08	um
1xVn.3	1x Vn must be fully covered by M1 or 1xMn. Enclosure by M1 or 1xMn must follow (1x Vn.3a and 1x Vn.3b) or 1x Vn.3d as below. DRC doesn't check INST region.			
1xVn.3a	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath 1x Vn.	\geq	0	um
1xVn.3b	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0\text{um}$ and $< 0.01\text{um}$ and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.03	um
1xVn.3c	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0.01\text{um}$ and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.025	um
1xVn.3d	Enclosure by M1 or 1xMn in four sides, and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.02	um
1xVn.3^[R]	1x Vn must be fully covered by M1 or 1xMn. Enclosure by 1xMn must follow (1x Vn.3a ^[R] and 1x Vn.3b ^[R]) or 1x Vn.3d ^[R] , and 1x Vn.3e ^[R] , and 1x Vn.3f ^[R] as below. DRC doesn't check INST region.			
1xVn.3a^[R]	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.01	um
1xVn.3b^[R]	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0.01\text{um}$ and $< 0.025\text{um}$ and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.05	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 150/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
1xVn.3d^[R]	Enclosure by M1 or 1xMn in four sides, and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.025	um
1xVn.3e^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width \geq 0.33um and \leq 0.7um, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.03	um
1xVn.3f^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width >0.7 um, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.04	um
1xVn.4	1x Vn must be fully covered by 1xMn+1. 1xMn+1 enclosure 1x Vn must follow (1x Vn.4a and 1x Vn.4b) or 1x Vn.4c or 1x Vn.4d as below. DRC doesn't check INST region.			
1xVn.4a	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0	um
1xVn.4b	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0um and $<$ 0.01um and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.03	um
1xVn.4c	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0.01um and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.025	um
1xVn.4d	Enclosure by 1xMn+1 in four sides and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.02	um
1xVn.4^[R]	1x Vn must be fully covered by 1xMn+1. 1xMn+1 enclosure 1x Vn must follow (1x Vn.4a ^[R] and 1x Vn.4b ^[R])or 1x Vn.4d ^[R] , and 1x Vn.4e ^[R] , and 1x Vn.4f ^[R] as below. DRC doesn't check INST region.			
1xVn.4a^[R]	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.01	um
1xVn.4b^[R]	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0.01um and $<$ 0.025um and	\geq	0.05	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 151/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	1xMn+1 is the metal layer directly above 1x Vn.			
1xVn.4d ^[R]	Enclosure by 1xMn+1 in four sides and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.025	um
1xVn.4e ^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width \geq 0.33um and \leq 0.7um, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.03	um
1xVn.4f ^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width $>$ 0.7um, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.04	um
1xVn.5a	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when 1. 1xMn width W: $0.05\text{um} < W \leq 0.055\text{um}$ 2. Space S1 $\leq 0.055\text{um}$, S2 $> 0.055\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check INST region.	\geq	0.005	um
1xVn.5b	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when 1. 1xMn width W: $0.055\text{um} < W \leq 0.07\text{um}$ 2. Space S1 $< 0.065\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check INST region.	\geq	0.005	um
1xVn.5c	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when 1. 1xMn width W: $0.07\text{um} < W \leq 0.16\text{um}$ 2. Space S1 $< 0.1\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check 1xVn: a) Two 1xVn with space $\leq 0.11\text{um}$ in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangular with space $\leq 0.11\text{um}$ in 1xMn and 1xMn+1 intersection region. DRC doesn't check INST region.	\geq	0.01	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 152/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
1xVn.5d	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when 1. 1xMn width W: $0.16\mu m < W \leq 4.5\mu m$ 2. Space S1 $< 0.13\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.015	um
1xVn.6a	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn+1 width W: $0.05\mu m < W \leq 0.055\mu m$ 2. Space S1 $\leq 0.055\mu m$, S2 $> 0.055\mu m$, the parallel run length $> 0.1\mu m$. DRC doesn't check INST region.	\geq	0.005	um
1xVn.6b	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn+1 width W: $0.055\mu m < W \leq 0.07\mu m$ 2. Space S1 $< 0.065\mu m$, the parallel run length $> 0.1\mu m$. DRC doesn't check INST region.	\geq	0.005	um
1xVn.6c	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn+1 width W: $0.07\mu m < W \leq 0.16\mu m$ 2. Space S1 $< 0.1\mu m$, the parallel run length $> 0.1\mu m$. DRC doesn't check 1xVn: a) Two 1xVn with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangular with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region. c) INST region.	\geq	0.01	um
1xVn.6d	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn +1 width W: $0.16\mu m < W \leq 4.5\mu m$ 2. Space S1 $< 0.13\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.015	um
1xVn.7	45-degree rotated 1x Vn is not allowed.			
1xVn.8	Single 1xVn is not allowed in "H-shape" 1xMn+1 when: 1. The 1xMn+1 has "H-shape" interact with two metal holes: both two metal holes length $\leq 6\mu m$ (L2) and two			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

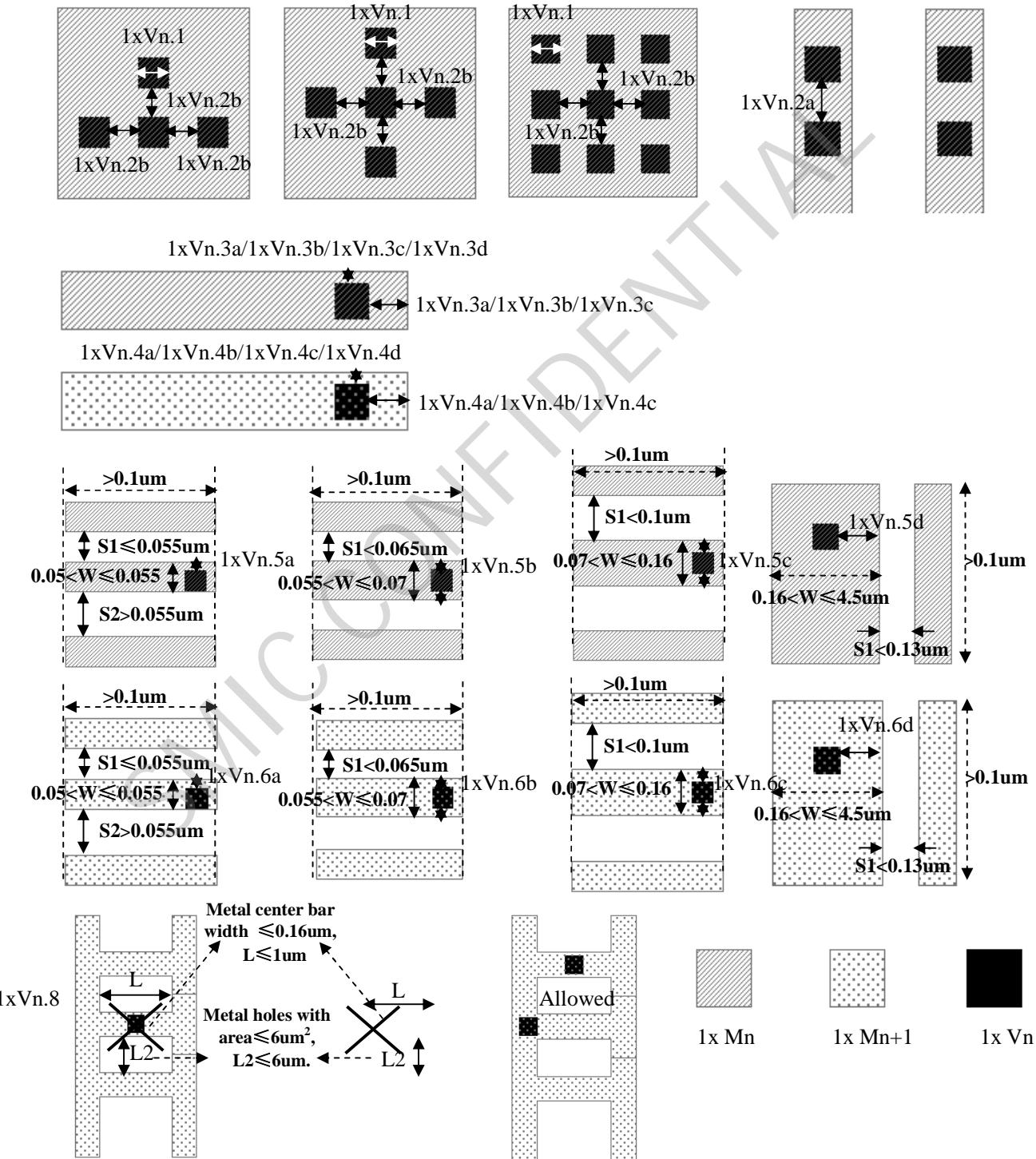


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 153/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	metal hole area \leq 6um ² . 2. The 1xVn overlaps on the center metal bar of this “H-shape” 1xMn+1. 3. The center metal bar length \leq 1um (L) and the metal bar width \leq 0.16um.			
1xVn. 9^[R]	Recommended consecutive stacked 1x Vn layer, which has only one 1x Vn for each 1x Vn layer to avoid high Rc. This rule doesn't check MARKS and DUPMK1 region.	\leq	4	
1xVn. 10^[R]	Recommended space between 1x Vn and 1xVn+1,where 1xVn and 1xVn+1 at different net and parallel run length > 0.02um	\geq	0.06	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 154/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 155/306
---------------------------	---	------------	----------------------	-------------------

7.2.20.2 1x RVn: 1x rectangular via design rules

Rule number	Description	Operation	Design Value	Unit
1xRVn.1a	Fixed width of rectangular 1x Vn DRC don't check square 1xVn, MARKG (0.15um 1xVn ring in MARKG region).	=	0.05	um
1xRVn.1b	Fixed length of rectangular 1x Vn DRC don't check square 1xVn and MARKG (0.15um 1xVn ring in MARKG region).	=	0.13	um
1xRVn.2a	Space between rectangular 1x Vns	\geq	0.08	um
1xRVn.2b	Space between rectangular 1x Vn and square Vn	\geq	0.075	um
1xRVn.2c	Space between rectangular 1x Vns when the run length $>0.04\text{um}$.	\geq	0.08	um
1xRVn.3	Rectangular 1x Vn must be fully covered by M1 or 1xMn. Enclosure by 1xMn must follow (1x RVn.3a and 1x RVn.3c) or 1x RVn.3b or 1x RVn.3d, or 1x RVn.3e ^[R] , or 1x RVn.3f ^[R] as below.			
1xRVn.3a	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.01	um
1xRVn.3b	Enclosure by M1 or 1xMn at rectangular 1xVn width side when enclosure by 1xMn (D1) at rectangular 1xVn length side is $\geq 0\text{um}$, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.04	um
1xRVn.3c	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0.01\text{um}$ and $< 0.02\text{um}$, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.03	um
1xRVn.3d	Enclosure by M1 or 1xMn when enclosure by 1xMn in four sides, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.02	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 156/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
1xRVn.3e ^[R]	Enclosure by M1 or 1x Mn (1x Mn width \geq 0.33um and \leq 0.7um), when enclosure by 1xMn on either perpendicular direction \geq 0.015um. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	\geq	0.03	um
1xRVn.3f ^[R]	Enclosure by M1 or 1x Mn (1x Mn width $>$ 0.7um), when enclosure by 1x Mn on either perpendicular direction \geq 0.03um. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	\geq	0.04	um
1xRVn.4	Rectangular 1x Vn must be fully covered by 1xMn+1. Enclosure by 1xMn+1 must follow (1x RVn.4a and 1x RVn.4c) or 1X RVn.4b or 1x RVn.4d, and 1x RVn.4e ^[R] , and 1x RVn.4f ^[R] as below.			
1xRVn.4a	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.01	um
1xRVn.4b	Enclosure by 1xMn+1 at rectangular 1xVn width side when enclosure by 1xMn+1 (D1) at rectangular 1xVn length side is \geq 0um, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.04	um
1xRVn.4c	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0.01um and $<$ 0.02um, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.03	um
1xRVn.4d	Enclosure by 1xMn+1 when enclosure by 1xMn+1 in four sides, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST region.	\geq	0.02	um
1xRVn.4e ^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width \geq 0.33um and \leq 0.7um), when enclosure by 1x Mn+1 on either perpendicular direction \geq 0.015um. 1x Mn+1 is the metal layer directly above rectangular 1x Vn.	\geq	0.03	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 157/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.			
1xRVn.4f ^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width >0.7um), when enclosure by 1x Mn+1 on either perpendicular direction $\geq 0.03\text{um}$. 1x Mn+1 is the metal layer directly above rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	\geq	0.04	um
1xRVn.5a	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangle 1x Vn., when 1. 1xMn width W: $0.05\text{um} < W \leq 0.055\text{um}$ 2. Space S1 $\leq 0.055\text{um}$, S2 $> 0.055\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check INST region.	\geq	0.005	um
1xRVn.5b	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangle 1x Vn., when 1. 1xMn width W: $0.055\text{um} < W \leq 0.07\text{um}$ 2. Space S1 $< 0.065\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check INST region.	\geq	0.005	um
1xRVn.5c	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangular 1x Vn., when 1. 1xMn width W: $0.07\text{um} < W \leq 0.16\text{um}$ 2. Space S1 $< 0.1\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check 1xRVn: a) Two rectangular 1x Vns with space $\leq 0.11\text{um}$ in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangular with space $\leq 0.11\text{um}$ in 1xMn and 1xMn+1 intersection region. c) INST region.	\geq	0.01	um
1xRVn.5d	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangle 1x RVn., when 1. 1xMn width W: $0.16\text{um} < W \leq 4.5\text{um}$ 2. Space S1 $< 0.13\text{um}$, the parallel run length $> 0.1\text{um}$.	\geq	0.015	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 158/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
1xRVn.6a	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.05\mu m < W \leq 0.055\mu m$ 2. Space $S1 \leq 0.055\mu m$, $S2 > 0.055\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.005	um
1xRVn.6b	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.055\mu m < W \leq 0.07\mu m$ 2. Space $S1 < 0.065\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.005	um
1xRVn.6c	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.07\mu m < W \leq 0.16\mu m$ 2. Space $S1 < 0.1\mu m$, the parallel run length $> 0.1\mu m$. DRC doesn't check 1xRVn: a) Two rectangular 1x Vns with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangular with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region	\geq	0.01	um
1xRVn.6d	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.16\mu m < W \leq 4.5\mu m$ 2. Space $S1 < 0.13\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.015	um
1xRVn.7 ^[NC]	Two square Vias are equal to one rectangular Via in the following rules (1xRVn.7).			
1xRVn.7	Redundant via requirement must be obeyed by one of following condition of via number and space for 1xMn and 1xMn+1 condition (one of 1xMn or 1xMn+1 width and length $W1 > 0.18\mu m$): 1. when $W1 > 0.18$ and $\leq 0.44\mu m$: a) At least one rectangular via; b) At least two square vias with space $\leq 0.1\mu m$; c) At least 4 square vias with space $\leq 0.6\mu m$ 2. when $W1 > 0.44\mu m$: a) At least 4 square vias with space $\leq 0.1\mu m$, which two square vias can be replaced by one rectangular via. space between (two rectangular vias) or (rectangular and square via) or (two square vias) $\leq 0.13\mu m$ when			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 159/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	<p>two square vias is replaced by one rectangular via.</p> <p>b) At least 9 square vias with space\leq0.85um, which two square vias can be replaced one rectangular via(at least 5 rectangular vias are equal to this 9 square vias. Rectangular via is prior to square via.</p>			
1xRVn.8a	<p>There should be at least one rectangular 1x Vn or two square 1x Vns in the intersection area of 1xMn and 1xMn+1, when either wide metal of 1xMn or 1xMn+1 with both length L$>$0.18um and width W$>$0.18um, the space between either via and wide metal is $<$1.65um (D3, D3 is the shortest running path length from Via to the wide metal).</p> <p>DRC doesn't check INST region.</p>			
1xRVn.8b	<p>There should be at least one rectangular 1x Vn or two square 1x Vns in the intersection area of 1xMn and 1xMn+1, when either wide metal of 1xMn or 1xMn+1 with both length L$>$1um and width W$>$1um, the space between either via and wide metal is \leq5um (D3, D3 is the distance \leq5um away from this wide metal).</p>			
1xRVn.8c	<p>There should be at least one rectangular 1x Vn or two square 1x Vns in the intersection area of 1xMn and 1xMn+1, when either wide metal of 1xMn or 1xMn+1 with both length L$>$5um and width W$>$1.5um, the space between either via and wide metal is \leq12um (D3, D3 is the distance \leq12um away from this wide metal).</p>			
1xRVn.9 ^[NC]	It's recommended to use rectangular via which is to avoid high resistance wherever layout allows.			
1xRVn.10	45-degree rotated rectangular 1x Vn is not allowed.			
1xRVn.11	<p>Single rectangular 1xVn is not allowed in "H-shape" 1xMn+1 when:</p> <ol style="list-style-type: none">1. The 1xMn+1 has "H-shape" interact with two metal holes: both two metal holes length \leq6um (L2) and two metal hole area \leq6um².2. The rectangular 1xVn overlaps on the center metal bar of this "H-shape" 1xMn+1.3. The center metal bar length\leq 1um (L) and the metal bar width \leq0.16um.			
1xRVn. 12 ^[R]	Recommended consecutive stacked rectangular 1x Vn layer,	\leq	4	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

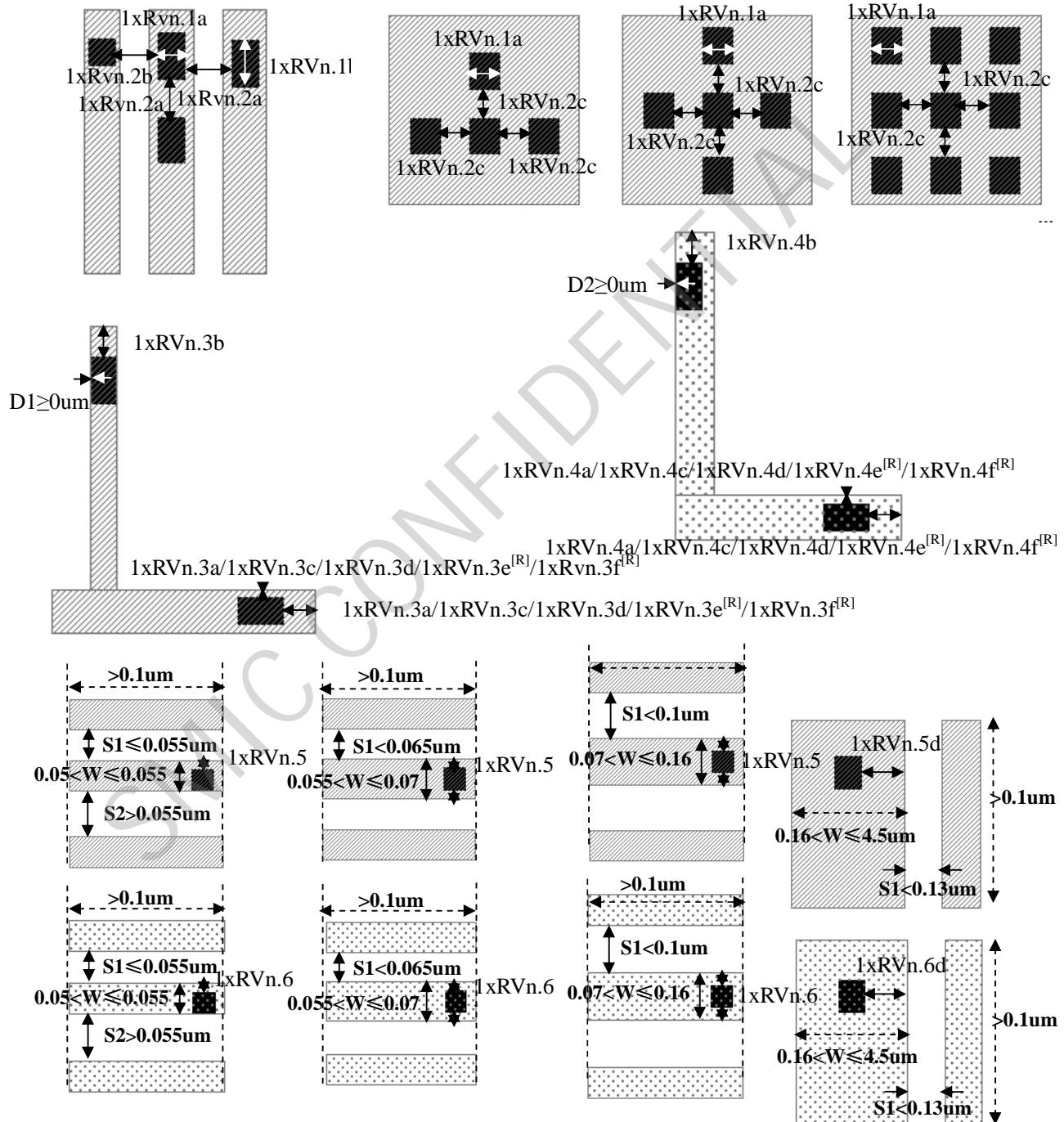


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 160/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	which has only one rectangular 1x Vn for each rectangular 1x Vn layer to avoid high Rc. This rule doesn't check MARKS and DUPMK1 region.			
1xRVn. 13^[R]	Recommended space between rectangular 1x Vn and 1xVn+1, where rectangular 1xVn and 1xVn+1 at different net and parallel run length > 0.02um	\geq	0.06	um

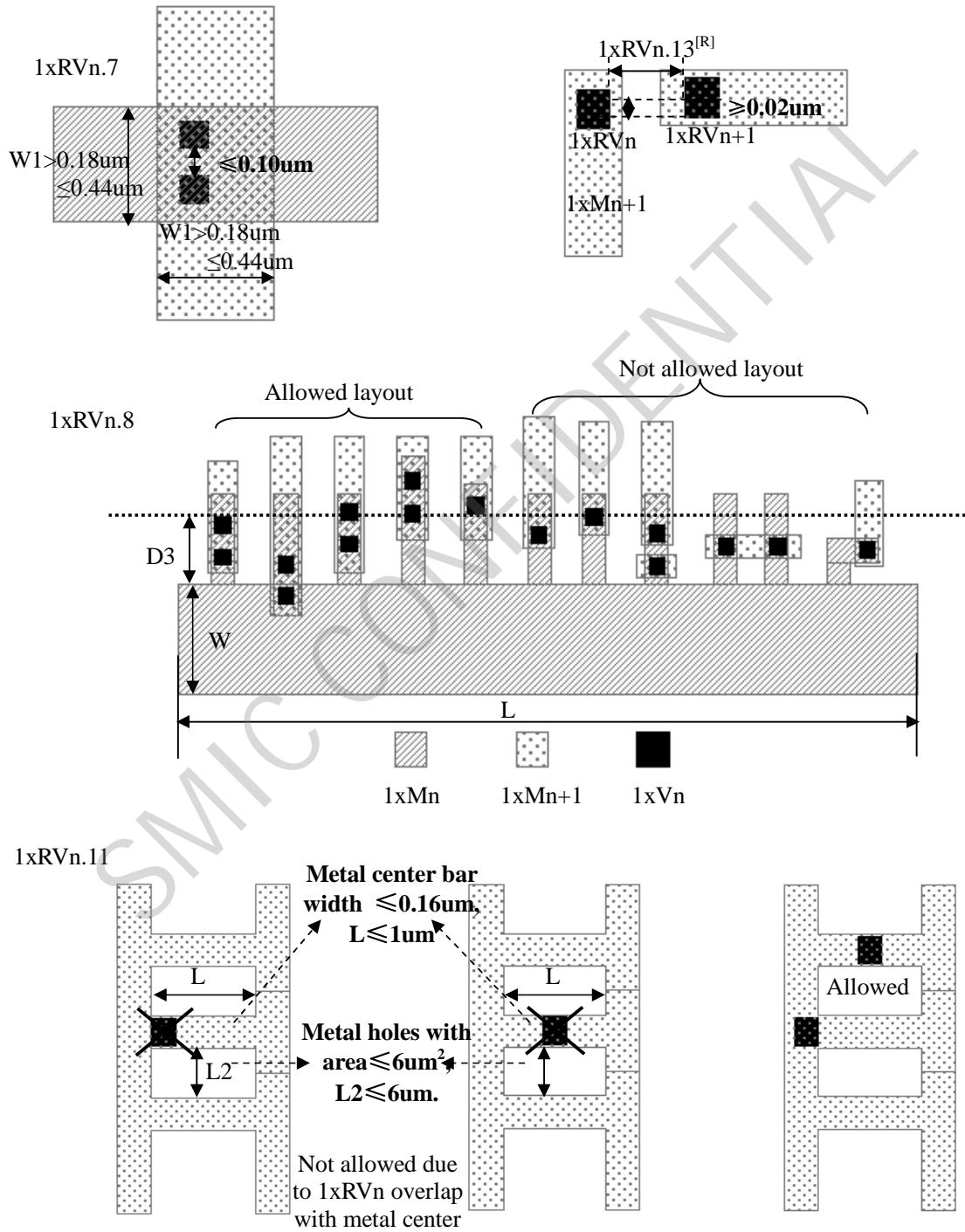
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	28nm Logic Low Power (Poly/SION)	Doc. Rev.:	Tech Dev	Page No.:
TD-LO28-DR-2006	Title: 1.05V/1.8V/2.5V Design Rules	2	Rev: 1.10.1	161/306



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 162/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 163/306
---------------------------	---	------------	----------------------	-------------------

7.2.21 2x Mn: 2x Metal design rules

Rule number	Description	Operation	Design Value	Unit
2xMn.1	2xMn width. DRC doesn't check DUPMK1 region for maximum rule check.	\geq	0.1	um
		\leq	12	um
2xMn.2a	Width of 45-degree 2xMn	\geq	0.34	um
2xMn.2b	Length of 45-degree 2xMn	\geq	1	um
2xMn.3a	Space between two 2xMns.	\geq	0.1	um
2xMn.3b	Space between two 2xMns when one or both 2xMn widths are >0.2um, and parallel run length of two 2xMns is >0.38um.	\geq	0.12	um
2xMn.3c	Space between two 2xMns when one or both 2xMn widths are >0.4um, and parallel run length of two 2xMns is >0.4um.	\geq	0.16	um
2xMn.3d	Space between two 2xMns when one or both 2xMn widths are >1.5um, and parallel run length of two 2xMns is >1.5um.	\geq	0.5	um
2xMn.3e	Space between two 2xMns when one or both 2xMn widths are >4.5um, and parallel run length of two 2xMns is >4.5um.	\geq	1.5	um
2xMn.4	Space between 2xMns and 2xMn dense line end (the parallel run length >-0.035um). 1. 2xMn line-end definition: 2xMn edge with length < 0.12um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.1um; 2. 2xMn dense line end definition: the space(S1) is <0.12um between any one adjacent edge of 2xMn line end and other 2xMn, other metal must be in the L1 and L2 extension region from metal line end, L1< 0.035um, L2 <0.12um. S1 should be the space between separate metal.	\geq	0.12	um
2xMn.5	Space between 2xMn(M) and 2xMn(N) with th parallel runlength>-0.035um, when space(S2) is <0.12um between 2xMn(N) line end and other 2xMn. 1. 2xMn line-end definition: 2xMn edge with length < 0.12um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.1um; 2. 2xMn(M) must be in the L1 and L2 extension region from metal line end, L1< 0.035um, L2 <0.12um.	\geq	0.12	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

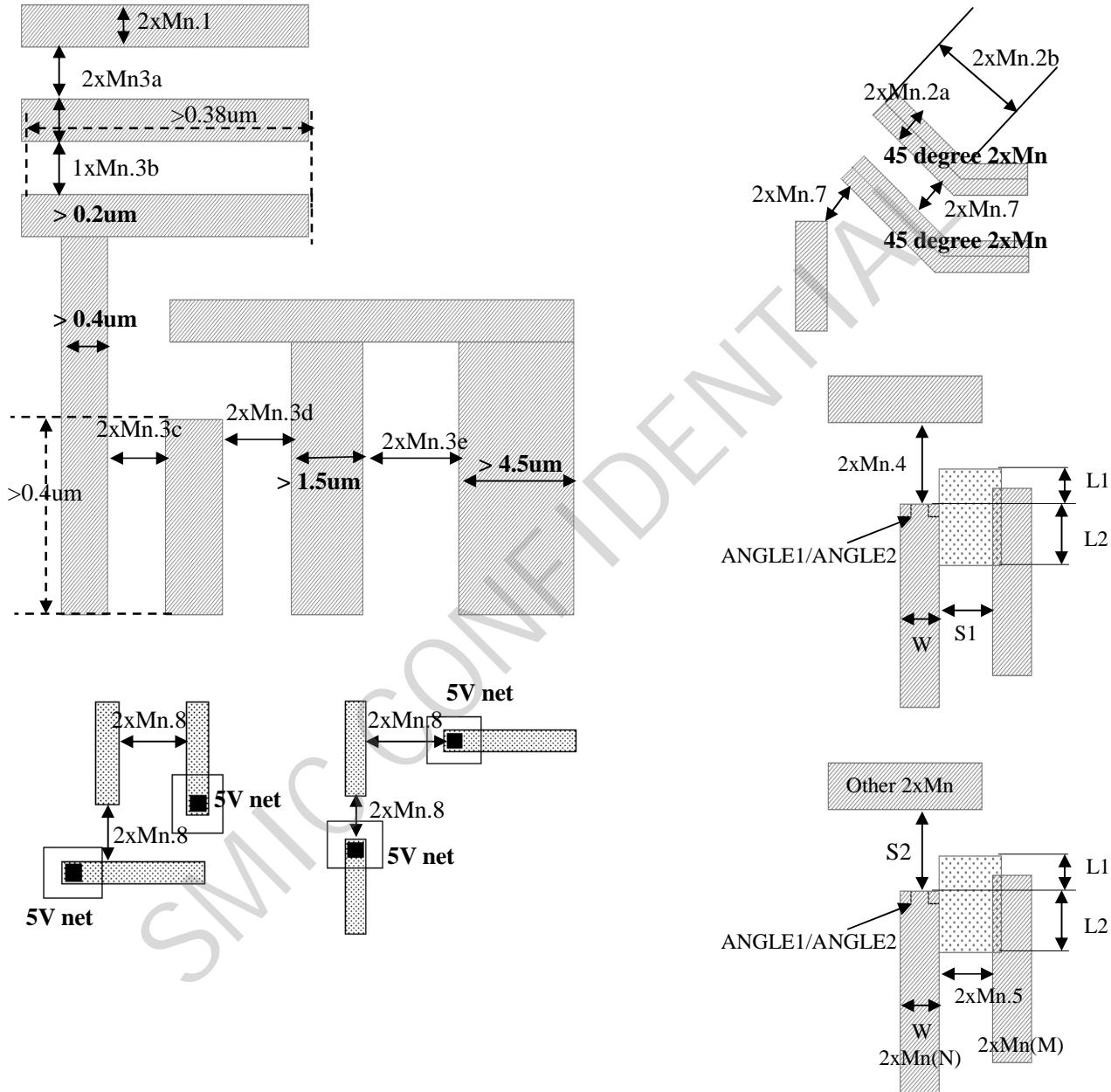


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 164/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
2xMn.6^[R]	Space between (2xMn or dummy 2xMn). DRC check maximum width of (NOT (2xMn or dummy 2xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LOGO.	\leq	4.5	um
2xMn.7	Space between 45-degree 2xMn and 2xMn	\geq	0.34	um
2xMn.8	Space between two 2xMns when one or both of 2xMn connects to 5V net	\geq	0.16	um
2xMn.9	2xMn area	\geq	0.06	um ²
2xMn.10	Enclosed dielectric area by 2xMn	\geq	0.26	um ²
2xMn.11	2xMn density (including dummy). Density check window size: 125um*125um, step size: 62.5um.	\geq	10%	
		\leq	85%	
2xMn.12	The density difference between any two neighboring checking windows (window 200*200, stepping 200um). DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	\geq	50%	
2xMn.13^[R]	2xMn density (including dummy) in DUMB/2xMnDUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMB/2xMnDUB width is >5um and <125um, where density ratio = 2xMn area / (DUMB/2xMnDUB) area.	\geq	10%	
		\leq	85%	
2xMn.14^[NC]	2xMn line-end must be rectangular.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 165/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 166/306
---------------------------	---	------------	----------------------	-------------------

7.2.22 2x Vn: 2x Via design rules

Rule number	Description	Operation	Design Value	Unit
2xVn.1	Fixed 2x Vn size (square shape)	=	0.1	um
2xVn.2	Space between 2x Vns	\geq	0.1	um
2xVn.3	Space between 2x Vn and its neighboring 2x Vn (T). The definition of neighboring 2x Vn (T) : 1. 2x Vn (T) is in a 2x Vn group 2.The number of this 2x Vn group is ≥ 4 , there are at least three 2x Vns neighboring to 2x Vn (T) 3.The space between 2x Vn (T) to other 2x Vns in this group <0.14um	\geq	0.13	um
2xVn.4	Space between two neighbor 2xVns at different net with the parallel run length>0)	\geq	0.13	um
2xVn.5	Space between two 2xVns when at least one 2xVn connects to 5V	\geq	0.16	um
2xVn.6	2x Vn must be fully covered by 2xMn or 1xMn. Enclosure by 2xMn or 1xMn must follow (2x Vn.6a or 2x Vn.6c or 2x Vn.6d) or (2x Vn.6b) or 2x Vn.6c or 2x Vn.6d)as below.			
2xVn.6a	Enclosure by 2xMn, where 2xMn is the metal layer directly underneath 2x Vn.	\geq	0	um
2xVn.6b	Enclosure by 1xMn, where 1xMn is the metal layer directly underneath 2x Vn.	\geq	0.02	um
2xVn.6c	Enclosure by 1xMn or 2xMn when enclosure by 1xMn or 2xMn on either perpendicular direction ≥ 0 um and <0.03um and 1xMn or 2xMn is the metal layer directly underneath 2x Vn.	\geq	0.04	um
2xVn.6d	Enclosure by 1xMn or 2xMn in four sides, and 1xMn or 2xMn is the metal layer directly underneath 2x Vn.	\geq	0.03	um
2xVn.7	2x Vn must be fully covered by 2xMn+1. Enclosure by 2xMn+1 must follow (2x Vn.7a or 2x Vn.7b or 2x Vn.7c)as below.			
2xVn.7a	Enclosure by 2xMn+1, where 2xMn+1 is the metal layer directly above 2x Vn.	\geq	0	um
2xVn.7b	Enclosure by 2xMn+1 when enclosure by 2xMn+1 on either	\geq	0.04	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



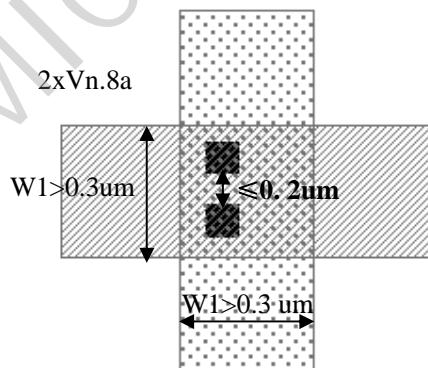
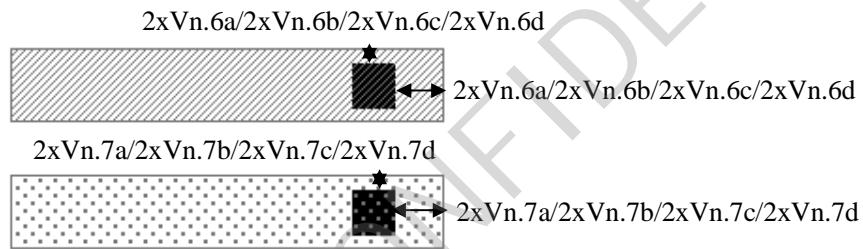
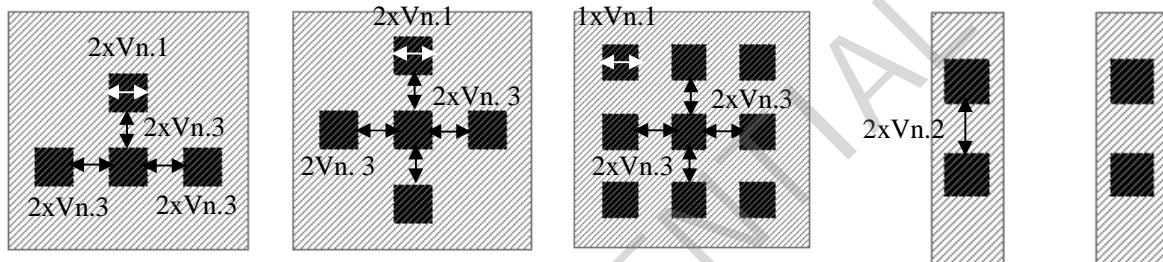
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 167/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	perpendicular direction $\geq 0\text{um}$ and $<0.03\text{um}$ and 1xMn is the metal layer directly above 2x Vn.			
2xVn.7c	Enclosure by 2xMn+1 in four sides, and 2xMn+1 is the metal layer directly above 2x Vn.	\geq	0.03	um
2xVn.8a	There should be at least two 2x Vns with space $\leq 0.2\text{um}$ (S1) or at least four 2xVns with space $\leq 0.25\text{um}$ (S2) in 2x Mn and 2x Mn+1 intersection area, when either 2x Mn and 2x Mn+1 width and length (W1) $> 0.3\text{um}$ and $\leq 0.7\text{um}$.			
2xVn.8b	There should be at least two 2x Vns with space $\leq 0.2\text{um}$ (S1) or at least four 2xVns with space $\leq 0.35\text{um}$ (S2) in 2x Mn and 2x Mn+1 intersection area, when either 2x Mn and 2x Mn+1 width and length (W1) $> 0.7\text{um}$.			
2xVn.9a	There should be at least two 2x Vn in the intersection area of 2xMn and 2xMn+1, when either wide metal of 2xMn or 2xMn+1 with both length L $> 0.3\text{um}$ and width W $> 0.3\text{um}$, the space between either via and wide metal is $\leq 0.8\text{um}$ (D3, D3 is the shortest running path length from 2xVn to the wide metal).			
2xVn.9b	There should be at least two 2x Vn in the intersection area of 2xMn and 2xMn+1, when either wide metal of 2xMn or 2xMn+1 with both length L $> 2\text{um}$ and width W $> 2\text{um}$, the space between either via and wide metal is $\leq 2\text{um}$ (D3, D3 is the shortest running path length from 2xVn to the wide metal).			
2xVn.9c	There should be at least two 2x Vn in the intersection area of 2xMn and 2xMn+1, when either wide metal of 2xMn or 2xMn+1 with both length L $> 10\text{um}$ and width W $> 3\text{um}$, the space between either via and wide metal is $\leq 5\text{um}$ (D3, D3 is the shortest running path length from 2xVn to the wide metal).			
2xVn.10	Single 2xVn is not allowed in "H-shape" 2xMn+1 when: 1. The 2xMn+1 has "H-shape" interact with two metal holes: both two metal holes length $\leq 6\text{um}$ (L2) and two metal hole area $\leq 6\text{um}^2$. 2. The 1xVn overlaps on the center metal bar of this "H-shape" 2xMn+1. 3. The center metal bar length $\leq 1\text{um}$ (L) and the metal bar width $\leq 0.3\text{um}$.			
2xVn.11^[NC]	It's recommended to use redundant vias to avoid high resistance wherever layout allows.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

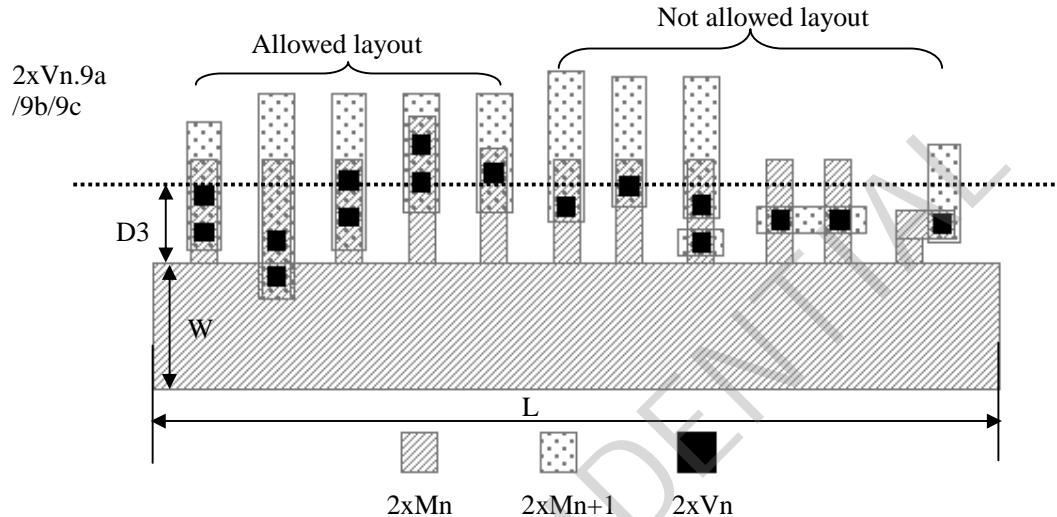
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 168/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
2xVn.12	45-degree rotated 2x Vn is not allowed.			

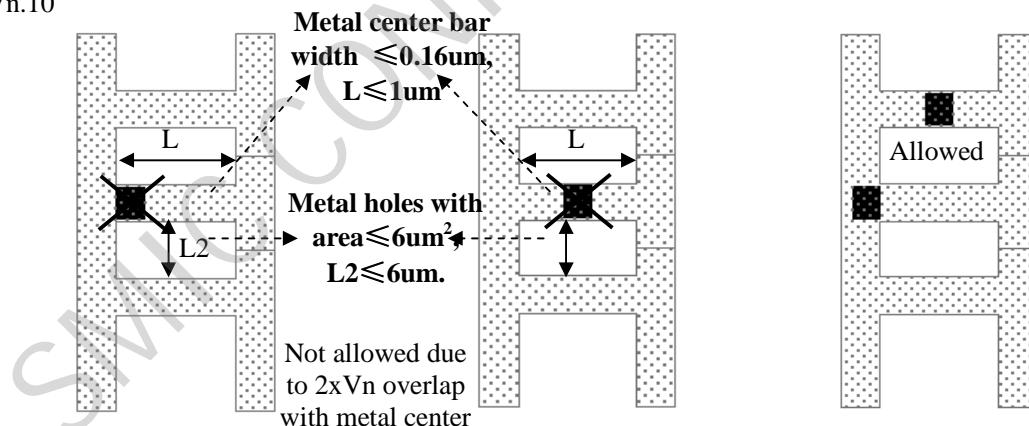


The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 169/306
---------------------------	---	------------	----------------------	-------------------



2xVn.10



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 170/306
---------------------------	---	------------	----------------------	-------------------

7.2.23 8x TVn: 8x Via(TV1/TV2) design rules

Rule number	Description	Operation	Design Value	Unit
8xTVn.1	Fixed 8x TVn size (square shape).	=	0.36	um
8xTVn.2a	Space between single 8x TVns.	\geq	0.34	um
8xTVn.2b	Space between 8x TVn and its neighboring 8x TVn (T). The definition of neighboring 8x TVn (T) : 1. 8x TVn (T) is in a 8x TVn group 2.The number of this 8x TVn group is ≥ 4 , there are at least 3 8x TVn s neighboring to 8x TVn (T) 3.The space between 8x TVn (T) to other 8x TVn s in this group <0.56um	\geq	0.54	um
8xTVn.3	8x TVn fully enclosure by 1x Mn/2x Mn/8x TM, where 1x Mn/2x Mn/8x TM is the metal layer directly underneath 8x TVn. 8x TVn must be fully enclosed by 1x Mn/2x Mn/8x TM	\geq	0.02	um
8xTVn.4	Enclosure by 1x Mn/2x Mn/8x TM when enclosure by 1x Mn/2x Mn/8x TM on either perpendicular direction ≥ 0.02 um, and 1x Mn/2x Mn/8x TM is the metal layer directly underneath 8x TVn.	\geq	0.08	um
8xTVn.5	8x TVn fully enclosure by 8x TM , where 8x TM is the metal layer directly above 8x TVn. 8x TVn must be fully enclosed by 8x TM	\geq	0.02	um
8xTVn.6	Enclosure by 8x TM when enclosure by 8x TM on either perpendicular direction ≥ 0.02 um, and 8x TM is the metal layer directly above 8x TVn.	\geq	0.08	um
8xTVn.7	There should be at least two 8x TVns with space ≤ 1.6 um (S1) in 8x TMn and 8x TMn+1 intersection area, when either 8x TMn or 8x TMn+1 width and length (W1) > 1.7 um.			
8xTVn.8	There should be at least two 8x TVns in the intersection area of 8xMn and 8xMn+1, when either wide metal of 8xTMn or 8xTMn+1 with both length L>10um and width W>3um, the space between either via and wide metal is ≤ 6 um (D3, D3 is the shortest running path length from 8xTVn to the wide metal).			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

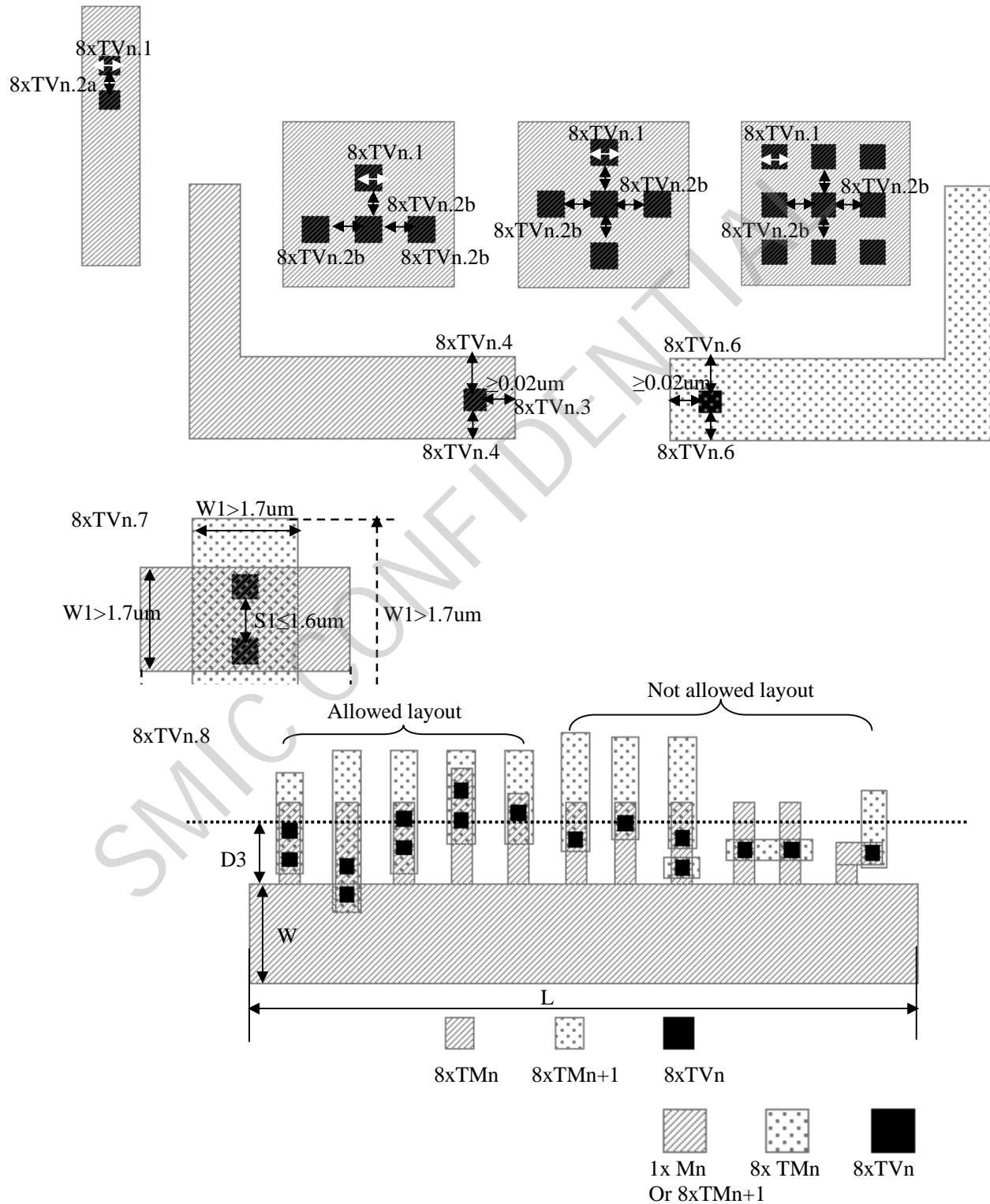


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 171/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
8xTVn.9	45-degree rotated 8x TVn is not allowed.			
8xTVn.10^[NC]	Recommend to use redundant vias to avoid high Rc wherever layout allows.			
8xTVn.11^[NC]	8x TVn and 10xTVn can't be used on same chip.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev:	Tech Dev Rev: 1.10.1	Page No.: 172/306
TD-LO28-DR-2006			2		



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 173/306
---------------------------	---	------------	----------------------	-------------------

7.2.24 8x TMn : 8x Metal (TM1 /TM2) design rules

Rule number	Description	Operation	Design Value	Unit
8xTMn .1	8x TMn width. Maximum width DRC doesn't check PAD, DUPMK1 and INDMY region.	\geq	0.4	um
		\leq	12	um
8xTMn .2a	Space between 8x TMns.	\geq	0.4	um
8xTMn .2b	Space between two 8x TMns that have a parallel run length >1.5um when at least one 8x TMn widths are >1.5um.	\geq	0.5	um
8xTMn .2c	Space between two 8x TMns that have a parallel run length >4.5um when at least one 8x TMn widths is >4.5um.	\geq	1.5	um
8xTMn .2d^[R]	Space between (8x TMn or dummy 8x TMn). DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	\leq	12	um
8xTMn .3	8x TMn area	\geq	0.56	um ²
8xTMn .4	Dielectric area enclosed by 8x TMn	\geq	0.572	um ²
8xTMn .5	8xTMn density (including dummy).Density check window size: 125um*125um, step size: 62.5um. DRC doesn't check DUPMK1 region.	\geq	10%	
		\leq	85%	
8xTMn .5^[R]	8xTMn density (including dummy) in DUMB/TMnDUB. Density check window size: 125um*125um, step size: 62.5um. DRC doesn't check DUPMK1 region. DRC need check the design if DUMB/TMnDUB width is >5um and <125um, where density ratio= 8xTMn area/(DUMB/TMnDUB) area.	\geq	10%	
		\leq	85%	
8xTMn .6^[R]	TMn density (including dummy) in full chip	\geq	20%	
8xTMn .7	The density difference between any two neighbouring checking windows (window 200*200, stepping 200um).	\leq	50%	
8xTMn .8^[NC]	8xTMn line-end must be rectangular. Other shaped are not allowed.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



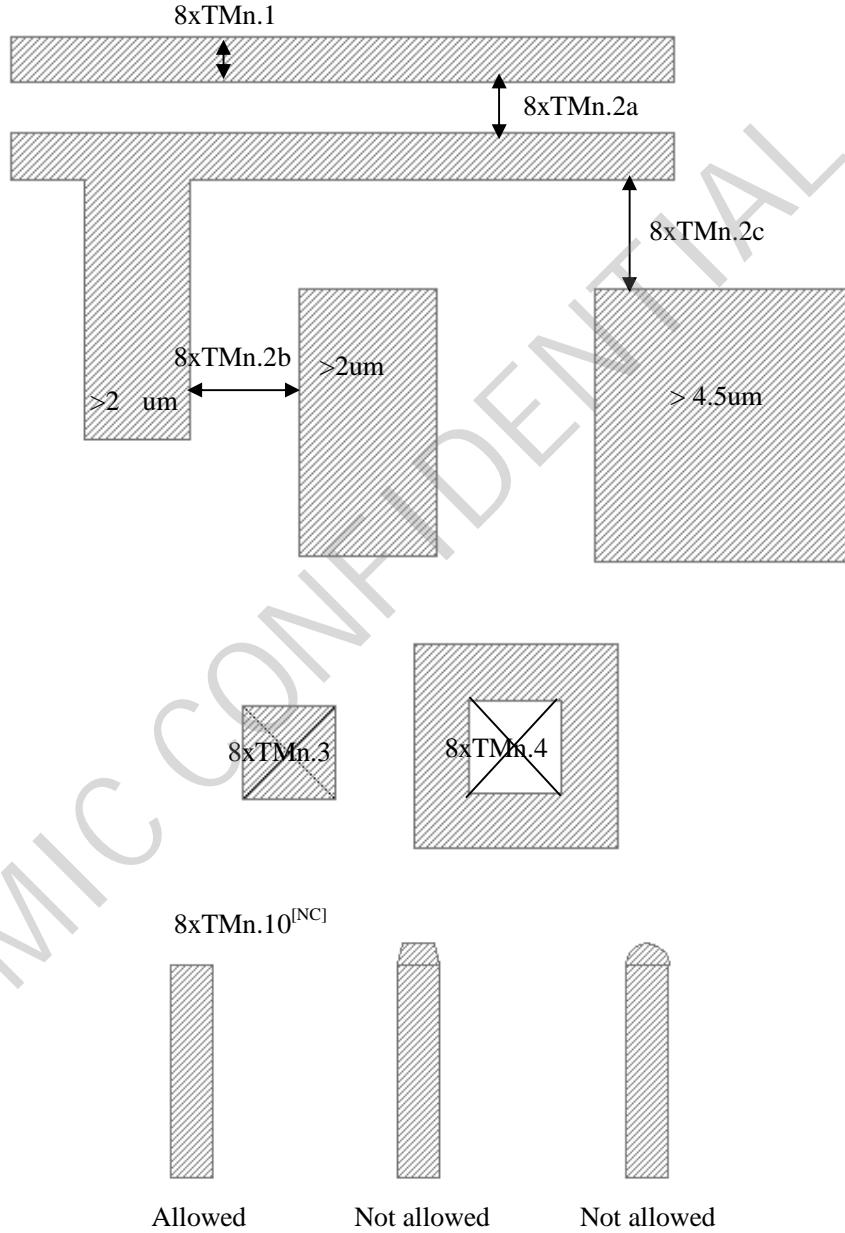
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 174/306
---------------------------	---	------------	----------------------	-------------------

8xTMn .9^[NC]	8x TMn and 10xTMn can't be used on same chip.			
--------------------------------	---	--	--	--

SMIC CONFIDENTIAL

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 175/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 176/306
---------------------------	---	------------	----------------------	-------------------

7.2.25 10x TVn: 10x Via(TV1/TV2) design rules

Rule number	Description	Operation	Design Value	Unit
10xTVn.1	Fixed 10x TVn size (square shape).	=	0.46	um
10xTVn.2a	Space between single 10x TVns.	\geq	0.44	um
10xTVn.2b	Space between 10x TVns in 2x2 10x TVns array at the same net. Two Vias whose space $\leq 0.55\text{um}$ are considered to be in the same array.	\geq	0.54	um
10xTVn.2c	Space between 10x TVn and its neighboring 10x TVn (T). The definition of neighboring 10x TVn (T) : 1. 10x TVn (T) is in a 10x TVn group 2. The number of this 10x TVn group is ≥ 4 , there are at least 3 10x TVns neighboring to 10x TVn (T) 3. The space between 10x TVn (T) to other 10x TVns in this group $\leq 0.66\text{um}$	\geq	0.66	um
10xTVn.3	10x TVn enclosure by 1x Mn/2x Mn/10x TMn, where 1x Mn/2x Mn/10x TMn is the metal layer directly underneath 10x TVn. 10x TVn must be fully covered by 1x Mn/2x Mn/10x TMn.	\geq	0.02	um
10xTVn.4	Enclosure by 1x Mn/2x Mn/10x TMn when enclosure by 1x Mn/2x Mn/10x TMn on either perpendicular direction $\geq 0.02\text{um}$, and 1x Mn/2x Mn/10x TMn is the metal layer directly underneath 10x TVn.	\geq	0.08	um
10xTVn.5	10x TVn enclosure by 10x TMn , where 10x TMn is the metal layer directly above 10x TVn. 10x TVn must be fully covered by 10x TMn	\geq	0.02	um
10xTVn.6	Enclosure by 10x TMn when enclosure by 10x TMn on either perpendicular direction $\geq 0.02\text{um}$, and 10x TMn is the metal layer directly above 10x TVn.	\geq	0.08	um
10xTVn.7	At least two 10xTVns with space $\leq 1.6\text{um}$ (S1) in 10x TMn and 10x TMn+1 intersection area, when either 10x TMn or 10x TMn+1 width and length (W1) $> 1.7\text{um}$.			
10xTVn.8	There should be at least two 10xTVn in the intersection area of 10xTM and 10xTM+1, when either wide metal of 10xTM or 10xTM+1 with both length L $> 10\text{um}$ and			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

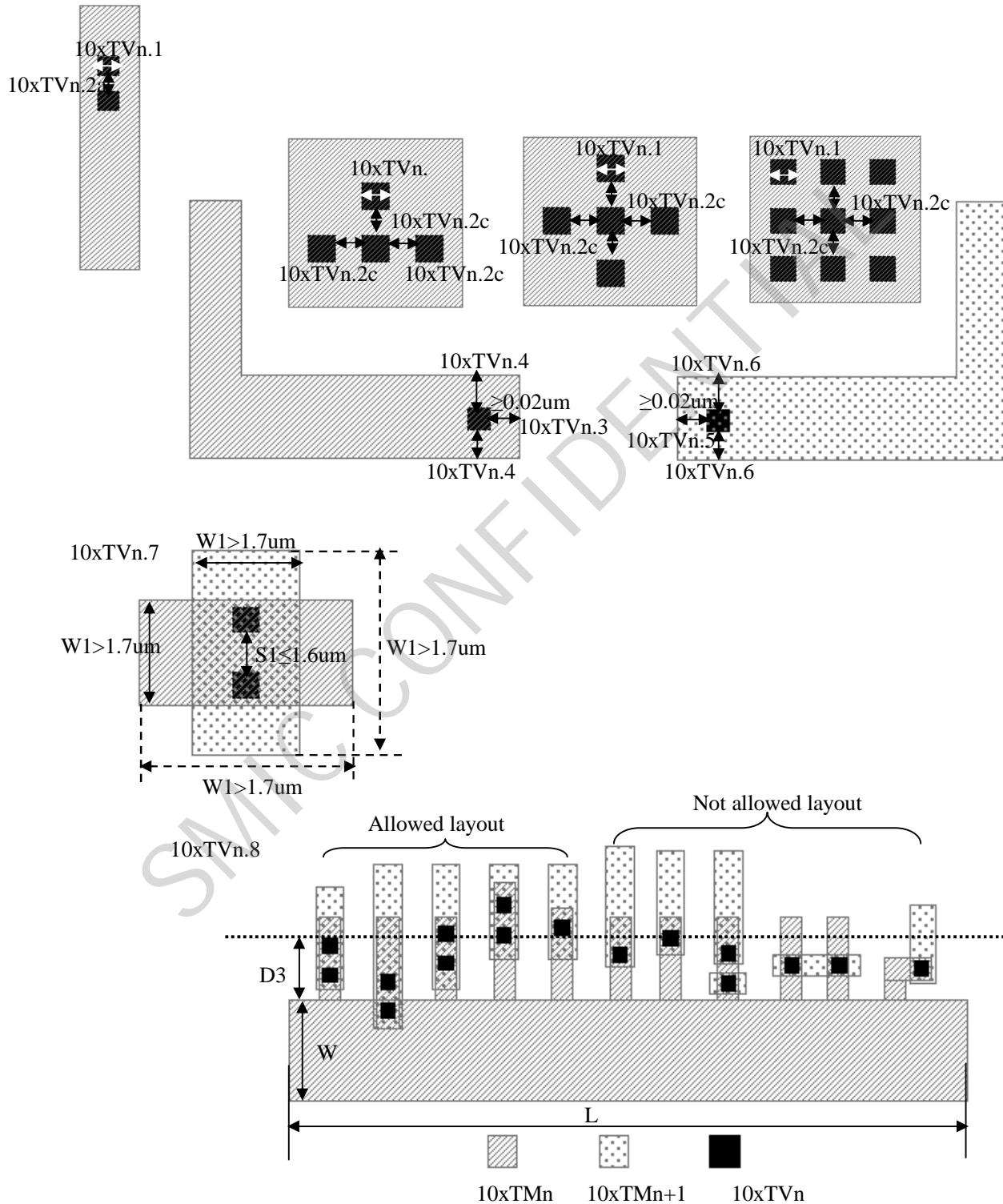


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 177/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
	width W>3um, the space between either via and wide metal is ≤6um (D3, D3 is the distance 5um away from this wide metal).			
10xTVn.9	45-degree rotated 10x TVn is not allowed.			
10xTVn.10^[NC]	Recommend to use redundant vias to avoid high Rc wherever layout allows.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 178/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

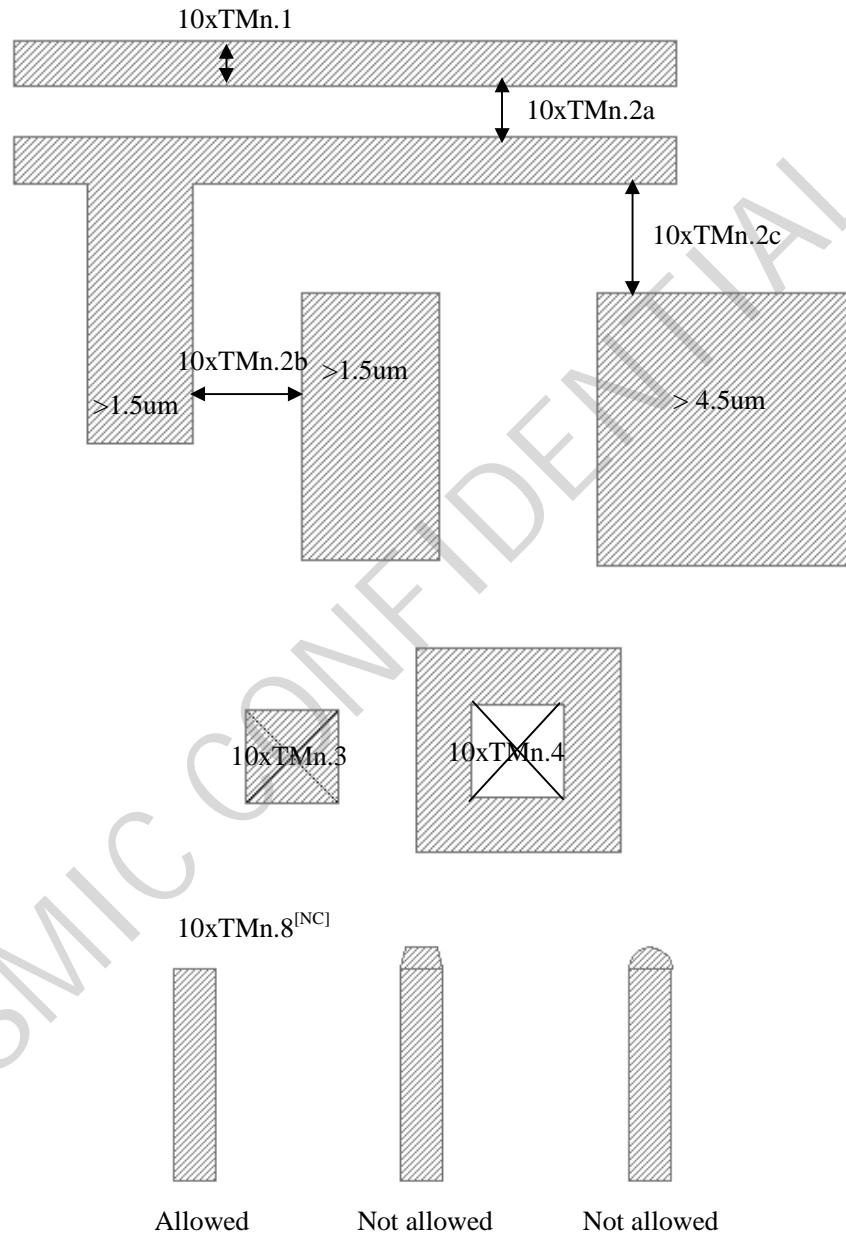
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 179/306
---------------------------	---	------------	----------------------	-------------------

7.2.26 10xTMn : 10x Metal (TM1 /TM2) design rules

Rule number	Description	Operation	Design Value	Unit
10xTMn .1	10x TMn width. Maximum width DRC doesn't check PAD, DUPMK1 and INDMY region.	\geq	0.5	um
		\leq	12	um
10xTMn .2a	Space between 10x TMns.	\geq	0.5	um
10xTMn .2b	Space between two 10x TMns that have a parallel run length >1.5um when at least one 10x TMn widths are >1.5um.	\geq	0.65	um
10xTMn .2c	Space between two 10x TMns that have a parallel run length >4.5um when at least one 10x TMn widths is >4.5um.	\geq	1.5	um
10xTMn .2d^[R]	Space between (10xTMn or dummy 10xTMn). DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	\leq	12	um
10xTMn .3	10x TMn area	\geq	1	um ²
10xTMn .4	Dielectric area enclosed by 10x TMn	\geq	2.5	um ²
10xTMn .5	10xTMn density (including dummy).Density check window size: 125um*125um, step size: 62.5um. DRC doesn't check DUPMK1 region.	\geq	10%	
		\leq	85%	
10xTMn .6^[R]	10xTMn density (including dummy) in DUMB/TMnDUB. Density check window size: 125um*125um, step size: 62.5um. DRC doesn't check DUPMK1 region. DRC need check the design if DUMB/TMnDUB width is >5um and <125um, where density ratio= 10xTMn area/(DUMB/TMnDUB) area.	\geq	10%	
		\leq	85%	
10xTMn .7	The density difference between any two neighbouring checking windows (window 200*200um, stepping 200um).	\leq	50%	
10xTMn .8^[NC]	10xTMn line-end must be rectangular.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 180/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

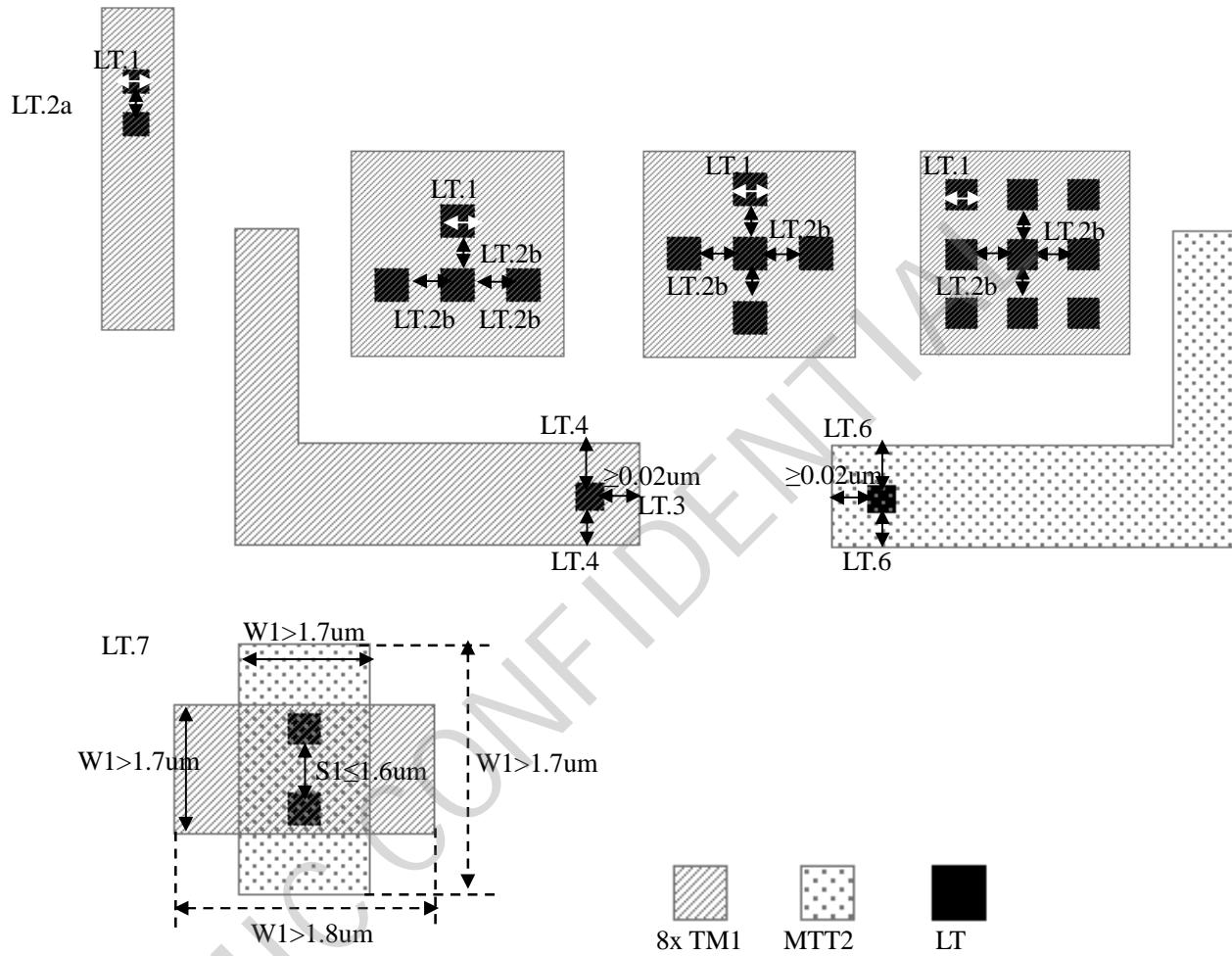
Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 181/306
-----------	-------------	--	------------	----------------------	-------------------

7.2.27 8x UTV: 8x UTV(LT) design rules

Rule number	Description	Operation	Design Value	Unit
LT.1	Fixed LT size (square shape).	=	0.36	um
LT.2a	Space between single LTs.	\geq	0.34	um
LT.2b	Space between LT and its neighboring LT (T). The definition of neighboring LT (T) : 1. LT (T) is in a LT group 2. The number of this LT group is ≥ 4 , there are at least 3 LT s neighboring to LT (T) 3. The space between LT (T) to other LT s in this group <0.56um	\geq	0.54	um
LT.3	(Purposely blank)			
LT.4	Enclosure by 1x Mn/2x Mn/8x TM1, 1x Mn/2x Mn/8x TM1 is the metal layer directly underneath LT. LT must be fully covered by 1x Mn/2x Mn/8x TM1	\geq	0.08	um
LT.5	(Purposely blank)			
LT.6	Enclosure by MTT2 when enclosure by MTT2 LT must be fully covered by MTT2	\geq	0.3	um
LT.7	There should be at least two LTs with space $\leq 1.6\text{um}$ (S1) in 8x TM1 and MTT2 intersection area, when either 8x TM1 or MTT2 width and length (W1) $> 1.7\text{um}$.			
LT.8	There should be at least two LTs in the intersection area of 8x TM1 and MTT2, when either wide metal of 8x TM1 or MTT2 with both length L $> 10\text{um}$ and width W $> 3\text{um}$, the space between either via and wide metal is $\leq 6\text{um}$ (D3, D3 is the shortest running path length from Via to the wide metal).			
LT.9	45-degree rotated LT is not allowed.			
LT.10^[NC]	Recommend to use redundant vias to avoid high Rc wherever layout allows.			

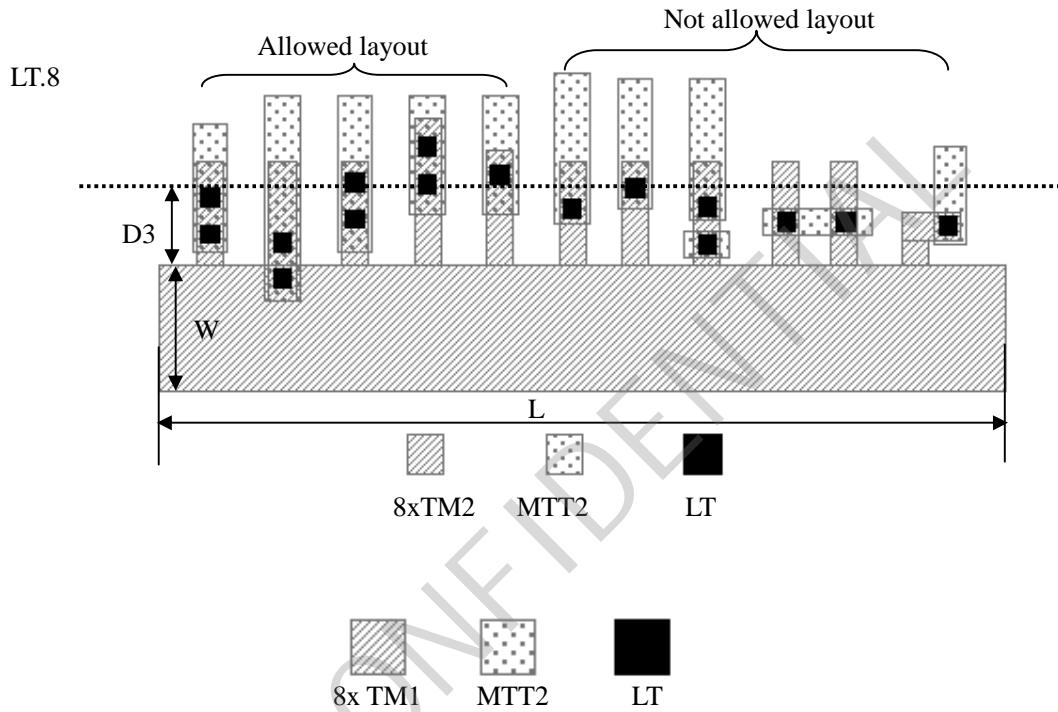
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 182/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 183/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 184/306
---------------------------	---	------------	----------------------	-------------------

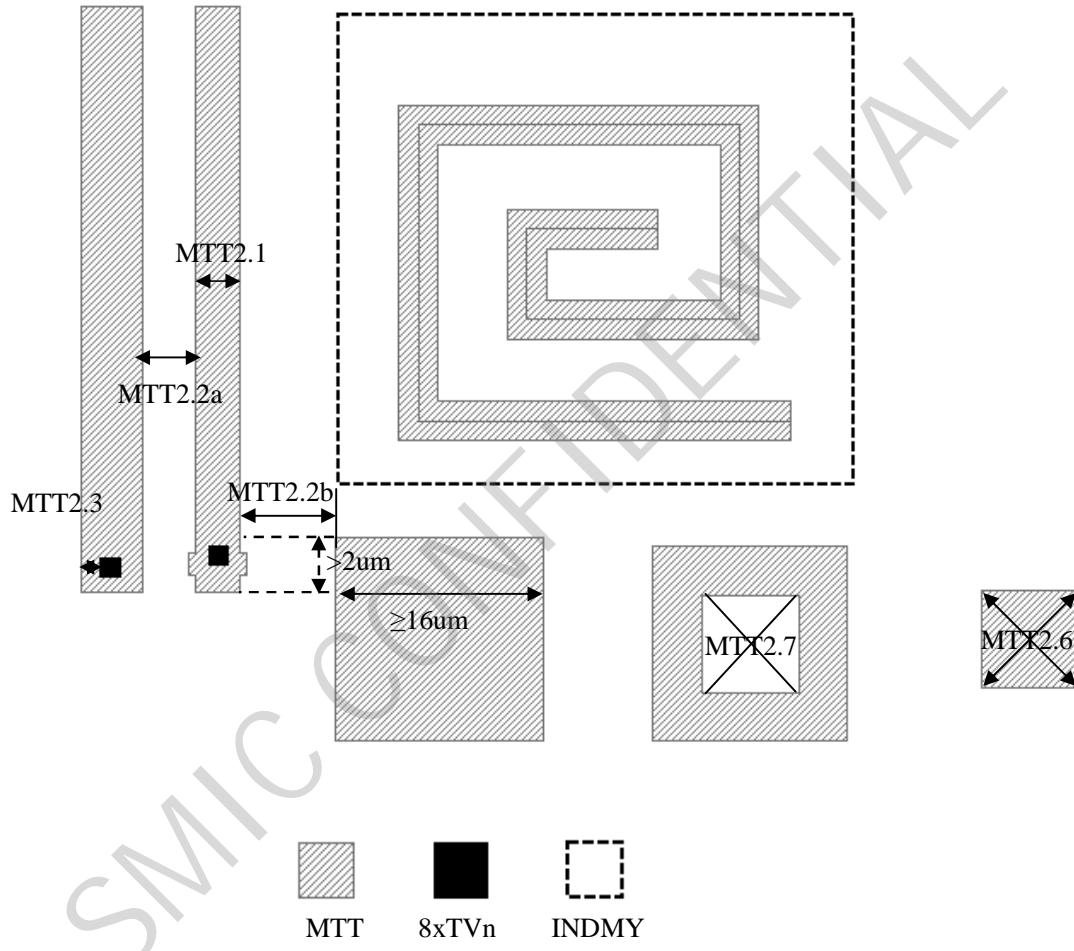
7.2.28 MTT2 design rules (ultra-thick metal)

MTT2 design rules are only used for ultra-thick top metal (3.35um).

Rule number	Description	Operation	Design Value	Unit
MTT2.1	Metal width.	\geq	2	um
MTT2.2a	Space between two MTT2 regions.	\geq	1	um
MTT2.2b	Space between two MTT2s that have a parallel run length >4.5um when at least one MTT2 width is >4.5um.	\geq	1.5	um
MTT2.3	(Purposely blank)			
MTT2.4	(Purposely blank)			
MTT2.5	(Purposely blank)			
MTT2.6	MTT2 Area (um ²).	\geq	9	um ²
MTT2.7	Dielectric area enclosed by MTT2 (in um ²).	\geq	9	um ²
MTT2.8	Density of MTT2 (including dummy). Density check window size: 125um*125um, step size: 62.5um, exclude: 1. DUPMK1. 2. Chip corner and seal ring. 3. LOGO.	\geq	10%	
		\leq	85%	
MTT2.9	MTT2 density in full chip(including dummy)	\geq	20%	
		\leq	55%	
MTT2.10	(Purposely blank)			
MTT2.11	(Purposely blank)			
MTT2.12	(Purposely blank)			
MTT2.13^[NC]	(Purposely blank)			
MTT2.14	MTT2 line width allowed. DRC doesn't check the MTT2 underneath of MD, DUPMK1 and INDMY region	\leq	12	um
MTT2.15^[NC]	MTT2 line-end must be rectangular.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev:	Tech Dev Rev: 1.10.1	Page No.: 185/306
TD-LO28-DR-2006			2		



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 186/306
---------------------------	---	------------	----------------------	-------------------

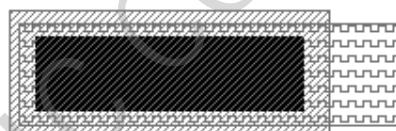
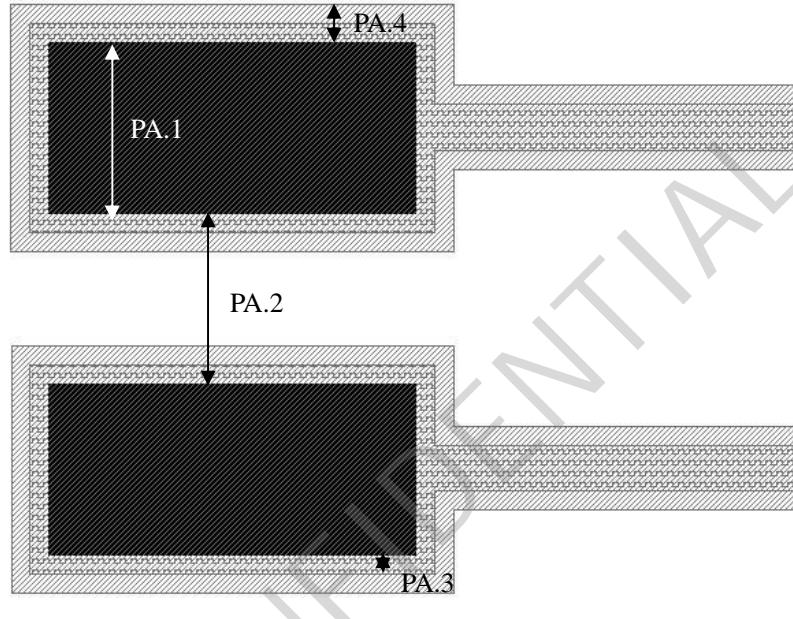
7.2.29 PA: Passivation 1 design rules

Passivation 1 can be used for pad opening and AL RDL Via opening.

Rule Number	Description	Operation	Design Value	Unit
PA.1	PA width	\geq	2	um
PA.2	Space between two PA	\geq	2	um
PA.3	ALPA enclosure of PA	\geq	0.5	um
PA.4	TM2, MTT2 enclosure of PA. PA must be fully covered by TM2, MTT2	\geq	0.5	um
PA.5	PA without ALPA above it is not allowed.			
PA.6	45-degree rotated PA is not allowed (except INDMY)			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

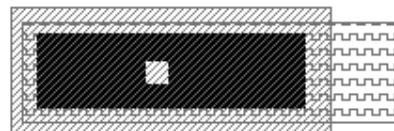
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 187/306
---------------------------	---	------------	----------------------	-------------------



PA.5: Correct layout



PA.5 : Not allowed for no ALPA on PA



PA.5: Not allowed for ALPA hole within PA



TM2/MMT2



PA



ALPA

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 188/306
---------------------------	---	------------	----------------------	-------------------

7.2.30 ALPA design rules

ALPA layers can be used to draw Al inter-connect lines (ALRDL), Al fuse metal lines, Al bumping pads, and re-distribution Al pads.

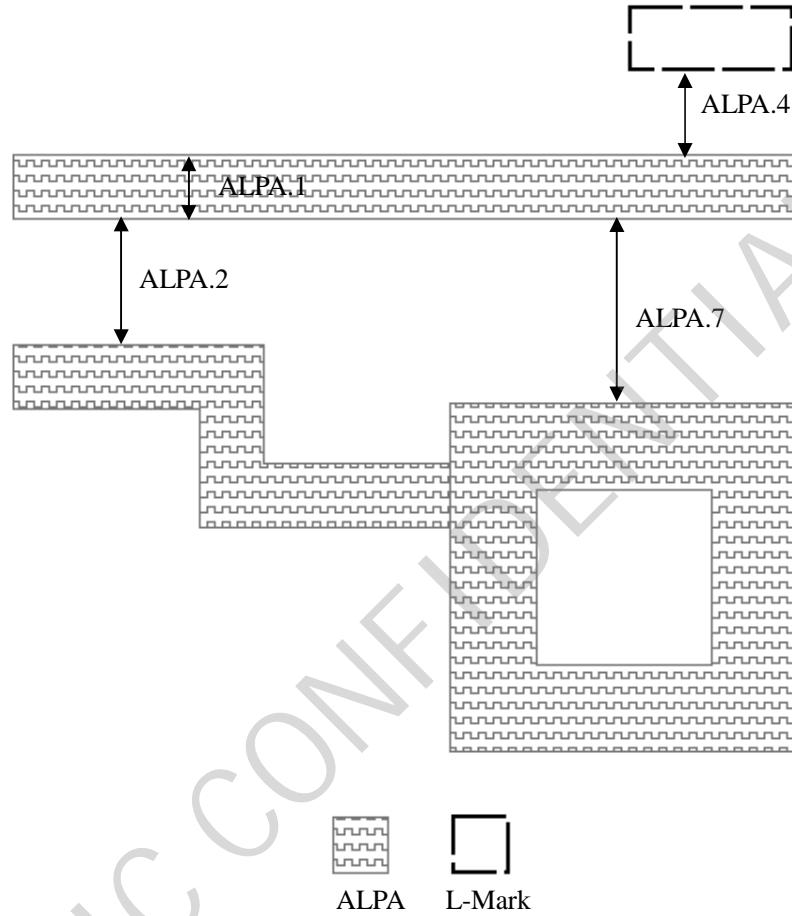
Rule number	Description	Operation	Design Value	Unit
ALPA.1	ALPA width.	\geq	2	um
ALPA.2	ALPA space. This rule doesn't check the space in the same polygon.	\geq	2	um
ALPA.3^[R]	ALPA density (including dummy) with 100um*100um window, with exemption of interacting inductor.	\geq	10%	
ALPA.4^{[R][NC]}	Space between ALRDL and L mark window.	\geq	10	um
ALPA.5	ALPA density(including dummy).	\geq	10%	
ALPA.6	ALPA density(including dummy).	\leq	70%	
ALPA.7	Space between (ALPA AND (MD sizing up 3um)) and ((ALPA AND (MD sizing up 3um)) or ALRDL). ALRDL is defined as ALPA layer width equal or smaller than 35um. This rule doesn't check the space in the same polygon.	\geq	2.5	um
ALPA.8^[NC]	ALPA must be drawn layer.			
ALPA.9^[NC]	ALPA includes ALPA Pad and ALRDL. ALRDL is defined as ALPA layer width equal or smaller than 35um. ALPA pad is defined as ALPA layer width larger than 35um.			

Note:

1. In addition to the design rules above, the PA design rules must be observed.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 189/306
---------------------------	---	------------	----------------------	-------------------



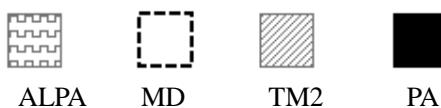
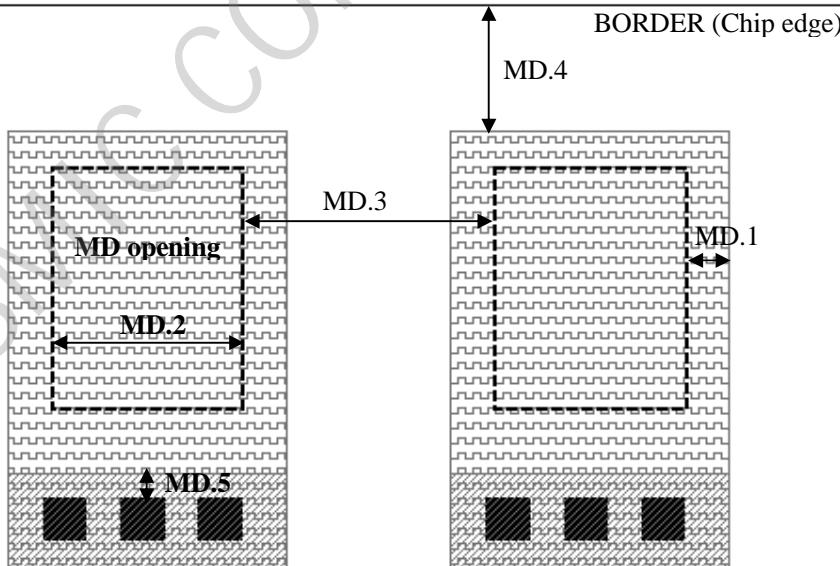
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 190/306
---------------------------	---	------------	----------------------	-------------------

7.2.31 MD(Passivation 2) design rules

MD is used for opening of Al redistributed patterns. MD should follow the rules below.

Rule number	Description	Operation	Design Value	Unit
MD.1	MD enclosure by ALPA.	\geq	1	um
MD.2	MD width	\geq	14	um
MD.3	MD space	\geq	5	um
MD.4^[R]	MD must be within BORDER (chip edge)	\geq	3	um
MD.5	Space between MD and PA. Space=0 is allowed	\geq	1.7	um
MD.6^[R]	(Purposely blank)			
MD.7	Inductor is prohibited under MD wire-bond pad opening		-	
MD.8^[NC]	MD must be a drawn layer			
MD.9	MD is prohibited to interact with PA(PA size <3um)			



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 191/306
---------------------------	---	------------	----------------------	-------------------

7.2.32 DUP(Device Under Pad) design rules

DUPMK1 (89;156) is the marking layer for DUP pad.

DUP pad area in below rules is (DUPMK1 AND MD).

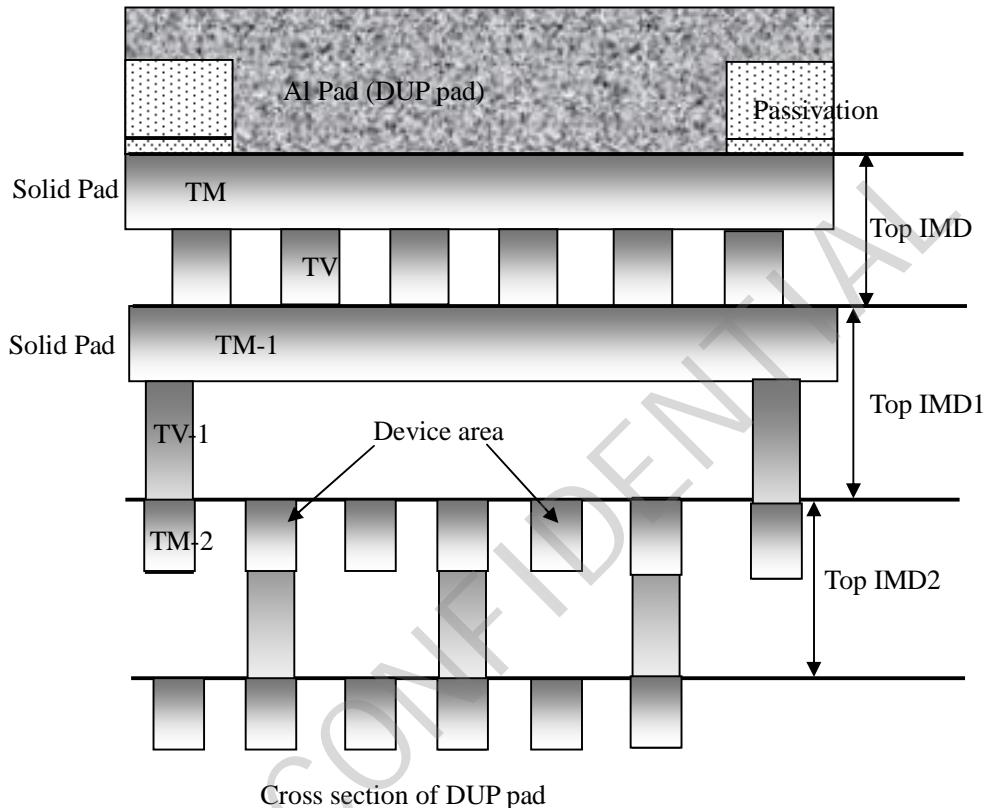
Rules Number	Description	Operation	Design Value	Unit
DUP.1	For MD that interacts with DUPMK1, this piece of MD must be fully covered by DUPMK1.			
DUP.2	Two metal layers (TM and TM-1) are needed between DUP pad and device, where the metal design must be solid.			
DUP. 2a^[NC]	It's not allowed to add metal slots for TM and TM-1 under the DUP pad opening area.			
DUP.3^[NC]	Device must be located underneath TM-1 layer.			
DUP.4	TV-1 pattern is not allowed under the DUP pad opening area.			
DUP.5	TV array (minimum 3*3) must be drawn between TM and TM-1 layer under the DUP pad opening area. Two Via areas whose space is within 0.70um are considered to be in the same array for 8xTV or 10xTV or LT process. It's required to follow TV space general rule 8xTVn.2b or 10xTVn.2c or LT.2b to draw TV array at the DUP pad opening area.			

Notes:

1. TM is TM2 or STM2 or MTT2 as top metal layer.
2. TM-1 is metal layer directly underneath TM layer, it can be inter-metal (1xMn/2xMn) or (TM1 or STM1).
3. TV is TV2 or STV2 or LT as top via layer. TV-1 is via layer directly underneath TV layer, it can be inter-via (1xVn/2xVn) or (TV1 or STV1).

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 192/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 193/306
---------------------------	---	------------	----------------------	-------------------

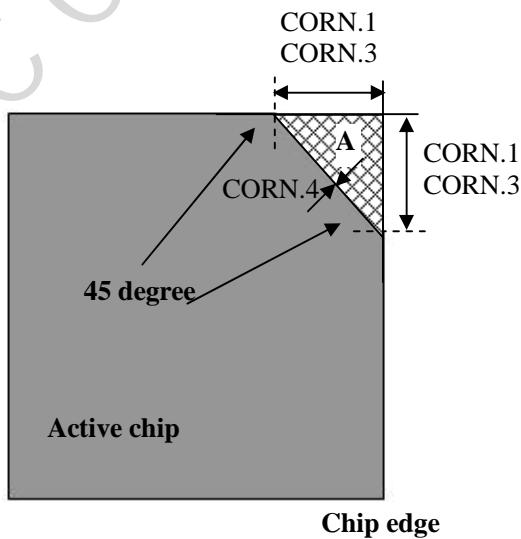
7.2.33 Chip corner design rules

This section describes the chip corner requirements to prevent the chip design interferes with seal ring.

Rule number	Description	Operation	Design Value	Unit
CORN.1	NODMF is dummy block layer for chip corner chamfer area A, and must fully cover chamfer area A.			
CORN.2	Chamfer area A size at the chip corner.	\geq	70	um
CORN.3	Chamfer area A size must be same as NODMF size.			
CORN.4	Space between NODMF and BORDER (127;0) before seal ring insertion.	=	0	um
CORN.5	The layers (listed in Note1) should not overlap with chamfer area A			

Notes:

1. The DRC executes this section rule check on following layers: AA, AADMP, DNW, NW, PSUB, LVT_N, LVT_P, DG, TG, GT, GTDMP, GTMK2, P2, SN, SP, SAB, CT, M1, 1xMn, 1xVn, 2xMn, 2xVn, 8xTVn, 8xTMn, 10xTVn, 10xTMn, LT, MTT2, PA, ALPA, MD, BORDER.
2. This rule section only applies for those chips that need have seal ring insertion. The chip corner rule check option is default turned on in DRC script.
3. In case for the building block/IP level design, or the chip level design with seal ring already inserted, please turn off the chip corner rule check option.



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 194/306
---------------------------	---	------------	----------------------	-------------------

7.2.34 BORDER(Chip edge) layer design rule

BORDER layer is used to define chip edge. Designers must draw BORDER layer following BORDER design rules below.

Rules Number	Description	Operation	Design Value	Unit
BD.1	The BORDER layer must cover the layers layout patterns (listed in Note1), which all chip layout patterns include seal ring if seal ring has been added by designers.			
BD.2	BORDER must fully cover the layers layout patterns except DNW (listed in Note1) if it needs SMIC to add seal ring.	\geq	0.32	um
BD.3	BORDER must fully cover DNW if it needs SMIC to add seal ring.	\geq	0.45	um
BD.4^[INC]	BORDER layer size should be exact same with the seal ring window edge if seal ring has been added by designers.			
BD.5	Enclosure of seal ring outer ring outline edge by BORDER layer if seal ring has been added by designers.	=	5	um
BD.6^[INC]	BORDER layer size should be exact same with chip window size in LDDI form (chip window size when tape-out).			
BD.7^[INC]	BORDER layer rules BD.1~ BD.6 are only for chip level design rules; DRC does not check IP level BORDER.			

Notes:

1. The DRC executes this section rule check on following layers: AA, AADMP, DNW, NW, PSUB, LVT_N, LVT_P, DG, TG, GT, GTDMP, GTMK2, P2, SN, SP, SAB, CT, M1, 1xMn, 1xVn, 2xMn, 2xVn, 8xTVn, 8xTMn, 10xTVn, 10xTMn, LT, MTT2, PA, ALPA, MD.
2. DRC sunset provides switch for BORDER rule DRC check, which is turn-on by default, this switch can be turn-off for IP level DRC check.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 195/306
---------------------------	---	------------	----------------------	-------------------

7.2.35 AA resistor design rules

RESAA is the marking layer for AA resistor. AA resistor must within RESAA layer. DIFRES is the LVS marking layer for AA resistor.

Non-Sicilidied AA resistor: (AA AND DIFRES) AND SAB

Sicilidied AA resistor: AA AND DIFRES

Rule Number	Description	Operation	Design Value	Unit
RESAA.1	Non-sicilidied resistor width, suggest resistor square number (length/width ratio) ≥ 1 for stable resistance.	\geq	0.4	um
RESAA.2	Non-sicilidied resistor length	\geq	0.4	um
RESAA.3	RESAA enclosure of resistor AA (RESAA CUT resistor AA) is not allowed.	\geq	0.19	um
RESAA.4	(Purposely blank)			
RESAA.5	(SN or SP) enclosure resistor AA Resistor AA CUT (SN OR SP) is not allowed.	\geq	0.1	um
RESAA.6	DIFRES enclosure of AA resistor in width direction (both for non-silicide resistor and silicide resistor)	\geq	0	um
RESAA.7	DIFRES edge should align with SAB edge along non-silicide AA resistor length direction.			
RESAA.8	DIFRES edge should align with CT edge along silicide AA resistor length direction.			
RESAA.9^[R]	It's strongly recommended space between CT and SAB for non-sicilidied AA resistor for spice model accuracy	$=$	0.12	um
RESAA.10	Space between SAB and non-related AA	\geq	0.22	um
RESAA.11	Space between SAB and non-related poly	\geq	0.3	um
RESAA.12	(Purposely blank)			
RESAA.13	Space between P+ non-silicidied AA resistor and SN Space between N+ non-silicidied AA resistor and SP	\geq	0.1	um
RESAA.14	For non-silicide AA resistor, make sure the AA is covered by SAB and implanted by either SN or SP.			
RESAA.15	AA non-silicide resistor with SP must lay on NW.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

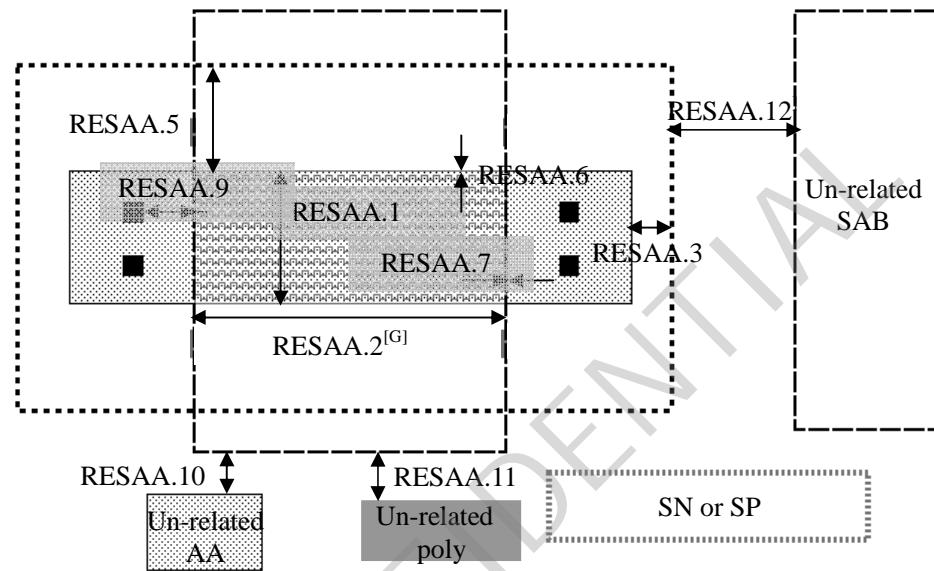
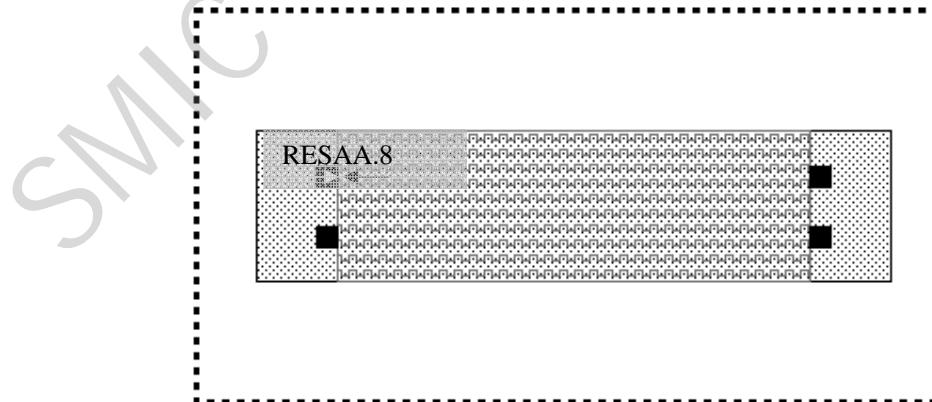


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 196/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
RESAA.16^[R]	AA resistor must be rectangular.			
RESAA.17^[R]	Recommended not use dog-bone design at the end of AA resistor for contact pick-up			
RESAA.18	It's not allowed butted SN and SP on non-silicide AA resistor.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 197/306
---------------------------	---	------------	----------------------	-------------------

Non-Silicide AA resistor**Silicide AA resistor**

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 198/306
---------------------------	---	------------	----------------------	-------------------

7.2.36 N-Well resistor design rules

RESNW layer is to define the NW resistor area where no other implantation layer except for NW. NW resistor must within RESNW layer.

7.2.36.1 NW resistor under AA design rules

NW resistor under AA: (RESNW and AA) and NW.

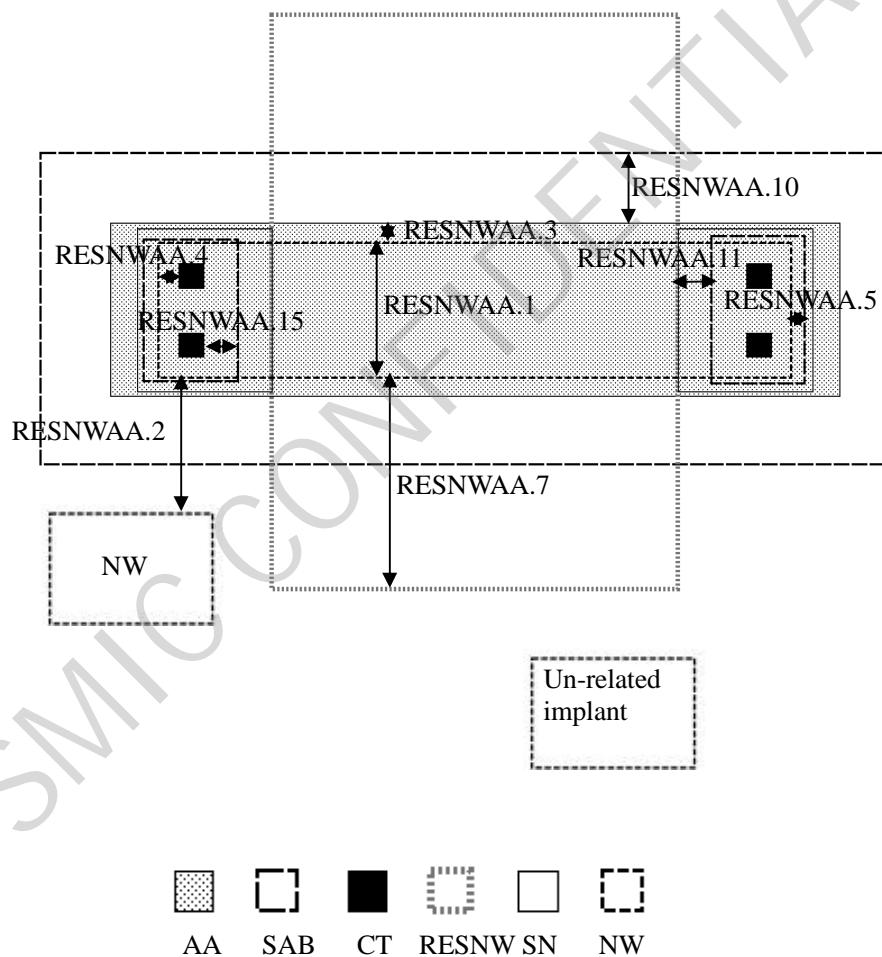
Resistor NW: NW INTERACT RESNW

Rule Number	Description	Operation	Design Value	Unit
RESNWAA.1	NW-resistor width. Suggest resistor square number (length/width ratio) ≥ 1 for stable resistance.	\geq	1.8	um
RESNWAA.2	Space between resistor NW and (resistor NW or NW).	\geq	1	um
RESNWAA.3	AA enclosure of resistor NW.	\geq	1	um
RESNWAA.4	Resistor NW enclosure of CT.	\geq	0.3	um
RESNWAA.5	Space between SAB and resistor NW.	\geq	0.3	um
RESNWAA.6	It's not allowed (AA AND RESNW) overlap with other implant layers (LVT_N/LVT_P/SP/SN) in the NW-resistor area.			
RESNWAA.7	Extension of RESNW outside of NW resistor along resistor width direction.	\geq	0.19	um
		\leq	0.5	um
RESNWAA.8	SAB must overlap with resistor NW except CT area.			
RESNWAA.9	(Purposely blank)			
RESNWAA.10	SAB enclosure of (AA NOT OUTSIDE RESNW).	\geq	0.22	um
RESNWAA.11	SAB overlap of SN	$=$	0.4	um
RESNWAA.12	NW resistor must be rectangle.			
RESNWAA.13	Only one (NW INTERACT RESNW) is allowed in one AA			
RESNWAA.14	Only two resistor N+ pickups are allowed in one NW resistor under AA.			
	Only one SAB hole in each resistor N+ pickup region is allowed.			
	The definition of resistor N+ pickup:			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 199/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
	((AA AND SN) AND (NW INTERACT RESNW))			
RESNWAA.15^[R]	Recommended space between SAB and CT	=	0.3	um



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 200/306
---------------------------	---	------------	----------------------	-------------------

7.2.36.2 NW resistor under STI design rules

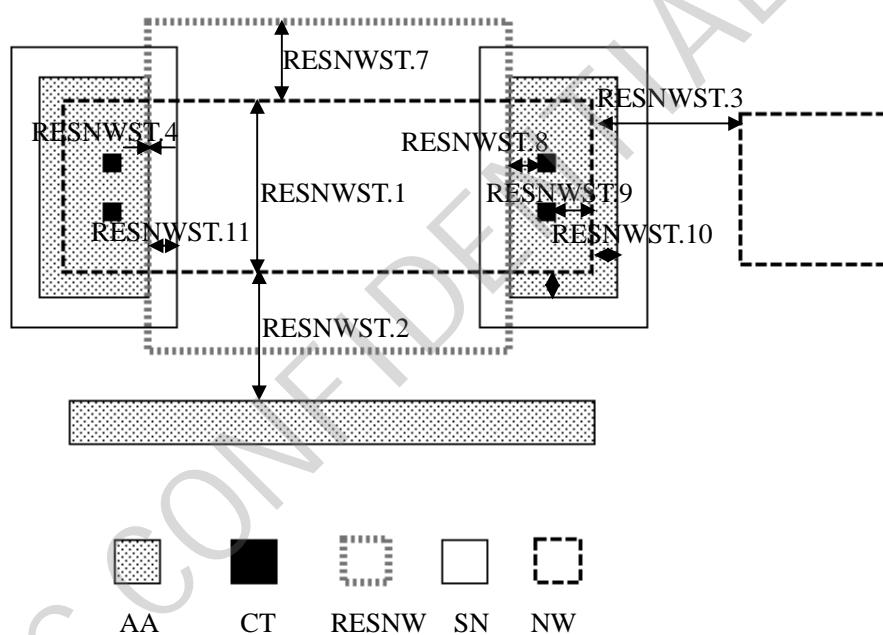
NW resistor under STI: (RESNW and NW) NOT AA.

Resistor NW: NW INTERACT RESNW

Rule Number	Description	Operation	Design Value	Unit
RESNWST.1	NW-resistor width. Suggest resistor square number length/width ratio) ≥ 1 for stable resistance.	\geq	1.8	um
RESNWST.2	Space between resistor NW and adjacent AA.	\geq	0.44	um
RESNWST.3	Space between resistor NW and (resistor NW or AA).	\geq	1	um
RESNWST.4	Space between RESNW and silicided AA area.	$=$	0	um
RESNWST.5	(Purposely blank)			
RESNWST.6	It's not allowed (SN INTERACT RESNW) overlap with LVT_P in the resistor area.			
RESNWST.7	Extension of RESNW outside of NW resistor along resistor width direction.	\geq	0.19	um
		\leq	0.5	um
RESNWST.8	AA enclosure of CT (AA INTERACT RESNW). It's strongly recommended AA enclosure of CT (AA INTERACT RESNW) =0.3um for spice model accuracy.	\geq	0.3	um
RESNWST.8^[R]	It's strongly recommended AA enclosure of CT (AA INTERACT RESNW) =0.3um along resistor length direction for spice model accuracy.	$=$	0.3	um
RESNWST.9	Resistor NW enclosure of CT.	\geq	0.3	um
RESNWST.10	AA enclosure of resistor NW	\geq	0.3	um
RESNWST.11	SN enclosure of AA.	\geq	0.4	um
RESNWST.12	NW resistor must be rectangle.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 201/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 202/306
---------------------------	---	------------	----------------------	-------------------

7.2.37 Poly resistor design rules

RESP1 is the marking layer for poly resistor. Poly resistor must within RESP1 layer. PLRES is the LVS marking layer for poly resistor.

Non-Sicilidized poly resistor: (poly AND PLRES) AND SAB

Sicilidized poly resistor: poly AND PLRES

Rule Number	Description	Operation	Design Value	Unit
RESP1.1	Non-sicilidized resistor width, suggest resistor square number (length/width ratio) ≥ 1 for stable resistance.	\geq	0.4	um
RESP1.2	Non-sicilidized resistor length	\geq	0.4	um
RESP1.3	RESP1 enclosure resistor poly. (RESP1 CUT resistor poly) is not allowed.	\geq	0.19	um
RESP1.4	SAB extension outside of non-sicilidized poly resistor along resistor width direction.	\geq	0.22	um
RESP1.5	(SN or SP) enclosure resistor poly. (SN or SP CUT resistor poly) is not allowed.	\geq	0.1	um
RESP1.6	PLRES enclosure of poly resistor in width direction (both for non-silicide resistor and silicide resistor)	\geq	0	um
RESP1.7	PLRES edge should align with SAB edge along non-silicide poly resistor length direction.			
RESP1.8	PLRES edge should align with CT edge along silicide poly resistor length direction.			
RESP1.9^[R]	It's strongly recommended space between CT and SAB for non-sicilidized poly resistor for spice model accuracy.	$=$	0.12	um
RESP1.10	Space between SAB and non-related AA	\geq	0.22	um
RESP1.11	(Purposely blank)			
RESP1.12	(Purposely blank)			
RESP1.13	Space between RESP1 and GATE in source/drain direction (overlap is not allowed)	\geq	0.165	um
RESP1.14	Space between P+ non-silicidized poly resistor and SN Space between N+ non-silicidized poly resistor and SP	\geq	0.1	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

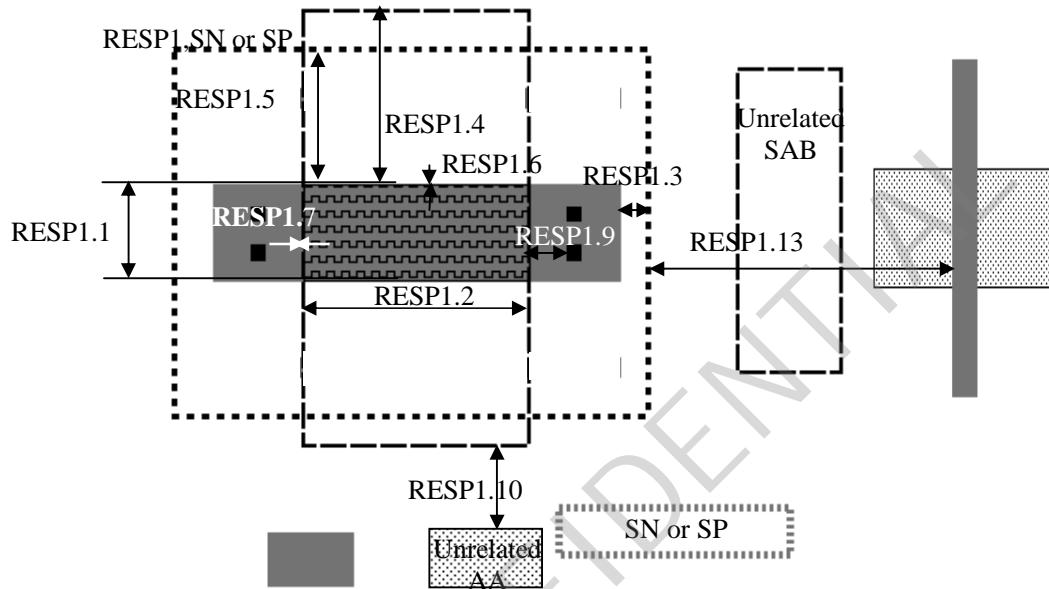
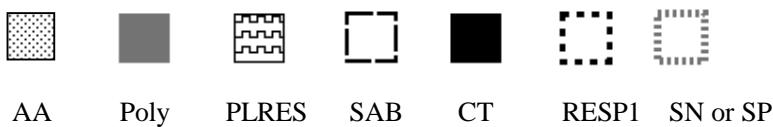
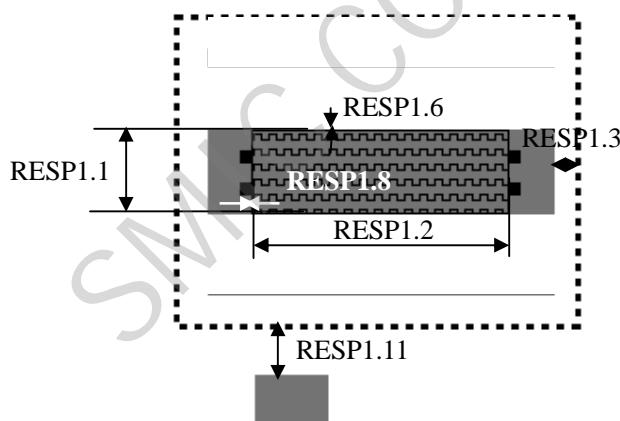


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 203/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
RESP1.15	For non-salicide poly resistor, make sure the poly is covered by SAB and implanted by either SN or SP.			
RESP1.16^[R]	Poly resistor must be rectangular.			
RESP1.17	Dog-bone design at the end of poly resistor for contact pick-up is not suggested			
RESP1.18	It's not allowed butted SN and SP on non-silicide poly resistor.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 204/306
---------------------------	---	------------	----------------------	-------------------

Non-Silicide poly resistor**Silicide poly resistor**

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 205/306
---------------------------	---	------------	----------------------	-------------------

7.2.38 Poly E-Fuse design rules

For the fuse component, it must be drawn EFUSE (81;2), GTFUSE (81;1), FUSEAD(81;4), FUSEMK1 (81;152) and marker layer.

E-fuse element is covered by EFUSE (81;2).

E-fuse function area is marked with GTFUSE (81;1).

E-fuse anode is marked with FUSEAD (81;4).

All fuse component must be fully covered by FUSEMK1 (81;152).

Rules Number	Description	Operation	Design Value	Unit
EFU.1^[NC]	FUSEMK1(81;152) must fully cover all fuse component, including EFUSE (81;2) region, program transistor, etc.			
EFU.1b	FUSEMK1 (81;152) must interact with EFUSE (81;2) region.			
EFU.1c	FUSEMK1 (81;152) must fully cover EFUSE (81;2) region.			
EFU.2a^[NC]	EFUSE (81;2) must fully cover the whole fuse element and related dummy region.			
EFU.2b	EFUSE (81;2) must interact with GTFUSE(81;1).			
EFU.2c	EFUSE (81;2) must fully cover GTFUSE(81;1).			
EFU.3^[NC]	(GTFUSE AND poly) is just the EFUSE function area.			
EFU.4^[NC]	It is strongly recommended to adopt SMIC standard efuse element, including program transistor.			
EFU.5^[NC]	If designers plan to adopt customer own design, designers must provide efuse layout to SMIC for risk assessment before design start.			
EFU.6	Space between ((GATE sizing up 0.06um) AND poly) (0.04um ≤ channel length ≤ 0.09um) and (neighboring ((poly or POLY_DMY) NOT POLY_JOG)) for core NMOS/PMOS in FUSEMK1 region. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um.	=	0.1/0.11	um
EFU.7	Space between CT and its neighboring CT (T) in EFUSE region. The definition of neighboring CT (T) : 1.CT (T) is in a CT group 2.The number of this CT group is ≥4, there are at least 3 CTs neighboring to CT (T)	≥	0.07	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 206/306
---------------------------	---	------------	----------------------	-------------------

Rules Number	Description	Operation	Design Value	Unit
	3.The space between CT (T) to other CTs in this group <0.09um.			
EFU.8	CT enclosure by (poly or GTDMP or GTDOP) when enclosure by (poly or GTDMP or GTDOP) on either perpendicular direction $\geq 0\text{um}$ in EFUSE region.	\geq	0.022	um
EFU.9	Space between 1x Vns when the run length $>-0.04\text{um}$ in FUSEMK1 region.	\geq	0.07	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 207/306
---------------------------	---	------------	----------------------	-------------------

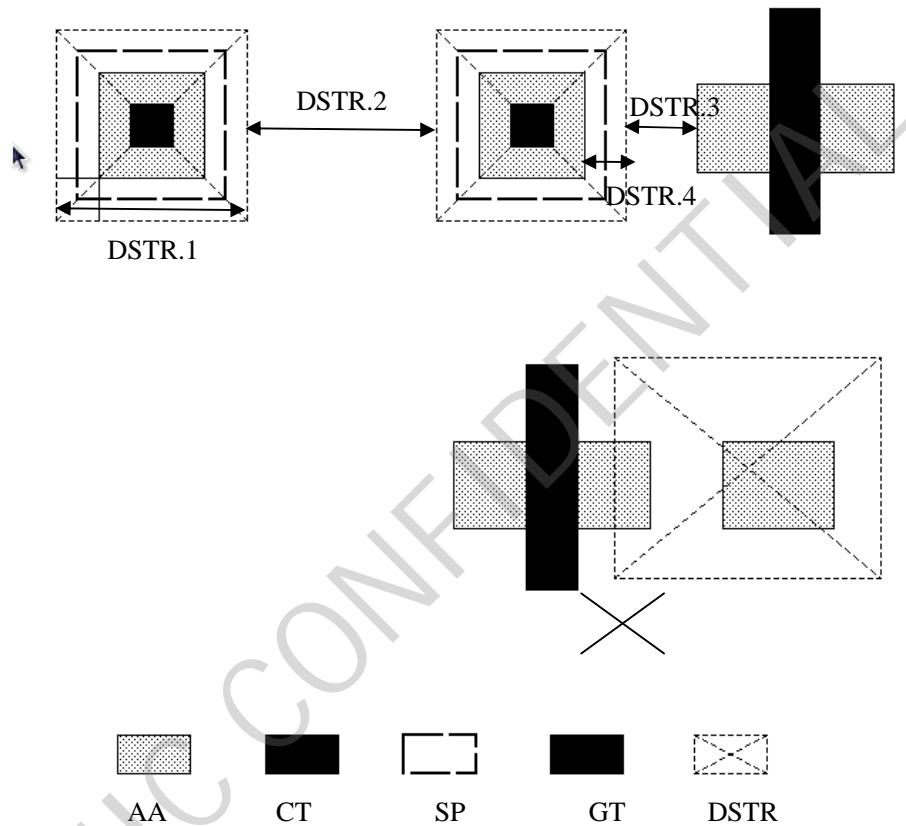
7.2.39 Diode design rules

DSTR is the marking layer for diode.

Rule Number	Description	Operation	Design Value	Unit
DSTR.1	Width of (DSTR INTERACT P+AA)	\geq	0.16	um
DSTR.2	Space between two (DSTR INTERACT P+AA)	\geq	0.16	um
DSTR.3	Space between (DSTR INTERACT P+AA) and P+AA. It's not allowed P+AA CUT DSTR.	\geq	0.065	um
DSTR.4	DSTR enclosure of P+AA,when 1. P+AA NOT INTERACT ((poly OR GTDMP) OR GTDOP), 2. P+AA NOT INTERACT RESAA, 3. P+AA INTERACT CT.	\geq	0.065	um
DSTR.5	Area of (DSTR INTERACT P+AA)	\geq	0.1	um
DSTR.6	Enclosed of (DSTR INTERACT P+AA)	\geq	0.1	um
DSTR.7	P+AA must be fully covered by DSTR in core region,when 1. P+AA NOT INTERACT ((poly OR GTDMP) OR GTDOP), 2. P+AA NOT INTERACT RESAA, 3. P+AA INTERACT CT. DRC doesn't check BIPOLA and CLPDMY region.			
DSTR.8	DSTR overlap (AA INTERACT ((poly OR GTDMP) OR GTDOP)) and AADUM is prohibited.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 208/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 209/306
---------------------------	---	------------	----------------------	-------------------

7.2.40 MOM design rules

MOM (metal oxide metal) capacitor is based on the capacitance between parallel same layer metal lines and different layer metal lines

SMIC only provided M1 and 1xMn ($n=2\sim 8$) MOM spice model and PDK. It is strongly recommended designers to use the MOM provided by SMIC PDK to have better characterization prediction and LVS check.

The CAD layers are used for MOM designs:

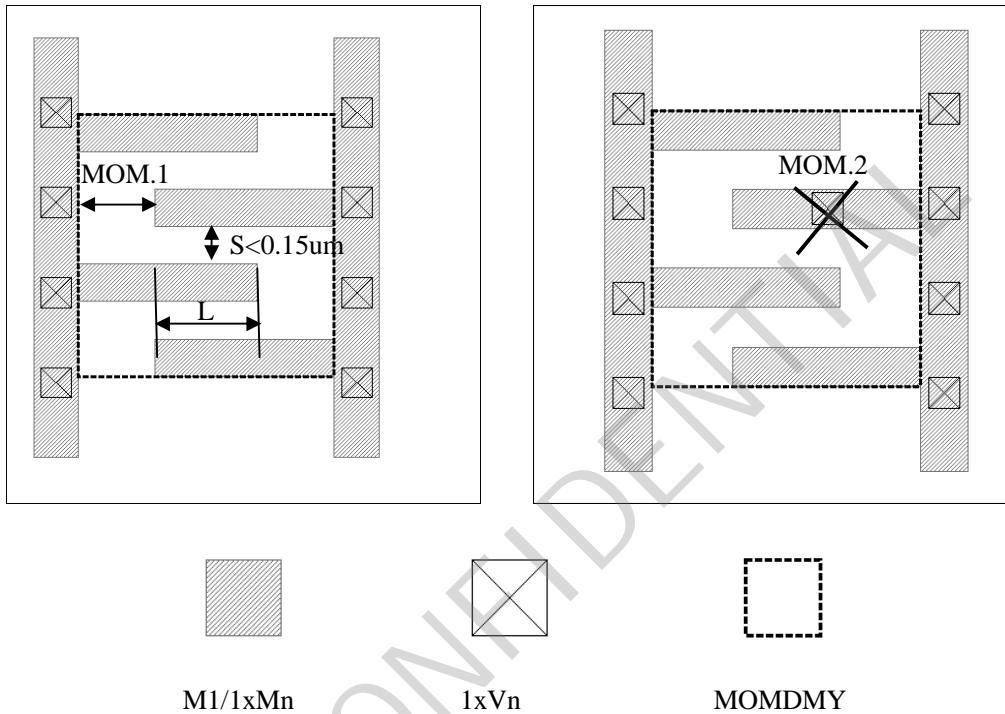
- MOMDMY (211;1) is DRC/LVS mark layer for MOM device.
- MOMTEM(211;2) LVS marking layer for MOM region
- MOMP1 (211;3) is LVS marking layer for MOM capacitor mesh terminal one
- MOMP2 (211;4) is LVS marking layer for MOM capacitor mesh terminal two
- MOMMES (211;5) is LVS marking layer for MOM mesh capacitor
- RFMOM (211;6) is LVS marking layer for RF MOM capacitor
- RF3T (183;2) is DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM

Dummy block layer MnDUB ($n=1\sim 8$) are applied in SMIC inductor designs with pre-inserted dummy. So SMIC dummy script will block out MOM region for auto dummy insertion

Rules number	Description	Operation	Design Value	Unit
MOM. 1	Space between M1/1xMn line-end and M1/1xMn in MOMDMY region M1/1x Mn line-end definition: M1/1x Mn edge with length $< 0.07\mu m$ (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 $\geq 0.05\mu m$.	\geq	0.1	um
MOM.2 ^[NC]	It is not allowed 1xVn (connecting to 1xMn of MOM structures) overlap with MOMDMY			
MOM.3 ^[NC]	Each MOM cell must be covered by MOMDMY(211;1).			
MOM.4 ^[NC]	Use symmetrical dummy metal around the matched pairs of MOM cells instead of auto inserted dummy.			
MOM.5 ^[NC]	Active device underneath or above MOM cell should be put into couple capacitance consideration in design.			
MOM.6	Sidewall area of total metals (M1 and 1xMn) in MOMDMY. For the definition of the sidewall area: (metal length in MOMDMY (L)) * metal thickness. (Pls refer metal option table for metal thickness); Total sidewall area is to calculate the area of (finger number-1). DRC check MOM sidewall area when metal space S<0.15um.	\leq	9.00E+06	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 210/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 211/306
---------------------------	---	------------	----------------------	-------------------

7.2.41 LOGO design rules

Rules number	Description	Operation	Design Value	Unit
LOGO.1	Space between LOGO and (AA/poly/M1/1xMn/2xMn/8xTMn /10TMn/MMT2/ALPA OUTSIDE LOGO).	\geq	10	um
LOGO.2	It's not allowed LOGO overlap with PA.			
LOGO.3^[NC]	It's not allowed a circuit is in the LOGO.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 212/306
---------------------------	---	------------	----------------------	-------------------

7.2.42 Metal low density design rules

LDNMK1 (131;170) is used for metal low density (M1/1xMn) region such as LOGO etc.

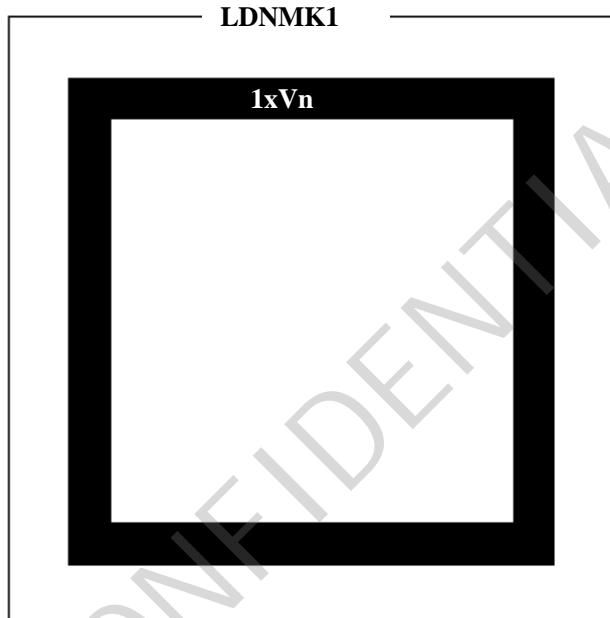
1xVn bar definition: 1xVn polygon with width=0.15um.

Rule number	Description	Operation	Design Value	Unit
LDNMK1.1	Width of M1 or M1DOP within LDNMK1 region.	\geq	0.14	um
LDNMK1.2	Width of M1DUM within LDNMK1 region.	\geq	0.12	um
LDNMK1.3	Width of 1xMn or MnDOP within LDNMK1 region.	\geq	0.14	um
LDNMK1.4	Width of 1xMn dummy within LDNMK1 region.	\geq	0.12	um
LDNMK1.5	Space between M1/M1DOP and M1/M1DOP within LDNMK1 region	\geq	0.14	um
LDNMK1.6	Space between M1DUM and M1DUM within LDNMK1 region	\geq	0.12	um
LDNMK1.7	Space between 1xMn/1xMnDOP (n=2~8) and 1xMn/1xMnDOP (n=2~8) within LDNMK1 region.	\geq	0.14	um
LDNMK1.8	Space between 1xMnDUM(n=2~8) and 1xMnDUM(n=2~8) within LDNMK1 region.	\geq	0.12	um
LDNMK1.9	Guardring(MARKG) must be put in the region (LDNMK1 NOT (LDNMK1 sizing down 1um))			
LDNMK1.10	1xVn bar must be continuous as a ring within (LDNMK1 NOT (LDNMK1 sizing down 4um)). DRC doesn't check when (LDNMK1 INTERACT INDMY)).			
LDNMK1.11	1xVn bar is allowed in (LDNMK1 NOT (LDNMK1 sizing down 4um)).			
LDNMK1.12	Width of 1xVn bar in guard ring	$=$	0.15	um
LDNMK1.13	Space between 1xVn bar in LDNMK1 and 1xVn/1xRVn	\geq	0.35	um
LDNMK1.14	Space between 1xVn bar and 1xVn bar within LDNMK1	\geq	0.6	um
LDNMK1.15	1xVn bar enclosure by M1/1xMn(n=1~8) within LDNMK1	\geq	0.1	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 213/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 214/306
---------------------------	---	------------	----------------------	-------------------

7.2.43 Antenna Ratio Effect rules

The "Antenna Ratio Effect" is a common name for the effects of charge accumulation in isolated nodes of an integrated circuit during its processing. This effect is also sometimes called "Plasma Induced Damage"(PID) or "charging effect". In those cases that the discharging of the isolated nodes is done through the thin gate oxide of the transistor, it might cause damage to the transistors and degrade their performance.

Antenna Ratio effect generic prevention rules are intended to reduce gate oxide damage, which was caused when exposed polysilicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler-Nordheim tunneling current to flow through the oxide during high density plasma processing in chip fabrication. Given the known process charge fluence, a figure of exposed conductor area to transistor gate area ratio is determined which guarantees Gate Oxide Integrity (GOI) reliability requirements. Failure to consider antenna rules in a design may lead to either reduced performance in transistors exposed to process induced damage, or may lead to total failure if the antenna rules are seriously violated.

Rule Number	Description	Operation	Design Value	Unit
ANT.GT1	Drawn ratio of field (poly NOT P2) perimeter area to the active poly gate area (1.05VCore, 1.8V/2.5V IO)connected directly to it	\leq	500	
ANT.GT2	Drawn ratio of field (poly NOT P2) top area to the active poly gate area (1.05VCore, 1.8V/2.5V IO) connected directly to it	\leq	250	
ANT.GT3	Drawn ratio of CT area to the active poly gate area (1.05VCore, 1.8V/2.5V IO) connected directly to it	\leq	10	
ANT.GT4a	When a protection diode is not used, the ratio of cumulative metal area to the active poly gate area (1.05V Core, 2.5VIO) from M1 to TM (if double TM used, TM layer defined as TM2 layer)	\leq	5000	
ANT.GT4b	When a protection diode is not used, the ratio of cumulative metal area to the active poly gate area (1.8V IO) from M1 to TM (if double TM used, TM layer defined as TM2 layer)	\leq	1000	
ANT.GT5a	When a protection diode is used, the ratio of cumulative M1 to Mn (Mn is inter metal layer directly underneath TM2) area to the active poly gate area (1.05VCore, 1.8V/2.5V IO)connected directly to it	\leq	diode area*500 + 44000	
ANT.GT5b	When a protection diode is used, the ratio of cumulative TM _n (n=1,2) area to the active poly gate area (1.05VCore, 1.8V/2.5V IO) connected directly to it	\leq	diode area*998 4+55000	
ANT.GT6a	When the protection diode is not used, the drawn ratio of single layer Via area to the active poly gate area (1.05VCore, 1.8V/2.5V IO) connected directly to it	\leq	20	
ANT.GT6b	When the protection diode is not used, the drawn ratio of cumulative Via area to the active poly gate area (1.05VCore, 1.8V/2.5V IO) connected directly to it	\leq	50	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 215/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
ANT.GT7	When the protection diode is used, the drawn ratio of cumulative Via area to the active poly gate area (1.05VCore, 1.8V/2.5V IO)connected directly to it	\leq	diode area * 200 + 1000	
ANT.GT8a	When the protection diode is not used, the drawn ratio of PA area to the active poly gate area (1.8V/2.5V IO) connected directly to it	\leq	20	
ANT.GT8b	When the protection diode is not used, the drawn ratio of PA area to the active poly gate area (1.05V Core) connected directly to it	\leq	200	
ANT.GT9a	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the active poly gate area (1.8V/2.5V IO) connected directly to it. ALPA has two kinds of thickness (14.5K and 28K) for each metal option.	\leq	1000	
ANT.GT9b	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the active poly gate area (1.05V Core) connected directly to it. ALPA has two kinds of thickness (14.5K and 28K) for each metal option.	\leq	2000	
ANT.GT10	When the protection diode is used, the drawn ratio of PA area to the active poly gate area (1.05V Core, 1.8V/2.5V IO) connected directly to it	\leq	diode area * 100 + 400	
ANT.GT11	When the protection diode is used, the drawn ratio of ALPA side-wall area to the active poly gate area (1.05V Core, 1.8V/2.5V IO) connected directly to it. ALPA has two kinds of thickness (14.5K and 28K) for each metal option.	\leq	diode area * 8500 + 30000	
ANT.GT12	Area ratio of ((M1 or 1xMn) to upper 1xVn) in the same net,when M1 or 1xMn connects to gate with area > 10000um ² and doesn't connect to AA.	\leq	300000	
ANT.GT13	Area ratio of ((1xMn or 2xMn) to upper 2xVn) in the same net,when 1xMn or 2xMn connects to gate with area > 10000um ² and doesn't connect to AA.	\leq	300000	
ANT.GT14	Area ratio of ((1xMn or 2xMn or 8xTMn) or to upper 8xTVn) in the same net,when (1xMn or 2xMn or 8xTMn) connects to gate with	\leq	300000	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 216/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
	area > 10000um ² and doesn't connect to AA.			
ANT.GT15	Area ratio of ((1xMn or 2xMn or 10xTMn) or to upper 10xTVn) in the same net,when (1xMn or 2xMn or 10xTMn) connects to gate with area > 10000um ² and doesn't connect to AA.	\leq	300000	

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 217/306
---------------------------	---	------------	----------------------	-------------------

A. The definition of Field Poly Perimeter antenna ratio

$$\text{Ratio} = 2[(L+W1)x t] / (W2 \times l)$$

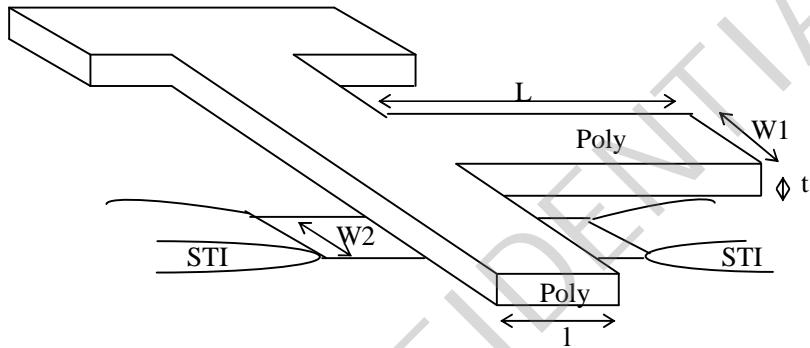
L : floating field poly length connected to gate

W1 : floating field poly width connected to gate

t : field poly thickness (poly thickness is 700A)

W2 : connected transistor channel width

l : connected transistor channel length

**B. The definition of Field Poly Top Area antenna ratio is**

$$\text{Ratio} = (\text{Apoly}) / (W2 \times l)$$

Apoly : Effective poly area that is electrically connected to gate.

C. The definition of CT, Via1-Via7 antenna ratio is

$$\text{Ratio} = \{\text{total CT (Via) area}\} / (W2 \times l)$$

D. The definition of Cumulative Metal antenna ratio is

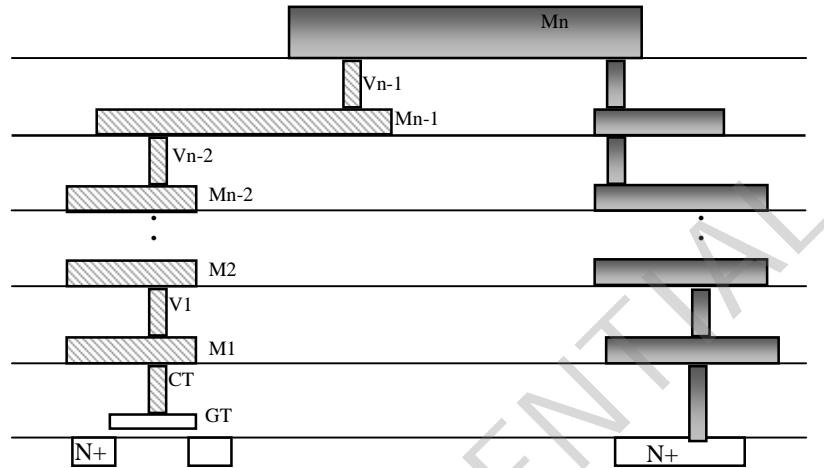
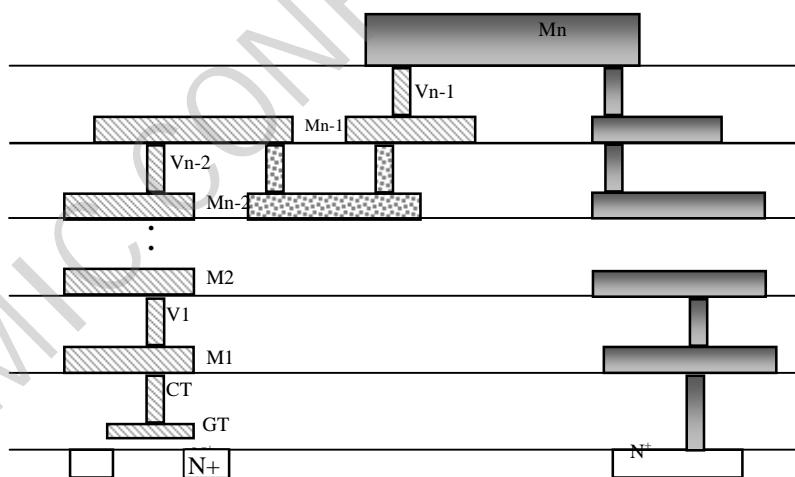
$$\text{Ratio} = (\text{AM1} + \dots) / (W2 \times l)$$

AMx : Effective metal(x) area that is electrically connected to gate without using Metal(x+1), and not to connected to active area. Cumulative Metal antenna ratio is relative to total effective metal layer area.

Note: if the metal area is connected to the poly which is cut from active poly gate by using P2 layer, that is, the metal area is not electrically connected to active poly gate. It will not take into account for metal antenna ratio calculation.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 218/306
---------------------------	---	------------	----------------------	-------------------

•In case of n-level metal (I)**•In case of n-level of metal (II)**

E. The definition of the effective diode area is:
((SN OR SP) AND AA) NOT poly

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 219/306
---------------------------	---	------------	----------------------	-------------------

7.2.44 SRAM marking layer design rules

Customers must use SMIC provided standard SRAM bit cells, customer-designed SRAM bit cells are not allowed to tape-out in SMIC.

SRAM related marking layer INST and other bit cell marking layers must follow the design rules in this section.

Rules Number	Description	Operation	Design Value	Unit
SRAM.1^[NC]	INST (60;0) is the marking layer of SRAM area.			
SRAM.2^[NC]	INST is required to cover all SRAM cells which include bit cells, strap cells, edge cells (or dummy cells) and tracking cells.			
SRAM.3^[NC]	Edges of INST layer must be aligned with the boundary of SRAM cell arrays.			
SRAM.4^[NC]	The area covered by INST is required to follow SRAM rules.			
SRAM.5^[NC]	The area covered by INST is required to follow the general rules if it isn't defined in SRAM rules.			
SRAM.6^[NC]	Bit cell marking layer (STSRAM, DPSRAM, LRSRAM, 2PSRAM) for each type SRAM cell is must for LVS purpose. Those marking layers (STSRAM, DPSRAM, LRSRAM, 2PSRAM) must cover all SRAM cells which include bit cells, strap cells, edge cells (or dummy cells) and tracking cells (see Figure1 below).			
SRAM.7	Edges of bit cell marking layer (STSRAM, DPSRAM, LRSRAM, 2PSRAM) are required to be aligned with INST layer edges.			
SRAM.8	If the gate is covered by INST layer, it should be also covered by bit cell marking layers (STSRAM, DPSRAM, LRSRAM, 2PSRAM).			
SRAM.9	If the area is covered by bit cell marking layers (STSRAM, DPSRAM, LRSRAM, 2PSRAM), it should be also covered by INST layer.			
SRAM.10	HPBL is the marking layer for low voltage SRAM, the edge of HPBL layer must be aligned with the boundary of STSRAM, DPSRAM, LRSRAM, 2PSRAM.			
SRAM.11	INST width	≥	0.16	um
SRAM.12	INST space	≥	0.16	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 220/306
---------------------------	---	------------	----------------------	-------------------

Rules Number	Description	Operation	Design Value	Unit
SRAM.13	Space between INST and (GATE NOT INTERACT INST)	\geq	0.115	um
SRAM.14	INST enclosure GATE along source/drain direction	\geq	0.115	um
SRAM.15	INST enclosure GATE along poly length direction	\geq	0.065	um
SRAM.16	INST extension outside of NW (NW interact AA). Extension=0um is allowed.	\geq	0.16	um
SRAM.17	Overlap of INST and NW (NW interact AA). Overlap=0um is allowed.	\geq	0.16	um
SRAM.18	It's not allowed (AA, CT and V1) cut INST.			
SRAM.19	It's not allowed P2 cut INST.			
SRAM.20	GATE direction must be same in INST region.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 221/306
---------------------------	---	------------	----------------------	-------------------

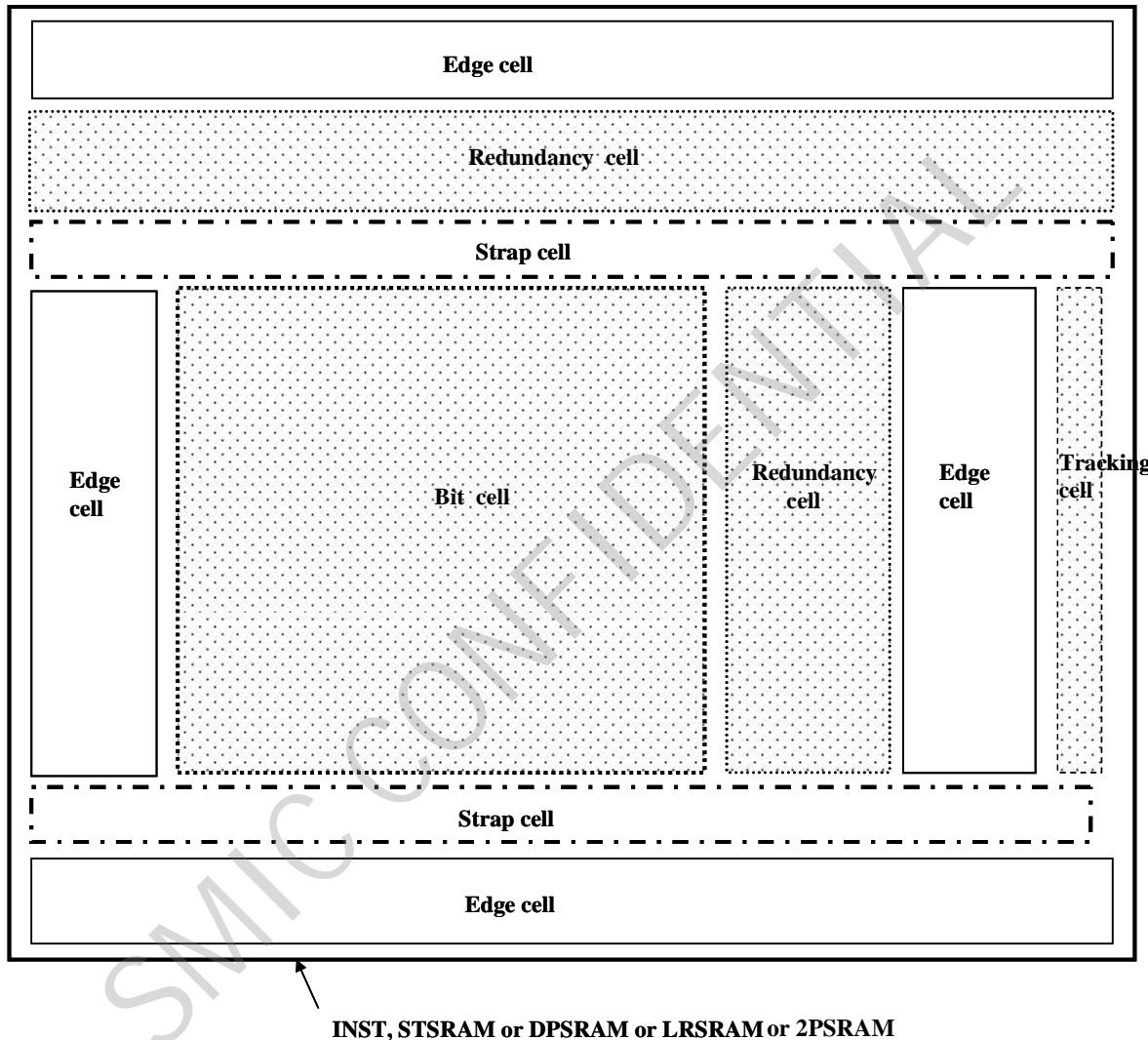


Figure1 SRAM marking layer figure

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 222/306
---------------------------	---	------------	----------------------	-------------------

7.3 Layout Guideline

7.3.1 Varactor layout guidelines

VARMOS is the marking layer varactor device.

Rules Number	Description	Operation	Design Value	Unit
VAR.1 ^[G]	Channel length of core varactor MOS	≥	0.2	um
		≤	10	um
VAR.2 ^[G]	Channel length of I/O varactor MOS	≥	0.2	um
		≤	10	um
VAR.3 ^[G]	Channel width of varactor MOS	≥	0.4	um
VAR.4 ^[G]	Space between (poly or POLY_DMY) and neighboring GATE for core device in VARMOS	≥	0.12	um
VAR.5 ^[G]	(Purposely blank)			
VAR.6 ^[G]	(Purposely blank)			
VAR.7 ^[G]	Space between VARMOS and GATE	≥	0.16	um
VAR.8 ^[G]	VARMOS enclosure AA	≥	0.16	um
VAR.9 ^[G]	SN fully enclosure (GATE AND VARMOS) AND NW along the channel length direction	≥	0.32	um
VAR.10 ^[G]	SN fully enclosure (GATE AND VARMOS) AND NW along the channel width direction	≥	0.13	um
VAR.11 ^[G]	SP fully enclosure (GATE AND VARMOS) NOT NW along the channel length direction	≥	0.32	um
VAR.12 ^[G]	SP fully enclosure (GATE AND VARMOS) NOT NW along the channel width direction	≥	0.13	um
VAR.13 ^[G]	(Purposely blank)			
VAR.14 ^[G]	AA extension outside of (poly or POLY_DMY) for VARMOS core device	≥	0.095	um
VAR.15 ^[G]	(Purposely blank)			
VAR.16 ^[G]	SN extension outside of VARMOS. Extension = 0um is allowed.	≥	0.16	um
VAR.17 ^[G]	SP extension outside of VARMOS. Extension = 0um is allowed.	≥	0.16	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

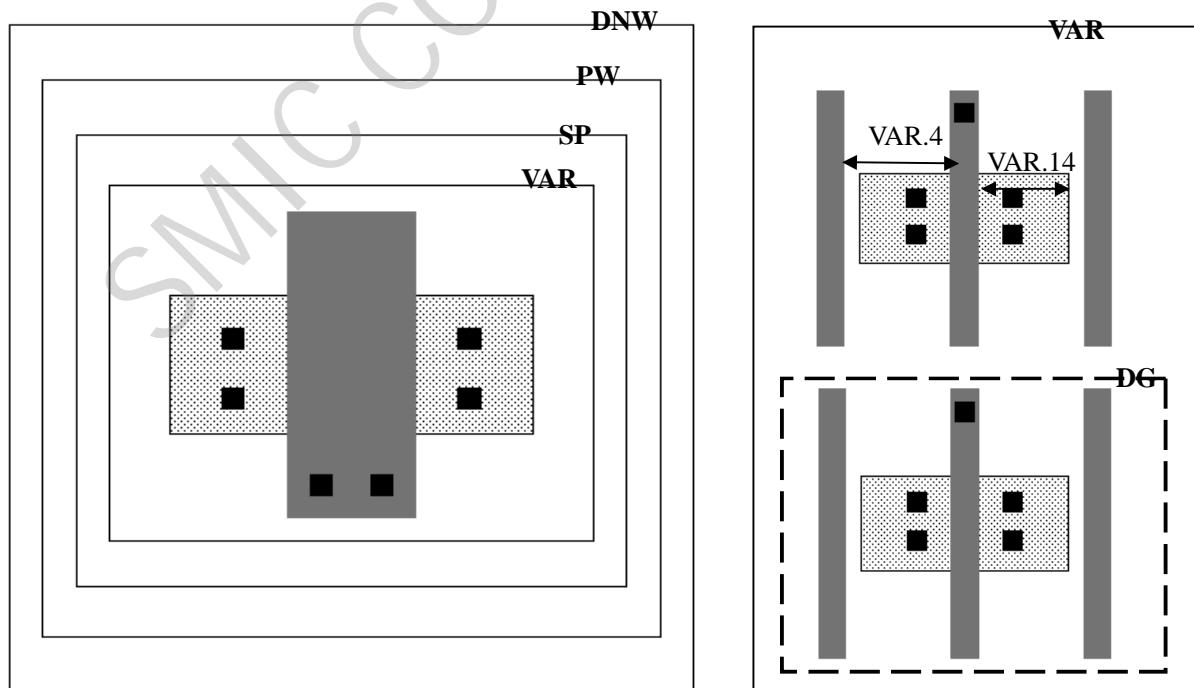
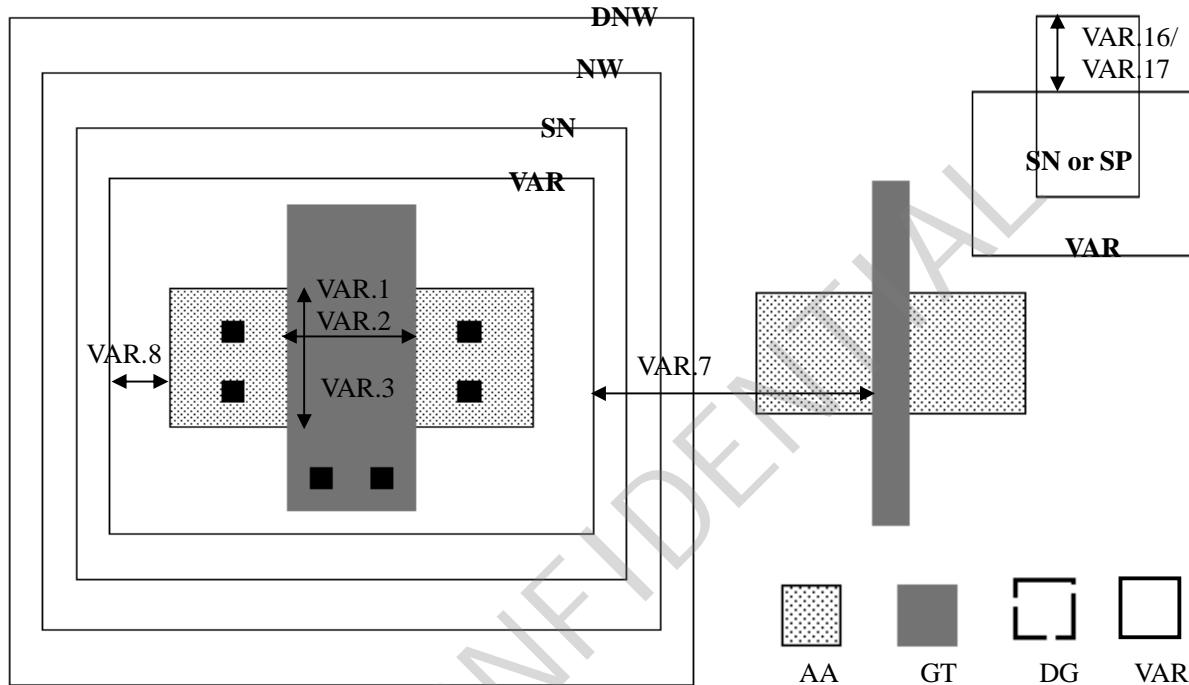


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 223/306
---------------------------	---	------------	----------------------	-------------------

Rules Number	Description	Operation	Design Value	Unit
VAR.18^[G]	VARMOS marking layer must be drawn to fully cover the varactor devices. Definition of varactor devices: GATE NOT OUTSIDE VARMOS.			
VAR.19^[G]	It's not allowed VARMOS overlap LVT_N,LVT_P, PSUB, SAB.			
VAR.20^[G]	It's not allowed SP overlap (GATE AND NW) AND VARMOS).			
VAR.21^[G]	It's not allowed SN overlap (GATE NOT NW) AND VARMOS).			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	TD-LO28-DR-2006	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	2	Tech Dev Rev:	1.10.1	Page No.:	224/306
-----------	-----------------	-------------	--	----------	---	---------------	--------	-----------	---------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 225/306
---------------------------	---	------------	----------------------	-------------------

7.3.2 BIPOLA layout guidelines

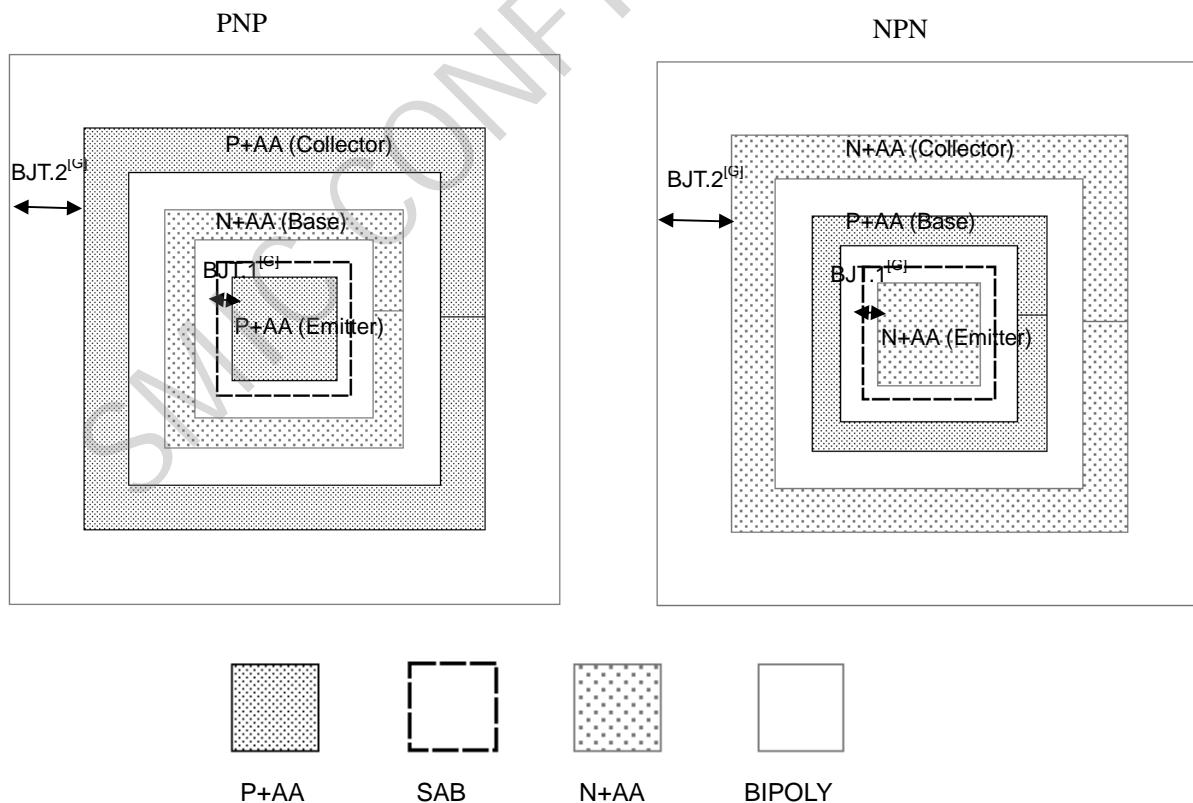
SMIC provide two kinds of vertical bipolar, PNP bipolar (P+/NW) and NPN bipolar (N+/PW/DNW).

Emitter AA definition: (N+AA INSIDE BIPOLA) for NPN bipolar or (P+ AA INSIDE BIPOLA) for PNP bipolar

Collector AA definition: (N+ pickup AA INSIDE BIPOLA) for NPN bipolar or (P+ pickup AA INSIDE BIPOLA) for PNP bipolar

Base AA definition: (P+ pickup AA INSIDE BIPOLA) for NPN bipolar or (N+ pickup AA INSIDE BIPOLA) for PNP bipolar

Rules Number	Description	Operation	Design Value	Unit
BJT.1^[G]	SAB enclosure Emitter AA	≥	0.3	um
BJT.2^[G]	BIPOLA enclosure of Collector AA	≥	1	um
BJT.3^[G]	BIPOLA overlap of PSUB, poly, LVT_N,LVT_P, VARMOS, and INST is prohibited.			



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 226/306
---------------------------	---	------------	----------------------	-------------------

7.3.3 Inductor design guidelines

SMIC provide inductor spice model and PDK, to have better device characterization prediction and LVS check, it is recommended to use SMIC PDK.

The inductor devices must be covered by inductor marking layer INDMY (212;0). INDMY should not be used for other purpose than inductor device.

Dummy block layer DUMBA/ DUMB/PUMB are applied in SMIC inductor designs. So SMIC dummy script will block out inductor region for auto dummy insertion.

Rules number	Description	Operation	Design Value	Unit
IND.1^[G]	M1, M1DUM, and M1DOP width in INDMY.	\geq	0.28	um
IND.2^[G]	1xMn, 1xMnDUM, and 1xMnDOP width in INDMY	\geq	0.28	um
IND.3^[G]	2xMn, 2xMnDUM, and 2xMnDOP width in INDMY	\geq	0.8	um
IND.4^[G]	8xTMn and 8xTMnDUM width in INDMY	\geq	0.75	um
		\leq	30	um
IND.5^[G]	10xTMn and 10xTMnDUM width in INDMY	\geq	0.75	um
		\leq	30	um
IND.6^[G]	MTT2 and MTT2DM width in INDMY	\geq	2	um
		\leq	30	um
IND.7^[G]	INDMY width or length	\leq	580	um
IND.8^[G]	M1, M1DUM, and M1DOP space in INDMY	\geq	0.28	um
IND.9^[G]	1xMn, 1xMnDUM, and 1xMnDOP space in INDMY	\geq	0.28	um
IND.10^[G]	2xMn, 2xMnDUM, and 2xMnDOP space in INDMY	\geq	0.4	um
IND.11^[G]	8xTMn, 8xTMnDUM space in INDMY	\geq	0.75	um
IND.12^[G]	10xTMn and 10xTMnDUM space in INDMY	\geq	0.75	um
IND.13^[G]	MTT2 and MTT2DM space in INDMY	\geq	1	um
IND.14^[G]	8xTMn and 8xTMnDUM /10xTMn and 10xTMnDUM /MTT2 and MTT2DM space in INDMY when at least one metal line width > 12um and the parallel run length > 12um	\geq	2	um
IND.15^[G]	Space between MTT2/8xTMn /10xTMn / ALPA (as Inductor) and other MTT2/8xTMn /10xTMn/ALPA outside of INDMY.	\geq	30	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 227/306
---------------------------	---	------------	----------------------	-------------------

Rules number	Description	Operation	Design Value	Unit
IND.16^[G]	INDMY extension outside of M1/1xMn/2xMn/MMT2/8xTMn /10xTMn/ALPA metal designs.	\geq	15	um
IND.17^[G]	Space between active device and INDMY. Active device is all devices in device truth table.	\geq	10	um
IND.18^[G]	INDMY density in full chip	\leq	4%	
IND.19^[G]	M1/1xMx/2xMn/8xTMn/10xTMn metal density in full chip (include dummy pattern)	\geq	20%	
IND.20^[G]	INDMY density. DRc check window size 1600*1600um, step size: 800um	\leq	10%	
IND.21^[G]	There should be at least four 8xTVn with space \leq 1.7um to connect (two 8xTMn layers) or (8xTMn to 1xMn) or (8xTMn to 2xMn) in INDMY			
IND.22^[G]	There should be at least four 10xTVn with space \leq 1.7um to connect (two 10xTMn layers) or (10xTMn to 1xMn) or (10xTMn to 1xMn) in INDMY			
IND.23^[G]	There should be at least four UTV(LT) with space \leq 1.7um to connect (MTT2 to 8xMn) or (MTT2 to 2xMn) or (MTT2 to 1xMn) in INDMY			
IND.24^[G]	(Purposely blank)			
IND.25^[G]	All devices listed in device table inside INDMY region are prohibited.			
IND.26^{[G][R]}	It is recommended PSUB fully covers the inductor coil and guardring to achieve the high quality. DRC check method: PSUB fully cover ((AA INTERACT INDMY) INTERACT SP)).			
IND.27^{[G][NC]}	Do not allow non-inductor related layouts within INDMY. Only the patterns been put into inductor characterization allowed.			
IND.28^{[G][NC]}	Make the inductor regions within chip to be evenly spread to have balanced pattern density.			
IND.29^{[G][NC]}	Inductor components (including inductor circuit, guard ring, dummy patterns) must be covered by INDMY layer.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 228/306
---------------------------	---	------------	----------------------	-------------------

Rules number	Description	Operation	Design Value	Unit
IND.30^{[G][NC]}	MGBL layer is must for inductor device with shielding to reserve poly during process, it is forbidden to draw MGBL under inductor device without shielding.			
IND.31^[G]	It allows 0.01um checking tolerance in IND MY region for rule IND.1-26.			
IND.32^[G]	It allows 0.01um checking tolerance in IND MY region for rule PA.1-4, ALPA.1-2. It allows 0.06um ² checking tolerance in IND MY region for MTT2.6 and MTT2.7.			

Note:

1. For all device DRC check in IND.25^[G], DRC follows device marking layer to check diode, MOM, Bipola, VARMOS, resistor,etc. For MOS device, the definition is for DRC identify as below:

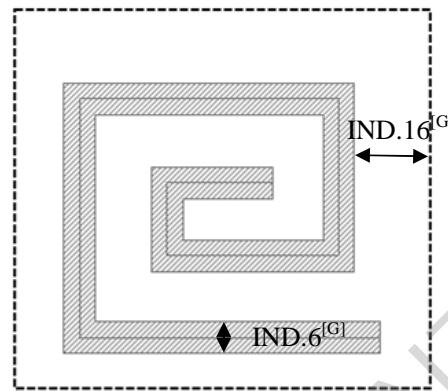
GATE0 = (poly AND AA)

AA1 = (AA INTERACT GATE0) NOT GATE0

MOS = GATE0 TOUCH AA1 == 2

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 229/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 230/306
---------------------------	---	------------	----------------------	-------------------

7.3.4 LDMOS layout guideline

LDBK layer is the mark layer to identify LDMOS area. The LDMOS described here is covered by DG and LDBK layers. It is parasitical device of 1.8V IO. The LDMOS follows 1.8V IO related design rules and the rules described below. The drain side is for 5V operation; the GATE side with 1.8V operation voltage; the source side is connected to ground.

Rule No	Description	Operation	Design value	Unit
LD.1a^[G]	Effective channel length(Leff) for NLDMOS transistors	\geq	0.22	um
LD.1b^[G]	Effective channel length(Leff) for PLDMOS transistors	\geq	0.2	um
LD.2^[G]	Drain AA width (LD) along source/drain direction for LDMOS transistors	\geq	0.2	um
LD.3^[G]	STI width along source/drain direction	$=$	0.15	um
LD.4^[G]	Overlap of poly and STI along source/drain direction	\geq	0.05	um
LD.5^[G]	NLDMOS GATE overlaps with NW in source/drain direction length. PLDMOS GATE not in NW in source/drain direction length	$=$	0.2	um
LD.6^[G]	LDMOS channel width	\geq	2	um
LD.7a^[G]	Space between LDMOS source side AA and pickup AA along source/drain direction	\geq	0.6	um
LD.7b^[G]	Space between LDMOS source/drain side AA and pickup AA along GATE poly direction	\geq	0.8	um
LD.8^[G]	NW extension outside of N LDMOS AA along GATE poly direction. NW space to P LDMOS AA along gate poly direction	\geq	0.25	um
LD.9a^[G]	Space between NW in LDBK region and P+ pickup AA.	\geq	0.065	um
LD.9b^[G]	Space between ((NW hole INSIDE DNW) in LDBK region and N+ pickup AA.	\geq	0.25	um
LD.10^[G]	LDBK extension outside of (GATE, source, drain)'s AA	\geq	0.4	um
LD.11^[G]	Space between one LDMOS GATE poly to another LDMOS GATE poly on source side	\geq	0.18	um
LD.12^[G]	One LDMOS unit must has two polys and a common drain. Single poly structure is not allowed.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 231/306
---------------------------	---	------------	----------------------	-------------------

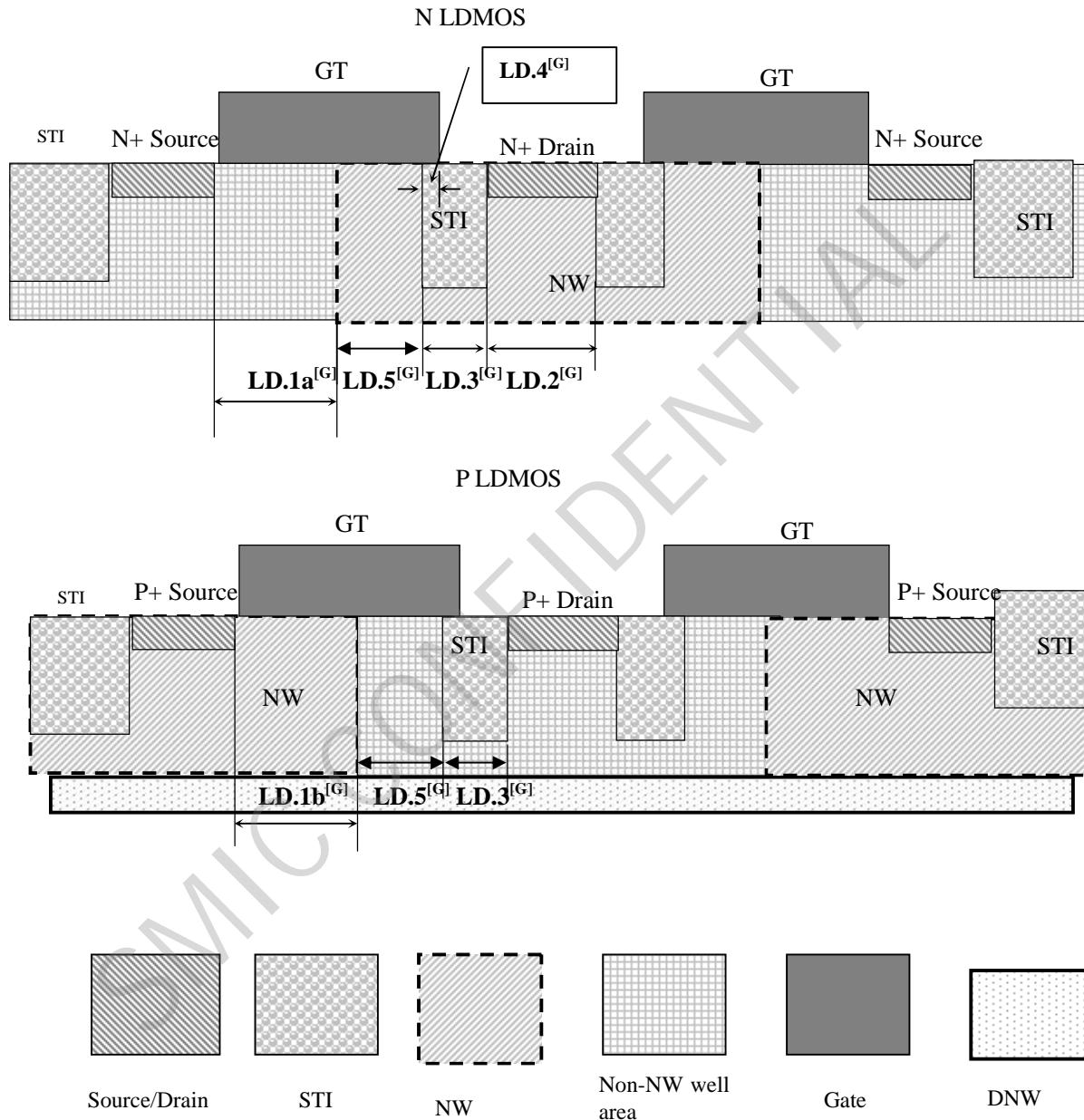
LD.13 ^{[G][R]}	Common source is allowed only for multi-finger LDMOS structure in LDBK region.(Drain/Source/GATE is connected together respectively.)			
-------------------------	---	--	--	--

Note:

1. Effective channel length(L_{eff}):
 - a) NLDMOS effective channel length: GT not in NW part channel length in source/drain direction
 - b) PLDMOS effective channel length: GT in NW part channel length in source/drain direction

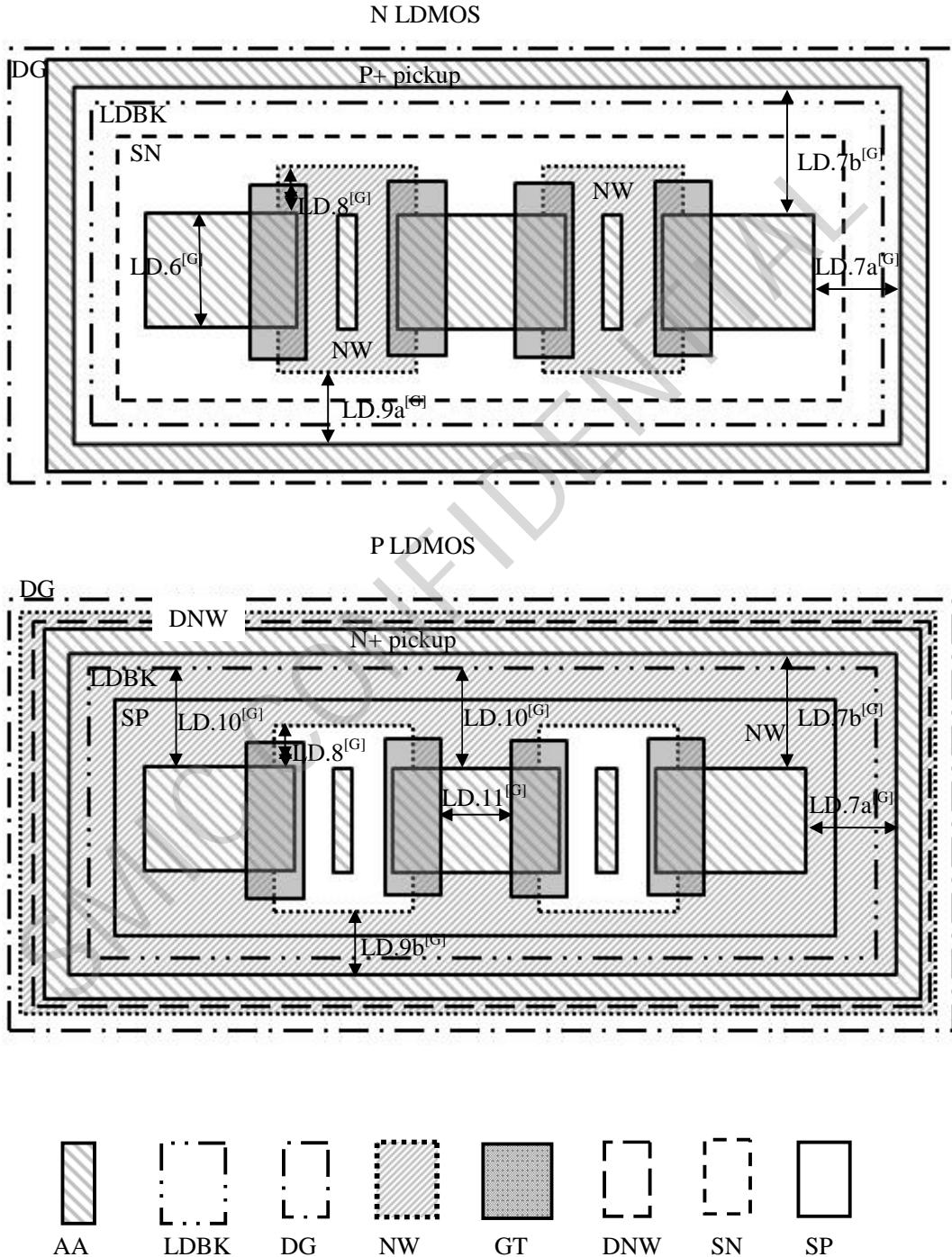
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	TD-LO28-DR-2006	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev:	2	Tech Dev Rev:	1.10.1	Page No.:	232/306
-----------	-----------------	-------------	--	-----------	---	---------------	--------	-----------	---------



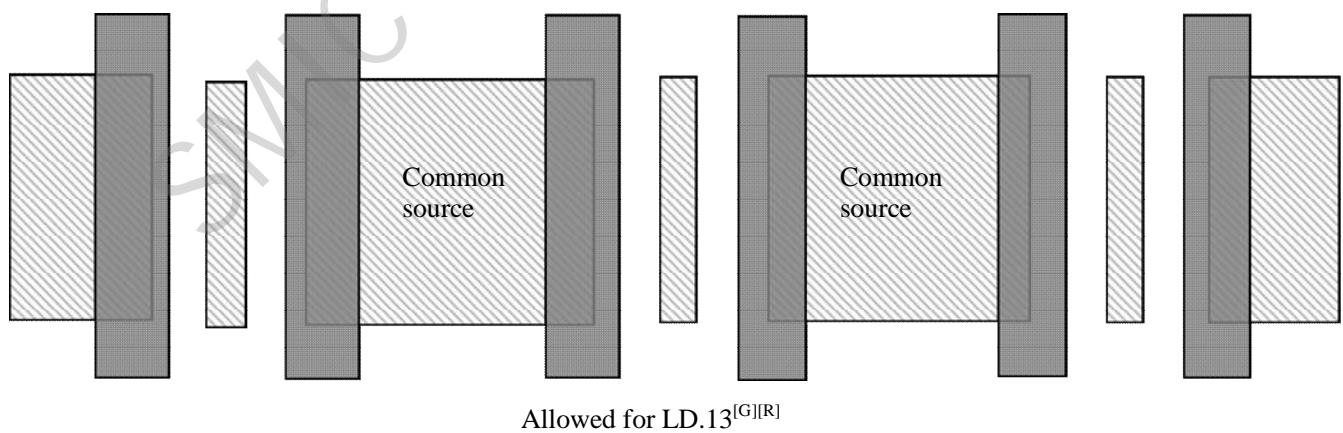
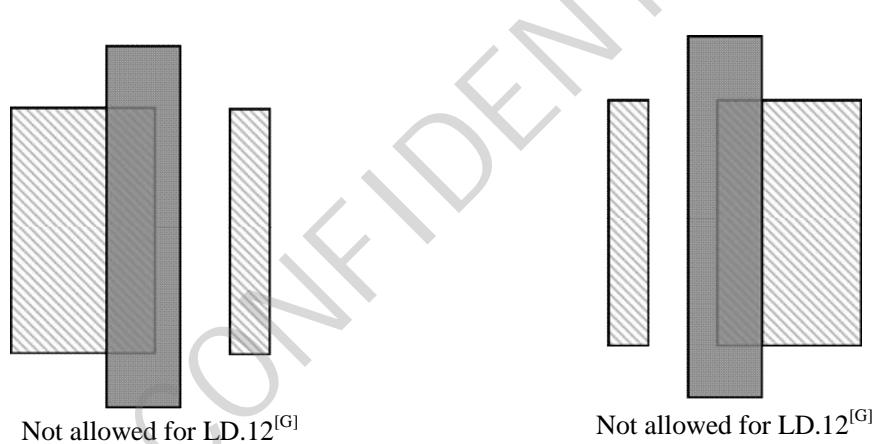
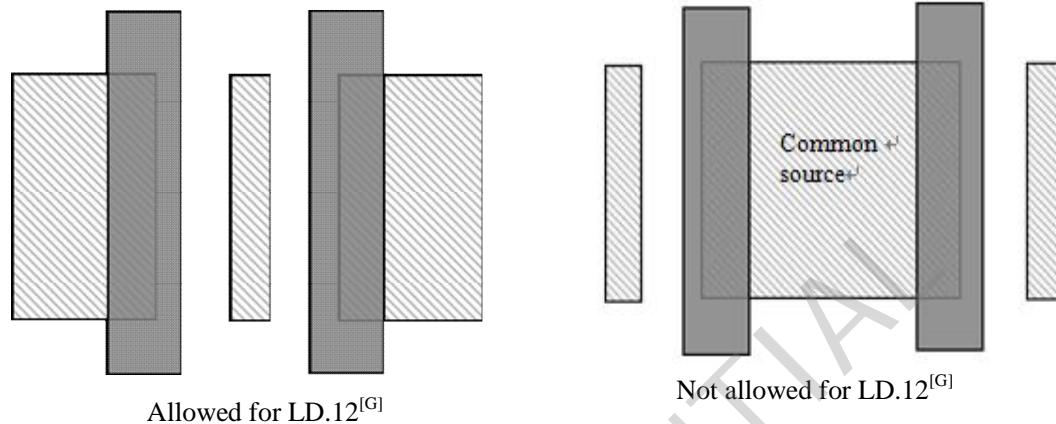
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev. 2	Tech Dev Rev: 1.10.1	Page No.: 233/306
-----------	-------------	--	-------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev:	Tech Dev Rev: 1.10.1	Page No.: 234/306
TD-LO28-DR-2006			2		



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 235/306
---------------------------	---	------------	----------------------	-------------------

7.3.5 Seal ring layout guideline

A. Use of the scribe lane seal ring (guard ring) to protect test chip is recommended

A continuous scribe lane and seal ring is required on all sides of a chip that is intended for dicing and packaging. The seal ring provides both a low resistance path to ground for surge currents and a metal seal against ionic contaminations. 45 degree bent is expected around every die corner. Multiple stacked via/Metal trench are considered to suppress crack risk during dicing saw operation in assembly.

B. Typical structure of scribe lane seal ring (guard ring)

For products less than 10 metal layers, please skip the metal and via layers that are not used in the product.

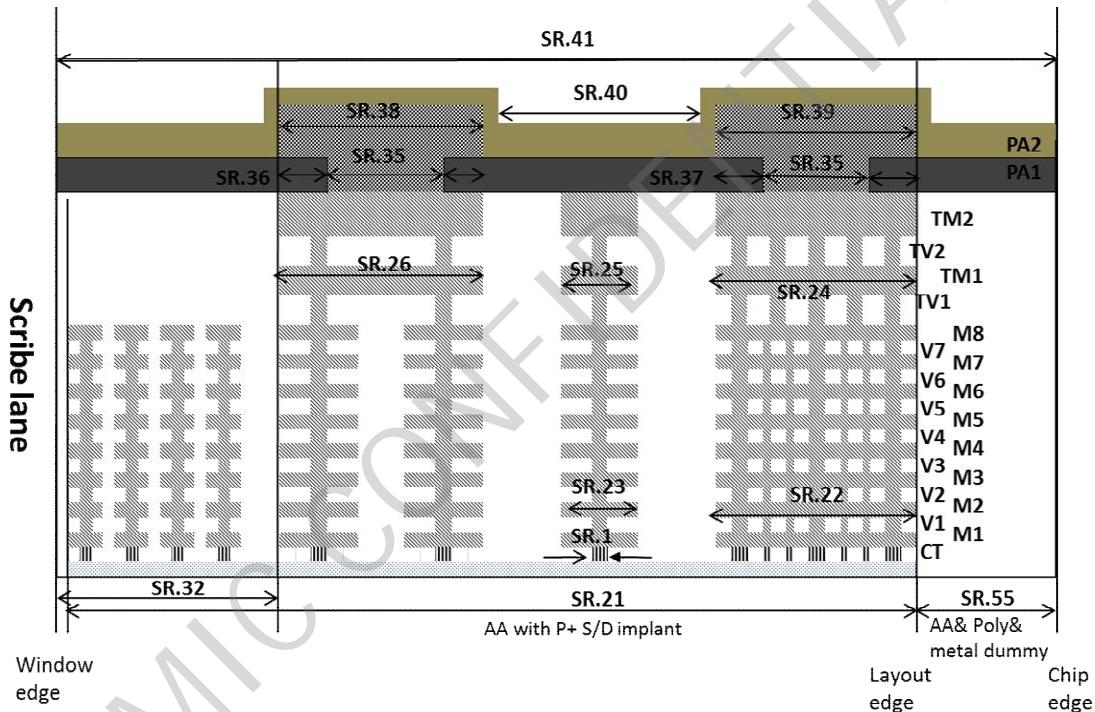


Figure.1 Cross sectional schematic of 10 metal seal ring structure

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 236/306
---------------------------	---	------------	----------------------	-------------------

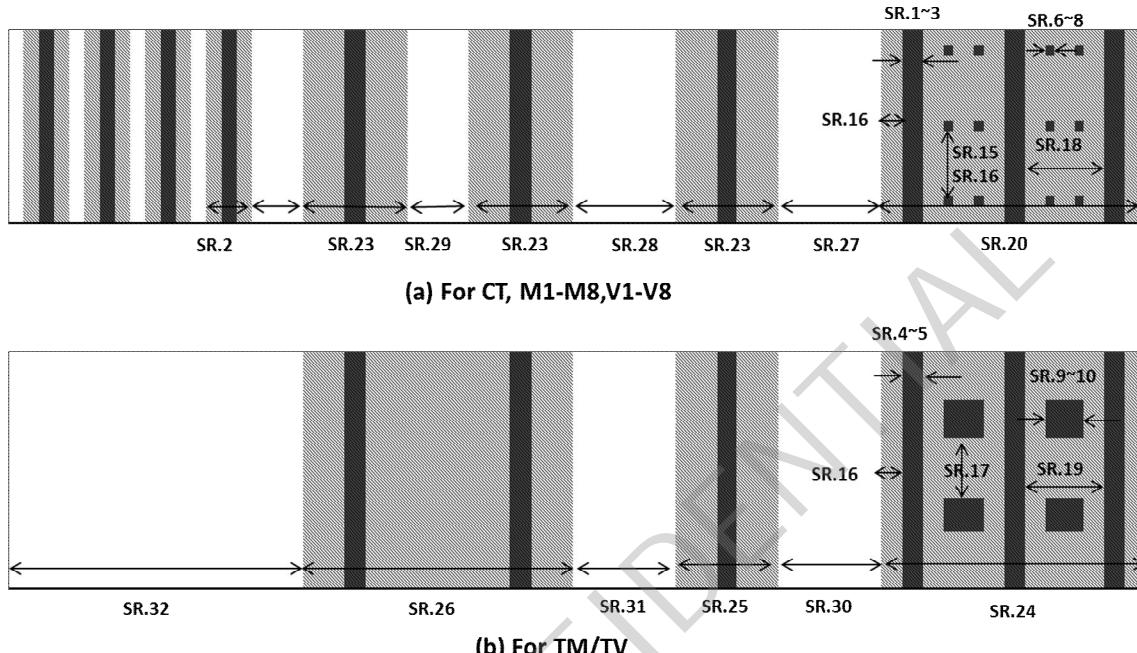


Figure2 Schematic top view of the seal ring structure

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

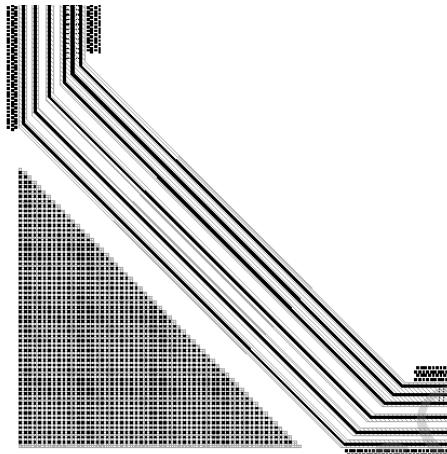
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 237/306
---------------------------	---	------------	----------------------	-------------------

C. Die Corner Layout

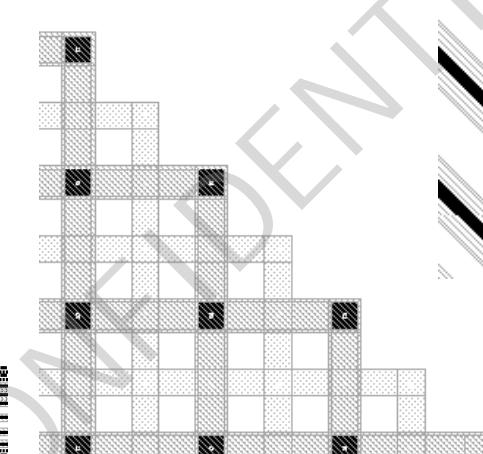
The chamfer region is required for all chips for process robustness. A chamfer or corner bevel of more than 82.2um is required to be cut from each corner of the chip. The chamfer area is triangular and has an area of more than half of 82.2 um x 82.2 um square.

The seal ring corner layout in Figure.3~Figure.5 is recommended to SMIC's customers to manage local stress at each die corner. Metal & via dummy pattern is recommended at each corner of seal ring. The dimension of each segment in the corner layout is given in Figure.3~4.

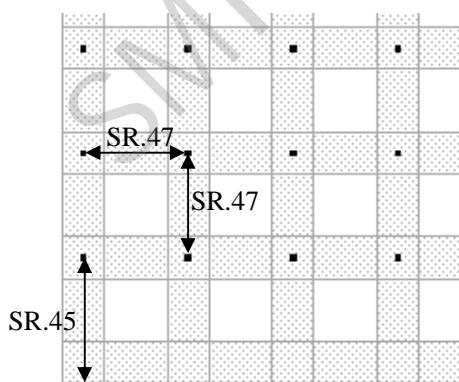
Please customer follows SMIC standard of seal ring corner rule (figure.4, figure.5) both for the situations that seal ring design and layout implemented in SMIC and customer sides.



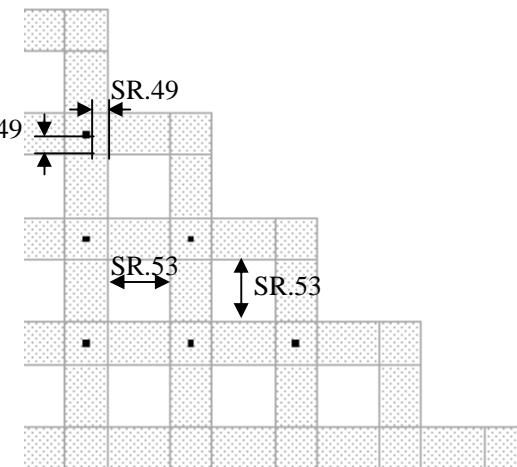
(a) Die corner stress relief structure layout



(b) Zoom-in image for the corner 45 degree edge area of (a)



(c) Zoom-in image in the cross of left side and bottom side area of (a) for M1-M8, CT, V1-V8



(d) Zoom-in image in for the corner 45 degree edge area of (a) for M1-M8, CT, V1-V8

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 238/306
---------------------------	---	------------	----------------------	-------------------

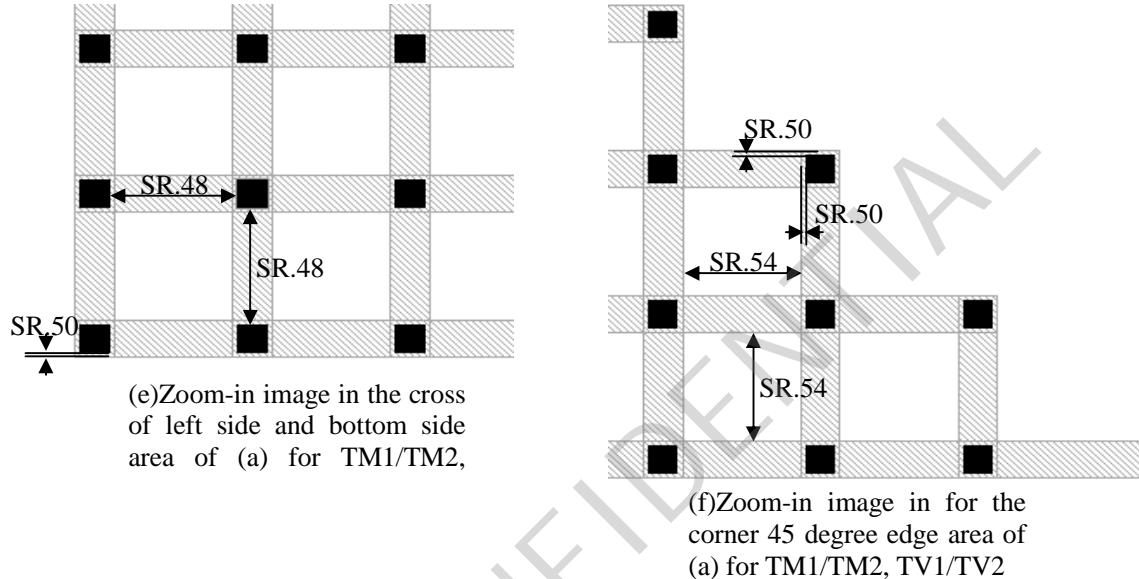


Figure3 Die corner stress relief structure

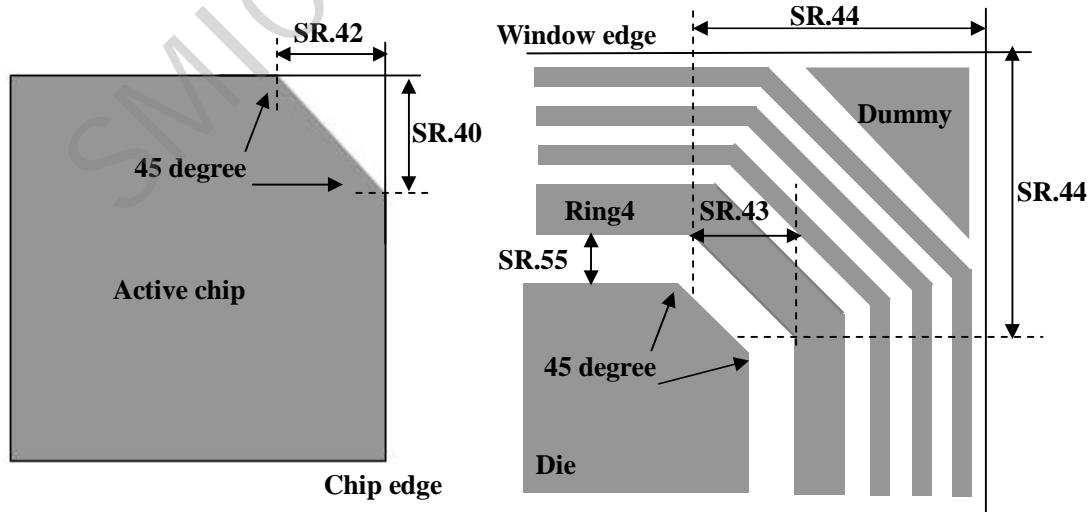


Figure4 Chamfer area at chip corner

Figure5 Seal ring corner if applied by SMIC

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 239/306
---------------------------	---	------------	----------------------	-------------------

Table 1 Dimension of Seal ring structure (this section rule is not for DRC check)

Rule number	Description	Operation	Design Value	Unit
SR.1^[G]	Fixed width of CT slot, it is allowed $\sqrt{2}$ variation (rule value is $0.06\sim 0.06*\sqrt{2}$) at 45 degree angle area.	=	0.06	um
SR.2a^[G]	Fixed width of 1x Vn slot at straight direction	=	0.56 or 0.1	um
SR.2b^[G]	Fixed width of 1x Vn slot at 45 degree angle area	=	0.56~0.56* $\sqrt{2}$ or 0.1~0.1* $\sqrt{2}$	um
SR.3a^[G]	Fixed width of 2x Vn slot at straight direction	=	0.56 or 0.1	um
SR.3b^[G]	Fixed width of 2x Vn slot at 45 degree angle area	=	0.56~0.56* $\sqrt{2}$ or 0.1~0.1* $\sqrt{2}$	um
SR.4a^[G]	Fixed width of 8x Vn slot at straight direction	=	0.56	um
SR.4b^[G]	Fixed width of 8x Vn slot at 45 degree angle area	=	0.56~0.56* $\sqrt{2}$	um
SR.5a^[G]	Fixed width of 10x Vn slot at straight direction	=	0.56	um
SR.5b^[G]	Fixed width of 10x Vn slot at 45 degree angle area	=	0.56~0.56* $\sqrt{2}$	um
SR.6^[G]	Fixed square CT size	=	0.04	um
SR.7^[G]	Fixed width of square 1xVn size	=	0.05	um
SR.8^[G]	Fixed width of square 2xVn size	=	0.1	um
SR.9^[G]	Fixed width of square 8x TV size	=	0.4	um
SR.10^[G]	Fixed width of square 10x TV size	=	0.51	um
SR.11^[G]	CT slot, 1xVn slot, 2xVn slot, 8xVn and 10xVn slot are be drawn in seal ring region (slot pattern is NOT square pattern).			
SR.12^[G]	CT enclosure by M1	\geq	0.1	um
SR.13^[G]	Via slot enclosure by metal	\geq	0.05	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 240/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
SR.14^[G]	Seal ring must be a close ring excluding RF device(RFDEV region).			
SR.15^[G]	Space between square CTs in metal ring along the direction of seal ring	=	1.045	um
SR.16^[G]	Space between square 1xVns/2xVns in metal ring along the direction of seal ring	=	1.01	um
SR.17^[G]	Space between square 8x TVns/10x TVs in metal ring along the direction of seal ring	=	0.6	um
SR.18^[G]	Space between 1xVn/2xVn/8xTVn/10xTVn slot and the metal ring edge	≥	0.5	um
SR.19^[G]	Space between 1xVn/2xVn/8xTVn/10xTVn slots	≥	1.38	um
SR.20^[G]	Space between 1xVn/2xVn/8xTVn/10xTVn slot and 1xVn/2xVn/8xTVn/10xTVn	≥	0.4	um
SR.21^[G]	Width of P+ AA beneath CT in seal ring	=	19.5	um
SR.22^[G]	M1/1x Mn/2x Mn width of ring4	=	5.56	um
SR.23^[G]	M1/1x Mn/2x Mn width of ring1,ring2, ring3	=	1.67	um
SR.24^[G]	8x TMn/10x TMn width of ring3	=	5.56	um
SR.25^[G]	8x TMn/10x TMn width of ring2	=	1.67	um
SR.26^[G]	8x TMn/10x TMn width of ring1	=	4.45	um
SR.27^[G]	Space between M1/1x Mn/2x Mn ring4 and ring3	=	1.67	um
SR.28^[G]	Space between M1/1x Mn/2x Mn ring3 and ring2	=	1.67	um
SR.29^[G]	Space between M1/1x Mn/2x Mn ring2 and ring1	=	1.11	um
SR.30^[G]	Space between 8x TMn/10x TMn ring3 and ring2	=	1.67	um
SR.31^[G]	Space between 8x TMn/10x TMn ring2 and ring1	=	1.67	um
SR.32^[G]	Space between M1/1x Mn/2x Mn/8x TMn/10x TMn ring1 and window edge	=	5	um
SR.33^[G]	Space between M1/1x Mn/2x Mn ring4 and layout edge	=	0	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 241/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
SR.34^[G]	Space between 8x TMn/10x TMn ring3 and layout edge	=	0	um
SR.35^[G]	PA slot width	=	2.4	um
SR.36^[G]	Space between PA slot and M1/1x Mn/2x Mn/8x TMn//10x TMn ring1 edge	=	1.025	um
SR.37^[G]	Space between PA slot and M1/1xMn/2x Mn/8x TMn/10x TMn edge	=	1.58	um
SR.38^[G]	Al ring1 width	=	4.44	um
SR.39^[G]	Al ring2 width	=	5.56	um
SR.40^[G]	Space between Al ring1 and Al ring2	=	5	um
SR.41^[G]	Total seal ring width	=	26.7	um
SR.42^[G]	Chamfer area size at the chip corner	\geq	70	um
SR.43^[G]	Chamfer length of ring4 of seal ring in the bevel corner. This rule is for customer layout and chip design. This rule is for SMIC to apply seal rings for customer.	\geq	70	um
SR.44^[G]	Distance from window edges to the point that ring4 start to bend 45 degree at seal ring corner. This rule is for SMIC to apply seal rings for customer.	=	94	um
SR.45^[G]	Space between first column square 1x Vn/2x Vn and dummy area edge in the die corner dummy relief area	=	2.23	um
SR.46^[G]	Space between first column 8x TVn/10x TVn and dummy area edge in the die corner dummy relief area.	=	2.025	um
SR.47^[G]	Space between 1x Vns/2x Vns in dummy relief area.	=	1.9	um
SR.48^[G]	Space between 8x TVns/10x TVns in dummy relief area.	=	1.49	um
SR.49^[G]	Space between 1x Vns/2x Vns and metal edge in the dummy relief area	=	0.23	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 242/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
SR.50^[G]	Space between 8x TVns/10x TV and metal edge in the dummy relief area	=	0.025	um
SR.51^[G]	M1/1x Mn/2x Mn width in the dummy relief area	=	0.56	um
SR.52^[G]	8x TMn/10x TMn width in the dummy relief area	=	0.56	um
SR.53^[G]	Space between M1s/1x Ms/2x Ms in the dummy relief area	=	1.44	um
SR.54^[G]	Space between 8x TMn/10x TMs in the dummy relief area	=	1.44	um
SR.55^[G]	Space between seal ring layout edge and chip edge(BORDER layer)	=	6.667	um
SR.56^[G]	Chip corner chamfer area should be covered by NODMF			
SR.57^[G]	NODMF layer size at chip corner chamfer area	≥	70	um

Note: The numbers in the above table are gds drawn dimension for 28nm design (pre 10% shrinkage).

Table 2 Key Dimension of Seal ring structure for DRC

Rule number	Description	Operation	Design Value	Unit
SR.1^[G]	Fixed width of contact slot, it is allowed $\sqrt{2}$ variation(rule value is $0.06\sim0.06*\sqrt{2}$) at 45 degree angle area.	=	0.06	um
SR.2a^[G]	Fixed width of 1x Vn slot at straight direction	=	0.56 or 0.1	um
SR.2b^[G]	Fixed width of 1x Vn slot at 45 degree angle area	=	$0.56\sim0.56*\sqrt{2}$ or $0.1\sim0.1*\sqrt{2}$	um
SR.3a^[G]	Fixed width of 2x Vn slot at straight direction	=	0.56 or 0.1	um
SR.3b^[G]	Fixed width of 2x Vn slot at 45 degree angle area	=	$0.56\sim0.56*\sqrt{2}$ or $0.1\sim0.1*\sqrt{2}$	um
SR.4a^[G]	Fixed width of 8x TVn slot at straight direction	=	0.56	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 243/306
---------------------------	---	------------	----------------------	-------------------

Rule number	Description	Operation	Design Value	Unit
SR.4b^[G]	Fixed width of 8x TVn slot at 45 degree angle area	=	0.56~0.56* $\sqrt{2}$	um
SR.5a^[G]	Fixed width of 10x TVn slot at straight direction	=	0.56	um
SR.5b^[G]	Fixed width of 10x TVn slot at 45 degree angle area	=	0.56~0.56* $\sqrt{2}$	um
SR.6^[G]	Fixed square CT size	=	0.04	um
SR.7^[G]	Fixed width of square 1xVn size	=	0.05	um
SR.8^[G]	Fixed width of square 2x Vn size	=	0.1	um
SR.9^[G]	Fixed width of square 8x TV size	=	0.4	um
SR.10^[G]	Fixed width of square 10x TV size	=	0.51	um
SR.11	CT slot, 1xVn slot, 2xVn slot, 8x TVn and 10x TVn slot are be drawn in seal ring region (slot pattern is NOT square pattern).			
SR.12^[J]	CT slot enclosure by M1	\geq	0.1	um
SR.13	Via slot enclosure by metal	\geq	0.05	um
SR.14	Seal ring must be a close ring excluding RF device(RFDEV region).			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 244/306
TD-LO28-DR-2006					

7.3.6 ESD design rules and guideline

The ESD guidelines are targeted to meet HBM-2KV(Human Body Mode) and MM-200V (Machine mode) spec according to EIA/JEDEC standard and EIA/JESD22 test standard, SMIC does not guarantee the final ESD device performance. If designers do not follow SMIC ESD guideline, chip level ESD test should be done for ESD verification.

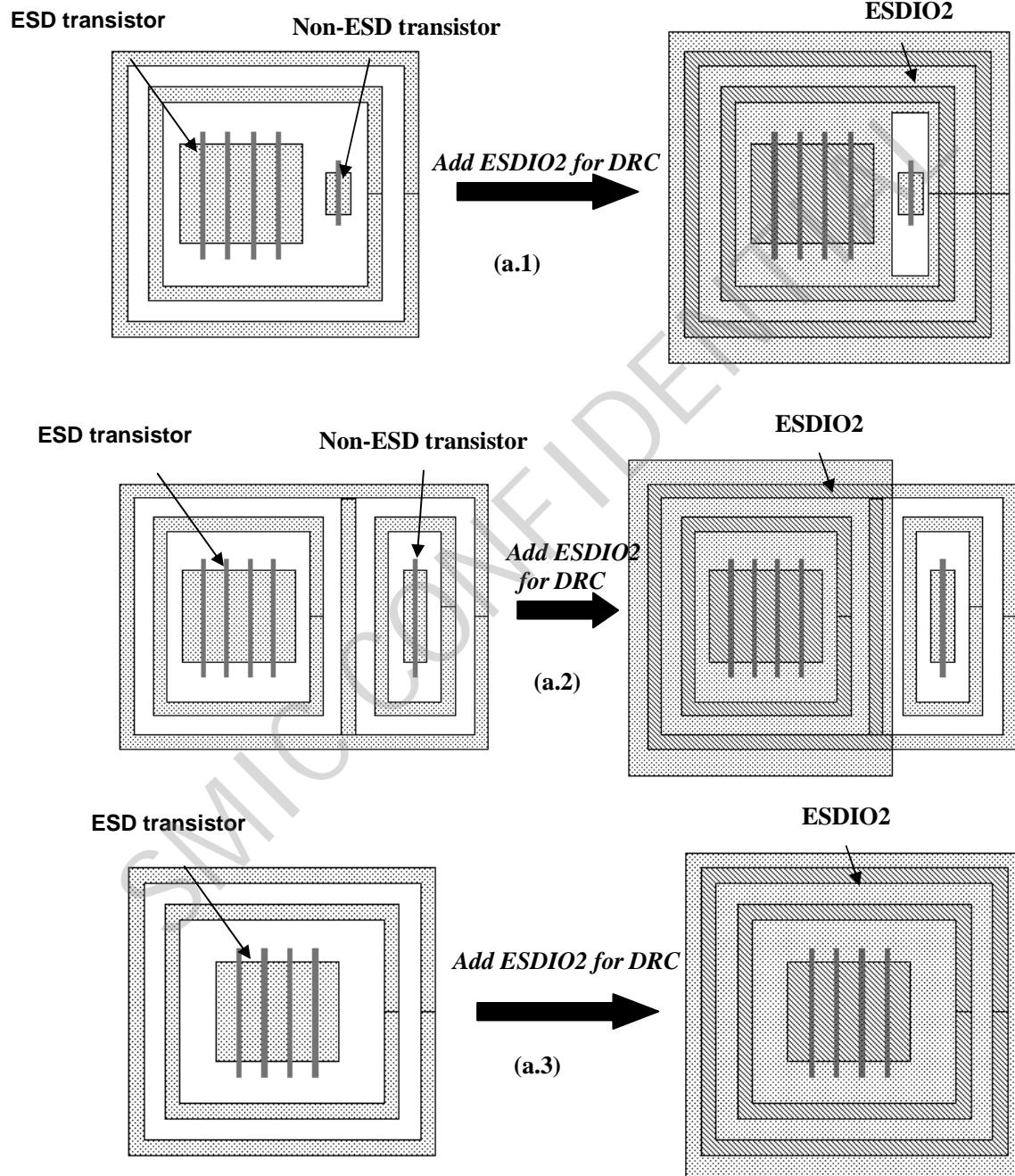
7.3.6.1 ESDIO2 (DRC marker layer for ESD component)

ESDIO2 (GDS No: 133;3) is DRC marking layer for I/O ESD N/PMOS including power clamp big MOS protection devices and circuits identification. This layer should cover ESD transistors and its N and P guard rings, but non-ESD transistor inside the same guard ring should be excluded. Otherwise, all the devices and circuits inside ESDIO2 will be regarded as ESD transistors and may induce false DRC alarms. ESDIO2 should be drawn at each individual ESD protection device.

ESDHV (GDS: 133;1) is DRC marking layer for HV tolerant ESD protection devices using cascaded N/PMOS. Please refer to the examples in Fig.1.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 245/306
---------------------------	---	------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 246/306
---------------------------	---	------------	----------------------	-------------------

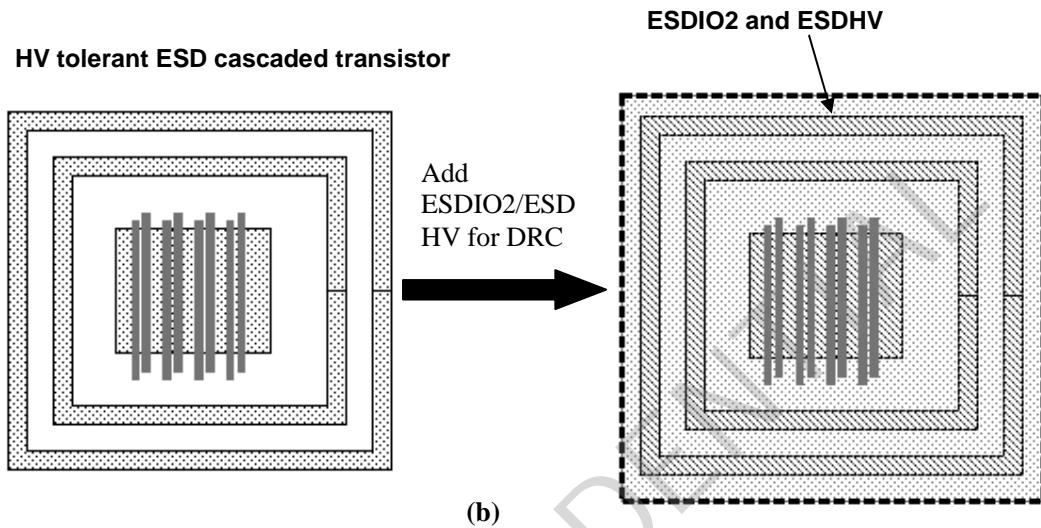


Fig.1 Examples of ESDIO2/ESDHV for ESD DRC

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 247/306
---------------------------	---	------------	----------------------	-------------------

7.3.6.2 ESD design and layout guideline

The guideline provided layout structure and dimension for N/P MOS ESD protection device design.
SAB on drain side is essential for ESD protection devices.

Rule Number	Description	Operation	Design Value	Unit
ESD.1^[NC]	Finger-type structure with uniform finger width is suggested for N/P MOS ESD protection design			
ESD.2^[G]	Unit finger width (F) of NMOS and PMOS for ESD protection device (Fig.2)	\geq	5	um
		\leq	30	um
ESD.3^[G]	ESD.3a ^[G] and ESD.3b ^[G] are defined for total channel width of ESD N/PMOS. The total channel width is calculated by the ESD MOS in the same Drain connection. The connectivity can be formed by all metal, via, ALPA, PA and MD but not broken by resistors. SAB is used for drain recognition in DRC runset.			
ESD.3a^[G]	Channel width (W) of NMOS for ESD protection device (Channel width=Finger width x Finger No.)	\geq	360	um
ESD.3b^[G]	Channel width (W) of PMOS for ESD protection device (Channel width=Finger width x Finger No.)	\geq	450	um
ESD.4a^[G]	Channel length of core N/PMOS for protection device	\geq	0.08	um
ESD.4b^[G]	Channel length of 1.8V/1.5V (under drive) I/O N/PMOS for protection device	\geq	0.15	um
ESD.4c^[G]	Channel length of 2.5V/1.8V (under drive) I/O N/PMOS for protection device	\geq	0.27	um
ESD.4d^[G]	Channel length of 2.5V overdrive 3.3V I/O NMOS for protection device	\geq	0.55	um
ESD.4e^[G]	Channel length of 2.5V overdrive 3.3V I/O PMOS for protection device	\geq	0.44	um
ESD.5^[G]	(Purposely blank)			
ESD.6^[G]	(Purposely blank)			
ESD.7^[G]	SAB should block on drain side of NMOS and PMOS (contact region should be kept silicided.) SAB drawn on source side is not necessary.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 248/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
ESD.8^[G]	Width of SAB on the drain side (A) for 1.0/1.2/1.8 NMOS and PMOS, note: A does not include the overlap of SAB area and GT(Fig. 4 and Fig.6)	\geq	0.6	um
ESD.9^[G]	ESD protection devices should be surrounded by guard ring, this guard ring also can be designed as the pickup of the ESD device. (Fig.2)			
ESD.10^[NC]	The NMOS/PMOS should be added after the input resistor R as the secondary ESD protection for better ESD immunity if there is no conflict with circuit operation.			
ESD.11^[NC]	value of input resister R. (Fig. 3)	\geq	200	Ω
ESD.12^[NC]	The suggested channel width for secondary ESD protection device	$=$	20	um
ESD.13a^[NC]	Channel length of core N/PMOS for secondary protection device	$=$	0.08	um
ESD.13b^[NC]	Channel length of 1.8V/1.5V (under drive) I/O N/PMOS for secondary protection device	$=$	0.15	um
ESD.13c^[NC]	Channel length of 2.5V/1.8 (under drive) I/O N/PMOS for secondary protection device	$=$	0.27	um
ESD.13d^[NC]	Channel length of 2.5V overdrive 3.3V NMOS for secondary protection device	$=$	0.55	um
ESD.13e^[NC]	Channel length of 2.5V overdrive 3.3V PMOS for secondary protection device	$=$	0.44	um
ESD.14a^[G]	The overlap (Sd) of SAB and poly for all I/O ESD N/PMOS (Fig. 4)	\geq	0.05	um
ESD.14b^[G]	The overlap (Sd) of the SAB and poly for core ESD N/PMOS	\geq	0.02	um
ESD.15^[G]	For high voltage tolerant I/O using Cascoded NMOS, ESD implant is required. (refer to Fig.5& 6)			
ESD.16a^[G]	Channel length for 2.5V tolerant I/O using 1.8V cascaded N/PMOS	\geq	0.15	um
ESD.16b^[G]	Channel length for 3.3V tolerant I/O using 2.5V cascaded N/PMOS	\geq	0.27	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 249/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
ESD.16c^[G]	Channel length for 5V tolerant I/O using 3.3V (2.5V overdrive) cascoded N/PMOS	\geq	0.55	um
ESD.17^[G]	The space (S) between active poly gate and inactive poly gate of cascoded NMOS should be (Fig.6)	\leq	0.3	um
ESD.18^[G]	For high voltage tolerant I/O designed by cascoded N/PMOS, SAB should cover all top poly gates and extend to overlap the second poly gate by (Fig. 6)	\geq	0.05	um
ESD.19^[NC]	Contacts should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of contact drawn on rule is	\geq	370	count
ESD.20^[NC]	Vias should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of via drawn on rule is	\geq	650	count
ESD.21a^[NC]	Total width (W2) of each individual inter metal(M1~M8) lines of the nearest current path between ESD devices and bonding pad	\geq	15	um
ESD.22b^[NC]	Total width (W2) of each individual top metal(TM1,TM2) line of the nearest current path between ESD devices and bonding pad	\geq	3	um
ESD.23^[NC]	In Chip level ESD guideline, the poly gate of N/PMOS of internal and I/O circuit is not allowed to connect to power/ground or input/output pad directly. Please refer to ESD.21a, ESD.21b, ESD.21c rules below.			
ESD.23a^[NC]	Secondary ESD protection or tie-high/tie-low cell is strongly recommended to insert between poly gate and power/ground pad or input/out pad.			
ESD.23b^[NC]	N/PMOS used for capacitor is not recommended to connect power/ground or input/output pad directly.			
ESD.23c^[NC]	Poly resistor and ESD protection N/PMOS (including primary and secondary ESD protection) can be exempt for this rule.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 250/306
---------------------------	---	------------	----------------------	-------------------

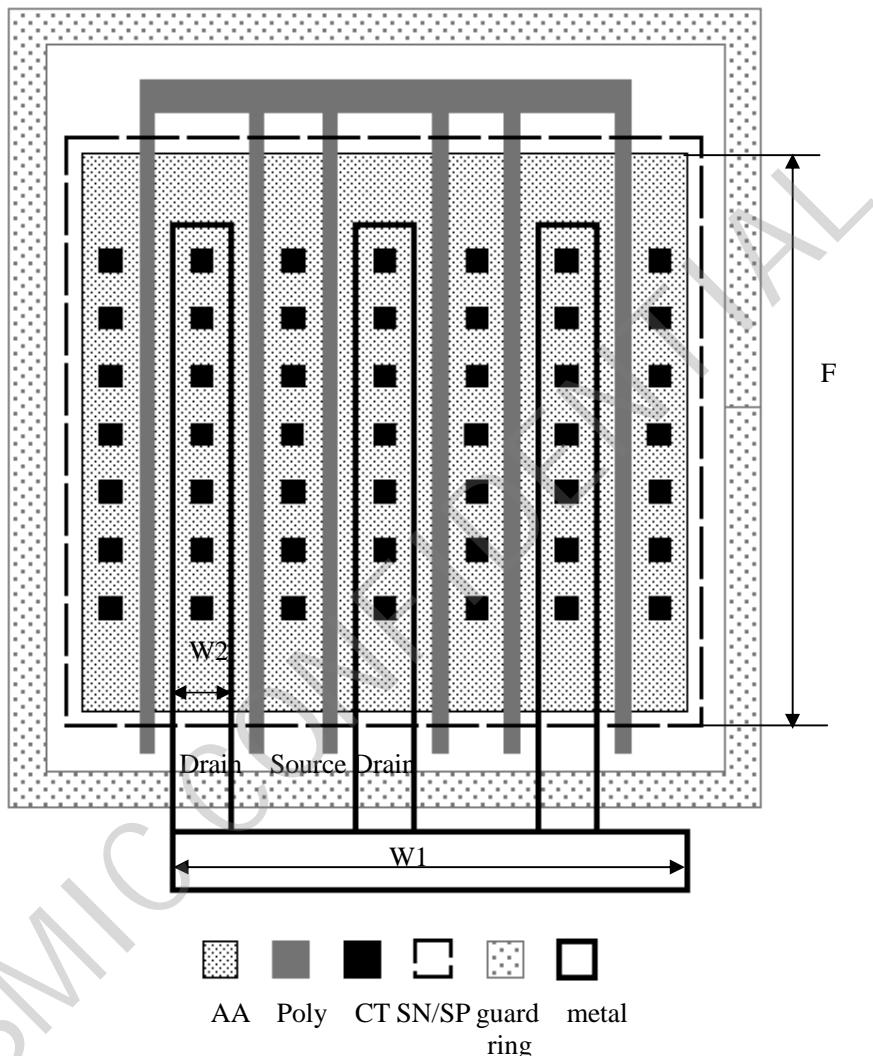


Fig.2 ESD Cell Layout Example

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 251/306
---------------------------	---	------------	----------------------	-------------------

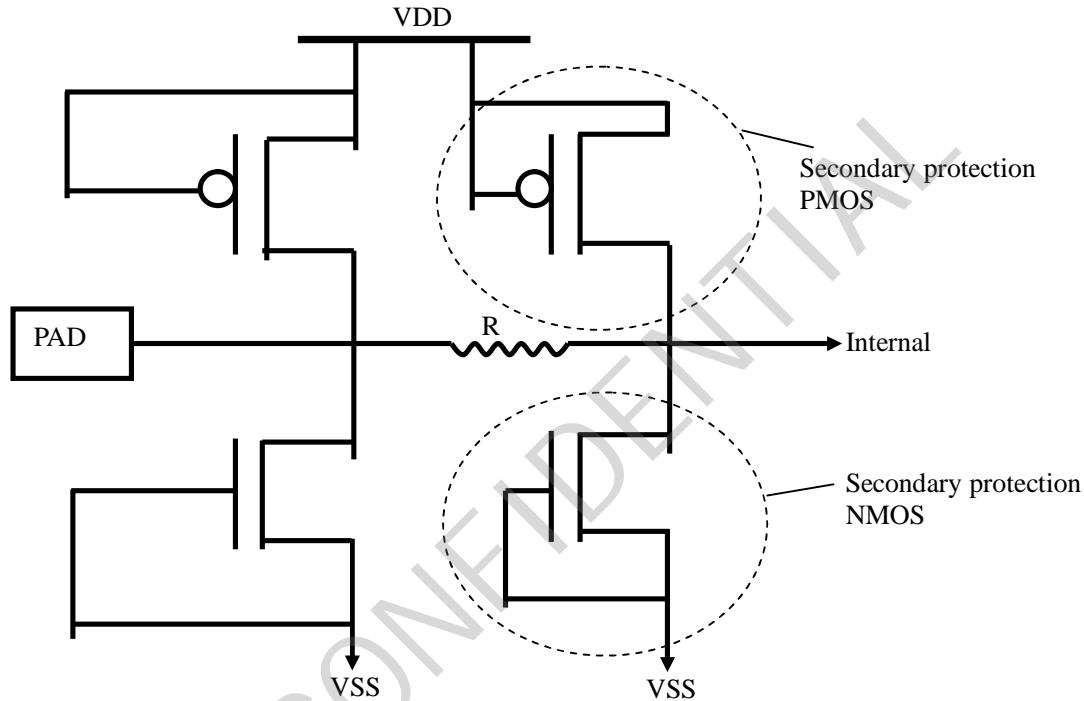


Fig. 3 ESD Protection Scheme

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 252/306
---------------------------	---	------------	----------------------	-------------------

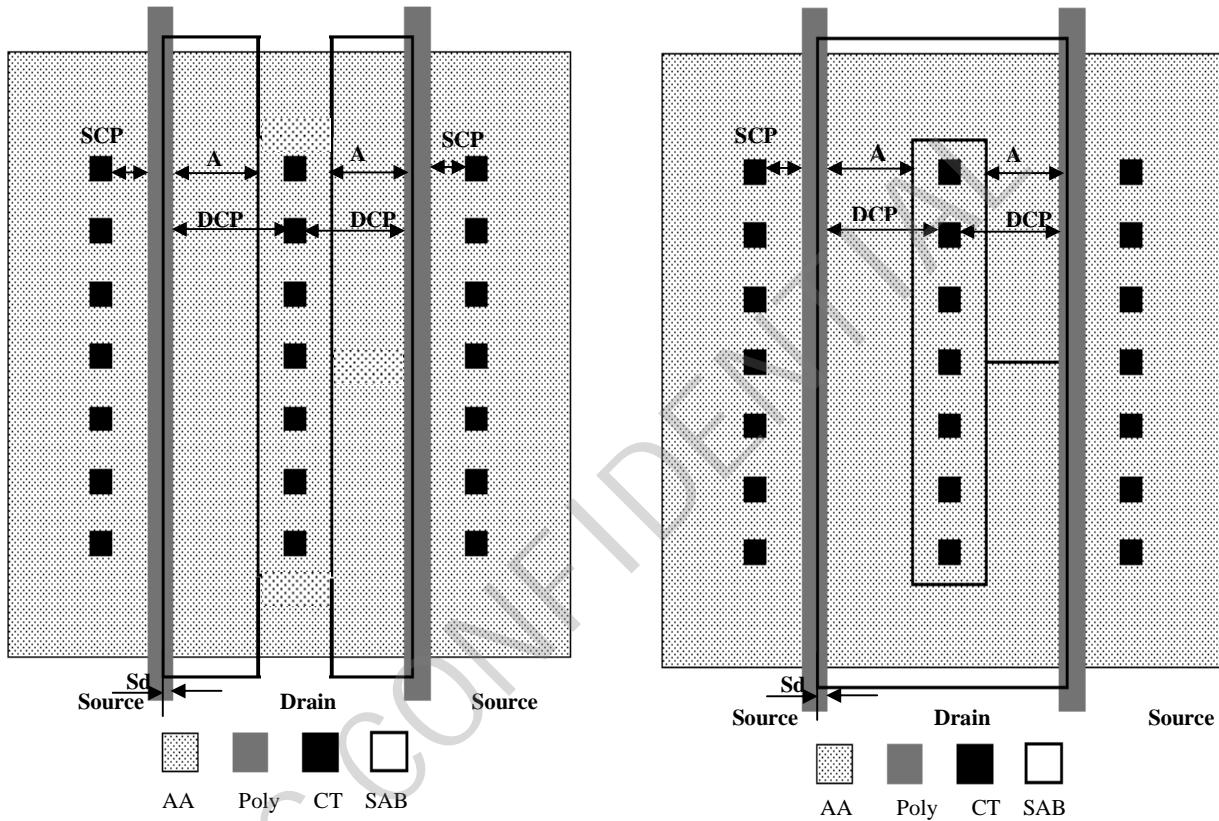


Fig.4 NMOS/PMOS I/O for ESD Protection with two layout styles of SAB

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 253/306
---------------------------	---	------------	----------------------	-------------------

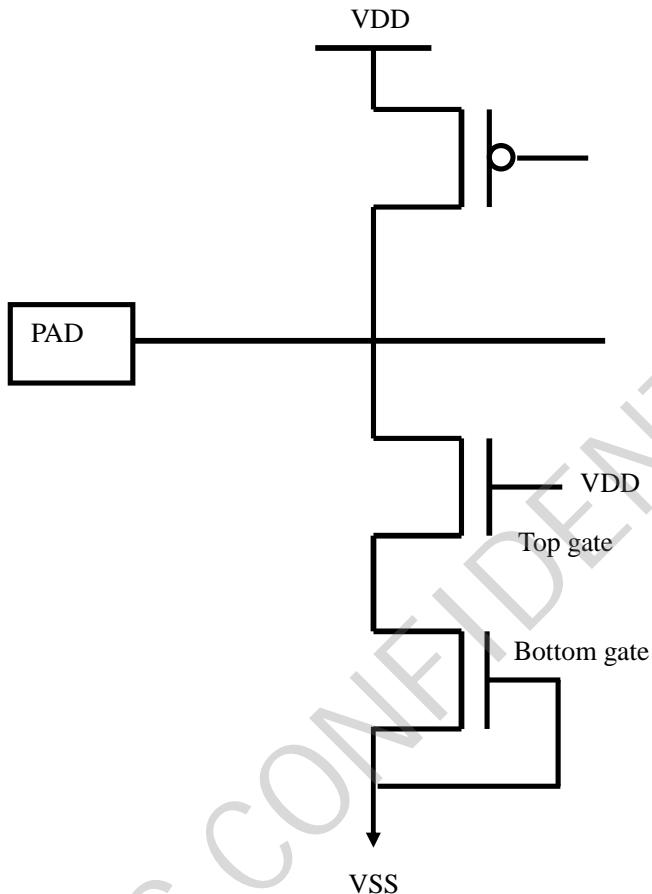


Fig. 5 HV Tolerant I/O ESD protection using cascaded NMOS

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 254/306
---------------------------	---	------------	----------------------	-------------------

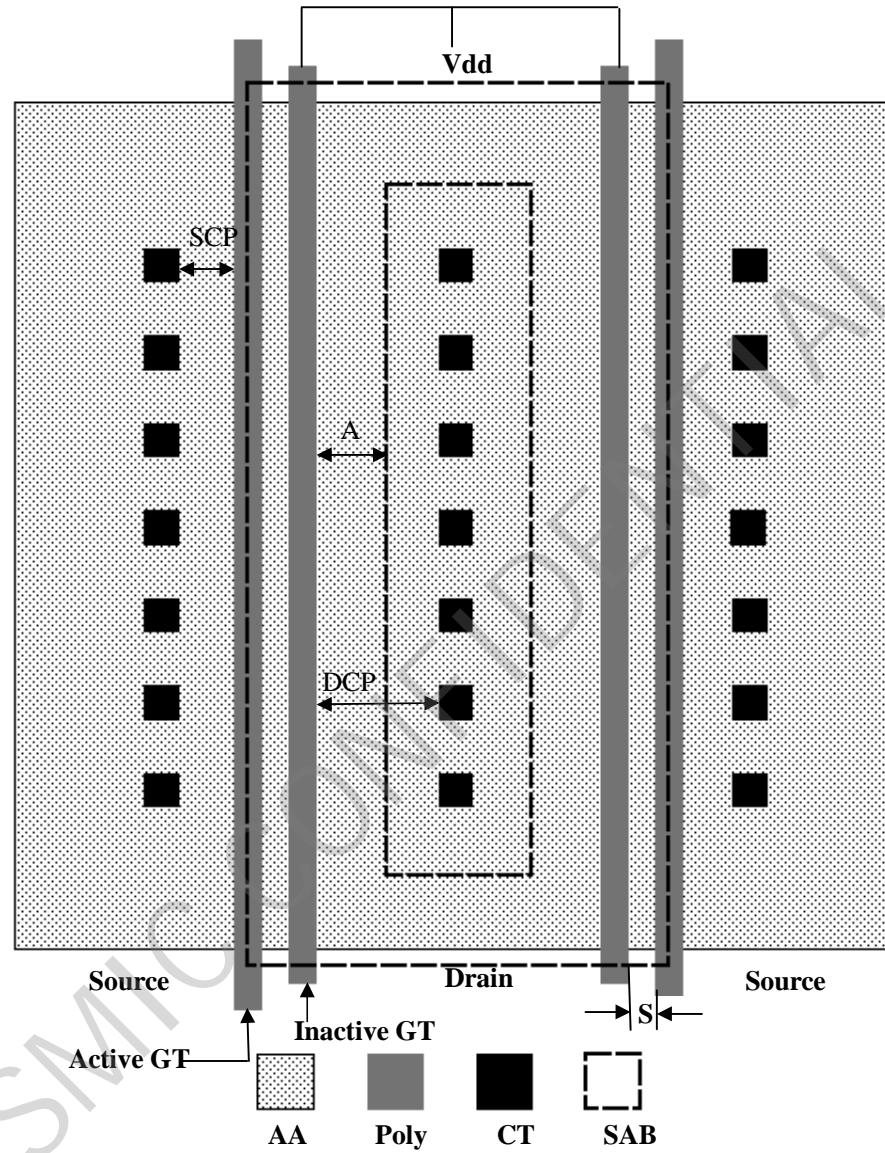


Fig.6 Cascoded NMOS for HV Tolerant I/O (two layout styles of SAB as Fig.4 are allowed)

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 255/306
---------------------------	---	------------	----------------------	-------------------

7.3.6.3 ESD1 implant layer rules

ESD1 implant layer is an optional layer to define ESD implant location for N type ESD device to improve ESD performance. The implant layer must be drawn in the area that needs ESD implant.

Rule Number	Description	Operation	Design Value	Unit
ESD1.1	ESD1 width.	\geq	0.5	um
ESD1.2	Space between two ESD1s. Merge if space is less than this value.	\geq	0.5	um
ESD1.3	ESD1 area.	\geq	1	um ²
ESD1.4	ESD1 enclosed area.	\geq	1	um ²
ESD1.5	CT enclosure by ESD1.	\geq	0.2	um
ESD1.5a^[R]	The recommended CT enclosure by ESD1.	\geq	0.4	um
ESD1.6	Space between an ESD1 implant to an N-channel Poly gate.	\geq	0.2	um
ESD1.7	ESD1 must be fully covered by AA at least.	\geq	0.2	um
ESD1.8	ESD1 implant region is not allowed to overlap with SP.			
ESD1.9^[NC]	ESD1 must be a drawn layer if there is need of ESD implant.			
ESD1.10	ESD1 isn't allowed to interact with poly in drain side.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 256/306
---------------------------	---	------------	----------------------	-------------------

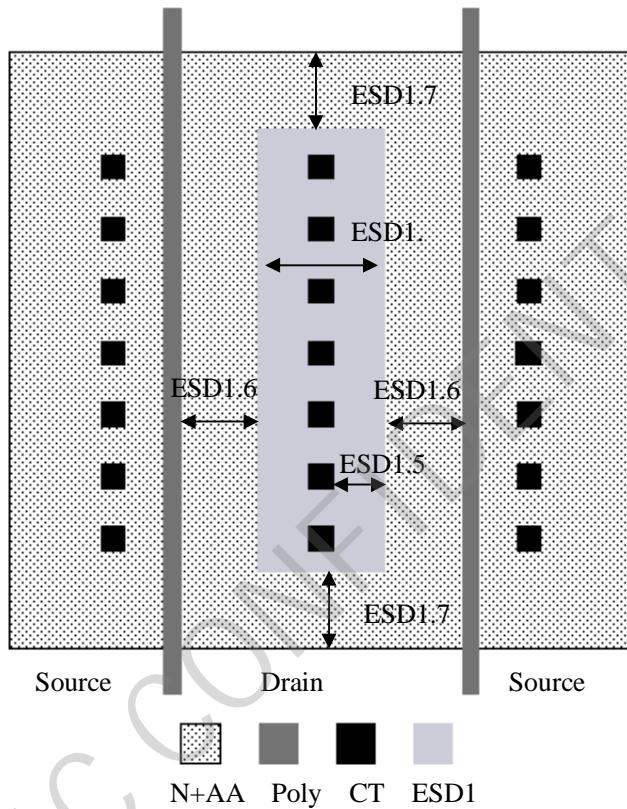


Fig. 7 ESD1 in N type ESD device

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 257/306
---------------------------	---	------------	----------------------	-------------------

7.3.6.4 Power Clamp guidelines

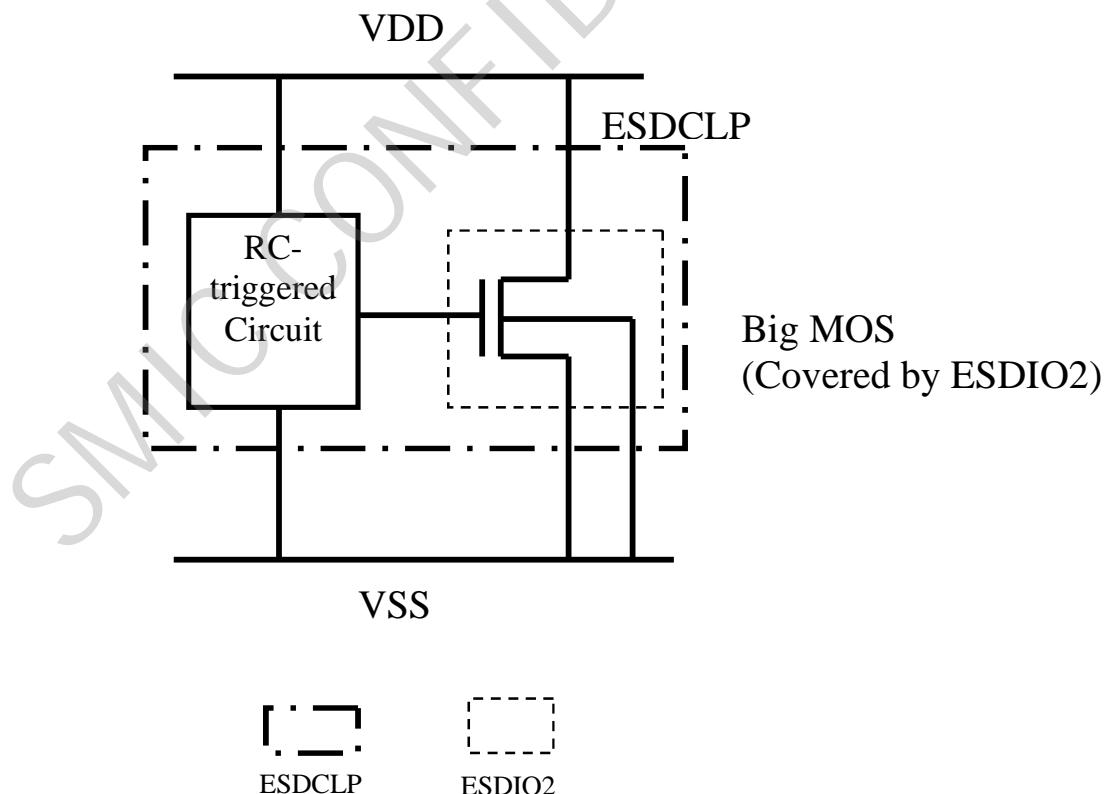
- ESDCLP (41; 2) is the marking layer for ESD RC-triggered power clamp structures connected to a power supply pad.
- Power clamp includes one RC trigger circuit and one big MOS. The trigger circuit will turn on the big MOS during ESD even and keep the big MOS off at normal operation.
- There are two kinds of power clamp devices: one is with SAB using snapback current to discharge (SAB type) and the other is without SAB using the normal turn-on current of MOS to discharge (non-SAB type).
- DRC uses ((N+ AA and ESDCLP and ESDIO2) NOT INTERACT SAB) to recognize non-SAB type power clamp NMOS and ((P+ AA and ESDCLP and ESDIO2) NOT INTERACT SAB) to recognize non-SAB type power clamp PMOS.
- DRC uses ((N+ AA and ESDCLP and ESDIO2) AND INTERACT SAB) to recognize SAB type power clamp NMOS and ((P+ AA and ESDCLP and ESDIO2) AND INTERACT SAB) to recognize SAB type power clamp PMOS.

Rule Number	Description	Operation	Design Value	Unit
ESD.30^[NC]	Finger-type structure with uniform finger width is suggested for both SAB type and non-SAB type Power Clamp.			
ESD.31^[G]	ESD.31a ^[G] , ESD.31b ^[G] and ESD.31c ^[G] are defined for total channel width of non-SAB and SAB type of Power Clamp N/PMOS. For non-SAB type (ESD.31a ^[G] and ESD.31b ^[G]), the total channel width is calculated by the ESD MOS in the same Source or Drain connection. With either one of calculated total channel width with the same source or drain connection larger than the defined value, DRC does not flag the violation. The connectivity can be formed by all metal, via, ALPA, PA and MD but not broken by resistors. For SAB type (ESD.31c ^[G]), the total channel width is calculated by the ESD MOS in the same Drain connection. The connectivity can be formed by all metal, via, ALPA, PA and MD but broken by resistors. SAB is used for drain recognition in DRC runset.			
ESD.31a^[G]	Channel width (W) of core non-SAB type power clamp N/PMOS (Channel width=Finger width x Finger No.)	≥	1500	um
ESD.31b^[G]	Channel width (W) of 1.8V/2.5V (and all underdrive or overdrive) I/O non-SAB type power clamp N/PMOS (Channel width=Finger width x Finger No.)	≥	1000	um
ESD.31c^[G]	Channel width (W) of 1.8V/2.5V (and all underdrive or overdrive) I/O SAB type power clamp N/PMOS	≥	1000	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 258/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
	(Channel width=Finger width x Finger No.)			
ESD.32^[G]	For non-SAB type power clamp, the spacing of source/drain CT to poly	\geq	0.2	um
ESD.33^[G]	For SAB type power clamp, ESD.2, ESD.4~ESD.10 must follow.			
ESD.34^[G]	For non-SAB type power clamp, ESD.4, ESD.9, ESD.10 must follow			
ESD.35^{[G][NC]}	For core and 1.8V application, non-SAB type power clamp is recommended to use. For 2.5V or higher application voltage, SAB-type power clamp is recommended to use.			

**Fig.8 Power Clamp schematic**

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 259/306
---------------------------	---	------------	----------------------	-------------------

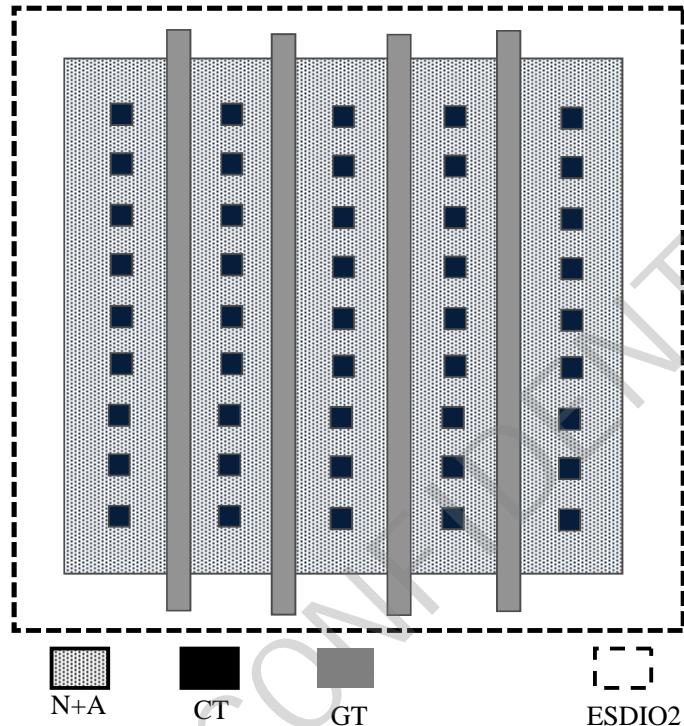


Fig.9 Non-SAB type Power Clamp NMOS (ESDIO2 drawing follow 7.3.5.1)

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 260/306
---------------------------	---	------------	----------------------	-------------------

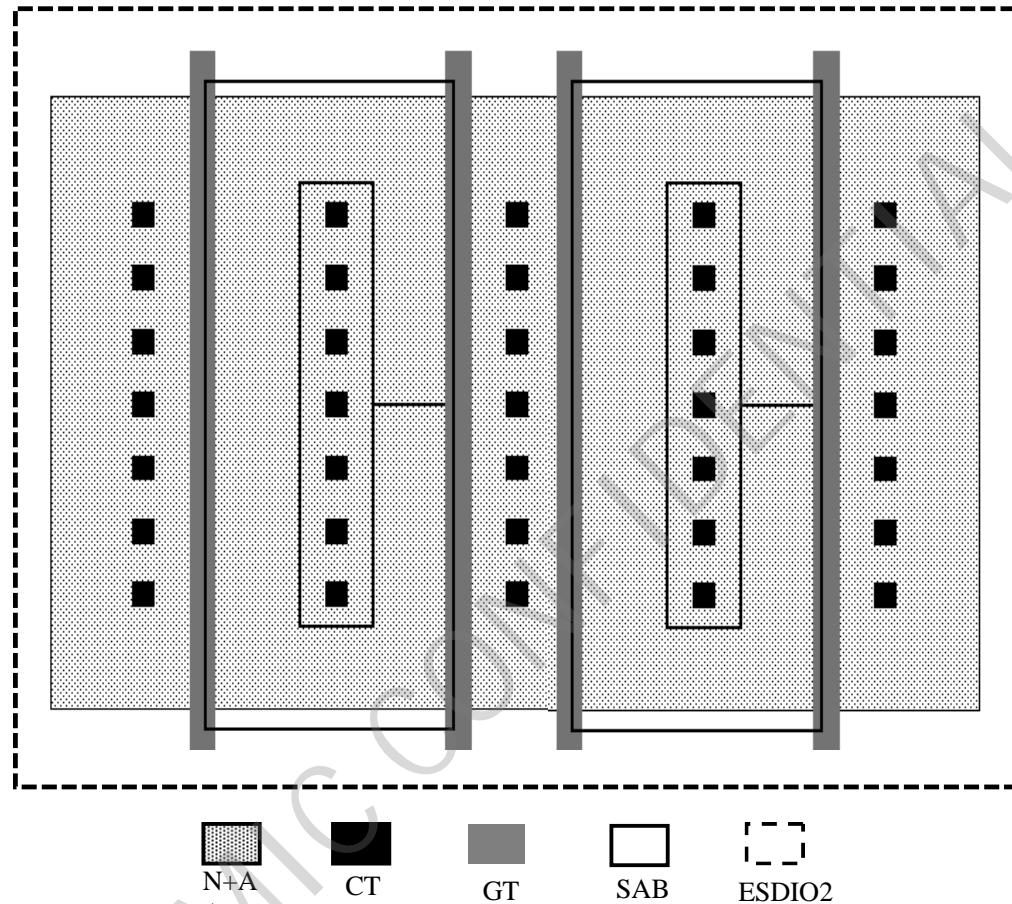


Fig.10 SAB type Power Clamp NMOS (ESDIO2 drawing follows 7.3.5.1; **two layout styles of SAB as Fig.4 are allowed**)

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 261/306
---------------------------	---	------------	----------------------	-------------------

7.3.6.5 ESD Diode guidelines

- ESD diode can be used for logic or RF ESD protection.
- ESD level is proportional to the diode perimeter; however, the parasitic capacitance increase at the same time.
- CLPDMY (87; 2) is the marking layer for STI ESD bounded diode; ESDPOB (41; 8) is the marking layer for poly bounded (gated) ESD diode.
- The values in the ESD diode guidelines are the suggested number for design reference; customer can adjust the layout parameters according to the spec/capacitance need.

Rule Number	Description	Operation	Design Value	Unit
ESD.40^{[G][NC]}	Finger-type structure with uniform finger width is suggested for both STI bounded ESD diode and poly bounded ESD diode.			
	ESD.41~ESD.46 are defined for STI ESD diode			
ESD.41^{[G][NC]}	Unit finger length of STI ESD diode (Ls)	≥	0.5	um
		≤	1.5	
ESD.42^{[G][NC]}	Unit finger width of STI ESD diode (Ws)	≥	5	um
		≤	30	
ESD.43^{[G][NC]}	Total perimeter of STI ESD diode [(L+W)*2]	≥	400	um
ESD.44^{[G][NC]}	The PW/NW pickup width (A) should be larger than N+AA/P+AA width (L)			
ESD.45^{[G][NC]}	The AA spacing of the longer side of N+AA/P+AA between N+AA/P+AA and PW/NW pickup AA (C)	≥	0.3	um
		≤	0.4	
ESD.46^{[G][NC]}	The AA spacing of the shorter side of N+AA/P+AA between N+AA/P+AA and PW/NW pickup AA (B)	≥	0.6	um
		≤	0.8	
ESD.47^{[G][NC]}	Only I/O gated diode is allowed, that is gated diode must be covered by DG			
	ESD.48~ESD.50 are defined for gated ESD diode			
ESD.48^{[G][NC]}	Unit finger length of gated ESD diode (Lg)	≥	0.16	um
ESD.49^{[G][NC]}	Unit finger width of gated ESD diode (Wg)	≥	5	um
		≤	30	
ESD.50^{[G][NC]}	Total finger width of gated ESD diode (Wg*N)	≥	360	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 262/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
	ESD.48~ESD.50 are defined for both STI ESD diode and gated ESD diode			
ESD.51^{[G][NC]}	Contacts and Vias should be as many as possible			
ESD.52^{[G][NC]}	Total metal width ($W_1 + W_2 + W_3 + \dots$) of anode or cathode connected to pad	\geq	20	um

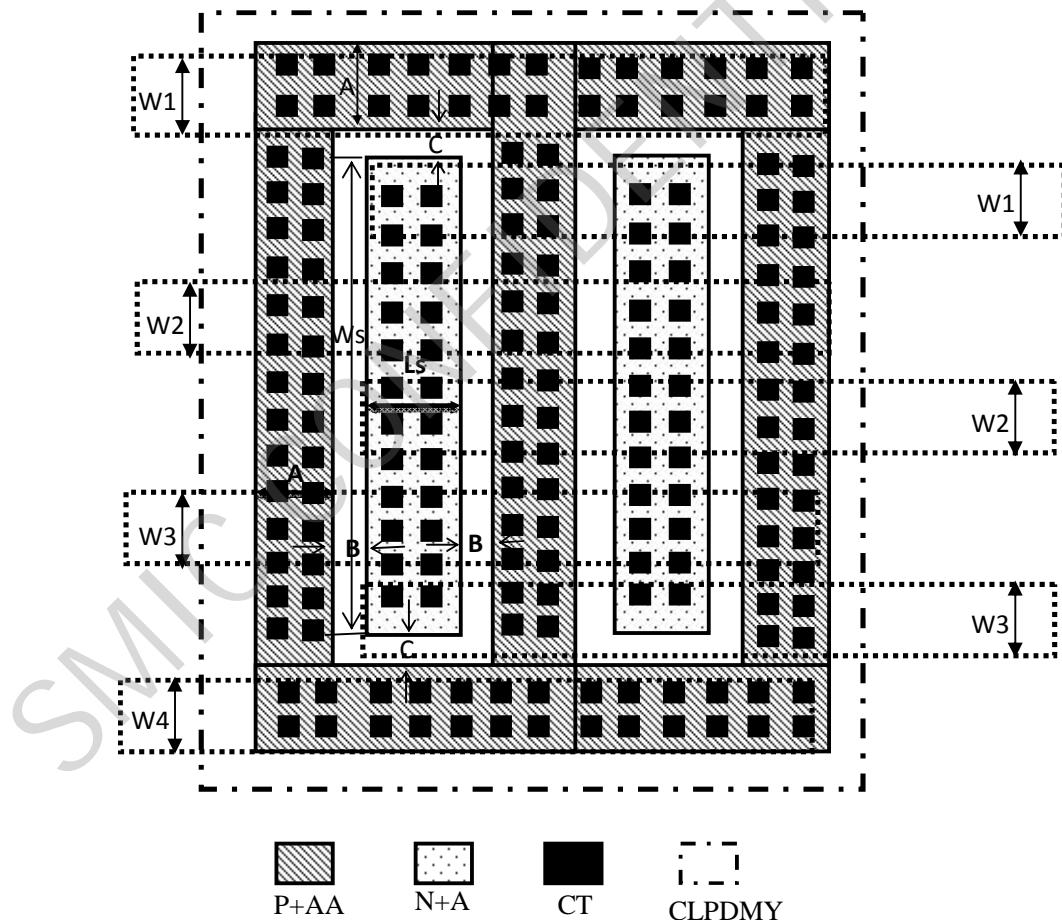


Fig.11 Multi-finger STI bounded ESD Diode

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev:	Tech Dev Rev:	Page No.:
TD-LO28-DR-2006			2	1.10.1	263/306

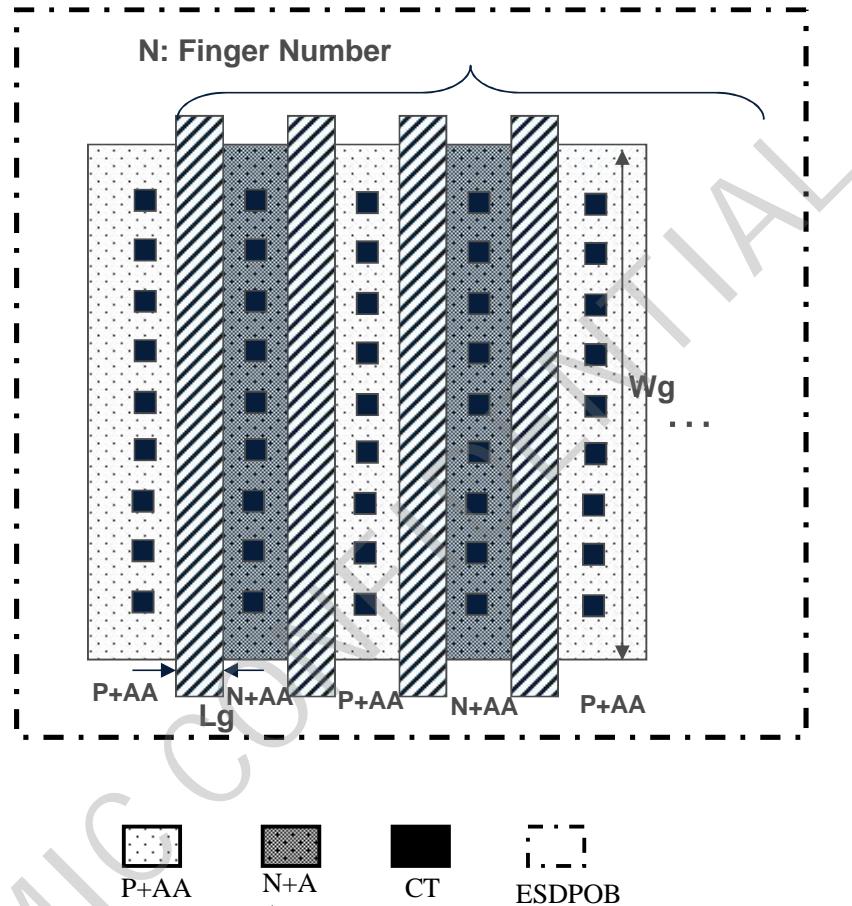


Fig.12 Multi-finger Poly bounded (gated) Diode

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 264/306
---------------------------	---	------------	----------------------	-------------------

7.3.7 Latch-Up prevention layout guidelines

I. Definition of nomenclature in latch up guidelines

Name	Definitions
I/O pads	Pads except Vdd pad, Vss pad.
Power Pads	Vdd pad, Vss pad
Guard-ring	Complete un-broken ring-type AA and M1 with CT as many as possible, connected to Vdd or Vss
P+ guard-ring	Complete un-broken ring-type (SP AND AA) and M1 with CT as many as possible, connected to Vss.
N+ guard-ring	Complete un-broken ring-type (SN AND AA) and M1 with CT as many as possible, connected to Vdd.
AA injector	Any AA directly connected to I/O pad, ex. MOS, diode, AA resistor, and well resistor directly connected to I/O pad.
P+ injector	((SP AND AA) NOT GT) directly connected to I/O pad
N+ injector	((SN AND AA) NOT GT) directly connected to I/O pad

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

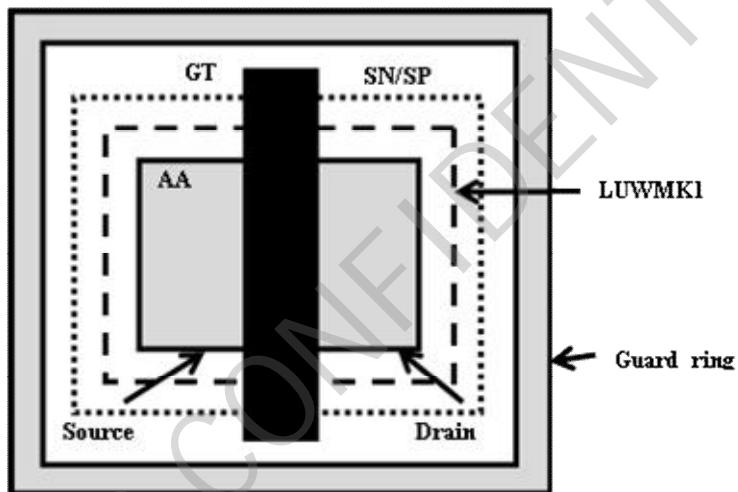
Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev. 2	Tech Dev Rev: 1.10.1	Page No.: 265/306
TD-LO28-DR-2006					

II. Definition of Latch up Dummy Layer

LUWMK1 (131;177) is a dummy layer for designer to waive latch up rules (LU.1~LU.3)

Note:

- 1) DRC will not check the area which is blocked by LUWMK1.
 - 2) It will have risk if designer draw this layer to exempt latch up rule check without silicon proven of package level latch up test.
 - 3) This layer is for DRC use, not a tapeout required CAD layer.
 - 4) Designer need to follow the following guidelines to draw LUWMK1.
- Draw LUWMK1 to fully cover AA injector, including the source, gate, drain, diode and resistor, but not necessarily to cover well pickup and guard-ring.



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 266/306
---------------------------	---	------------	----------------------	-------------------

III. DRC use the following features to check the connectivity:

- 1) The connectivity is formed by metal, via, ALPA, PA, MD and MTT2.
- 2) If resistors including AA resistor, poly resistor, well resistor are between PAD and AA injector, the connection is broken.
- 3) The switch of CONNECT_ALL_RESISTOR (to connect AA resistor, poly resistor, well resistor between PAD and AA injector) can control the connectivity of resistor. This switch is off by default.
- 4) DRC runset provides the following options for designer's control.

Option	Turn on CONNECT_ALL_RESISTOR
A	No (default)
B	Yes

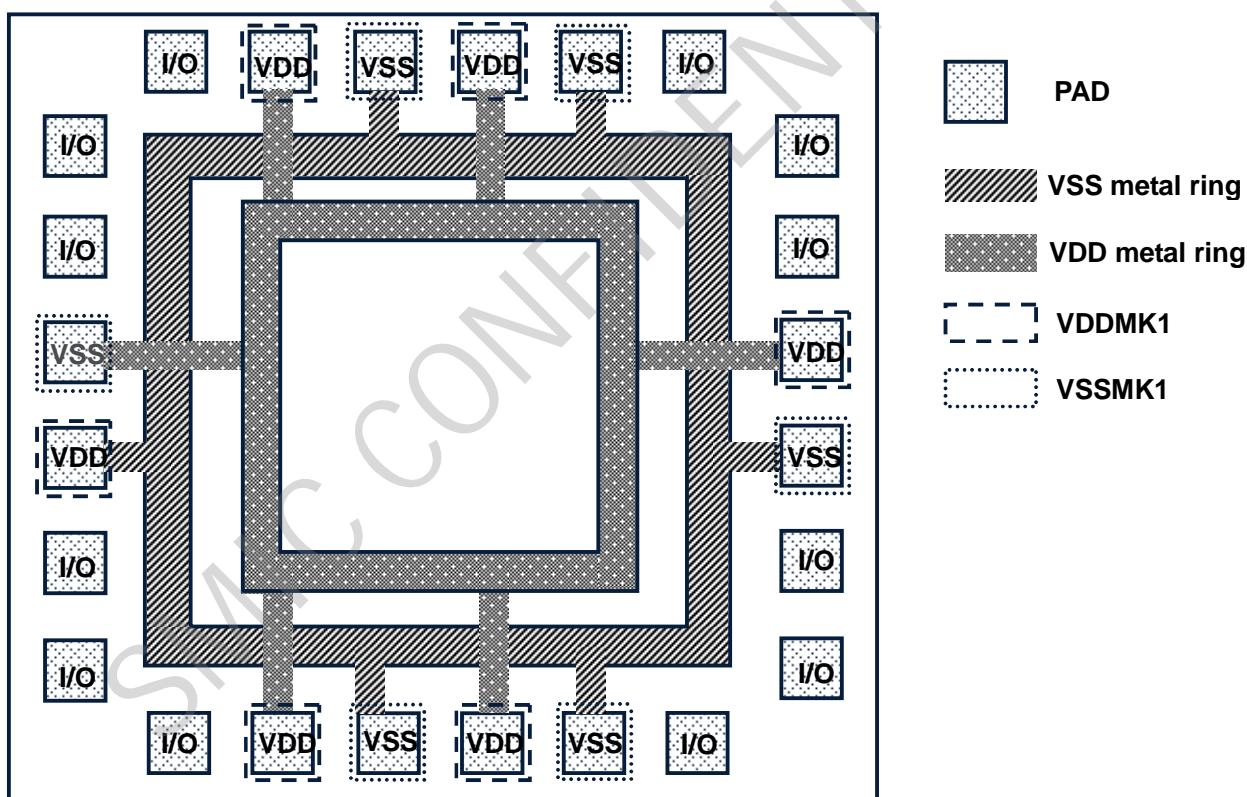
The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 267/306
---------------------------	---	------------	----------------------	-------------------

IV. DRC use the following features to identify the Power PAD and I/O PAD.

- 1) DRC will recognize the PAD by MD layer according to the connectivity defined in III.
- 2) Check the PAD with VDDMK1(131;175) and VSSMK1(131;176) to recognize Power PAD.
VDDMK1 (131;175): Marking layer for Power (Vdd) PAD for DRC use
VSSMK1 (131;176): Marking layer for Power (Vss) PAD for DRC use
- 3) Recognize Power PAD with the label of top level pin text of ALPATXT(83;2). This function is optional when VDDMK1 and VSSMK1 are not drawn by designer.
 - a. Control by the switch of #DEFINE_PAD_BY_TEXT. The switch is on by default.
 - b. Default Power text name are "?VDD?", "?VCC?", "?VSS?", "?GND?".

Except for the recognized Power PAD, all the other pads are defined as I/O PAD.



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

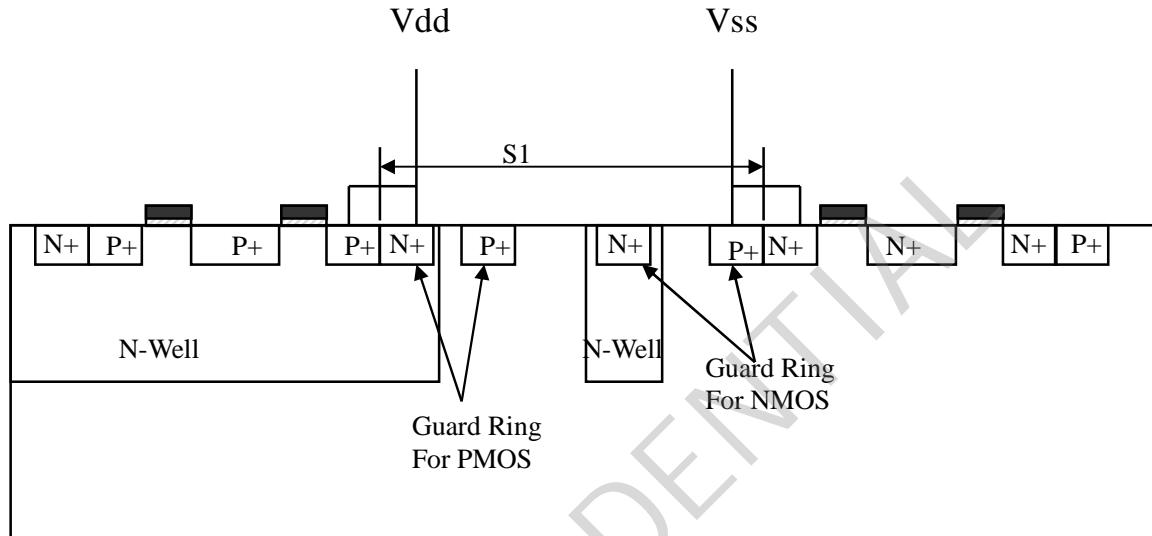


Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 268/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
LU.1 ^[G]	Guard ring should be used to surround AA injector or a group of AA injectors which are connected to an I/O pad. N+ injector must be surrounded by a P+ guard-ring. P+ injector must be surrounded by a N+ guard-ring.			
LU.2 ^[G]	Guard-ring width for AA injector connected to an I/O pad	\geq	0.2	um
LU.3 ^[G]	LU.3a-LU.3d define minimum space (S1) between NMOS and PMOS with either one of NMOS or PMOS AA connected to I/O pad. (Fig.1).			
LU.3a ^[G]	For core N/PMOS AA connected to an I/O pad Spacing between NMOS and PMOS.	\geq	2	um
LU.3b ^[G]	For 1.8V N/PMOS AA connected to an I/O pad Spacing between 1.8V NMOS and 1.8V/Core PMOS and Spacing between 1.8V PMOS and 1.8V/Core NMOS.	\geq	2.3	um
LU.3c ^[G]	For 2.5 V N/PMOS AA connected to an I/O pad Spacing between 2.5V NMOS and 2.5V/Core PMOS and Spacing between 2.5V PMOS and 2.5V/Core NMOS.	\geq	3.2	um
LU.3d ^[G]	For 3.3 V N/PMOS (2.5V overdrive) AA connected to an I/O pad Spacing between 3.3V NMOS and 3.3V/Core PMOS and Spacing between 3.3V PMOS and 3.3V/Core NMOS.	\geq	5	um
LU.4 ^[G]	Space (S2) from any point within the Source/Drain region to the nearest pickup AA region inside the same well for I/O and internal circuits. (Fig.2). DRC doesn't check OCCD region.	\leq	35	um
LU.5 ^[NC]	Space between I/O buffer and internal circuit region. (Fig.3).	\geq	15	um
LU.6 ^[NC]	All the guard rings and pickups should be connected to VDD/VSS with low series resistance. Contacts and Via's should be used as many as possible.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

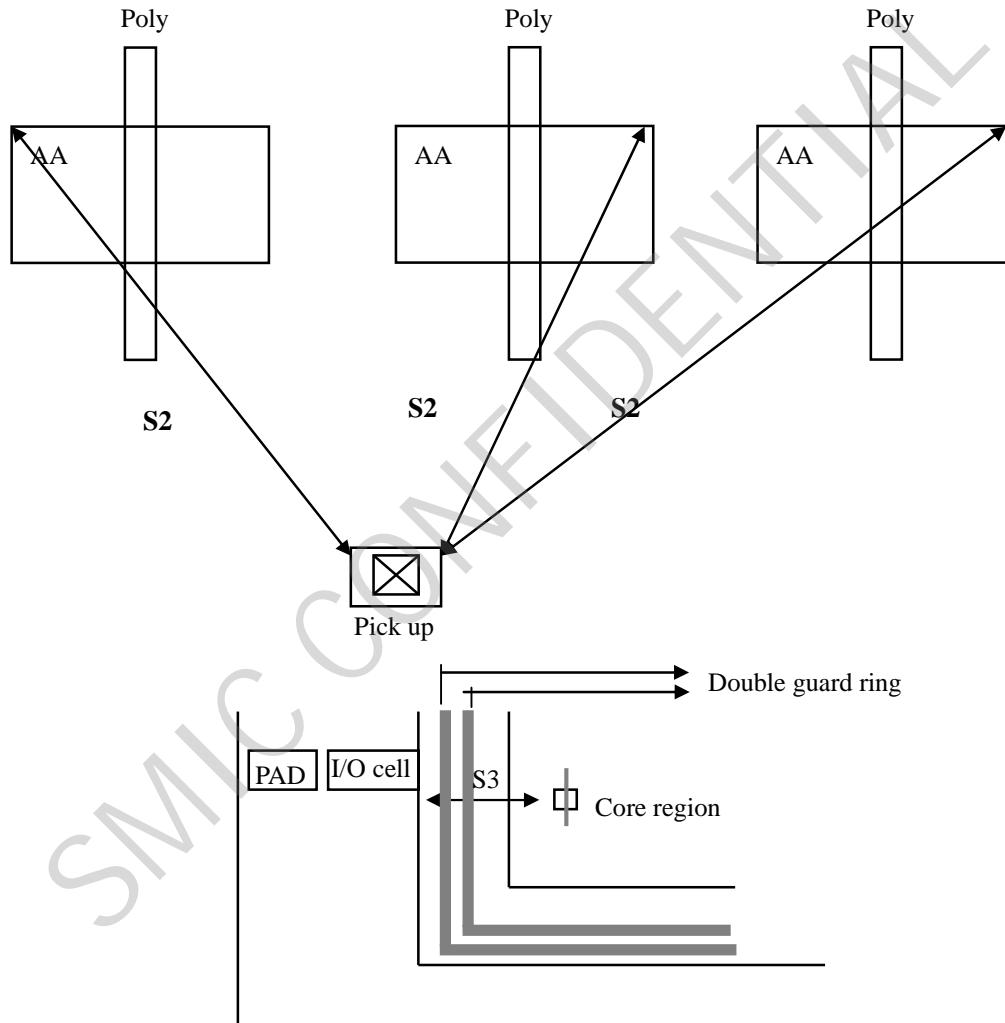
Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 269/306
---------------------------	---	------------	----------------------	-------------------



7.3.6 Fig.2 space (S1) between NMOS and PMOS connected to I/O pad

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 270/306
---------------------------	---	------------	----------------------	-------------------



7.3.6 Fig.3 illustration of the spacing of MOS AA to pickup AA (S2)

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 271/306
---------------------------	---	------------	----------------------	-------------------

7.3.8 Redundant Via insertion guidelines

For better yield and reliability, it is strongly recommended to utilize SMIC offered qualified Redundant via Auto Insertion utilities to do redundant via insertion which will replace the single square vias with the rectangular vias in 1x Vn(n=1-7) layers and replace the single square vias with double square vias in 2x Vn layers(W0,W1) wherever the layout and design rules permit. Application notice please refer to redundant via utilities; designers can download the utilities from SMIC NOW.

Features of this utility:

1. The utility strictly follows design rules for these layers Mn(n=1-8), Vn(n=1-7), W0,B1,W1,B2.
2. The new generated redundant vias will be marked by VnRM (n=1-7), W0RM, W1RM.
3. For putting redundant vias to replace the single square vias with the rectangular vias in 1x Vn layers or with double square vias in 2x Vn layers as required by design rules, metal lines can be extended. Therefore, designers should ensure LVS,DRC&timing result pass after using redundant via utilities. Designers can also refer to design reference flow offered by SMIC for LVS check and timing analysis.

The following layers will prevent the utility from redundant via insertion:

1. VnRB (n=1-7), W0RB,W1RB are the block layers for redundant via auto insertion. User can draw these layers where the DFM Via layout enhancement is not desired, especially for timing or resistance sensitive circuit area.
2. INDMY(212;0), LOGO(26;0), MARKG(189;0), MARKS(189;151), MARKF(190;0), MOMDMY(211;1), DSTR(138;0), JVARDUM(183;0), MnR(n=1-8), B1R, B2R, MnDUB (n=1-8),VnDUB(n=1-7),B1DUB,B2DUB, DUMBMB, INST/RFSRAM(60;0, 60;9 only follow main rule 1xRVn.7/1xRVn.8a/b/c to insert) are also redundant via block layers.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 272/306
---------------------------	---	------------	----------------------	-------------------

7.3.9 AA/GT/Metal/Via/ALPA Dummy insertion method selection guideline

- a. This is to guide designers about how to select dummy AA/POLY/P2/PSR/METAL/VIA/ALPA (AADUM, AADOP, GTDUM, GTDOP, P2DUM, PSRDUM, PSRNDUM, M1DUM~M8DUM, M1DOP~M8DOP, B1DUM, B2DUM, B1DOP, B2DOP, TM1DUM, TM2DUM, STM1DM, STM2DM, MTT2DM, ALDUM, V1DUM~V7DUM) insertion method in the utility provided by SMIC. Auto fills dummy is .1 and .7 data type.
- b. SMIC auto dummy fills insertion utility now supports both FEOL and BEOL insertion design manual.
- c. It's strongly recommended designers to use SMIC model based dummy insertion utility to do dummy insertion which has better performance to comply with density rules. Application notice please refer dummy insertion utility; designers can download these utilities from SMIC NOW. In order to get layout uniform and friendly globally for process control, you must to use SMIC's auto dummy insertion utility (document: TD-LO28-DT-2010).
- d. If designers still found DRC violations after use SMIC-provided dummy insertion utilities, SMIC will review the results and take proactive steps to close the DRC violation issues. If you use non-SMIC-provided dummy fill scripts, you must ensure DRC clean, and consult with SMIC.
- e. Please designers ensure timing closure post dummy insertion. It is strongly recommended design to check timing with dummy fillings.
- f. It is recommended to fill on the whole chip again; even dummy fill is done in blocks or chip. It is high risky to use dummy utility only on the instance blocks. We supposed STD cell block area is well defined with dummy fillers because STD cell block area cannot be inserted dummy by SMIC current auto filling dummy utilities.
- g. For RF device or the other concerning circuits with dummy auto insertion, you can draw dummy block layers to prevent dummy auto fill. It is suggest to manually draw dummy using manual draw dummy rules (.8 data type) but you should make sure this areas are meet DRC density requirement. Please refer to 7.1.11 Device table for dummy insertion.
- h. Need evaluate dummy fills related mask revision, please refer to 7.3.8 Mask Re-tooling Guidelines Related with Dummy Insertion.
- i. It is recommended to fill Metal/VIA dummy using SMIC P&R Metal/VIA Dummy utilities.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 273/306
-----------	-------------	--	------------	----------------------	-------------------

7.3.10 Mask Re-tooling Guidelines Related with Dummy Insertion

This section provides guidelines to judge which masks related with dummy insertion need to re-tool in case of GDS modification. Table 7.3.10.1 is the GDS and Mask relationship through dummy pattern interaction. The “Y” and “N” stands for impact level in this table: “Y” is high risk of mask re-tooling; need to run DRC to evaluate if need mask re-tooling, follow flow chart of 7.3.10.2; “N” is no need of re-tooling

7.3.10.1 Table of GDS and Mask relationship through dummy pattern interaction

Modified GDS Layer	Related Mask ->	AA	GT	Mn (n=1~8)	Vn (n=1~7)	Bn (n=1~2)	TMn (n=1~2)	STMn (n=1~2)	MTT2	ALPA
	Related Dummy Layer ->	AADUM AADOP	GTDUM GTDOP	MnDUM MnDOP	VnDUM	BnDUM BnDOP	TMnDUM	STMnDM	MTT2D M	ALDU M
AA	Y	Y	N	N	N	N	N	N	N	N
AADMP	Y	Y	N	N	N	N	N	N	N	N
GT	Y	Y	N	N	N	N	N	N	N	N
GTDMP	Y	Y	N	N	N	N	N	N	N	N
Mn	N	N	Y	Y	N	N	N	N	N	N
Vn	N	N	Y	Y	N	N	N	N	N	N
Bn	N	N	N	N	Y	N	N	N	N	N
TMn	N	N	N	N	N	Y	N	N	N	N
STMn	N	N	N	N	N	N	Y	N	N	N
MTT2	N	N	N	N	N	N	N	N	Y	N
ALPA	N	N	N	N	N	N	N	N	N	Y
DUMBA	Y	Y	N	N	N	N	N	N	N	N
DUMBp	Y	Y	N	N	N	N	N	N	N	N
DUMBm	N	N	Y	Y	Y	Y	Y	Y	Y	Y
MnDUB(n=1~8)	N	N	Y	Y	N	N	N	N	N	N
VnDUB(n=1~7)	N	N	Y	Y	N	N	N	N	N	N
BnDUB(n=1~2)	N	N	N	N	Y	N	N	N	N	N
TMnDUB(n=1~2)	N	N	N	N	N	Y	N	N	N	N
STMnDB(n=1~2)	N	N	N	N	N	N	Y	N	N	N
MTT2DB	N	N	N	N	N	N	N	N	Y	N
ALDUB	N	N	N	N	N	N	N	N	N	Y
NODMF	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
LOGO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RESAA	Y	Y	N	N	N	N	N	N	N	N
RESNW	Y	Y	N	N	N	N	N	N	N	N
INDMY	N	N	Y	Y	Y	N	N	N	N	Y
INST/RFSRAM	Y	Y	N	N	N	N	N	N	N	N

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 274/306
---------------------------	---	------------	----------------------	-------------------

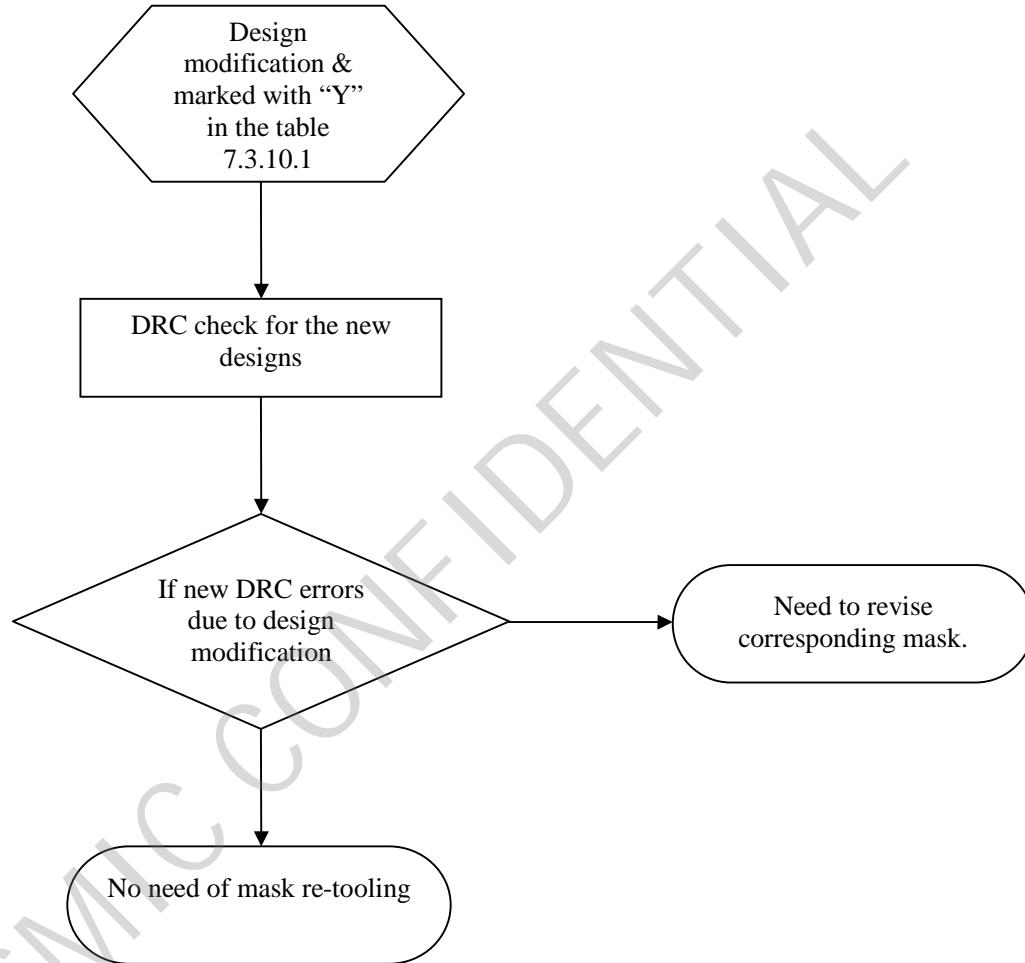
Related Mask ->	AA	GT	Mn (n=1~8)	Vn (n=1~7)	Bn (n=1~2)	TMn (n=1~2)	STMn (n=1~2)	MTT2	ALPA
Related Dummy Layer ->	AADUM AADOP	GTDUM GTDOP	MnDUM MnDOP	VnDUM	BnDUM BnDOP	TMnDUM	STMnDM	MTT2D M	ALDU M
MARKS/MAR KG	Y	Y	Y	Y	Y	Y	Y	Y	Y
P4	Y	Y	N	N	N	N	N	N	N

SMIC CONFIDENTIAL

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 275/306
---------------------------	---	------------	----------------------	-------------------

7.3.10.2 Flow chart of dummy related re-tooling evaluation procedures.



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 276/306
---------------------------	---	------------	----------------------	-------------------

7.3.11 Inline OCCD and OCOVL monitor cell guidelines

7.3.11.1 OCCD On chip CD cell guidelines

The purpose of on chip CD (CAD layer OCCD: 91;4) structure is to enable FEOL AA, Poly and BEOL metal layers' CD uniformity measurement and control within a large chip. This section describes the guidelines of OCCD structure placement.

SMIC provides OCCD GDS files for insertion. The CAD layer OCCD (91;4) is must for both FEOL and BEOL OCCD GDS cell. Two types of FEOL OCCD GDS are provided for different direction, one is horizontal direction FEOL OCCD cell, using CAD layer OCCDFH (91;6); another is vertical direction FEOL OCCD cell, using CAD layer OCCDFV (91;7). The Polys in OCCDFH or OCCDFV are all in vertical direction, which is same with the GATE direction of core device region. One BEOL OCCD GDS is provided, using CAD layer OCCDB (91;10). OCCD (91;4) layer drawn size is identical to each OCCD cell marker layer: OCCDFH, OCCDFV, OCCDB..

FEOL horizontal OCCD gds: IDCD_SMIC_PSFEOL_H0.gds

FEOL vertical OCCD gds: IDCD_SMIC_PSFEOL_V0.gds

BEOL OCCD gds: 28nm_OCCD_SMIC_BEOL.gds

SMIC also provides the OCCD block layer to exclude OCCD cell insertion, so if designers don't want to insert OCCD cell in certain design region, please draw OCCD block layers below:

FEOL OCCD cell block layer: OCCDFDB (91;8); BEOL OCCD cell block layer: OCCDBDB (91;9).

OCCD structures can be placed with following design rule or using SMIC auto insertion utility (xxx) to achieve suggested distribution.

Rule Number	Description	Operation	Design Value	Unit
OCCD.1 ^{[G][NC]}	Insert one OCCD structure in each 2000um x 2000um window of chip. No insertion of OCCD if window size smaller than 1000um x 1000um. It needs insert OCCD when chip window size is >1000um x 1000um, and <2000um x 2000um.			
OCCD.2 ^[G]	Space between two OCCDFH structures, Space between two OCCDFV structures, Space between OCCDFH and OCCDFV structures, Space between two OCCDB structures, which each OCCDFH/OCCDFV/OCCDB structure in each 2000um x 2000um window.	≥	150	um
OCCD.3 ^[G]	Space between OCCDFH/OCCDFV to AA, poly, SN, SP, LOGO, MARKS, MARKG, DUMBA, DUMBP outside of OCCD	≥	2	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 277/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
OCCD.4 ^[G]	At least insert one OCCD structure in two neighboring 2000um x 2000um window of chip.			
OCCD.5 ^[G]	OCCDFH/OCCDFV overlap of DG, PSUB, EFUSE, SAB, RESAA, RESP1, VARMOS, LVT_N, LVT_P, INST, ESDIO1, ESDIO2, BIPOLA, INDMY, MOMDMY is not allowed.			
OCCD.6 ^[G]	OCCDB can't overlap with CT, MnDUM(n=1~8), MnDOP(n=1~8), VnDUM(n=1~7), or INDMY			
OCCD.7 ^[G]	OCCDFH and OCCDFV can't overlap each other			
OCCD.8 ^[G]	OCCDFH and OCCDFV can't interact with OCQVL			
OCCD.9 ^[G]	Poly in OCCDFH/OCCDFV must be in vertical direction.			
OCCD.10 ^{[G][INC]}	Mirror or 180° rotation on OCCD structure in X,Y is allowed, 90° or 270° rotation is not allowed			
OCCD.11 ^{[G][INC]}	OCCD(91;4) must cover all OCCD cell structures, Following rules can be waived inside OCCD:			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 278/306
---------------------------	---	------------	----------------------	-------------------

7.3.11.2 OCOVL On chip cell guidelines

The purpose of on chip OVL (CAD layer, OCOVL: 91;5) structure is to enable the overlay measurement and control within a big chip. It will rationalize the overlay target distribution in field and enable high order correction modeling.

SMIC provides two types of on chip OVL marks, OVL mark of Poly to AA (OVL_GT_AA), and OVL mark of CT to Poly (OVL_CT_GT).

One OCOVL cell GDS is offered combined OVL_GT_AA and OVL_GT_AA in both horizontal and vertical direction. The CAD layer OCOVL (91;5) is must for on chip OVL cell.

OCOVL cell GDS : IDOVSMIC_N.gds

OCOVL structures can be placed with following design rule or using SMIC auto insertion utility (xxx) to achieve suggested distribution.

Rule number	Description	Operation	Design value	Unit
OCOVL.1 ^{[G][NC]}	Insert one OCOVL structure in each 2000x2000 um window of chip. No insertion of OCOVL if window size smaller than 1000um x 1000um. It needs insert OCCD when chip window size is >1000um x 1000um, and <2000um x 2000um.			
OCOVL.2 ^[G]	Space between two OCOVL structures DRC check methodology for the maximum space: (((NOT (OCOVL)) sd 6500um) su 6500um)	≥	2000	um
		≤	13000	um
OCOVL.3 ^[G]	Space between OCOVL to AA, Poly, SN, SP, CT, M1, LOGO, MARKS, MARKG, DUMBA, DUMBP, DUMBMB outside of OCOVL	≥	2	um
OCOVL.4 ^{[G][NC]}	Mirror or 180° rotation on OCOVL structure in X,Y is allowed, 90o or 270o rotation is not allowed			
OCOVL.5 ^{[G][NC]}	OCOVL (91;5) must cover OCOVL cell structures.			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 279/306
---------------------------	---	------------	----------------------	-------------------

7.4 Dummy Check Rule

Dummy AA include layer AADUM (10; 1) and AADOP (10; 7).
Dummy GT include layer GTDUM (30; 1) and GTDOP (30; 7).
Dummy P2 include layer P2DUM (31; 1).
Dummy 1x Metal include layer MnDUM (6n; 1) and MnDOP (6n; 7), n=1~8.
Dummy 2x Metal include layer BnDUM and BnDOP(14n; 1), n=1~2.
Dummy 8x Metal include layer TM1DUM (120; 1) and TM2DUM (122; 1).
Dummy 10x Metal include layer STM1DM (228; 1) and STM2DM (229; 1).
Dummy 1x Via include layer VnDUM (7n; 1), n=0~6.
Dummy MTT2 include layer MTT2DM (231; 1).
Dummy ALPA include layer ALDUM (83; 11).

AA dummy check rules				
Rule No.	Description	Operation	Design Value	Unit
DUMC_AA.00	DRC also check the poly dummy and flag the violations on main rules: AA.1, AA.3, AA.4a, AA.4c, AA.5, AA.22, AA.23a, AA.23b, AA.24, AA.25, AA.30, AA.31			
DUMC_AA.01	(AADUM or AADOP) width.	≥	0.1	um
DUMC_AA.02	Space between AADUM and AADUM.	≥	0.19	um
DUMC_AA.03	Space between AADUM and AADOP.	≥	0.2	um
DUMC_AA.04	Space between AADUM and GTDUM.	≥	0.025	um
DUMC_AA.05	Space between AADUM and GTDOP.	≥	0.2	um
DUMC_AA.06	Space between AADOP and AADOP outside DG/TG	≥	0.13	um
DUMC_AA.07	Space between AADOP and AADOP not outside DG/TG	≥	0.15	um
DUMC_AA.08	Space between AADOP and GTDOP.	≥	0.025	um
DUMC_AA.09	Space between AADOP and GTDUM.	≥	0.2	um
DUMC_AA.10	(AADUM or AADOP) area (in um2).	≥	0.03	um2
DUMC_AA.11	(AADUM or AADOP) must not interact (AA, Poly, AADMP, GTDMP, P2, GTFUSE, DUMBA, NODMF, RESNW, RESP1, MARKG, MARKS, INST, 2PSRAM) layers.			
DUMC_AA.12	Space between (AADUM or AADOP) and (DUMBA, NODMF, RESP1, MARKG, MARKS, INST, 2PSRAM) layers.	≥	0.4	um
DUMC_AA.13	Space between (AADUM or AADOP) and (AA, poly, AADMP, GTDMP).	≥	0.15	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 280/306
---------------------------	---	------------	----------------------	-------------------

DUMC_AA.14	Space between (AADUM or AADOP) and GTFUSE.	≥	1	um
DUMC_AA.15	(AADUM or AADOP) overlap with CT is not allowed.			um
DUMC_AA.16	Space between (AADUM or AADOP) and SAB.	≥	0.22	um
DUMC_AA.17	(AADUM or AADOP) enclosed by SAB, (AADUM or AADOP) cut SAB is not permitted	≥	0.22	um
DUMC_AA.18	Space between (AADUM or AADOP) and P2	≥	0.04	um
DUMC_AA.19	Space between (AADUM or AADOP) and RESNW	≥	0.5	um
DUMC_AA.20	Space between AADUM and NW.	≥	0.16	um
DUMC_AA.21	AADUM enclosed by NW, AADUM cut NW is not permitted.	≥	0.16	um
DUMC_AA.22	Space between AADOP and NW.	≥	0.1	um
DUMC_AA.23	AADOP enclosed by NW, AADOP cut NW is not permitted.	≥	0.1	um
DUMC_AA.24	Space between 45-degree AA and (AADUM or AADOP).	≥	0.45	um
DUMC_AA.25	Space between AADOP and PSUB.	≥	0.15	um
DUMC_AA.26	Space between AADUM and DUMBA.	≥	0.6	um
DUMC_AA.27	Space between (AADUM or AADOP) and DG/TG.	≥	0.08	um
DUMC_AA.28	(AADUM or AADOP) enclosed by DG/TG, (AADUM or AADOP) cut DG/TG is not permitted.	≥	0.08	um
DUMC_AA.29	Space between (AADUM or AADOP) and SP.	≥	0.07	um
DUMC_AA.30	(AADUM or AADOP) enclosed by SP, (AADUM or AADOP) cut SP is not permitted.	≥	0.07	um
DUMC_AA.31	Space between (AADUM or AADOP) and INDMY.	≥	1.2	um
DUMC_AA.32	AADUM extension GTDUM	≥	0.095	um
DUMC_AA.33	AADOP extension GTDOP	≥	0.075	um
DUMC_AA.34	Space between (AADUM or AADOP) and (OCCDFH, OCCDFV, OCOVL) mark layer.	≥	0.6	um
DUMC_AA.35	Space between (AADUM or AADOP) and CT	≥	0.05	um
Poly dummy check rules				
DUMC_GT.00	DRC also check the poly dummy and flag the violations on main rules: GT.1, GT.2, GT.10, GT.37, GT.40, GT.41, GT.42			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 281/306
---------------------------	---	------------	----------------------	-------------------

DUMC.GT.01	(GTDUM or GTDOP) width.	≥	0.03	um
DUMC.GT.02	(GTDUM or GTDOP) length.	≥	0.3	um
DUMC.GT.03	Space between (GTDUM or GTDOP) and (GTDUM or GTDOP) if at least one (GTDUM or GTDOP) width \geq 0.03um, and \leq 0.09um, and the parallel run length >0.09um.	≥	0.1	um
DUMC.GT.04	Space between (GTDUM or GTDOP) and (GTDUM or GTDOP) if at least one (GTDUM or GTDOP) width > 0.09um, and the parallel run length >0.09um.	≥	0.12	um
DUMC.GT.05	Space between GTDOP) and GTDOP.	≥	0.1	um
DUMC.GT.06	Space between GTDUM and GTDOP.	≥	0.2	um
DUMC.GT.07	(GTDUM or GTDOP) area (in um ²).	≥	0.0138	um ²
DUMC.GT.08	(GTDUM or GTDOP) must not interact (AA, Poly, AADMP, GTDMP, P2, GTFUSE, SAB, DUMBP, NODMF, RESAA, RESNW, MARKG, MARKS, INST, 2PSRAM) layers.			
DUMC.GT.09	Space between (GTDUM or GTDOP) and (DUMBP, NODMF, RESAA, RESNW, MARKG, MARKS, INST, 2PSRAM) layers.	≥	0.4	um
DUMC.GT.10	Space between (GTDUM or GTDOP) and (AA, poly, AADMP, GTDMP).	≥	0.15	um
DUMC.GT.11	Space between (GTDUM or GTDOP) and GTFUSE.	≥	1.30	um
DUMC.GT.12	Space between (AADUM or AADOP) and (GTDUM or GTDOP) on field oxide (On STI).	≥	0.025	um
DUMC.GT.13	(GTDUM or GTDOP) overlap with CT is not allowed.			
DUMC.GT.14	Space between (GTDUM or GTDOP) and SAB	≥	0.38	um
DUMC.GT.15	Space between GTDOP and P2	≥	0.04	um
DUMC.GT.16	Space between GTDUM and P2.	≥	0.3	um
DUMC.GT.17	Space between (GTDUM or GTDOP) and INDMY	≥	1.2	um
DUMC.GT.18	Space between (GTDUM or GTDOP) and CT	≥	0.08	um
DUMC.GT.19	Space between (GTDUM or GTDOP) and Poly_JOG	≥	0.17	um
DUMC.GT.20	GTDUM extension AADUM	≥	0.085	um
DUMC.GT.21	GTDOP extension AADOP	≥	0.08	um
DUMC.GT.22	(Purposely blank)			

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 282/306
---------------------------	---	------------	----------------------	-------------------

DUMC.GT.23	Space between (GTDUM or GTDOP) and (OCCDFH, OCCDFV, OCOVL) mark layer.	\geq	0.6	um
------------	--	--------	-----	----

P2 dummy check rules

DUMC.P2.00	DRC also check the poly dummy and flag the violations on main rules: P2.13, P2.15, P2.16			
DUMC.P2.01	P2DUM width.	\geq	0.08	um
DUMC.P2.02	P2DUM length.	\geq	0.15	um
DUMC.P2.03	Space between P2DUM and (P2, P2DUM).	\geq	0.09	um
DUMC.P2.04	Space between P2DUM and ((poly or GTDMP) or (GTDUM or GTDOP)). Overlap between P2DUM and ((poly or GTDMP) or (GTDUM or GTDOP)) is not allowed.	\geq	0.04	um
DUMC.P2.05	Space between P2DUM and ((AA or AADMP) or (AADUM or AADOP)). Overlap between P2DUM and ((AA or AADMP) or (AADUM or AADOP)) is not allowed.	\geq	0.035	um
DUMC.P2.06	Space between P2DUM and CT (overlap is not allowed).	\geq	0.02	um
DUMC.P2.07	Space between P2DUM and (DG or PSUB or TG).	\geq	0.06	um
DUMC.P2.08	P2DUM must not interact (AA, Poly, GTDMP, AADMP, GTDUM, AADUM, GTDOP, AADOP, P2, DG, PSUB, TG) layers.			
DUMC.P2.09	Area of P2DUM.	\geq	0.01	um ²
DUMC.P2.10	(P2 or P2DUM) full chip density	\geq	5%	
		\leq	12%	
DUMC.P2.11	Space between P2DUM and (OCCDFH, OCCDFV, OCOVL) mark layer.	\geq	0.6	um

M1 dummy check rules

DUMC.M1.00	DRC also check the M1 dummy and flag the violations on main rules: M1.1, M1.3, M1.5a, M1.5b, M1.5c, M1.5d, M1.5e, M1.5f, M1.5g, M1.6a, M1.6b, M1.8, M1.9, M1.17a, M1.17b, M1.17c, M1.18			
DUMC.M1.01	(M1DUM or M1DOP) width.	\geq	0.07	um
DUMC.M1.02	Space between two (M1DUM or M1DOP).	\geq	0.08	um
DUMC.M1.03	Dummy M1 area (um ²).	\geq	0.0238	um ²

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 283/306
---------------------------	---	------------	----------------------	-------------------

DUMC.M1.04	Space between (M1DUM or M1DOP) and (M1, V1).	≥	0.16	um
DUMC.M1.05	(M1DUM or M1DOP) can not interact GTFUSE; Space between dummy M1 and GTFUSE.	≥	1	um
DUMC.M1.06	(M1DUM or M1DOP) must not interact (M1, V1, NODMF, M1DUB, MARKG, MARKS, INST, 2PSRAM, OCCDB, DUMBMB) layers.			
DUMC.M1.07	Space between (M1DUM or M1DOP) and (NODMF, M1DUB, MARKG, MARKS, INST, 2PSRAM, OCCDB, DUMBMB) layers.	≥	0.6	um

1x Mn: 1x Metal (M2~M8) dummy check rules

DUMC.Mn.00	DRC also check the 1x Mn dummy and flag the violations on main rules: 1xMn.1, 1xMn.3, 1xMn.4a, 1xMn.4b, 1xMn.4c, 1xMn.4d, 1xMn.4e, 1xMn.4f, 1xMn.4g, 1xMn.4h, 1xMn.5a, 1xMn.5b, 1xMn.6 ^[R] , 1xMn.7, 1xMn.15a, 1xMn.15b, 1xMn.16, 1xMn.17			
DUMC.Mn.01	(MnDUM or MnDOP (n=2~8)) width.	≥	0.07	um
DUMC.Mn.02	Space between two (MnDUM or MnDOP (n=2~8)).	≥	0.08	um
DUMC.Mn.03	(MnDUM or MnDOP (n=2~8)) area (um ²).	≥	0.0238	um ²
DUMC.Mn.04	Space between (MnDUM or MnDOP (n=2~8)) and Mn ((M2~M8), Vn (n=2~7), Vn-1 (n=2~8)).	≥	0.16	um
DUMC.Mn.05	(MnDUM or MnDOP (n=2, 3)) cannot interact GTFUSE; Space between (MnDUM or MnDOP (n=2, 3)) and GTFUSE.	≥	1	um
DUMC.Mn.06	(MnDUM or MnDOP (n=2~8)) must not interact (Mn (M2~M8), Vn (V2~V7), Vn-1 (n=2~8), NODMF, MnDUB (n=2~8), MARKG, MARKS, (INST, 2PSRAM, only for M2~M3), OCCDB, DUMBMB) layers.			
DUMC.Mn.07	Space between (MnDUM or MnDOP, n=2~8) and (NODMF, MnDUB (n=2~8), MARKG, MARKS, (INST, 2PSRAM, only for M2~M3), OCCDB, DUMBMB) layers.	≥	0.6	um

2x Bn: 2x Metal (B1, B2) dummy check rules

DUMC.Bn.00	DRC also check the 1x Mn dummy and flag the violations on main rules: 2xMn.1, 2xMn.3a, 2xMn.3b, 2xMn.3c, 2xMn.3d, 2xMn.3e, 2xMn.4, 2xMn.5, 2xMn.6 ^[R] , 2xMn.7, 2xMn.9, 2xMn.10			
DUMC.Bn.01	Dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) width.	≥	0.20	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 284/306
---------------------------	---	------------	----------------------	-------------------

DUMC.Bn.02	Space between two dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP).	≥	0.20	um
DUMC.Bn.03	Dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) area (um2).	≥	0.16	um ²
DUMC.Bn.04	Space between dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) and Bn (B1, B2) pattern.	≥	0.30	um
DUMC.Bn.05	Dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) must not interact (Bn (B1, B2), BnDUB (B1DUB, B2DUB), NODMF, MARKG, MARKS, DUMBM) layers.			
DUMC.Bn.06	Space between dummy Bn (B1DUM, B1DOP, B2DUM, and B2DOP) and (BnDUB (B1DUB, B2DUB), DUMBM, NODMF) layers.	≥	0.50	um
DUMC.Bn.07	Space between dummy Bn (B1DUM, B1DOP, B2DUM, and B2DOP) and (MARKG, MARKS) layers.	≥	1.00	um

8x TMn: 8x Metal (TM1, TM2) dummy check rules

DUMC.TMn.0	DRC also check the 10xMn dummy and flag the violations on main rules: 8xTMn.1, 8xTMn.2a, 8xTMn .2b, 8xTMn .2c, 8xTMn .3, 8xTMn .4			
DUMC.TMn.1	Dummy TMn (TM1, TM2) width.	≥	0.75	um
DUMC.TMn.2	Space between two dummy TMn (TM1, TM2).	≥	0.75	um
DUMC.TMn.3	Dummy TMn (TM1, TM2) area (um2).	≥	1.5	um ²
DUMC.TMn.4	Space between dummy TMn (TM1, TM2) and TMn (TM1, TM2) pattern.	≥	0.75	um
DUMC.TMn.5	Dummy TMn (TM1, TM2) must not interact (TMn (TM1, TM2), TVn (TV1, TV2), NODMF, TMnDUB (n=1, 2), MARKG, MARKS, DUMBM) layers.			
DUMC.TMn.6	Space between dummy TMn (TM1, TM2) and (NODMF, TMnDUB (n=1, 2), MARKG, MARKS, DUMBM) layers.	≥	0.7	um

10x STMn: 10x Metal (STM1, STM2) dummy check rules

DUMC.STMn.00	DRC also check the 10x TMn dummy and flag the violations on main rules: 10xTMn .1, 10xTMn .2a, 10xTMn .2b, 10xTMn .2c, 10xTMn .3, 10xTMn .4			
DUMC.STMn.01	Dummy STMn (STM1DM, STM2DM) width.	≥	0.75	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 285/306
---------------------------	---	------------	----------------------	-------------------

DUMC.STMn.02	Space between two dummy STMn (STM1DM, STM2DM).	\geq	0.75	um
DUMC.STMn.03	Dummy STMn (STM1DM, STM2DM) area (um ²).	\geq	1.5	um ²
DUMC.STMn.04	Space between dummy STMn (STM1DM, STM2DM) and STMn (STM1DM, STM2DM) pattern.	\geq	0.75	um
DUMC.STMn.05	Dummy STMn (STM1DM, STM2DM) must not interact (STMn (STM1, STM2), STVn (STV1, STV2), NODMF, STMnDB (n=1, 2), MARKG, MARKS, DUMBMB) layers.			
DUMC.STMn.06	Space between dummy STMn (STM1DM, STM2DM) and (NODMF, STMnDB (n=1, 2), MARKG, MARKS, DUMBMB) layers.	\geq	0.7	um

V1 dummy check rules

DUMC.V1.00	DRC also check the V1 dummy and flag the violations on main rules: 1xVn.2a, 1xVn.2b, 1xVn.3, 1xVn.3a , 1xVn.3b, 1xVn.3c , 1xVn.3d , 1xVn.4, 1xVn.4a , 1xVn.4b , 1xVn.4c , 1xVn.4d , 1xVn.8			
DUMC.V1.01	V1DUM exact width (square shape).	=	0.05	um
DUMC.V1.02	Space between two V1DUM.	\geq	0.35	um
DUMC.V1.03	Enclosure by M1DUM; overlap with M1DOP is not permitted; and must be fully cover by M1DUM.	\geq	0.055	um
DUMC.V1.04	Enclosure by M2DUM; overlap with M2DOP is not permitted; and must be fully cover by M2DUM.	\geq	0.055	um
DUMC.V1.05	V1DUM must not interact (V1, M1, M2, V1DUB, MARKG, MARKS, NODMF, INDMY, OCCDBDB, DUMBMB) layers.			

1x Vn: 1x Via (V2~V7) dummy check rules

DUMC.1xVn.00	DRC also check the V1 dummy and flag the violations on main rules: 1xVn.2a, 1xVn.2b, 1xVn.3, 1xVn.3a , 1xVn.3b, 1xVn.3c , 1xVn.3d , 1xVn.4, 1xVn.4a , 1xVn.4b , 1xVn.4c , 1xVn.4d , 1xVn.8			
DUMC.1xVn.01	VnDUM (n=2~7) exact width (square shape).	=	0.05	um
DUMC.1xVn.02	Space between two VnDUM (n=2~7).	\geq	0.35	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 286/306
---------------------------	---	------------	----------------------	-------------------

DUMC.1xVn.03	Enclosure by MnDUM (n=2~7) and MnDUM (n=2~7) is the metal layer directly underneath VnDUM (n=2~7); overlap with MnDOP (n=2~7) is not permitted; and must be fully cover by MnDUM (n=2~7).	≥	0.055	um
DUMC.1xVn.04	Enclosure by MnDUM (n=3~8) and MnDUM (n=3~8) is the metal layer directly above VnDUM (n=2~7); overlap with MnDOP (n=2~7) is not permitted; and must be fully cover by MnDUM (n=3~8).	≥	0.055	um
DUMC.1xVn.05	VnDUM (n=2~7) must not interact (1x Vn, 1x Mn, 1x Mn+1, VnDUB (n=2~7), MARKG, MARKS, NODMF, OCCDBDB, INDMY, DUMBMB) layers.			

MTT2 dummy check rules

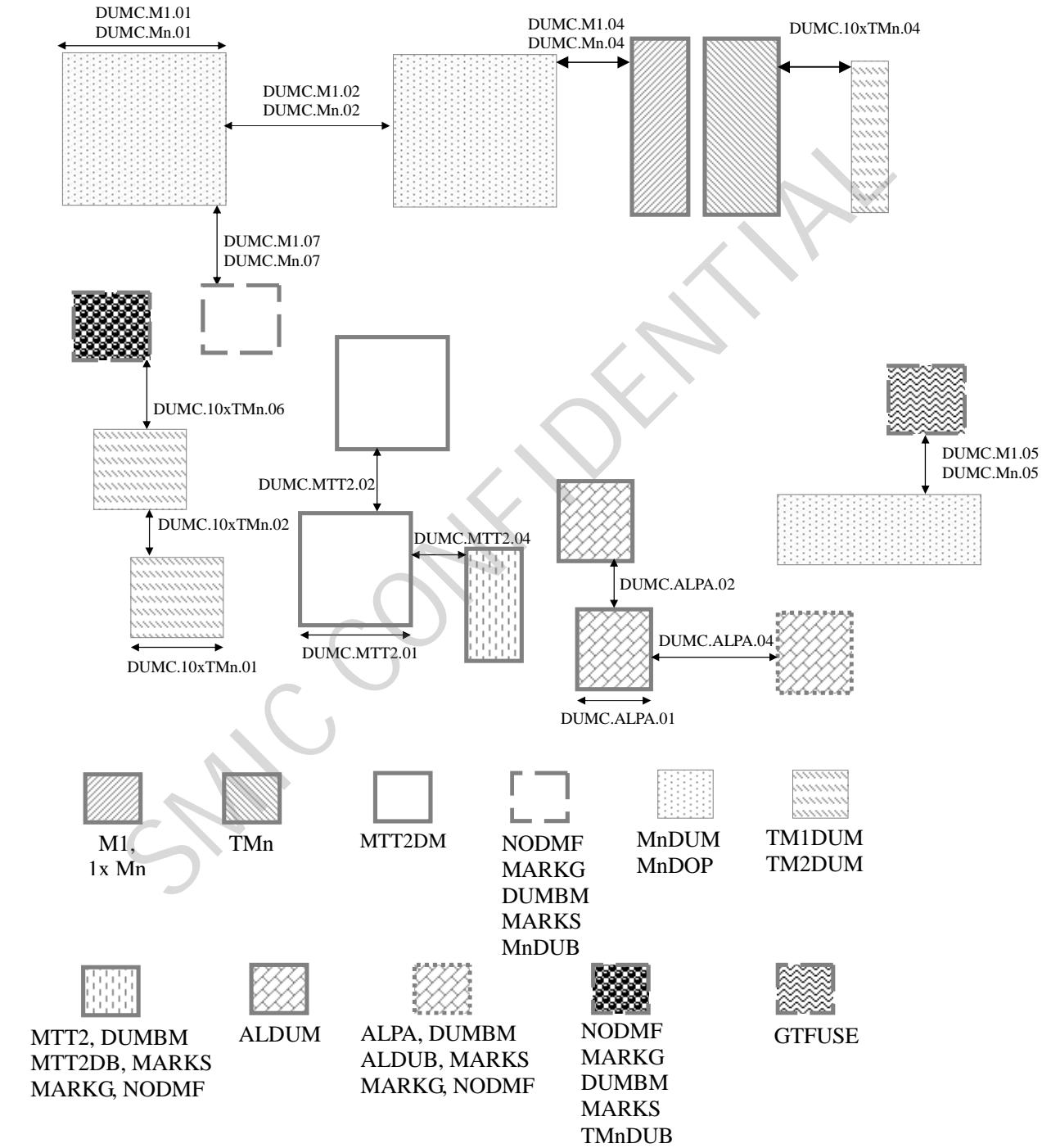
DUMC.MTT2.00	DRC also check the MTT2 dummy and flag the violations on main rules: MTT2.1, MTT2.2a, MTT2.2b, MTT2.6, MTT2.7, MTT2.14			
DUMC.MTT2.01	MTT2DM width.	≥	3.6	um
DUMC.MTT2.02	Space between MTT2DM and MTT2DM.	≥	1.78	um
DUMC.MTT2.03	MTT2DM must not interact (MTT2, NODMF, MTT2DB, MARKG, MARKS, DUMBMB) layers.			
DUMC.MTT2.04	Space between d MTT2DM and (MTT2, NODMF MTT2DB, MARKG, MARKS, DUMBMB) layers.	≥	1.78	um

ALPA dummy check rules

DUMC.ALPA.00	DRC also check the ALPA dummy and flag the violations on main rules: ALPA.1, ALPA.2			
DUMC.ALPA.01	ALDUM width.	≥	7	um
DUMC.ALPA.02	Space between ALDUM and ALDUM.	≥	3.6	um
DUMC.ALPA.03	ALDUM must not interact (ALPA, NODMF, ALDUB, MARKG, MARKS, DUMBMB) layers.			
DUMC.ALPA.04	Space between ALDUM and (ALPA, NODMF ALDUB, MARKG, MARKS, DUMBMB) layers.	≥	2.85	um

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.:	Doc. Title:	28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc. Rev. 2	Tech Dev Rev: 1.10.1	Page No.: 287/306
-----------	-------------	--	-------------	----------------------	-------------------



The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 288/306
------------------------------	---	---------------	----------------------	----------------------

7.5 Design for Manufacturability (DFM) Rules

7.5.1 Introduction

All the recommendations have been listed in the following DFM rules' section, it is recommended to follow them as much as possible, which can achieve large process window, better device and reliability performance, and higher yield.

DFM rules have been grouped with different priority levels. Higher priority indicates higher risk of manufacturability and yield loss when the rule is not obeyed. Users should follow DFM priority 1 and priority 2 rules strictly, DRC clean of DFM priority 1 and priority 2 rules is must for tape-out, if users intend to waive a violation of a priority 1 and priority 2 rules for any reason, need to review with SMIC before waiver. Priority 3 rules also impact manufacturability and yield, but they are not the gating items for tape-out.

DRC check methodology for DFM rules: there are two switches in DRC deck related with DFM rules. One switch is for DFM priority 1 and priority 2 rules which is turn on by default; another switch is only for priority 3 DFM rules, users can turn on it to check DFM priority 3 rules' DRC results.

7.5.2 DFM Rules

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
AA.1a ^[R]	Recommended AA width. DRC doesn't check INST region.	3	Device	\geq	0.06	off
AA.1b ^[R]	Recommended AA width,	3	Process	\leq	30	off
AA.4a ^[R]	Recommended space between two AAs to prevent AA bridge. DRC doesn't check INST, INDMY region.	3	Process	\geq	0.075	off
AA.9 ^[R]	Space between (AA or AA_DMY) DRC check maximum STI width. DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	3	Process	\leq	10	off

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 289/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
AA.21b ^[R]	(AA and AA_DMY) density. Density check window size: 20um*20um, step size: 10um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	3	Device	\geq	20%	off
AA.21f ^[R]	(AA or AA_DMY) density inside of the dummy block area(DUMBA), Density check window size: 20um*20um, step size: 10um DRC need check the design if DUMBA width is >5um and <20um, where density ratio= AA area/DUMBA area.	3	Process	$>$	20%	off
AADMP.18 ^[R]	(AA or AA_DMY) density. DRC check window follow: ((AA OR poly) INTERACT GATE) sizing up 2um) NOT ((AA OR poly) sizing up 0.15um)) This rule doesn't check DG, TG, VARMOS, NODMF, INST, OCOVL and OCCD regions.	3	Device	\geq	10%	off
NW.3 ^[R]	Space between NWs if at least one NW width<0.28um	2	Process	\geq	0.28	on
PSUB.3 ^[R]	Space of PSUBs if at least one PSUB width<0.28um	2	Process	\geq	0.28	on
LVT_N.3 ^[R]	Space between LVT_Ns with parallel run length >0.24um, when one LVT_N width >0.22um. DRC doesn't highlight the violation which INTERACT both SN and SP.	3	Process	\geq	0.18	off

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 290/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
LVT_P.3 ^[R]	Space between LVT_Ps with parallel run length >0.24um, when one LVT_P width >0.22um. DRC doesn't highlight the violation which INTERACT both SN and SP.	3	Process	\geq	0.18	off
GT.16f ^[R]	Space between GATE and neighboring (poly or POLY_DMY) for I/O NMOS/PMOS. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.51um. This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP,ESDPOB, LPDMY , LDBK and VARMOS region.	3	Device	=	0.18	off
GT.29a ^[R]	Extension of AA outside of (poly INTERACT CT) for core device with channel length \leq 0.09um. This rule isn't applicable for PSUB, VARMOS,ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, EFUSE,OCCD and INST region.	3	Device	\geq	0.205	off
GT.30a ^[R]	Extension of AA outside of (poly or POLY_DMY) for I/O device region. This rule isn't applicable for ESDIO1, ESDIO2,ESDCLP,ESDPOB, CLPDMY, VARMOS, LDMOS drain site region.	3	Device	=	0.155	off
GT.43 ^[R]	O-shape poly is not allowed, except the LOGO area.	3	Device			off
GT.45 ^[R]	((Poly NOT INSIDE (DG OR TG)) NOT P2) must be rectangle. This rule doesn't check NODMF, EFUSE, LOGO and INST region.	3	Device			off
GT.46 ^[R]	(((Poly NOT P2) OUTSIDE (DG or TG)) INTERACT AA)) must be rectangle. DRC doesn't check INST region.	3	Device			off

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 291/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
GT.49 ^[R]	In core device region, rectangle (poly NOT INTERACT AA) must be vertical, which is same as GATE poly direction. This rule doesn't check BIPOLA, DSTR, LOGO, and square pattern.	3	Device			off
GT.51 ^[R]	Recommended poly width on same AA must be same for core device with channel length \geq 0.15um. DRC doesn't check ESDIO1, ESDIO2, ESDCLP,ESDPOB,CLPDMY and INST regions.	3	Process			off
GTDMP.18 ^[R]	((Poly or POLY_DMY) NOT P2) density. DRC check region follow: (((AA OR poly) INTERACT GATE) sizing up 2um) NOT ((AA OR poly) sizing up 0.15um)) DRC doesn't check VARMOS, NODMF, INST, DG, TG, OCOVL and OCCD region.	3	Device	\geq	7%	off
P2.22 ^[R]	Recommended (P2 or P2DUM or P2DOP) density in full chip	2	Process	\geq	5%	on
SN.3 ^[R]	Space between SNs with parallel run length $>0.24\mu m$, when one SN width $>0.22\mu m$.	3	Process	\geq	0.18	off
SP.3 ^[R]	Space between SPs with parallel run length $>0.24\mu m$, when one SP width $>0.22\mu m$	3	Process	\geq	0.18	off
CT.6a ^[R]	CT enclosure by AA for a CT landed on AA when channel length $>0.09\mu m$ to avoid high RC. DRC doesn't check INST and OCOVL region	3	Process	\geq	0.015	off

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 292/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
CT.6b ^[R]	CT enclosure by AA for a CT landed on AA when enclosure by AA on either perpendicular direction $\geq 0.005\text{um}$ to avoid high RC. DRC doesn't check INST and OCOVL region	3	Process	\geq	0.04	off
CT.7e ^[R]	Recommended enclosure by poly when enclosure by poly on either perpendicular direction $\geq 0\text{um}$, and poly width $> 0.09\text{um}$.	3	Process	\geq	0.03	off
CT.9a ^[R]	Recommended enclosure by M1. DRC doesn't check INST region.	3	Process	\geq	0.01	off
CT.9b ^[R]	Recommended enclosure by M1 when enclosure by M1 on either perpendicular direction $\geq 0.01\text{um}$ and $< 0.02\text{um}$. DRC doesn't check INST region.	3	Process	\geq	0.035	off
CT.9c ^[R]	Recommended enclosure by M1 in the four sides. DRC doesn't check INST region.	3	Process	\geq	0.02	off
CT.9d ^[R]	Recommended enclosure by M1(M1 width $\geq 0.08\text{um}$, M1 and M1 space $< 0.06\text{um}$) This rule doesn't check two CTs (when CTs space $< 0.08\text{um}$)	3	Process	\geq	0.015	off
CT.10 ^[R]	Recommended inner vertex AA enclosure of CT. This rule doesn't check the N+/P+ pickup regions	3	Process	\geq	0.04	off
CT.9e ^[R]	Enclosure by M1 (metal width $\geq 0.33\text{um}$ and $\leq 0.7\text{um}$) when enclosure by M1 on either perpendicular direction $\geq 0.015\text{um}$. DRC violation is allowed if only one CT meets this rule for the redundant CTs pattern.	2	Process	\geq	0.02	on

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 293/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
CT.16^{[NC][R]}	Recommend put more CTs avoid high resistance wherever layout allows.	3	Device			
M1.4^[R]	Recommended M1 width, when 1. Space between M1 and two side-wall M1 is 0.05 um, with parallel run length> 0.16um; 2. CT/V1 enclosure by this M1: 0.02um≤E1≤0.03um; 3. Space between this M1 line end and M1: 0.07um≤S≤0.08um.	3	Process	≥	0.06	off
M1.7^[R]	Space between (M1 or dummy M1). DRC check maximum width of (NOT (M1 or dummy M1)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um, LOGO and INDMY.	3	Process	≤	4.5	off
M1.17a^[R]	Recommended M1 area	3	Process	≥	0.023	off
M1.21^[R]	M1 density (including dummy) in DUMB/M1DUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMB/M1DUB width is >5um and<125um, where density ratio= M1 area/ (DUMB/M1DUB) area.	2	Process	≥	10%	on
		2	Process	≤	85%	on
1xMn.6^[R]	Space between (1xMn or dummy 1xMn). DRC check maximum width of (NOT (1xMn or dummy 1xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um, LOGO and INDMY.	3	Process	≤	4.5	off
1xMn.15a^[R]	Recommended 1xMn area	3	Process	≥	0.023	off

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 294/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xMn.20^[R]	1xMn density (including dummy) in DUMB/MnDUB region. Density check window size: 125um*125um, step size: 62.5um.	2	Process	\geq	10%	on
	DRC need check the design if DUMB/MnDUB width is $>5\text{um}$ and $<125\text{um}$, where density ratio= 1xMn area/ (DUMB/MnDUB) area.	2	Process	\leq	85%	on
1xVn.3^[R]	1x Vn must be fully covered by M1 or 1xMn. Enclosure by 1xMn must follow (1x Vn.3a ^[R] and 1x Vn.3b ^[R]) or 1x Vn.3d ^[R] , and 1x Vn.3e ^[R] , and 1x Vn.3f ^[R] as below.	3	Device			off
1xVn.3a^[R]	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath 1x Vn.	3	Device	\geq	0.01	off
1xVn.3b^[R]	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction ≥ 0.01 and $<0.025\text{um}$ um and 1xMn is the metal layer directly underneath 1x Vn.	3	Device	\geq	0.05	off
1xVn.3d^[R]	Enclosure by M1 or 1xMn in four sides, and 1xMn is the metal layer directly underneath 1x Vn.	3	Device	\geq	0.025	off
1xVn.3e^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width $\geq 0.33\text{um}$ and $\leq 0.7\text{um}$, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.03	on
1xVn.3f^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width $>0.7\text{um}$, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.04	on

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 295/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xVn.4^[R]	1x Vn must be fully covered by 1xMn+1. 1xMn+1 enclosure 1x Vn must follow (1x Vn.4a ^[R] and 1x Vn.4b ^[R]) or 1x Vn.4d ^[R] , and 1x Vn.4e ^[R] , and 1x Vn.4f ^[R] as below.	3	Device			off
1xVn.4a^[R]	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above 1x Vn.	3	Device	\geq	0.01	off
1xVn.4b^[R]	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction $\geq 0.01\text{um}$ and $< 0.025\text{um}$ and 1xMn+1 is the metal layer directly above 1x Vn.	3	Device	\geq	0.05	off
1xVn.4d^[R]	Enclosure by 1xMn+1 in four sides and 1xMn+1 is the metal layer directly above 1x Vn.	3	Device	\geq	0.025	off
1xVn.4e^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width $\geq 0.33\text{um}$ and $\leq 0.7\text{um}$, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.03	on
1xVn.4f^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width $> 0.7\text{um}$, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.04	on
1xVn. 9^[R]	Recommended consecutive stacked 1x Vn layer, which has only one 1x Vn for each 1x Vn layer to avoid high Rc. This rule doesn't check MARKS and DUPMK1 region.	3	Process	\leq	4	off
1xVn. 10^[R]	Recommended space between 1x Vn and 1xVn+1, where 1xVn and 1xVn+1 at different net and parallel run length $> 0.02\text{um}$	3	Device	\geq	0.06	off

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 296/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xRVn.3e^[R]	Enclosure by M1 or 1x Mn (1x Mn width $\geq 0.33\mu m$ and $\leq 0.7\mu m$), when enclosure by 1xMn on either perpendicular direction $\geq 0.01\mu m$. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.03	on
1xRVn.3f^[R]	Enclosure by M1 or 1x Mn (1x Mn width $> 0.7\mu m$), when enclosure by 1x Mn on either perpendicular direction $\geq 0.03\mu m$. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.04	on
1xRVn.4e^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width $\geq 0.33\mu m$ and $\leq 0.7\mu m$), when enclosure by 1x Mn+1 on either perpendicular direction $\geq 0.015\mu m$. 1x Mn+1 is the metal layer directly above rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.03	on
1xRVn.4f^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width $> 0.7\mu m$), when enclosure by 1x Mn+1 on either perpendicular direction $\geq 0.03\mu m$. 1x Mn+1 is the metal layer directly above rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.04	on

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 297/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xRVn. 12^[R]	Recommended consecutive stacked rectangular 1x Vn layer, which has only one rectangular 1x Vn for each rectangular 1x Vn layer to avoid high Rc. This rule doesn't check MARKS and DUPMK1 region.	3	Process	\leq	4	off
1xRVn. 13^[R]	Recommended space between rectangular 1x Vn and 1xVn+1, where rectangular 1xVn and 1xVn+1 at different net and parallel run length > 0.02um	3	Device	\geq	0.06	off
2xMn.6^[R]	Space between (2xMn or dummy 2xMn). DRC check maximum width of (NOT (2xMn or dummy 2xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LOGO.	3	Process	\leq	4.5	off
2xMn.13^[R]	2xMn density (including dummy) in DUMB/2xMnDUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMB//2xMnDUB width is >5um and <125um, where density ratio= 2xMn area/ (DUMB/2xMnDUB) area.	2	Process	\geq	10%	on
		2	Process	\leq	85%	on
8xTMn .2d^[R]	Space between (8x TMn or dummy 8x TMn). DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	3	Process	\leq	12	off
8xTMn .5^[R]	8xTMn density (including dummy) in DUMB/TMnDUB. Density check window size: 125um*125um, step size:	2	Process	\geq	10%	on

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 298/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
	62.5um. DRC doesn't check DUPMK1 region. DRC need check the design if DUMB/TMnDUB width is >5um and <125um, where density ratio= 8xTMn area/(DUMB/TMnDUB) area.	2	Process	\leq	85%	on
8xTMn .6^[R]	TMn density (including dummy) in full chip	2	Process	\geq	20%	on
10xTMn .2d^[R]	Space between (10xTMn or dummy 10xTMn). DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	3	Process	\leq	12	off
10xTMn .6^[R]	10xTMn density (including dummy) in DUMB/TMnDUB. Density check window size: 125um*125um, step size: 62.5um. DRC doesn't check DUPMK1 region. DRC need check the design if DUMB/TMnDUB width is >5um and <125um, where density ratio= 10xTMn area/(DUMB/TMnDUB) area.	2	Process	\geq	10%	on
	2	Process	\leq	85%	on	
ALPA.3^[R]	ALPA density (including dummy) with 100um*100um window, with exemption of touching inductor.	2	Process	\geq	10%	on
MD.4^[R]	MD must be within BORDER (chip edge)	2	Process	\geq	3	on
RESAA.16^[R]	AA resistor must be rectangular.	3	Device			off
RESAA.9^[R]	It's strongly recommended space between CT and SAB for non-sicilidized AA resistor for spice model accuracy.	2	Device	=	0.12	on
RESAA.17^[R]	Recommended not use dog-bone design at the end of AA resistor for contact pick-up	3	Device			off

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 299/306
---------------------------	---	------------	----------------------	-------------------

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
RESNWAA.15^[R]	Recommended space between SAB and CT	3	Device	=	0.3	off
RESNWST.8^[R]	It's strongly recommended AA enclosure of CT (AA INTERACT RESNW)	3	Device	=	0.3	off
RESP1.9^[R]	It's strongly recommended space between CT and SAB for non-sicilidized poly resistor for spice model accuracy.	2	Device	=	0.12	on
RESP1.16^[R]	Poly resistor must be rectangular.	3	Device			off
IND.26^{[G][R]}	<p>It is recommended PSUB fully covers the inductor coil and guardring to achieve the high quality.</p> <p>DRC check method:</p> <p>PSUB fully cover ((AA INTERACT INDMY) INTERACT SP)).</p>	3	Device			off
ESD1.5a^[R]	The recommended CT enclosure by ESD1.	2	Device	\geq	0.4	on

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 300/306
---------------------------	---	------------	----------------------	-------------------

7.6 Current Density Guidelines

7.6.1 Metal line/CT/Vn/PA Current Density

Rule Number	Description	Operation	Design Value	Unit
Jmax is maximum DC current allowed per um of metal line width or per via of via/contact.				
Metal Line (metal line width: Wx0.9)				
CDR.1	Jmax of M1 line at 110°C	≤	1	mA/um
CDR.2	Jmax of 1xMn line at 110°C	≤	1	mA/um
CDR.3	Jmax of 2xMn line at 110°C	≤	1.9	mA/um
CDR.4	Jmax of 8xMn line at 110°C	≤	8.8	mA/um
CDR.5	Jmax of 10xMn line at 110°C	≤	12	mA/um
CDR.6	Jmax of MTT2 line at 110°C	≤	32	mA/um
CDR.7	Jmax of ALPA(14.5K) line at 110°C	≤	2.8	mA/um
CDR.8	Jmax of ALPA(28K) line at 110°C	≤	5.6	mA/um
CT and Via				
CDR.9	Jmax of CT at 110°C	≤	0.083	mA/CT
CDR.10	Jmax of 1xVn at 110°C	≤	0.04	mA/via
CDR.11	Jmax of 2xVn at 110°C	≤	0.16	mA/via
CDR.12	Jmax of 8xVn at 110°C, for the 8xVn landing on 1xMn	≤	1	mA/via
CDR.13	Jmax of 8xVn at 110°C, for the 8xVn landing on 2xMn	≤	1.9	mA/via
CDR.14	Jmax of 8xVn at 110°C, for the 8xVn landing on 8xMn	≤	3	mA/via
CDR.15	Jmax of 10xVn at 110°C, for the 10xVn landing on 1xMn	≤	1.2	mA/via
CDR.16	Jmax of 10xVn at 110°C, for the 10xVn landing on 2xMn	≤	2.7	mA/via
CDR.17	Jmax of 10xVn at 110°C, for the 10xVn landing on 8xMn	≤	5.4	mA/via
CDR.18	Jmax of UTV(LT) at 110°C, for the UTV(LT) landing on 1xMn	≤	1	mA/via

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 301/306
---------------------------	---	------------	----------------------	-------------------

Rule Number	Description	Operation	Design Value	Unit
CDR.19	Jmax of UTV(LT) at 110°C, for the UTV(LT) landing on 2xMn	≤	1.9	mA/via
CDR.20	Jmax of UTV(LT) at 110°C, for the UTV(LT) landing on 8xMn	≤	3	mA/via
CDR.21	Jmax of PA(size=3um) line at 110°C	≤	7	mA/PA
CDR.22	Jmax of PA(size=2um) line at 110°C	≤	5.4	mA/PA

Note:

1. Suggest use as much as CT/Via numbers in layout design for reliability margin agreement.
2. Minimal required metal width and CT/Via numbers are determined by allowed design current.
3. Preferentially use maximal CT/Via design numbers for perpendicular current

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.

Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 302/306
---------------------------	---	------------	----------------------	-------------------

7.6.2 Metal line Irms definition

$$I_{rms} = \sqrt{\frac{1}{t_w} \int_0^{t_w} i^2(t) dt}$$

Tw=Irms check period. Typically, current period.

i(t)= current

W(in um): the width of the metal line

ΔT (°C): the temperature rise due to Joule heating

Conduction Layer	Operation	Irms	Unit
M1	≤	SQRT[ΔT * (11.06 * (w*0.9)^2 + 8.44 * (w*0.9))]	mA
M2	≤	SQRT[ΔT * (5.11 * (w*0.9)^2 + 7.73 * (w*0.9))]	mA
M3	≤	SQRT[ΔT * (3.55 * (w*0.9)^2 + 4.47 * (w*0.9))]	mA
M4	≤	SQRT[ΔT * (3.52 * (w*0.9)^2 + 6.17 * (w*0.9))]	mA
M5	≤	SQRT[ΔT * (3.15 * (w*0.9)^2 + 4.91 * (w*0.9))]	mA
M6	≤	SQRT[ΔT * (3.03 * (w*0.9)^2 + 5.22 * (w*0.9))]	mA
M7	≤	SQRT[ΔT * (2.78 * (w*0.9)^2 + 4.14 * (w*0.9))]	mA
M8	≤	SQRT[ΔT * (6.67 * (w*0.9)^2 + 3.3 * (w*0.9))]	mA
8xTM	≤	SQRT[ΔT * (9.81 * (w*0.9)^2 + 51.04 * (w*0.9))]	mA
10xTM	≤	SQRT[ΔT * (11.96 * (w*0.9)^2 + 62.84 * (w*0.9))]	mA
MTT2	≤	SQRT[ΔT * (62.83 * (w*0.9)^2 + 267.4 * (w*0.9))]	mA
ALPA(14.5K)	≤	SQRT[ΔT * (12.86 * (w*0.9)^2 + 43.03 * (w*0.9))]	mA
ALPA(28K)	≤	SQRT[ΔT * (24.19 * (w*0.9)^2 + 116.38 * (w*0.9))]	mA

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 303/306
---------------------------	---	------------	----------------------	-------------------

7.6.3 Temperature coefficient

7.6.3.1 Cu Temperature coefficient

Temperature C	100	105	110	115	120	125
Factor	2.149	1.459	1	0.692	0.484	0.341

7.6.3.2 Contact(CT) temperature coefficient

CT temperature coefficient is the same as Cu.

7.6.3.3 Aluminum temperature coefficient

Temperature C	70	85	100	110	125
Factor	3.443	2.097	1.329	1	0.6707

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 304/306
---------------------------	---	------------	----------------------	-------------------

8. Attachment:[28_Sealring_Sample_V1.2_0825.gds](#)

Note: Any DRC violation please confirm with SMIC.

Change History:

Document Change History				
Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
OR	1.0	2014-07-09	Jenny Pang	Initial for 28nm poly SION.
1R	1.10	2015-01-15	Jenny Pang	<ol style="list-style-type: none">1. 7.1.3: exclude OCCDB in DGR.1;update DGR4 for INDMY checking.2. 7.1.5: add density check DRC check guideline.3. 7.1.6: add explanation for metal option table.4. 7.1.8: Add LUWMK1,M1B,M2B,M3B,M4B,M5B,M6B, M7B,M8B,TM1B,TM2B,B1B,B2B,STM1B,STM2B, MTT2B,ALPAB, PRBOUN,ERCMK1, RFDN5T layer; modify DUMBM layer definition; add sequence No.5. 7.1.9 Mask layer mapping table: add MVN,NDRN, ULVN,ULVP layer, and adjust layer sequence based on process sequence.6. 7.1.10: add ESD device notes, update TG from "0" to "*" for resistor device to align DG.7. 7.1.12: add LDMOS drain definition.8. 7.1.15: add DRC Connectivity Definition.9. 7.2.2: AA.6: change rule value to 0.13; change 5um to 0.09um for AA.27a/b; AA.23: optimize non-DRC check condition.10. 7.2.3/10: downgrade AADMP.18/GTDMP.18 to DFM priority3 rule and exclude OCOVL; add max rule for AADMP.1; add AADMP.9/GTDMP.8; add min rule for AADMP.17; change AADMP.13 value to 0.08um; change GTDMP.24 to main rule.11. 7.2.6: add P+AA for LVT_N.11 and add N+AA for LVT_P.11.12. 7.2.7/7.2.8: add DG.16/17, TG.15/16.

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 305/306
---------------------------	---	------------	----------------------	-------------------

		<p>13. 7.2.9:GT.5/36: exclude OCOVL; GT.6a/7a: exclude VARMOS; GT.8d: exclude FUSEMK1,delete EFUSE in non-DRC check condition; GT.22: optimize non-DRC check condition; GT.27: exclude INDMY; GT.30a/30a^[R]: change LDBK to LDMOS drain site; GT.35: change channel length to >0.06um; GT.36^[R]:change to main rule; GT.31/55: optimize description;GT.28/56: optimize voltage.</p> <p>14. 7.2.13/14: add SN.15b/SP.15b, change SN.15/SP.15 rule No to SN.15a/SP.15a.</p> <p>15. 7.2.15: SAB.5/12: exclude INDMY.</p> <p>16. 7.2.16: add it for process concern.</p> <p>17. 7.2.17: CT.6/6a/6b/6c//6a^[R]/6b^[R]:exclude OCOVL. CT.9/9a/9b/9c: exclude OCCD;CT.12: exclude INDMY.</p> <p>18. 7.2.18:M1.7^[R]: exclude INDMY; M1.11c: change runlength to -0.12; M1.12-15: add non-DRC check condition; M1.17b/17c: update non-DRC check condition; add M1.30; delete Note4.</p> <p>19. 7.2.19 1xMn.1:update non-DRC check condition; 1xMn.6^[R]/1xMn.24: exclude INDMY;1xMn.10-13: add non-DRC check condition;1xMn.15b: update non-DRC check condition;delete Note4.</p> <p>20. 7.2.20 1xRVn.7:delete item2 condition c),update condition a);1xRVn.8:exclude INST.</p> <p>21. 7.2.21: 2xMn.1: add non-DRC check condition.</p> <p>22. 7.2.24 8xTMn.2c: change rule value to 1.5; 8xTMn.5/.5^[R] : update non-DRC check condition.</p> <p>23. 7.2.26: 10xTMn.5/.6^[R]: update non-DRC check condition.</p> <p>24. 7.2.27: LT.4/6:optimize description and change LT.6 value to 0.3.</p> <p>25. 7.2.28: MTT2.5:update description, change rule value to 1.5; delete INDMY in MTT2.8/9.</p> <p>26. 7.2.29:PA.4: optimize description.</p> <p>27. 7.2.32 DUP: add 8xTV in DUP.5,update Notes.</p> <p>28. 7.2.35/37: RESAA.5^[G]/RESP1.5^[G]: change rule value from 0.19 to 0.1; add RESAA.13^[G]/RESP1.14^[G].</p> <p>29. 7.2.38: EFU.6: add 0.1um in rule value; EFU.8:change rule value to 0.022um.</p> <p>30. 7.2.43: ANT.GT9a/9b/11:change 14K to 14.5K.</p>
--	--	---

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO28-DR-2006	Doc. Title: 28nm Logic Low Power (Poly/SION) 1.05V/1.8V/2.5V Design Rules	Doc.Rev: 2	Tech Dev Rev: 1.10.1	Page No.: 306/306
---------------------------	---	------------	----------------------	-------------------

				<p>31. 7.3.3: overall update inductor rule based on inductor design.</p> <p>32. 7.3.4: new define LDMOS rule.</p> <p>33. 7.3.5 seal ring section:update Table1;separate table2 SR.2^[G]/3^[G]/4^[G]/5^[G] to two rules at straight direction and at 45 degree angle area; and change SR.6^[G]/7^[G] rule value, update SR.14^[G] description;delete [G] for SR.11-14.7.3.5:</p> <p>34. 7.3.6: add DRC check method, update LU.1/2/3/6 description, exclude OCCD in LU.4.</p> <p>35. 7.3.7: ESD.5[G]/6[G] :delete; ESD.8[G]: Change rule value to 0.6.</p> <p>36. 7.3.8: update it based on latest utility.</p> <p>37. 7.3.10:add Bn and STMn related layer.</p> <p>38. 7.4: DUMC.GT.07: change rule value to 0.0138; delete DUMC.GT.22;update DUMC.Mn.00, DUMC.P2.05, DUMC.M1.06-07, DUMC.Mn.05-07.</p> <p>39. 7.5.2 DFM: define 2xMn.6^[R]/13^[R];delete MD.6^[R]/ ALPA.4^[R];change AA.1b^[R]/ AA.21f^[R]/ M1.7^[R]/ 1xMn.6^[R]/ 2xMn.6^[R]/ 8xTMn .2d^[R]/ 10xTMn .2d^[R] to pri 3;add IND.26^{[G][R]} and LD.13^{[G][R]} ; 8xTMn.5/.5^[R]/10xTMn.5/.6^[R]: update non-DRC check condition.</p> <p>40. Update seal ring GDS: change 8xTM/TV size, and add 10xTMn/TVn/LT design.</p>
2	1.10.1	Minna Xu	2016-09-09	<p>1. Update 8 attachment: in order to solve the DRC violation of seal ring, PIE updated the GDS sample</p> <p>2. Add "Note: Any DRC violation please confirm with SMIC" in item 8.</p>

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.