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Security Level:					
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Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description	
0T	0.5	2013-11-21	Jenny Pang	Initiate	
1T	0.5	2014-02-07	Jessy Xu	1. Only upload one attachment of the seal ring GDS sample without modifying any rule. 2. Update the float chart in 7.3.7.2	
2R	1.0	2014-06-25	Jenny Pang	<p>Overall update design rule which is based on process/electric/reliability data, device strategy and customer design request.</p> <p>1. 7.1.2/3/5-10/12: update. 2. 7.1.14.1: update figure in flow chart. 3. Replace ESDIO2 with ESDIO2, ESDCLP, ESDPOB, CLPDMY for the related rules. 4. 7.2.1: update DNW.8/9. 5. 7.2.2: update AA.1/4/13/37/2^[R]/6/7/14/15/20/23/31/32/33/36a/36b /43/20; add AA.8/9/10/12/31b/34; change AA.1 max rule to AA.1b^[R] DFM2 rule. 6. 7.2.3: update AADMP.5/8/13/15-18; add AADMP.10. 7. 7.2.4: update NW.8/9/10. 8. 7.2.5: update PSUB.6/10/11. 9. 7.2.6-9: separate N/P type layer; 10. 7.2.10/11: update DG3/4b/5/6b/13/14, TG3/4b/5/6b/13/14. 11. 7.2.12: update GT.2/6/8b/9c/10-12/14a/14b/16^[R]/17^[R]/19/20/23/24a /33/40/31/32/37^[R]/42a/42b/43/45/50/54/56; add GT.15/24b/24e/28a/ 28b/ 29a^[R]/57; delete GT.32/55. 12. 7.2.13: update GTDMP.5/21/23/18/25/26/30/32. 13. 7.2.14: update GB.1^[NC]/12; add GB.11. 14. 7.2.15: update P2. 5/6/11/13/20/22^[R]. 15. 7.2.16/17: update SN.11-14/23/25/29, SP.6/11/12/14/24/26/29. 16. 7.2.18: update SAB.5/9/10/11/13; add SAB.6b/6c; delete SAB.8. 17. 7.2.19: update P4.8-10/12/15; add P4.7. 18. 7.2.21: update CT.1/4a/4b/4d/5/7a/7b/7d/7e/8a/8b/9a-9c/12; add CT.6c/13/7e^[R]/9^[R]/9a^[R]/9b^[R]/9c^[R]/ 9d^[R]/10^[R]/18; delete rectangular CT. 19. 7.2.22: update M1.2b/5d/5e/14/15/18/2a/11/12/13/17/17^[R]/20; add M1.4^[R]/11b/11c/17b/17c/22/23/25-29; delete M1.8. 20. 7.2.23: update 1xMn.1/2b/4a/4e/4f/12/13/17/9/10/11/15/15^[R]/16; add 1xMn.9b/9c//15b/21-24/26-30.</p>	

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		<p>21. 7.2.24.1: update 1xVn.1/5b/6b; add 1xVn.3^[R]/3a^[R]/ 3b^[R] / 3e^[R] / 3f^[R] /3d^[R]/4^[R]/4a^[R] / 4b^[R] / 4e^[R] / 4f^[R] / 4d^[R]/9^[R]/8.</p> <p>22. 7.2.24.2: update 1xRVn.1a/1b/3e^[R]/5b/5c/6a/6b/6c/7/8; add 1xRVn.8b/8c/11/12^[R]/13^[R].</p> <p>23. 7.2.27: update 8xTVn.1/7; add 8xTVn.8.</p> <p>24. 7.2.28: update 8xTMn.1/ 2d^[R]/6.</p> <p>25. 7.2.29: update 10xTVn.1/2c/7; add 10xTVn.8.</p> <p>26. 7.2.30: update 10xTM.3/4/1.</p> <p>27. 7.2.32: update MTT2.6/7/8/2.3/14; delete MTT2.4/5/10/11/12/13.</p> <p>28. 7.2.34: update ALPA.2/7/4.</p> <p>29. 7.2.35: delete MD.6^[R].</p> <p>30. 7.2.37/38: update.</p> <p>31. 7.2.39: change RESAA.7 value; update RESAA.9 as DFM2 rule and description; add RESAA.22; add RESAA.2 max rule.</p> <p>32. 7.2.40: update RESNWAA.6/7, RESNWST.6/7.</p> <p>33. 7.2.41: update HR.21/22/25/12/14/ 16/17n; add HR.28; delete HR.11.</p> <p>34. 7.2.42: update MR.5/8/11/13/14/18; delete MR.10.</p> <p>35. 7.2.47: update ANT.GT1/ 2/ 9a/ 9b/11,add ANT.GT12-15.</p> <p>36. 7.3.1: update VAR.3^[G]/9^[G]/11^[G]/10^[G]/12^[G] 1^[G]/2^[G]/11^[G]/16^[G]/17^[G] /19^[G]/4^[G]/5^[G]/14^[G]/15^[G]; add VAR.1b^[G]/2b^[G]; delete VAR.6^[G]/13^[G].</p> <p>37. 7.3.2: update EFU.2b^[G]/ 2c^[G].</p> <p>38. 7.2.20/25/26/31/43-46;7.3.3/4/11: add SiGe density, 2xMn/Vn, UTV, diode, MOM, inductor, LOGO, metal low density rule, BIPOLA, inline OCCD/OCOVL by design request.</p> <p>39. 7.3.6: add ESD 2.5V rules, and add ESD power clamp/ diode guideline by designer request.</p> <p>40. 7.4: update dummy check rule to align the latest dummy insertion script.</p> <p>41. 7.5.2:update DFM rule to align the recommended rules.</p> <p>42. 7.6: update current density rule based on electric data.</p> <p>43. 7.3.5,8: Add small size ring in seal ring GDS to improve performance, update rule to match design.</p> <p>44. Updated item 8 and add gds IDOVSMIC_N.gds IDCD_SMIC_FEOL_H0.gds IDCD_SMIC_FEOL_V0.gds 28nm_OCCD_SMIC_BEOL.gds</p>			

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**SEMICONDUCTOR MANUFACTURING INTERNATIONAL
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Version 1.0

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1. Title:

28nm Logic HKMG 0.9V/1.8V/2.5V Design Rules

2. Purpose:

Patterns Design Guideline for 28nm Logic HKMG Process

3. Scope:

SMIC TD

4. Nomenclature:

NA

5. Reference:

NA

6. Responsibility:

Technology Development Center

7. Subject content:**7.1 User Guideline****7.1.1 Introduction**

This document provides 32nm layout dimension, 28nm logic HKMG product is 90% liner shrinkage from this 32nm layout dimension and layout 90% shrinkage is implemented in SMIC after product tape-out.

7.1.2 Grid size

1. Layout grid size is 0.001um.
2. Design geometry grid size:
0.005um (OUTSIDE ((INST OR RFSRAM) **OR FUSEMK1**) covered region);
0.001um (NOT OUTSIDE ((INST OR RFSRAM) **OR FUSEMK1**) covered region).

7.1.3 Design requirements

Designers should follow design requirement guidelines in this section in order to reduce the OPC loading and then enhance the OPC efficiency.

Guidelines number	Description
DGR.1	All the geometry design must be an integer multiple of 0.005um (OUTSIDE ((INST OR RFSRAM) OR FUSEMK1) OR INDMY) covered region). DRC check DNW, AA, AADMP, NW, PSUB, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, UHVT_N, UHVT_P, DG, TG, GT, GTDMP, GBU15, GBD20, P2, SN, SP, SAB, P4, CT, M1, 1xMn, 1xVn, 2xMn, 2xVn, 8xTVn, 8xTMn, 10xTVn, 10xTMn, LT, MTT2, PA,

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Guidelines number	Description
	NODMF, BORDER layers
DGR.2 ^[NC]	All the geometry design must be an integer multiple is 0.001um (NOT OUTSIDE ((INST OR RFSRAM) OR FUSEMK1) OR INDMY) covered region).
DGR.3 ^[NC]	Design geometry shape must be polygons
DGR.4	Only shapes of geometry that are orthogonal or 45-degree angle are allowed. DRC doesn't check MARKS and MD region.
DGR.5 ^[NC]	Only unidirectional, straight transistor channels are allowed
DGR.6 ^[NC]	Recommended to design simple rectangular shape geometry as possible, avoid L, U, H, or O shapes.
DGR.7 ^[NC]	All line-end are must be rectangular
DGR.8 ^[NC]	Self-intersecting shape are not allowed
DGR.9 ^[NC]	All the text or labels in the chip must be covered by the marker layer LOGO (26;0)
DGR.10 ^[NC]	Make sure the designs are DRC clean
DGR.11 ^[NC]	Recommended to avoid small jogs ($\leq 0.005\mu m$) of geometry.
DGR.12 ^[NC]	The layout of designs should have the well organized hierarchical structures.
DGR.13 ^[NC]	The layout of auto dummy insertion designs should be put in a separate hierarchy from the main designs, and try to avoid the flattened dummy insertion designs.

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7.1.4 Non-DRC check guideline

1. No DRC for the design rules with the superscript of [NC]
2. No DRC for Notes.

7.1.5 DRC check guideline

1. The rules with the superscript of [R] are recommended rules which require performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow recommended rules which purpose is to ensure better performance for process and device. Customers can waive violations based on their own judgment, and please consult with integration engineers if customers feel the need.

2. The rules with the superscript of [G] are layout guidelines which require performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow layout guidelines which purpose is to ensure better performance for process and device. Customers can waive violations based on their own judgment, and please consult with integration engineers if customers feel the need.

SMIC spice model and PDK is based on SMIC design rule guidelines. And SMIC don't provide spice model and PDK if customers don't follow the layout guidelines.

3. **The design rules in this document are not applicable for seal ring area (marked with MARKS layer). For seal ring constrains and dimension, please refer Seal Ring design guideline section.**

4. Pls follow guidelines for DRC checking as below:

Category	Rules	DRC switch setting by default
Guideline (Rule number with superscript of [G])	Metal E-FUSE	Turn-off
	Varactor	Turn-on
	BIPOLA	Turn-on
	Seal Ring	Turn-on
	ESD	Turn-off
	Latch Up	Turn-on
	Inline OCCD and OCOVL	Turn-on

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7.1.6 Metallization Options

28nm metal options definition scheme was denoted in this section for metal layer and dielectric type, and is limited only to those materials present in the stack.

The scheme uses the following naming: xPyM_zMa_nMb_mIc_pTMc_qSTMc_sMTTc_tALPA

Where:

P = poly layers,

M = total metal layers excluding AL pad/Al RDL,

Ma = 1x metal layers,

Mb = 2x metal layers,

Ic = Cu inter metal layers (included M1),

TMc = Cu 8x top metal layers,

STMc = Cu 10x top metal layers,

MTTc = Cu Ultra thick metal layers,

ALPA = AL pad/AL RDL layers,

x = number of poly layers,

y = number of total metal layers excluding AL pad/Al RDL, (**y** = **m+p+q+s**)

z = number of 1x metal layers (included M1)

n = number of 2x metal layers,

m = number of Cu inter metal layers (included M1, **m=z+n**),

p = number of 8x Cu top metal layers,

q = number of 10x Cu top metal layers,

s = number of Cu ultra thick metal layers.

t = number of AL pad/AL RDL layers

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Table 1 8xTMn/TVn optional table:

		1x +2x +8x metal option																						
Metal option		IP5M_4Ma_4Ic_1TMc_ALPA IP6M_4Ma_1Mb_5Ic_1TMc_ALPA IP7M_4Ma_2Mb_6Ic_1TMc_ALPA IP6M_4Ma_4Ic_2TMc_ALPA IP7M_4Ma_1Mb_5Ic_2TMc_ALPA IP8M_4Ma_2Mb_6Ic_2TMc_ALPA IP6M_5Ma_5Ic_1TMc_ALPA IP7M_5Ma_1Mb_6Ic_2TMc_ALPA IP8M_5Ma_2Mb_7Ic_2TMc_ALPA IP7M_6Ma_6Ic_1TMc_ALPA IP8M_6Ma_1Mb_7Ic_1TMc_ALPA IP9M_6Ma_2Mb_8Ic_1TMc_ALPA IP8M_6Ma_6Ic_2TMc_ALPA IP9M_6Ma_1Mb_7Ic_2TMc_ALPA IP10M_6Ma_2Mb_8Ic_2TMc_ALPA IP8M_7Ma_7Ic_1TMc_ALPA IP9M_7Ma_1Mb_8Ic_1TMc_ALPA IP10M_7Ma_2Mb_9Ic_1TMc_ALPA IP11M_7Ma_2Mb_9Ic_2TMc_ALPA IP9M_8Ma_8Ic_1TMc_ALPA IP10M_8Ma_1Mb_9Ic_1TMc_ALPA IP11M_8Ma_2Mb_10Ic_1TMc_ALPA IP10M_8Ma_3Ic_2TMc_ALPA IP11M_8Ma_1Mb_9Ic_2TMc_ALPA IP12M_8Ma_2Mb_10Ic_2TMc_ALPA																						
Total metal layers(excluding ALPA)		5	6	7	6	7	8	6	7	8	7	8	9	7	8	9	8	9	10	8	9	10	11	12
M1 wiring level in CVD ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um M1 typical thickness: 1000A M1 typical Sheet Resistance: 0.5 ohm/sq		160	M1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		178	V1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Ix (thin) wiring levels in ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um Mn typical thickness: 1000A Mn typical Sheet Resistance: 0.5 ohm/sq		180	M2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		179	V2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		181	M3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		177	V3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		182	M4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		176	V4																					
		183	M5																					
		175	V5																					
		184	M6																					
		174	V6																					
		185	M7																					
		173	V7																					
		186	M8																					
2x (thin) wiring levels in BDI dielectric metal minimum pitch W / S = 0.1um / 0.1um Mn typical thickness: 2250A Mn typical Sheet Resistance: 0.18 ohm/sq		270	W0			X			X		X			X		X		X			X		X	
		280	B1			X			X		X			X		X		X			X		X	
		271	W1	X	X		X		X	X	X	X		X	X	X	X	X	X	X	X	X	X	
		281	B2	X	X		X	X		X	X			X	X	X	X	X	X	X	X	X	X	
8x (thick) wiring levels in TEOS dielectric TMn minimum pitch W / S = 0.40um / 0.40um TMn typical thickness: 9000A TMn typical Sheet Resistance: 0.022 ohm/sq		142	TV1				X	X	X			X	X	X			X	X	X			X	X	
		141	TM1				X	X	X			X	X	X			X	X	X			X	X	
		144	TV2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
		143	TM2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

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Table 2 10xTMn/TVn optional table:

Metal option		1x +2x +10x metal option																																												
		IP5M_4Ma_4Mb_5lc_1STMc_ALPA	IP6M_4Ma_1Mb_5lc_1STMc_ALPA	IP6M_4Ma_2Mb_6lc_1STMc_ALPA	IP7M_4Ma_4lc_2STMc_ALPA	IP7M_4Ma_1Mb_5lc_2STMc_ALPA	IP8M_4Ma_2Mb_6lc_2STMc_ALPA	IP8M_5Ma_5lc_1STMc_ALPA	IP7M_5Ma_1Mb_6lc_1STMc_ALPA	IP8M_5Ma_2Mb_7lc_1STMc_ALPA	IP7M_5Ma_5lc_2STMc_ALPA	IP9M_5Ma_2Mb_7lc_2STMc_ALPA	IP7M_6Ma_1Mb_7lc_1STMc_ALPA	IP8M_6Ma_2Mb_8lc_1STMc_ALPA	IP9M_6Ma_2Mb_8lc_2STMc_ALPA	IP8M_6Ma_1Mb_7lc_2STMc_ALPA	IP9M_6Ma_1Mb_8lc_1STMc_ALPA	IP10M_6Ma_2Mb_8lc_2STMc_ALPA	IP9M_7Ma_1Mb_9lc_1STMc_ALPA	IP10M_7Ma_2Mb_9lc_2STMc_ALPA	IP10M_7Ma_1Mb_8lc_2STMc_ALPA	IP9M_8Ma_8lc_1STMc_ALPA	IP11M_7Ma_2Mb_9lc_1STMc_ALPA	IP10M_8Ma_1Mb_9lc_2STMc_ALPA	IP11M_8Ma_2Mb_10lc_1STMc_ALPA	IP10M_8Ma_8lc_2STMc_ALPA	IP11M_8Ma_1Mb_9lc_2STMc_ALPA	IP12M_8Ma_2Mb_10lc_2STMc_ALPA																		
Total metal layers(excluding ALPA)		5	6	7	6	7	8	6	7	8	7	8	9	7	8	9	8	9	10	8	9	10	9	10	11	9	10	11	10	11	12															
M1 wiring level in CVD ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um M1 typical thickness: 1000Å M1 typical Sheet Resistance: 0.5 ohm/sq	160	M1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X												
	178	V1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X												
1x (thin) wiring levels in ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um Mn typical thickness: 1000Å Mn typical Sheet Resistance: 0.5 ohm/sq	180	M2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X											
	179	V2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X											
	181	M3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X											
	177	V3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X											
	182	M4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X											
	176	V4																																												
	183	M5																																												
	175	V5																																												
	184	M6																																												
	174	V6																																												
	185	M7																																												
	173	V7																																												
	186	M8																																												
2x (thin) wiring levels in BDI dielectric metal minimum pitch W / S = 0.1um / 0.1um Mn typical thickness: 2250Å Mn typical Sheet Resistance: 0.18 ohm/sq	270	W0			X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X					
	280	B1			X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X					
	271	W1	X	X		X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X							
	281	B2	X	X		X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X		X	X	X							
10x (thick) wiring levels in TEOS dielectric STMn minimum pitch: W / S = 0.50um / 0.50um STMn typical thickness: 12.5kÅ STMn typical Sheet Resistance: 0.016 ohm/sq	442	STV1				X	X	X				X	X	X				X	X	X				X	X	X																				
	441	STM1					X	X	X				X	X	X				X	X	X				X	X	X																			
	444	STV2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
	443	STM2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								

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Table 3 8xTMn/TVn + MTT2 optional table:

		1x +2x+ 8x + MTT2 metal option											
		IP5M_4Ma_4lc_1MTTc_ALPA IP6M_5Ma_5lc_1MTTc_ALPA IP7M_6Ma_6lc_1MTTc_ALPA IP8M_7Ma_7lc_1MTTc_ALPA IP9M_8Ma_8lc_1MTTc_ALPA IP6M_4Ma_4lc_1TMC_1MTTc_ALPA IP7M_5Ma_5lc_1TMC_1MTTc_ALPA IP8M_6Ma_6lc_1TMC_1MTTc_ALPA IP9M_7Ma_7lc_1TMC_1MTTc_ALPA IP10M_8Ma_8lc_1TMC_1MTTc_ALPA IP8M_5Ma_1Mb_6lc_1TMC_1MTTc_ALPA											
		5	6	7	8	9	6	7	8	9	10	8	
Metal option	160	M1	X	X	X	X	X	X	X	X	X	X	
	178	V1	X	X	X	X	X	X	X	X	X	X	
Total metal layers(excluding ALPA)	180	M2	X	X	X	X	X	X	X	X	X	X	
	179	V2	X	X	X	X	X	X	X	X	X	X	
	181	M3	X	X	X	X	X	X	X	X	X	X	
	177	V3	X	X	X	X	X	X	X	X	X	X	
	182	M4	X	X	X	X	X	X	X	X	X	X	
	176	V4		X	X	X		X	X	X	X	X	
	183	M5		X	X	X		X	X	X	X	X	
	175	V5			X	X	X		X	X	X	X	
	184	M6			X	X	X		X	X	X	X	
	174	V6				X	X			X	X		
	185	M7					X	X			X	X	
	173	V7						X			X		
	186	M8						X				X	
1x (thin) wiring levels in ultralow-k dielectric metal minimum pitch W / S = 0.05um / 0.05um Mn typical thickness: 1000A Mn typical Sheet Resistance: 0.5 ohm/sq	270	W0											
	280	B1											
	271	W1										X	
	281	B2										X	
2x (thin) wiring levels in BDI dielectric metal minimum pitch W / S = 0.1um / 0.1um Mn typical thickness: 2250A Mn typical Sheet Resistance: 0.18 ohm/sq	142	8X TV1						X	X	X	X	X	
	141	8X TM1						X	X	X	X	X	
	144	8X TV2											
	143	8X TM2											
MTT2 minimum pitch W / S = 1.50um / 1.50um MTT2 typical thickness: 35kA MTT2 typical Sheet Resistance: 5mhm/sq	240	LT	X	X	X	X	X	X	X	X	X	X	
	543	MTT2	X	X	X	X	X	X	X	X	X	X	

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7.1.7 SMIC Drawn layer Mapping Table

Sequence number	Design layer name	GDS layer No	GDS data type	Layer Description
1	AA	10	0	Active Area
2	KV	9	0	Alignment Mark Clear Out
3	DNW	19	0	Deep N well
4	NW	14	0	N-Well for core and IO
5	SDOP	99	0	SRAM Cell Implant
6	DG	29	0	1.8V IO device
7	TG	125	0	2.5V IO device
8	GT	30	0	Poly
9	P2	31	0	Poly trim slot
10	SN	40	0	N+ S/D Implant
11	SP	43	0	P+ S/D Implant
12	SAB	48	0	Salicide Block
13	P4	33	0	HKMG PMOS poly remove
14	CT	50	0	Contact
15	M1	61	0	Metal-1
16	V1	70	0	Via-1
17	M2	62	0	Metal-2
18	V2	71	0	Via-2
19	M3	63	0	Metal-3
20	V3	72	0	Via-3
21	M4	64	0	Metal-4
22	V4	73	0	Via-4
23	M5	65	0	Metal-5
24	V5	74	0	Via-5
25	M6	66	0	Metal-6
26	V6	75	0	Via-6
27	M7	67	0	Metal-7
28	V7	76	0	Via-7 Hole
29	M8	68	0	Metal-8
30	W0	225	0	2x Via-1
31	B1	141	0	2x Metal-1
32	W1	226	0	2x Via-2
33	B2	142	0	2x Metal-2
34	TV1	121	0	8x top via1
35	TM1	120	0	8x top metal1
36	TV2	123	0	8x top via2
37	TM2	122	0	8x top metal2

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Sequence number	Design layer name	GDS layer No	GDS data type	Layer Description		
38	STV1	243	0	10x top via1		
39	STM1	228	0	10x top metal1		
40	STV2	244	0	10x top via2		
41	STM2	229	0	10x top metal2		
42	LT	200	0	8x UTV		
43	PA	80	0	Passivation 1		
44	ALPA	83	0	AL Bonding Pad and RDL		
45	MD	130	0	Passivation 2 opening		
46	MTT2	231	0	Second Ultra Thick Top Metal		
47	ESD1	41	0	ESD Implant		
48	ULVT	159	152	Marker layer for Ultra low Vth device of 0.9V		
49	UHVT	159	151	Marker layer for Ultra high Vth device of 0.9V		
50	LVT	159	12	Marking layer for low-Vt devices		
51	HVT	159	11	Marking layer for high-Vt devices		
52	PSUB	85	0	Marking layer for native device		
53	GBD20	89	158	Marking layer for poly/GT CD size down 2nm (before shrink).		
54	GBU15	89	159	Marking layer for poly/GT CD size up 1.5nm/side (before shrink).		
55	PSRBL	6	239	Marking layer for SiGe PFET Si recess(GS)		
56	PSRDUM	6	1	PSR Dummy Layer		
57	PSRNNDUM	6	11	PSR Dummy Layer (For dummy PSR insertion)		
58	VARMOS	93	0	Block Layer to cover all MOS-type varactor		
59	BIPOLA	159	1	Marking layer for PNP and NPN bipolar		
60	DSTR	138	0	Diode Marker (identifies a diode, for LVS only)		
61	NLDB	12	150	N+ LDD and pocket implant		
62	PLDB	13	150	P+ LDD and pocket implant		
63	RESNW	95	0	Marking layer for NW resistor		
64	RESAA	97	0	Dummy Pattern for AA Resistor		
65	RESP2	96	2	Marking layer for H-R & Metal resistor portion		
66	SNBL	12	138	Marking layer for blocking N+ S/D Implant		
67	SPBL	13	239	Marking layer for blocking P+ S/D Implant		
68	INST	60	0	DRC marking layer for SP127/SP155/DP315/2PSRAM SRAM bitcell,edge cell, strap cell.		
69	RFSRAM	60	9	DRC/LVS marking layer to identify RF10T SRAM cells		
70	UDSRAM	60	3	Marking layer to identify standard voltage read port (SVT) in 2P240 SRAM region.		

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Sequence number	Design layer name	GDS layer No	GDS data type	Layer Description
71	AADUM	10	1	AA Dummy Layer(For dummy AA insertion)
72	AADOP	10	7	AA Dummy pattern layer for OPC engineering
73	GTDUM	30	1	GT Dummy Layer
74	GTDOP	30	7	GT Dummy pattern layer for OPC engineering
75	M1DUM	61	1	Metal1 Dummy Layer
76	M1DOP	61	7	Metal 1 Dummy pattern layer for OPC engineering
77	M2DUM	62	1	Metal2 Dummy Layer
78	M2DOP	62	7	Metal 2 Dummy pattern layer for OPC engineering
79	M3DUM	63	1	Metal3 Dummy Layer
80	M3DOP	63	7	Metal 3 Dummy pattern layer for OPC engineering
81	M4DUM	64	1	Metal4 Dummy Layer
82	M4DOP	64	7	Metal 4 Dummy pattern layer for OPC engineering
83	M5DUM	65	1	Metal5 Dummy Layer
84	M5DOP	65	7	Metal 5 Dummy pattern layer for OPC engineering
85	M6DUM	66	1	Metal6 Dummy Layer
86	M6DOP	66	7	Metal 6 Dummy pattern layer for OPC engineering
87	M7DUM	67	1	Metal7 Dummy Layer
88	M7DOP	67	7	Metal 7 Dummy pattern layer for OPC engineering
89	M8DUM	68	1	Metal8 Dummy Layer
90	M8DOP	68	7	Metal 8 Dummy pattern layer for OPC engineering
91	B1DUM	141	1	2x Metal-1 Dummy Layer
92	B1DOP	141	7	2x Metal-1 Dummy pattern layer for OPC engineering
93	B2DUM	142	1	2x Metal-2 Dummy Layer
94	B2DOP	142	7	2x Metal-2 Dummy pattern layer for OPC engineering
95	TV1DUM	121	1	8x top via1 dummy
96	TM1DUM	120	1	8x top metal1 dummy
97	TV2DUM	123	1	8x top via2 dummy
98	TM2DUM	122	1	8x top metal2 dummy
99	STV1DM	243	1	10x top via1 dummy
99	STM1DM	228	1	10x top metal 1 dummy
100	STV2DM	244	1	10x top via2 dummy
101	STM2DM	229	1	10x top metal2 dummy
102	MTT2DM	231	1	MTT2 Dummy layer
103	ALDUM	83	11	ALPA Dummy layer
104	V1DUM	70	1	via-1 Dummy Layer
105	V2DUM	71	1	via-2 Dummy Layer
106	V3DUM	72	1	via-3 Dummy Layer
107	V4DUM	73	1	via-4 Dummy Layer
108	V5DUM	74	1	Via-5 Dummy Layer

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Sequence number	Design layer name	GDS layer No	GDS data type	Layer Description
109	V6DUM	75	1	via-6 Dummy Layer
110	V7DUM	76	1	via-7 Dummy Layer
111	AADMP	10	8	Manually drawn AA dummy layer with OPC engineering
112	GTDMP	30	8	Manually drawn poly dummy layer with OPC engineering
113	P2DUM	31	1	P2 layer dummy(for dummy P2 insertion)
114	P2DOP	31	7	P2 dummy pattern layer for OPC engineering
115	LVT_N	159	158	Marking layer for N-type low-Vt devices
116	LVT_P	159	168	Marking layer for P-type low-Vt devices
117	ULVT_N	159	159	Marker layer for N-type Ultra low Vth device
118	ULVT_P	159	169	Marker layer for P-type Ultra low Vth device
119	HVT_N	159	156	Marking layer for N-type high-Vth devices
120	HVT_P	159	166	Marking layer for P-type high-Vth devices
121	UHVT_N	159	155	Marker layer for N-type Ultra high Vth device of 0.9V
122	UHVT_P	159	165	Marker layer for P-type Ultra high Vth device of 0.9V
123	MGBL	131	150	Marker layer for blocking metal gate formation

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7.1.8 SMIC CAD layer Mapping Table

Layer name	GDS No	Data Type	Description
STSRAM	60	1	LVS marking layer to identify SP127 SRAM cells
DPSRAM	60	4	LVS marking layer to identify DP315 dualport SRAM cells;
LRSRAM	60	5	LVS marking layer to identify SP155 SRAM cells
6TMK	60	151	Marking layer to identify 6T SRAM transistor in 2P240 and RF10T SRAM.
HPBL	60	150	Marking layer to identify low leakage SRAM.
2PSRAM	60	12	LVS marking layer to identify 2P240 SRAM cells
LDBK	216	150	Marking layer to identify LDMOS function area.
NODMF	180	0	Area not to add AA/GT/Metal dummies
MOMDMY	211	1	DRC/LVS mark layer for MOM
JVARDUM	183	0	Junction Varactor recognition for DRC/LVS
DGOD	29	2	To block over drive poly
DGUD	29	3	To block under drive poly
MARKF	190	0	Fuse area mark for Fuse DRC check
MARKG	189	0	Guard ring mark for DRC check
MARKS	189	151	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage
INDMY	212	0	DRC/LVS mark layer for inductor
DTDMY	191	3	Marker layer for different net AA
DIFRES	97	3	LVS mark layer for AA resistor extraction.
RESP1	96	0	LVS mark layer for H-R/metal gate resistor extraction
RESP3T	96	1	Dummy layer for Poly-1 Resistor with 3 terminal
RFDEV	181	0	DRC/LVS mark layer for RF device
RFMOSD	182	0	DRC/LVS mark layer for RF mos drain terminal
JVARDUM	183	0	DRC/LVS mark layer for junction varactor
VARJUN	94	0	DRC/LVS mark layer for junction varactor
RF3T	183	2	DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM
SUBD	131	1	LVS substrate separation layer
MOSCKT	131	2	LVS dummy layer to distinguish bsim mos and subckt mos
RESCKT	131	3	LVS dummy layer for subckt resistor
PLDMK	131	4	LVS marking layer for device dummy poly
NFDMK	131	5	LVS marking layer for mos multiple fingers
DNWTR	19	2	LVS mark layer for DNW MOS and parasitic diode extraction
M1R	171	0	M1 resistor layer
M2R	172	0	M2 resistor layer

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Layer name	GDS No	Data Type	Description
M3R	173	0	M3 resistor layer
M4R	174	0	M4 resistor layer
M5R	175	0	M5 resistor layer
M6R	176	0	M6 resistor layer
M7R	177	0	M7 resistor layer
M8R	178	0	M8 resistor layer
B1R	194	154	2xmetal 1 resistor layer
B2R	194	155	2xmetal 2 resistor layer
TM1R	201	0	8x top metal1 resistor layer
TM2R	202	0	8x top metal2 resistor layer
STM1R	194	150	10x top metal1 resistor layer
STM2R	194	151	10x top metal2 resistor layer
MTT2R	194	153	MTT2 resistor layer
ALPAR	83	1	ALPA resistor layer
DCTY	139	0	Area with no Extraction for LVS
RFSD	181	3	RF MOS of even finger with S/D permute for LVS
RFDN6T	181	4	6-terminal RF MOS in deep NWELL for LVS, the sixth terminal is psub.
MOMTEM	211	2	LVS mark layer for MOM terminal
LOGO	26	0	LOGO
EXDFM	239	1	DFM erorrwaive
EXLFD	239	2	LFD errors waive
BORDER	127	0	Marking layer for chip edge
DUPMK1	89	156	Marking layer for DUP(pad with device underneath)
ESDIO1	133	0	DRC marking layer for SMIC IO ESD protection devices and circuits identification.
ESDIO2	133	3	DRC marking layer for ESD protection devices and circuits identification.
ESDHV	133	1	DRC marking layer for HV tolerant ESD protection devices using cascaded NMOS.
M1V12	89	16	DRC and LVS marking layer for 1.2V M1
M1V15	89	17	DRC and LVS marking layer for 1.5V M1
M1V18	89	11	DRC and LVS marking layer for 1.8V M1
M1V25	89	12	DRC and LVS marking layer for 2.5V M1
M1V33	89	13	DRC and LVS marking layer for 3.3V M1
M1V50	89	15	DRC and LVS marking layer for 5V M1
M2V12	89	26	DRC and LVS marking layer for 1.2V M2
M2V15	89	27	DRC and LVS marking layer for 1.5V M2

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Layer name	GDS No	Data Type	Description
M2V18	89	21	DRC and LVS marking layer for 1.8V M2
M2V25	89	22	DRC and LVS marking layer for 2.5V M2
M2V33	89	23	DRC and LVS marking layer for 3.3V M2
M2V50	89	25	DRC and LVS marking layer for 5V M2
M3V12	89	36	DRC and LVS marking layer for 1.2V M3
M3V15	89	37	DRC and LVS marking layer for 1.5V M3
M3V18	89	31	DRC and LVS marking layer for 1.8V M3
M3V25	89	32	DRC and LVS marking layer for 2.5V M3
M3V33	89	33	DRC and LVS marking layer for 3.3V M3
M3V50	89	35	DRC and LVS marking layer for 5V M3
M4V12	89	46	DRC and LVS marking layer for 1.2V M4
M4V15	89	47	DRC and LVS marking layer for 1.5V M4
M4V18	89	41	DRC and LVS marking layer for 1.8V M4
M4V25	89	42	DRC and LVS marking layer for 2.5V M4
M4V33	89	43	DRC and LVS marking layer for 3.3V M4
M4V50	89	45	DRC and LVS marking layer for 5V M4
M5V12	89	56	DRC and LVS marking layer for 1.2V M5
M5V15	89	57	DRC and LVS marking layer for 1.5V M5
M5V18	89	51	DRC and LVS marking layer for 1.8V M5
M5V25	89	52	DRC and LVS marking layer for 2.5V M5
M5V33	89	53	DRC and LVS marking layer for 3.3V M5
M5V50	89	55	DRC and LVS marking layer for 5V M5
M6V12	89	66	DRC and LVS marking layer for 1.2V M6
M6V15	89	67	DRC and LVS marking layer for 1.5V M6
M6V18	89	61	DRC and LVS marking layer for 1.8V M6
M6V25	89	62	DRC and LVS marking layer for 2.5V M6
M6V33	89	63	DRC and LVS marking layer for 3.3V M6
M6V50	89	65	DRC and LVS marking layer for 5V M6
M7V12	89	76	DRC and LVS marking layer for 1.2V M7
M7V15	89	77	DRC and LVS marking layer for 1.5V M7
M7V18	89	71	DRC and LVS marking layer for 1.8V M7
M7V25	89	72	DRC and LVS marking layer for 2.5V M7
M7V33	89	73	DRC and LVS marking layer for 3.3V M7
M7V50	89	75	DRC and LVS marking layer for 5V M7
M8V12	89	86	DRC and LVS marking layer for 1.2V M8
M8V15	89	87	DRC and LVS marking layer for 1.5V M8
M8V18	89	81	DRC and LVS marking layer for 1.8V M8
M8V25	89	82	DRC and LVS marking layer for 2.5V M8

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Layer name	GDS No	Data Type	Description
M8V33	89	83	DRC and LVS marking layer for 3.3V M8
M8V50	89	85	DRC and LVS marking layer for 5V M8
B1V18	89	91	DRC and LVS marking layer for 1.8V 2x metal 1
B1V25	89	92	DRC and LVS marking layer for 2.5V 2x metal 1
B1V33	89	93	DRC and LVS marking layer for 3.3V 2x metal 1
B1V50	89	95	DRC and LVS marking layer for 5V 2x metal 1
B1V12	89	96	DRC and LVS marking layer for 1.2V 2x metal 1
B1V15	89	97	DRC and LVS marking layer for 1.5V 2x metal 1
B2V18	89	101	DRC and LVS marking layer for 1.8V 2x metal 2
B2V25	89	102	DRC and LVS marking layer for 2.5V 2x metal 2
B2V33	89	103	DRC and LVS marking layer for 3.3V 2x metal 2
B2V50	89	105	DRC and LVS marking layer for 5V 2x metal 2
B2V12	89	106	DRC and LVS marking layer for 1.2V 2x metal 2
B2V15	89	107	DRC and LVS marking layer for 1.5V 2x metal 2
M1TXT	61	250	Metal-1 Text Layer, label text
M2TXT	62	250	Metal-2 Text Layer, label text
M3TXT	63	250	Metal-3 Text Layer, label text
M4TXT	64	250	Metal-4 Text Layer, label text
M5TXT	65	250	Metal-5 Text Layer, label text
M6TXT	66	250	Metal-6 Text Layer, label text
M7TXT	67	250	Metal-7 Text Layer, label text
M8TXT	68	250	Metal-8 Text Layer, label text
B1TXT	141	250	2xmetal 1 text Layer , label text
B2TXT	142	250	2xmetal 2 text Layer , label text
TM1TXT	120	3	8x top metal 1 Text Layer, label text
TM2TXT	122	3	8x top metal 2 Text Layer, label text
STM1TXT	228	3	10x top metal 1 Text Layer, label text
STM2TXT	229	3	10x top metal 2 Text Layer, label text
MTT1TXT	230	3	MTT1 Text Layer, label text
MTT2TXT	231	3	MTT2 Text Layer, label text
ALPATXT	83	2	ALPA Text Layer, label text
SUBTXT	161	0	Substrate Pin Text Layer
WELTXT	162	0	Wells Pin Text Layer
DIFTXT	163	0	Diffusion Pin Text Layer
POLYTXT	164	0	Poly Pin Text Layer
TTXT	87	0	Text for Top Structure
BTXT	88	0	Text for Block
CTXT	89	0	Text for Cell
0M	1	0	Dummy layer for SMIC internal design switch layer

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Layer name	GDS No	Data Type	Description
DUMBA	91	0	Block Layer for Dummy operation on AA
DUMBP	92	0	Block Layer for Dummy operation on GT
M1DUB	151	1	Metal-1 Dummy Block layer for M1 dummy fill
M2DUB	152	1	Metal-2 Dummy Block layer for M2 dummy fill
M3DUB	153	1	Metal-3 Dummy Block layer for M3 dummy fill
M4DUB	154	1	Metal-4 Dummy Block layer for M4 dummy fill
M5DUB	155	1	Metal-5 Dummy Block layer for M5 dummy fill
M6DUB	156	1	Metal-6 Dummy Block layer for M6 dummy fill
M7DUB	157	1	Metal-7 Dummy Block layer for M7 dummy fill
M8DUB	158	1	Metal-8 Dummy Block layer for M8 dummy fill
B1DUB	141	6	2x Metal-1 Dummy Block layer for 2x Metal-1 dummy fill
B2DUB	142	6	2x Metal-2 Dummy Block layer for 2x Metal-2 dummy fill
TM1DUB	193	1	8x top Metal 1 Dummy Block layer for TM1 dummy fill
TM2DUB	194	1	8x top Metal 2 Dummy Block layer for TM2 dummy fill
STM1DB	194	5	10x top Metal 1 Dummy Block layer for TM1 dummy fill
STM2DB	194	4	10x top Metal 2 Dummy Block layer for TM2 dummy fill
MTT2DB	194	2	MTT2 Dummy block layer for MTT2 dummy fill
ALDUB	83	6	ALPA Dummy block layer for ALPA dummy fill
DUMBMB	90	0	Block Layer for all Metal layer dummy fill
V1DUB	70	6	Via-1 Dummy Blockage.
V2DUB	71	6	Via-2 Dummy Blockage.
V3DUB	72	6	Via-3 Dummy Blockage.
V4DUB	73	6	Via-4 Dummy Blockage.
V5DUB	74	6	Via-5 Dummy Blockage.
V6DUB	75	6	Via-6 Dummy Blockage.
V7DUB	76	6	Via-7 Dummy Blockage.
V1RB	70	8	Via-1 blockage layer to skip redundant via insertion
V2RB	71	8	Via-2 blockage layer to skip redundant via insertion
V3RB	72	8	Via-3 blockage layer to skip redundant via insertion
V4RB	73	8	Via-4 blockage layer to skip redundant via insertion
V5RB	74	8	Via-5 blockage layer to skip redundant via insertion
V6RB	75	8	Via-6 blockage layer to skip redundant via insertion
V7RB	76	8	Via-7 blockage layer to skip redundant via insertion
W0RB	225	8	2xVia 1 blockage layer to skip redundant via insertion
W1RB	226	8	2xVia 2 blockage layer to skip redundant via insertion
TV1RB	121	8	8x top via1 blockage layer to skip redundant via insertion
TV2RB	123	8	8x top via1 blockage layer to skip redundant via insertion
STV1RB	243	8	10x top via1 blockage layer to skip redundant via insertion

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Layer name	GDS No	Data Type	Description
STV2RB	244	8	10x top via1 blockage layer to skip redundant via insertion
V1RM	70	10	V1 mark layer to identify redundant via
V2RM	71	10	V2 mark layer to identify redundant via
V3RM	72	10	V3 mark layer to identify redundant via
V4RM	73	10	V4 mark layer to identify redundant via
V5RM	74	10	V5 mark layer to identify redundant via
V6RM	75	10	V6 mark layer to identify redundant via
V7RM	76	10	V7 mark layer to identify redundant via
W0RM	225	10	2xVia 1 mark layer to identify redundant via
W1RM	226	10	2xVia 2 mark layer to identify redundant via
TV1RM	121	10	8x top via1 mark layer to identify redundant via
TV2RM	123	10	8x top via1 mark layer to identify redundant via
STV1RM	243	10	10x top via1 mark layer to identify redundant via
STV2RM	244	10	10x top via1 mark layer to identify redundant via
VSIA	63	63	VSIA tagging layer(Text Only)
DMPNP	134	0	LVS mark layer for BJT
PWMK1	89	165	Marking layer for EDA modeling
MOMP1	211	3	MOM capacitor mesh terminal one
MOMP2	211	4	MOM capacitor mesh terminal one
MOMMES	211	5	MOM capacitor mesh LVS marking layer
TGV	125	1	Marking layer for 2.5V under drive 1.8V IO device
OVERDR	125	3	Marking layer for 2.5V over drive 3.3V IO device
DGV	29	1	Marking layer for 1.8V under drive to 1.2V IO device
RFMK1	181	6	Marking layer for RF device
DCTY	139	0	Marking layer for non-LVS check
FUSEMK1	81	152	Marking layer for fuse bitcell
EFUSE	81	2	Marking layer for metal fuse element and related dummy region.
MTFUSE	81	3	Marking layer for metal fuse function area
FUSEAD	81	4	Marking layer for fuse anode side
P2DUB	31	6	P2 dummy blockage(for dummy P2 insertion) and exclude dummy insertion
RFMOM	211	6	LVS mark layer for RF MOM
INDR	212	1	LVS mark layer for inductor radius calculation
ESDCLP	41	2	Marking layer for ESD RC-triggered power clamp structures connected to a power supply pad
ESDPOB	41	8	Marking layer for Poly-bound ESD diode
CLPDMY	87	2	Marking layer for STI ESD diode
LBESD	41	7	Marking layer used to identify input/output pads in ESD/latch up DRC decks
LDNMK1	131	170	Marking layer of metal low density area
OCCD	91	4	Marking layer of chip CD

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Layer name	GDS No	Data Type	Description
OCOVL	91	5	Marking layer of chip OVL
OCCDFH	91	6	Marking layer of horizontal direction FEOL OCCD cell
OCCDFV	91	7	Marking layer of vertical direction FEOL OCCD cell
OCCDFDB	91	8	FEOL OCCD cell block layer
OCCDBDB	91	9	BEOL OCCD cell block layer
OCCDB	91	10	Marking layer of BEOL OCCD cell
INDTEM	212	3	Marking layer of inductor inter via
CPMK1	131	171	Marking layer for critical path identification
ANMK1	131	172	Marking layer for analog medium level mismatching requirement
ANMK2	131	173	Marking layer for analog high level mismatching requirement
PDMK1	131	174	Marking layer for PMOS pair devices in analog circuit or current mirror design

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7.1.9 SMIC Mask layer Mapping Table

28nm HKMG Top tier is: LCMO28-V00

Mas k ID	Proces s Name	Dig. Area Ton e	Drawn	Description	Layers in Logic Operation Formula
120	AA	D	Drawn	Active Area	AA,AADOP,AADMP,AADUM
901	KV	C	Drawn	Alignment Mark Clear Out	KV
292	DNW	C	Drawn	Deep N well	DNW
192	NW	C	Drawn	N-Well for core and IO	NW
191	PW	C	Generated	P-Well for core and IO	NW,PSUB,INST
492	NWH	C	Generated	1.8V I/O device PMOS Vth adjust Implant	NW,DG,TG,RESAA
491	PWH	C	Generated	1.8V I/O device NMOS Vth adjust Implant	NW,DG,TG,RESAA
296	MVN	C	Generated	Core SVT, HVT, UHVT and SARM NMOS VT implant	NW,PSUB,LVT_N,ULVT_N,DG,TG
295	MVP	C	Generated	Core ULVT, LVT , SVT, HVT,UHVT and SARM PMOS VT implant	NW,DG,TG
196	TN	C	Generated	Core ULVT, LVT NMOS VT implant	NW,PSUB,ULVT_N,LVT_N,INST,RESAA,RESNW,RESP2,VAR MOS,BIPOLA,DSTR
146	SDOP	C	Drawn	SRAM Cell Implant	SDOP
131	DG	D	Generated	Dual GATE	DG,TG
130	GT	D	Generated	Poly	GT,GTDMP,UHVT_N,UHVT_P,GBD20,GBU15,DG,TG,PSUB, GTDUM,GTDOP
132	P2	C	Drawn	Poly trim slot	P2,P2DUM,P2DOP
201	PSR	C	Generated	eSiGe PFET Si recess	SP,NW,DG,TG,RESAA,RESNW,BIPOLA,DSTR,RESP2,VARMOS,PSRBL
200	NSR	D	Generated	non PFET SIN recess	SP,NW,DG,TG,RESAA,RESNW,BIPOLA,DSTR,RESP2,VARMOS,PSRBL
193	NC	C	Generated	LL SRAM NMOS LDD Implant	SN,NW,INST,UDSRAM,HPBL,NLDB
194	PC	C	Generated	LL SRAM PMOS LDD Implant	SP,NW,INST,UDSRAM,HPBL,PLDB
314	DDN	C	Generated	GL SRAM NMOS LDD Implant	SN,NW,INST,UDSRAM,HPBL,NLDB
315	DDP	C	Generated	GL SRAM PMOS LDD Implant	SP,NW,INST,UDSRAM,HPBL,PLDB
596	LVN	C	Generated	0.9V uLVT NMOS LDD IMP	ULVT_N,PSUB,DG,TG,SN,NW,INST,RESAA,RESNW,RESP2,

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Mask ID	Process Name	Dig. Area Tone	Drawn	Description	Layers in Logic Operation Formula
					VARMOS,BIPOLA,NLDB
595	LVP	C	Generated	0.9V uLVT PMOS LDD IMP	ULVT_P,SP,NW,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA,PLDB
312	UNLL	C	Generated	0.9V uHVT NMOS LDD IMP	SN,NW,UHVT_N,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA, NLDB
317	UPLL	C	Generated	0.9V uHVT PMOS LDD IMP	SP,NW,UHVT_P,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA, PLDB
116	NLL	C	Generated	NMOS LDD Implant for 0.9V standard Vt device and LVT device	SN,NW,DG,TG,ULVT_N,HVT_N,UHVT_N,PSUB,INST,RESAA,RESNW,RESP2,VARMOS, NLDB,UDSRAM
113	PLL	C	Generated	PMOS LDD Implant for 0.9V standard Vt device	SP,NW,DG,TG,ULVT_P,HVT_P,UHVT_P,INST,RESAA,RESNW,RESP2,VARMOS,PLDB,UDSRAM
195	TP	C	Generated	0.9V LVT PMOS LDD IMP	SP,NW,LVT_P,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA,PLDB
396	VTNH	C	Generated	0.9V HVT NMOS LDD IMP	SN,NW,HVT_N,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA,NLDB
395	VTPH	C	Generated	0.9V HVT PMOS LDD IMP	SP,NW,HVT_P,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA,PLDB
114	NLH	C	Generated	NMOS LDD Implant for 1.8v device	SN,NW,DG,TG,PSUB,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA,NLDB
115	PLH	C	Generated	PMOS LDD Implant for 1.8v device	SP,NW,DG,TG,PSUB,INST,RESAA,RESNW,RESP2,VARMOS,BIPOLA,PLDB
198	SN	C	Generated	N+ S/D Implant	SN,RESP2,SPBL
197	SP	C	Generated	P+ S/D Implant	SP,RESP2,SPBL
155	SAB	D	Drawn	Salicide Block	SAB
134	P4	C	Generated	HKMG PMOS WF poly remove	P4,RESP2,SAB
420	MGR	C	Generated	NMOS gate poly remove marking layer	RESP2,SAB
156	CT	C	Drawn	Contact	CT
160	M1	C	Generated	Metal-1	M1,M1DUM,M1DOP
178	V1	C	Generated	Via-1	V1,V1DUM

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Mask ID	Process Name	Dig. Area Tone	Drawn	Description	Layers in Logic Operation Formula
180	M2	C	Generated	Metal-2	M2,M2DUM,M2DOP
179	V2	C	Generated	Via-2	V2,V2DUM
181	M3	C	Generated	Metal-3	M3,M3DUM,M3DOP
177	V3	C	Generated	Via-3	V3,V3DUM
182	M4	C	Generated	Metal-4	M4,M4DUM,M4DOP
176	V4	C	Generated	Via-4	V4,V4DUM
183	M5	C	Generated	Metal-5	M5,M5DUM,M5DOP
175	V5	C	Generated	Via-5	V5,V5DUM
184	M6	C	Generated	Metal-6	M6,M6DUM,M6DOP
174	V6	C	Generated	Via-6	V6,V6DUM
185	M7	C	Generated	Metal-7	M7,M7DUM,M7DOP
173	V7	C	Generated	Via-7 Hole	V7,V7DUM
186	M8	C	Generated	Metal-8	M8,M8DUM,M8DOP
270	W0	C	Generated	2xVia-1	W0
280	B1	C	Generated	2xMetal-1	B1, B1DUM,B1DOP
271	W1	C	Generated	2xVia-2	W1
281	B2	C	Generated	2xMetal-2	B2, B2DUM,B2DOP
142	TV1	C	Drawn	8x Top Via1	TV1
141	TM1	C	Generated	8x Top Metal	TM1,TM1DUM
144	TV2	C	Drawn	8x Top Via2	TV2
143	TM2	C	Generated	8x Top Metal2	TM2,TM2DUM
442	STV1	C	Drawn	10x Top Via1	STV1
441	STM1	C	Generated	10x Top Metal	STM1,STM1DM
444	STV2	C	Drawn	10x Top Top Via2	STV2
443	STM2	C	Generated	10x Top Top Metal2	STM1,STM2DM
107	PA	C	Generated	Passivation 1	PA
108	ALPA	D	Generated	AL Bonding Pad and RDL	ALPA,ALDUM
163	MD	C	Drawn	Passivation 2 opening	MD
543	MTT2	C	Generated	Second Ultra Thick Top Metal	MTT2,MTT2DM
240	LT	C	Drawn	8x UTV	LT
110	ESD1	C	Drawn	ESD Implant	ESD1

Note: Please refer DCC document **PM-DATA-02-2001** layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

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7.1.10 Device Layout Truth Table

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Drawing layer GDS No							
			AA	DNW	NW		
			10	19	14		
			0	0	159	ULVT_N	
			0	0	159	ULVT_P	
			0	0	159	LVT_N	
			0	0	159	LVT_P	
			0	0	159	HVT_N	
			0	0	159	HVT_P	
			0	0	159	UHVT_N	
			0	0	165	UHVT_P	
			0	0	0	SDOP	
			0	0	0	DG	
			0	0	0	DGUD	
			0	0	0	DGV	
			0	0	0	TG	
			0	0	0	OVERDR	
			0	0	0	TGV	
			0	0	0	GT	
			0	0	0	P4	
			0	0	0	SP	
			0	0	0	SN	
			0	0	0	PSUB	
			0	0	0	SAB	
			0	0	0	INST	
			0	0	0	STSRAM	
			0	0	0	LRSRAM	
			0	0	0	DPSRAM	
			0	0	0	2PSRAM	
			0	0	0	UDSRAM	
			0	0	0	6TMK	
			0	0	0	HPBL	
			0	0	0	RFSP2	
			0	0	0	RESP1	
			0	0	0	RESNW	
			0	0	0	RESAA	
			0	0	0	DIFRES	
			0	0	0	VARMOS	
			0	0	0	FUSEMK1	
			0	0	0	EFUSE	
			0	0	0	MTFUSE	
			0	0	0	FUSEAD	
			0	0	0	MOMDMY	
			0	0	0	BIPOLA	
			0	0	0	INDMY	

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2008-06-27



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Drawing layer GDS No		
Drawing layer GDS No		
Drawing layer GDS data type		
	NPN_IO (NPN25)	NPN25A10 0_CKT NPN25A25 _CKT NPN25A4_ CKT NPN25A2P 56_CKT
	PNP (PNP09)	PNP09A10 0_CKT PNP09A25 _CKT PNP09A4_ CKT PNP09A2P 56_CKT
	PNP_IO (PNP18)	PNP18A10 0_CKT PNP18A25 _CKT PNP18A4_ CKT PNP18A2P 56_CKT

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Drawing layer GDS No				AA	10	10	19	DNW
Drawing layer GDS No				NW	14	0	14	ULVT_N
Drawing layer GDS data type				ULVT_P	159	159	159	LVT_N
	PLD_MO_S_25	PLD25_CKT	1	1	0	159	159	159
	Capacitor	MOM Cap	MOM_CKT MOM_MS_CKT (2T/3T/4T/5T)	*	*	*	*	ULVT_N
Efuse	Metal fuse			0	*	*	0	0
Inductor	Inductor			0	0	0	0	0

Notes:

1. For the ESD device, please refer to the ESD design guidelines.
 2. The MOS device covered by ESDIO1 or ESDIO2 can have SAB layer as an option.
 3. The “1” in device layout truth table is must drawn layer for device.
 4. The “*” in device layout truth table is optional layer for device.
 5. The “0” in device layout truth table is non-exist layer for device.

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7.1.11 Device table for dummy insertion

Designers can refer to below device table for dummy pattern insertion and need add dummy block layers to avoid dummy patterns insertion.

Dummy patterns device category	Marker Layer	GDS No.	AA Dummy	Poly Dummy	Inter Metal Dummy	Inter Via Dummy	Top Metal dummy	ALPA Dummy	Remark
LDMOS	LDBK	216; 150	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement.
SRAM	INST	60; 0	N	N	N	Y	Y	Y	M4 ~ M8, V3 ~ V7 dummy should be "Y" for INST.
	RFSRAM	60; 9	N	N	N	Y	Y	Y	M4 ~ M8, V3 ~ V7 dummy should be "Y" for RFSRAM.
AA Resistor	RESAA	97; 0	Y	N	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
NW Resistor	RESNW	95; 0	N	N	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
HR/MG resistor	RESP2	96; 2	N	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
Diode	DSTR	138; 0	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
BJT	BIPOLA	159;1	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
MOS Varactor	VARMOS	93; 0	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
MOM	MOMDMY	211;1	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
Inductor	INDMY	212; 0	Y	Y	Y	N	Y	N	Designers can draw dummy block layer based on their requirement
e-fuse	MTFUSE	81;3	Y	Y	Y	Y	Y	Y	M1 ~ M4, V1 ~ V4 dummy should be "N" for MTFUSE.
Seal Ring	MARKS	189;151	N	N	N	N	N	N	
Guard Ring	MARKG	189; 0	N	N	N	N	N	N	

Y: do dummy filling by script automatically.

N: block dummy filling by marker layer of device, and will be defined in the dummy insertion rules to avoid dummy filling.

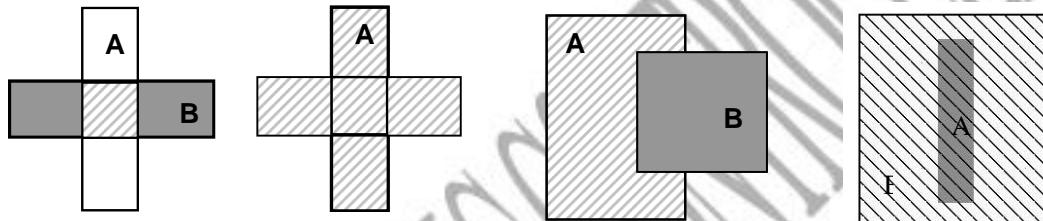
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7.1.12 Design Rules Nomenclatures and Abbreviations

(A) Logic Function Definition

Logic Function	Definition
A and B	Define the intersection area of A and B.
A or B	Define the union area of A and B.
A not B	Define the area of A excluding the common area of A and B.
B cover A	Define the B area where there is A inside B.



A and B

A or B

A not B

B cover A



Logic Function Definition Area

(B) Nomenclatures and Abbreviations

Name	Definitions
PW	Any chip area not (NW or PSUB).
Poly	GT with GDS No (30;0)
GATE	GATE = AA AND poly
Channel Length	The dimension (from poly edge to poly edge) over AA.
Channel Width	The dimension (from AA edge to AA edge) over poly.
MOS AA	MOS AA refers to an AA that is part of a transistor active area. When a poly pattern is on top of an AA, the AA is treated as MOS AA. If there is no poly pattern on top of an AA, the AA is not a MOS AA. Dummy AA is not a MOS AA.
N+AA	((AA and SN) NOT NW)
P+AA	((AA and SP) AND NW)
N+ pick-up AA	((AA and SN) AND NW)
P+ pick-up AA	((AA and SP) NOT NW)
STI	Not (AA or AA dummy)

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Share contact	Connects AA and poly, and the length is larger than the width, which is in INST/RFSRAM region.			
Different or same net	Electrically based connectivity using all conducting layers (unless otherwise noted), including diffusion, poly, and all back-end-of-line (BEOL) metal and via layers in the stack (M1 through last metal). It also includes connectivity through the substrate, through n-wells and p-wells and between n-wells through the deep n-well (for triple-well designs).			
Source/Drain	((AA INTERACT GATE) NOT (((poly OR GTDUM) OR GTDOP) OR GTDMP)) NOT Pick-up			
POLY_DMY	(GTDUM OR GTDOP) OR GTDMP)			
AA_DMY	(AADUM OR AADOP) OR AADMP)			
H-R resistor	High resistance resistor			

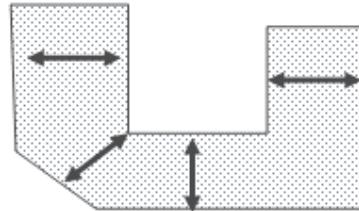
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7.1.13 Definition of terminology used in these design rules

1. Width

- The distance of interior-facing sides of one layer edges.



2. Length

- Distance from one inside edge to a parallel inside edge within a same rectangular shape along the longer dimension of the shape.



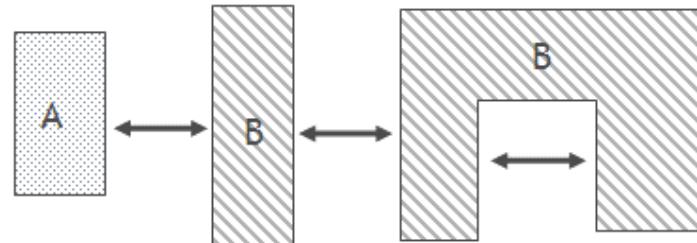
3. Line / Line-end

- (Poly or POLY_DMY) line: (Poly or POLY_DMY) edges with length > 0.1 um;
- (Poly or POLY_DMY) line-end: (Poly or POLY_DMY) edges with length ≤ 0.1 um



4. Space

- The distance of exterior-facing sides of one or two layer edges.

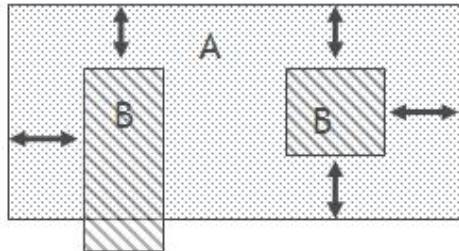


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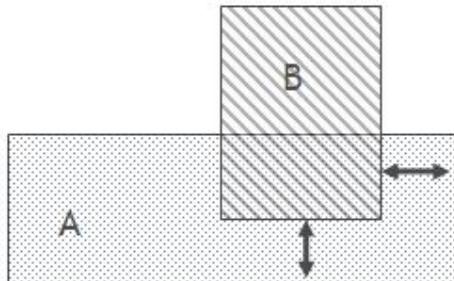
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5. Enclosure

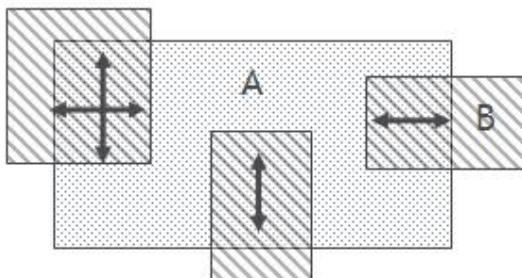
- The distance between the interior-facing sides of layer A edges and the exterior-facing sides of layer B edges.

**6. Extension**

- The distance between the interior-facing sides of layer A edges and the exterior-facing sides of layer B edges.

**7. Overlap**

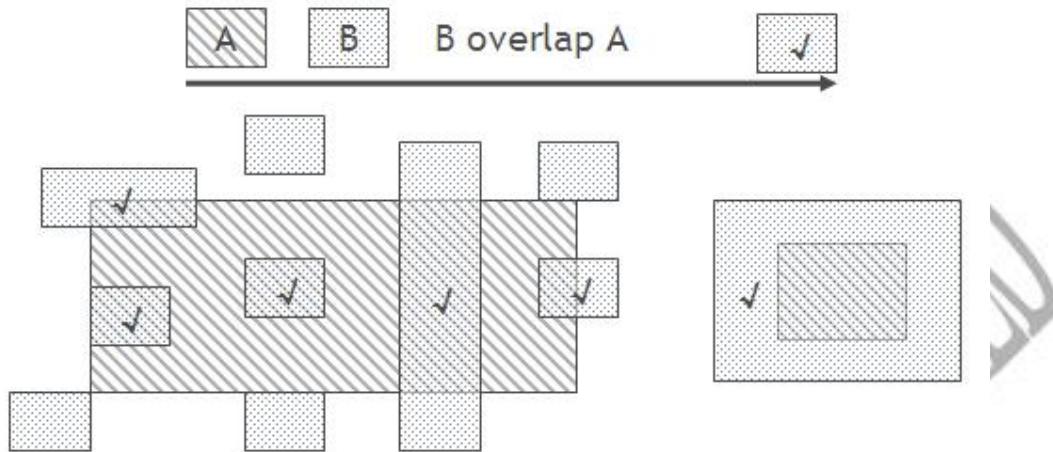
- For the overlap-required rule: The distance between the interior-facing sides of layer A edges and the interior-facing sides of layer B edges



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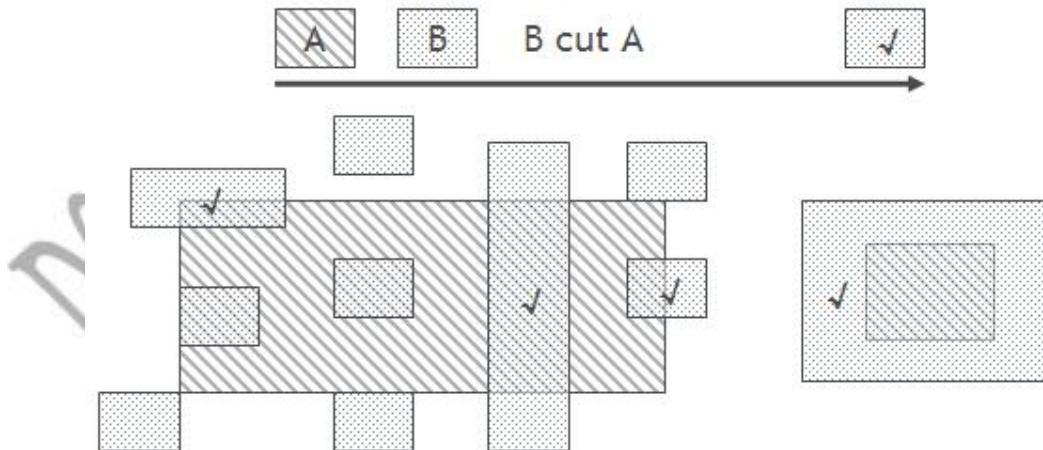
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- For the non-overlap-required rule: Two layers share part (or all) of area.



8. Cut

- A cut B: A share part (not all) of area with B;
- B cut A: B share part (not all) of area with A.

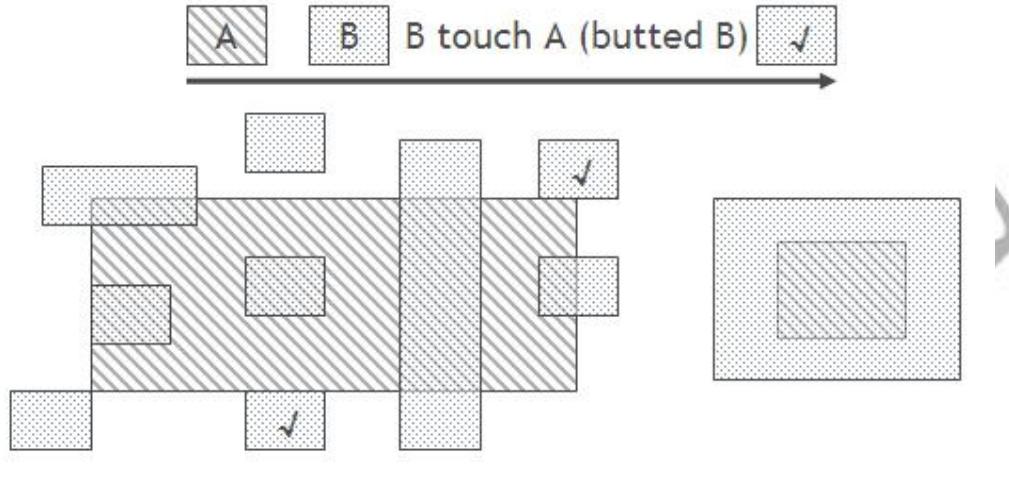


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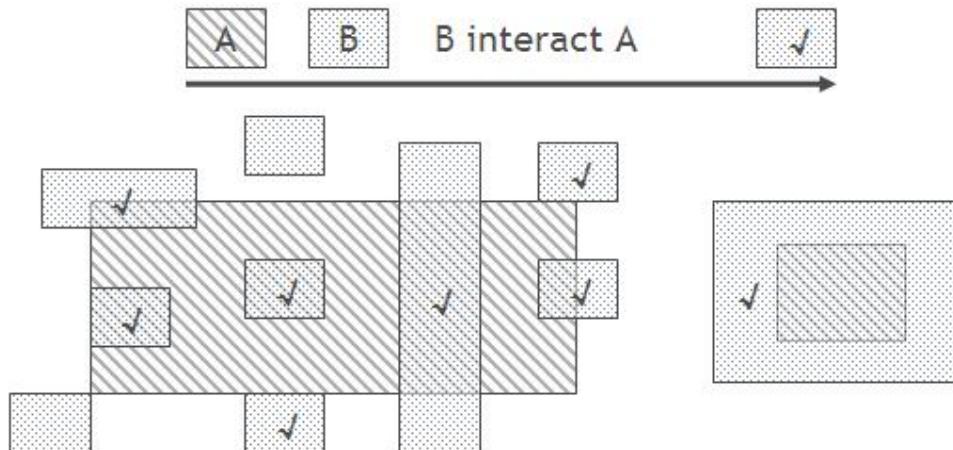
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9. Butted

- Butted A: A share at least one edge (or edge segment) with B from outside;
- Butted B: B share at least one edge (or edge segment) with A from outside;

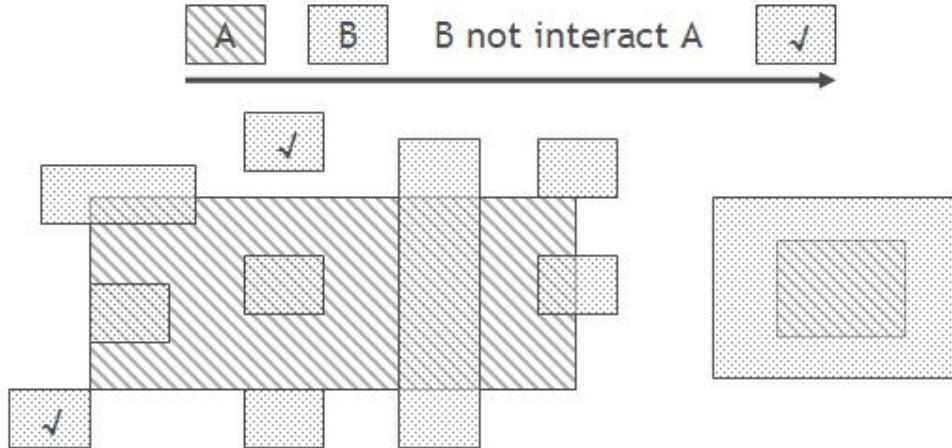
**10. Interact**

- A interact B: A touch or overlap B;
- B interact A: B touch or overlap A.

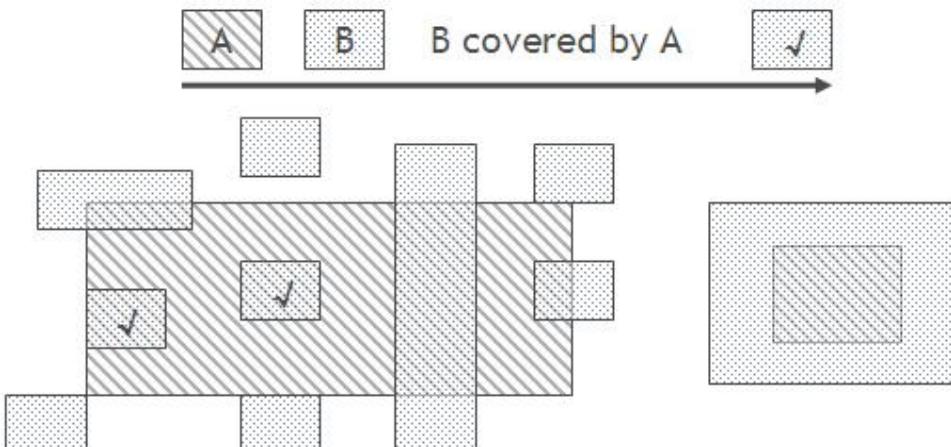


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11. Not Interact**12. Cover**

- A covered by B: A share all area with B;
- B covered by A: B share all area with A;

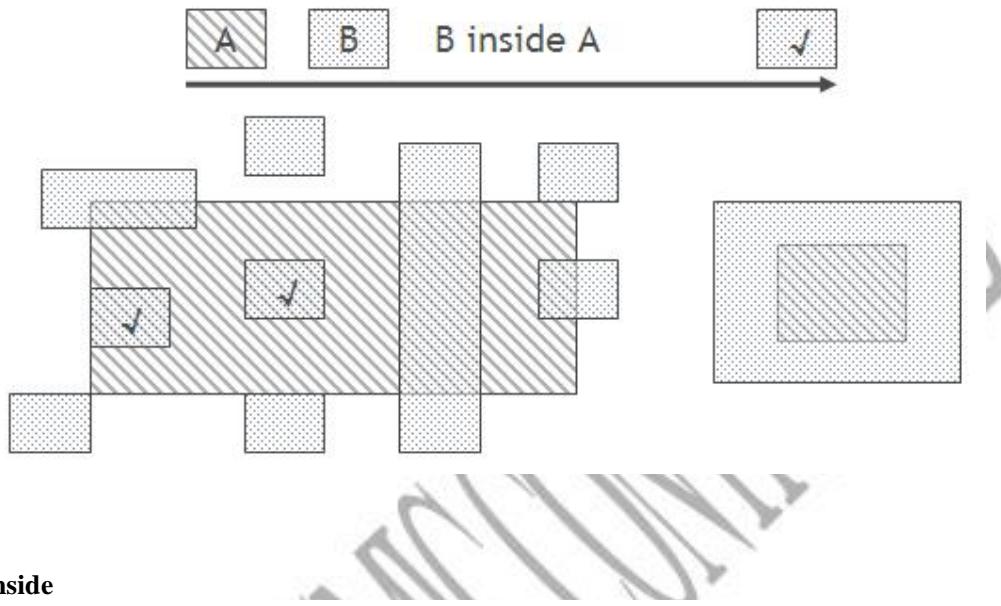
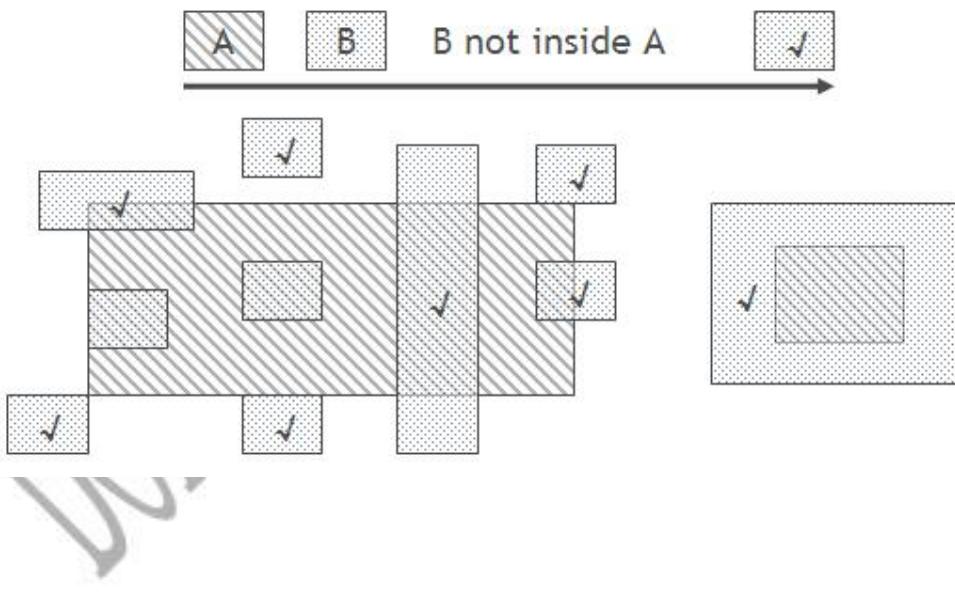


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13. Inside

- A inside B (A covered by B): A share all area with B;
- B inside A (B covered by A): B share all area with A.

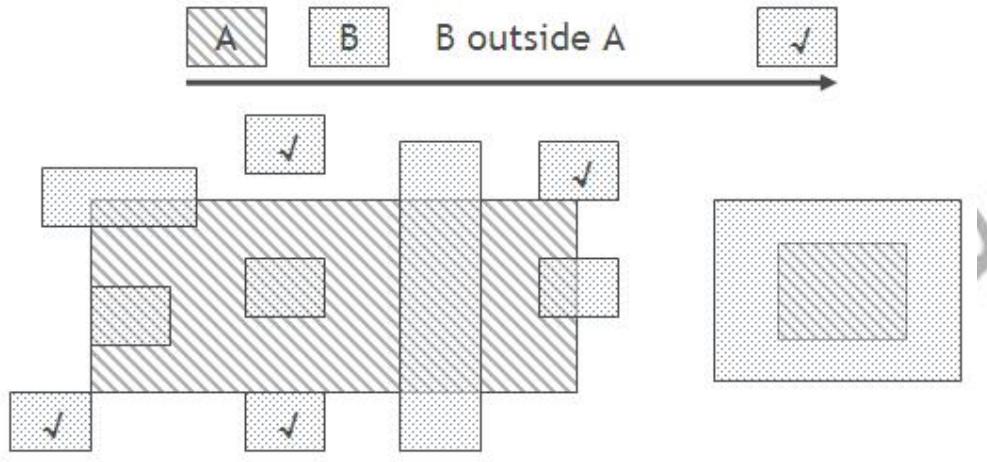
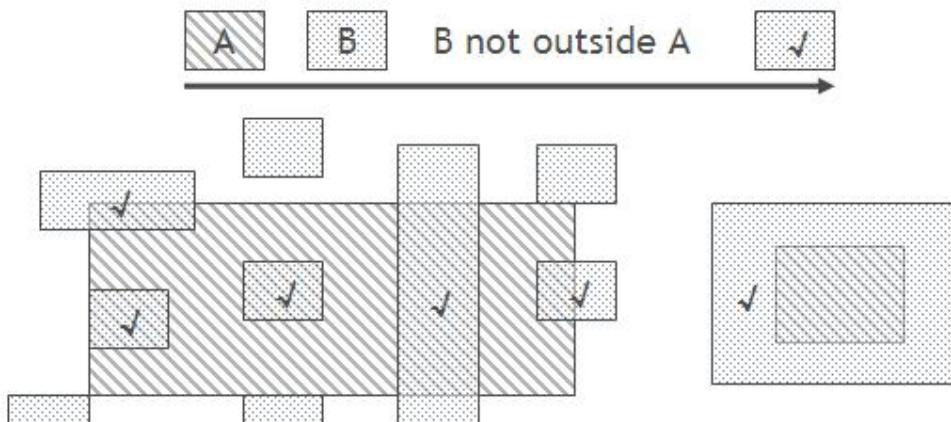
**14. Not Inside**

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15. Outside

- A outside B: A doesn't share any area with B;
- B outside A: B doesn't share any area with A.

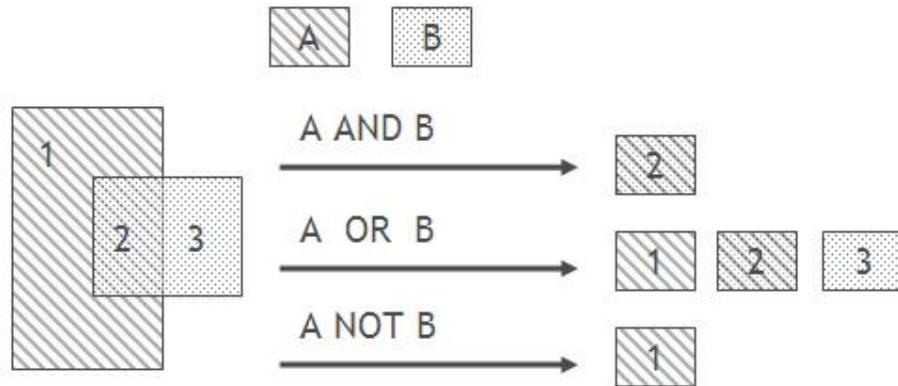
**16. Not Outside**

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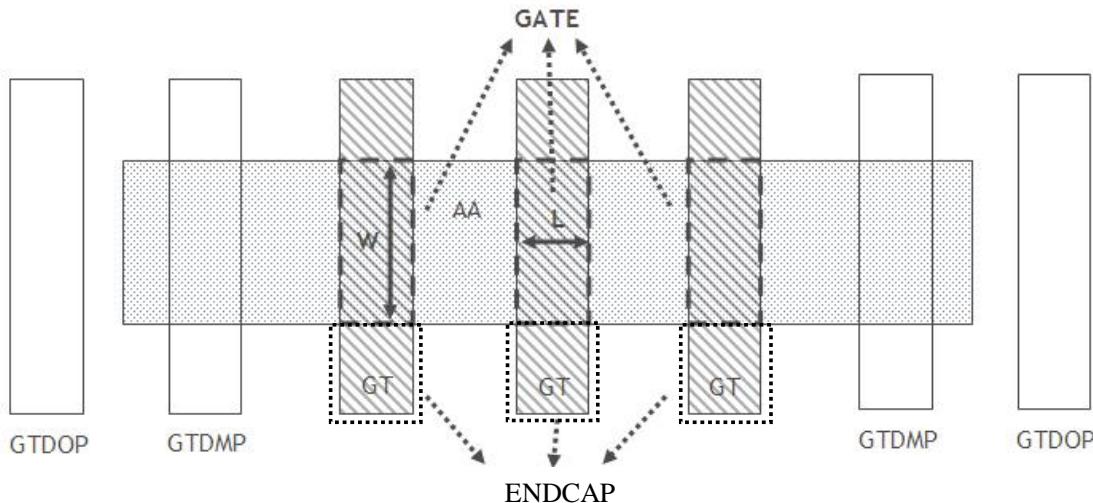
17. AND / OR / NOT

- A AND B: Output the shared area of A and B;
- A OR B: A and B merge as one layer;
- A NOT B: A exclude the shared area of A and B.



18. GATE

- GATE = AA AND poly;
- Channel Length (L in figure): The distance between interior-facing sides of poly edge segments inside AA;
- Channel Width (W in figure): The distance between interior-facing sides of AA edge segments inside poly;
- ENDCAP: poly extension outside GATE in the channel width direction.

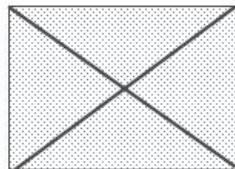


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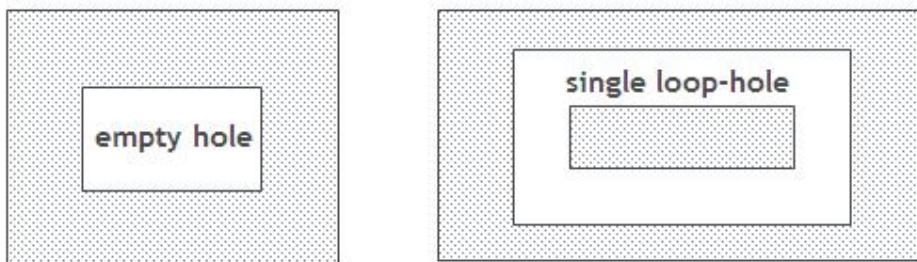
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19. Area

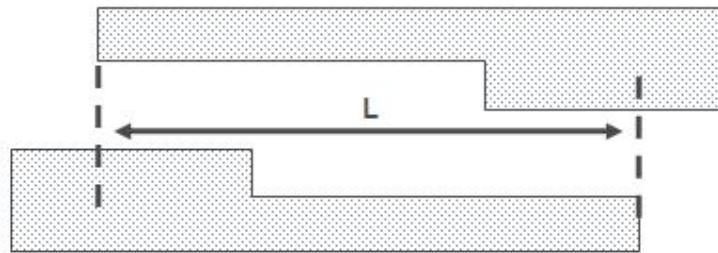
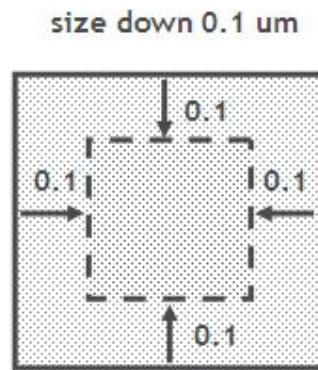
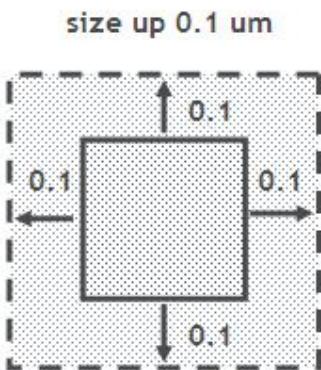
- The area of the polygon.

**20. Enclosed Area**

- The area of empty hole or single loop-hole.

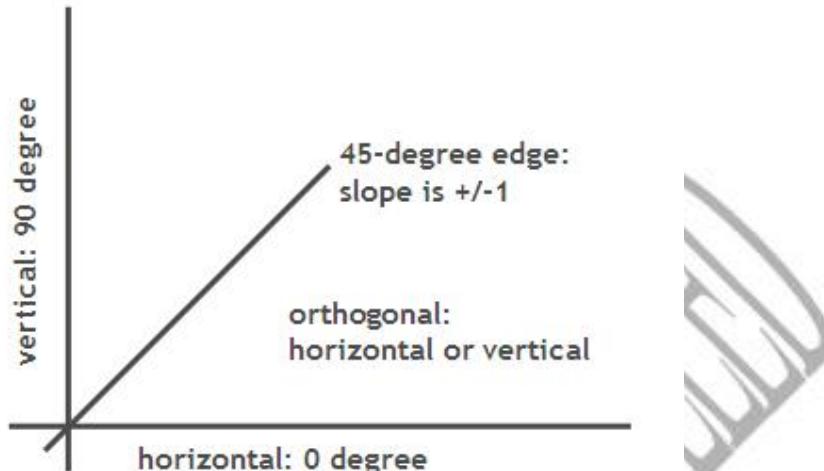
**21. Parallel Run Length**

- Projection length between two polygons.

**22. Size Up / Size Down**

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23. Horizontal / Vertical / 45-degree / Orthogonal**24. Rectangle / Square**

- Rectangle: Orthogonal polygon with 4 vertexes;
- Square: Rectangle with aspect ratio equal to 1.

rectangle: all edges are orthogonal, vertex = 4

rectangle with aspect ratio > 1



rectangle with aspect ratio = 1

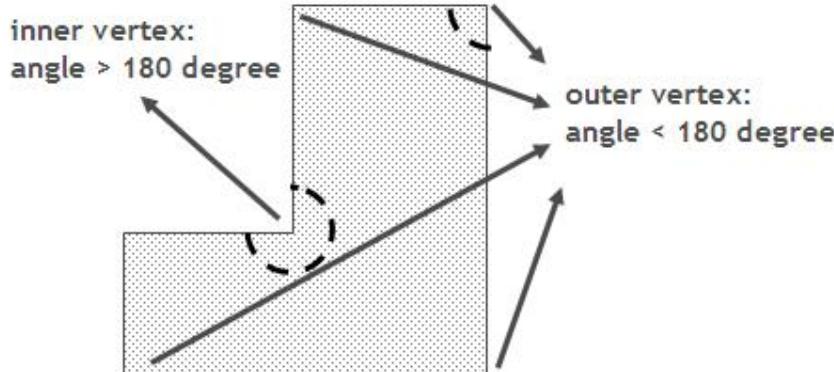
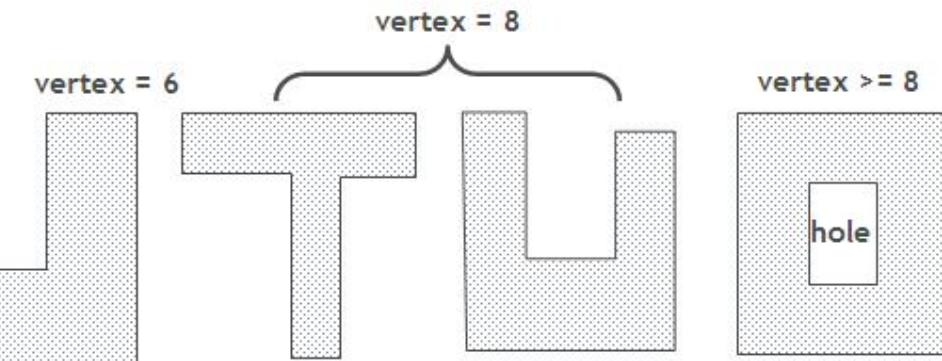


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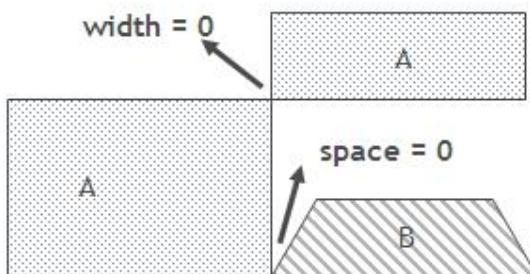
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25. Vertex / Inner Vertex / Outer Vertex

- Inner Vertex (Concave Corner): angle > 180 degree measured inside polygon;
- Outer Vertex (Convex Corner): angle < 180 degree measured inside polygon.

**26. Single L/T/U-shape / O-shape****27. Single-Point-Interaction**

- One or two layers share one vertex from outside.

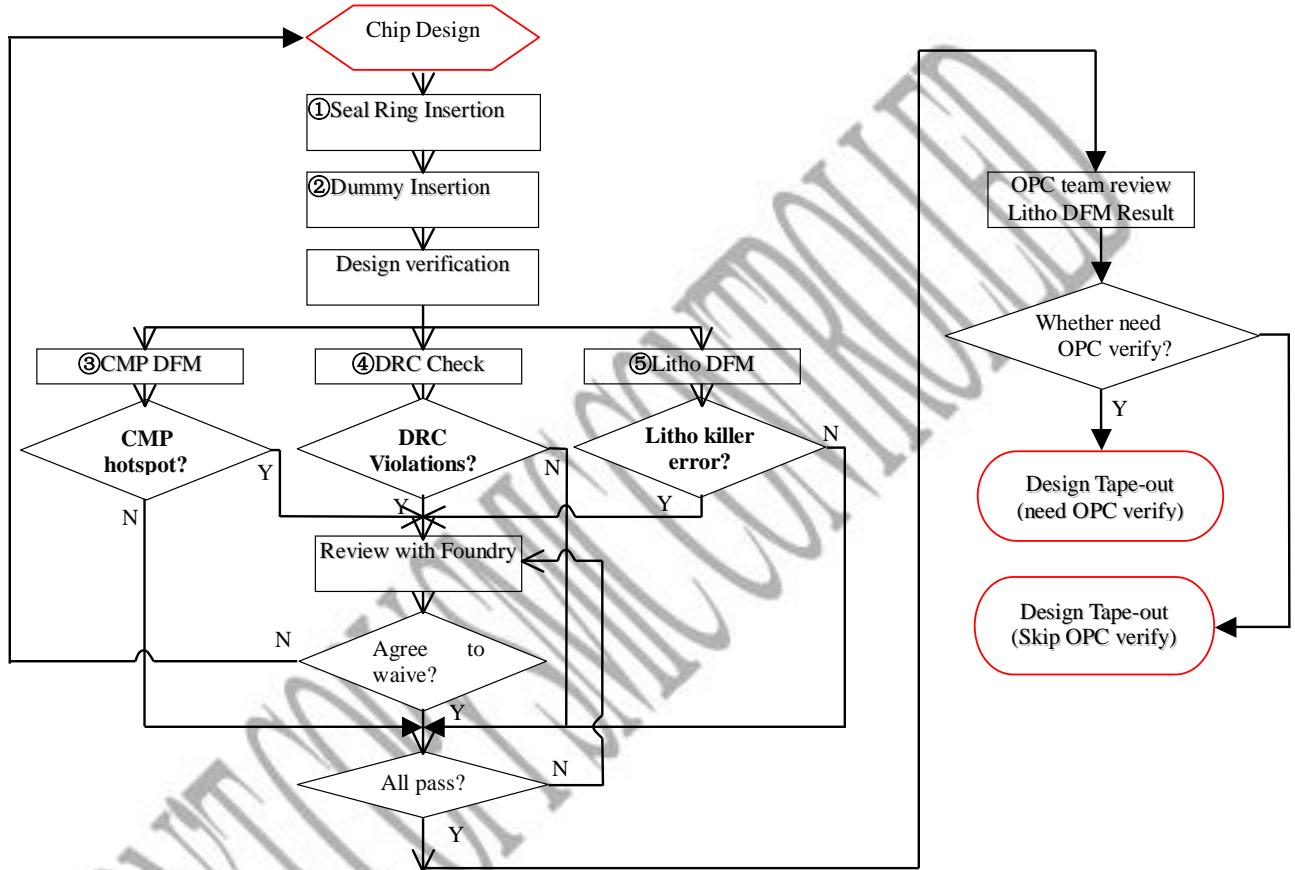


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7.1.14 Design Check Flow for Tape out

7.1.14.1 Design Check Flow before Tape out



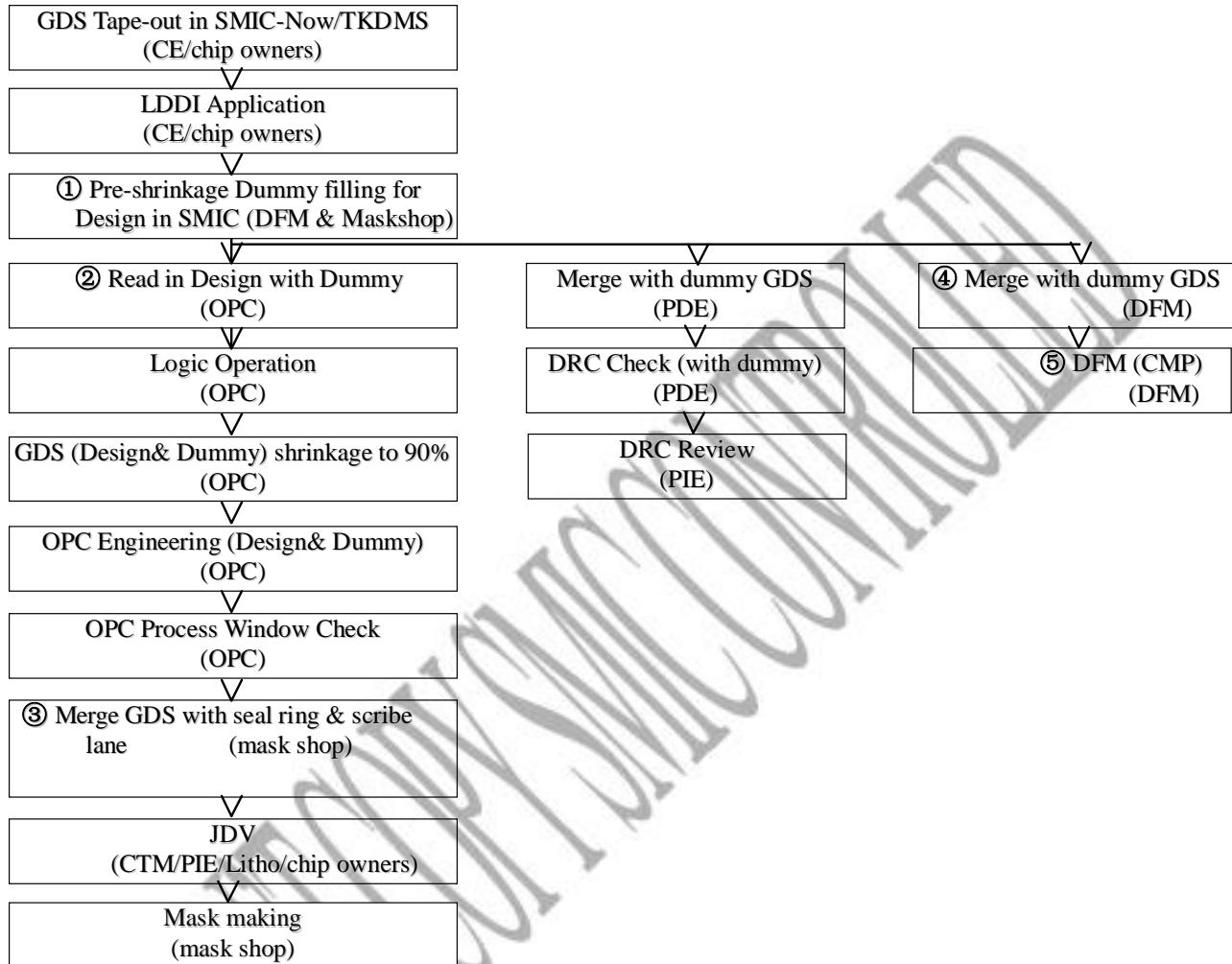
Notes:

1. Designer must clean DRC and DFM litho killer errors before tape-out. Non-cleans can not be waived unless SMIC does so after reviews.
2. Recommend designers to add seal ring (Step①) before DRC and DFM check following SMIC 28nm seal ring GDS sample.
3. Recommend designers to do dummy insertions (Step②) before DRC and DFM check. Without dummy inserted, design verification, CMP DFM, and DRC results related to dummy patterns will not be accurate.
4. Recommend designers to do the steps of ③, ④ and ⑤ by themselves. SMIC can help to do the work before tape out if designers have concerns or difficulties.

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7.1.14.2 Post-Tape out Working Flow



Notes:

- If designers have inserted dummies and do not request SMIC to add dummy. Dummy patterns will be treated as design patterns. Steps of ① related with dummy will be skipped.
- If designers revised GDS layout (mask re-tooling) for the layers which need dummy insertion, in the step ①, all layers' dummies of this GDS should be generated again by DFM team, and then DFM team will pass the new version dummy file to relative departments.
- If designers have added seal ring before tape out, seal ring merge in the step of ③ will be skipped. The seal ring GDS in step ③ is post shrinkage design (28nm).
- DRC violations and DFM litho killer errors must be clean before tape-out. Designers must pass the results to SMIC.
- If designers have added dummy filling and performed DFM CMP simulation before tape-out, step ④ and ⑤ can be skipped.

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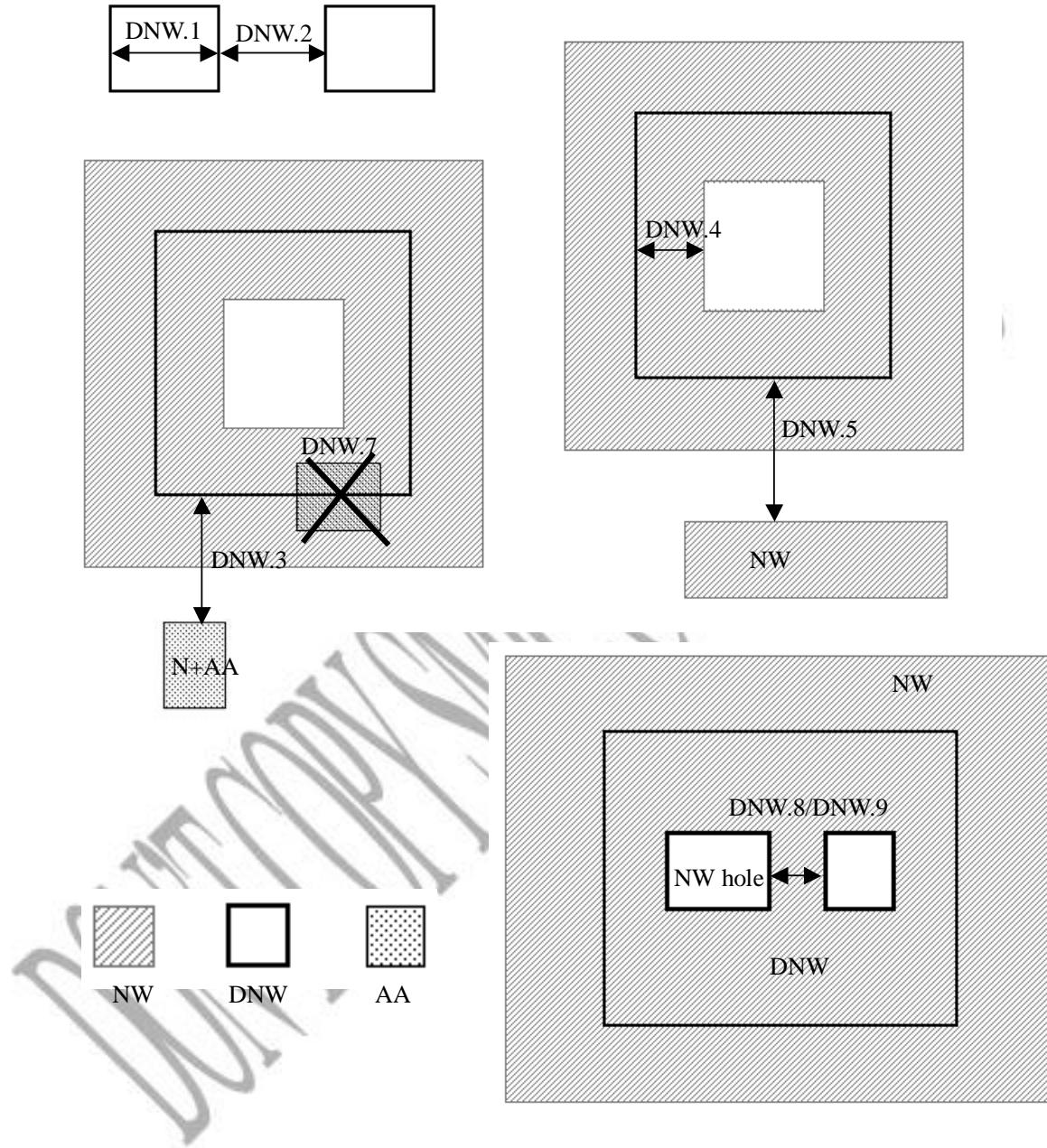
7.2 Layout Rule Description

7.2.1 DNW: Deep N-Well design rules

Rule number	Description	Operation	Design Value	Unit
DNW.1	DNW width	\geq	3	um
DNW.2	Space between DNWs	\geq	3.5	um
DNW.3	Space between DNW and N+AA (N+AA outside of DNW or NW)	\geq	1.65	um
DNW.4	Overlap of NW and DNW	\geq	0.4	um
DNW.5	Space between DNW and NW at different nets	\geq	2.5	um
DNW.6	N+AA enclosure by DNW	\geq	0.465	um
DNW.7	It is not allowed that N+AA CUT DNW			
DNW.8	Space between ((NW hole INSIDE DNW) NOT INTERACT (DG OR TG)) and ((NW hole INSIDE DNW) NOT INTERACT (DG OR TG)) or (PW NOT DNW) at different nets.	\geq	0.8	um
DNW.9	Space between ((NW hole INSIDE DNW) INTERACT (DG OR TG)) and (NW hole INSIDE DNW) or (PW NOT DNW) at different nets. DRC doesn't check LDBK region.	\geq	1	um

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7.2.2 AA: Active Area design rules

Rule number	Description	Operation	Design Value	Unit
AA.1	AA width DRC doesn't check INST and RFSRAM region.	\geq	0.05	um
AA.1a ^[R]	Recommended AA width. DRC doesn't check INST and RFSRAM region.	\geq	0.06	um
AA.1b ^[R]	Recommended AA width.	\leq	30	um
AA.2 ^[R]	Width of (((AA or AA_DMY) sizing up 0.39um) sizing down 0.39um) NOT (poly or POLY_DMY)) DRC doesn't check BIPOLA and DSTR region.	\leq	7	um
AA.3a	Channel width for core NMOS/PMOS transistors.	\geq	0.1	um
	DRC doesn't check for PSUB, VARMOS, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY , INST, RFSRAM region, and AA without CT.	\leq	3	um
AA.3b	Channel width for I/O NMOS/PMOS transistors. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region, and AA without CT.	\geq	0.27	um
AA.4	Width of 45-degree AA.	\geq	0.45	um
AA.5	Space between two AAs. DRC doesn't check INDMY, INST and RFSRAM region.	\geq	0.07	um
AA.5 ^[R]	Recommended space between two AAs to prevent AA bridge. DRC doesn't check INST and RFSRAM region.	\geq	0.075	um
AA.6	Space between two AAs inside DG/TG DRC doesn't check LDBK region	\geq	0.15	um
AA.7	Space between two AAs when one or both AA widths are >0.09um , and parallel run length of two AAs is >0 . DRC doesn't check INDMY, INST and RFSRAM region.	\geq	0.08	um
AA.8	At least one side space between (AA or AA_DMY), when 1. Width of (AA or AA_DMY) W1 = 0.05um, the width is measured in parallel to space direction; 2. Width of two neighboring (AA or AA_DMY) W2 > 0.09um, the width is measured in parallel to space direction;	\geq	0.09	um

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Rule number	Description	Operation	Design Value	Unit
	3. The parallel run length of (AA or AA_DMY) and W1 and W2 > 0um.			
AA.9	Space between two (AA or AA_DMY), when 1. Width of (AA or AA_DMY) W1 > 0.09um; 2. Width of (AA or AA_DMY) W2 > 0.05um and < 0.07um; 3. The parallel run length > 0.3um	≥	0.1	um
AA.10	Space between two (AA or AA_DMY), when 1. Width of (AA or AA_DMY) W1 > 0.09um; 2. Width of (AA or AA_DMY) W2 < 0.09um ,and ≥ 0.07um; 3. The parallel run length > 0.3um.	≥	0.09	um
AA.11	Space between 45-degree AA and AA. DRC doesn't check INDMY region.	≥	0.45	um
AA.12	Space between U-shape (or O-shape) AA inner edges.	≥	0.13	um
AA.13	Space between U-shape (or O-shape) AA inner edges when the U-shape (or O-shape) AA interact with poly.	≥	0.21	um
AA.14	(AA or AA_DMY) space which (AA or AA_DMY) space is covered by DUMBA. DRC check maximum STI width in DUMBA.	≤	10	um
AA.14 ^[R]	(AA or AA_DMY) space which (AA or AA_DMY) space is covered by DUMBA. DRC check maximum STI width in DUMBA.	≤	5	um
AA.15	Space between (AA or AA_DMY) DRC check maximum STI width. DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	≤	10	um
AA.15 ^[R]	Space between (AA or AA_DMY) DRC check maximum STI width. DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	≤	5	um
AA.16	Space between AA and (AA INTERACT poly) along channel width direction, when channel width < 0.15um, AA area < 0.0468um ² , and the runlength between AA and channel >0um.	≥	0.09	um

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Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check INST and RFSRAM region.			
AA.17	(Purposely blank)			
AA.18	NW enclosure of N+ pickup AA. DRC doesn't check resistor NW, LDBK, INST, RFSRAM region.	\geq	0.065	um
AA.19	Space between NW and N+AA. DRC doesn't check resistor NW, LDBK, INST, RFSRAM region.	\geq	0.065	um
AA.20	Space between N+AA corner edge and NW corner edge. DRC follows below conditions to check: 1. The edge of E1 \leq 0.105um, the edge of E2 \leq 0.065um. 2. DRC only flags the opposite space between E1 and E2. 3. DRC flags the space between concave corner and convex corner. DRC doesn't check resistor NW, INST, RFSRAM and LDBK region.	\geq	0.105	um
AA.21	Space between NW and (N+AA INTERCACT (DG OR TG)) DRC doesn't check resistor NW region and LDBK region.	\geq	0.18	um
AA.22	NW enclosure of P+AA. DRC doesn't check LDBK, INST, RFSRAM region.	\geq	0.065	um
AA.23	NW corner edge enclosure of P+AA corner edge. 1. The edge of E1 \leq 0.105um, the edge of E2 \leq 0.065um 2. DRC only flags the opposite space between E1 and E2. 3. DRC flags the enclosure between concave corner and concave corner; or the enclosure between convex corner and convex corner. DRC doesn't check LDBK region.	\geq	0.105	um
AA.24	NW enclosure of (P+AA INTERACT (DG OR TG)). DRC doesn't check LDBK region.	\geq	0.18	um
AA.25	Space between NW and P+ pickup AA. DRC doesn't check LDBK, INST, RFSRAM region.	\geq	0.065	um

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Rule number	Description	Operation	Design Value	Unit
AA.26	(AA and AA_DMY) density. Density check window size: 20um*20um, step size: 10um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\geq	20%	
AA.27	(AA and AA_DMY) density for non-IO region. Density check window size: 150um*150um, step size: 75um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\leq	80%	
AA.28	(AA and AA_DMY) for IO region. Density check window size: 150um*150um, step size: 75um DRC don't check: 1. NW resistor 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 3. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.	\leq	90%	
AA.29	(AA or AA_DMY) density in full chip	\geq \leq	25% 75%	
AA.30 ^[R]	(AA or AA_DMY) density inside of the dummy block area(DUMBA), Density check window size: 20um*20um, step size: 10um DRC need check the design if DUMBA width is >5um and <20um, where density ratio= AA area/DUMBA area.	\geq	20%	
AA.31a	AA area. DRC doesn't check INST and RFSRAM region.	\geq	0.018	um ²
AA.31b	AA area when AA all of edge length <0.13um	\geq	0.04	um ²

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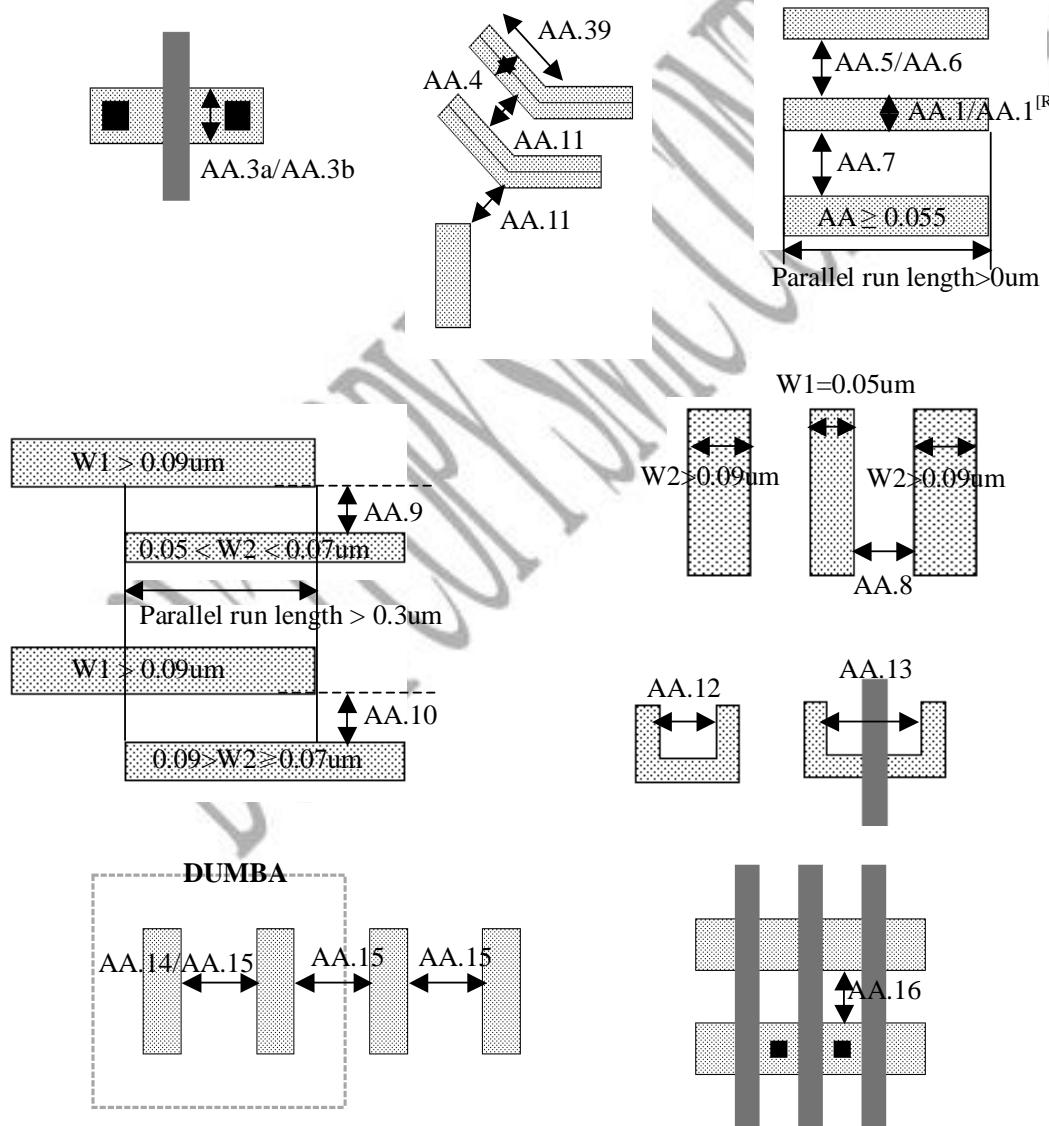
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Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check INST region and the AA with 0.1um x 0.3um rectangular patterns			
AA.32	AA area when AA any edge length <0.1um. DRC doesn't check INST and RFSRAM region.	\geq	0.03	um ²
AA.33	AA enclosed area.	\geq	0.0288	um ²
AA.34	AA enclosed area when any of inner edge length < 0.13um	\geq	0.04	um ²
AA.35	Area sum of ((AA AND SP) INTERACT poly) NOT ((poly or GTDMP) or GTDOP)) in the same AA for core PMOS device.	\leq	280	um
AA.36a	AA length between two CTs when AA width <0.1um. This rule doesn't check the region of (MOMDMY sizing up 5um).	\leq	18	um
AA.36b	AA length between one CT and this AA line-end when AA width <0.1um. AA line-end definition: AA edge <0.1um, and the AA edge is between two consecutive 90degree outer vertex. This rule doesn't check the region of (MOMDMY sizing up 5um).	\leq	18	um
AA.37	L-shape AA edge length (L1) (AA INTERACT poly) when L-shape AA width (W1) <0.18um in source/drain direction. L-shape AA edge definition: the edge is between consecutive 90degree outer vertex and 270 degree inner vertex.	\leq	0.275	um
AA.38	(Purposely blank)			
AA.39	45-degree AA edge length	\geq	0.45	um
AA.40	Any edge length of (AA INTERACT poly) with another adjacent edge length <0.13um. DRC doesn't check INST and RFSRAM region.	\geq	0.13	um
AA.41	(Purposely blank)			
AA.42^[R]	Recommended at least two polys interact horizontal edge of T-shape AA. This check doesn't check LOGO, INST and RFSRAM region.			
AA.43	AA must be fully covered by (SP or SN) (except AA_DMY and RESNW related region).			

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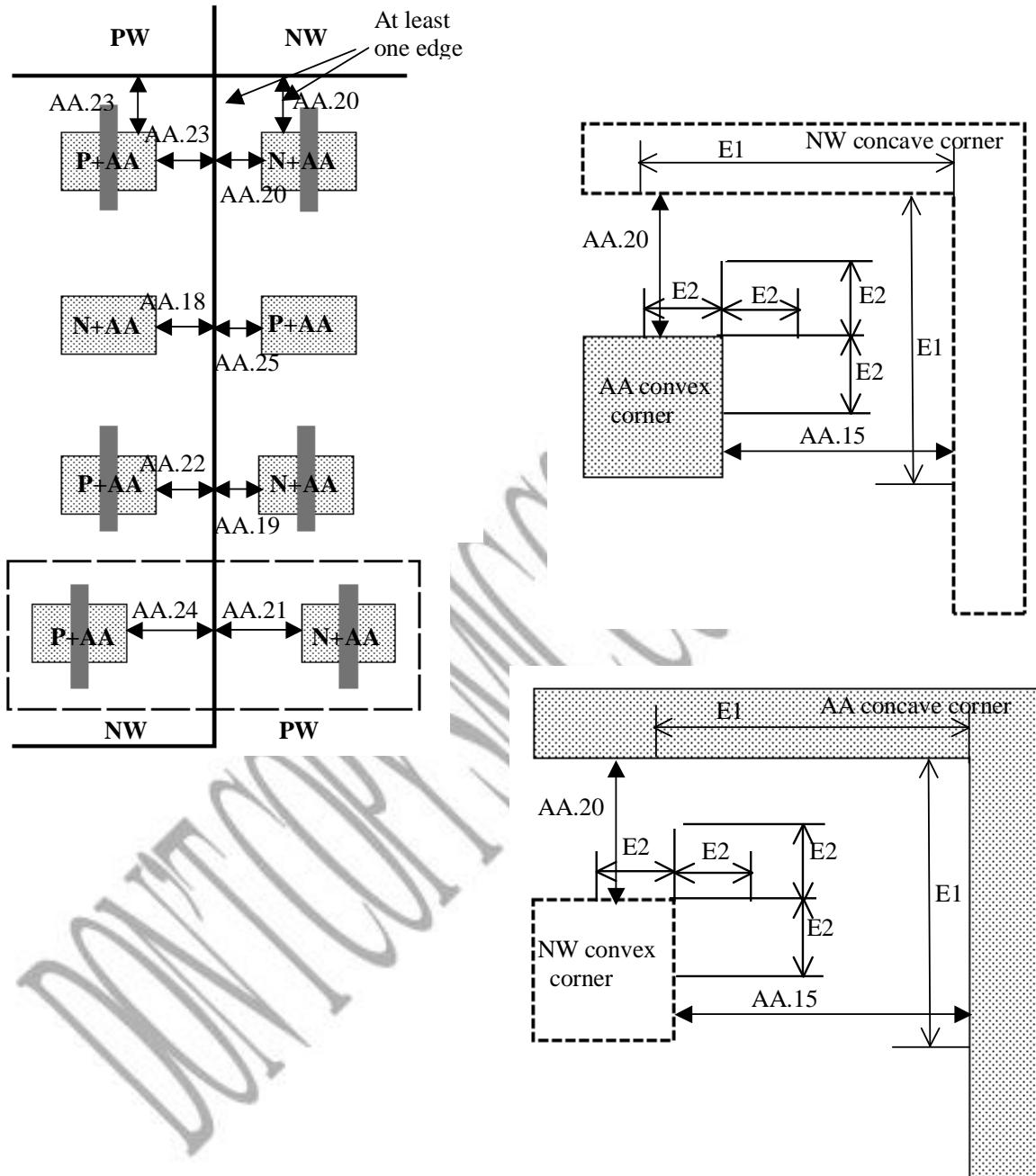
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Rule number	Description	Operation	Design Value	Unit
	DRC doesn't check LOGO and OCOVL region.			
AA.44	(AA INTERACT poly) must be rectangular, single L-, T-, or U-shape and the GATE direction must be perpendicular to the edge (E) of this T- or U-shape design. (45-degree edge is not allowed) DRC doesn't check INDMY, LOGO, INST and RFSRAM region.			



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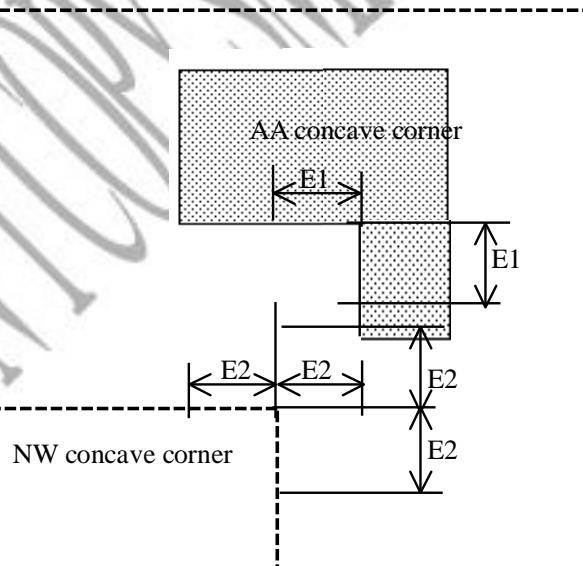
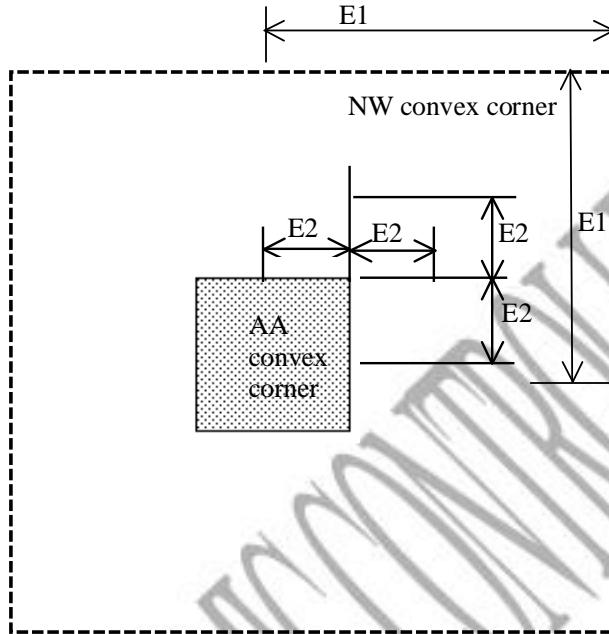
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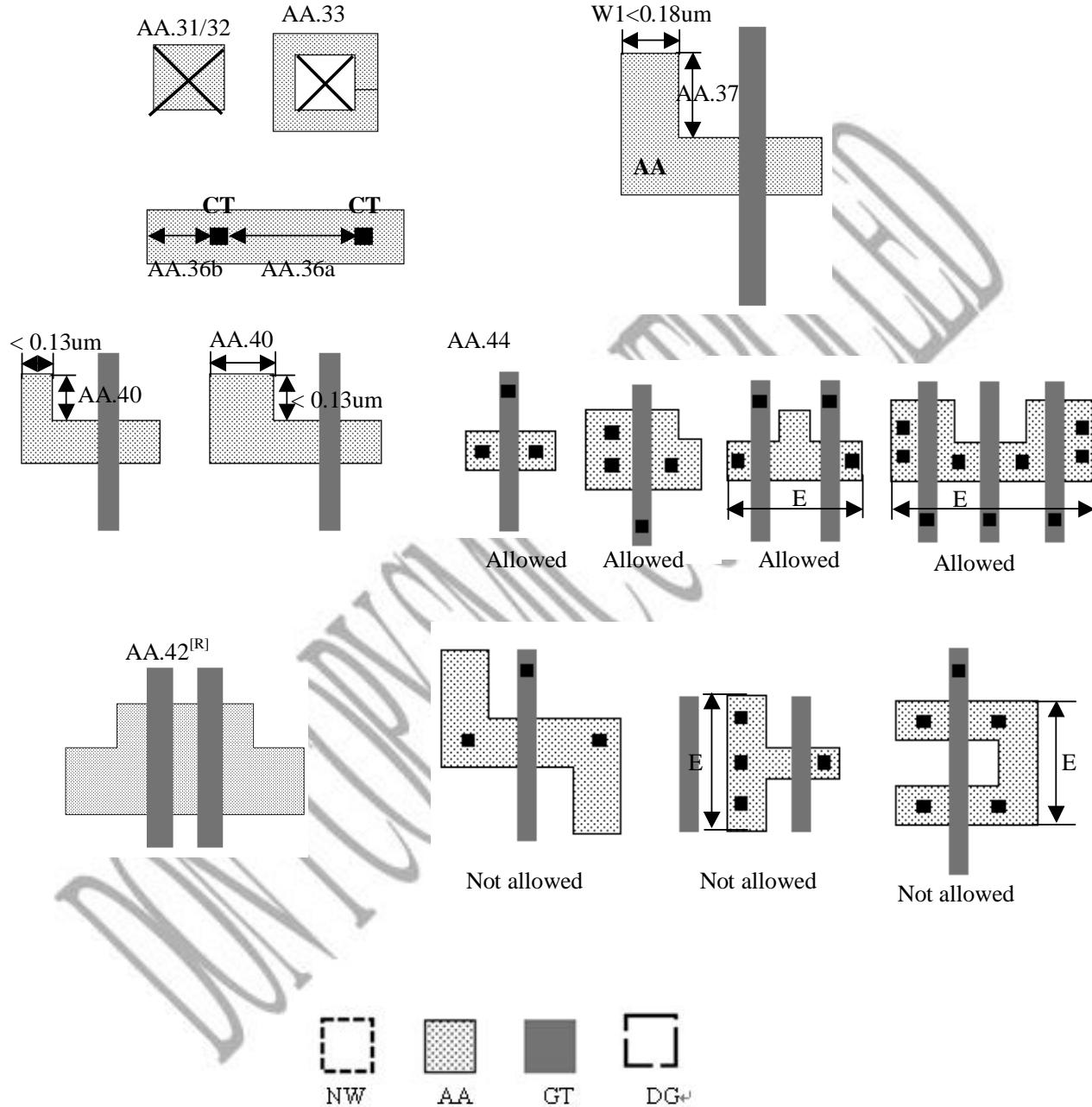
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AA.23



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7.2.3 AADMP: AA Dummy rules

Rule number	Description	Operation	Design Value	Unit
AADMP.1	AADMP width	\geq	0.05	um
AADMP.2	AADMP width inside DG/TG	\geq	0.1	um
AADMP.3	Space between AADMP and (AA or AA_DMY). (AADMP and AA overlap is not allowed)	\geq	0.08	um
AADMP.4	Space between AADMP and (AA or AA_DMY) inside DG/TG (overlap is not allowed)	\geq	0.15	um
AADMP.5	Space between AADMP and 45-degree AA	\geq	0.45	um
AADMP.6	Space between AADMP and (poly OR GTDOP OR GTDMP) (It's not allowed AADMP overlap with ((poly OR GTDUM) OR GTDOP))	\geq	0.025	um
AADMP.7	Space between AADMP and NW	\geq	0.08	um
AADMP.8	Space between AADMP and RESNW (overlap is not allowed)	\geq	0.7	um
AADMP.9	(Purposely blank)			
AADMP.10	Space between AADMP and PSUB (overlap is not allowed if AA inside PSUB) DRC doesn't check MOMDMY region.	\geq	0.14	um
AADMP.11	Space between AADMP and DG/TG. It's not allowed AADMP CUT DG/TG	\geq	0.08	um
AADMP.12	Space between AADMP and SP It's not allowed AADMP CUT SP.	\geq	0.065	um
AADMP.13	NW enclosure of AADMP. DRC doesn't check OCCD region.	\geq	0.065	um
AADMP.14	DG/TG enclosure of AADMP	\geq	0.08	um

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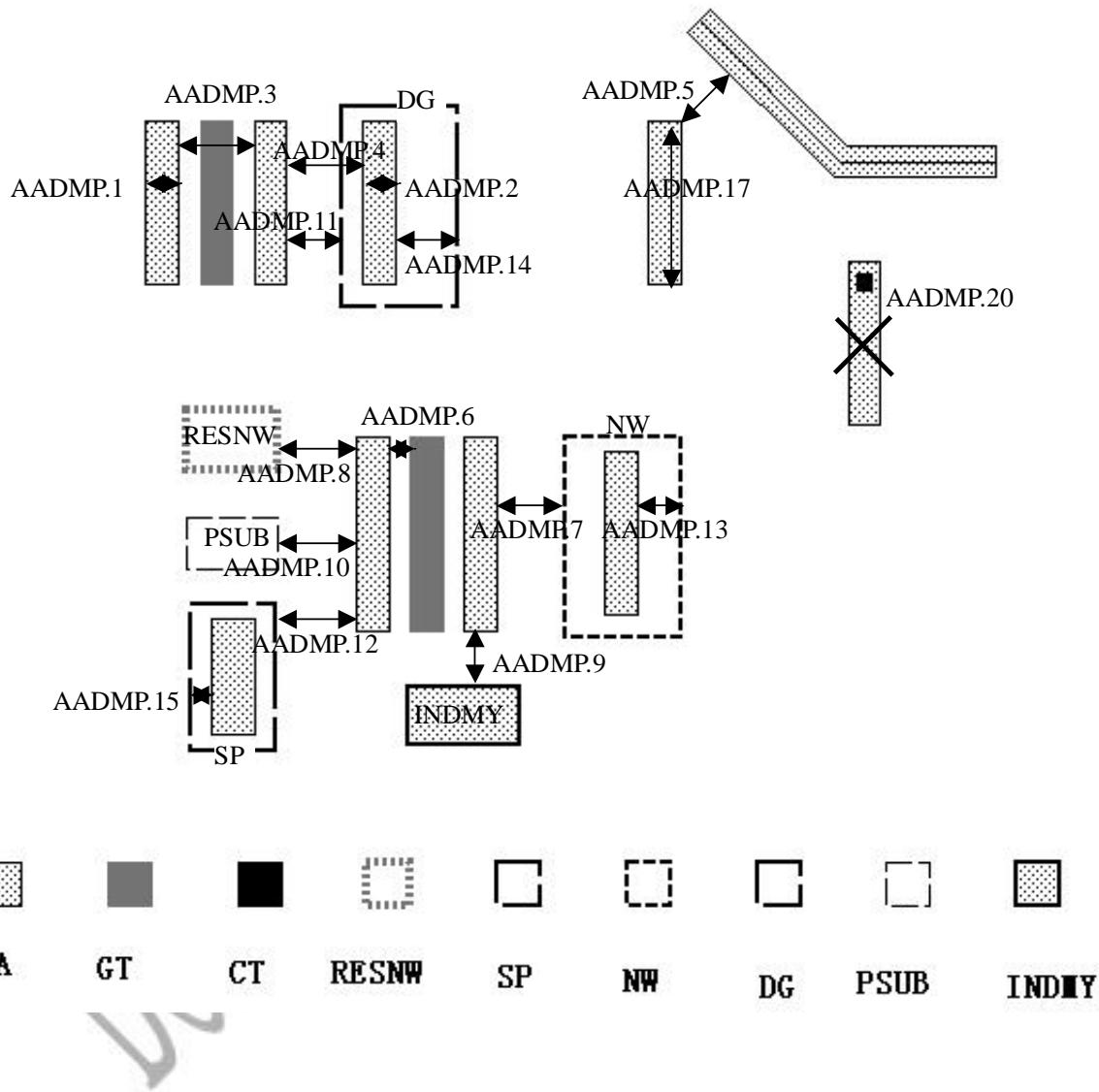


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Rule number	Description	Operation	Design Value	Unit
AADMP.15	SP enclosure of AADMP. DRC doesn't check OCCD region.	\geq	0.065	um
AADMP.16	AADMP area	\geq	0.03	um ²
AADMP.17	AADMP length. This rule doesn't check RESP2, RESAA and MOMDMY regions.	\leq	16	um
AADMP.18	(AADMP AND AADOP) density. DRC check window follow: ((AA OR poly) INTERACT GATE) sizing up 2um) NOT ((AA OR poly) sizing up 0.15um)) This rule doesn't check DG, TG, VARMOS, NODMF, INST, RFSRAM, OCOVL, OCCD regions.	\geq	10%	
AADMP.19	It's not allowed 45-degree AADMP.			
AADMP.20	CT is not allowed to INTERACT with AADMP			
AADMP.21	AADMP must be rectangular. DRC doesn't check OCCD region.			

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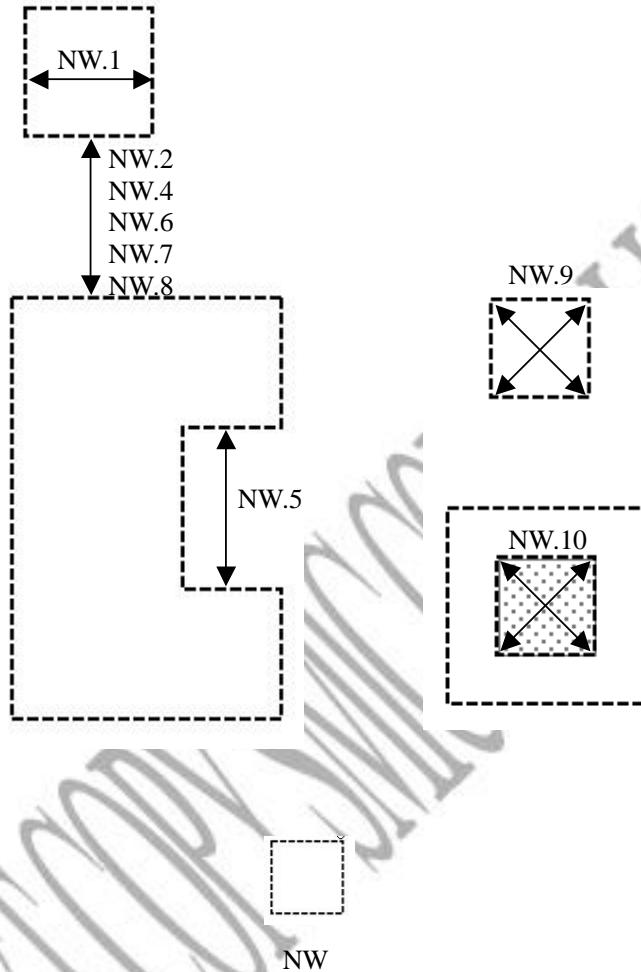
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7.2.4 NW: N-Well rule

Rule number	Description	Operation	Design Value	Unit
NW.1	NW width. DRC doesn't check INST and RFSRAM region.	\geq	0.24	um
NW.2	NW space	\geq	0.24	um
NW.3^[R]	Space between NWs if at least one NW width<0.28um. DRC doesn't check INST and RFSRAM region.	\geq	0.28	um
NW.4	Space between NWs with parallel run length >0.5um, which NWs space is on STI (NOT INTERACT AA or AA_DMY)	\geq	0.3	um
NW.5	Space between NWs at same net	\geq	0.24	um
NW.6	Space between 0.9V NWs at different net.	\geq	0.8	um
NW.7	Space between 0.9V NW and 1.8V/2.5V NW at different net	\geq	1	um
NW.8	Space between 1.8V/2.5V NWs at different net DRC doesn't check LDBK region	\geq	1	um
NW.9	NW area	\geq	0.4	um ²
NW.10	NW enclosed area	\geq	0.4	um ²
NW.11	Area of (NW NOT DG), (DG AND NW), (NW NOT TG), (TG AND NW)	\geq	0.35	um ²
NW.12	Enclosed area of (NW NOT DG), (DG AND NW), (NW NOT TG), (TG AND NW)	\geq	0.35	um ²

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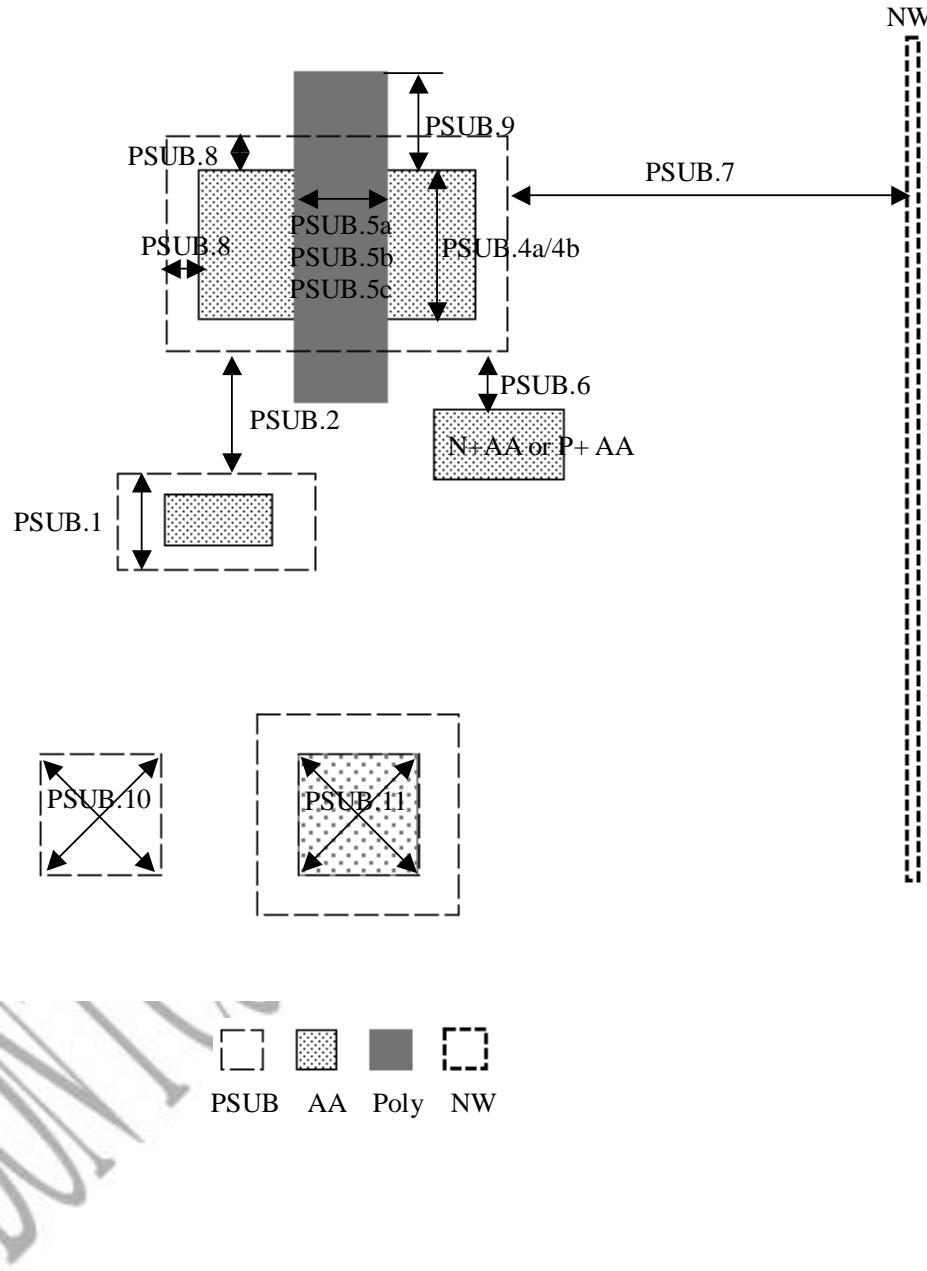
7.2.5 PSUB: PSUB design rules to define native NMOS

PSUB is to define the area for a native NMOS device on a P-substrate

Rule number	Description	Operation	Design Value	Unit
PSUB.1	PSUB width	\geq	0.24	um
PSUB.2	PSUB space	\geq	0.24	um
PSUB.3^[R]	Space of PSUBs if at least one PSUB width<0.28um	\geq	0.28	um
PSUB.4	Channel width for native NMOS	\geq	0.5	um
PSUB.5a	Channel length for 0.9V NMOS	\geq	0.2	um
		\leq	1	um
PSUB.5b	Channel length for 1.8V IO NMOS	\geq	0.8	um
		\leq	2	um
PSUB.5c	Channel length for 2.5V IO NMOS	\geq	1.2	um
		\leq	2	um
PSUB.6	Space between PSUB and N+AA or P+AA.	\geq	0.38	um
PSUB.7	Space between PSUB and NW.	\geq	0.8	um
PSUB.8	MOS AA enclosure by PSUB. DRC doesn't check IND MY region.	=	0.16	um
PSUB.9	((Poly extension outside of AA) NOT OUTSIDE PSUB) along poly length direction. DRC doesn't check IND MY region.	\geq	0.24	um
PSUB.10	PSUB area.	\geq	0.4	um ²
PSUB.11	PSUB enclosed area.	\geq	0.4	um ²
PSUB.12	PSUB must not overlap NW or DNW.			
PSUB.13	One AA shape per PSUB shape, except for NMOS capacitors, pickup region.			
PSUB.14	It's not allowed P+ GATE in PSUB. DRC doesn't check IND MY region.			

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7.2.6 Low Vt MOS design rules

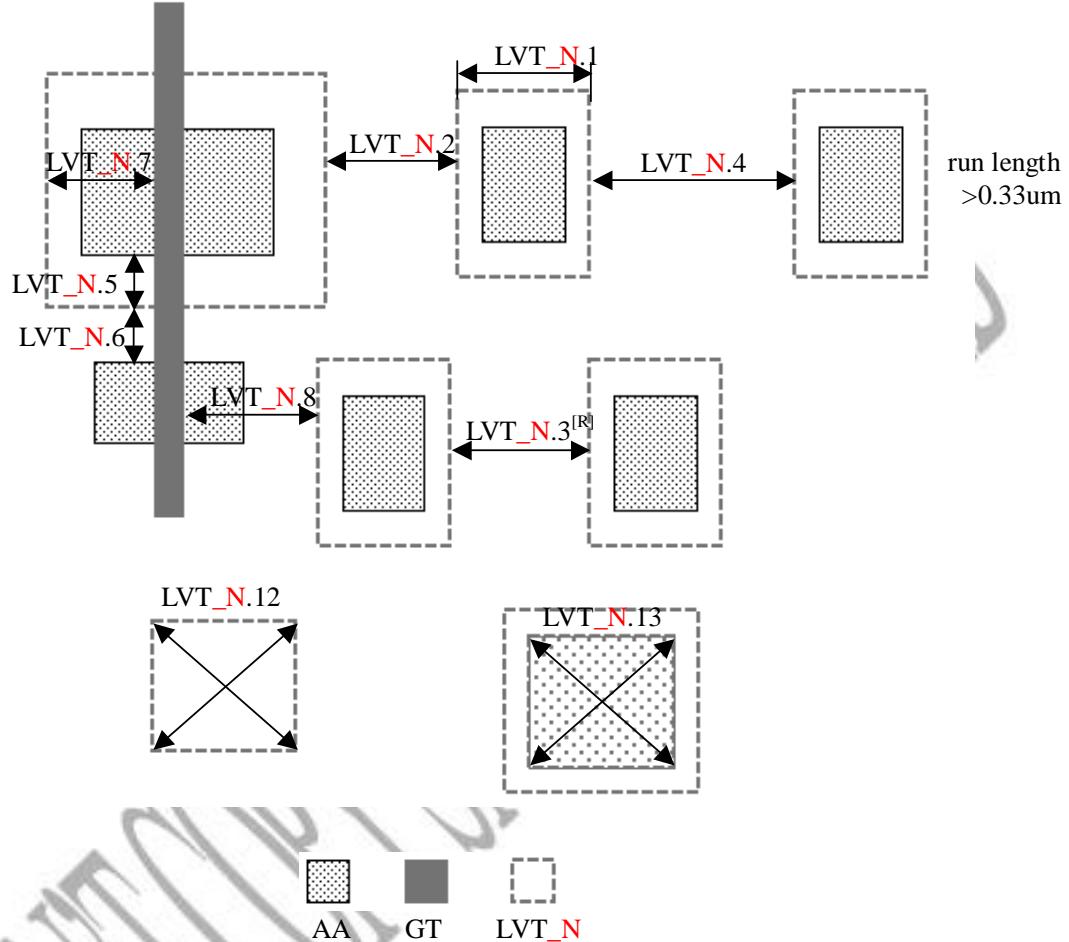
7.2.6.1 LVT_N : Low Vt NMOS design rules

A drawn LVT_N layer is needed to define low Vt NMOS devices. LVT_N is for Ncore low Vt devices only.

Rule number	Description	Operation	Design Value	Unit
LVT_N.1	LVT_N width. Single-point-interaction is allowed. DRC doesn't highlight the violation when LVT_N opposite side width $\geq 0.135\mu m$, and $< 0.16\mu m$.	\geq	0.16	um
LVT_N.2	Space between LVT_Ns. DRC doesn't highlight the violation when LVT_N opposite side width $\geq 0.135\mu m$, and $< 0.16\mu m$.	\geq	0.16	um
LVT_N.3 ^[R]	Space between LVT_Ns with parallel run length $> 0.24\mu m$, when one LVT_N width $> 0.22\mu m$.	\geq	0.18	um
LVT_N.4	Space between LVT_Ns with parallel run length $> 0.33\mu m$, and LVT_N space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
LVT_N.5	LVT_N extension outside of GATE along GATE poly direction.	\geq	0.065	um
LVT_N.6	Space between LVT_N and GATE along GATE poly direction.	\geq	0.065	um
LVT_N.7	LVT_N extension outside of GATE along source/drain direction.	\geq	0.115	um
LVT_N.8	Space between LVT_N and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT LVT_N) is not allowed.	\geq	0.115	um
LVT_N.9	Space between LVT_N and non-silicided AA/H-R resistor	\geq	0.15	um
LVT_N.10	45-degree edge length	\geq	0.52	um
LVT_N.11	LVT_N overlap HVT_N, ULVT_N, UHVT_N, LVT_P, HVT_P, ULVT_P, UHVT_P, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA, LOGO is prohibited.			
LVT_N.12	LVT_N area	\geq	0.1	um ²
LVT_N.13	LVT_N enclosed area	\geq	0.1	um ²

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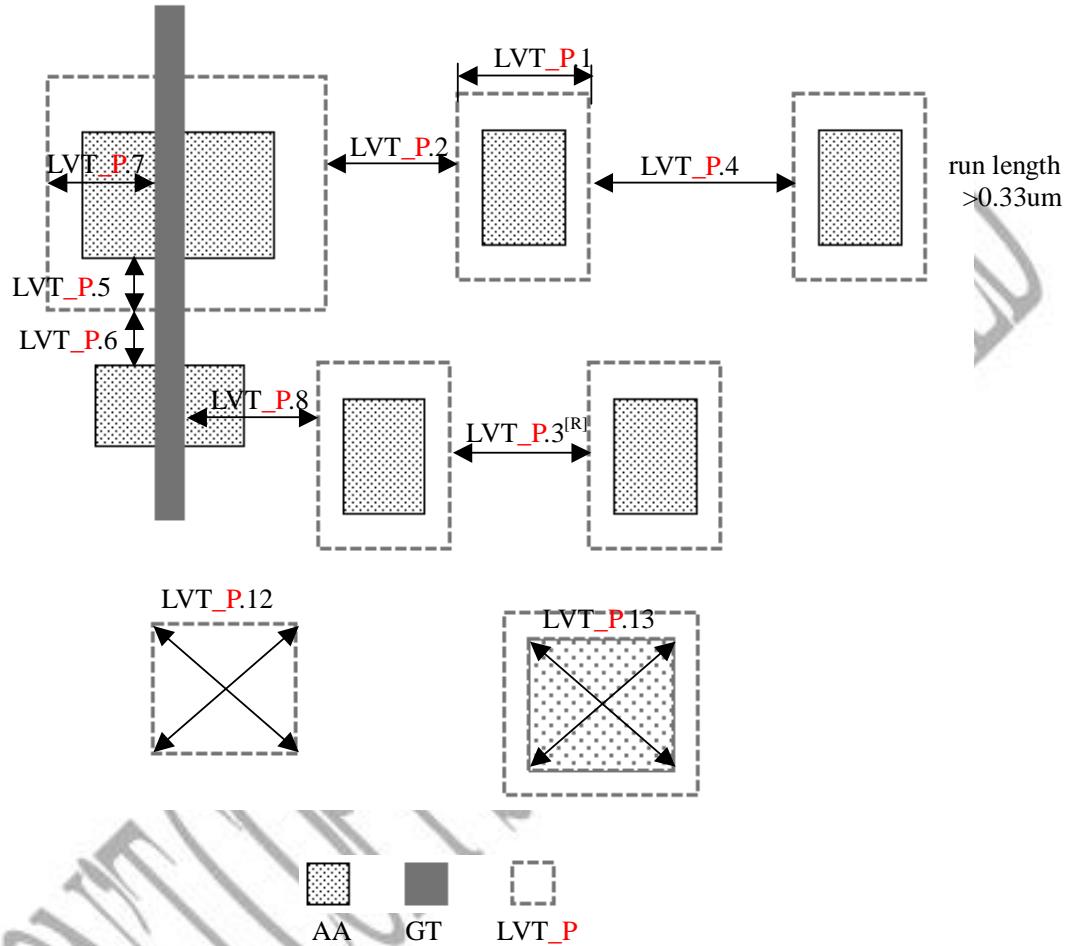
7.2.6.2 LVT_P : Low Vt PMOS design rules

A drawn LVT_P layer is needed to define low Vt PMOS devices. LVT_P is for Pcore low Vt devices only.

Rule number	Description	Operation	Design Value	Unit
LVT_P.1	LVT_P width. Single-point-interaction is allowed. DRC doesn't highlight the violation when LVT_P opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
LVT_P.2	Space between LVT_Ps. DRC doesn't highlight the violation when LVT_P opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
LVT_P.3 ^[R]	Space between LVT_Ps with parallel run length $>0.24\text{um}$, when one LVT_P width $>0.22\text{um}$.	\geq	0.18	um
LVT_P.4	Space between LVT_Ps with parallel run length $>0.33\text{um}$, and LVT_P space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
LVT_P.5	LVT_P extension outside of GATE along GATE poly direction.	\geq	0.065	um
LVT_P.6	Space between LVT_P and GATE along GATE poly direction.	\geq	0.065	um
LVT_P.7	LVT_P extension outside of GATE along source/drain direction.	\geq	0.115	um
LVT_P.8	Space between LVT_P and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT LVT_P) is not allowed.	\geq	0.115	um
LVT_P.9	Space between LVT_P and non-silicided AA/H-R resistor	\geq	0.15	um
LVT_P.10	45-degree edge length	\geq	0.52	um
LVT_P.11	LVT_P overlap HVT_N, ULVT_N, UHVT_N, LVT_N, HVT_P, ULVT_P, UHVT_P, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA, LOGO is prohibited.			
LVT_P.12	LVT_P area	\geq	0.1	um ²
LVT_P.13	LVT_P enclosed area	\geq	0.1	um ²

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7.2.7 High Vt MOS design rules

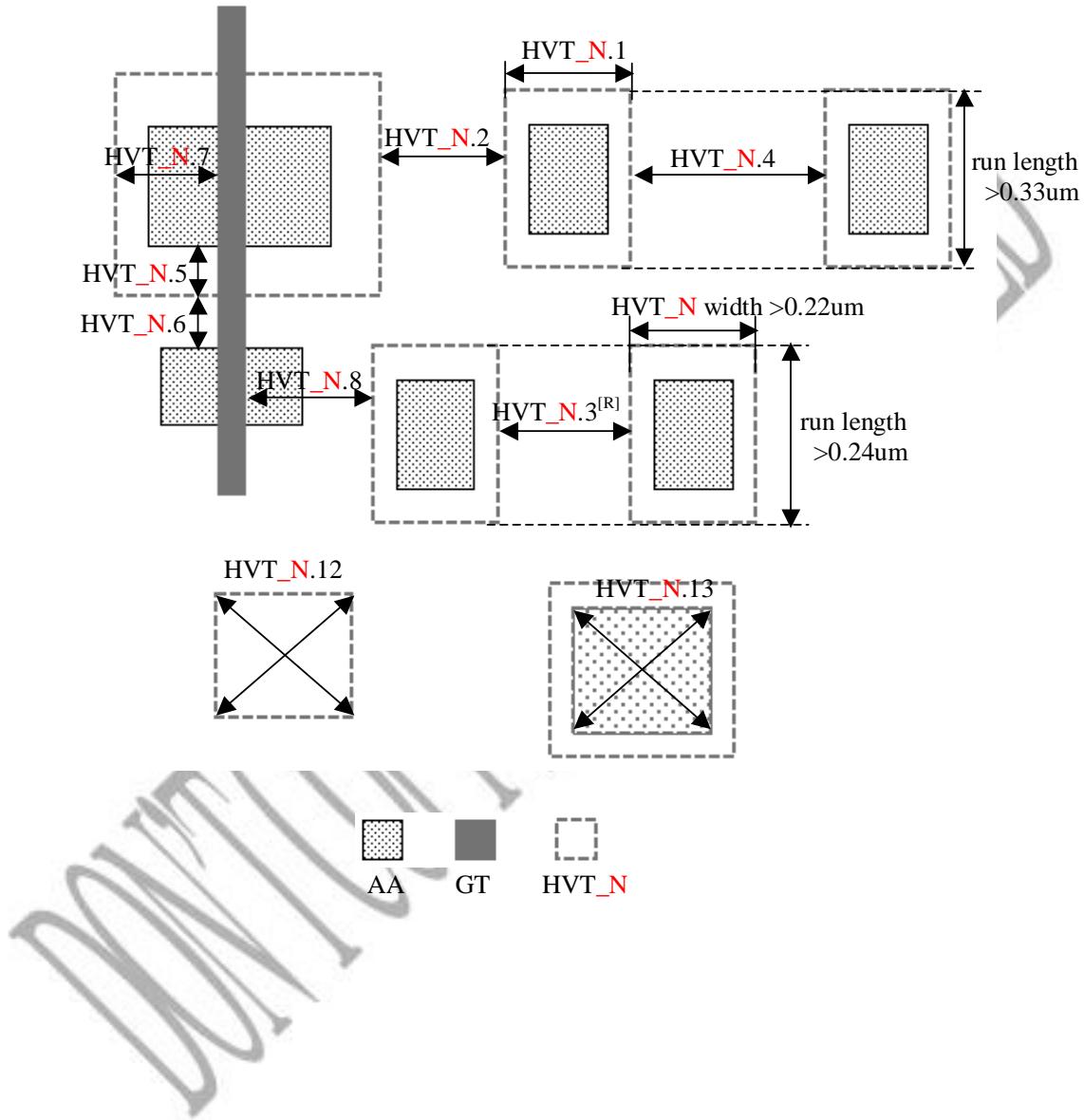
7.2.7.1 HVT_N : How Vt NMOS design rules

A drawn HVT_N layer is needed to define high Vt NMOS devices. HVT_N is for Ncore high Vt devices only.

Rule number	Description	Operation	Design Value	Unit
HVT_N.1	HVT_N width. Single-point-interaction is allowed. DRC doesn't highlight the violation when HVT_N opposite side width $\geq 0.135\mu m$, and $< 0.16\mu m$.	\geq	0.16	um
HVT_N.2	Space between HVT_Ns. DRC doesn't highlight the violation when HVT_N opposite side width $\geq 0.135\mu m$, and $< 0.16\mu m$.	\geq	0.16	um
HVT_N.3^[R]	Space between HVT_Ns with parallel run length $> 0.24\mu m$, when one HVT_N width $> 0.22\mu m$.	\geq	0.18	um
HVT_N.4	Space between HVT_Ns with parallel run length $> 0.33\mu m$, and HVT_N space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
HVT_N.5	HVT_N extension outside of GATE along GATE poly direction.	\geq	0.065	um
HVT_N.6	Space between HVT_N and GATE along GATE poly direction.	\geq	0.065	um
HVT_N.7	HVT_N extension outside of GATE along source/drain direction.	\geq	0.115	um
HVT_N.8	Space between HVT_N and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT HVT_N) is not allowed.	\geq	0.115	um
HVT_N.9	Space between HVT_N and non-silicided AA/H-R resistor	\geq	0.15	um
HVT_N.10	45-degree edge length	\geq	0.52	um
HVT_N.11	HVT_N overlap LVT_N, UHVT_N, ULVT_N, LVT_P, HVT_P, ULVT_P, UHVT_P, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA, LOGO is prohibited.			
HVT_N.12	HVT_N area	\geq	0.1	um ²
HVT_N.13	HVT_N enclosed area	\geq	0.1	um ²

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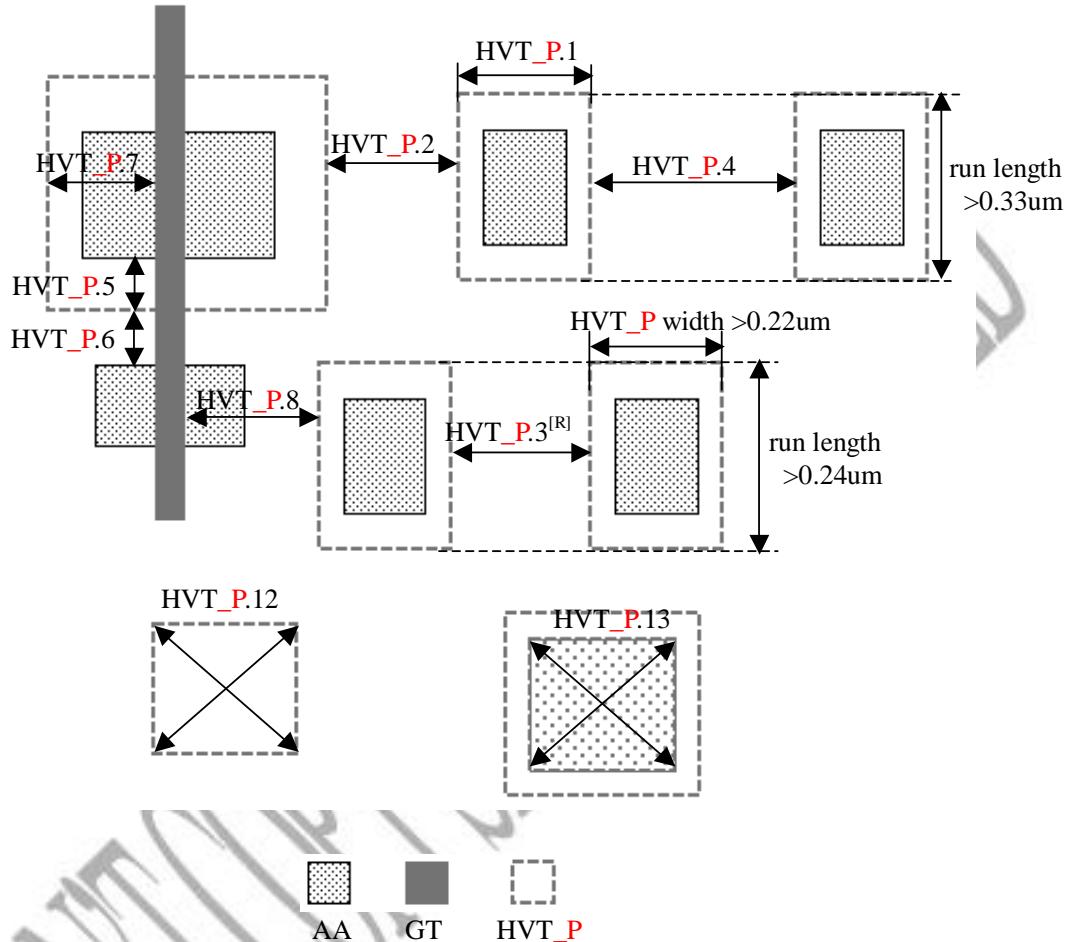
7.2.7.2 HVT_P : How Vt PMOS design rules

A drawn HVT_P layer is needed to define high Vt PMOS devices. HVT_P is for Pcore high Vt devices only.

Rule number	Description	Operation	Design Value	Unit
HVT_P.1	HVT_P width. Single-point-interaction is allowed. DRC doesn't highlight the violation when HVT_P opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
HVT_P.2	Space between HVT_Ps. DRC doesn't highlight the violation when HVT_P opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
HVT_P.3 ^[R]	Space between HVT_Ps with parallel run length $>0.24\text{um}$, when one HVT_P width $>0.22\text{um}$.	\geq	0.18	um
HVT_P.4	Space between HVT_Ps with parallel run length $>0.33\text{um}$, and HVT_P space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
HVT_P.5	HVT_P extension outside of GATE along GATE poly direction.	\geq	0.065	um
HVT_P.6	Space between HVT_P and GATE along GATE poly direction.	\geq	0.065	um
HVT_P.7	HVT_P extension outside of GATE along source/drain direction.	\geq	0.115	um
HVT_P.8	Space between HVT_P and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT HVT_P) is not allowed.	\geq	0.115	um
HVT_P.9	Space between HVT_P and non-silicided AA/H-R resistor	\geq	0.15	um
HVT_P.10	45-degree edge length	\geq	0.52	um
HVT_P.11	HVT_N overlap LVT_N, UHVT_N, ULVT_N, HVT_N, LVT_P, ULVT_P, UHVT_P, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA, LOGO is prohibited.			
HVT_P.12	HVT_P area	\geq	0.1	um ²
HVT_P.13	HVT_P enclosed area	\geq	0.1	um ²

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7.2.8 Ultra low Vt MOS design rules

7.2.8.1 ULVT_N : Ultra low Vt NMOS design rules

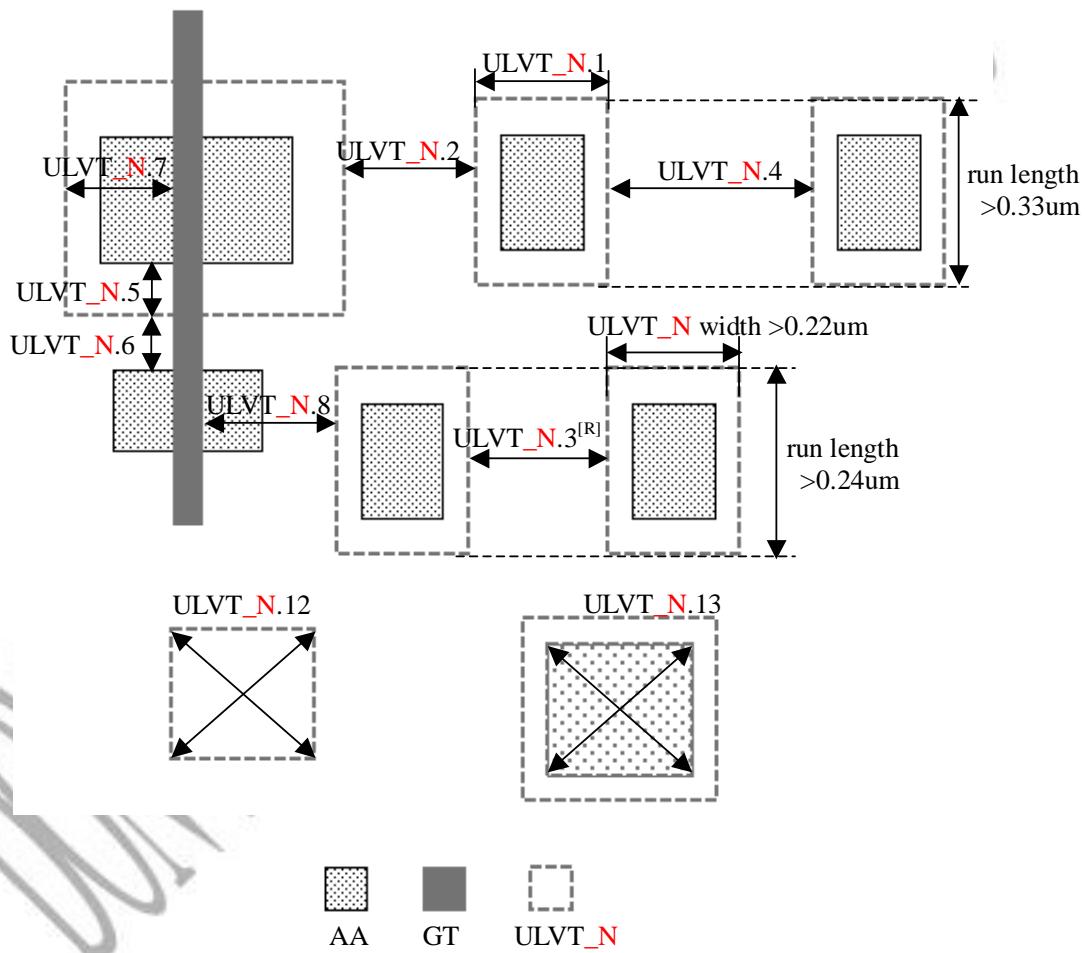
A drawn ULVT_N layer is needed to define ultra low Vt NMOS devices. ULVT_N is for Ncore ultra low Vt devices only.

Rule number	Description	Operation	Design Value	Unit
ULVT_N.1	ULVT_N width. Single-point-interaction is allowed. DRC doesn't highlight the violation when ULVT_N opposite side width \geq 0.135um, and $<$ 0.16um.	\geq	0.16	um
ULVT_N.2	Space between ULVT_Ns. DRC doesn't highlight the violation when ULVT_N opposite side width \geq 0.135um, and $<$ 0.16um.	\geq	0.16	um
ULVT_N.3 ^[R]	Space between ULVT_Ns with parallel run length $>$ 0.24um, when one ULVT_N width $>$ 0.22um.	\geq	0.18	um
ULVT_N.4	Space between ULVT_Ns with parallel run length $>$ 0.33um, and ULVT_N space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
ULVT_N.5	ULVT_N extension outside of GATE along GATE poly direction.	\geq	0.065	um
ULVT_N.6	Space between ULVT_N and GATE along GATE poly direction.	\geq	0.065	um
ULVT_N.7	ULVT_N extension outside of GATE along source/drain direction.	\geq	0.115	um
ULVT_N.8	Space between ULVT_N and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT ULVT_N) is not allowed.	\geq	0.115	um
ULVT_N.9	Space between ULVT_N and non-silicided AA/H-R resistor	\geq	0.15	um
ULVT_N.10	45-degree edge length	\geq	0.52	um
ULVT_N.11	ULVT_N overlap LVT_N, HVT_N, UHVT_N, LVT_P, HVT_P, UHVT_P, ULVT_N, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA,			

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Rule number	Description	Operation	Design Value	Unit
	LOGO is prohibited.			
ULVT_N.12	ULVT_N area	\geq	0.1	μm^2
ULVT_N.13	ULVT_N enclosed area	\geq	0.1	μm^2



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7.2.8.2 ULVT_P : Ultra low Vt PMOS design rules

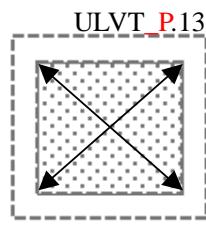
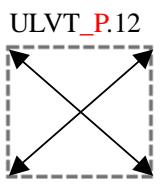
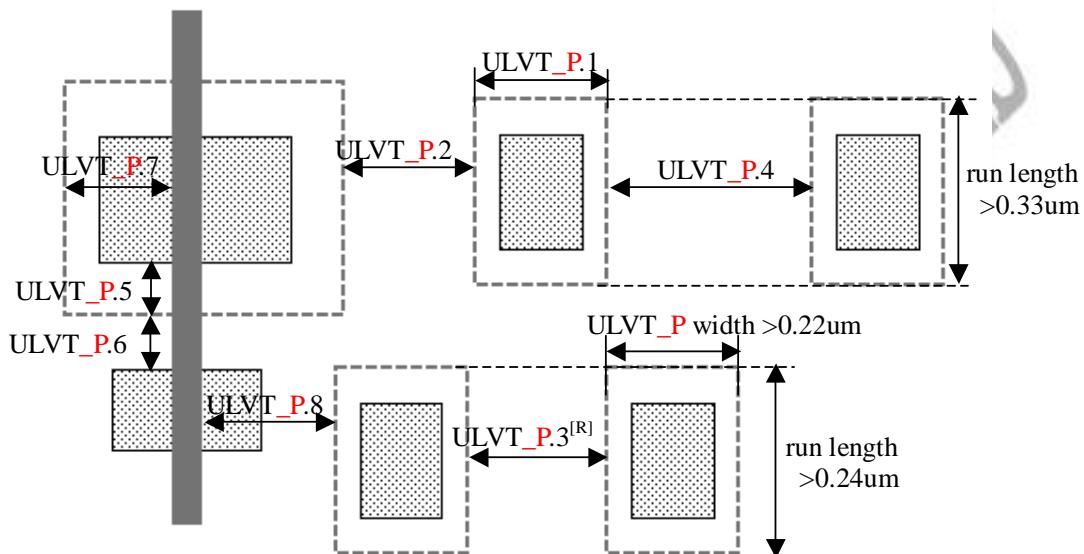
A drawn ULVT_P layer is needed to define ultra low Vt PMOS devices. ULVT_P is for Pcore ultra low Vt devices only.

Rule number	Description	Operation	Design Value	Unit
ULVT_P.1	ULVT_P width. Single-point-interaction is allowed. DRC doesn't highlight the violation when ULVT_P opposite side width \geq 0.135um, and $<$ 0.16um.	\geq	0.16	um
ULVT_P.2	Space between ULVT_Ps. DRC doesn't highlight the violation when ULVT_P opposite side width \geq 0.135um, and $<$ 0.16um.	\geq	0.16	um
ULVT_P.3 ^[R]	Space between ULVT_Ps with parallel run length $>$ 0.24um, when one ULVT_P width $>$ 0.22um.	\geq	0.18	um
ULVT_P.4	Space between ULVT_Ps with parallel run length $>$ 0.33um, and ULVT_P space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
ULVT_P.5	ULVT_P extension outside of GATE along GATE poly direction.	\geq	0.065	um
ULVT_P.6	Space between ULVT_P and GATE along GATE poly direction.	\geq	0.065	um
ULVT_P.7	ULVT_P extension outside of GATE along source/drain direction.	\geq	0.115	um
ULVT_P.8	Space between ULVT_P and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT ULVT_P) is not allowed.	\geq	0.115	um
ULVT_P.9	Space between ULVT_P and non-silicided AA/H-R resistor	\geq	0.15	um
ULVT_P.10	45-degree edge length	\geq	0.52	um
ULVT_P.11	ULVT_P overlap LVT_N, HVT_N, UHVT_N, ULVT_N, LVT_P, HVT_P, UHVT_P, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA, LOGO is prohibited.			

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Rule number	Description	Operation	Design Value	Unit
ULVT_P.12	ULVT_P area	\geq	0.1	μm^2
ULVT_P.13	ULVT_P enclosed area	\geq	0.1	μm^2



AA
 GT
 ULVT_P

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7.2.9 Ultra high Vt MOS design rules

7.2.9.1 UHVT_N : Ultra high Vt NMOS design rules

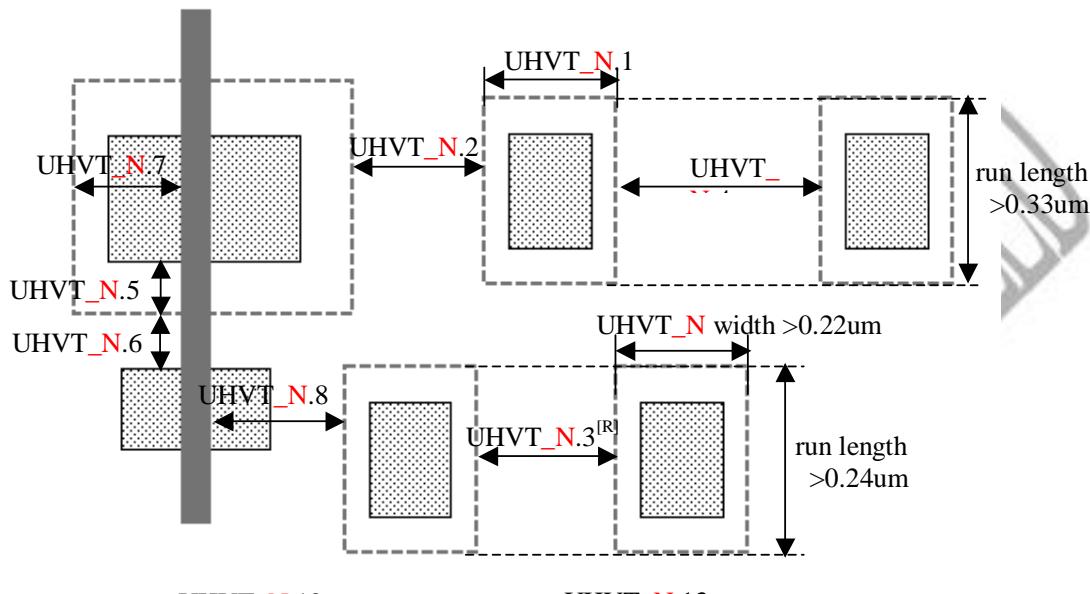
A drawn UHVT_N layer is needed to define ultra high Vt NMOS devices. UHVT_N is for Ncore ultra high Vt devices only.

Rule number	Description	Operatio n	Design Value	Unit
UHVT_N.1	UHVT_N width. Single-point-interaction is allowed. DRC doesn't highlight the violation when UHVT_N opposite side width \geq 0.135um, and $<$ 0.16um.	\geq	0.16	um
UHVT_N.2	Space between UHVT_N s. DRC doesn't highlight the violation when UHVT_N opposite side width \geq 0.135um, and $<$ 0.16um.	\geq	0.16	um
UHVT_N.3 ^[R]	Space between UHVT_N s with parallel run length $>$ 0.24um, when one UHVT_N width $>$ 0.22um.	\geq	0.18	um
UHVT_N.4	Space between UHVT_N s with parallel run length $>$ 0.33um, and UHVT_N space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
UHVT_N.5	UHVT_N extension outside of GATE along GATE poly direction.	\geq	0.065	um
UHVT_N.6	Space between UHVT_N and GATE along GATE poly direction.	\geq	0.065	um
UHVT_N.7	UHVT_N extension outside of GATE along source/drain direction.	\geq	0.115	um
UHVT_N.8	Space between UHVT_N and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT UHVT_N) is not allowed.	\geq	0.115	um
UHVT_N.9	Space between UHVT_N and non-silicided AA/H-R resistor	\geq	0.15	um
UHVT_N.10	45-degree edge length	\geq	0.52	um
UHVT_N.11	UHVT_N overlap HVT_N, ULVT_N, LVT_N, LVT_P, HVT_P, ULVT_P, UHVT_P, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA, LOGO is prohibited.			
UHVT_N.12	UHVT_N area	\geq	0.1	um ²

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UHVT_N.13	UHVT_N enclosed area	\geq	0.1	μm^2
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AA GT UHVT_N

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7.2.9.2 UHVT_P : Ultra high Vt PMOS design rules

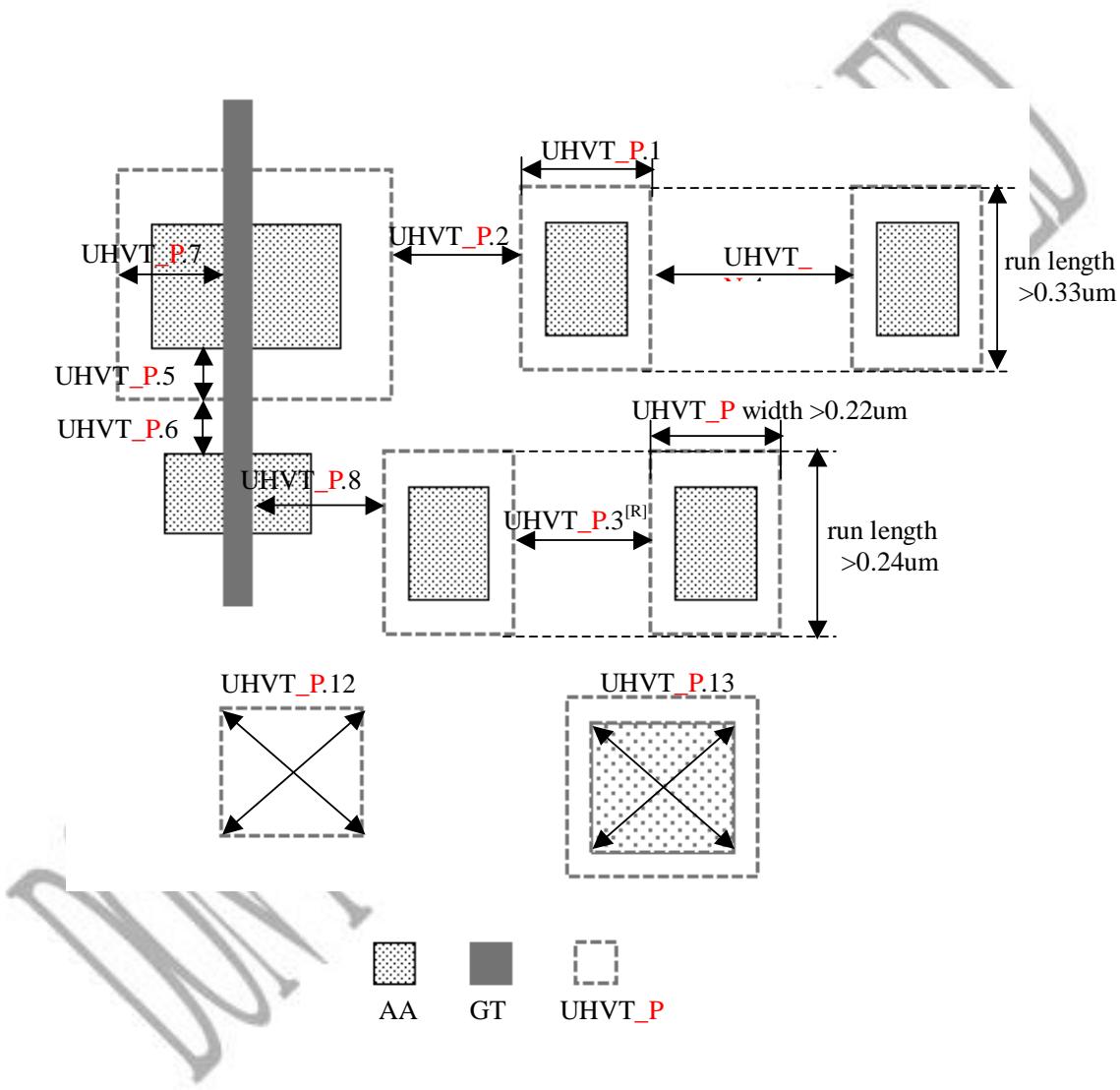
A drawn UHVT_P layer is needed to define ultra high Vt PMOS devices. UHVT_P is for Pcore ultra high Vt devices only.

Rule number	Description	Operatio n	Design Value	Unit
UHVT_P.1	UHVT_P width. Single-point-interaction is allowed. DRC doesn't highlight the violation when UHVT_P opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
UHVT_P.2	Space between UHVT_Ps. DRC doesn't highlight the violation when UHVT_P opposite side width $\geq 0.135\text{um}$, and $<0.16\text{um}$.	\geq	0.16	um
UHVT_P.3 ^[R]	Space between UHVT_Ps with parallel run length $>0.24\text{um}$, when one UHVT_P width $>0.22\text{um}$.	\geq	0.18	um
UHVT_P.4	Space between UHVT_Ps with parallel run length $>0.33\text{um}$, and UHVT_P space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
UHVT_P.5	UHVT_P extension outside of GATE along GATE poly direction.	\geq	0.065	um
UHVT_P.6	Space between UHVT_P and GATE along GATE poly direction.	\geq	0.065	um
UHVT_P.7	UHVT_P extension outside of GATE along source/drain direction.	\geq	0.115	um
UHVT_P.8	Space between UHVT_P and GATE along source/drain direction. (((N+AA OR P+AA) OR GATE) CUT UHVT_P) is not allowed.	\geq	0.115	um
UHVT_P.9	Space between UHVT_P and non-silicided AA/H-R resistor	\geq	0.15	um
UHVT_P.10	45-degree edge length	\geq	0.52	um
UHVT_P.11	UHVT_P overlap HVT_N, ULVT_N, LVT_N, UHVT_N, LVT_P, HVT_P, ULVT_P, PSUB, DG, TG, INST, RFSRAM, RESAA, RESNW, RESP2, VARMOS, BIPOLA, LOGO is prohibited.			
UHVT_P.12	UHVT_P area	\geq	0.1	um ²

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Rule number	Description	Operatio n	Design Value	Unit
UHVT_P.13	UHVT_P enclosed area	\geq	0.1	μm^2



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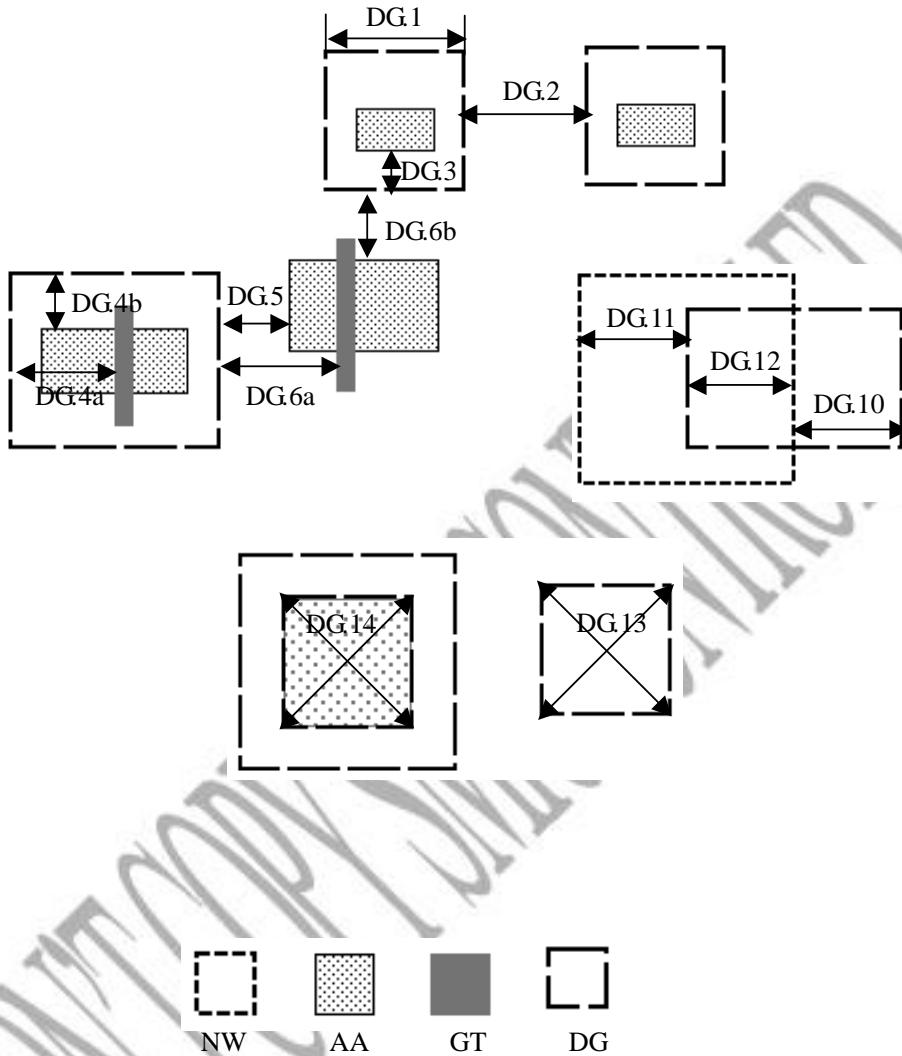
Doc. No:	Doc. Title:	28nm Logic HKMG 0.9V/1.8V/2.5V Design Rules	Doc. Rev: 2R	Tech Dev Rev: 1.0	Page No.: 90/90
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7.2.10 DG: Dual GATE design rules to define 1.8V IO device

Rule number	Description	Operation	Design Value	Unit
DG.1	DG width	\geq	0.32	um
DG.2	Space between two DGs.	\geq	0.32	um
DG.3	DG enclosure of AA. Pick-up AAs do not need to follow this rule.	\geq	0.13	um
DG.4a	DG enclosure of GATE along S/D direction.	\geq	0.24	um
DG.4b	DG enclosure of GATE along poly length direction.	\geq	0.13	um
DG.5	Space between DG and AA (except pickup AA). It is not allowed that AA CUT DG (except pickup AA).	\geq	0.13	um
DG.6a	Space between DG and GATE along S/D direction.	\geq	0.24	um
DG.6b	Space between DG and GATE along poly direction.	\geq	0.13	um
DG.7	Space between DG and NW. Space= 0um is allowed.	\geq	0.24	um
DG.8	Space between (NW NOT DG) and (NW NOT DG)	\geq	0.24	um
DG.9	Space between (DG AND NW) and (DG AND NW)	\geq	0.24	um
DG.10	DG extension outside of NW. Extension = 0um is allowed.	\geq	0.24	um
DG.11	NW extension outside of DG. Extension = 0um is allowed.	\geq	0.24	um
DG.12	DG overlap of NW. Overlap= 0um is allowed.	\geq	0.24	um
DG.13	DG area	\geq	0.4	um ²
DG.14	DG enclosed area	\geq	0.4	um ²
DG.15	DG and TG can't be used on same chip.			

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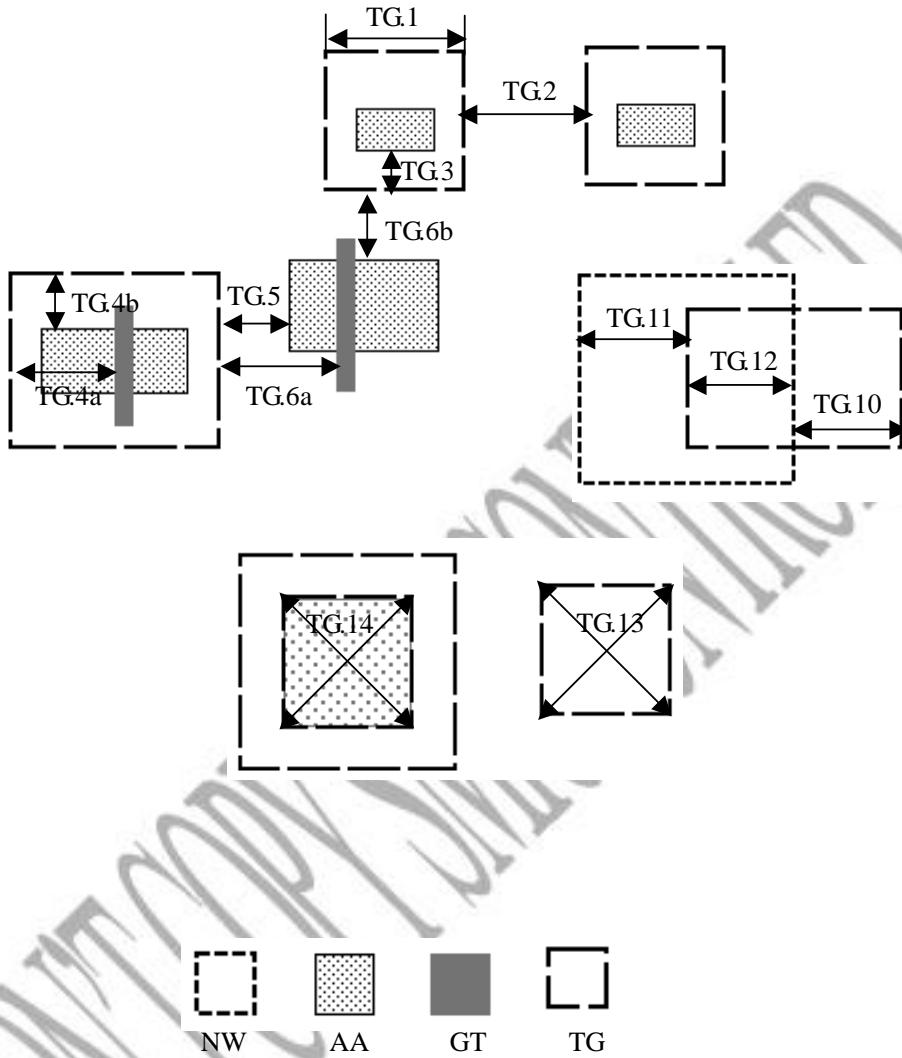
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7.2.11 TG: Dual GATE design rules to define 2.5V IO device

Rule number	Description	Operation	Design Value	Unit
TG1	TG width	\geq	0.32	um
TG2	Space between two TGs.	\geq	0.32	um
TG3	TG enclosure of AA. Pick-up AAs do not need to follow this rule.	\geq	0.13	um
TG4a	TG enclosure of GATE along S/D direction.	\geq	0.24	um
TG4b	TG enclosure of GATE along poly length direction.	\geq	0.13	um
TG5	Space between TG and AA (except pickup AA). It is not allowed that AA CUT TG (except pickup AA).	\geq	0.13	um
TG6a	Space between TG and GATE along S/D direction.	\geq	0.24	um
TG6b	Space between TG and GATE along poly direction.	\geq	0.13	um
TG7	Space between TG and NW. Space = 0um is allowed.	\geq	0.24	um
TG8	Space between (NW NOT TG) and (NW NOT TG)	\geq	0.24	um
TG9	Space between (TG AND NW) and (TG AND NW)	\geq	0.24	um
TG10	TG extension outside of NW. Extension = 0um is allowed.	\geq	0.24	um
TG11	NW extension outside of TG. Extension = 0um is allowed.	\geq	0.24	um
TG12	TG overlap of NW. Overlap = 0um is allowed.	\geq	0.24	um
TG13	TG area	\geq	0.4	um ²
TG14	TG enclosed area	\geq	0.4	um ²

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7.2.12 GT: Poly design rules

Rule number	Description	Operation	Design Value	Unit
GT.1	Width	\geq	0.03	um
		\leq	2	um
GT.2	Width of vertical poly outside of DG/TG This rule isn't applicable for RESP2, ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , VARMOS, LDBK and PSUB region, and DRC skip to check 0.032um width poly design in 2PSRAM region.	=	0.03/0.035/0.04/0.05/0.06/0.08/0.09~1	um
GT.3	Width of poly in DG/TG This rule isn't applicable for the region ((poly INTERACT (DGUD OR DGV).	\geq	0.15	um
GT.4	Width of horizontal poly. DRC only check opposite side.	\geq	0.07	um
GT.5	(Purposely blank)			
GT.6	Channel Length for core NMOS /PMOS transistor. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , VARMOS, PSUB, LOGO, OCOVL , INST and RFSSRAM region.	=	0.03/0.035/0.04/0.05/0.06/0.08/0.09-1	um
GT.7a	Channel Length for 1.8V I/O NMOS/PMOS transistor. This rule isn't applicable for DGUD, DGV, ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY region.	\geq	0.15	um
	\leq	2	um	
GT.7b	Channel Length for 1.8V I/O NMOS/PMOS transistor (for 1.5V under drive). This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY region.	\geq	0.105	um
	\leq	2	um	
GT.7c	Channel Length for 1.8V I/O NMOS/PMOS transistor (for 1.2V vertical poly under drive). This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY region.	\geq	0.09	um
	\leq	2	um	
GT.7d	Channel Length for 1.8V I/O NMOS/PMOS	\geq	0.1	um

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Rule number	Description	Operation	Design Value	Unit
	transistor (for 1.2V horizontal poly under drive). This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\leq	2	um
GT.8a	Channel Length for 2.5V I/O NMOS/PMOS transistor. This rule isn't applicable for TGV, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.27	um
		\leq	2	um
GT.8b	Channel Length for 2.5V I/O NMOS/PMOS transistor (for 1.8V under drive). This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.25	um
		\leq	2	um
GT.8c	Channel Length for 2.5V I/O NMOS transistor (for 3.3V over drive). This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.55	um
		\leq	2	um
GT.8d	Channel Length for 2.5V I/O PMOS transistor (for 3.3V over drive). This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.44	um
		\leq	2	um
GT.9a	Width of 1st poly (or POLY_DMY) neighboring GATE (channel length = 0.03um) for core NMOS/PMOS. 1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE <0.23um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, INST and RFSRAM region.	=	0.03	um
GT.9b	Width of 1st poly (or POLY_DMY) neighboring GATE (channel length = 0.035um/0.040um) for core NMOS/PMOS. 1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE <0.23um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, INST and RFSRAM region.	=	0.03/0.035/0.04/0.05	um

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Rule number	Description	Operation	Design Value	Unit
GT.9c	<p>Width of 1st poly (or POLY_DMY) neighboring GATE (channel length $\geq 0.05\text{um}$ and $\leq 0.09\text{ um}$) for core NMOS/PMOS.</p> <p>1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE $< 0.23\text{um}$.</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMDY, VARMOS, FUSEMK1, INST and RFSRAM region.</p>	=	0.04~0.09	um
GT.9d	<p>Width of 1st poly (or POLY_DMY) neighboring GATE (channel length $> 0.09\text{ um}$) for core NMOS/PMOS.</p> <p>1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE $< 0.23\text{um}$.</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMDY, FUSEMK1, VARMOS, INST and RFSRAM region.</p>	\geq	0.04	um
GT.10 ^[R]	<p>Width of 1st POLY_DMY neighboring GATE for I/O NMOS/PMOS.</p> <p>1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE $< 0.51\text{um}$.</p> <p>This rule doesn't check the neighboring GATE in ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMDY region.</p>	\geq	0.1	um
GT.11	<p>Width of 2nd poly (or POLY_DMY) neighboring GATE (channel length is $0.03\text{um}/0.035\text{um}/0.040\text{um}$) for core NMOS/PMOS, when 2nd poly (or POLY_DMY) to neighboring GATE space $= 0.23\text{um} \sim 0.28\text{um}$.</p> <p>The violation is allowed when the violation parallel length is $\leq 10\%$ of neighboring GATE width.</p> <p>2nd poly (or POLY_DMY) neighboring GATE is must to be drawn for channel length 0.03um, 0.035um, 0.040um core NMOS and PMOS.</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMDY, INST and</p>	=	0.03~0.12	um

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Rule number	Description	Operation	Design Value	Unit
	RFSRAM region.			
GT.12	Space. DRC doesn't check INDMDY region.	\geq	0.08	um
GT.13	Space between (poly inside DG/TG) and poly	\geq	0.18	um
GT.14a	Space between poly and (poly or POLY_DMY) if at least one (poly or POLY_DMY) width \geq 0.03um, and \leq 0.09um, and the parallel run length $>$ 0.09um.	\geq	0.1	um
GT.14b	Space between poly and (poly or POLY_DMY) if at least one (poly or POLY_DMY) width $>$ 0.09um, and the parallel run length $>$ 0.09um. DRC doesn't check OCCD, INST and RFSRAM region.	\geq	0.12	um
GT.15	At least one side space between vertical (poly or POLY_DMY), when 1. Width of (poly or POLY_DMY) W1 $<$ 0.04um; 2. Width of two neighboring (poly or POLY_DMY) W2 \geq 0.06um; 3. The parallel run length $>$ 0.07um.	\geq	0.12	um
GT.16 ^[R]	Space between (poly or POLY_DMY) in DUMBP region. DRC check maximum (NOT (poly or POLY_DMY)) width in DUMBP. DRC doesn't check OCOVL region.	\leq	3	um
GT.17 ^[R]	Space between (poly or POLY_DMY). DRC check the maximum (NOT (poly or POLY_DMY)) width. DRC doesn't check 1. DSTR, OCOVL and BIPOLA region. 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	\leq	3	um
GT.18a	Space between ((GATE sizing up 0.06um) AND poly) (channel length \leq 0.09um) and neighboring (poly or POLY_DMY) for core NMOS/PMOS. Poly (or POLY_DMY) is must when the space	$=$	0.1	um

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Rule number	Description	Operation	Design Value	Unit
	between poly (or POLY_DMY) and neighboring GATE <0.23um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , FUSEMK1, VARMOS, FUSEMK1, INST and RFSRAM region.			
GT.18b	Space between ((GATE sizing up 0.06um) AND poly) (channel length > 0.09um) and neighboring (poly or POLY_DMY) for core NMOS/PMOS. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , FUSEMK1, VARMOS, INST and RFSRAM region.	=	0.12	um
GT.18c	Space between ((GATE sizing up 0.06um) AND poly) and neighboring (poly or POLY_DMY) for core device in ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY region. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.23um.	\geq	0.12	um
GT.19	Space between ((GATE sizing up 0.06um) AND poly) and neighboring (poly or POLY_DMY) for I/O NMOS/PMOS. Poly (or POLY_DMY) is must when the space between poly (or POLY_DMY) and neighboring GATE <0.51um. This rule isn't applicable for GATE in ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , LDBK and VARMOS region.	=	0.18	um
GT.20	Space between 1st (poly or POLY_DMY) neighboring GATE (channel length = $\sum_{i=1}^n \sum_{j=1}^{m_i} \sum_{k=1}^{n_j} \sum_{l=1}^{m_k} \sum_{p=1}^{n_l} \sum_{q=1}^{m_p}$)	\geq	0.1	um

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Rule number	Description	Operation	Design Value	Unit
	<p>0.03um/0.035um/0.040um) and 2nd (poly or POLY_DMY) for core NMOS/PMOS.</p> <p>2nd (poly or POLY_DMY) is must when the space between 2nd poly (or POLY_DMY) and neighboring GATE =0.23um~0.28um.</p> <p>The violation is allowed when the violation parallel length is \leq10% of neighboring GATE width.</p> <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, INST and RFSRAM region.</p>	\leq	0.15	um
GT.21	(Purposely blank)			
GT.22	(Purposely blank)			
GT.23	Space between AA and poly (or POLY_DMY) on STI.	\geq	0.025	um
GT.24a	Space between (((poly or POLY_DMY) NOT P2) INTERACT AA) and (((AA or AA_DMY) NOT INTERACT poly)) INTERACT CT), when width of (AA or AA_DMY) <0.07um, and the parallel run length > 0.09um	\geq	0.05	um
GT.24b	<p>Space between (poly or POLY_DMY) and (AA or AA_DMY), when width of (AA or AA_DMY) <0.07um and the parallel run length >0um and \leq 0.09um.</p> <p>DRC doesn't check INST and RFSRAM region.</p>	\geq	0.05	um
GT.24c	<p>Space between (poly or POLY_DMY) and AA, when</p> <ol style="list-style-type: none"> 1. Space between two (poly or POLY_DMY) > 0.27um; 2. The parallel run length of (poly or POLY_DMY) and AA > 0.09um. <p>This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.</p>	\geq	0.035	um
GT.24d	<p>Space between poly and (AA or AA_DMY), when</p> <ol style="list-style-type: none"> 1. Space between poly and (poly or POLY_DMY) > 0.27um; 2. The parallel run length of polys and (AA or 	\geq	0.035	um

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Rule number	Description	Operation	Design Value	Unit
	AA_DMY) > 0.09um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.			
GT.24e	Space between (AA INTERACT CT) and ((poly NOT P2) INTERCACT CT), when 1.AA width \geq 0.07um and <0.1um excluding L-shap AA with AA width =0.07um; 2.(Poly NOT P2) extension CT <0.08um; 3. AA and poly are at different net DRC doesn't check INST and RFSRAM region.	\geq	0.04	um
GT.25	Space between AA and L-shape or U-shape poly on the same MOS in IO device, when L-shape or U-shape poly length (L) \leq 0.08um.	\geq	0.25	um
GT.26	Space between poly end to L-shape poly line (NOT P2) in vertical direction.	\geq	0.18	um
GT.27	Space between (poly or POLY_DMY) and ((poly or POLY_DMY) AND SAB)	\geq	0.16	um
GT.28a	Space between (poly NOT P2) and ((AA INTERACT CT) NOT INSIDE (DG OR TG)), which poly connects to (1.5V and 1.8V) net. DRC check follows metal voltage marking layer for (1.5V and 1.8V) net.	\geq	0.065	um
GT.28b	Space between two (((poly NOT P2) INTERACT CT) NOT INSIDE (DG OR TG)), and either (poly NOT P2) connects to (1.5V and 1.8V) net. DRC check follows metal voltage marking layer for (1.5V and 1.8V) net.	\geq	0.17	um
GT.29a	Extension of AA outside of (poly or POLY_DMY) for core device with channel length \leq 0.09um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, INST and RFSRAM region.	=	0.075	um
GT.29a ^[R]	Extension of AA outside of (poly INTERACT CT) for core device with channel length \leq 0.09um. This rule isn't applicable for PSUB, VARMOS, ESDIO2, ESDCLP, ESDPOB, CLPDMY, EFUSE	\geq	0.205	um

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Rule number	Description	Operation	Design Value	Unit
	region.			
GT.29b	Extension of AA outside of (poly or POLY_DMY) for core device with channel length > 0.09um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , VARMOS region.	=	0.095	um
GT.29c	Extension of AA outside of (poly or POLY_DMY) for core device in ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY region.	\geq	0.095	um
GT.30a	Extension of AA outside of (poly or POLY_DMY) for I/O device in ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY .	\geq	0.155	um
GT.30b	Extension of AA outside of (poly or POLY_DMY) for I/O device region. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , VARMOS, LDBK region.	=	0.155	um
GT.31	Extension of poly outside of AA This rule isn't applicable for INDMY, LDBK, LOGO , INST and RFSRAM region.	\geq	0.08	um
GT.32	(Purposely blank)			
GT.33	Extension of poly outside of AA when the poly to L-shape AA (in same MOS) space <0.1um.	\geq	0.095	um
GT.34	((Poly or POLY_DMY) NOT P2) density in full chip	\geq	15%	
		\leq	40%	
GT.35	((Poly or POLY_DMY) NOT P2) density. Density check window: Window size: 10um*10um, step size: 5um. For low density , DRC don't check : 1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. Seal ring (MARKS) sizing up 0.4um if seal ring	\geq	10%	

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Rule number	Description	Operation	Design Value	Unit
	is added by customer. 3. MOMDMY, BIPOLA, RESAA, LOGO, (DSTR AND AA), (INDMY sizing up 2um) region For high density, DRC doesn't check H-R resistor region: ((poly AND RESP2) INTERACT SAB).	\leq	65%	
GT.35 ^[R]	((Poly or POLY_DMY) NOT P2) density. Density check window: Window size: 10um*10um, step size: 5um. For low density , DRC don't check : 1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer. 3. MOMDMY, BIPOLA, RESAA, LOGO, (DSTR AND AA), (INDMY sizing up 2um) region For high density, DRC doesn't check H-R resistor region: ((poly AND RESP2) INTERACT SAB).	\geq	15%	
		\leq	55%	
GT.36	((Poly or POLY_DMY) NOT P2) density. Density check window: Window size: 20um*20um, step size: 10um. For low density , DRC don't check : 1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer. For high density, DRC doesn't check H-R resistor region: ((poly AND RESP2) INTERACT SAB).	\geq	10%	
		\leq	65%	
GT.36 ^[R]	((Poly or POLY_DMY) NOT P2) density. Density check window: Window size: 20um*20um, step size: 10um. For low density , DRC don't check : 1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer. For high density, DRC doesn't check H-R resistor region: ((poly AND RESP2) INTERACT SAB).	\geq	15%	
		\leq	55%	

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Rule number	Description	Operation	Design Value	Unit
GT.37 ^[R]	((Poly or POLY_DMY) NOT P2)) density inside of the dummy block area(DUMBP).Density check window size: 10um*10um, step size: 5um DRC need check the design if DUMBP width is >3um and <10um, where density ratio= ((poly or POLY_DMY) NOT P2) area/DUMBP area. DRC doesn't check OCOVL region.	≥	10%	
GT.38	(Purposely blank)			
GT.39	(Purposely blank)			
GT.40	Rectangular poly length	≥	0.26	um
GT.41	((Poly or POLY_DMY) NOT P2)) length when (poly or POLY_DMY) width <0.05um. It's recommended to restrict poly length as short as possible.	≤	180	um
GT.42a	(Poly NOT P2) length between two CTs (the two CTs on same poly), when poly width <0.06um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMDY , RESP2 and (poly INTERACT MOMDMY) region.	≤	18	um
GT.42b	The length from the any point inside GATE to (the nearest CT on GATE poly) (without P2 between GATE and CT), when poly width <0.06um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMDY and (poly INTERACT MOMDMY) region.	≤	18	um
GT.43	Poly area. This check doesn't check rectangle (poly INTERACT AA) with length ≥0.32 um	≥	0.0115	um ²
GT.44	Maximum ((poly or POLY_DMY) NOT P2) area. This rule doesn't check the area below: 1) H-R resistor region (((poly or POLY_DMY) AND RESP2) INTERACT SAB), BIPOLA and (GTDMP AND RESAA); 2) All (poly or POLY_DMY) width ≤0.2um in check window and density ≤ 50%, density check	≤	3	um ²

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Rule number	Description	Operation	Design Value	Unit
	window is 10um*10um, stepping is 5um.			
GT.44 ^[R]	Maximum ((poly or POLY_DMY) NOT P2) area. This rule doesn't check the area below: 1) H-R resistor region (((poly or POLY_DMY) AND RESP2) INTERACT SAB), BIPOLA and (GTDMP AND RESAA); 2) All (poly or POLY_DMY) width \leq 0.2um in check window and density \leq 50%, density check window is 10um*10um, stepping is 5um.	\leq	2	um ²
GT.45	Only axes of poly geometry at 0-degree (X), 90-degree (Y) are allowed, 45-degree poly is not allowed. DRC doesn't check NODMF, INDMY and LOGO region			
GT.46	O-shape poly is not allowed. DRC doesn't check INST and RFSRAM region.			
GT.47 ^[NC]	Poly line-end must be rectangular.			
GT.48	((Poly NOT P2) NOT INSIDE (DG OR TG) must be rectangle or L-shape. DRC doesn't check FUSEMK1, NODMF, LOGO, INST and RFSRAM region.			
GT.49	(((Poly NOT P2) OUTSIDE (DG OR TG)) INTERACT AA) must be rectangle. DRC doesn't check FUSEMK1, INST and RFSRAM region.			
GT.50	Floating ((poly NOT P2) NOT INTERACT CT) must be a rectangle DRC doesn't check 1) The poly with width \geq 0.15um 2) INST, LOGO and RFSRAM region.			
GT.51	GATE of core device must be in vertical direction. DRC doesn't check VARMOS, LOGO, NODMF region.			
GT.52	In core device region, rectangle (poly NOT			

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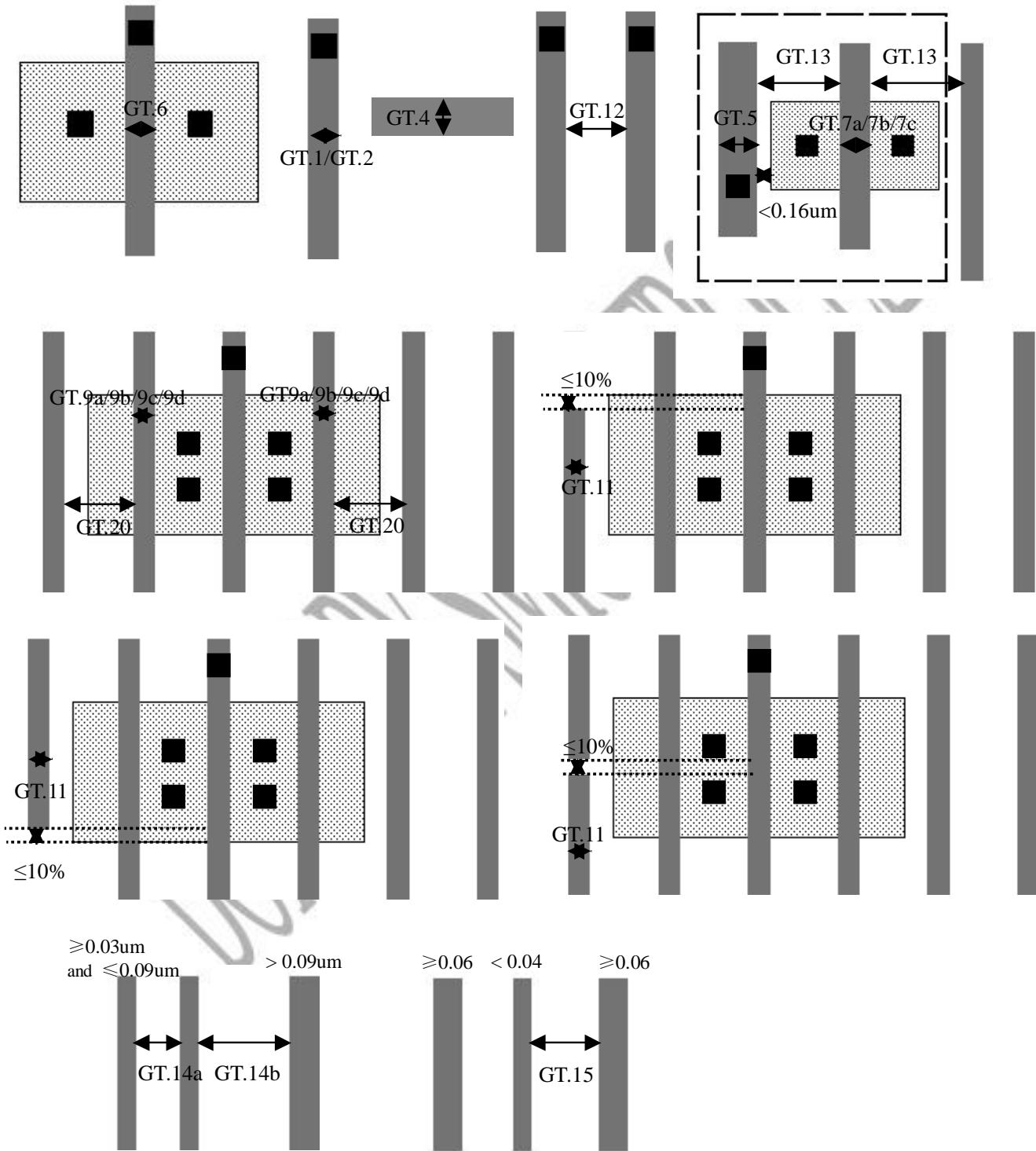


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Rule number	Description	Operation	Design Value	Unit
	INTERACT AA) must be vertical, which is same as GATE poly direction. This rule doesn't check BIPOLA, DSTR, LOGO, ((poly INTERACT RESP2) INTERACT SAB), (((poly INTERACT RESP2) NOT INTERACT SAB) with poly width $\geq 0.15\mu m$), also doesn't check square pattern.			
GT.53	(Poly or POLY_DMY) width on same AA must be same for core device region with channel length $< 0.15\mu m$. DRC doesn't check ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY, INST and RFSRAM region.			
GT.54	Poly interacting AA must separate at least two AA diffusions. DRC doesn't check LDBK, INDMY, LOGO, OCOVL, (poly INTERACT INST) and RFSRAM region.			
GT.55	(Purposely blank)			
GT.56	Floating GATE is prohibited (except dummy pattern). Definition of floating GATE: ((poly INTERACT AA) NOT INTERACT CT). DRC doesn't check OCCD, INST and RFSRAM region, skip to check when source/drain is connected to different (MOS AA NOT poly), or different pickup AA, different GATE, or different ALPA pad.			
GT.57	((((poly OR GTDMP) OR GTDOP) NOT P2) NOT INSIDE (DG OR TG)) can't apply the voltage $> 2.5V$.			

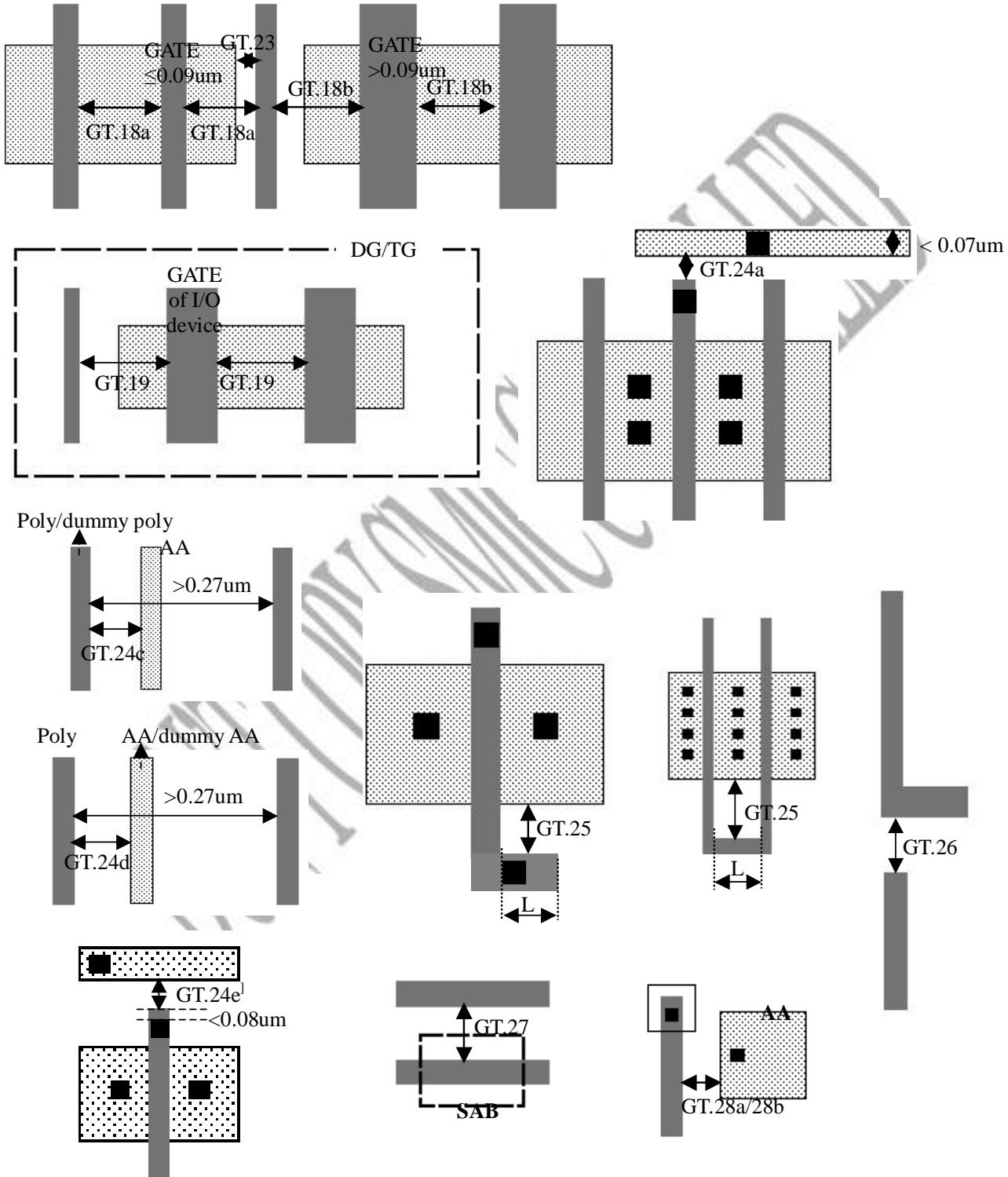
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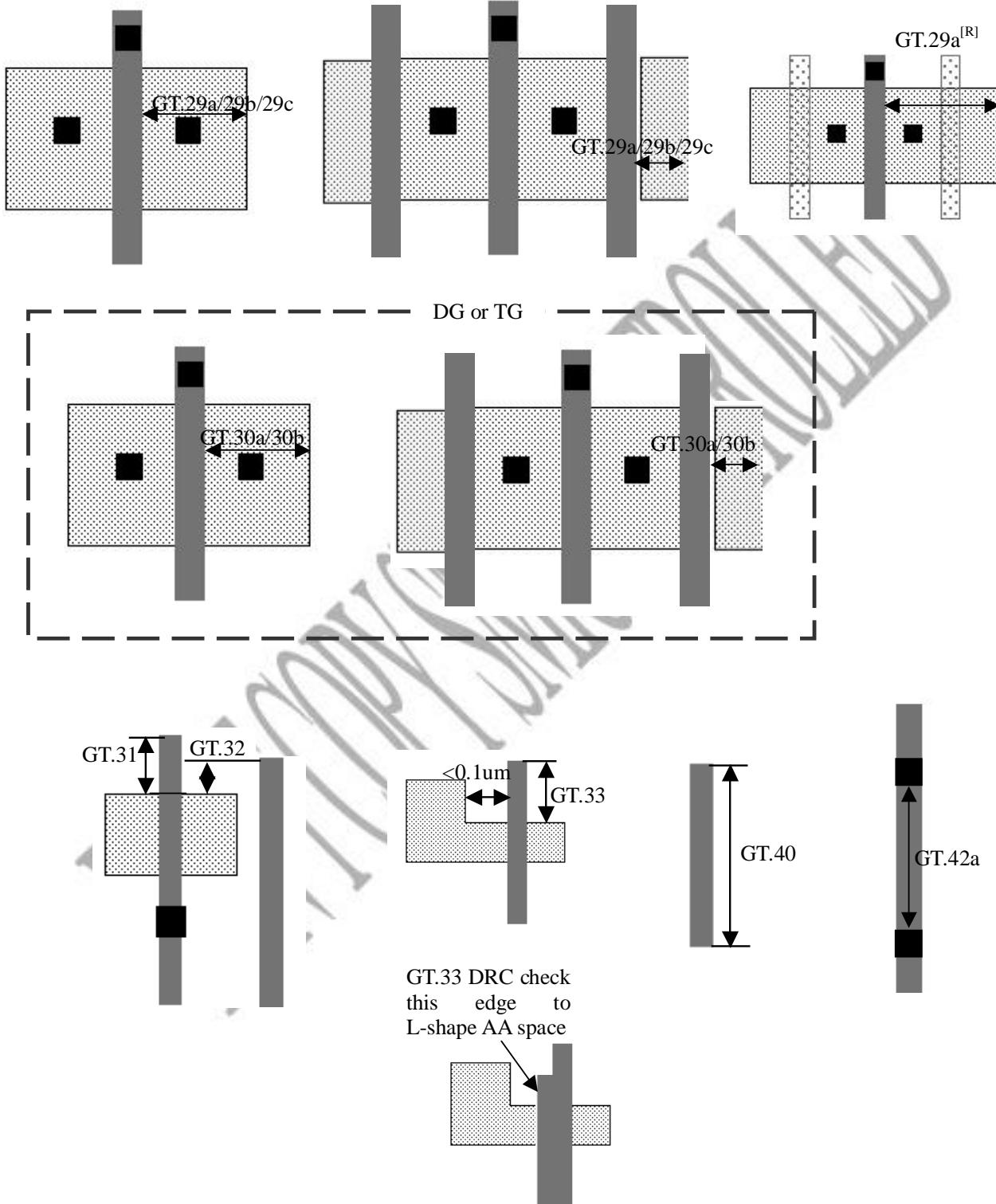
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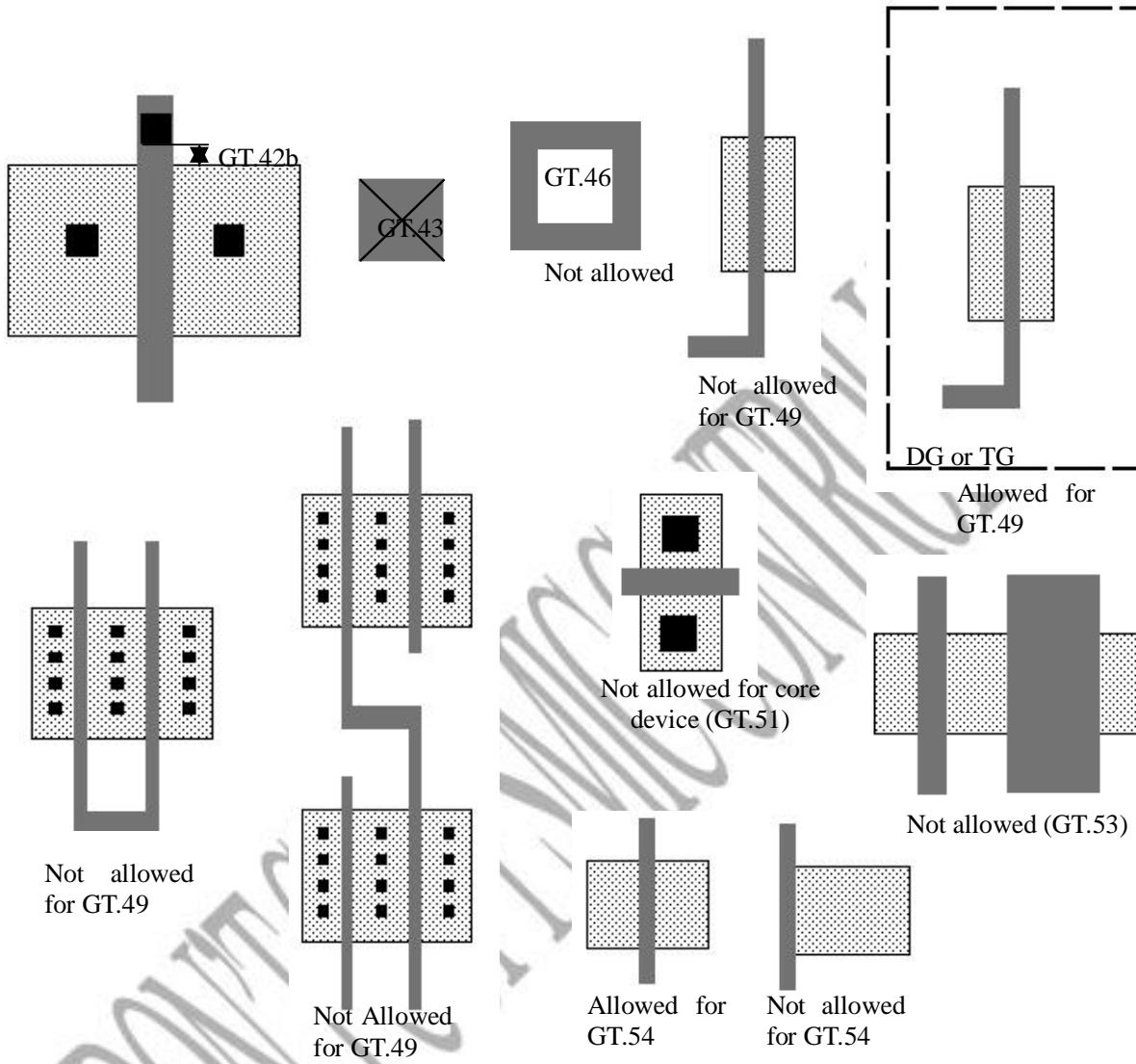
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7.2.13 GTDMP: GT Dummy rules

Rule number	Description	Operation	Design Value	Unit
GTDMP.1	Width	\geq	0.03	um
		\leq	2	um
GTDMP.2	Width of (GTDMP NOT INTERACT AA) outside of (DG OR TG))	\geq	0.03	um
GTDMP.3	Width inside DG/TG DRC doesn't check DGV region.	\geq	0.1	um
GTDMP.4	Width of GTDMP (GTDMP NOT INTERACT AA) in IO ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMDY regions	=	0.1	um
GTDMP.5	Width of horizontal (GTDMP NOT OUTSIDE (DG OR TG))	\geq	0.1	um
GTDMP.6a	Width of (GTDMP INTERACT AA) inside 1.8V IO region along source/drain direction. DRC doesn't check DGUD region.	\geq	0.15	um
GTDMP.6b	Width of (GTDMP INTERACT AA) inside 1.8V underdrive to 1.5V IO region along source/drain direction	\geq	0.105	um
GTDMP.6c	Width of GTDMP not outside 1.8V underdrive to 1.2V IO region	\geq	0.09	um
GTDMP.6d	Width of horizontal GTDMP not outside 1.8V underdrive to 1.2V IO region	\geq	0.1	um
GTDMP.7a	Width of (GTDMP INTERACT AA) inside 2.5V IO region along source/drain direction. DRC doesn't check TGV, OVERDR region.	\geq	0.27	um
GTDMP.7b	Width of (GTDMP INTERACT AA} inside 2.5V underdrive to 1.8V IO region along source/drain direction	\geq	0.24	um
GTDMP.7c	Width of (GTDMP INTERACT AA} inside 2.5V overdrive to 3.3V IO region along source/drain direction	\geq	0.27	um
GTDMP.8	Space between two GTDMPS if at least one GTDMP width $\geq 0.03\text{um}$, and $\leq 0.09\text{um}$, and the parallel run length $> 0.08\text{um}$	\geq	0.1	um
GTDMP.9	Space between two GTDMPS if at least one GTDMP width $> 0.09\text{um}$, and the GTDMP parallel run length $>$	\geq	0.12	um

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Rule number	Description	Operation	Design Value	Unit
	0.08um			
GTDMP.10	Space between GTDMP and ((poly or GTDMP) or GTDOP). It's not allowed GTDMP interact poly outside P2.	\geq	0.08	um
GTDMP.11	Space between GTDMP (GTDMP INTERACT AA) and (neighboring poly or GTDMP) (width \leq 0.09um) for core device. DRC check the space between (neighboring poly or GTDMP) and (GTDMP INTERACT AA) $<$ 0.23um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY and VARMOS region.	=	0.1	um
GTDMP.12	Space between GTDMP (GTDMP INTERACT AA) and (neighbouring poly or GTDMP) (width $>$ 0.09um) for core device. DRC check the space between (neighboring poly or GTDMP) and (GTDMP INTERACT AA) $<$ 0.23um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY and VARMOS region.	=	0.12	um
GTDMP.13	Space between GTDMP (GTDMP INTERACT AA) and (neighbouring poly or GTDMP) for IO device. DRC check the space between (neighboring poly or GTDMP) and (GTDMP INTERACT AA) $<$ 0.51um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY and VARMOS region.	=	0.18	um
GTDMP.14	Space between two (GTDMP AND AA) inside DG/TG in the same AA	\geq	0.18	um
GTDMP.15	(Purposely blank)			
GTDMP.16	Space between GTDMP (GTDMP AND AA) and SAB ((GTDMP AND AA) and SAB overlap is not allowed). This rule isn't applicable for RESP2, ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.38	um
GTDMP.17	Space between (GTDMP AND AA) and CT for core device when GTDMP width \leq 0.09um. ((GTDMP AND AA) and CT overlap is not allowed)	\geq	0.03	um
GTDMP.18	Space between (GTDMP AND AA) and CT for core device	\geq	0.04	um

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Rule number	Description	Operation	Design Value	Unit
	when GTDMP width > 0.09um. ((GTDMP AND AA) and CT overlap is not allowed)			
GTDMP.19	Space between (GTDMP AND AA) and CT for IO device. ((GTDMP AND AA) and CT overlap is not allowed)	≥	0.07	um
GTDMP.20	GTDMP extension outside of AA	≥	0.08	um
GTDMP.21	GTDMP extension outside of AADMP	≥	0.08	um
GTDMP.22	AADMP extension outside of GTDMP	≥	0.075	um
GTDMP.23	Rectangular GTDMP length	≥	0.26	um
GTDMP.24	GTDMP area	≥	0.0115	um ²
GTDMP.25	(GTDMP AND GTDOP) density. DRC check region follow: (((AA OR poly) INTERACT GATE) sizing up 2um) NOT ((AA OR poly) sizing up 0.15um)) DRC doesn't check VARMOS, NODMF, INST, RFSRAM, DG, TG, OCOVL, OCCD region.	≥	7%	
GTDMP.26	GTDMP (NOT P2) must be rectangular. DRC doesn't check OCCD region.			
GTDMP.27^[NC]	GTDMP line-end must be rectangular.			
GTDMP.28	GTDMP interacting AA must separate at least two AA diffusions. DRC doesn't check MOMDMY region.			
GTDMP.29	(GTDMP AND AA) of core device must be vertical direction. This rule isn't applicable for the regions covered by BIPOLA, DSTR, NODMF and LOGO.			
GTDMP.30	In core device region, rectangle (GTDMP NOT INTERACT AA) must be vertical, which is same as GATE poly direction. This rule doesn't check NODMF, BIPOLA, DSTR, LOGO, RESAA, OCCD, ((GTDMP INTERACT RESP2) INTERACT SAB) and square pattern.			
GTDMP.31^[NC]	GTDMP (30;8) can't form device.			
GTDMP.32^[R]	CT is not allowed to land on GTDMP			

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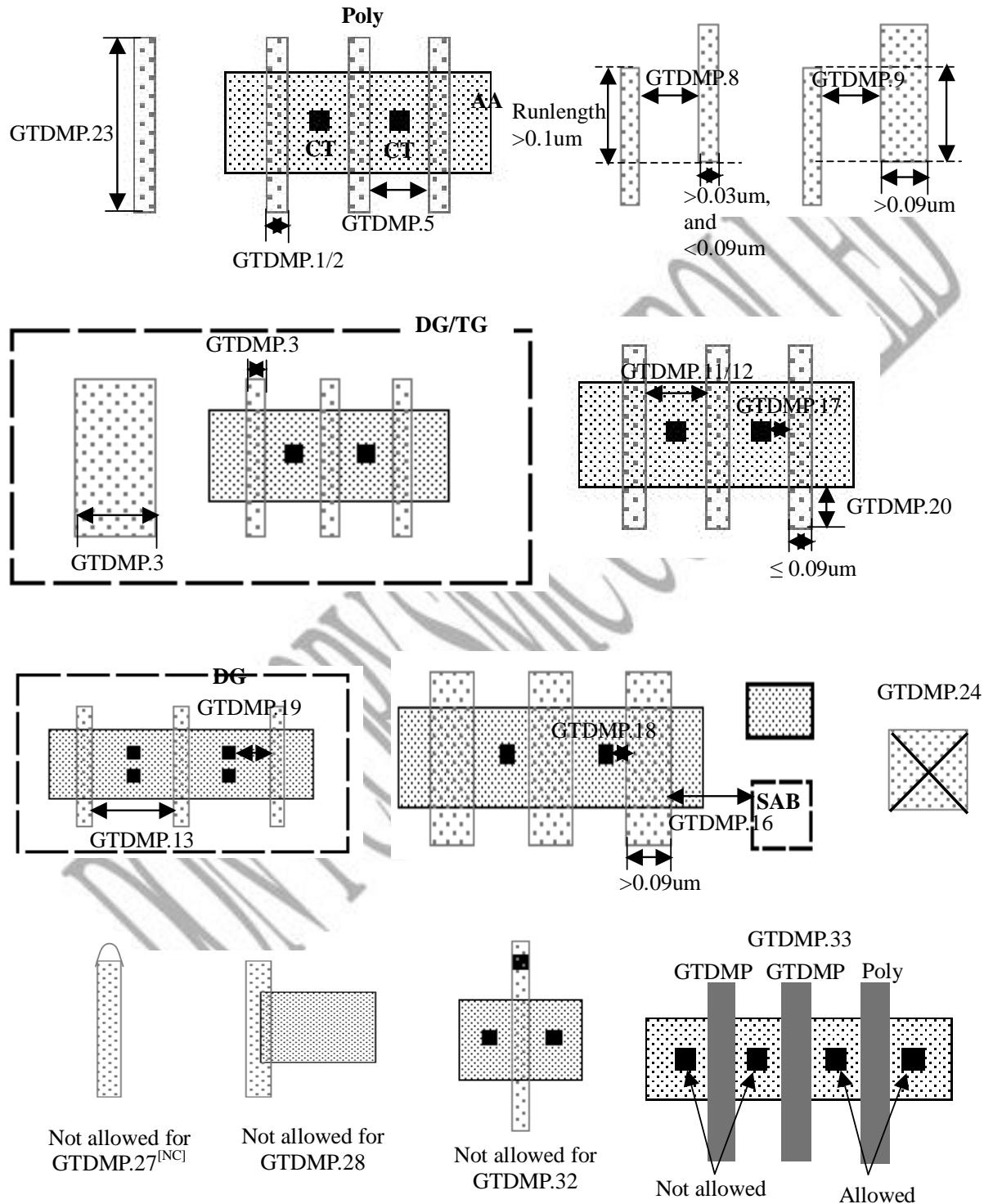
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Rule number	Description	Operation	Design Value	Unit
GTDMP.33	CT is not allowed to be placed between GTDMP and AA edge, or two GTDMPS.			

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7.2.14 GB: GT bias marking layer design rule

GBU15 or GBD20 are marking layers for core NMOS/PMOS GATE poly CD sizing.

GBU15 is GATE CD size up 1.5nm/side pre-shrink.

GBD20 is GATE CD size down 2nm/side pre-shrink.

Rule number	Description	Operation	Design Value	Unit
GB.1 ^[NC]	GBU15 is applied for ULVT, HVT, LVT, SVT device, can't apply for UHVT device.			
GB.2 ^[NC]	GBD20 is applied for all core device (ULVT, LVT, SVT, HVT, UHVT).			
GB.3a	Width of (((poly OR GTDMP) OR GTDOP) NOT P2) for core NMOS/PMOS transistor which covered by GBU15.	=	0.03/0.035	um
GB.3b	Width of (((poly OR GTDMP) OR GTDOP) NOT P2) for core NMOS/PMOS transistor which covered by GBD20.	=	0.035	um
GB.4	Space between (GBU15 or GBD20) and (AA INTERACT ((poly OR GTDMP) OR GTDOP)).	≥	0.06	um
GB.5	Space between (GBU15 OR GBD20) and GATE along gate poly direction.	≥	0.065	um
GB.6	(GBU15 OR GBD20) enclosure AA	≥	0.02	um
GB.7	(GBU15 OR GBD20) extension outside of GATE along gate poly direction.	≥	0.065	um
GB.8	(GBU15 or GBD20) must fully cover (poly NOT P2) along gate poly direction, when poly extension AA <0.12um.	≥	0.005	um
GB.9	It's not allowed (AA INTERACT poly) CUT (GBU15 or GBD20).			
GB.10	(GBU15 OR GBD20) must fully cover GATE, it's not allowed ((GBU15 or GBD20) NOT INTERACT GATE).			
GB.11	(GBU15 or GBD20) CUT (poly or GTDMP or GTDOP) along the core GATE poly direction is not allowed.			
GB.12	It's not allowed GBU15 interact with (UHVT_N AND GATE),(UHVT_P AND GATE),((DGOR TG) AND GATE) and ESDIO1/ESDIO2 /ESDCLP/ESDPOB/CLPDMY.			
GB.13	It's not allowed GBD20 interact with ((DG OR TG) AND GATE) and ESDIO1/ESDIO2/ESDCLP/ESDPOB/CLPDMY..			

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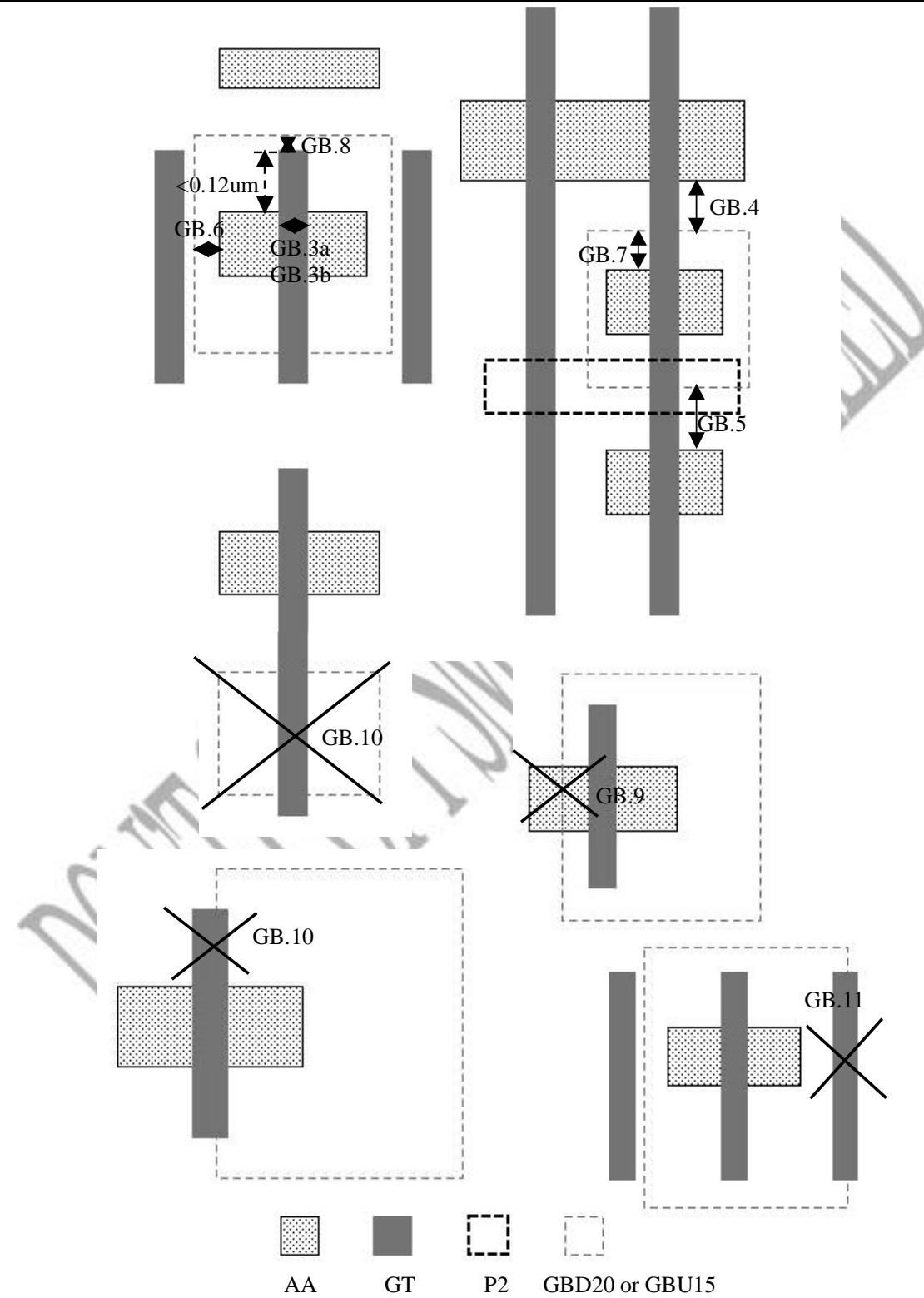


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Rule number	Description	Operation	Design Value	Unit
GB.14	It's not allowed GBU15 and GBD20 overlap each other.			
GB.15	GBU15 or GBD20 must be rectangular.			
GB.16	Width of 1st poly (or POLY_DMY) neighboring GATE (channel length = 0.035um) for core NMOS/PMOS, where the neighboring GATE is inside of GBD20. 1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE <0.23um. This rule isn't applicable for ESDIO1, ESDIO2 region.	=	0.03/0.035/0.04	

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7.2.15 P2: Poly cut design rules

Rule number	Description	Operation	Rule value	Unit
P2.1	P2 width. DRC doesn't check INST and RFSRAM region.	=	0.08	um
P2.2	P2 length. DRC doesn't check INST and RFSRAM region.	≥	0.15	um
P2.3	Poly width which the poly is cut by P2. DRC only check (P2 overlap poly) region.	≤	0.1	um
P2.4	Space between P2 and P2	≥	0.09	um
P2.5	Space between P2 and ((poly OR GTDMP) OR GTDOP) in P2 length direction	≥	0.04	um
P2.6	Space between P2 and ((poly OR GTDMP) OR GTDOP) excluding P2 length direction.	≥	0.02	um
P2.7	Space between P2 and AA (overlap is not allowed). DRC doesn't check INST and RFSRAM region.	≥	0.035	um
P2.8	Space between P2 and GATE in P2 width direction when space between poly and L-shape AA in the same MOS < 0.1um (overlap is not allowed). DRC doesn't check INST and RFSRAM region.	≥	0.05	um
P2.9	Space between P2 and CT (overlap is not allowed). DRC doesn't check INST and RFSRAM region.	≥	0.02	um
P2.10	P2 extension outside of ((poly OR GTDMP) OR GTDOP) in P2 length direction	≥	0.05	um
P2.11	P2 extension outside of ((poly OR GTDMP) OR GTDOP) in P2 width direction. DRC doesn't check INST and RFSRAM region.	=	0.03/0.035	um
P2.12	((Poly OR GTDMP) OR GTDOP) extension outside of P2	≥	0.1	um
P2.13	It's not allowed P2 overlap DG/TG/PSUB/AA/CT.			
P2.14	P2 must INTERACT ((poly OR GTDMP) OR GTDOP)			
P2.15	P2 must be in the horizontal direction which is perpendicular to the core GATE poly length direction in a same chip.			

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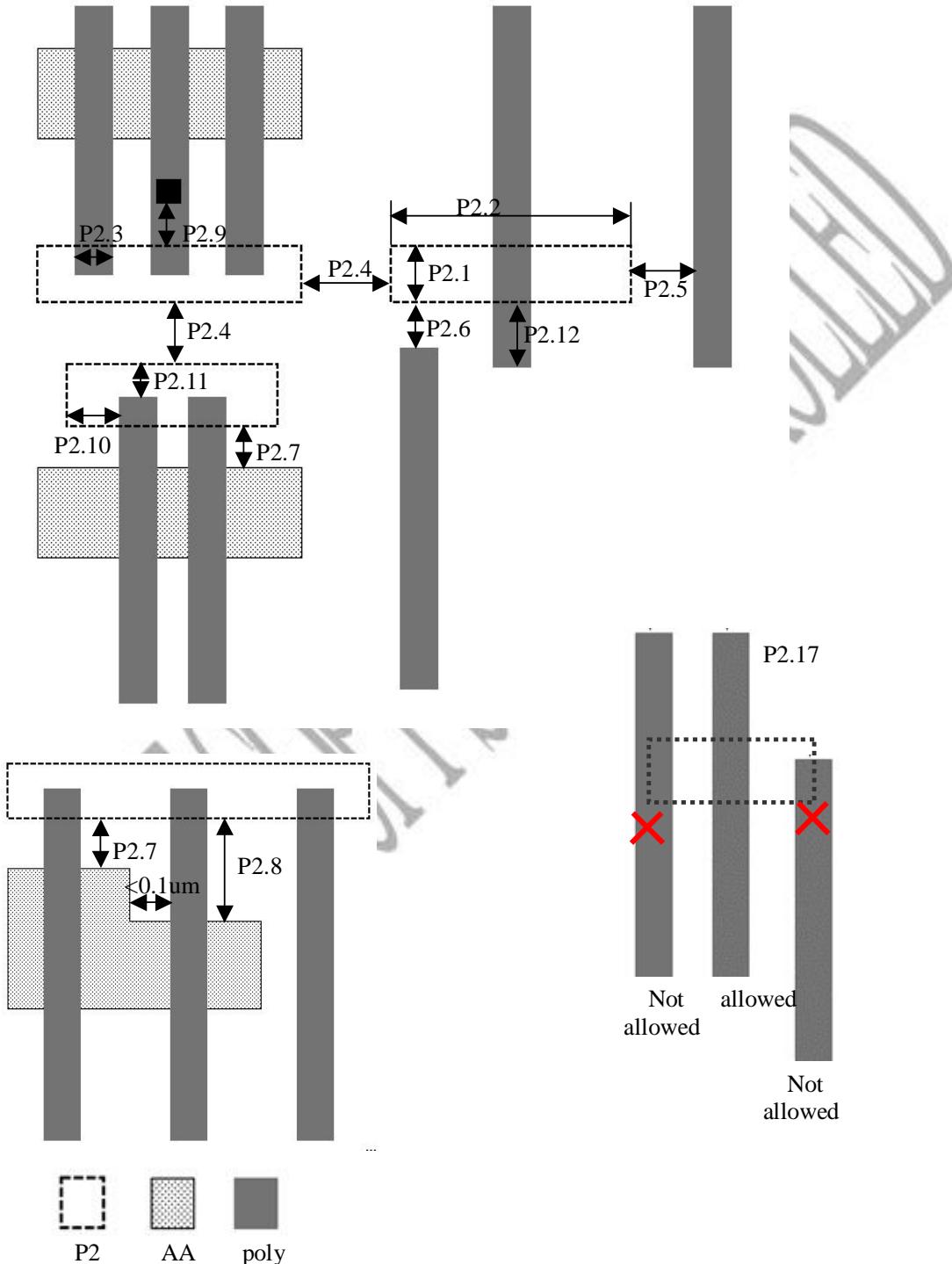


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Rule number	Description	Operation	Rule value	Unit
P2.16	P2 must be rectangular			
P2.17	It's not allowed (any vertex of P2) INTERACT ((poly OR GTDMP) OR GTDOP)			
P2.18	((Poly OR GTDMP) OR GTDOP) AND P2) must be rectangular except small jogs (jog \leq 0.005um)			
P2.19	Area of (((poly OR GTDMP) OR GTDOP) NOT P2). This rule doesn't check rectangle (((poly OR GTDMP) OR GTDOP) NOT P2) INTERACT AA) any edge \geq 0.23um.	\geq	0.009	um ²
P2.20	Overlap area of P2 and AA_DMY.	\leq	0.01	um ²
P2.21	The outermost ((Poly OR GTDMP) INTERACT P2) must be floating when P2 length \geq 18um. The floating definition is: (((Poly OR GTDMP) NOT P2) NOT INTERACT CT).			
P2.22 ^[R]	Recommended (P2 or P2DUM or P2DOP) density in full chip	\geq	5%	

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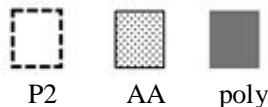
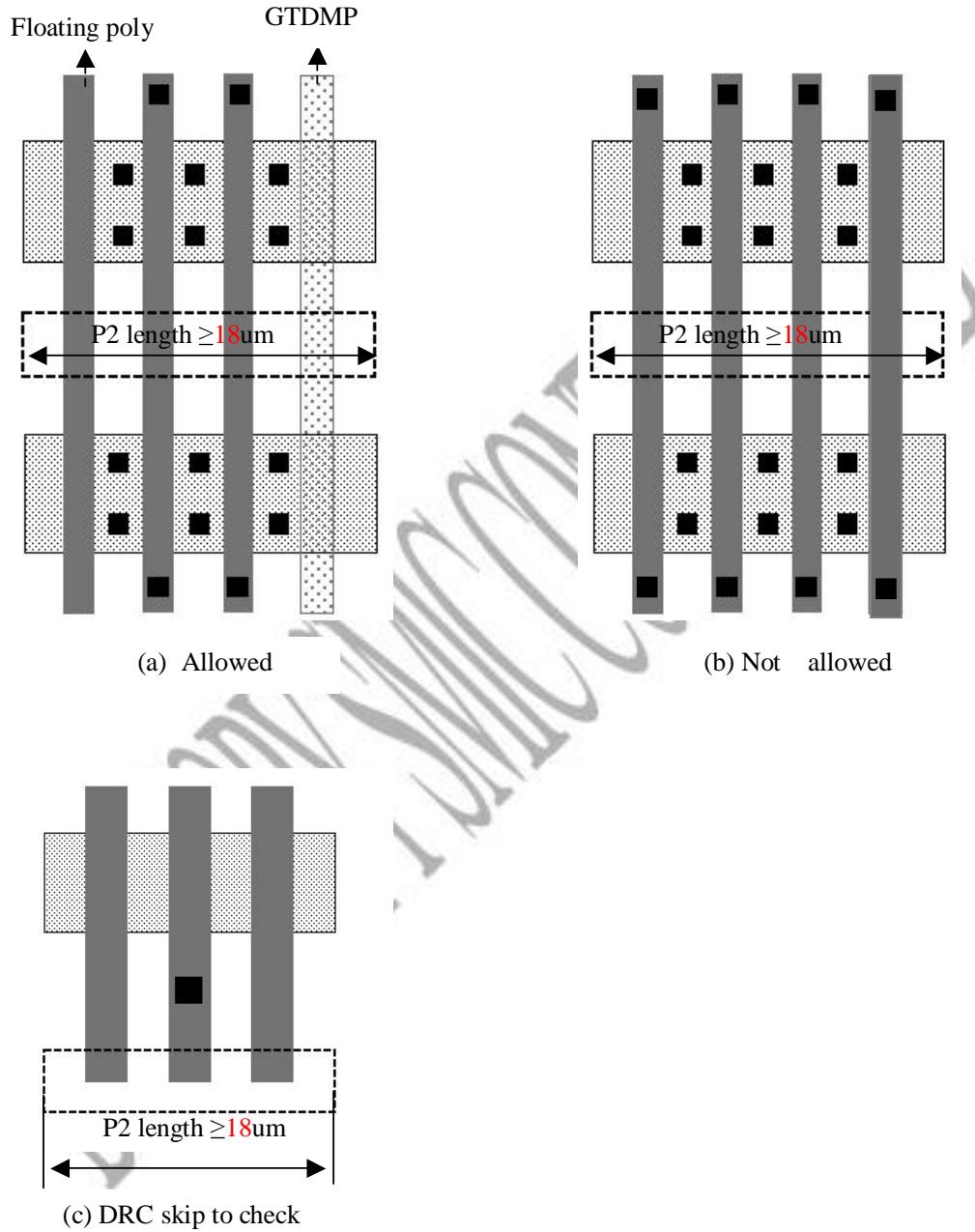
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P2.21



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7.2.16 SN: N+ source/drain implantation design rules

Rule number	Description	Operation	Design Value	Unit
SN.1	SN width. Single-point-interaction is allowed. DRC doesn't check INST and RFSRAM region.	\geq	0.16	um
SN.2	Space between SNs. Single-point-interaction is allowed.	\geq	0.16	um
SN.3 ^[R]	Space between SNs with parallel run length >0.24um, when one SN width >0.22um.	\geq	0.18	um
SN.4	Space between SNs, when one or both SNs width (W1) < 0.22um. DRC only check opposite side.	\geq	0.22	um
SN.5	Space between SNs with parallel run length >0.33um and SN space is on STI (not INTERACT AA OR AA_DMY).	\geq	0.25	um
SN.6	Space between SN and GATE along the source/drain direction. DRC doesn't check INST and RFSRAM region.	\geq	0.14	um
SN.7	Space between SN and GATE along GATE poly direction. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um
SN.8	Space between SN and non-butted P+AA. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um
SN.9	Space between SN and non-butted P+ pick-up AA	\geq	0.02	um
SN.10 ^[NC]	Space between SN and butted P+AA or P+ pick-up AA	=	0	um
SN.11	Space between butted N+ pick-up AA and PMOS GATE in the same AA.	\geq	0.165	um
SN.12	Space between butted N+ pick-up AA (in L shape AA) and PMOS GATE poly in the same AA, when this butted N+ pick-up AA extrusion: $0 < h < 0.08\text{um}$	\geq	0.165	um
SN.13	SN extension outside of GATE along the source/drain direction.	\geq	0.14	um
SN.14	SN extension outside of NMOS GATE along the source/drain direction where there is a butted P+ pick-up AA in the same AA	\geq	0.165	um
SN.15	SN extension outside of GATE along the GATE poly	\geq	0.065	um

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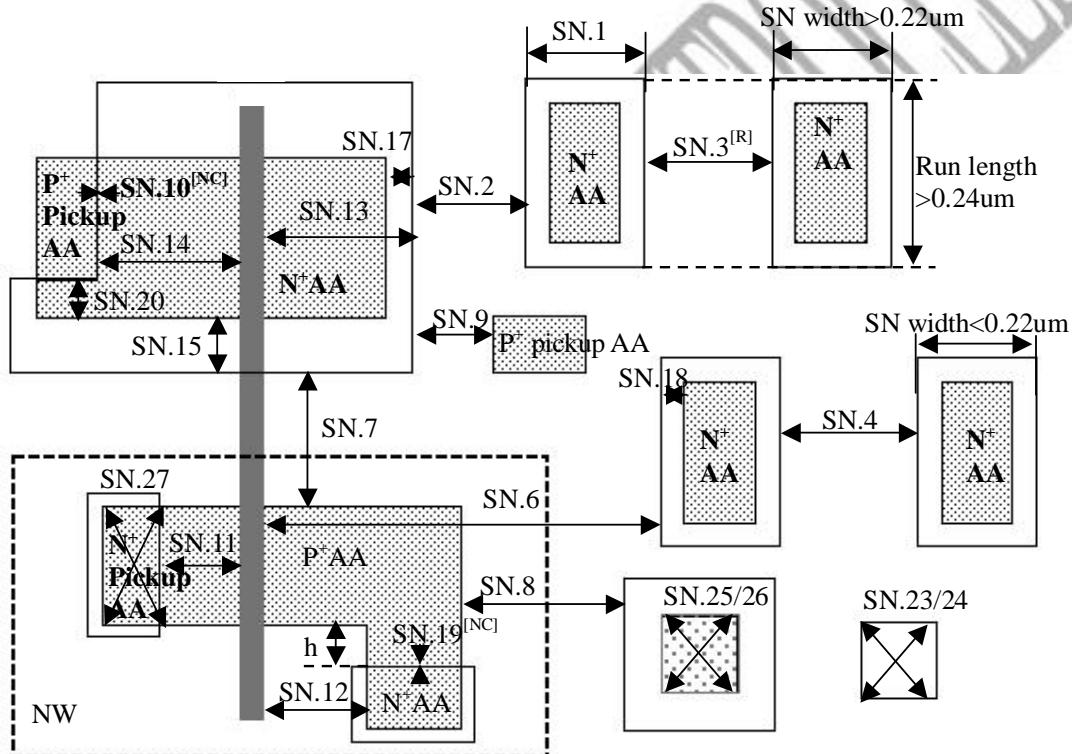
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Rule number	Description	Operation	Design Value	Unit
	direction. DRC doesn't check INST and RFSRAM region.			
SN.16	SN extension outside of NW/DG/TG. Extension=0um is allowed. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SN.17	Enclosure of N+AA by SN. DRC doesn't check INST, RFSRAM and (AA INTERACT RESNW) region.	\geq	0.065	um
SN.18	Enclosure of non-butted N+ pickup AA by SN.	\geq	0.02	um
SN.19^[NC]	Enclosure of butted N+ pickup AA by SN.	\geq	0	um
SN.20	SN and AA overlap	\geq	0.08	um
SN.21	SN and DG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SN.22	SN and TG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SN.23	Area of SN, while (((((SN NOT NW) INTERACT CT)sizing up 0.079um)sizing down 0.158um)sizing up 0.079um) DRC doesn't check INST and RFSRAM region. DRC doesn't flag the rectangle pattern, when 1. Any one of the edge length =0.33um, 2. The space between any two outer vertexes =0.16um.	\geq	0.1	um ²
SN.24	Area of SN.	\geq	0.07	um ²
SN.25	Enclosed area of SN, while (((((SN NOT NW) INTERACT CT) sizing up 0.079) sizing down 0.158) sizing up 0.079). DRC doesn't check INST and RFSRAM region. DRC doesn't flag the rectangle pattern, when 1. Any one of the edge length =0.33um, 2. The space between any two inner vertexes =0.16um.	\geq	0.1	um ²
SN.26	Enclosed area of SN.	\geq	0.07	um ²
SN.27	N+ butted AA in NW area(the area interact with CT)	\geq	0.024	um ²

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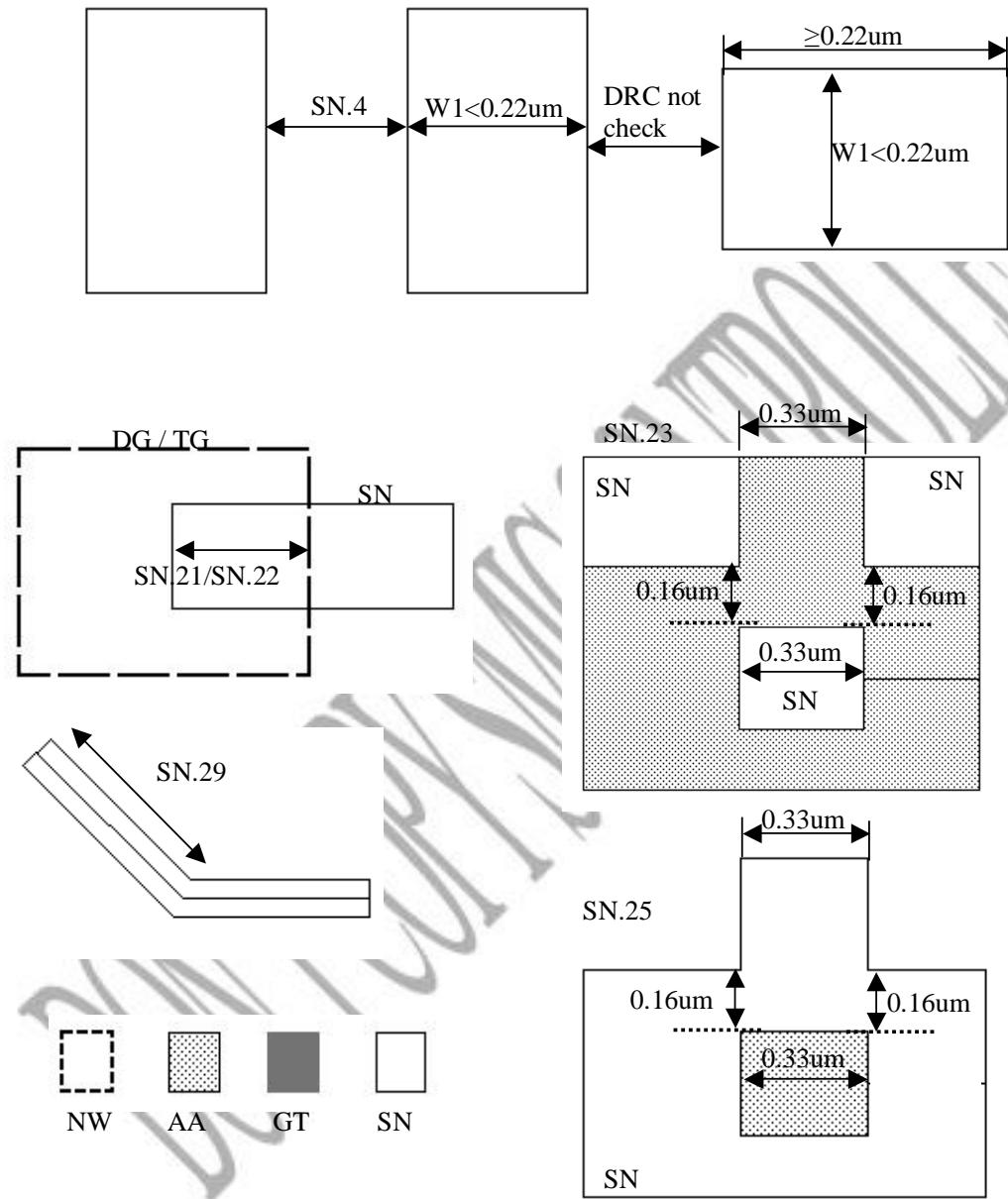
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Rule number	Description	Operation	Design Value	Unit
SN.28	SN and SP overlap is forbidden			
SN.29	45-degree edge length	\geq	0.52	um
SN.30	(SN AND (AA AND poly)) in NW is not allowed, except LDBK and VARMOS region.			



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7.2.17 SP : P+ source/drain implantation design rules

Rule number	Description	Operation	Design Value	Unit
SP.1	SP width. Single-point-interaction is allowed.	\geq	0.16	um
SP.2	Space between SPs. Single-point-interaction is allowed. DRC doesn't check INST and RFSRAM region.	\geq	0.16	um
SP.3 ^[R]	Space between SPs with parallel run length >0.24um, when one SP width >0.22um	\geq	0.18	um
SP.4	Space between SPs when one or both SPs width (W1) < 0.22um. DRC only check opposite side.	\geq	0.22	um
SP.5	Space between SPs with parallel run length >0.33um and SP space on STI(not INTERACT AA OR AA_DMY)	\geq	0.25	um
SP.6	Space between SP and GATE along the source/drain direction.	\geq	0.14	um
SP.7	Space between SP and GATE along GATE poly direction. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um
SP.8	Space between SP and non-butted N+AA. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um
SP.9	Space between SP and non-butted N+ pickup AA	\geq	0.02	um
SP.10 ^[NC]	Space between SP and butted N+ AA or N+ pick-up AA	=	0	um
SP.11	Space between butted P+ pick-up AA and NMOS GATE in the same AA.	\geq	0.165	um
SP.12	Space between butted P+ pick-up AA (in L shape AA) and NMOS GATE poly in the same AA, when this butted P+ pick-up AA extrusion: $0 < h < 0.08\text{um}$	\geq	0.165	um
SP.13	SP extension outside of GATE along the source/drain direction. DRC doesn't check INST and RFSRAM region.	\geq	0.14	um
SP.14	SP extension outside of PMOS GATE along the source/drain direction where there is a butted N+ pick-up AA in the same AA	\geq	0.165	um
SP.15	SP extension outside of GATE along the GATE poly direction. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um

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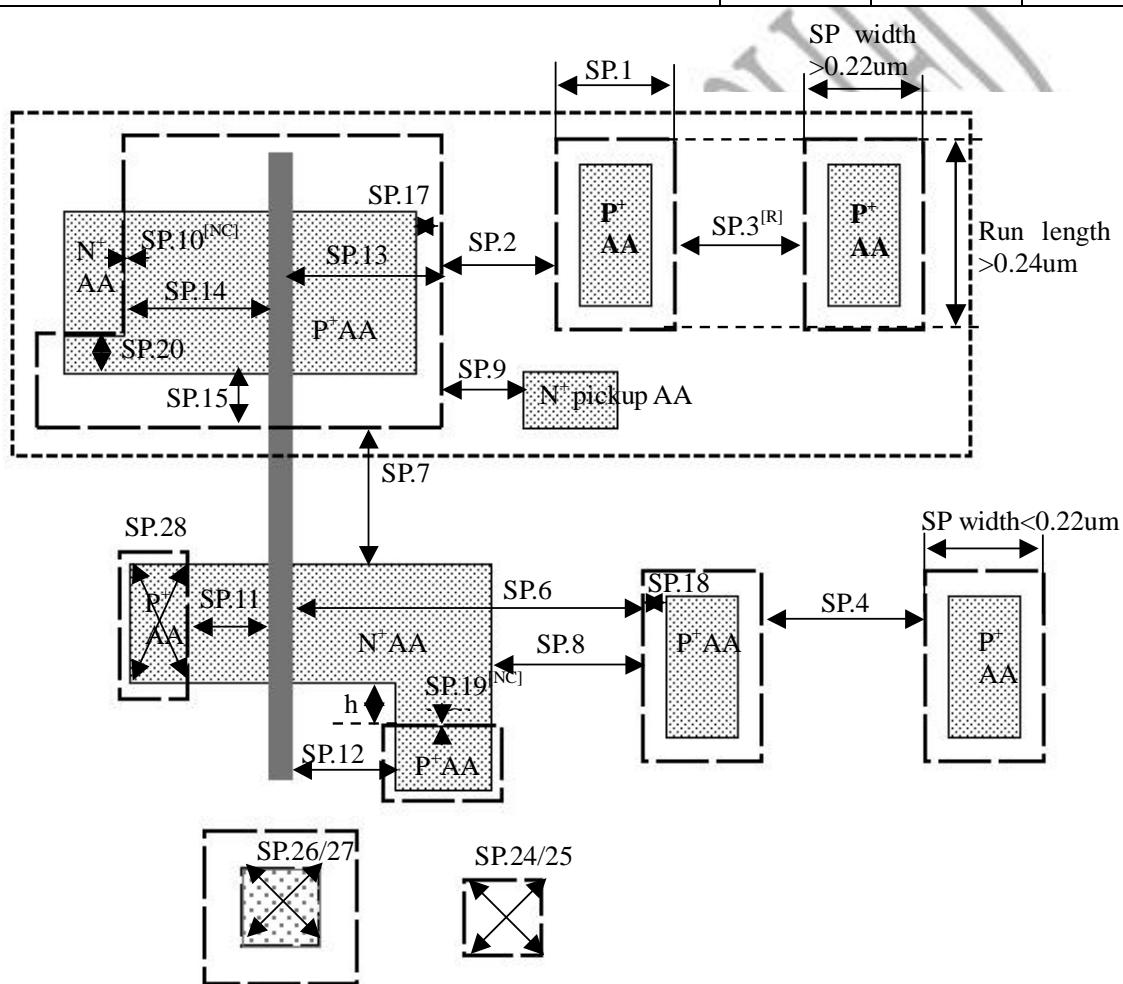
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Rule number	Description	Operation	Design Value	Unit
SP.16	SP extension outside of DG/TG. Extension=0um is allowed. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.17	Enclosure of P+AA by SP. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um
SP.18	Enclosure of non-butted P+ pickup AA by SP	\geq	0.02	um
SP.19^[NC]	Enclosure of butted P+ pickup AA by SP	\geq	0	um
SP.20	SP and AA overlap	\geq	0.08	um
SP.21	SP and NW overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.22	SP and DG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.23	SP and TG overlap. DRC flag the violation (INTERACT AA).	\geq	0.16	um
SP.24	Area of SP, while (((((SP AND NW) INTERACT CT) sizing up 0.079um) sizing down 0.158um) sizing up 0.079um). DRC doesn't check INST and RFSRAM region. DRC doesn't flag the rectangle pattern, when 1. Any one of the edge length =0.33um, 2. The space between any two outer vertexes =0.16um.	\geq	0.1	um ²
SP.25	Area of SP.	\geq	0.07	um ²
SP.26	Enclosed area of SP, while (((((SP AND NW) INTERACT CT) sizing up 0.079um) sizing down 0.158um) sizing up 0.079um). DRC doesn't check INST and RFSRAM region. DRC doesn't flag the rectangle pattern, when 1. Any one of the edge length =0.33um, 2. The space between any two inner vertexes =0.16um.	\geq	0.1	um ²
SP.27	Enclosed area of SP.	\geq	0.07	um ²
SP.28	P+ butted AA in P-well area(the area interact with CT)	\geq	0.024	um ²

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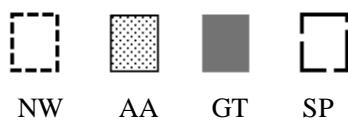
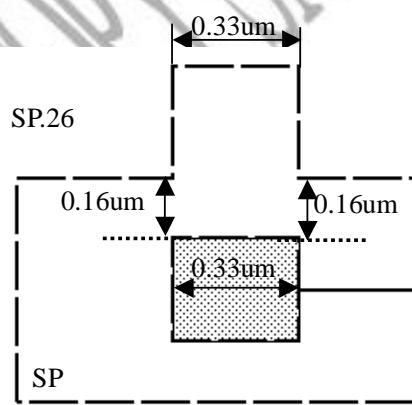
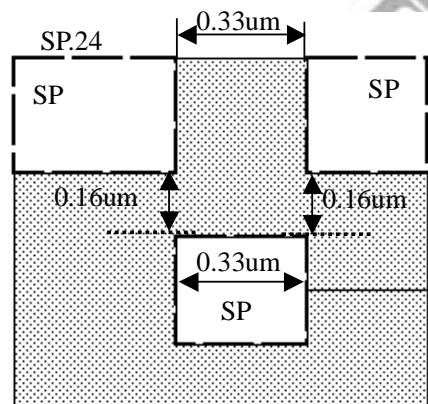
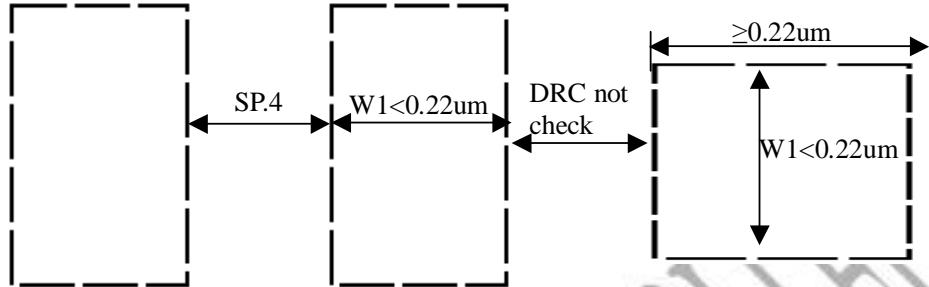
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Rule number	Description	Operation	Design Value	Unit
SP.29	45-degree edge length	\geq	0.52	um
SP.30	(SP AND (AA AND poly)) in PW is not allowed. DRC doesn't check LDBK, VARMOS, INST and RFSRAM region.			



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7.2.18 SAB: Salicide block design rules

Rule number	Description	Operation	Design Value	Unit
SAB.1	SAB width	\geq	0.32	um
SAB.2	Space between SABs	\geq	0.32	um
SAB.3	Extension of related AA outside of SAB	\geq	0.22	um
SAB.4	Space between SAB and AA	\geq	0.22	um
SAB.5	Space between SAB and GATE. Overlap of SAB and GATE is not allowed. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY , OCOVL region.	\geq	0.38	um
SAB.6a	Extension of SAB outside of unsilicided AA resistor or H-R resistor ((poly AND RESP2) INTERACT SAB). This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP , ESDPOB , CLPDMY region.	\geq	0.22	um
SAB.6b	Extension of SAB outside of unsilicided AA resistor or non-silicide poly resistor when SAB width and length >10um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.3	um
SAB.6c	Extension of SAB outside of unsilicided AA resistor or non-silicide poly resistor when SAB width \leq 0.43um. This rule isn't applicable for ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	\geq	0.3	um
SAB.7	Space between SAB and CT	\geq	0.12	um
SAB.8	(Purposely blank)			
SAB.9	SAB area	\geq	0.9	um ²
SAB.10	SAB enclosed area	\geq	0.9	um ²
SAB.11	Space between SAB and (poly on STI).	\geq	0.3	um
SAB.12	SAB and poly must not overlap one another, except poly interact with RESP2, ESDIO1, and ESDIO2, ESDCLP , ESDPOB , CLPDMY . DRC ignore the violation poly without CT.			

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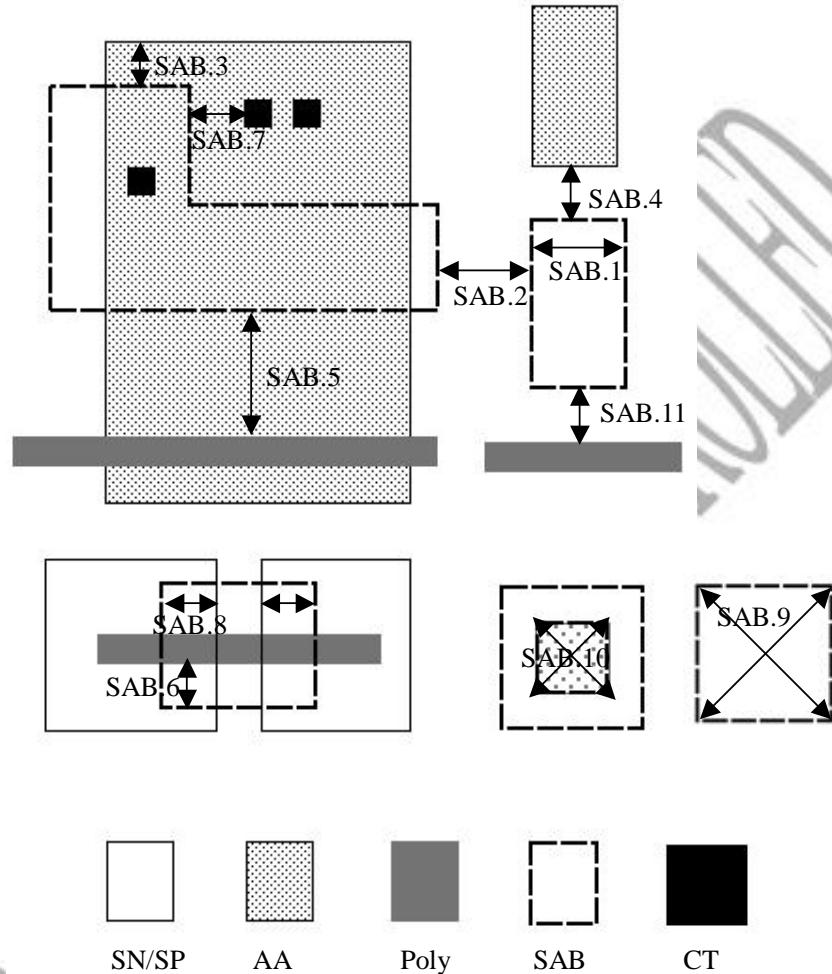
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Rule number	Description	Operation	Design Value	Unit
SAB.13	AA_DMY extension outside of SAB	≥	0.12	um

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7.2.19 P4: P4 design rules

Rule number	Description	Operation	Design Value	Unit
P4.1	P4 width	\geq	0.16	um
P4.2	Space between two P4s	\geq	0.16	um
P4.3 ^[R]	Space between P4s with parallel run length $>0.24\text{um}$, when one P4 width $>0.22\text{um}$.	\geq	0.18	um
P4.4	Space between P4s when one or both P4s width $< 0.22\text{um}$. DRC only check opposite side.	\geq	0.22	um
P4.5	Space between P4 and NMOS GATE. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um
P4.6	Space between P4 and ((Poly or POLY_DMY) NOT P2) DRC doesn't check INST and RFSRAM region.	\geq	0.04	um
P4.7	PMOS GATE must be fully covered by P4. DRC skip to check (GATE INTERACT (AA without CT)) in 2PSRAM.			
P4.7a	PMOS GATE must be fully covered by P4 in core region. DRC doesn't check INST and RFSRAM region.	\geq	0.04	um
P4.7a ^[R]	Recommended enclosure of PMOS GATE along poly length direction in core device region. DRC doesn't check INST and RFSRAM region.	\geq	0.065	um
P4.7b	PMOS GATE must be fully covered by P4 in IO region	\geq	0.09	um
P4.8a	Enclosure of ((poly or POLY_DMY) NOT P2) by P4. DRC doesn't check OCCD, INST and RFSRAM region.	\geq	0.04	um
P4.8b	Enclosure of ((poly or POLY_DMY) NOT P2) edge by P4, when the edge length $>0.17\text{um}$ and the parallel run length >0 . DRC doesn't check the region covered by OCCD, LOGO, DG and TG.	\geq	0.05	um
P4.8c	Enclosure of (((poly or POLY_DMY) NOT P2) INSIDE DG/TG)	\geq	0.09	um
P4.9	P+ Metal gate resistor and H-R resistor must be fully	\geq	0.19	um

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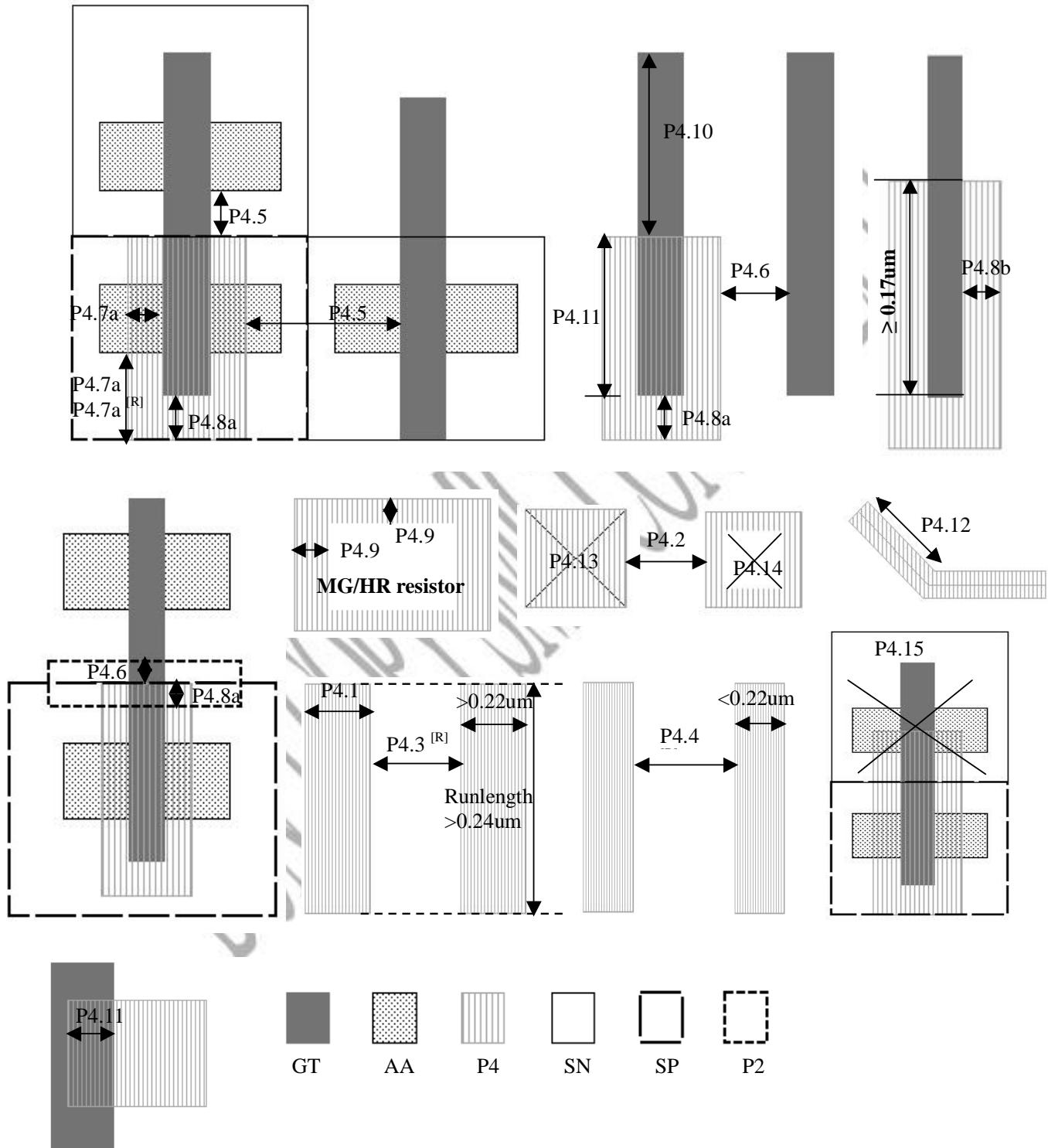


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Rule number	Description	Operation	Design Value	Unit
	covered by P4			
P4.10	((Poly or POLY_DMY) NOT P2) extension outside of P4. DRC doesn't check OCCD, INST and RFSRAM region.	\geq	0.1	um
P4.11	Overlap of P4 and ((poly or POLY_DMY) NOT P2). DRC check opposite side.	\geq	0.1	um
P4.12	The length of 45-degree P4 edge	\geq	0.52	um
P4.13	P4 area	\geq	0.1	um
P4.14	P4 enclosed area	\geq	0.1	um
P4.15	It is not allowed that P4 overlap with NMOS GATE, PSUB, RESAA, BIPOLA , DSTR and MGBL.			

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7.2.20 (Purposely blank)

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7.2.21 CT: Contact design rules

Below rules are only used for square CT region.

Rule number	Description	Operation	Design Value	Unit
CT.1	Fixed CT size (square shape) DRC don't check share CT in SRAM and OCOVL region.	=	0.04	um
CT.2a	Space between CTs. DRC doesn't check INST and RFSRAM region.	\geq	0.07	um
CT.2b	Space between CT and its neighboring CT (T). The definition of neighboring CT (T) : 1.CT (T) is in a CT group; 2.The number of this CT group is ≥ 4 , there are at least 3 CTs neighboring to CT (T); 3.The space between CT (T) to other CTs in this group $< 0.09\text{um}$. DRC doesn't check INST and RFSRAM region.	\geq	0.085	um
CT.2c	Space between CT on different nets. DRC doesn't check INST and RFSRAM region.	\geq	0.08	um
CT.3	Space between AA and CT on poly. DRC doesn't check INST and RFSRAM region.	\geq	0.035	um
CT.4a	Space between GATE and CT on AA for core device when channel length of core device $\leq 0.09\text{um}$.	\geq	0.03	um
CT.4b	Space between GATE and CT on AA for core device when channel length of core device $> 0.09\text{um}$.	\geq	0.04	um
CT.4c	Space between GATE and CT on AA for IO device.	\geq	0.07	um
CT.4d	Space between (poly or GTDMP or GTDOP) and CT on AA in vertical direction.	\geq	0.04	um
CT.5	Space between (CT AND (INST OR RFSRAM)) and (CT NOT (INST OR RFSRAM))	\geq	0.2	um
CT.6	CT must be fully covered by AA. Enclosure by AA must follow (CT.6a and CT.6b) or CT.6c as below.			
CT.6a	Enclosure by AA for a CT landed on AA. DRC doesn't check INST and RFSRAM region.	\geq	0.005	um

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Rule number	Description	Operation	Design Value	Unit
CT.6a ^[R]	Enclosure by AA for CT landed on AA when channel length > 0.09um to avoid high resistance. DRC doesn't check INST and RFSRAM region.	≥	0.015	um
CT.6b	Enclosure by AA for CT landed on AA when enclosure by AA on either perpendicular direction ≥ 0.005um. DRC doesn't check INST and RFSRAM region.	≥	0.03	um
CT.6b ^[R]	Enclosure by AA for CT landed on AA when enclosure by AA on either perpendicular direction ≥ 0.005um to avoid high resistance. DRC doesn't check INST and RFSRAM region.	≥	0.04	um
CT.6c	Enclosure by AA, when 1. AA width W1: 0.07um ≤ W1 ≤ 0.09um, 2. Space between AA and ((AA OR Aadmp) OR Aadop) is 0.07um, and width of ((AA OR Aadmp) OR Aadop) is 0.05um	≥	0.01	um
CT.7	CT must be fully covered by ((poly sizing up 0.005um) NOT P2). Enclosure by poly must follow (CT.7a and CT.7c) or (CT.7b and CT.7d) or (CT.7b and CT.7e) or CT.7f as below.			
CT.7a	Enclosure by poly when poly width < 0.04um.	≥	-0.005	um
CT.7b	Enclosure by poly when poly width ≥ 0.04um.	≥	0	um
CT.7c	Enclosure by poly when enclosure by poly on either perpendicular direction ≥ -0.005um, and poly width < 0.04um.	≥	0.05	um
CT.7d	Enclosure by poly when enclosure by poly on either perpendicular direction ≥ 0um, and poly width ≥ 0.04um and ≤ 0.09um.	≥	0.05	um
CT.7e	Enclosure by poly when enclosure by poly on either perpendicular direction ≥ 0um, and poly width > 0.09um.	≥	0.02	um
CT.7e ^[R]	Recommended enclosure by poly when enclosure by poly on either perpendicular direction ≥ 0um, and poly width > 0.09um.	≥	0.03	um
CT.7f	Enclosure by poly in the four sides when the poly width > 0.09um	≥	0.015	um
CT.8a	CT enclosure by AA in IO region, when space between AA	≥	0.015	um

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Rule number	Description	Operation	Design Value	Unit
	and poly < 0.05um and the parallel run length between CT and S1 >0um			
CT.8b	CT enclosure by poly in IO region, when space between poly and AA < 0.05um and the parallel run length between CT and S1 >0um	≥	0.015	um
CT.9	CT must be fully covered by M1. Enclosure by M1 must follow (CT.9a and CT.9b) or CT.9c, and CT.9d, CT.9f, as below.			
CT.9a	Enclosure by M1. DRC doesn't check OCOVL, INST and RFSRAM region.	≥	0	um
CT.9b	Enclosure by M1 when enclosure by M1 on either perpendicular directions ≥0um and <0.015um. DRC doesn't check OCOVL, INST and RFSRAM region.	≥	0.02	um
CT.9c	Enclosure by M1 in the four sides. DRC doesn't check OCOVL, INST and RFSRAM region.	≥	0.015	um
CT.9d	Enclosure by M1 in adjacent S1 side (M1 width ≥0.08um, M1 and M1 space S1 <0.06um, and the parallel run length >0.18um) This rule doesn't check two CTs (when CTs space <0.08um).	≥	0.015	um
CT.9f	Enclosure by M1 (metal width >0.7um) in the four sides. DRC violation is allowed if only one CT meets this rule for the redundant CTs pattern.	≥	0.03	um
CT.9g	Enclosure by M1 when enclosure by M1 on either perpendicular direction ≥0, and M1 area < 0.014um ² . DRC doesn't check INST and RFSRAM region.	≥	0.03	um
CT.9 ^[R]	CT must be fully covered by M1. Enclosure by M1 must follow (CT.9a ^[R] and CT.9b ^[R]) or CT.9c ^[R] , and CT.9d ^[R] , and CT.9e ^[R] as below.			
CT.9a ^[R]	Recommended enclosure by M1. DRC doesn't check INST and RFSRAM region.	≥	0.01	um
CT.9b ^[R]	Recommended enclosure by M1 when enclosure by M1 on either perpendicular direction ≥0.01um and <0.02um. DRC doesn't check INST and RFSRAM region.	≥	0.035	um

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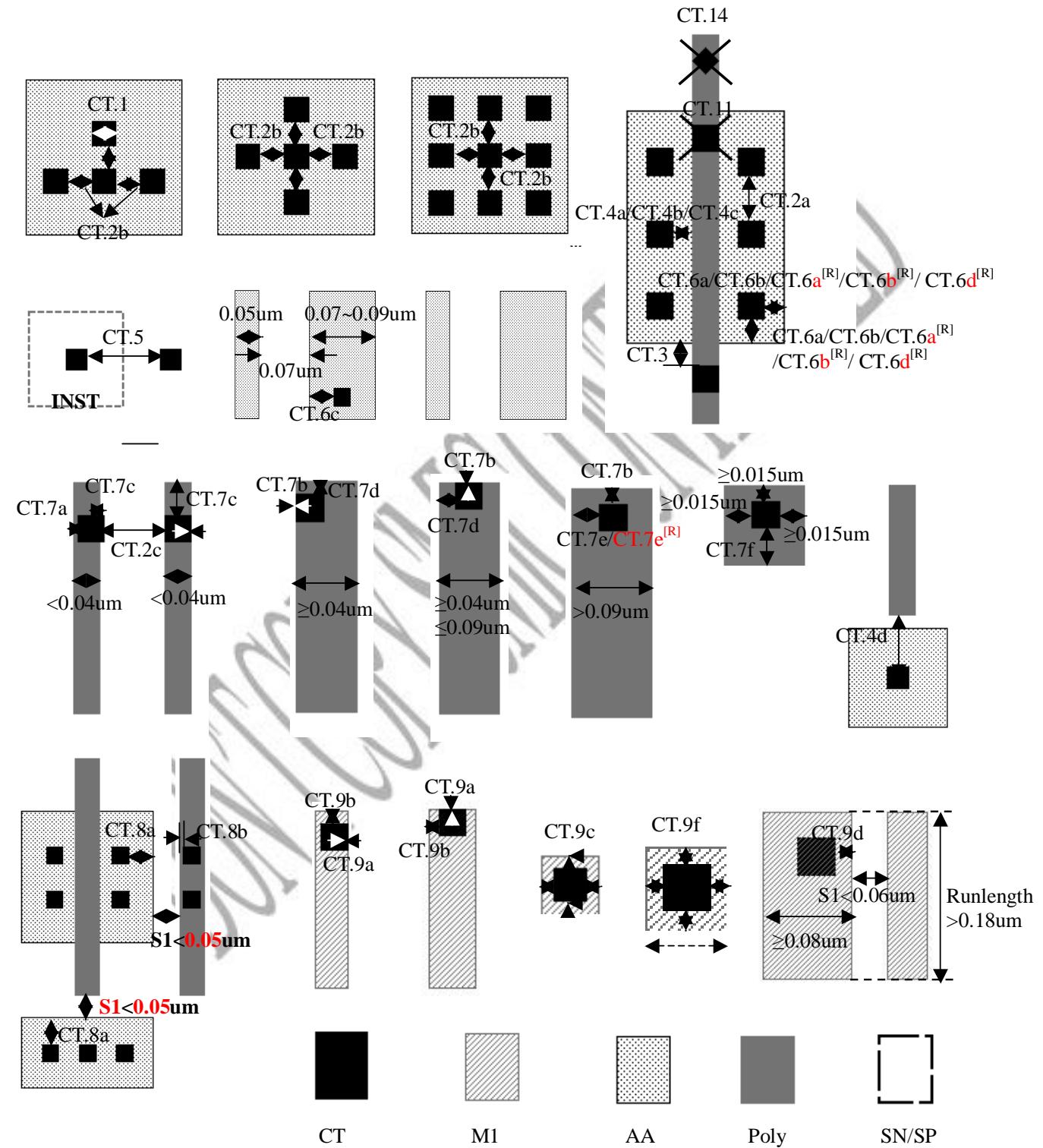


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Rule number	Description	Operation	Design Value	Unit
CT.9c ^[R]	Recommended enclosure by M1 in the four sides. DRC doesn't check INST and RFSRAM region.	\geq	0.02	um
CT.9d ^[R]	Recommended enclosure by M1(M1 width \geq 0.08um, M1 and M1 space $<$ 0.06um) This rule doesn't check two CTs (when CTs space $<$ 0.08um)	\geq	0.015	um
CT.9e ^[R]	Enclosure by M1 (metal width \geq 0.33um and \leq 0.7um) when enclosure by M1 on either perpendicular direction \geq 0.015um. DRC violation is allowed if only one CT meets this rule for the redundant CTs pattern.	\geq	0.02	um
CT.10 ^[R]	Recommended inner vertex AA enclosure of CT. This rule doesn't check the N+/P+ pickup regions	\geq	0.04	um
CT.11	CT is not allowed to land on GATE. DRC doesn't check INDMY, INST and RFSRAM region.			
CT.12	CT is not allowed to land on SAB, and can't land on STI without Poly. This rule isn't applicable for SRAM and OCOVL region.			
CT.13	CT enclosed by butted SN/SP edge on AA	\geq	0.035	um
CT.14	45-degree rotated CT is not allowed.			
CT.15	CT can't overlap with SN/SP boundary (for CTs on AA).			
CT.16 ^{[INC][R]}	Recommend put more CTs avoid high resistance wherever layout allows.			
CT.17	It's not allowed CT overlap with AA silicided resistor or metal gate resistor. Pls refer the definition of AA silicided resistor or metal gate resistor in AA resistor/MG section.			
CT.18	It's not allowed CT connects to \geq 5V net outside DG/TG region.			

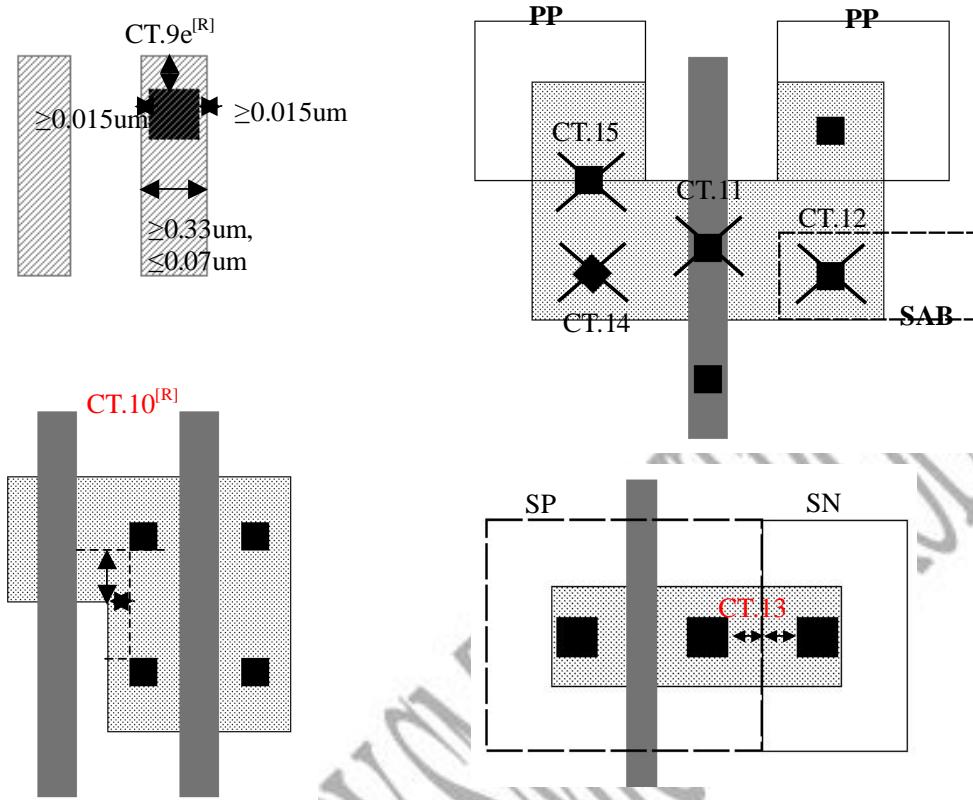
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7.2.22 M1: Metal 1 design rules

Rule number	Description	Operation	Design Value	Unit
M1.1	M1 width	\geq	0.05	um
		\leq	4.5	um
M1.2a	Width of 45-degree M1. The vertex of 45-degree pattern should be on 0.005um grid. DRC doesn't check INDMY region for the vertex of 45-degree pattern grid.	\geq	0.17	um
M1.2b	Length of 45-degree M1	\geq	0.5	um
M1.3	M1 edge length when the adjacent edge $< 0.05\text{um}$, and these two edges formed by 3 consecutive 270 degree inner vertex-90 degree outer vertex-270 degree inner vertex. DRC doesn't flag if there is M1 in the region which is formed by 0.16um extension from these two edges and the 90-degree outer vertex.	\geq	0.065	um
M1.4^[R]	Recommended M1 width, when 1. Space between M1 and two side-wall M1 is 0.05 um, with parallel run length $> 0.16\text{um}$; 2. CT/V1 enclosure by this M1; $0.02\text{um} \leq E1 \leq 0.03\text{um}$; 3. Space between this M1 line end and M1: $0.07\text{um} \leq S \leq 0.08\text{um}$.	\geq	0.06	um
M1.5a	Space between two M1s. DRC doesn't check INST and RFSRAM region.	\geq	0.05	um
M1.5b	Space between two M1s when one or both M1 widths are $> 0.1\text{um}$, and parallel run length of two M1s is $> 0.22\text{um}$.	\geq	0.06	um
M1.5c	Space between two M1s when one or both M1 widths are $> 0.18\text{um}$, and parallel run length of two M1s is $> 0.22\text{um}$.	\geq	0.1	um
M1.5d	Space between two M1s when one or both M1 widths are $> 0.47\text{um}$, and parallel run length of two M1s is $> 0.47\text{um}$.	\geq	0.13	um
M1.5e	Space between two M1s when one or both M1 widths are $> 0.63\text{um}$, and parallel run length of two M1s is $> 0.63\text{um}$.	\geq	0.15	um

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Rule number	Description	Operation	Design Value	Unit
M1.5f	Space between two M1s when one or both M1 width are >1.5um, and parallel run length of two M1s is >1.5um.	\geq	0.5	um
M1.6a	Space between M1 and M1 line end, and the parallel run length is >0.025um. M1 line-end definition: M1 edge with length < 0.07um (W) between two outer vertex, ANGEL1=ANGEL2=90, adjacent edge A1/A2 \geq 0.05um. DRC doesn't check INST and RFSRAM region.	\geq	0.06	um
M1.6b	Space between M1 and dense M1 line-end, when parallel run length >0.025um. 1. M1 line-end definition: M1 edge with length < 0.07um (W) between two outer vertex, ANGEL1=ANGEL2=90, adjacent edge A1/A2 \geq 0.05um; 2. Dense M1 line end definition: (W+S) < 0.12um, other metal must be in the region R, L1 and L2 is the extension from metal line end, L1 < 0.025um, L2 < 0.07um, S should be the space between separate metal. DRC doesn't check INST and RFSRAM region.	\geq	0.07	um
M1.7 ^[R]	Space between (M1 or dummy M1). DRC check maximum width of (NOT (M1 or dummy M1)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LOGO.	\leq	4.5	um
M1.8	(Purposely blank)			
M1.9	Space between 45-degree M1 and M1	\geq	0.17	um
M1.10	Space between two M1s when one or both of M1 connects to 3.3V net	\geq	0.07	um
M1.11a	Space between M1 line and line when one or both of M1 connects to 5V net, parallel run length >-0.11um. M1 line definition: M1 edge \geq 0.08um.	\geq	0.11	um
M1.11b	Space between M1 line and line end when one or both of M1 connects to 5V net, parallel run length >-0.14um. M1 line end definition: M1 edge < 0.08um between two outer vertex. M1 line definition: NOT M1 line end.	\geq	0.14	um

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Rule number	Description	Operation	Design Value	Unit
M1.11c	Space between M1 line end and line end when one or both of M1 connects to 5V net, parallel run length >-0.14um. M1 line end definition: M1 edge < 0.08um between two outer vertex.	≥	0.12	um
M1.12	Space between M1 and neighboring V1 when either V1 or M1 connects to 1.5V net.	≥	0.06	um
M1.13	Space between M1 and neighboring V1 when either V1 or M1 connects to 1.8V and 2.5V net.	≥	0.08	um
M1.14	Space between M1 and neighboring V1 when either V1 or M1 connects to 3.3V net.	≥	0.087	um
M1.15	Space between M1 and neighboring V1 when either V1 or M1 connects to 5V net.	≥	0.165	um
M1.16	(Purposely blank)			
M1.17a	M1 area. DRC doesn't check INST and RFSRAM region.	≥	0.0115	um ²
M1.17a ^[R]	Recommended M1 area. DRC doesn't check INST and RFSRAM region.	≥	0.023	um ²
M1.17b	M1 area when all of M1 edge length < 0.2um, any M1 edge length ≥ 0.13um DRC doesn't check when 0.05um * 0.2um rectangular M1 pattern, and doesn't check INST and RFSRAM region.	≥	0.014	um ²
M1.17c	M1 area when all of M1 edge length < 0.13um. DRC doesn't check when 0.05um * 0.13um rectangular M1 pattern, and doesn't check INST and RFSRAM region.	≥	0.04	um ²
M1.18	Dielectric area enclosed by M1	≥	0.2	um ²
M1.19	M1 density (including dummy). Density check window size: 125um*125um, step size: 62.5um.	≥	10%	
M1.20	The density difference between any two neighboring checking windows (window 200*200, stepping 200um). DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	≤	85%	
		≤	50%	

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Rule number	Description	Operation	Design Value	Unit
M1.21 ^[R]	M1 density (including dummy) in DUMB and M1DUB region. Density check window size: 125um*125um, step size: 62.5um.	≥	10%	
	DRC need check the design if DUMB/M1DUB width is >5um and<125um, where density ratio= M1 area/(DUMB or M1DUB)area.	≤	85%	
M1.22	<p>M1 density (including dummy).Density check window size: 80um*80um, step size 40um DRC don't check:</p> <p>1. Chip corner triangle region(NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1. DRC only check the region with width of (checking window NOT above excluding region) ≥ 40um</p>	≥	1%.	
M1.23	<p>Maximum M1 area of merged low density windows must follow item (1) and (2).</p> <p>The definition of low density window: window size 10um*10um, step size: 5um, density <1%</p> <p>(1) Maximum area of merged low density window ≤ 6000um², except merged low density windows width ≤ 30um.</p> <p>(2) Maximum area of merged low density window ≤ 16000um².</p> <p>DRC don't check:</p> <p>1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1. DRC only check the region with width of (checking window NOT above excluding region) ≥ 5um</p>			
M1.24 ^[NC]	M1 line-end must be rectangular.			
M1.25	<p>Space of metal space segments with S2 < 0.08 and L2 ≤ 0.22um.</p> <p>Metal space segments definition:</p> <p>1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region;</p> <p>2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);</p> <p>3). metal space segments at least abut one metalwith width > 0.25um (W1);</p>	≥	0.3	um

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Rule number	Description	Operation	Design Value	Unit
	4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.25a	Width (S2) of metal space segments with $L2 > 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ (W1) and the parallel run length $> 0.3\mu m$ (L1) in metal space $< 0.29\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.25\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.1	um
M1.25b	Width (S2) of metal space segments with $L2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ (W1) and the parallel run length $> 0.3\mu m$ (L1) in metal space $< 0.29\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.25\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
M1.25c	Space of metal space segments with $S2 < 0.1$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ (W1) and the parallel run length $> 0.3\mu m$ (L1) in metal space $< 0.19\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);	\geq	0.3	um

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Rule number	Description	Operation	Design Value	Unit
	<p>3). metal space segments at least abut one metal with width > 0.25um (W1);</p> <p>4). L2 is the width of metal space segments which is parallel with L1 direction;</p> <p>5). S2 is the width of metal space segments which is perpendicular with L1 direction.</p>			
M1.26	<p>Space of metal space segments with S2 < 0.13 and L2 ≤ 0.22um.</p> <p>Metal space segments definition:</p> <p>1). at least one metal line width > 0.47um (W1) and the parallel run length > 0.5um (L1) in metal space < 0.32um (S1) region;</p> <p>2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);</p> <p>3). metal space segments at least abut one metal with width > 0.47um (W1);</p> <p>4). L2 is the width of metal space segments which is parallel with L1 direction;</p> <p>5). S2 is the width of metal space segments which is perpendicular with L1 direction.</p>	≥	0.3	um
M1.26a	<p>Width (S2) of metal space segments with L2 > 0.22um</p> <p>Metal space segments definition:</p> <p>1). at least one metal line width > 0.47um (W1) and the parallel run length > 0.5um (L1) in metal space < 0.32um (S1) region;</p> <p>2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);</p> <p>3). metal space segments at least abut one metal with width > 0.47um (W1);</p> <p>4). L2 is the width of metal space segments which is parallel with L1 direction;</p> <p>5). S2 is the width of metal space segments which is perpendicular with L1 direction.</p>	≥	0.13	um
M1.26b	<p>Width (S2) of metal space segments with L2 ≤ 0.22um</p> <p>Metal space segments definition:</p> <p>1). at least one metal line width > 0.47um (W1) and the parallel run length > 0.5um (L1) in metal space < 0.32um (S1) region;</p> <p>2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular</p>	≥	0.06	um

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Rule number	Description	Operation	Design Value	Unit
	with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.47um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.27	Space of metal space segments with $S2 < 0.15$ and $L2 \leq 0.22\text{um}$. Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
M1.27a	Width (S2) of metal space segments with $L2 > 0.22\text{um}$ Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.15	um
M1.27b	Width (S2) of metal space segments with $L2 \leq 0.22\text{um}$ Metal space segments definition: 1). at least one metal line width > 0.63um (W1) and the parallel run length > 0.7um (L1) in metal space < 0.34um (S1) region;	\geq	0.06	um

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Rule number	Description	Operation	Design Value	Unit
	<p>2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);</p> <p>3). metal space segments at least abut one metal with width $> 0.63\mu m$ (W1);</p> <p>4). L2 is the width of metal space segments which is parallel with L1 direction;</p> <p>5). S2 is the width of metal space segments which is perpendicular with L1 direction.</p>			
M1.28	<p>Space of metal space segments with $S2 < 0.3$ and $L2 \leq 0.22\mu m$.</p> <p>Metal space segments definition:</p> <p>1). at least one metal line width $> 1.5\mu m$ (W1) and the parallel run length $> 1.5\mu m$ (L1) in metal space $< 0.5\mu m$ (S1) region;</p> <p>2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);</p> <p>3). metal space segments at least abut one metal with width $> 1.5\mu m$ (W1);</p> <p>4). L2 is the width of metal space segments which is parallel with L1 direction;</p> <p>5). S2 is the width of metal space segments which is perpendicular with L1 direction.</p>	\geq	0.3	um
M1.28a	<p>Width (S2) of metal space segments with $L2 > 0.22\mu m$</p> <p>Metal space segments definition:</p> <p>1). at least one metal line width $> 1.5\mu m$ (W1) and the parallel run length $> 1.5\mu m$ (L1) in metal space $< 0.5\mu m$ (S1) region;</p> <p>2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);</p> <p>3). metal space segments at least abut one metal with width $> 1.5\mu m$ (W1);</p> <p>4). L2 is the width of metal space segments which is parallel with L1 direction;</p> <p>5). S2 is the width of metal space segments which is perpendicular with L1 direction.</p>	\geq	0.3	um
M1.28b	<p>Width (S2) of metal space segments with $L2 \leq 0.22\mu m$</p> <p>Metal space segments definition:</p> <p>1). at least one metal line width $> 1.5\mu m$ (W1) and the</p>	\geq	0.06	um

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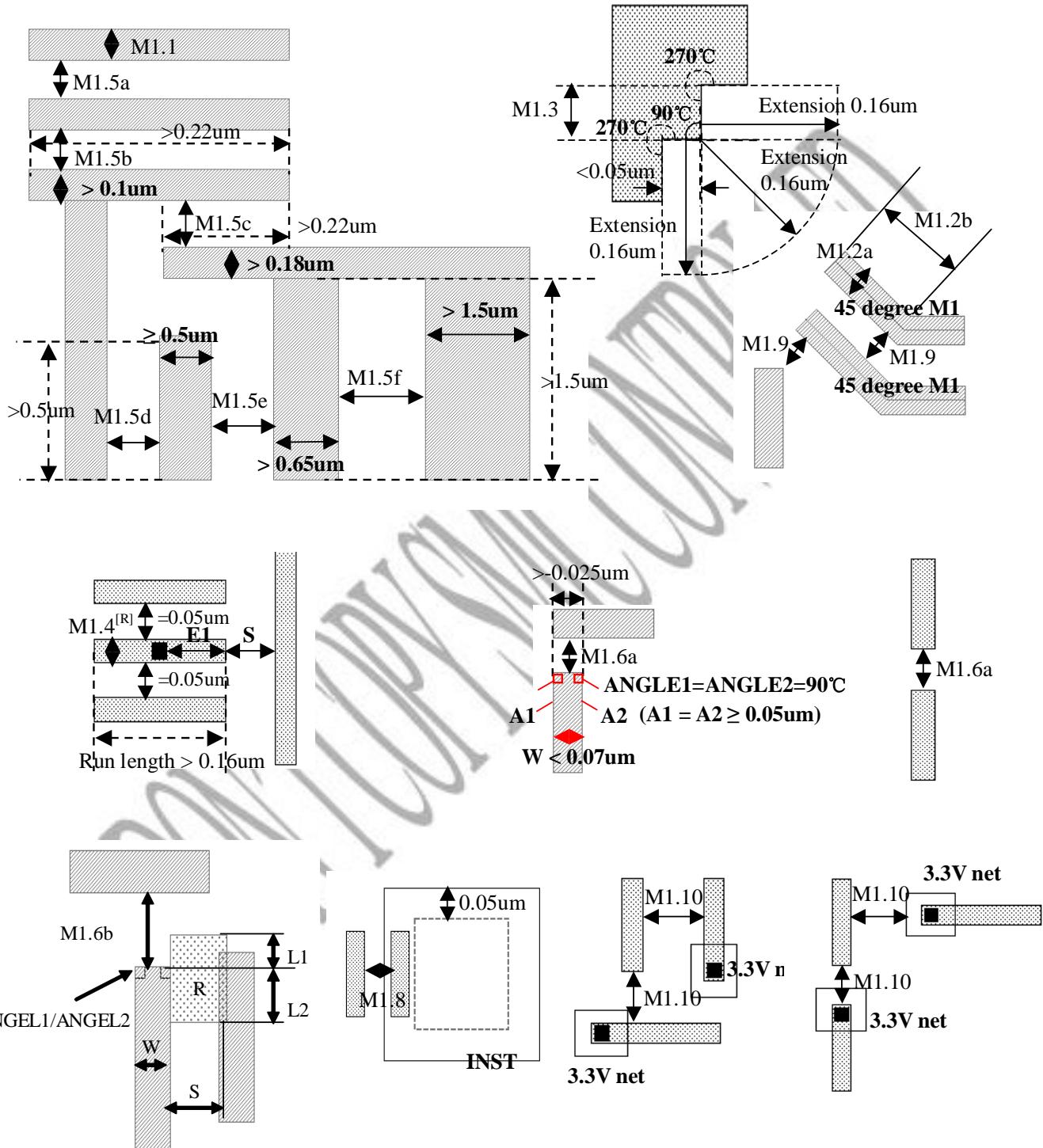
Rule number	Description	Operation	Design Value	Unit
	parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
M1.29	It is not allowed for M1 zone, and M1 Zone definition as below: 1), W1, W3 and W5 are same polygons, W2 and W4 are same polygons; 2), Width of M1 (W2,W3,W4) = 0.05um; 3), Space of M1 (S1,S2,S3,S4) =0.05um; 4), Space of M1 line-end to opposite M1(S5) < 0.08um; 5), parallel run length of 5 M1 lines L1 <= 0.4um.			

Note:

1. CT and via enclosure by M1 should be as large as the layout allows.
2. It is recommended that the lengths of metal lines are orthogonal to the lengths of metal lines on neighboring layers.
3. The marking layers have priority, higher voltage marking layer have higher priority. For example, the M1 will be identified as 2.5V M1 when there are two marking layer as M1V18 and M1V25.
4. DUMB layers are used to block metal dummy layers from being placed on the area. DUMB block dummy patterns on all metal layers.

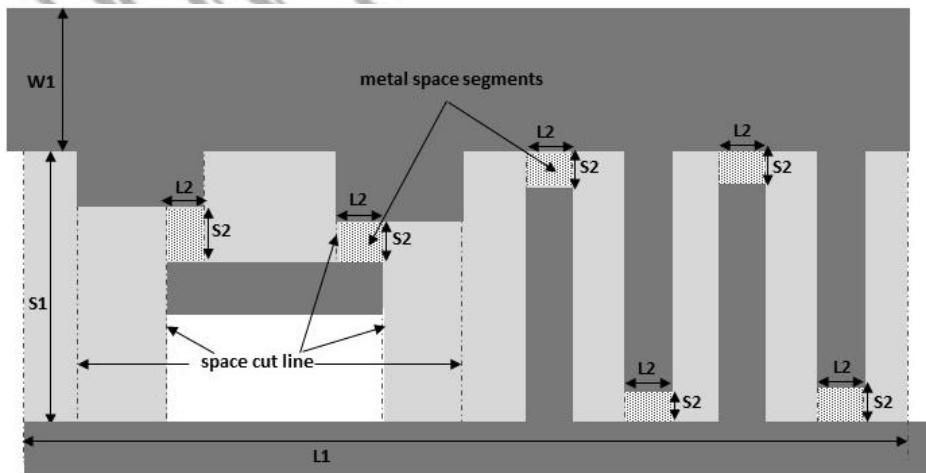
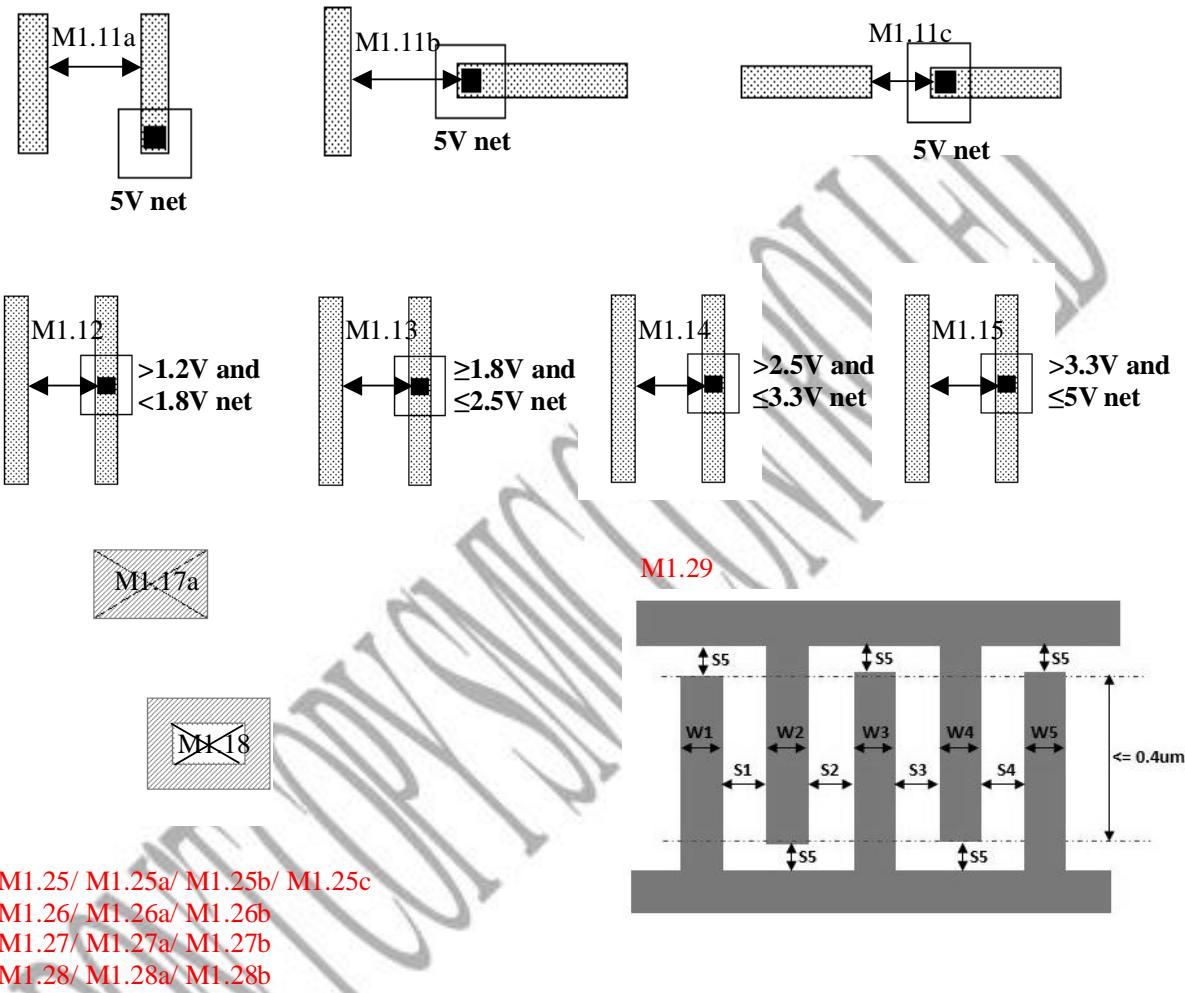
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7.2.23 1x Mn: 1x Metal design rules

Rule number	Description	Operation	Design Value	Unit
1xMn.1	1xMn width.	\geq	0.05	um
		\leq	4.5	um
1xMn.2a	Width of 45-degree 1xMn	\geq	0.17	um
1xMn.2b	Length of 45-degree 1xMn	\geq	0.5	um
1xMn.3	1xMn edge length when the adjacent edge < 0.05um, and these two edges formed by 3 consecutive 270 degree inner vertex-90 degree outer vertex-270 degree inner vertex. DRC doesn't flag if there is 1xMn in the region which is formed by 0.16um extension from these two edges and the 90-degree outer vertex.	$>$	0.065	um
1xMn.4a	Space between two 1xMns.	\geq	0.05	um
1xMn.4b	Space between two 1xMns when one or both 1xMn widths are >0.09um, and parallel run length of two 1xMns is >0.22um.	\geq	0.06	um
1xMn.4c	Space between two 1xMns when one or both 1xMn widths are >0.13um, and parallel run length of two 1xMns is >0.22um.	\geq	0.08	um
1xMn.4d	Space between two 1xMns when one or both 1xMn widths are >0.16um, and parallel run length of two 1xMns is >0.22um.	\geq	0.1	um
1xMn.4e	Space between two 1xMns when one or both 1xMn widths are >0.47um, and parallel run length of two 1xMns is >0.47um.	\geq	0.13	um
1xMn.4f	Space between two 1xMns when one or both 1xMns width are >0.63um, and parallel run length of two 1xMns is >0.63um.	\geq	0.15	um
1xMn.4g	Space between two 1xMns when one or both 1xMns width are >1.5um, and parallel run length of two 1xMns is >1.5um.	\geq	0.5	um
1xMn.5a	Space between 1xMn end to 1xMn, and the parallel run length is > 0.025um.	\geq	0.07	um

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Rule number	Description	Operation	Design Value	Unit
	length is >-0.025um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGEL1=ANGEL2=90, adjacent edge A1/A2 ≥ 0.05um. DRC doesn't check INST and RFSRAM region.			
1xMn.5b	Space between 1xMn line end and end, and the parallel run length is >-0.025um. 1xMn line definition: 1xMn edge ≥ 0.07um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGEL1=ANGEL2=90, adjacent edge A1/A2 ≥ 0.05um. DRC doesn't check INST and RFSRAM region.	≥	0.08	um
1xMn.5c	Space between 1xMn line and dense 1xMn line-end with 1xVn-1/or 1xRVn-1(E ≤ 0.05um) (the parallel run length >-0.025um). 1xMn line definition: 1xMn edge ≥ 0.07um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGEL1=ANGEL2=90, adjacent edge A1/A2 ≥ 0.05um Dense 1xMn line end definition: (W+S) <0.115um, other metal must be in the region R, L1 and L2 is the extension from metal line end, L1< 0.025um, L2 <0.07um, S should be the space between separate metal.	≥	0.08	um
1xMn.5d	Space between 1xMn line and 1xVn-1 or 1xRVn-1 (dense 1xMn line-end enclosure of 1xVn-1 or 1xRVn-1 E≤ 0.05um), the parallel run length of 1xMn line and dense 1xMn line-end >-0.025um. 1xMn line definition: 1xMn edge ≥ 0.07um. 1xMn line-end definition: 1xMn edge with length < 0.07um (W) between two outer vertex, ANGEL1=ANGEL2=90, adjacent edge A1/A2 ≥ 0.05um Dense 1xMn line end definition: (W+S) <0.115um, other metal must be in the region R, L1 and L2 is the extension from metal line end, L1< 0.025um, L2 <0.07um, S should be the space between separate metal.	≥	0.13	um
1xMn.6^[R]	Space between (1xMn or dummy 1xMn). DRC check maximum width of (NOT (1xMn or dummy	≤	4.5	um

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Rule number	Description	Operation	Design Value	Unit
	1xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LOGO.			
1xMn.7	Space between 45-degree 1xMn and 1xMn	\geq	0.17	um
1xMn.8	Space between two 1xMns when one or both of 1xMn connects to 3.3V net	\geq	0.07	um
1xMn.9a	Space between 1xMns line and line when one or both of 1xMn connects to 5V net, the parallel run length $>0.11\text{um}$. 1xMns line definition: 1xMns edge with length $\geq 0.08\text{um}$	\geq	0.11	um
1xMn.9b	Space between 1xMns line and line end when one or both of 1xMn connects to 5V net, the parallel run length $>0.14\text{um}$. 1xMns line-end definition: 1xMns edge with length $< 0.08\text{um}$ (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 $\geq 0.05\text{um}$. 1xMns line definition: 1xMns edge with length $\geq 0.08\text{um}$	\geq	0.14	um
1xMn.9c	Space between 1xMns line ends when one or both of 1xMn connects to 5V net, the parallel run length $>0.12\text{um}$. 1xMns line-end definition: 1xMns edge with length $< 0.08\text{um}$ (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 $\geq 0.05\text{um}$.	\geq	0.12	um
1xMn.10	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 1.5V net.	\geq	0.06	um
1xMn.11	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 1.8V and 2.5V net.	\geq	0.08	um
1xMn.12	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 3.3V net.	\geq	0.087	um
1xMn.13	Space between 1xMn and neighboring (Vn or Vn-1) when either (Vn or Vn-1) or 1xMn connects to 5V net.	\geq	0.165	um
1xMn.14	(Purposely blank)			
1xMn.15a	1xMn area (except M2) DRC doesn't check OCOVL region.	\geq	0.017	um ²

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Rule number	Description	Operation	Design Value	Unit
1xMn.15a ^[R]	Recommended 1xMn area. DRC doesn't check OCOVL, INST and RFSRAM region.	≥	0.023	um ²
1xMn.15b	1xMn area when all of 1xMn edge length < 0.13um. DRC doesn't check INST, 2PSRAM and RFSRAM region, and doesn't check when 0.05um * 0.13um rectangular 1xMn pattern.	≥	0.045	um ²
1xMn.16	M2 area. DRC doesn't check INST, RFSRAM and OCOVL region.	≥	0.014	um ²
1xMn.17	Dielectric area enclosed by 1xMn (um ²).	≥	0.2	um ²
1xMn.18	1xMn density (including dummy). Density check window size: 125um*125um, step size: 62.5um.	≥ ≤	10% 85%	
1xMn.19	The density difference between any two neighboring checking windows (window 200*200, stepping 200um).	≤	50%	
1xMn.20 ^[R]	1xMn density (including dummy) in DUMB and MnDUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMB/MnDUB width is >5um and <125um, where density ratio= 1xMn area/(DUMB or MnDUB)area.	≥ ≤	10% 85%	
1xMn.21	1xMn density (including dummy). Density check window size: 80um*80um, step size 40um DRC don't check: 1. Chip corner triangle region(NODMF) sizing up 0.4um if seal ring is added by SMIC. 2. The region covered by LDNMK1. DRC only check the region with width of (checking window NOT above excluding region) ≥ 40um	≥	1%.	
1xMn.22	Maximum 1x Mn area of merged low density windows must follow item (1) and (2). The definition of low density window: window size 10um*10um, step size: 5um, density <1% (1) Maximum area of merged low density window ≤ 6000um ² , except merged low density windows width ≤ 30um. (2) Maximum area of merged low density window ≤			

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Rule number	Description	Operation	Design Value	Unit
	<p>16000um².</p> <p>DRC don't check:</p> <ol style="list-style-type: none">1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.2. The region covered by LDNMK1. <p>DRC only check the region with width of (checking window NOT above excluding region) \geq 5um</p>			
1xMn.23	<p>It is not allowed to have local density > 85% of all 3 consecutive metal (1xMn, 1xMn+1 and 1xMn+2) over any window size 60*60um (stepping size 30um). The metal layers include M1/1xMn and dummy metals.</p> <p>DRC doesn't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC, seal ring region.</p>			
1xMn.24	<p>It is not allowed to have local density < 5% of all 3 consecutive metal (1xMn, 1xMn+1 and 1xMn+2) over any window 30*30um (stepping 15um). The metal layers include M1/1xMn and dummy metals.</p> <p>DRC does't check:</p> <ol style="list-style-type: none">1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.2. The region covered by LDNMK1. <p>DRC only check the region with width of (checking window NOT above excluding region) \geq 15um</p>			
1xMn.25 ^[NC]	1xMn line-end must be rectangular.			
1xMn.26	<p>Space of metal space segments with S2 < 0.08 and L2 \leq 0.22um.</p> <p>Metal space segments definition:</p> <ol style="list-style-type: none">1). at least one metal line width > 0.25um (W1) and the parallel run length > 0.3um (L1) in metal space < 0.29um (S1) region;2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);3). metal space segments at least abut one metal with width > 0.25um (W1);4). L2 is the width of metal space segments which is parallel with L1 direction;5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um

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Rule number	Description	Operation	Design Value	Unit
1xMn.26a	Width (S2) of metal space segments with $L_2 > 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ (W1) and the parallel run length $> 0.3\mu m$ (L1) in metal space $< 0.29\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.25\mu m$ (W1); 4). L_2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.1	um
1xMn.26b	Width (S2) of metal space segments with $L_2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ (W1) and the parallel run length $> 0.3\mu m$ (L1) in metal space $< 0.29\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.25\mu m$ (W1); 4). L_2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.06	um
1xMn.26c	Space of metal space segments with $S_2 < 0.1$ and $L_2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.25\mu m$ (W1) and the parallel run length $> 0.3\mu m$ (L1) in metal space $< 0.19\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.25\mu m$ (W1); 4). L_2 is the width of metal space segments which is parallel with L1 direction;	\geq	0.3	um

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Rule number	Description	Operation	Design Value	Unit
	5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.27	Space of metal space segments with $S2 < 0.13$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.47\mu m$ (W1) and the parallel run length $> 0.5\mu m$ (L1) in metal space $< 0.32\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.47\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
1xMn.27a	Width (S2) of metal space segments with $L2 > 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.47\mu m$ (W1) and the parallel run length $> 0.5\mu m$ (L1) in metal space $< 0.32\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.47\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.13	um
1xMn.27b	Width (S2) of metal space segments with $L2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.47\mu m$ (W1) and the parallel run length $> 0.5\mu m$ (L1) in metal space $< 0.32\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.47\mu m$ (W1);	\geq	0.06	um

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Rule number	Description	Operation	Design Value	Unit
	4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.28	Space of metal space segments with $S2 < 0.15$ and $L2 \leq 0.22\mu m$. Metal space segments definition: 1). at least one metal line width $> 0.63\mu m$ (W1) and the parallel run length $> 0.7\mu m$ (L1) in metal space $< 0.34\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.63\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.3	um
1xMn.28a	Width (S2) of metal space segments with $L2 > 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.63\mu m$ (W1) and the parallel run length $> 0.7\mu m$ (L1) in metal space $< 0.34\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width $> 0.63\mu m$ (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	\geq	0.15	um
1xMn.28b	Width (S2) of metal space segments with $L2 \leq 0.22\mu m$ Metal space segments definition: 1). at least one metal line width $> 0.63\mu m$ (W1) and the parallel run length $> 0.7\mu m$ (L1) in metal space $< 0.34\mu m$ (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1);	\geq	0.06	um

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Rule number	Description	Operation	Design Value	Unit
	3). metal space segments at least abut one metalwith width > 0.63um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.29	Space of metal space segments with S2 < 0.3 and L2 ≤ 0.22um. Metal space segments definition: 1). at least one metal line width > 1.5um (W1) and the parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metalwith width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.3	um
1xMn.29a	Width (S2) of metal space segments with L2 > 0.22um Metal space segments definition: 1). at least one metal line width > 1.5um (W1) and the parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metalwith width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.	≥	0.3	um
1xMn.29b	Width (S2) of metal space segments with L2 ≤ 0.22um Metal space segments definition: 1). at least one metal line width > 1.5um (W1) and the parallel run length > 1.5um (L1) in metal space < 0.5um (S1) region; 2). metal space segments within metal space (S1) region and are generated by space cut line which is perpendicular	≥	0.06	um

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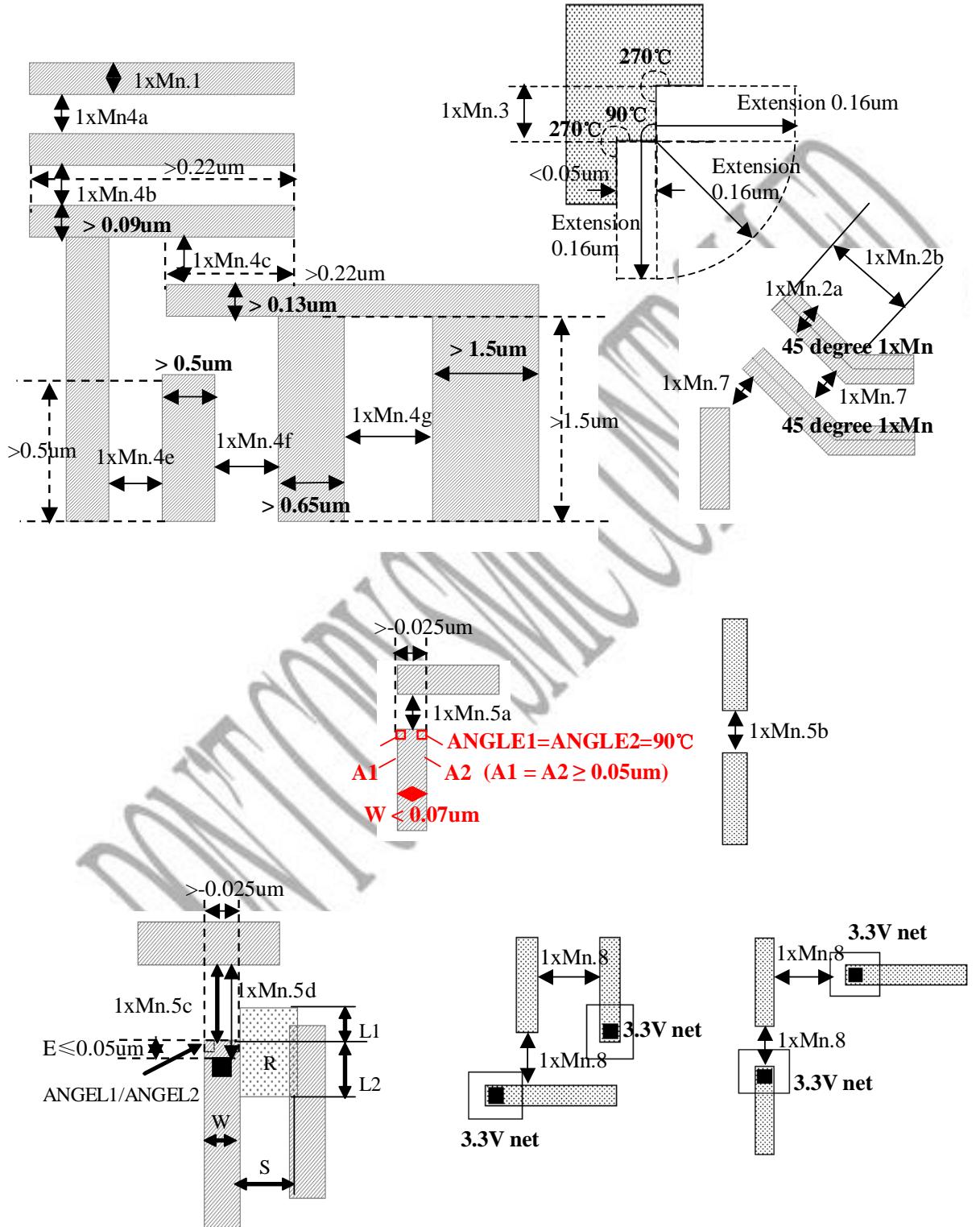
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	with L1 direction formed by all vertex in metal space region (S1); 3). metal space segments at least abut one metal with width > 1.5um (W1); 4). L2 is the width of metal space segments which is parallel with L1 direction; 5). S2 is the width of metal space segments which is perpendicular with L1 direction.			
1xMn.30	It is not allowed for 1xMn zone, and 1xMn Zone definition as below: 1), W1, W3 and W5 are same polygons, W2 and W4 are same polygons; 2), Width of 1xMn (W2,W3,W4) = 0.05um; 3), Space of 1xMn (S1,S2,S3,S4) = 0.05um; 4), Space of 1xMn line-end to opposite 1xMn (S5) < 0.08um; 5), parallel run length of 5 1xMn lines L1 <= 0.4um.			

Note:

1. CT and via enclosure by 1X Mn should be as large as the layout allows.
2. It is recommended that the lengths of metal lines are orthogonal to the lengths of metal lines on neighboring layers.
3. The marking layers have priority, higher voltage marking layer have higher priority. For example, the 1xMn will be identified as 2.5V 1xMn when there are two marking layer as MnV18 and MnV25 (n=2-8).
4. DUMBM layers are used to block metal dummy layers from being placed on the area. DUMBM block dummy patterns on all metal layers.

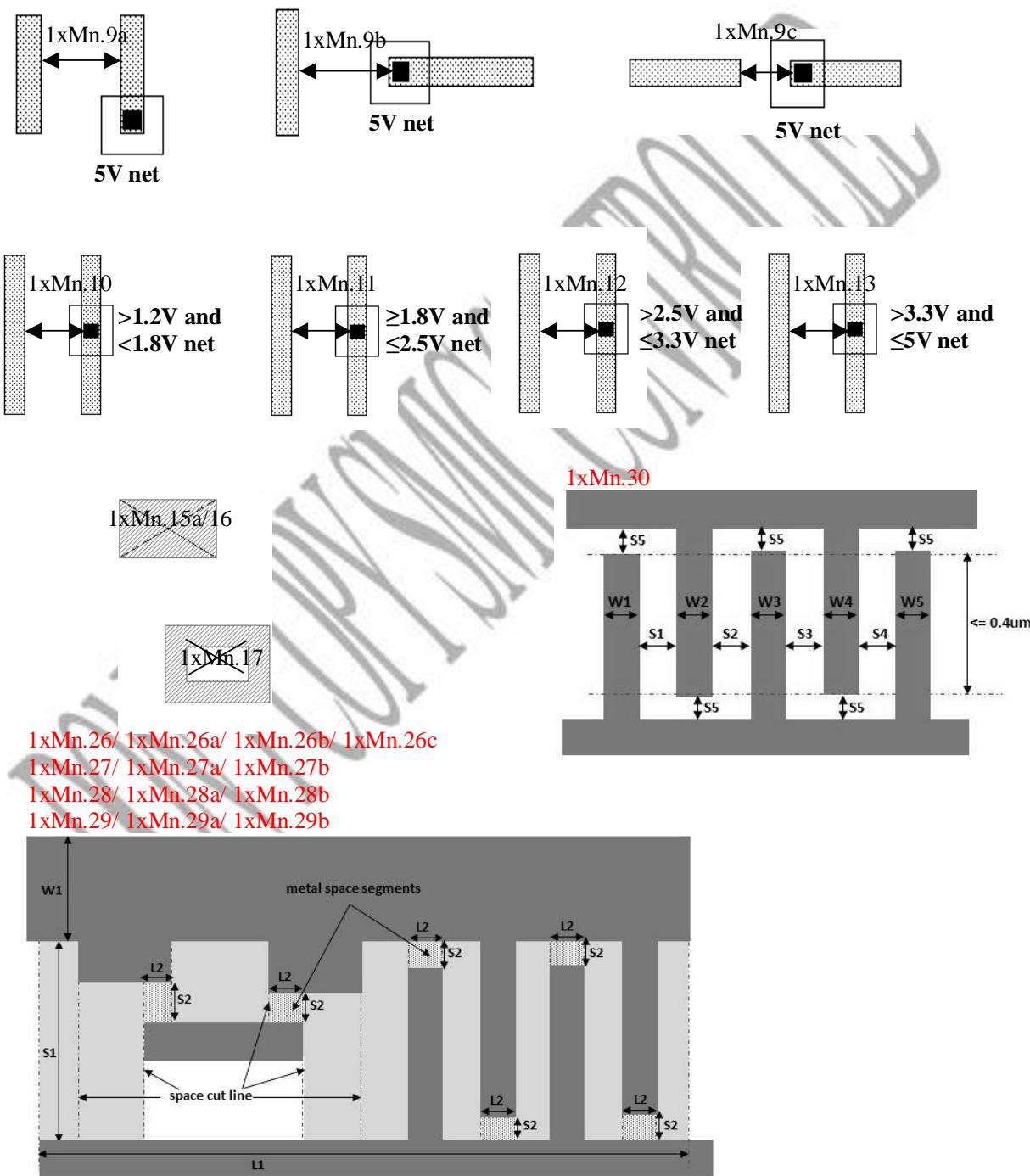
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7.2.24 1x Vn: 1x Via design rules

7.2.24.1 1x Vn: 1x square via design rules

Rule number	Description	Operation	Design Value	Unit
1xVn.1	Fixed 1x Vn size (square shape) DRC don't check rectangular 1xVn, FUSEMK1 and MARKG (0.15um 1xVn ring in MARKG region).	=	0.05	um
1xVn.2a	Space between 1x Vns when the parallel run length $\leq -0.04\text{um}$.	\geq	0.07	um
1xVn.2b	Space between 1x Vns when the parallel run length $>-0.04\text{um}$.	\geq	0.08	um
1xVn.3	1x Vn must be fully covered by M1 or 1xMn. Enclosure by M1 or 1xMn must follow (1x Vn.3a and 1x Vn.3b) or 1x Vn.3c or 1x Vn.3d as below. DRC doesn't check INST and RFSRAM region.			
1xVn.3a	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath 1x Vn.	\geq	0	um
1xVn.3b	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0\text{um}$ and $< 0.01\text{um}$ and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.03	um
1xVn.3c	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0.01\text{um}$ and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.025	um
1xVn.3d	Enclosure by M1 or 1xMn in four sides, and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.02	um
1xVn.3^[R]	1x Vn must be fully covered by M1 or 1xMn. Enclosure by 1xMn must follow (1x Vn.3a^[R] and 1x Vn.3b^[R]) or 1x Vn.3d^[R], and 1x Vn.3e^[R], and 1x Vn.3f^[R]as below. DRC doesn't check INST and RFSRAM region.			
1xVn.3a^[R]	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.01	um
1xVn.3b^[R]	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0.01\text{um}$ and $< 0.025\text{um}$ and 1xMn is the metal layer directly underneath 1x Vn.	\geq	0.05	um
1xVn.3d^[R]	Enclosure by M1 or 1xMn in four sides, and 1xMn is the	\geq	0.025	um

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Rule number	Description	Operation	Design Value	Unit
	metal layer directly underneath 1x Vn.			
1xVn.3e ^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width \geq 0.33um and \leq 0.7um, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.03	um
1xVn.3f ^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width $>$ 0.7um, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.04	um
1xVn.4	1x Vn must be fully covered by 1xMn+1. 1xMn+1 enclosure 1x Vn must follow (1x Vn.4a and 1x Vn.4b) or 1x Vn.4c or 1x Vn.4d as below. DRC doesn't check INST and RFSRAM region.			
1xVn.4a	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0	um
1xVn.4b	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0um and $<$ 0.01um and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.03	um
1xVn.4c	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0.01um and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.025	um
1xVn.4d	Enclosure by 1xMn+1 in four sides and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.02	um
1xVn.4 ^[R]	1x Vn must be fully covered by 1xMn+1. 1xMn+1 enclosure 1x Vn must follow (1x Vn.4a ^[R] and 1x Vn.4b ^[R]) or 1x Vn.4d ^[R] , and 1x Vn.4e ^[R] , and 1x Vn.4f ^[R] as below. DRC doesn't check INST and RFSRAM region.			
1xVn.4a ^[R]	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.01	um
1xVn.4b ^[R]	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0.01um and $<$ 0.025um and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.05	um

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Rule number	Description	Operation	Design Value	Unit
1xVn.4d^[R]	Enclosure by 1xMn+1 in four sides and 1xMn+1 is the metal layer directly above 1x Vn.	\geq	0.025	um
1xVn.4e^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width $\geq 0.33\text{um}$ and $\leq 0.7\text{um}$, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.03	um
1xVn.4f^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width $>0.7\text{um}$, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	\geq	0.04	um
1xVn.5a	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when 1. 1xMn width W: $0.05\text{um} < W \leq 0.055\text{um}$ 2. Space S1 $\leq 0.055\text{um}$, S2 $> 0.055\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check INST and RFSRAM region.	\geq	0.005	um
1xVn.5b	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when 1. 1xMn width W: $0.055\text{um} < W \leq 0.07\text{um}$ 2. Space S1 $< 0.065\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check INST and RFSRAM region.	\geq	0.005	um
1xVn.5c	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when 1. 1xMn width W: $0.07\text{um} < W \leq 0.16\text{um}$ 2. Space S1 $< 0.1\text{um}$, the parallel run length $> 0.1\text{um}$. DRC doesn't check 1xVn: a) Two 1xVn with space $\leq 0.11\text{um}$ in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangular with space $\leq 0.11\text{um}$ in 1xMn and 1xMn+1 intersection region. DRC doesn't check INST and RFSRAM region.	\geq	0.01	um
1xVn.5d	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath 1x Vn., when	\geq	0.015	um

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Rule number	Description	Operation	Design Value	Unit
	1. 1xMn width W: $0.16\mu m < W \leq 4.5\mu m$ 2. Space S1 $< 0.13\mu m$, the parallel run length $> 0.1\mu m$.			
1xVn.6a	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn+1 width W: $0.05\mu m < W \leq 0.055\mu m$ 2. Space S1 $\leq 0.055\mu m$, S2 $> 0.055\mu m$, the parallel run length $> 0.1\mu m$. DRC doesn't check INST and RFSRAM region.	\geq	0.005	um
1xVn.6b	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn+1 width W: $0.055\mu m < W \leq 0.07\mu m$ 2. Space S1 $< 0.065\mu m$, the parallel run length $> 0.1\mu m$. DRC doesn't check INST and RFSRAM region.	\geq	0.005	um
1xVn.6c	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn+1 width W: $0.07\mu m < W \leq 0.16\mu m$ 2. Space S1 $< 0.1\mu m$, the parallel run length $> 0.2\mu m$. DRC doesn't check 1xVn: a) Two 1xVn with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangular with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region. DRC doesn't check INST and RFSRAM region.	\geq	0.01	um
1xVn.6d	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above 1x Vn, when 1. 1xMn+1 width W: $0.16\mu m < W \leq 4.5\mu m$ 2. Space S1 $< 0.13\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.015	um
1xVn.7	45-degree rotated 1x Vn is not allowed.			
1xVn.8	Single 1xVn is not allowed in "H-shape" 1xMn+1 when: 1. The 1xMn+1 has "H-shape" interact with two metal holes: both two metal holes length $\leq 6\mu m$ (L2) and two metal hole area $\leq 6\mu m^2$. 2. The 1xVn overlaps on the center metal bar of this "H-shape" 1xMn+1.			

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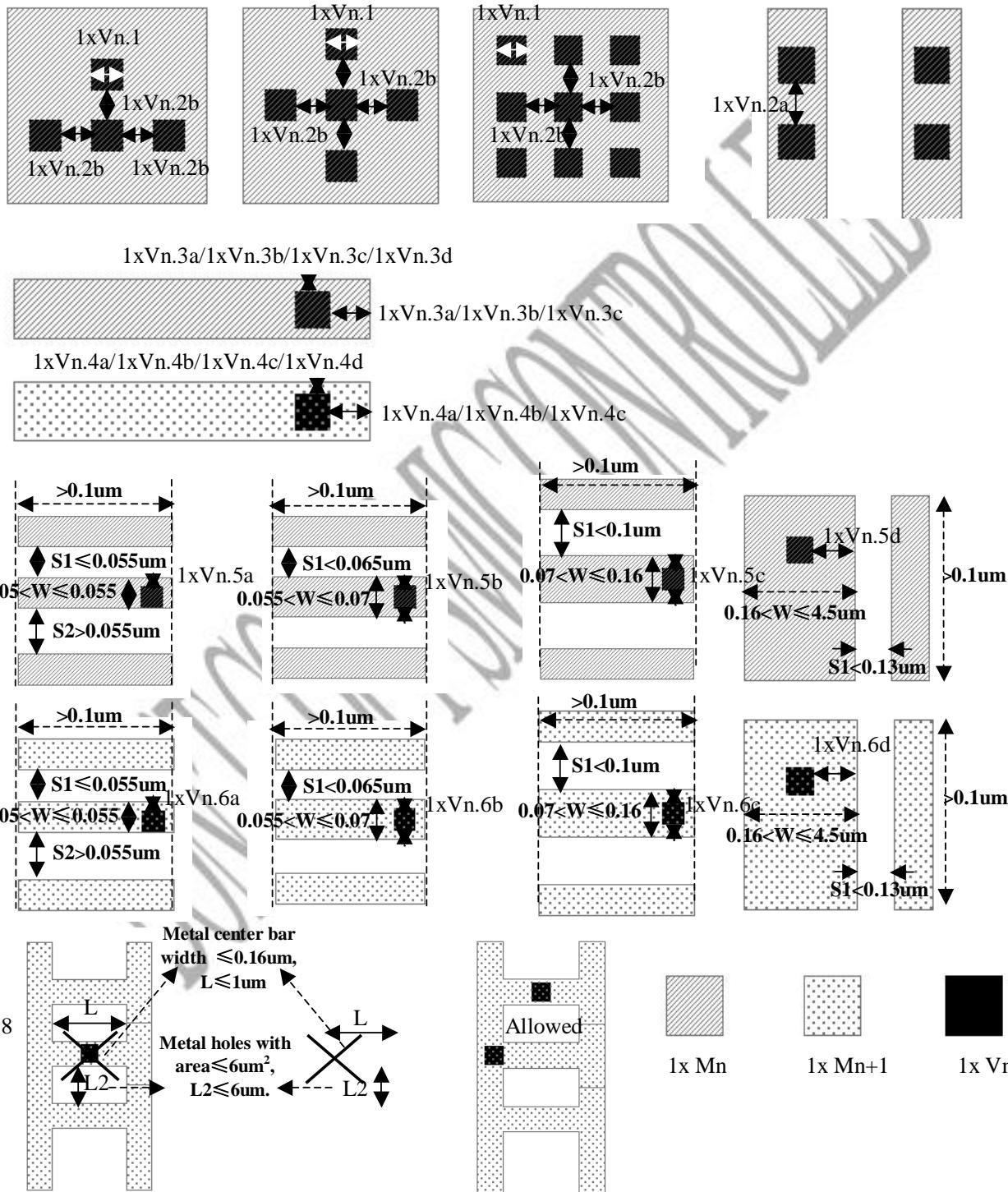


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Rule number	Description	Operation	Design Value	Unit
	3. The center metal bar length \leq 1um (L) and the metal bar width \leq 0.16um.			
1xVn. 9 ^[R]	Recommended consecutive stacked 1x Vn layer, which has only one 1x Vn for each 1x Vn layer to avoid high Rc. This rule doesn't check MARKS and DUPMK1 region.	\leq	4	
1xVn. 10 ^[R]	Recommended space between 1x Vn and 1xVn+1, where 1xVn and 1xVn+1 at different net and parallel run length > 0.02um	\geq	0.06	um

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7.2.24.2 1x RVn: 1x rectangular via design rules.

Rule number	Description	Operation	Design Value	Unit
1xRVn.1a	Fixed width of rectangular 1x Vn DRC don't check square 1xVn and MARKG (0.15um 1xVn ring in MARKG region).	=	0.05	um
1xRVn.1b	Fixed length of rectangular 1x Vn DRC don't check square 1xVn and MARKG (0.15um 1xVn ring in MARKG region).	=	0.13	um
1xRVn.2a	Space between rectangular 1x Vns	\geq	0.08	um
1xRVn.2b	Space between rectangular 1x Vn and square Vn	\geq	0.075	um
1xRVn.2c	Space between rectangular 1x Vns when the parallel run length $>0.04\text{um}$.	\geq	0.08	um
1xRVn.3	Rectangular 1x Vn must be fully covered by M1 or 1xMn. Enclosure by 1xMn must follow (1x RVn.3a and 1x RVn.3c) or 1x RVn.3b or 1x RVn.3d, or 1x RVn.3e, or 1x RVn.3f as below.			
1xRVn.3a	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.01	um
1xRVn.3b	Enclosure by M1 or 1xMn at rectangular 1xVn width side when enclosure by 1xMn (D1) at rectangular 1xVn length side is $\geq 0\text{um}$, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.04	um
1xRVn.3c	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction $\geq 0.01\text{um}$ and $<0.02\text{um}$, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.03	um
1xRVn.3d	Enclosure by M1 or 1xMn when enclosure by 1xMn in four sides, where 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.02	um

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Rule number	Description	Operation	Design Value	Unit
1xRVn.3e ^[R]	Enclosure by M1 or 1x Mn (1x Mn width \geq 0.33um and \leq 0.7um), when enclosure by 1xMn on either perpendicular direction \geq 0.015um. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	\geq	0.03	um
1xRVn.3f ^[R]	Enclosure by M1 or 1x Mn (1x Mn width > 0.7um), when enclosure by 1x Mn on either perpendicular direction \geq 0.03um. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	\geq	0.04	um
1xRVn.4	Rectangular 1x Vn must be fully covered by 1xMn+1. Enclosure by 1xMn+1 must follow (1x RVn.4a and 1x RVn.4c) or 1X RVn.4b or 1x RVn.4d, and 1x RVn.4e, and 1x RVn.4f as below.			
1xRVn.4a	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.01	um
1xRVn.4b	Enclosure by 1xMn+1 at rectangular 1xVn width side when enclosure by 1xMn+1 (D1) at rectangular 1xVn length side is \geq 0um, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.04	um
1xRVn.4c	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0.01um and $<$ 0.02um, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.03	um
1xRVn.4d	Enclosure by 1xMn+1 when enclosure by 1xMn+1 in four sides, where 1xMn+1 is the metal layer directly above rectangular 1x Vn. DRC doesn't check INST and RFSRAM region.	\geq	0.02	um
1xRVn.4e ^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width \geq 0.33um and \leq 0.7um), when enclosure by 1x Mn+1 on either perpendicular direction \geq 0.015um. 1x Mn+1 is the metal	\geq	0.03	um

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Rule number	Description	Operation	Design Value	Unit
	layer directly above rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.			
1xRVn.4f^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width >0.7um), when enclosure by 1x Mn+1 on either perpendicular direction ≥0.03um. 1x Mn+1 is the metal layer directly above rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	≥	0.04	um
1xRVn.5a	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangle 1x Vn., when 1. 1xMn width W: 0.05um<W≤0.055um 2. Space S1≤0.055um, S2>0.055um, the parallel run length > 0.1um. DRC doesn't check INST and RFSRAM region.	≥	0.005	um
1xRVn.5b	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangle 1x Vn., when 1. 1xMn width W: 0.055um<W≤0.07um 2. Space S1 < 0.065um, the parallel run length > 0.1um.	≥	0.005	um
1xRVn.5c	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangle 1x Vn., when 1. 1xMn width W: 0.07um<W≤0.16um 2. Space S1 < 0.1um, the parallel run length > 0.1um. DRC doesn't check rectangular 1xVn: a) Two 1xVns with space ≤0.11um in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangular with space ≤0.11um in 1xMn and 1xMn+1 intersection region.	≥	0.01	um
1xRVn.5d	Enclosure by 1xMn(n=2-8) in adjacent S1 side, where 1xMn is the metal layer directly underneath rectangle 1x Vn., when 1. 1xMn width W: 0.16um<W≤4.5um 2. Space S1 < 0.13um, the parallel run length > 0.1um.	≥	0.015	um

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Rule number	Description	Operation	Design Value	Unit
1xRVn.6a	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.05\mu m < W \leq 0.055\mu m$ 2. Space S1 $\leq 0.055\mu m$, S2 $> 0.055\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.005	um
1xRVn.6b	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.055\mu m < W \leq 0.07\mu m$ 2. Space S1 $< 0.065\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.005	um
1xRVn.6c	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.07\mu m < W \leq 0.16\mu m$ 2. Space S1 $< 0.1\mu m$, the parallel run length $> 0.2\mu m$. This rule doesn't check DRC doesn't check rectangle 1xVn: a) Two 1xVns with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region. b) One 1xVn and one rectangle with space $\leq 0.11\mu m$ in 1xMn and 1xMn+1 intersection region.	\geq	0.01	um
1xRVn.6d	Enclosure by 1xMn+1 in adjacent S1 side, where 1xMn+1 is the metal layer directly above rectangle 1x Vn., when 1. 1xMn+1 width W: $0.16\mu m < W \leq 4.5\mu m$ 2. Space S1 $< 0.13\mu m$, the parallel run length $> 0.1\mu m$.	\geq	0.015	um
1xRVn.7^[NC]	Two square Vias are equal to one rectangular Via in the following rules (1xRVn.7).			
1xRVn.7	Redundant via requirement must be obeyed by one of following condition of via number and space for 1xMn and 1xMn+1 condition (one of 1xMn or 1xMn+1 width and length $W1 > 0.18\mu m$): 1. when $W1 > 0.18$ and $\leq 0.44\mu m$: a) At least one rectangular via; b) At least two square vias with space $\leq 0.1\mu m$; c) At least 4 square vias with space $\leq 0.6\mu m$ 2. when $W1 > 0.44\mu m$: a) At least 4 square vias with space $\leq 0.1\mu m$; b) At least 9 square vias with space $\leq 0.85\mu m$, which two square vias can be replaced one rectangular			

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Rule number	Description	Operation	Design Value	Unit
	<p>via(at least 5 rectangular vias are equal to this 9 square vias. Rectangular via is prior to square via.</p> <p>c) At least one square via and two rectangular vias (space between two rectangular vias $\leq 0.13\mu m$).</p>			
1xRVn.8a	There should be at least one rectangular 1x Vn or two square 1x Vns in the intersection area of 1xMn and 1xMn+1, when either wide metal of 1xMn or 1xMn+1 with both length $L > 0.18\mu m$ and width $W > 0.18\mu m$, the space between either via and wide metal is $< 1.65\mu m$ (D3, D3 is the shortest running path length from Via to the wide metal).			
1xRVn.8b	There should be at least one rectangular 1x Vn or two square 1x Vns in the intersection area of 1xMn and 1xMn+1, when either wide metal of 1xMn or 1xMn+1 with both length $L > 1\mu m$ and width $W > 1\mu m$, the space between either via and wide metal is $\leq 5\mu m$ (D3, D3 is the distance $\leq 5\mu m$ away from this wide metal).			
1xRVn.8c	There should be at least one rectangular 1x Vn or two square 1x Vns in the intersection area of 1xMn and 1xMn+1, when either wide metal of 1xMn or 1xMn+1 with both length $L > 5\mu m$ and width $W > 1.5\mu m$, the space between either via and wide metal is $\leq 12\mu m$ (D3, D3 is the distance $\leq 12\mu m$ away from this wide metal).			
1xRVn.9^[NC]	It's recommended to use rectangular via which is to avoid high resistance wherever layout allows.			
1xRVn.10	45-degree rotated rectangular 1x Vn is not allowed.			
1xRVn.11	<p>Single rectangular 1xVn is not allowed in "H-shape" 1xMn+1 when:</p> <ol style="list-style-type: none"> The 1xMn+1 has "H-shape" interact with two metal holes: both two metal holes length $\leq 6\mu m$ (L2) and two metal hole area $\leq 6\mu m^2$. The rectangular 1xVn overlaps on the center metal bar of this "H-shape" 1xMn+1. The center metal bar length $\leq 1\mu m$ (L) and the metal bar width $\leq 0.16\mu m$. 			
1xRVn. 12^[R]	<p>Recommended consecutive stacked rectangular 1x Vn layer, which has only one rectangular 1x Vn for each rectangular 1x Vn layer to avoid high Rc.</p> <p>This rule doesn't check MARKS and DUPMK1 region.</p>	\leq	4	

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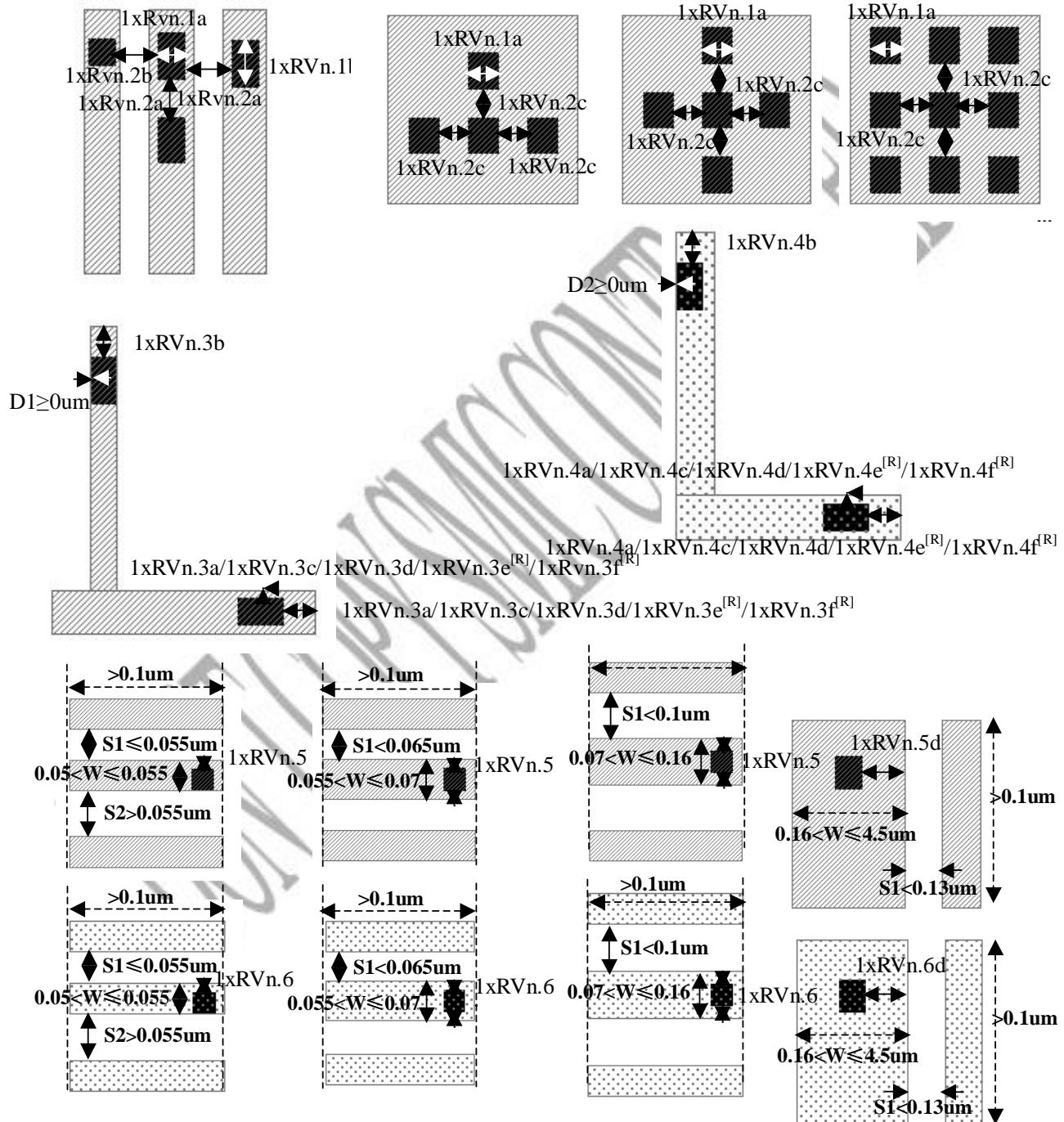
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Rule number	Description	Operation	Design Value	Unit
1xRVn. 13 ^[R]	Recommended space between rectangular 1x Vn and 1xVn+1, where rectangular 1xVn and 1xVn+1 at different net and parallel run length > 0.02um	≥	0.06	um

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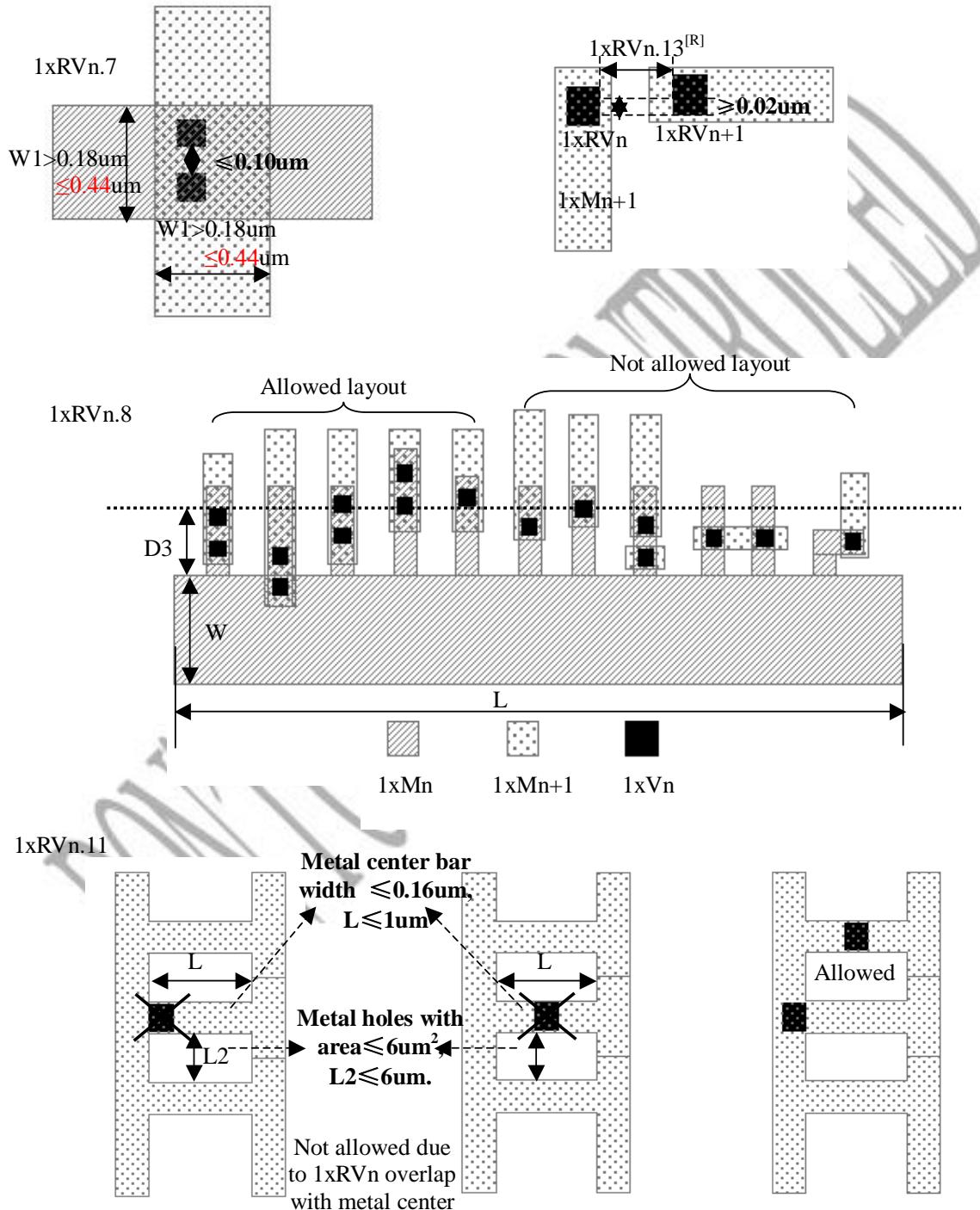
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7.2.25 2x Mn: 2x Metal design rules

Rule number	Description	Operation	Design Value	Unit
2xMn.1	2xMn width.	\geq	0.1	um
		\leq	12	um
2xMn.2a	Width of 45-degree 2xMn	\geq	0.34	um
2xMn.2b	Length of 45-degree 2xMn	\geq	1	um
2xMn.3a	Space between two 2xMns.	\geq	0.1	um
2xMn.3b	Space between two 2xMns when one or both 2xMn widths are >0.2um, and parallel run length of two 2xMns is >0.38um.	\geq	0.12	um
2xMn.3c	Space between two 2xMns when one or both 2xMn widths are >0.4um, and parallel run length of two 2xMns is >0.4um.	\geq	0.16	um
2xMn.3d	Space between two 2xMns when one or both 2xMn widths are >1.5um, and parallel run length of two 2xMns is >1.5um.	\geq	0.5	um
2xMn.3e	Space between two 2xMns when one or both 2xMn widths are >4.5um, and parallel run length of two 2xMns is >4.5um.	\geq	1.5	um
2xMn.4	Space between 2xMns and 2xMn dense line end (the parallel run length >-0.035um). 1. 2xMn line-end definition: 2xMn edge with length < 0.12um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.1um; 2. 2xMn dense line end definition: the space (S1) is <0.12um between any one adjacent edge of 2xMn line end and other 2xMn, other metal must be in the L1 and L2 extension region from metal line end, L1< 0.035um, L2 <0.12um. S1 should be the space between separate metal.	\geq	0.12	um
2xMn.5	Space between 2xMn (M) and 2xMn (N) with the parallel runlength >-0.035um, when space (S2) is <0.12um between 2xMn (N) line end and other 2xMn. 1. 2xMn line-end definition: 2xMn edge with length < 0.12um (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 \geq 0.1um; 2. 2xMn (M) must be in the L1 and L2 extension region from metal line end, L1< 0.035um, L2 <0.12um.	\geq	0.12	um

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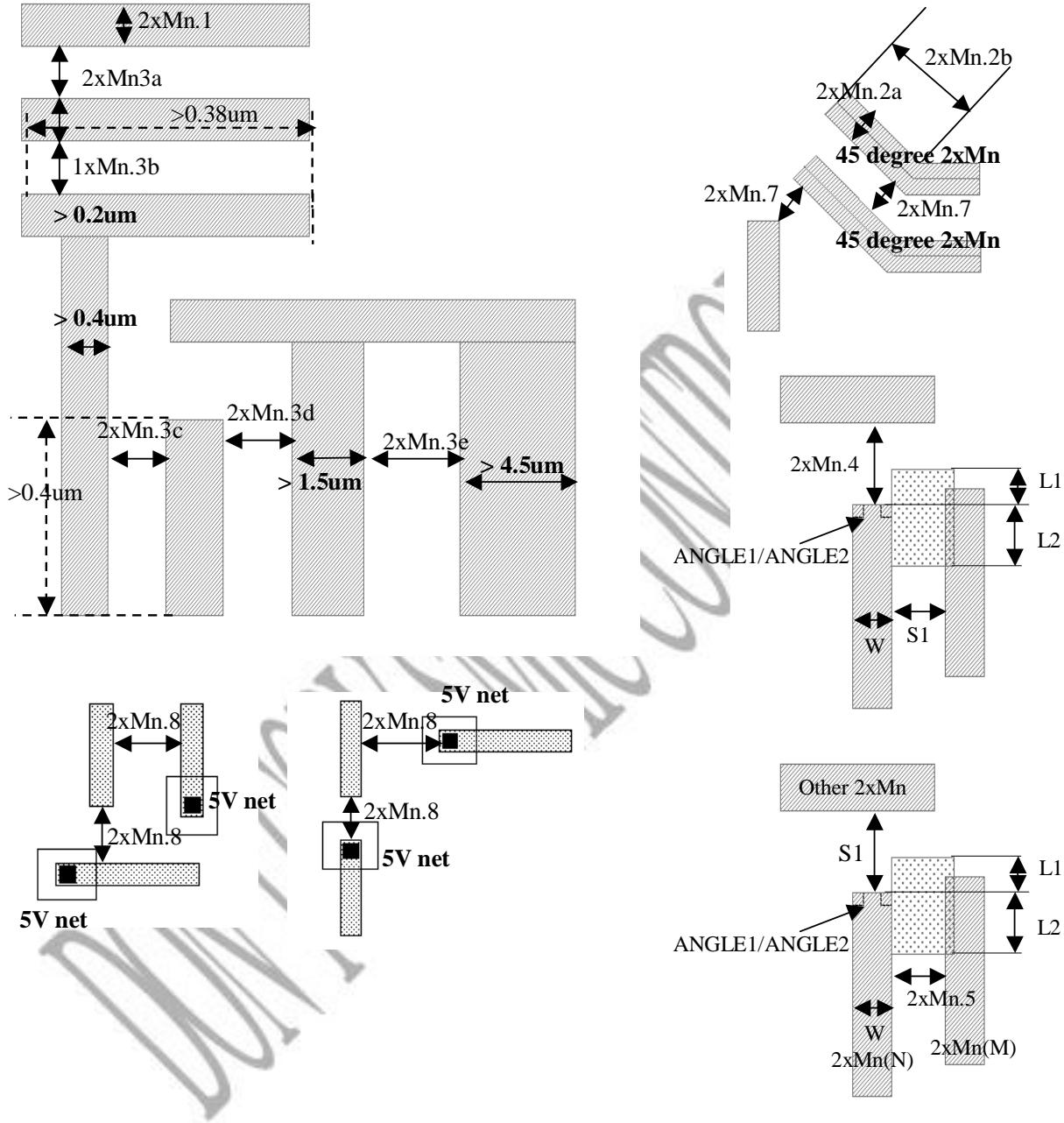


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Rule number	Description	Operation	Design Value	Unit
2xMn.6^[R]	Space between (2xMn or dummy 2xMn). DRC check maximum width of (NOT (2xMn or dummy 2xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LOGO.	\leq	4.5	um
2xMn.7	Space between 45-degree 2xMn and 2xMn	\geq	0.34	um
2xMn.8	Space between two 2xMns when one or both of 2xMn connects to 5V net	\geq	0.16	um
2xMn.9	2xMn area	\geq	0.06	um ²
2xMn.10	Enclosed dielectric area by 2xMn	\geq	0.26	um ²
2xMn.11	2xMn density (including dummy). Density check window size: 125um*125um, step size: 62.5um.	\geq \leq	10% 85%	
2xMn.12	The density difference between any two neighboring checking windows (window 200*200, stepping 200um). DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	\geq	50%	
2xMn.13^[R]	2xMn density (including dummy) in DUMBM and 2xMnDUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMBM/2xMnDUB width is >5um and <125um, where density ratio= 2xMn area/(DUMBM or 2xMnDUB)area.	\geq \leq	10% 85%	
2xMn.14^[NC]	2xMn line-end must be rectangular.			

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7.2.26 2x Vn: 2x Via design rules

Rule number	Description	Operation	Design Value	Unit
2xVn.1	Fixed 2x Vn size (square shape)	=	0.1	um
2xVn.2	Space between 2x Vns	≥	0.1	um
2xVn.3	Space between 2x Vn and its neighboring 2x Vn (T). The definition of neighboring 2x Vn (T) : 1. 2x Vn (T) is in a 2x Vn group 2.The number of this 2x Vn group is ≥4, there are at least three 2x Vns neighboring to 2x Vn (T) 3.The space between 2x Vn (T) to other 2x Vns in this group <0.14um	≥	0.13	um
2xVn.4	Space between two neighbor 2xVns at different net with the parallel run length>0)	≥	0.13	um
2xVn.5	Space between two 2xVns when at least one 2xVn connects to 5V	≥	0.16	um
2xVn.6	2x Vn must be fully covered by 2xMn or 1xMn. Enclosure by 2xMn or 1xMn must follow (2x Vn.6a or 2x Vn.6c or 2x Vn.6d) or (2x Vn.6b) or 2x Vn.6c or 2x Vn.6d) as below.			
2xVn.6a	Enclosure by 2xMn, where 2xMn is the metal layer directly underneath 2x Vn.	≥	0	um
2xVn.6b	Enclosure by 1xMn, where 1xMn is the metal layer directly underneath 2x Vn.	≥	0.02	um
2xVn.6c	Enclosure by 1xMn or 2xMn when enclosure by 1xMn or 2xMn on either perpendicular direction ≥0um and <0.03um and 1xMn or 2xMn is the metal layer directly underneath 2x Vn.	≥	0.04	um
2xVn.6d	Enclosure by 1xMn or 2xMn in four sides, and 1xMn or 2xMn is the metal layer directly underneath 2x Vn.	≥	0.03	um
2xVn.7	2x Vn must be fully covered by 2xMn+1. Enclosure by 2xMn+1 must follow (2x Vn.7a or 2x Vn.7b or 2x Vn.7c) as below.			
2xVn.7a	Enclosure by 2xMn+1, where 2xMn+1 is the metal layer directly above 2x Vn.	≥	0	um
2xVn.7b	Enclosure by 2xMn+1 when enclosure by 2xMn+1 on either perpendicular direction ≥0um and <0.03um and 1xMn is the metal	≥	0.04	um

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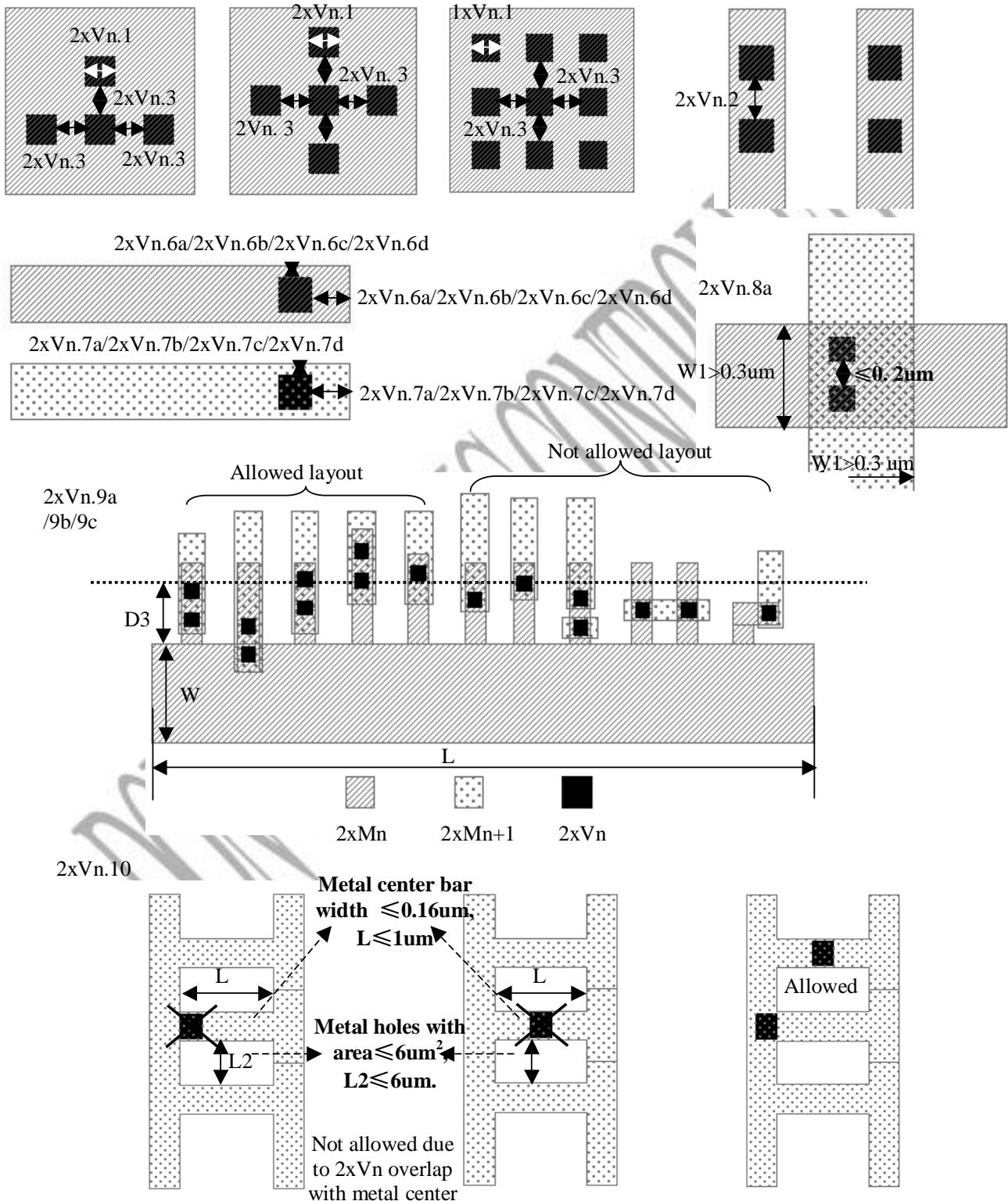


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Rule number	Description	Operation	Design Value	Unit
	layer directly above 2x Vn.			
2xVn.7c	Enclosure by 2xMn+1 in four sides, and 2xMn+1 is the metal layer directly above 2x Vn.	\geq	0.03	um
2xVn.8a	There should be at least two 2x Vns with space $\leq 0.2\text{um}$ (S1) or at least four 2xVns with space $\leq 0.25\text{um}$ (S2) in 2x Mn and 2x Mn+1 intersection area, when either 2x Mn and 2x Mn+1 width and length (W1) $> 0.3\text{um}$ and $\leq 0.7\text{um}$.			
2xVn.8b	There should be at least two 2x Vns with space $\leq 0.2\text{um}$ (S1) or at least four 2xVns with space $\leq 0.35\text{um}$ (S2) in 2x Mn and 2x Mn+1 intersection area, when either 2x Mn and 2x Mn+1 width and length (W1) $> 0.7\text{um}$.			
2xVn.9a	There should be at least two 2x Vn in the intersection area of 2xMn and 2xMn+1, when either wide metal of 2xMn or 2xMn+1 with both length L $> 0.3\text{um}$ and width W $> 0.3\text{um}$, the space between either via and wide metal is $\leq 0.8\text{um}$ (D3, D3 is the shortest running path length from Via to the wide metal).			
2xVn.9b	There should be at least two 2x Vn in the intersection area of 2xMn and 2xMn+1, when either wide metal of 2xMn or 2xMn+1 with both length L $> 2\text{um}$ and width W $> 2\text{um}$, the space between either via and wide metal is $\leq 2\text{um}$ (D3, D3 is the shortest running path length from Via to the wide metal).			
2xVn.9c	There should be at least two 2x Vn in the intersection area of 2xMn and 2xMn+1, when either wide metal of 2xMn or 2xMn+1 with both length L $> 10\text{um}$ and width W $> 3\text{um}$, the space between either via and wide metal is $\leq 5\text{um}$ (D3, D3 is the shortest running path length from Via to the wide metal).			
2xVn.10	Single 2xVn is not allowed in "H-shape" 2xMn+1 when: 1. The 2xMn+1 has "H-shape" interact with two metal holes: both two metal holes length $\leq 6\text{um}$ (L2) and two metal hole area $\leq 6\text{um}^2$. 2. The 1xVn overlaps on the center metal bar of this "H-shape" 2xMn+1. 3. The center metal bar length $\leq 1\text{um}$ (L) and the metal bar width $\leq 0.3\text{um}$.			
2xVn.11 ^[NC]	It's recommended to use redundant vias to avoid high resistance wherever layout allows.			
2xVn.12	45-degree rotated 2x Vn is not allowed.			

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7.2.27 8x TVn: 8x Via(TV1/TV2) design rules

Rule number	Description	Operation	Design Value	Unit
8xTVn.1	Fixed 8x TVn size (square shape).	=	0.36	um
8xTVn.2a	Space between single 8x TVns.	\geq	0.34	um
8xTVn.2b	Space between 8x TVn and its neighboring 8x TVn (T). The definition of neighboring 8x TVn (T) : 1. 8x TVn (T) is in a 8x TVn group 2.The number of this 8x TVn group is ≥ 4 , there are at least 3 8x TVn s neighboring to 8x TVn (T) 3.The space between 8x TVn (T) to other 8x TVn s in this group <0.56um	\geq	0.54	um
8xTVn.3	8x TVn fully enclosure by 1x Mn/2x Mn /8x TM, where 1x Mn/2x Mn /8x TM is the metal layer directly underneath 8x TVn. 8x TVn must be fully enclosed by 1x Mn/2x Mn /8x TM	\geq	0.02	um
8xTVn.4	Enclosure by 1x Mn/2x Mn /8x TM when enclosure by 1x Mn/2x Mn /8x TM on either perpendicular direction ≥ 0.02 um, and 1x Mn/2x Mn /8x TM is the metal layer directly underneath 8x TVn.	\geq	0.08	um
8xTVn.5	8x TVn fully enclosure by 8x TM , where 8x TM is the metal layer directly above 8x TVn. 8x TVn must be fully enclosed by 8x TM	\geq	0.02	um
8xTVn.6	Enclosure by 8x TM when enclosure by 8x TM on either perpendicular direction ≥ 0.02 um, and 8x TM is the metal layer directly above 8x TVn.	\geq	0.08	um
8xTVn.7	There should be at least two 8x TVns with space ≤ 1.6 um (S1) in 8x TMn and 8x TMn+1 intersection area, when either 8x TMn or 8x TMn+1 width and length (W1) > 1.7 um.			
8xTVn.8	There should be at least two 8x TVns in the intersection area of 8xMn and 8xMn+1, when either wide metal of 8xTMn or 8xTMn+1 with both length L>10um and width W>3um, the space between either via and wide metal is ≤ 6 um (D3, D3 is the shortest running path length from 8xTVn to the wide metal).			

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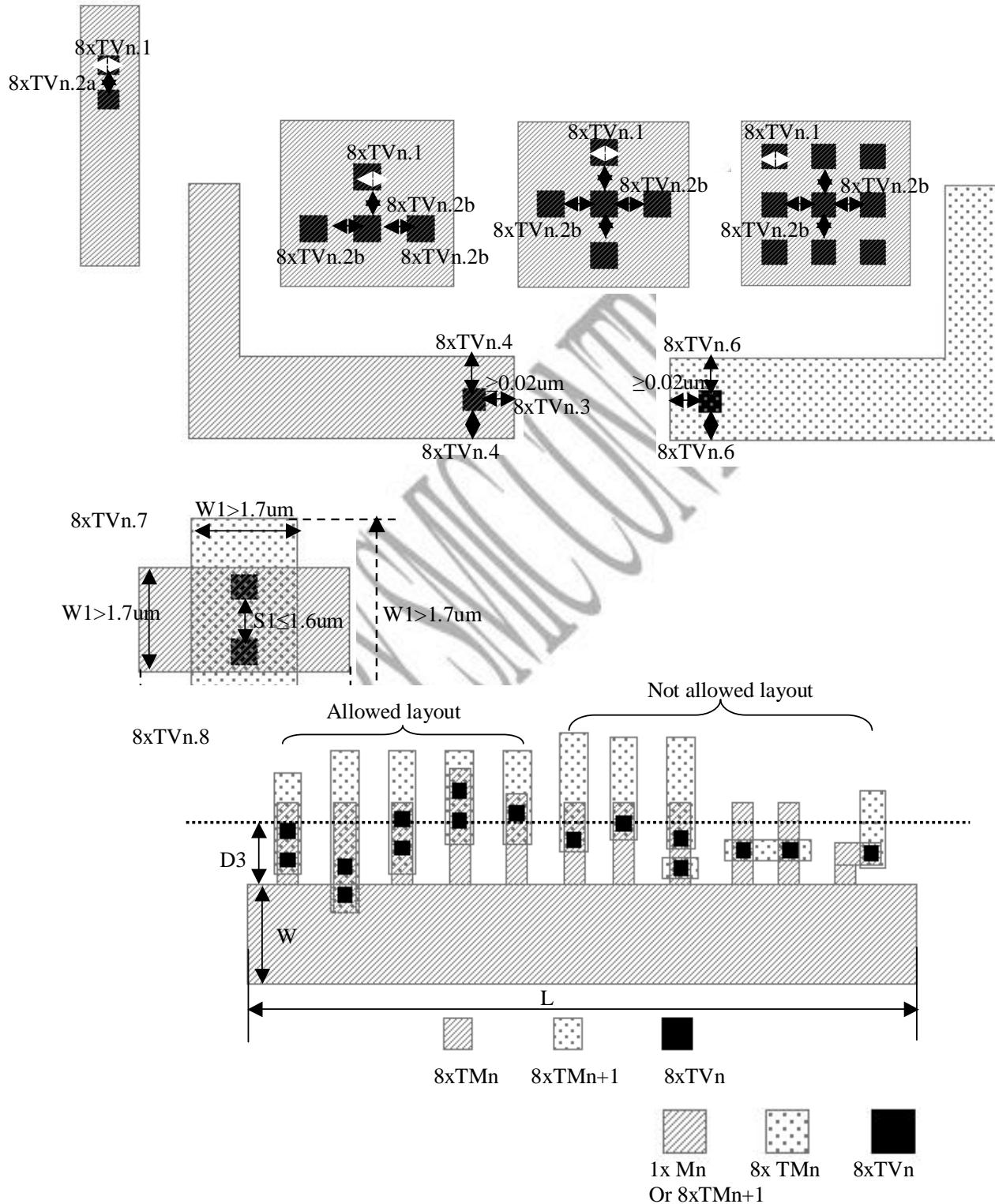


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Rule number	Description	Operation	Design Value	Unit
8xTVn.9	45-degree rotated 8x TVn is not allowed.			
8xTVn.10^[NC]	Recommend to use redundant vias to avoid high Rc wherever layout allows.			
8xTVn.11^[NC]	8x TVn and 10xTVn can't be used on same chip.			

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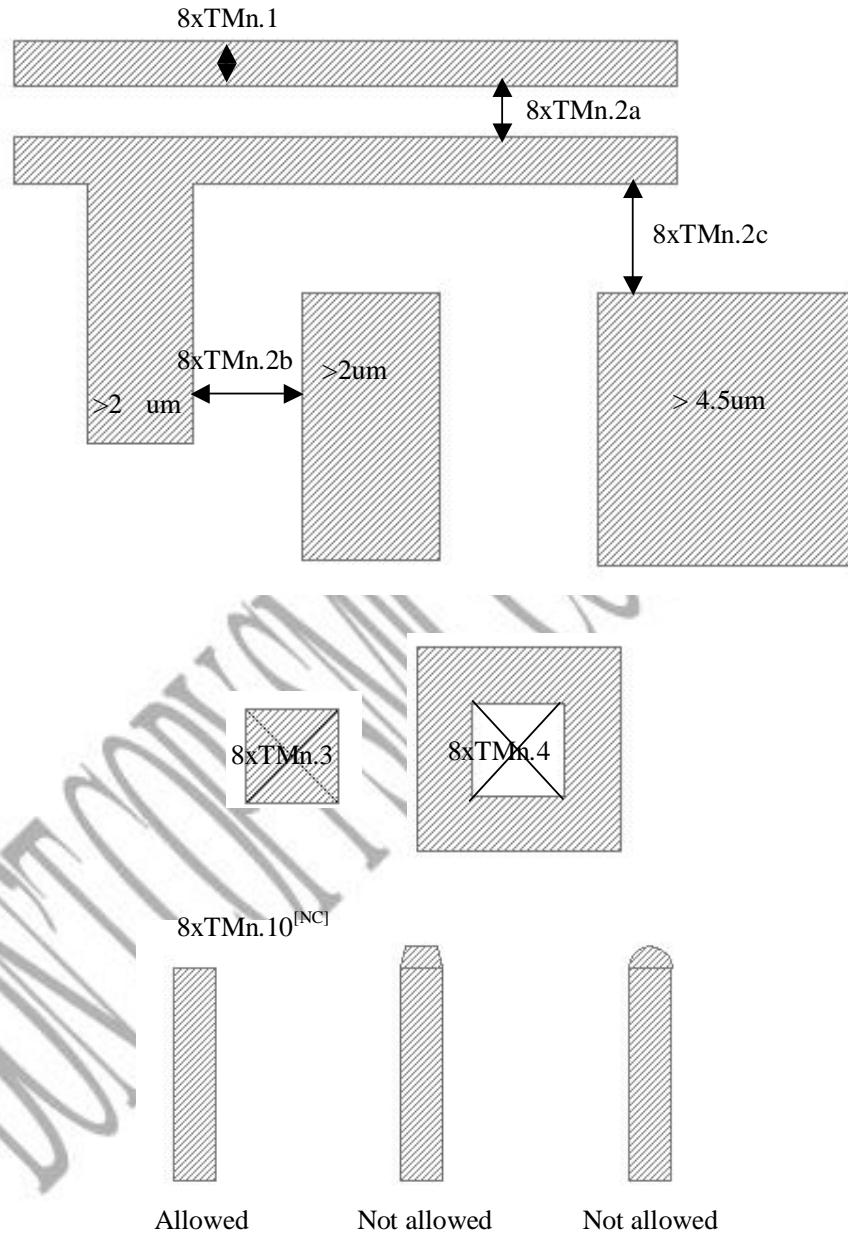
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7.2.28 8x TMn : 8x Metal (TM1 /TM2) design rules

Rule number	Description	Operation	Design Value	Unit
8xTMn .1	8x TMn width. Maximum width DRC doesn't check PAD, DUPMK1 and INDMY region.	\geq	0.4	um
		\leq	12	um
8xTMn .2a	Space between 8x TMns.	\geq	0.4	um
8xTMn .2b	Space between two 8x TMns that have a parallel run length >1.5um when at least one 8x TMn widths are >1.5um.	\geq	0.5	um
8xTMn .2c	Space between two 8x TMns that have a parallel run length >4.5um when at least one 8x TMn widths is >4.5um.	\geq	1.2	um
8xTMn .2d^[R]	Space between (8x TMn or dummy 8x TMn) DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	\leq	12	um
8xTMn .3	8x TMn area	\geq	0.56	um ²
8xTMn .4	Dielectric area enclosed by 8x TMn	\geq	0.572	um ²
8xTMn .5	8xTMn density (including dummy).Density check window size: 125um*125um, step size: 62.5um (exclude DUPMK1 region).	\geq	10%	
		\leq	85%	
8xTMn .5^[R]	8xTMn density (including dummy) in DUMB and TMnDUB. Density check window size: 125um*125um, step size: 62.5um (exclude DUPMK1 region). DRC need check the design if DUMB/TMnDUB width is >5um and <125um, where density ratio= 8xTMn area/(DUMB or TMnDUB)area.	\geq	10%	
		\leq	85%	
8xTMn .6^[R]	TMn density (including dummy) in full chip	\geq	20%	
8xTMn .7	The density difference between any two neighbouring checking windows (window 200*200, stepping 200um).	\leq	50%	
8xTMn .8^[NC]	8xTMn line-end must be rectangular. Other shaped are not allowed.			
8xTMn .9^[NC]	8x TMn and 10xTMn can't be used on same chip.			

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7.2.29 10x TVn: 10x Via(TV1/TV2) design rules

Rule number	Description	Operation	Design Value	Unit
10xTVn.1	Fixed 10x TVn size (square shape).	=	0.46	um
10xTVn.2a	Space between single 10x TVns.	\geq	0.44	um
10xTVn.2b	Space between 10x TVns in 2x2 10x TVns array at the same net. Two vias whose space $\leq 0.55\text{um}$ are considered to be in the same array.	\geq	0.54	um
10xTVn.2c	Space between 10x TVn and its neighboring 10x TVn (T). The definition of neighboring 10x TVn (T) : 1. 10x TVn (T) is in a 10x TVn group 2.The number of this 10x TVn group is ≥ 4 , there are at least 3 10x TVns neighboring to 10x TVn (T) 3.The space between 10x TVn (T) to other 10x TVns in this group $\leq 0.66\text{um}$	\geq	0.66	um
10xTVn.3	10x TVn enclosure by 1x Mn/2x Mn/10x TMn , where 1x Mn/2x Mn/10x TMn is the metal layer directly underneath 10x TVn. 10x TVn must be fully covered by 1x Mn/2x Mn/10x TMn	\geq	0.02	um
10xTVn.4	Enclosure by 1x Mn/2x Mn/10x TMn when enclosure by 1x Mn/2x Mn/10x TMn on either perpendicular direction $\geq 0.02\text{um}$, and 1x Mn/2x Mn/10x TMn is the metal layer directly underneath 10x TVn.	\geq	0.08	um
10xTVn.5	10x TVn enclosure by 10x TMn , where 10x TMn is the metal layer directly above 10x TVn. 10x TVn must be fully enclosed by 10x TMn	\geq	0.02	um
10xTVn.6	Enclosure by 10x TMn when enclosure by 10x TMn on either perpendicular direction $\geq 0.02\text{um}$, and 10x TMn is the metal layer directly above 10x TVn.	\geq	0.08	um
10xTVn.7	At least two 10xTVns with space $\leq 1.6\text{um}$ (S1) in 10x TMn and 10x TMn+1 intersection area, when either 10x TMn or 10x TMn+1 width and length (W1) $> 1.7\text{um}$.			
10xTVn.8	There should be at least two 10xTVn in the intersection area of 10xTM and 10xTM+1 , when either wide metal of 10xTM or 10xTM+1 with both length $L > 10\text{um}$ and width $W > 3\text{um}$, the space between either via and wide			

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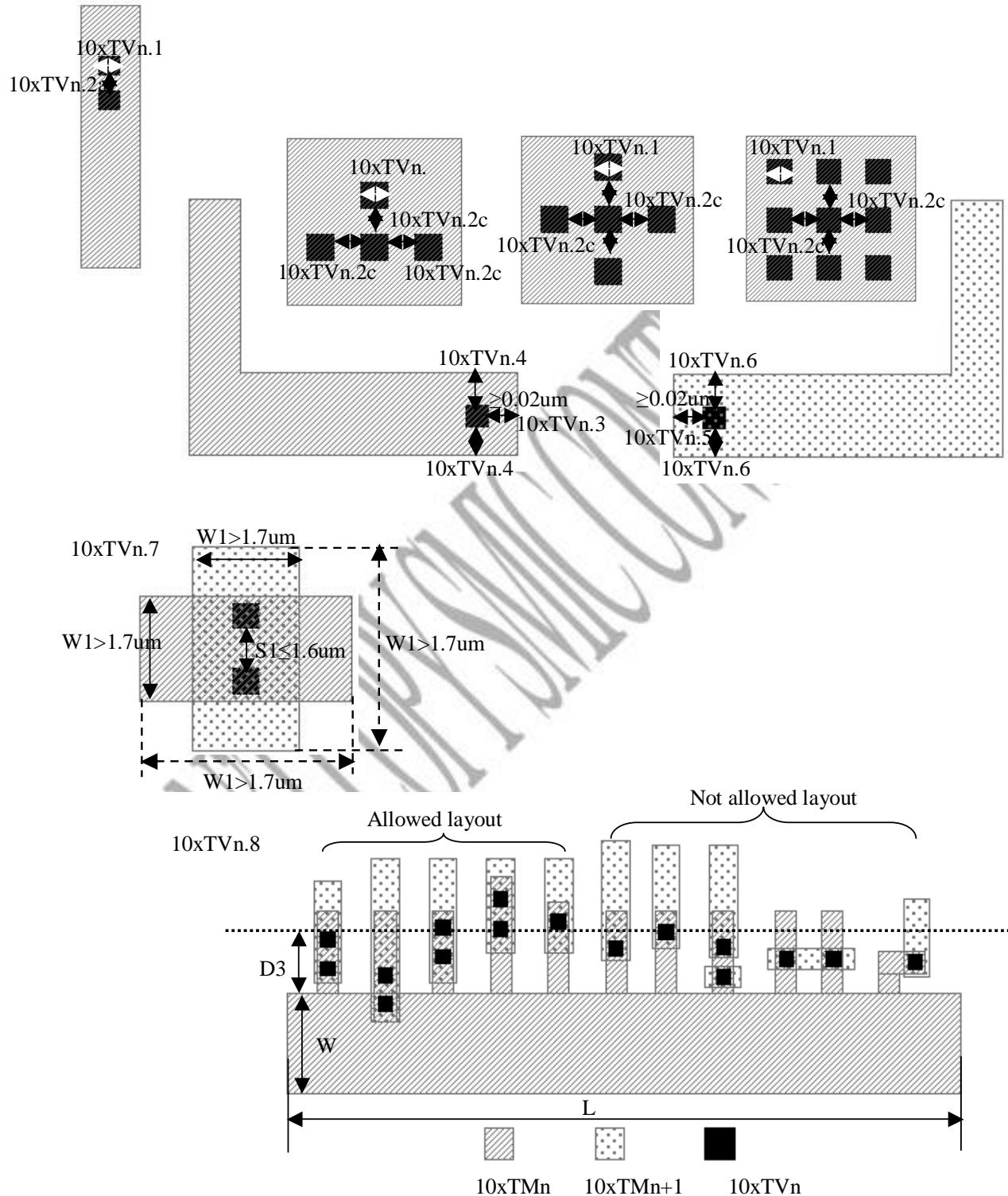


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Rule number	Description	Operation	Design Value	Unit
	metal is \leq 6um (D3, D3 is the distance 5um away from this wide metal).			
10xTVn.9	45-degree rotated 10x TVn is not allowed.			
10xTVn.10^[NC]	Recommend to use redundant vias to avoid high Rc wherever layout allows.			

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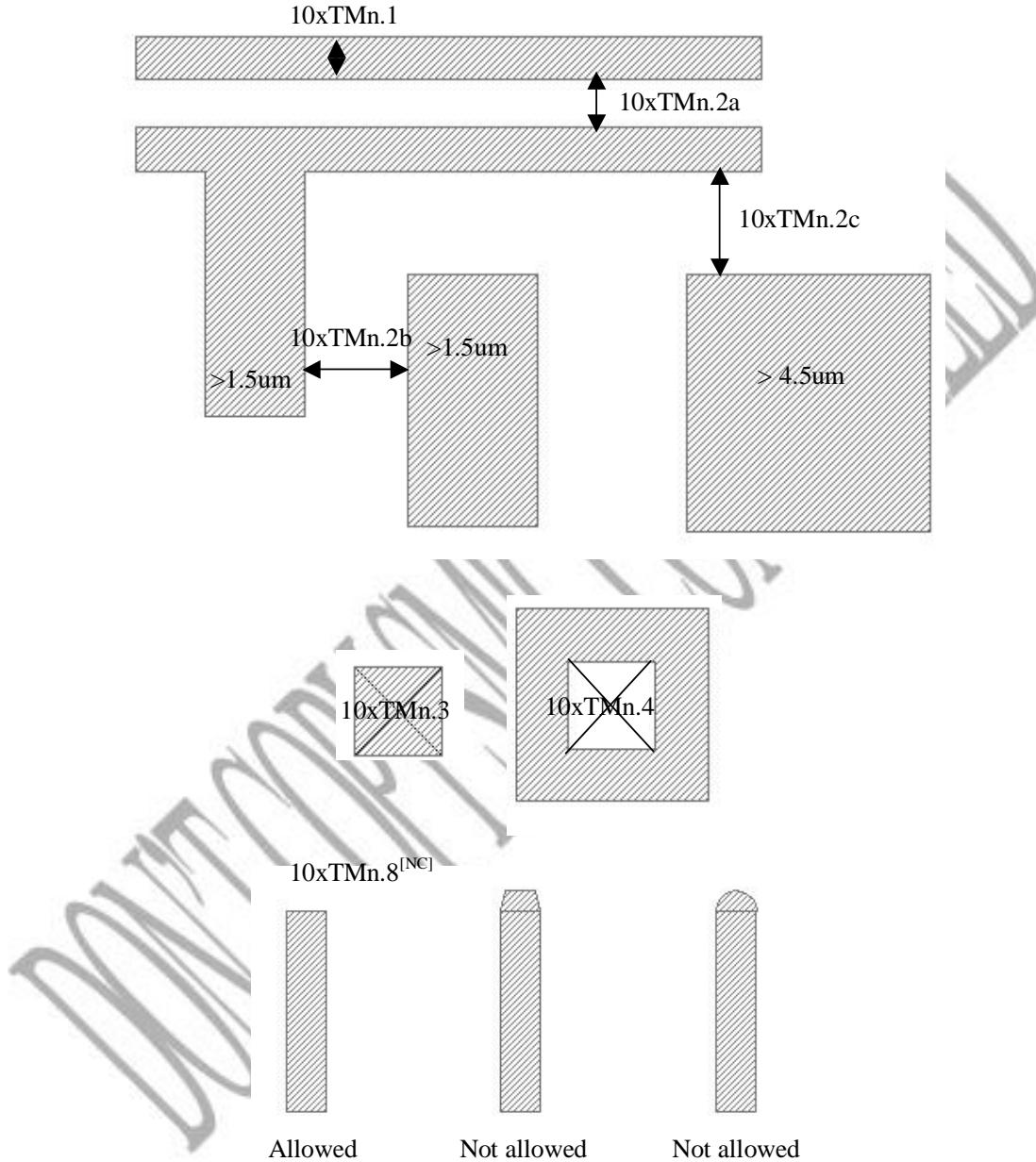
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7.2.30 10xTMn : 10x Metal (TM1 /TM2) design rules

Rule number	Description	Operation	Design Value	Unit
10xTMn .1	10x TMn width.	\geq	0.5	um
	Maximum width DRC doesn't check PAD and DUPMK1 and INDMY region.	\leq	12	um
10xTMn .2a	Space between 10x TMns.	\geq	0.5	um
10xTMn .2b	Space between two 10x TMns that have a parallel run length >1.5um when at least one 10x TMn widths are >1.5um.	\geq	0.65	um
10xTMn .2c	Space between two 10x TMns that have a parallel run length >4.5um when at least one 10x TMn widths is >4.5um.	\geq	1.5	um
10xTMn .2d^[R]	Space between (10xTMn or dummy 10xTMn) DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	\leq	12	um
10xTMn .3	10x TMn area	\geq	1	um ²
10xTMn .4	Dielectric area enclosed by 10x TMn	\geq	2.5	um ²
10xTMn .5	10xTMn density (including dummy).Density check window size: 125um*125um, step size: 62.5um (exclude DUPMK1 region).	\geq	10%	
		\leq	85%	
10xTMn .6^[R]	10xTMn density (including dummy) in DUMB and TMnDUB. Density check window size: 125um*125um, step size: 62.5um (excluding DUPMK1 region). DRC need check the design if DUMB/TMnDUB width is >5um and <125um, where density ratio= 10xTMn area/(DUMB or TMnDUB)area.	\geq	10%	
		\leq	85%	
10xTMn .7	The density difference between any two neighbouring checking windows (window 200*200um, stepping 200um).	\leq	50%	
10xTMn .8^[NC]	10xTMn line-end must be rectangular.			

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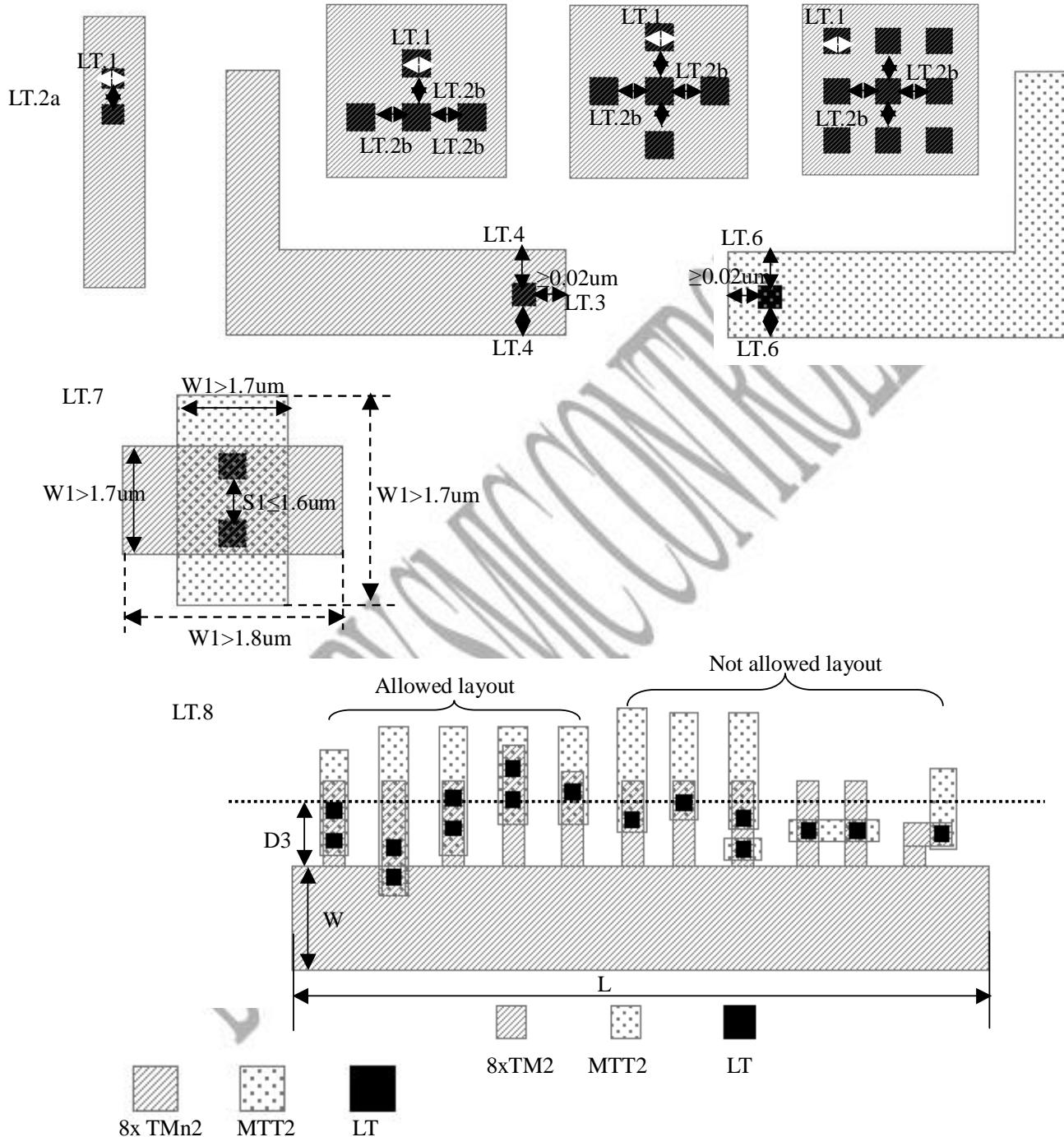
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7.2.31 8x UTV: 8x UTV(LT) design rules

Rule number	Description	Operation	Design Value	Unit
LT.1	Fixed LT size (square shape).	=	0.36	um
LT.2a	Space between single LTs.	\geq	0.34	um
LT.2b	Space between LT and its neighboring LT (T). The definition of neighboring LT (T) : 1. LT (T) is in a LTgroup 2.The number of this LT group is ≥ 4 , there are at least 3 LT s neighboring to LT (T) 3.The space between LT (T) to other LT s in this group <0.56um	\geq	0.54	um
LT.3	(Purposely blank)			
LT.4	Enclosure by 1x Mn/2x Mn/8x TM1, 1x Mn/2x Mn/8x TM1 is the metal layer directly underneath LT.	\geq	0.08	um
LT.5	(Purposely blank)			
LT.6	Enclosure by MTT2 when enclosure by MTT2	\geq	0.08	um
LT.7	There should be at least two LTs with space $\leq 1.6\text{um}$ (S1) in 8x TM1 and MTT2 intersection area, when either 8x TM1 or MTT2 width and length (W1) $> 1.7\text{um}$.			
LT.8	There should be at least two LTs in the intersection area of 8x TM1 and MTT2, when either wide metal of 8x TM1 or MTT2 with both length L $> 10\text{um}$ and width W $> 3\text{um}$, the space between either via and wide metal is $\leq 6\text{um}$ (D3, D3 is the shortest running path length from Via to the wide metal).			
LT.9	45-degree rotated LT is not allowed.			
LT.10^[NC]	Recommend to use redundant vias to avoid high Rc wherever layout allows.			

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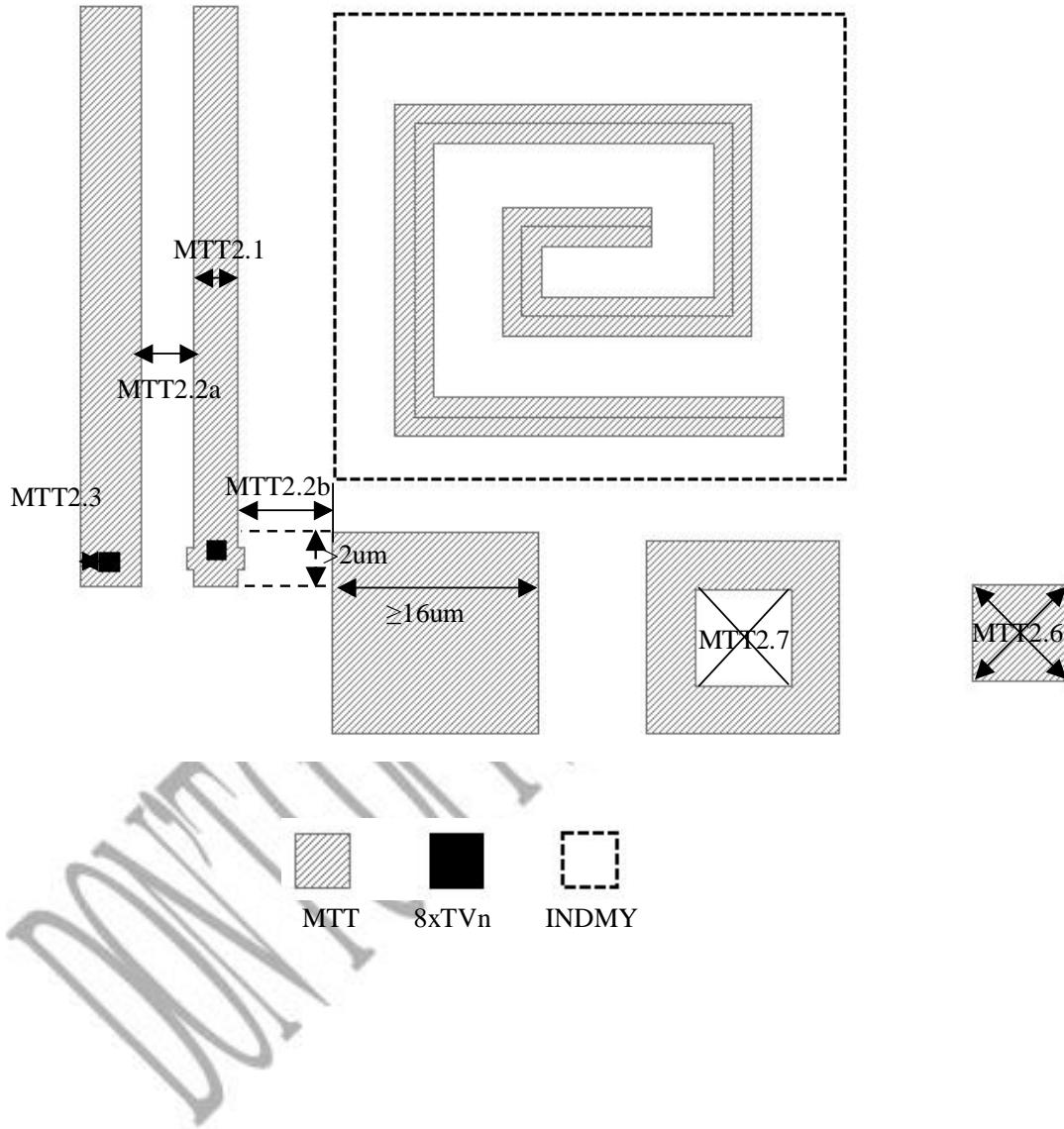
7.2.32 MTT2: MTT2 design rules (ultra-thick metal)

MTT2 design rules are only used for ultra-thick top metal (3.35um).

Rule number	Description	Operation	Design Value	Unit
MTT2.1	MTT2 width	\geq	2	um
MTT2.2a	Space between two MTT2 regions.	\geq	1	um
MTT2.2b	Space between two MTT2s having parallel segment larger than 2um with one or both MTT2 width larger than or equal to 16um.	\geq	2	um
MTT2.3	(Purposely blank)			
MTT2.4	(Purposely blank)			
MTT2.5	(Purposely blank)			
MTT2.6	MTT2 Area (um ²).	\geq	9	um ²
MTT2.7	Dielectric area enclosed by MTT2 (in um ²).	\geq	9	um ²
MTT2.8	Density of MTT2 (including dummy). Density check window size: 125um*125um, step size: 62.5um, exclude: 1. DUPMK1 region 2. Chip corner and seal ring. 3. LOGO/INDMY.	\geq \leq	10% 85%	
MTT2.9	MTT2 density in full chip(including dummy, not including INDMY region)	\geq \leq	20% 55%	
MTT2.10	(Purposely blank)			
MTT2.11	(Purposely blank)			
MTT2.12	(Purposely blank)			
MTT2.13^[NC]	(Purposely blank)			
MTT2.14	MTT2 line width allowed. DRC doesn't check the MTT2 underneath of MD, DUPMK1 and INDMY region	\leq	12	um
MTT2.15^[NC]	MTT2 line-end must be rectangular.			

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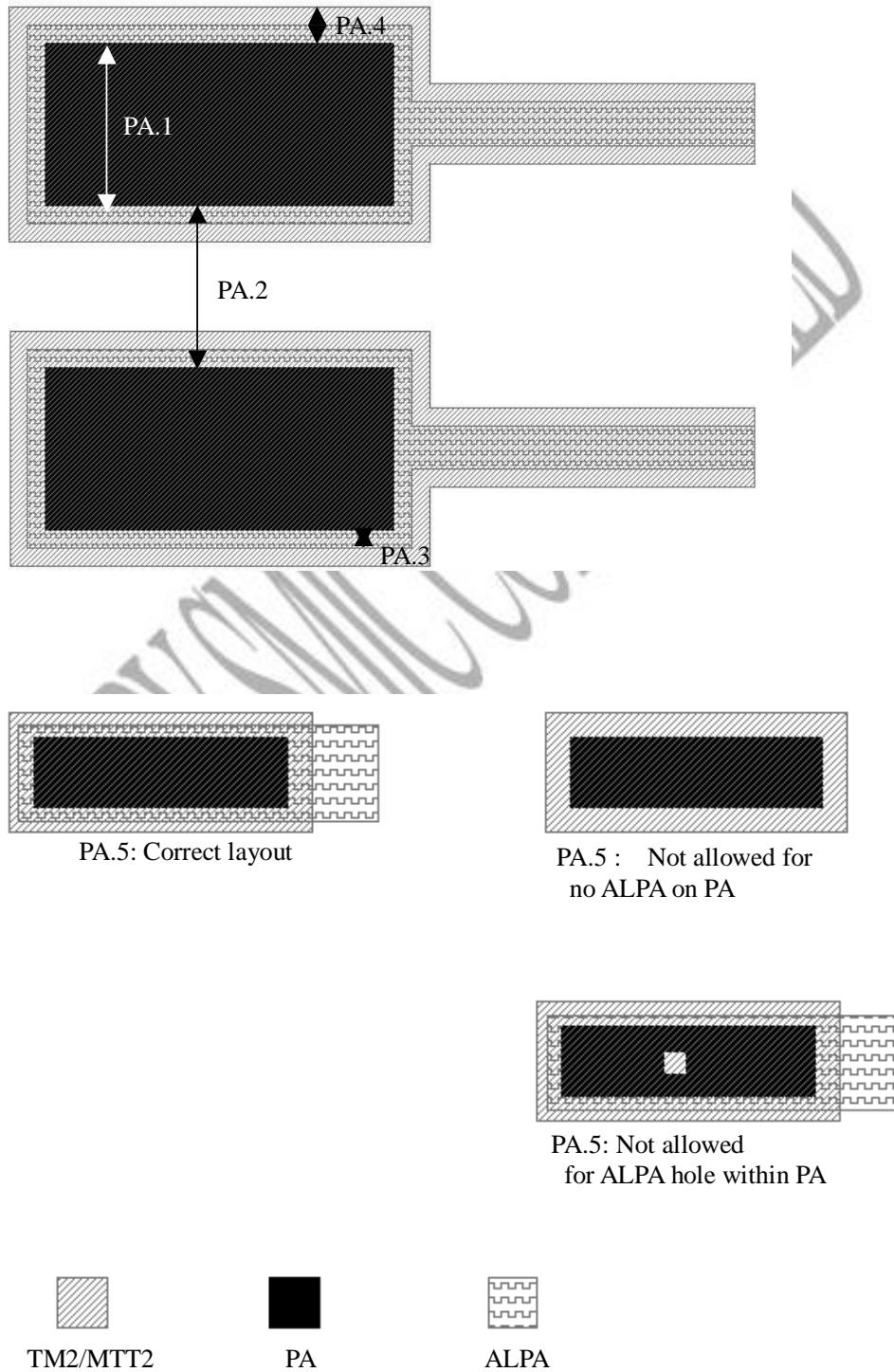
7.2.33 PA: Passivation 1 design rules

Passivation 1 can be used for pad opening and AL RDL via opening.

Rule Number	Description	Operation	Design Value	Unit
PA.1	PA width	\geq	2	um
PA.2	Space between two PA	\geq	2	um
PA.3	ALPA enclosure of PA	\geq	0.5	um
PA.4	TM2, MTT2 enclosure of PA	\geq	0.5	um
PA.5	PA without ALPA above it is not allowed.			
PA.6	45-degree rotated PA is not allowed (except INDMY)			

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7.2.34 ALPA design rules

ALPA layers can be used to draw Al inter-connect lines (ALRDL), Al fuse metal lines, Al bumping pads, and re-distribution Al pads.

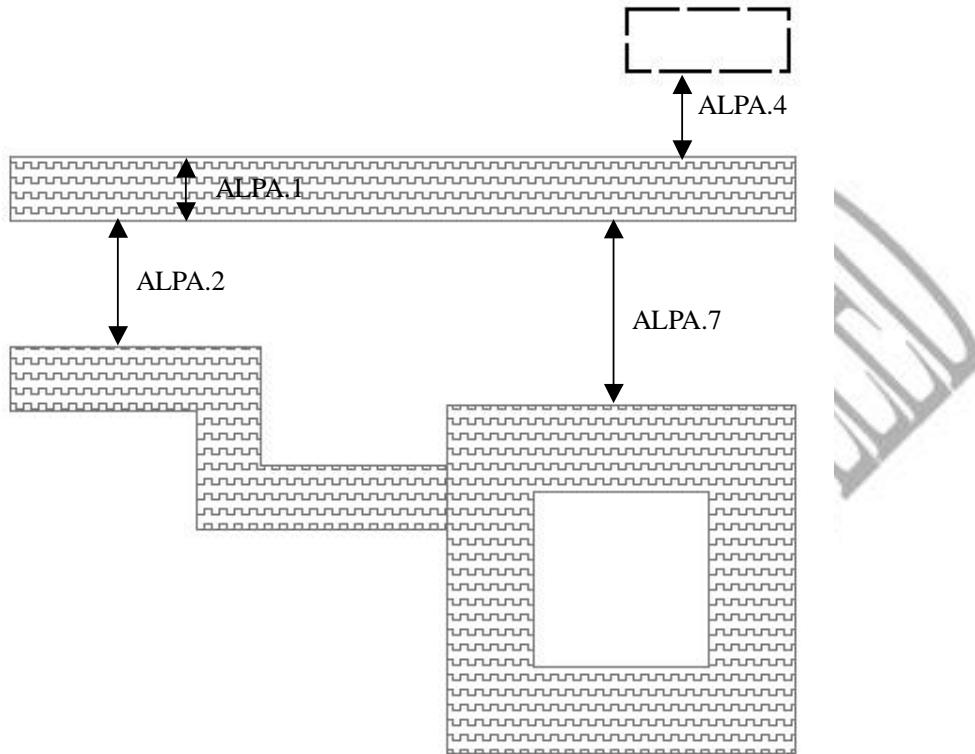
Rule number	Description	Operation	Design Value	Unit
ALPA.1	ALPA width.	\geq	2	um
ALPA.2	ALPA space. <i>DRC doesn't check the space in the same polygon.</i>	\geq	2	um
ALPA.3^[R]	ALPA density (including dummy) with 100um*100um window, with exemption of interacting inductor.	\geq	10%	
ALPA.4^{[R][NC]}	Space between ALRDL and L mark window.	\geq	10	um
ALPA.5	ALPA density (including dummy).	\geq	10%	
ALPA.6	ALPA density (including dummy).	\leq	70%	
ALPA.7	Space between (ALPA AND (MD sizing up 3um)) and (ALPA AND (MD sizing up 3um)) or ALRDL. ALRDL is defined as ALPA layer width equal or smaller than 35um. <i>This rule doesn't check the space in the same polygon.</i>	\geq	2.5	um
ALPA.8^[NC]	ALPA must be drawn layer.			
ALPA.9^[NC]	ALPA includes ALPA Pad and ALRDL. ALRDL is defined as ALPA layer width equal or smaller than 35um. ALPA pad is defined as ALPA layer width larger than 35um.			

Note:

1. In addition to the design rules above, the PA design rules must be observed.

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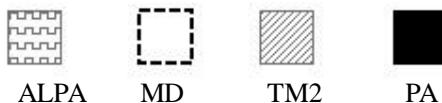
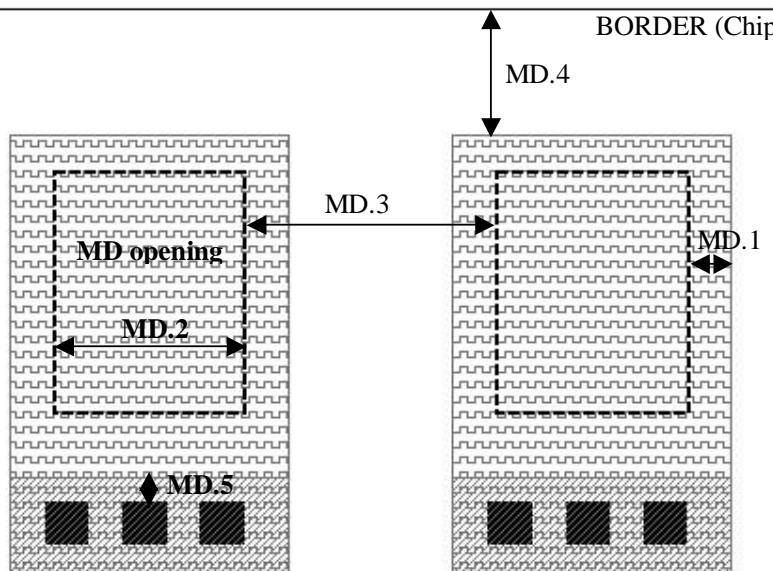
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7.2.35 MD(Passivation 2) design rules

MD is used for opening of Al redistributed patterns. MD should follow the rules below.

Rule number	Description	Operation	Design Value	Unit
MD.1	MD enclosure by ALPA.	\geq	1	um
MD.2	MD width	\geq	14	um
MD.3	MD space	\geq	5	um
MD.4^[R]	MD must be within BORDER (chip edge)	\geq	8	um
MD.5	Space between MD and PA Space=0 is allowed	\geq	1.7	um
MD.6^[R]	(Purposely blank)			
MD.7	Inductor is prohibited under MD wire-bond pad opening		-	
MD.8^[NC]	MD must be a drawn layer			
MD.9	MD is prohibited to interact with PA(PA size <3um)			



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7.2.36 DUP(Device Under Pad) design rules

DUPMK1 (89;156) is the marking layer for DUP pad.

DUP pad area in below rules is (DUPMK1 AND MD).

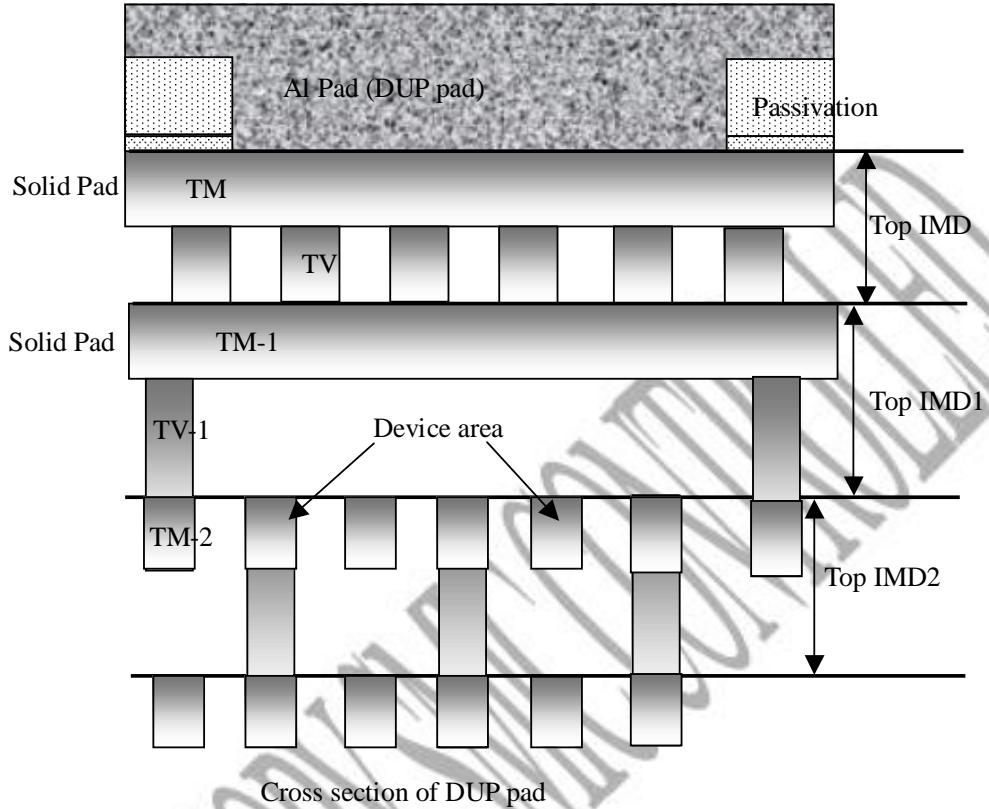
Rules Number	Description	Operation	Layout Value	Unit
DUP.1	For MD that interacts with DUPMK1, this piece of MD must be fully covered by DUPMK1.			
DUP.2	Two metal layers (TM and TM-1) are needed between DUP pad and device, where the metal design must be solid.			
DUP. 2a ^[NC]	It's not allowed to add metal slots for TM and TM-1 under the DUP pad opening area.			
DUP.3 ^[NC]	Device must be located underneath TM-1 layer.			
DUP.4	TV-1 pattern is not allowed under the DUP pad opening area.			
DUP.5	TV array (minimum 3*3) must be drawn between TM and TM-1 layer under the DUP pad opening area. Two Via areas whose space is within 0.70um are considered to be in the same array for 10xTV process. It's required to follow TV space general rule 10xTVn.2c to draw TV array at the DUP pad opening area.			

Notes:

1. TM is TM2 or MTT2.
2. TM-1 is directly underneath TM layer, it can be inter-metal (Mn) or TM1.
3. TV is TV2. TV-1 is directly underneath TV layer, it can be inter-via (Vn) or TV1.

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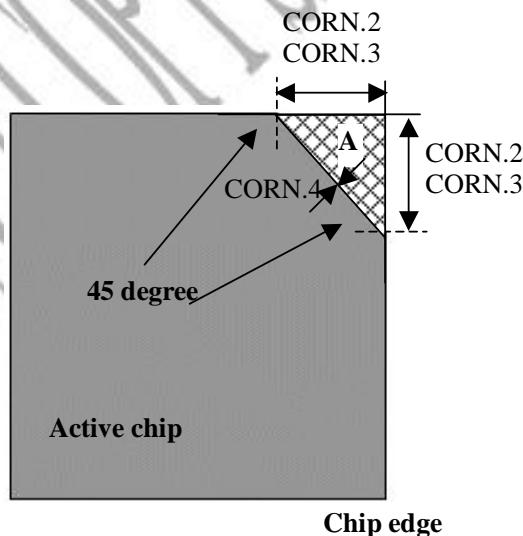
7.2.37 Chip corner Rules

This section describes the chip corner requirements to prevent the chip design interferes with seal ring.

Rule number	Description	Operation	Design Value	Unit
CORN.1	NODMF is dummy block layer for chip corner chamfer area A, and must fully cover chamfer area A.			
CORN.2	Chamfer area A size at the chip corner.	\geq	70	um
CORN.3	Chamfer area A size must be same as NODMF size.			
CORN.4	Space between NODMF and BORDER (127;0) before seal ring insertion.	=	0	um
CORN.5	The layers (listed in Note1) should not overlap with chamfer area A (excluding MARKS covered region).			

Notes:

1. The DRC executes this section rule check on following layers: AA, AADMP, DNW, NW, PSUB, **LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, UHVT_N, UHVT_P**, DG, TG, GT, GTDMP, GTMK2, P2, SN, SP, SAB, CT, M1, 1xMn, 1xVn, 2xMn, 2xVn, 8xTVn, 8xTMn, 10xTVn, 10xTMn, **LT, MTT2, PA, ALPA, MD, BORDER**.
2. This rule section only applies for those chips that need have seal ring insertion. The chip corner rule check option is default turned on in DRC script.
3. In case for the building block/IP level design, or the chip level design with seal ring already inserted, please turn off the chip corner rule check option.



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7.2.38 BORDER(Chip edge) layer design rule

BORDER layer is used to define chip edge. Designers must draw BORDER layer following BORDER design rules below.

Rules Number	Description	Operation	Design Value	Unit
BD.1	The BORDER layer must cover the layers layout patterns (listed in Note1), which all chip layout patterns include seal ring if seal ring has been added by designers.			
BD.2	BORDER must fully cover the layers layout patterns except DNW (listed in Note1) if it needs SMIC to add seal ring.	\geq	0.32	um
BD.3	BORDER must fully cover DNW if it needs SMIC to add seal ring.	\geq	0.45	um
BD.4^[NC]	BORDER layer size should be exact same with the seal ring window edge if seal ring has been added by designers.			
BD.5	Enclosure of seal ring outer ring outline edge by BORDER layer if seal ring has been added by designers.	$=$	5	um
BD.6^[NC]	BORDER layer size should be exact same with chip window size in LDDI form (chip window size when tape-out).			
BD.7^[NC]	BORDER layer rules BD.1~ BD.6 are only for chip level design rules; DRC does not check IP level BORDER.			

Notes:

1. The DRC executes this section rule check on following layers: AA, AADMP, DNW, NW, PSUB, **LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, UHVT_N, UHVT_P**, DG, TG, GT, GBU15, GBD20, GTDMP, P2, SN, SP, SAB, P4, CT, M1, 1xMn, 1xVn, **2xMn, 2xVn, 8xTVn, 8xTMn, 10xTVn, 10xTMn, LT, MTT2, PA, ALPA, MD**.
2. DRC runset provides switch for BORDER rule DRC check, which is turn-on by default, this switch can be turn-off for IP level DRC check.

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7.2.39 AA resistor design rules

RESAA is the marking layer for AA resistor. AA resistor must within RESAA layer. DIFRES is the LVS marking layer for AA resistor.

Non-Silicide AA resistor: (((AA AND RESAA) AND DIFRES) AND SAB)

Silicide AA resistor: (((AA AND RESAA) AND DIFRES) NOT INTERACT SAB)

Rule Number	Description	Operation	Design Value	Unit
RESAA.1	Resistor width, suggest resistor square number (length/width ratio) ≥ 1 for stable resistance.	\geq	0.4	um
		\leq	3	um
RESAA.2	AA resistor length	\geq	0.4	um
		\leq	100	um
RESAA.3	GTDM must to be drawn in RESAA region.			
RESAA.4	Width of GTDM within RESAA	\geq	0.15	um
RESAA.5a	The length of GTDM projection along AA non-silicide resistor width direction must be same as the length of ((AA AND RESAA) INTERACT SAB)			
RESAA.5b^[R]	The length of GTDM projection along AA silicide resistor width direction must be same as the length of ((AA AND RESAA) INTERACT DIFRES)			
RESAA.6	Space between SAB and non-related AA	\geq	0.22	um
RESAA.7	Space between SAB and non-related poly.	\geq	0.3	um
RESAA.8	(Purposely blank)			
RESAA.9^[R]	It's strongly recommended space between CT and SAB for non-silicided AA resistor for spice model accuracy	=	0.12	um
RESAA.10	Space between GTDM within RESAA and AA resistor along AA resistor width direction	\geq	0.04	um
RESAA.11	RESAA extension outside of resistor AA	\geq	0.19	um
RESAA.12	DIFRES enclosure of AA resistor in width direction (both for non-silicide resistor and silicide resistor)	\geq	0	um
RESAA.13	(SN or SP) enclosure AA resistor. (Resistor AA CUT (SN or SP)) is not allowed.	\geq	0.19	um
RESAA.14	DIFRES edge should align with SAB edge along non-silicide AA resistor length direction.			

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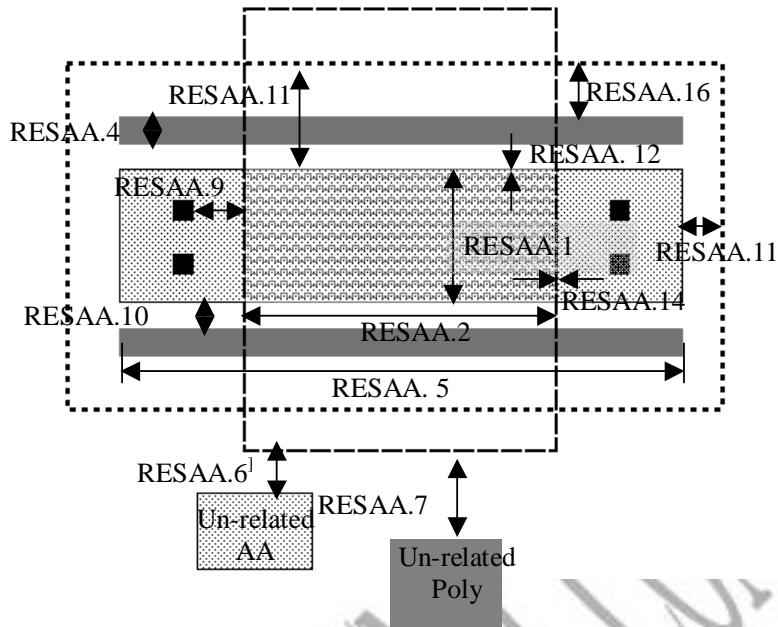
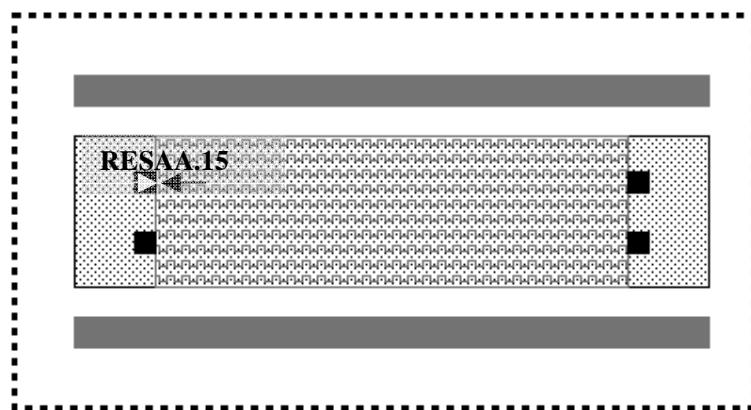


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Rule Number	Description	Operation	Design Value	Unit
RESAA.15	DIFRES edge should align with CT edge along silicide AA resistor length direction.			
RESAA.16	RESAA must fully cover (GTDMP INTERACT RESAA)	\geq	0	um
RESAA.17^[NC]	For non-silicide AA resistor, make sure the AA is covered by SAB			
RESAA.18	(AA INTERACT RESAA) must be fully covered by SN or SP.			
RESAA.19	GTDMP must be placed 2-sides beside AA resistor.			
RESAA.20	AA non-silicide resistor with SP must lay on NW.			
RESAA.21	AA resistor must be rectangular.			
RESAA.22	It's not allowed butted SN and SP on non-silicide AA resistor.			

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Non-Silicide AA resistor**Silicide AA resistor**

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7.2.40 N-Well resistor design rules

RESNW layer is to define the NW resistor area where no other implantation layer except for NW. NW resistor must within RESNW layer.

7.3.40.1 NW resistor under AA design rules

NW resistor under AA: (RESNW and AA) and NW.

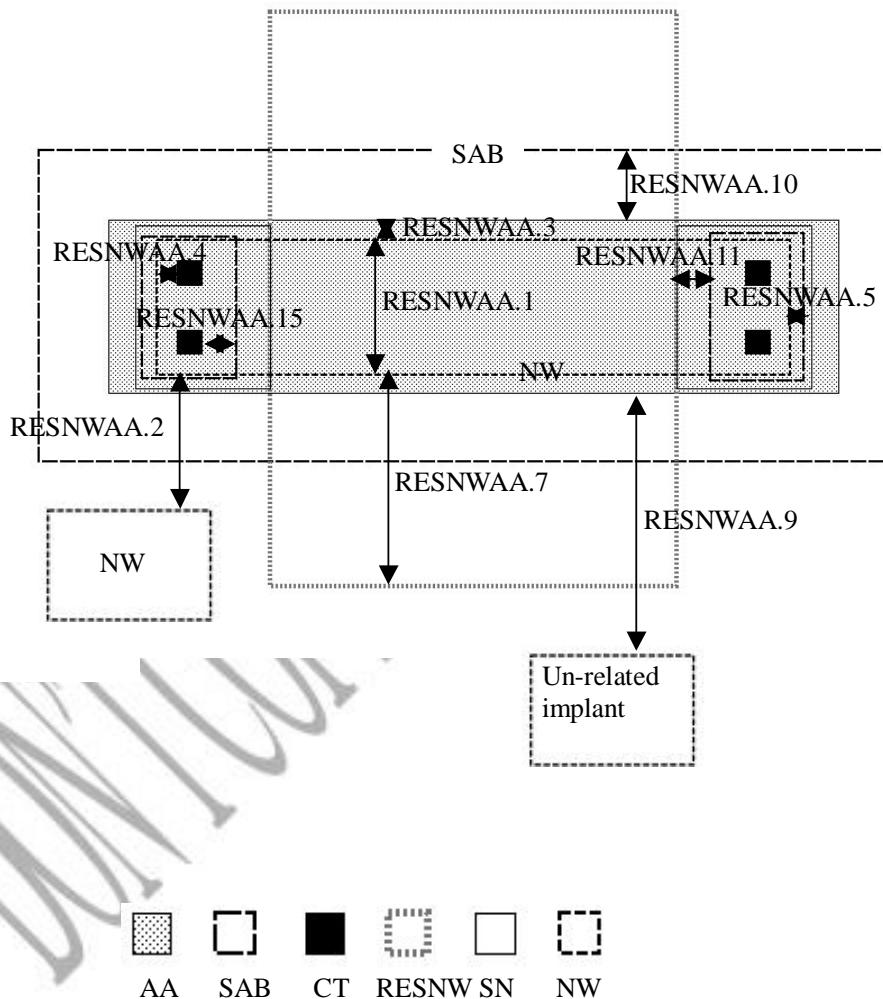
Resistor NW: NW INTERACT RESNW

Rule Number	Description	Operation	Design Value	Unit
RESNWAA.1	NW-resistor width. Suggest resistor square number (length/width ratio) ≥ 1 for stable resistance.	\geq	1.8	um
RESNWAA.2	Space between resistor NW and (resistor NW or NW).	\geq	1	um
RESNWAA.3	AA enclosure of resistor NW.	\geq	1	um
RESNWAA.4	Resistor NW enclosure of CT.	\geq	0.3	um
RESNWAA.5	Space between SAB and resistor NW.	\geq	0.3	um
RESNWAA.6	It's not allowed (AA AND RESNW) overlap with other implant layers (LVT_N/HVT_N/ULVLT_N/UHVT_N/LVT_P/HVT_P/ULVLT_P/UHVT_P/SN/SP) in the NW-resistor area.			
RESNWAA.7	Extension of RESNW outside of NW resistor along resistor width direction.	\geq	0.19	um
		\leq	0.5	um
RESNWAA.8	SAB must overlap with resistor NW except CT area.			
RESNWAA.9	(Purposely blank)			
RESNWAA.10	SAB enclosure of (AA NOT OUTSIDE RESNW).	\geq	0.22	um
RESNWAA.11	SAB overlap of SN	=	0.4	um
RESNWAA.12	NW resistor must be rectangle.			
RESNWAA.13	Only one (NW INTERACT RESNW) is allowed in one AA			
RESNWAA.14	Only two resistor N+ pickups are allowed in one NW resistor under AA.			
	Only one SAB hole in each resistor N+ pickup region is allowed.			
	The definition of resistor N+ pickup:			

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Rule Number	Description	Operation	Design Value	Unit
	((AA AND SN) AND (NW INTERACT RESNW))			
RESNWAA.15^[R]	Recommended space between SAB and CT	=	0.3	um



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7.3.40.2 NW resistor under STI design rules

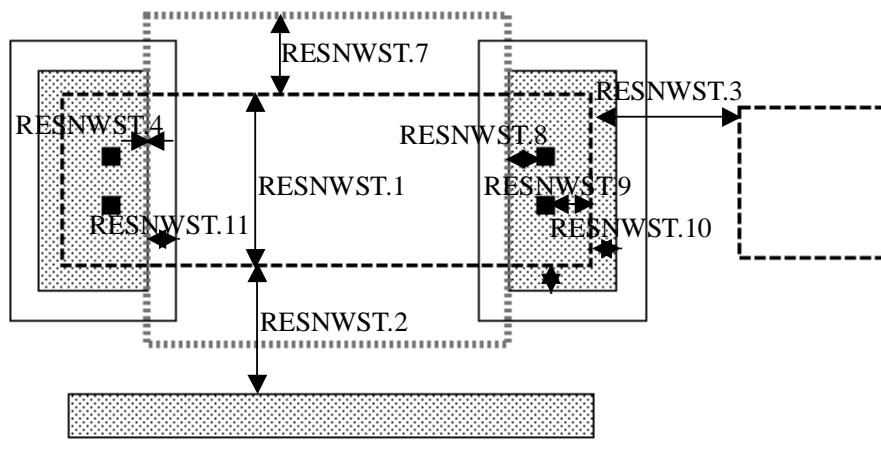
NW resistor under STI: (RESNW and NW) NOT AA.

Resistor NW: NW INTERACT RESNW

Rule Number	Description	Operation	Design Value	Unit
RESNWST.1	NW-resistor width. Suggest resistor square number length/width ratio) ≥ 1 for stable resistance.	\geq	1.8	um
RESNWST.2	Space between resistor NW and adjacent AA.	\geq	0.44	um
RESNWST.3	Space between resistor NW and (resistor NW or AA).	\geq	1	um
RESNWST.4	Space between RESNW and silicided AA area.	$=$	0	um
RESNWST.5	(Purposely blank)			
RESNWST.6	It's not allowed (SN INTERACT RESNW) overlap with other implant layers (LVT_P/HVT_P/ULVT_P/UHVT_P) in the resistor area.			
RESNWST.7	Extension of RESNW outside of NW resistor along resistor width direction.	\geq	0.19	um
		\leq	0.5	um
RESNWST.8	AA enclosure of CT (AA INTERACT RESNW).	\geq	0.3	um
RESNWST.8^[R]	It's strongly recommended AA enclosure of CT (AA INTERACT RESNW) =0.3um along resistor length direction for spice model accuracy.	\geq	0.3	um
RESNWST.9	Resistor NW enclosure of CT.	\geq	0.3	um
RESNWST.10	AA enclosure of resistor NW	\geq	0.3	um
RESNWST.11	SN enclosure of AA.	\geq	0.4	um
RESNWST.12	NW resistor must be rectangle.			

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7.2.41 High-resistance resistor design rules

RESP2 is the marking layer for high resistance resistor. High resistance resistor must be within RESP2 layer. RESP1 is the LVS marking layer for high resistance resistor.

High resistance resistor (H-R resistor): (((poly AND RERSP2) AND RESP1) AND SAB) AND SP) AND P4)

Rule Number	Description	Operation	Design Value	Unit
HR.1	Width of H-R resistor. It is recommended square number (length/width ratio) must be ≥ 1 for stable resistance.	\geq	0.4	um
		\leq	2	um
HR.2	Length of H-R resistor	\geq	0.4	um
		\leq	25	um
HR.3	GTDMP must to be drawn in RESP2 region			
HR.4	Width of GTDMP within RESP2	\geq	0.15	um
HR.5	The length of GTDMP projection along H-R resistor width direction must be same as the length of ((poly AND RESP2) INTERACT SAB)			
HR.6^{[NC][R]}	<p>It's recommended to manually draw AADMP in H-R resistor array region when H-R resistor array can't meet AA density rule(AA.26) and max (AA or AA_DMY) space rule (AA. 14, AA.15).</p> <p>Pls refer HR.7^[R], HR.8^[R], HR.16^[R], HR.17^[R] for AADMP drawing in HR resistor region.</p>			
HR.7^[R]	Width of AADMP within RESP2	\geq	0.05	um
HR.8^[R]	The length of AADMP projection along H-R resistor width direction must be same as the length of ((poly AND RESP2) INTERACT SAB) for H-R resistor array.			
HR.9	Space RESP2 and non-related AA (overlap is not allowed)	\geq	0.16	um
HR.10	Space between RESP2 and non-related AADMP (AADMP cut RESP2 is not allowed)	\geq	0.065	um
HR.11	(Purposely blank)			
HR.12^[R]	Space between H-R resistor and SN	\geq	0.1	um
HR.13	(Purposely blank)			
HR.14^[R]	Space between CT and SAB in RESP2 region	=	0.12	um

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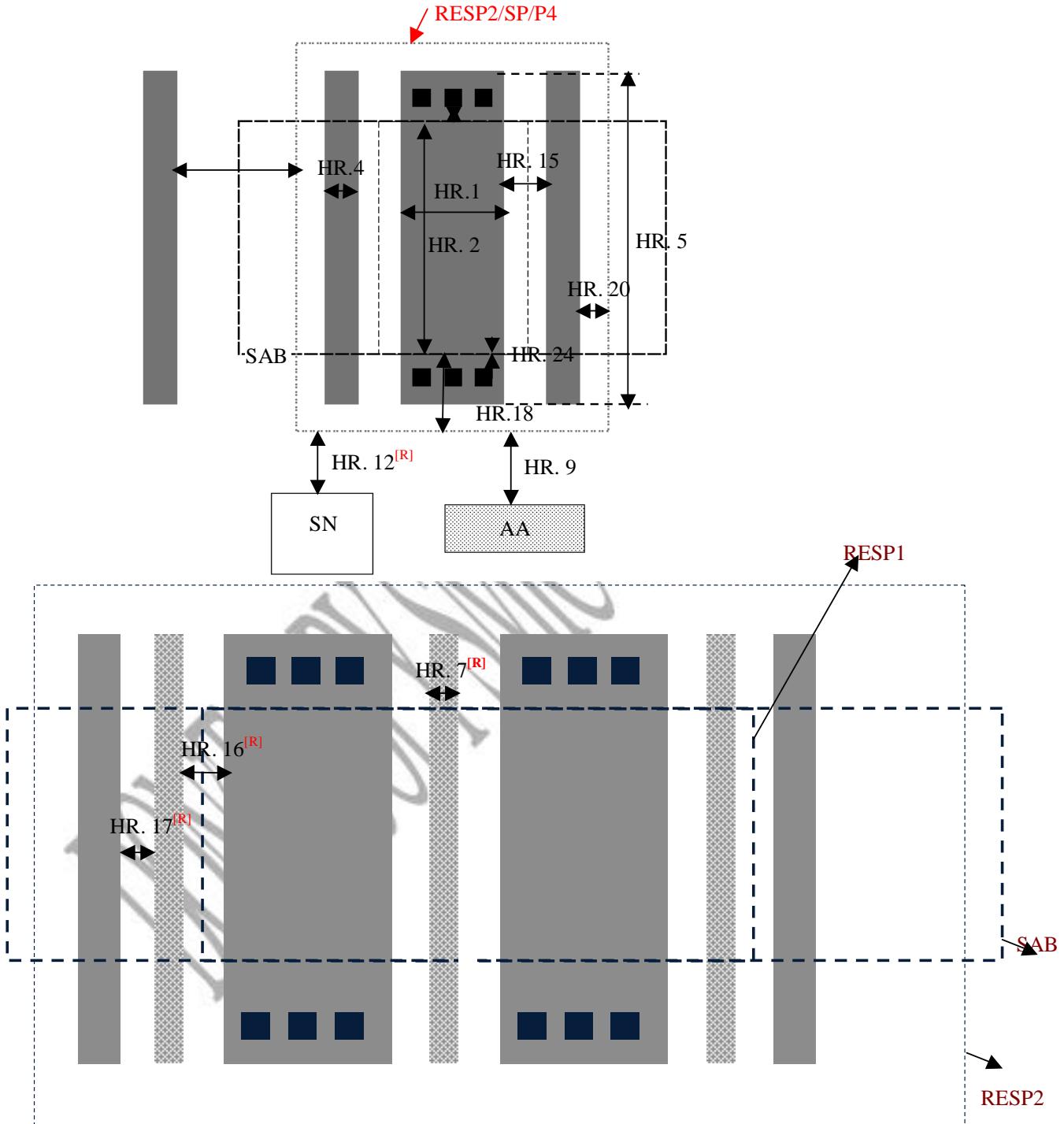


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Rule Number	Description	Operation	Design Value	Unit
HR.15	Space between GTDMP within RESP2 and neighboring H-R resistor along H-R resistor width direction	\geq	0.16	um
HR.16^[R]	Space between AADMP and neighboring H-R resistor within RESP2 along H-R resistor width direction	\geq	0.055	um
HR.17^[R]	Space between AADMP and GTDMP within RESP2 along H-R resistor width direction (AADMP and GTDMP overlap is not allowed.).	\geq	0.055	um
HR.18	H-R resistor must be fully covered by RESP2.	\geq	0.19	um
HR.19	RESP2 must fully cover (GTDMP INTERACT RESP2). GTDMP must be placed 2-side beside H-R resistor array edge inside RESP2			
HR.20	RESP2 must fully cover (GTDMP INTERACT RESP2) in width direction	\geq	0.22	um
		\leq	0.4	um
HR.21	(SP AND P4) must fully cover (((GT OR GTDMP) INTERACT SAB) AND RESP2) DRC doesn't check OCOVL region.	\geq	0.04	um
HR.22	RESP2 must fully cover (AADMP INTERACT RESP2)	\geq	0.065	um
HR.23^[NC]	H-R resistor must be covered by SAB			
HR.24	RESP1 enclosure of H-R resistor along H-R resistor length direction	\geq	0	um
HR.25^[R]	The length of (RESP1 AND ((Poly INTERACT CT) AND SAB)) should be same with (RESP2 AND ((Poly INTERACT CT) AND SAB))			
HR.26	SAB CUT RESP2 is not allowed			
HR.27	((poly OR GTDMP) INSIDE RESP2) must be rectangle			
HR.28	It's not allowed butted SN and SP on H-R resistor.			

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7.2.42 Metal Gate resistor design rules

RESP2 is the marking layer for metal gate resistor. Metal gate resistor must be within RESP2 layer. RESP1 is the LVS marking layer for metal gate resistor.

Metal gate resistor: (((Poly AND RESP2) AND RESP1) NOT INTERACT SAB)

Rule Number	Description	Operation	Design Value	Unit
MR.1	Width of metal gate resistor. Suggest resistor square number (length/width ratio) ≥ 1 for stable resistance.	\geq	0.03	um
		\leq	2	um
MR.2	GTDM must to be drawn in RESP2 region			
MR.3	Width of GTDM within RESP2	\geq	0.03	um
MR.4	The length of GTDM projection along metal gate resistor width direction must be same as the length of ((poly AND RESP2) INTERACT RESP1)			
MR.5^{[NC][R]}	AADMP is must to be drawn beside each in metal gate resistor array region. Metal gate resistor array definition: metal gate resistor (poly AND RESP2) number >1 along resistor width direction within one RESP2			
MR.6^[R]	Width of AADMP within RESP2	\geq	0.05	um
MR.7^[R]	The length of AADMP projection along metal gate resistor width direction must be same as the length of ((poly AND RESP2) INTERACT RESP1) for metal resistor array.			
MR.8	Space RESP2 and non-related AA (overlap is not allowed) DRC doesn't check OCOVL region.	\geq	0.16	um
MR.9	Space between RESP2 and non-related AADMP (AADMP cut RESP2 is not allowed)	\geq	0.065	um
MR.10	(Purposely blank)			
MR.11^[R]	Space between MG resistor and (SN or SP)	\geq	0.1	um
MR.12	Space between GTDM within RESP2 and neighboring metal gate resistor along MG resistor width direction	\geq	0.16	um
MR.13^[R]	Space between AADMP and neighboring metal gate resistor within RESP2 along metal gate resistor width	\geq	0.055	um

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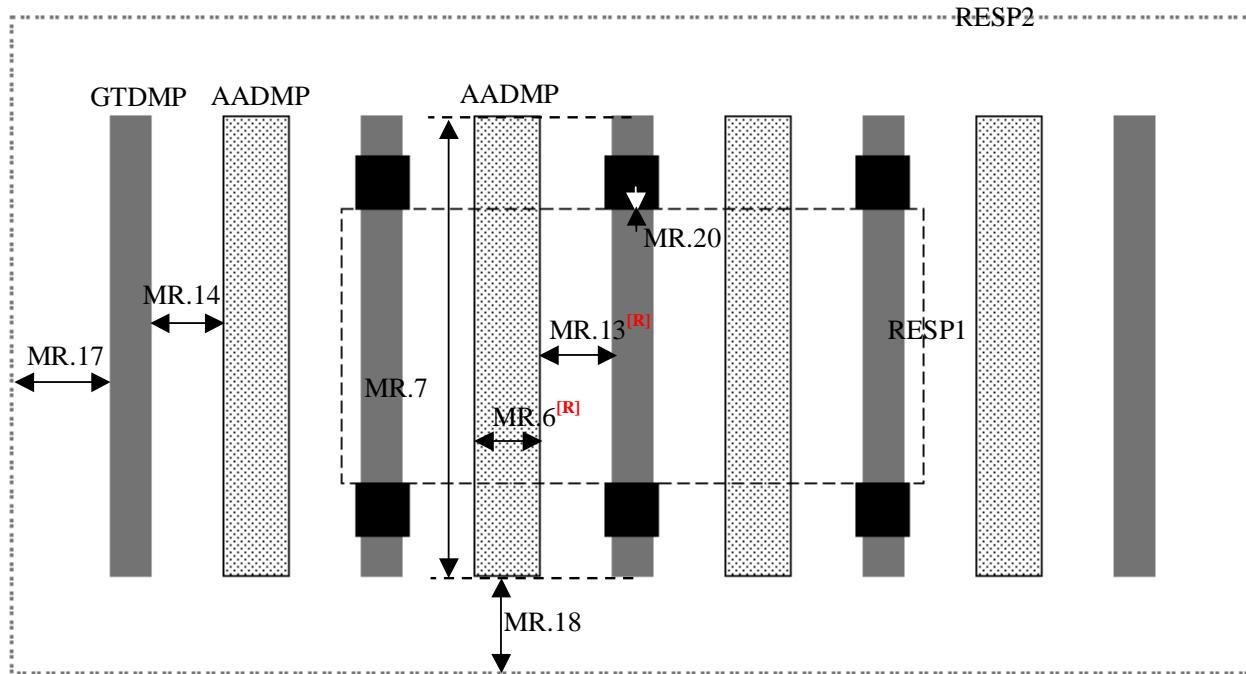
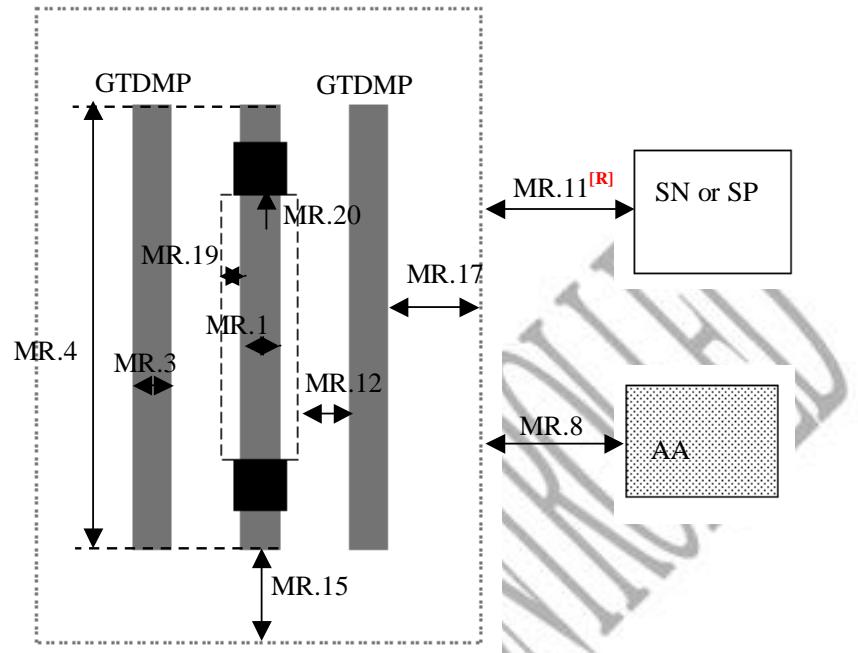


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Rule Number	Description	Operation	Design Value	Unit
	direction			
MR.14^[R]	Space between AADMP and GTDMP within RESP2 along metal gate resistor width direction (AADMP and GTDMP overlap is not allowed.).	\geq	0.055	um
MR.15	Metal gate resistor must be fully covered by RESP2.	\geq	0.19	um
MR.16	RESP2 must fully cover (GTDMP INTERACT RESP2). GTDMP must be placed 2-side beside metal gate resistor.			
MR.17	RESP2 must fully cover (GTDMP INTERACT RESP2) in width direction	\geq	0.22	um
		\leq	0.4	um
MR.18	RESP2 must fully cover AADMP. DRC doesn't check OCCD region.	\geq	0.065	um
MR.19	RESP1 enclosure of metal gate resistor along metal gate resistor width direction	\geq	0	um
MR.20	RESP1 edge should align with CT edge along metal gate resistor length direction.			
MR.21	For metal gate resistor (poly or GTDMP), the length must be same in same RESP2 region.			
MR.22	((Poly OR GTDMP) INSIDE RESP2) must be rectangle			

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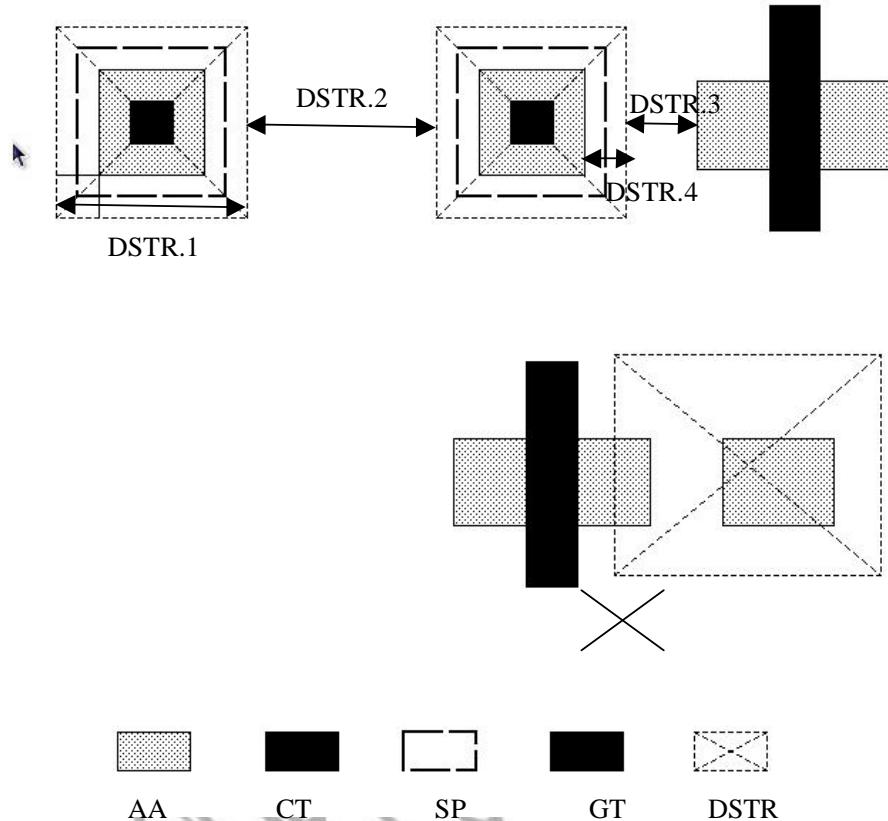
7.2.43 Diode design rules

DSTR is the marking layer for diode.

Rule Number	Description	Operation	Design Value	Unit
DSTR.1	Width of (DSTR INTERACT P+AA)	≥	0.16	um
DSTR.2	Space between two (DSTR INTERACT P+AA)	≥	0.16	um
DSTR.3	Space between (DSTR INTERACT P+AA) and P+AA. It's not allowed P+AA CUT DSTR.	≥	0.065	um
DSTR.4	DSTR enclosure of P+AA, when 1. P+AA NOT INTERACT ((poly OR GTDMP) OR GTDOP), 2. P+AA NOT INTERACT RESAA, 3. P+AA INTERACT CT.	≥	0.065	um
DSTR.5	Area of (DSTR INTERACT P+AA)	≥	0.1	um
DSTR.6	Enclosed of (DSTR INTERACT P+AA)	≥	0.1	um
DSTR.7	P+AA must be fully covered by DSTR in core region,when 1. P+AA NOT INTERACT ((poly OR GTDMP) OR GTDOP), 2. P+AA NOT INTERACT RESAA, 3. P+AA INTERACT CT. DRC doesn't check BIPOLA and CLPDMY region.			
DSTR.8	DSTR overlap (AA INTERACT ((poly OR GTDMP) OR GTDOP)) and AADUM is prohibited.			

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7.2.44 MOM design rules

MOM (metal oxide metal) capacitor is based on the capacitance between parallel same layer metal lines and different layer metal lines

SMIC only provided M1 and 1xMn ($n=2\sim 8$) MOM spice model and PDK. It is strongly recommended designers to use the MOM provided by SMIC PDK to have better characterization prediction and LVS check.

The CAD layers are used for MOM designs:

- a. MOMDMY (211;1) is DRC/LVS mark layer for MOM device.
- b. MOMTEM(211;2) LVS marking layer for MOM region
- c. MOMP1 (211;3) is LVS marking layer for MOM capacitor mesh terminal one
- d. MOMP2 (211;4) is LVS marking layer for MOM capacitor mesh terminal two
- e. MOMMES (211;5) is LVS marking layer for MOM mesh capacitor
- f. RFMOM (211;6) is LVS marking layer for RF MOM capacitor
- g. RF3T (183;2) is DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM

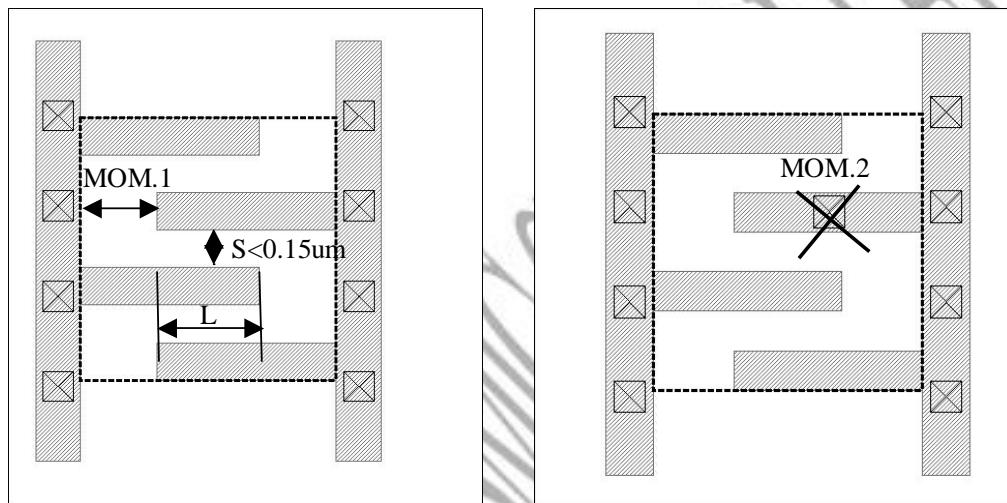
Dummy block layer MnDUB ($n=1\sim 8$) are applied in SMIC inductor designs with pre-inserted dummy. So SMIC dummy script will block out MOM region for auto dummy insertion

Rules number	Description	Operation	Design Value	Unit
MOM. 1	Space between M1/1xMn line-end and M1/1xMn in MOMDMY region. M1/1x Mn line-end definition: M1/1x Mn edge with length $< 0.07\mu m$ (W) between two outer vertex, ANGLE1=ANGLE2=90, adjacent edge A1/A2 $\geq 0.05\mu m$.	\geq	0.1	um
MOM.2 ^[NC]	It is not allowed 1xVn (connecting to 1xMn of MOM structures) overlap with MOMDMY			
MOM.3 ^[NC]	Each MOM cell must be covered by MOMDMY(211;1).			
MOM.4 ^[NC]	Use symmetrical dummy metal around the matched pairs of MOM cells instead of auto inserted dummy.			
MOM.5 ^[NC]	Active device underneath or above MOM cell should be put into couple capacitance consideration in design.			
MOM.6 ^[NC]	MGBL layer is must for MOM device with shielding to reserve poly during process, it is forbidden to draw MGBL under MOM device without shielding.			
MOM.7	Sidewall area of total metals (M1 and 1xMn) in MOMDMY. For the definition of the sidewall area: (metal length in MOMDMY (L)) * metal thickness. (Pls refer metal option table for metal thickness); Total sidewall area is to calculate the area of (finger	\leq	9.00E+06	

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Rules number	Description	Operation	Design Value	Unit
	number-1). DRC check MOM sidewall area when metal space $S < 0.15\mu m$.			



M1/1xMn



1xVn



MOMDMY

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7.2.45 LOGO design rules

Rules number	Description	Operation	Design Value	Unit
LOGO.1	Space between LOGO and (AA/poly/M1/1xMn/2xMn/8xTMn /10TMn/MMT2/ALPA OUTSIDE LOGO).	≥	10	um
LOGO.2	It's not allowed LOGO overlap with PA.			
LOGO.3 ^[NC]	It's not allowed a circuit is in the LOGO.			

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7.2.46 Metal low density design rules

LDNMK1 (131;170) is used for metal low density (M1/1xMn) region such as LOGO etc.

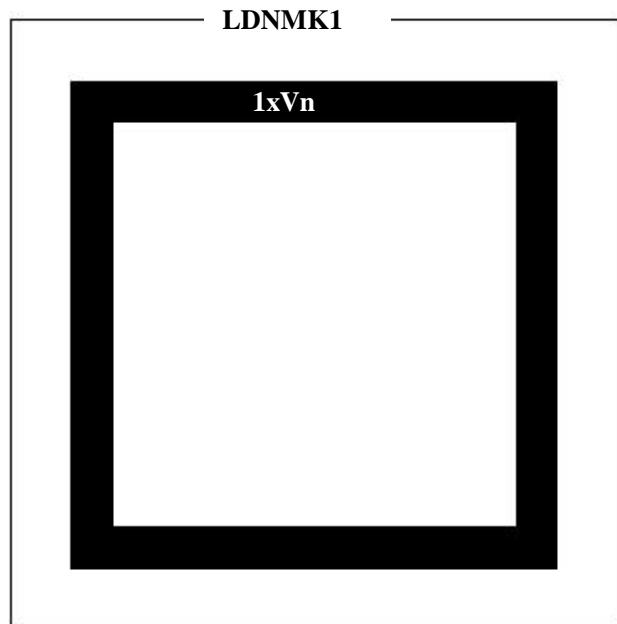
1xVn bar definition: 1xVn polygon with width=0.15um.

Rule number	Description	Operation	Design Value	Unit
LDNMK1.1	Width of M1 or M1DOP within LDNMK1 region.	\geq	0.14	um
LDNMK1.2	Width of M1DUM within LDNMK1 region.	\geq	0.12	um
LDNMK1.3	Width of 1xMn or MnDOP within LDNMK1 region.	\geq	0.14	um
LDNMK1.4	Width of 1xMn dummy within LDNMK1 region.	\geq	0.12	um
LDNMK1.5	Space between M1/M1DOP and M1/M1DOP within LDNMK1 region	\geq	0.14	um
LDNMK1.6	Space between M1DUM and M1DUM within LDNMK1 region	\geq	0.12	um
LDNMK1.7	Space between 1xMn/1xMnDOP (n=2~8) and 1xMn/1xMnDOP (n=2~8) within LDNMK1 region.	\geq	0.14	um
LDNMK1.8	Space between 1xMnDUM (n=2~8) and 1xMnDUM (n=2~8) within LDNMK1 region.	\geq	0.12	um
LDNMK1.9	Guard ring (MARKG) must be put in the region (LDNMK1 NOT (LDNMK1 sizing down 1um))			
LDNMK1.10	1xVn bar must be continuous as a ring within (LDNMK1 NOT (LDNMK1 sizing down 4um)). DRC doesn't check when (LDNMK1 INTERACT INDMD)). Pls refer LDNMK1.16 for 1xVn bar definition.			
LDNMK1.11	1xVn bar is allowed in (LDNMK1 NOT (LDNMK1 sizing down 4um)).			
LDNMK1.12	Width of 1xVn bar in guard ring	$=$	0.15	um
LDNMK1.13	Space between 1xVn bar in LDNMK1 and 1xVn/1xRVn	\geq	0.35	um
LDNMK1.14	Space between 1xVn bar and 1xVn bar within LDNMK1	\geq	0.6	um
LDNMK1.15	1xVn bar enclosure by M1/1xMn(n=1~8) within LDNMK1	\geq	0.1	um

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7.2.47 Antenna Ratio Effect rules

The "Antenna Ratio Effect" is a common name for the effects of charge accumulation in isolated nodes of an integrated circuit during its processing. This effect is also sometimes called "Plasma Induced Damage"(PID) or "charging effect". In those cases that the discharging of the isolated nodes is done through the thin gate oxide of the transistor, it might cause damage to the transistors and degrade their performance.

Antenna Ratio effect generic prevention rules are intended to reduce gate oxide damage, which was caused when exposed polysilicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler-Nordheim tunneling current to flow through the oxide during high density plasma processing in chip fabrication. Given the known process charge fluence, a figure of exposed conductor area to transistor gate area ratio is determined which guarantees Gate Oxide Integrity (GOI) reliability requirements. Failure to consider antenna rules in a design may lead to either reduced performance in transistors exposed to process induced damage, or may lead to total failure if the antenna rules are seriously violated.

Rule Number	Description	Operation	Design Value	Unit
ANT.GT1	Drawn ratio of field (poly NOT P2) perimeter area to the active poly gate area (Core, 1.8V/2.5V IO)connected directly to it	\leq	500	
ANT.GT2	Drawn ratio of field (poly NOT P2) top area to the active poly gate area (Core, 1.8V/2.5V IO) connected directly to it	\leq	250	
ANT.GT3	Drawn ratio of CT area to the active poly gate area (Core, 1.8V/2.5V IO) connected directly to it	\leq	10	
ANT.GT4a	When a protection diode is not used, the ratio of cumulative metal area to the active poly gate area (Core, 2.5V IO) from M1 to TM (if double TM used, TM layer defined as TM2 layer)	\leq	5000	
ANT.GT4b	When a protection diode is not used, the ratio of cumulative metal area to the active poly gate area (1.8V IO) from M1 to TM (if double TM used, TM layer defined as TM2 layer)	\leq	1000	
ANT.GT5a	When a protection diode is used, the ratio of cumulative M1 to Mn (Mn is inter metal layer directly underneath TM2) area to the active poly gate area (Core, 1.8V/2.5V IO)connected directly to it	\leq	diode area*500 + 44000	
ANT.GT5b	When a protection diode is used, the ratio of single TM _n (n=1,2) area to the active poly gate area (Core, 1.8V/2.5V IO) connected directly to it	\leq	diode area*998 4+55000	
ANT.GT6a	When the protection diode is not used, the drawn ratio of single layer Via area to the active poly gate area (Core, 1.8V/2.5V IO) connected directly to it	\leq	20	
ANT.GT6b	When the protection diode is not used, the drawn ratio of cumulative Via area to the active poly gate area (Core, 1.8V/2.5V IO) connected directly to it	\leq	50	

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Rule Number	Description	Operation	Design Value	Unit
ANT.GT7	When the protection diode is used, the drawn ratio of cumulative Via area to the active poly gate area (Core, 1.8V/2.5V IO)connected directly to it	\leq	diode area * 200 + 1000	
ANT.GT8a	When the protection diode is not used, the drawn ratio of PA area to the active poly gate area (1.8V/2.5V IO) connected directly to it	\leq	20	
ANT.GT8b	When the protection diode is not used, the drawn ratio of PA area to the active poly gate area (Core) connected directly to it	\leq	200	
ANT.GT9a	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the active poly gate area (1.8V/2.5V IO) connected directly to it ALPA has two kinds of thickness (14K and 28K) for each metal option.	\leq	1000	
ANT.GT9b	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the active poly gate area (Core) connected directly to it ALPA has two kinds of thickness (14K and 28K) for each metal option.	\leq	2000	
ANT.GT10	When the protection diode is used, the drawn ratio of PA area to the active poly gate area (Core, 1.8V/2.5V IO) connected directly to it	\leq	diode area * 100 + 400	
ANT.GT11	When the protection diode is used, the drawn ratio of ALPA side-wall area to the active poly gate area (Core, 1.8V/2.5V IO) connected directly to it ALPA has two kinds of thickness (14K and 28K) for each metal option.	\leq	diode area * 8500 + 30000	
ANT.GT12	Area ratio of ((M1 or 1xMn) to upper 1xVn) in the same net,when M1 or 1xMn connects to gate with area > 10000um ² and doesn't connect to AA.	\leq	300000	
ANT.GT13	Area ratio of ((1xMn or 2xMn) to upper 2xVn) in the same net,when 1xMn or 2xMn connects to gate with area > 10000um ² and doesn't connect to AA.	\leq	300000	
ANT.GT14	Area ratio of ((1xMn or 2xMn or 8xTMn) or to upper 8xTVn) in the same net,when (1xMn or 2xMn or 8xTMn) connects to gate with area > 10000um ² and doesn't connect to AA.	\leq	300000	

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Rule Number	Description	Operation	Design Value	Unit
ANT.GT15	Area ratio of ((1xMn or 2xMn or 10xTMn) or to upper 10xTVn) in the same net, when (1xMn or 2xMn or 10xTMn) connects to gate with area > 10000um ² and doesn't connect to AA.	≤	300000	

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A. The definition of Field Poly Perimeter antenna ratio

$$\text{Ratio} = 2[(L+W1)x t] / (W2 \times l)$$

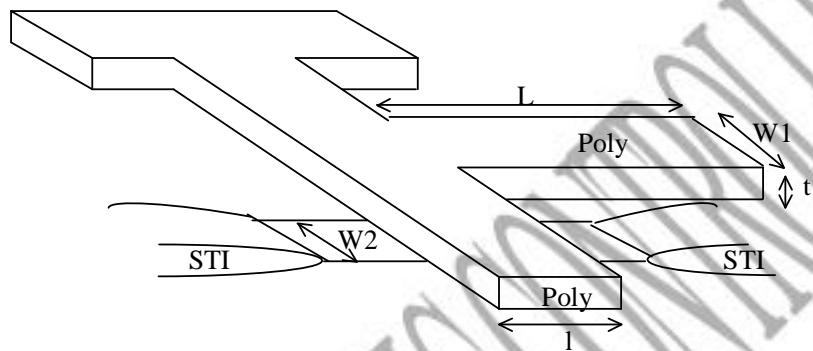
L : floating field poly length connected to gate

W1 : floating field poly width connected to gate

t : field poly thickness (poly thickness is 700A)

W2 : connected transistor channel width

l : connected transistor channel length

**B. The definition of Field Poly Top Area antenna ratio is**

$$\text{Ratio} = (\text{Apoly}) / (W2 \times l)$$

Apoly : Effective poly area that is electrically connected to gate.

C. The definition of CT, Via1-Via7 antenna ratio is

$$\text{Ratio} = \{\text{total CT (Via) area}\} / (W2 \times l)$$

D. The definition of Cumulative Metal antenna ratio is

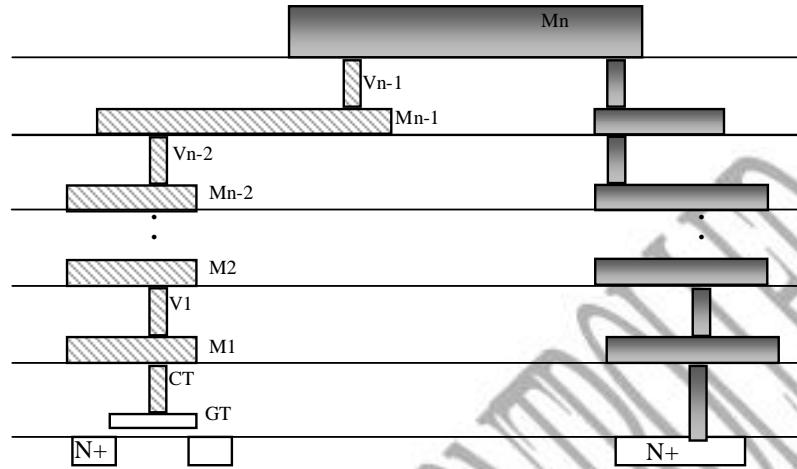
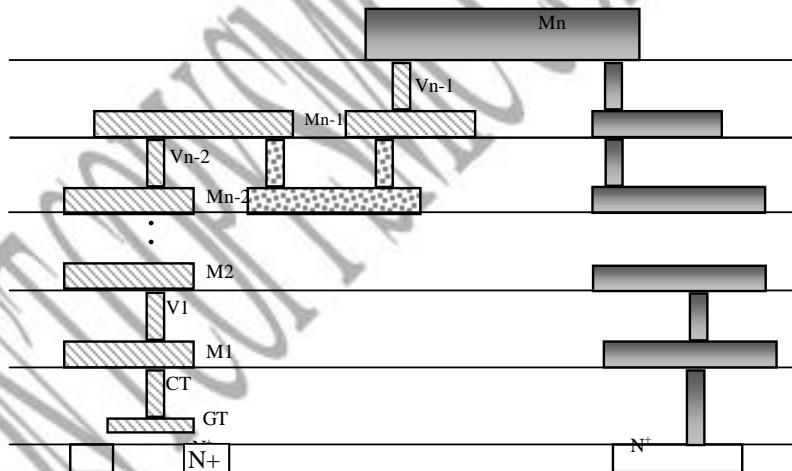
$$\text{Ratio} = (\text{AM1} + \dots) / (W2 \times l)$$

AMx : Effective metal(x) area that is electrically connected to gate without using Metal(x+1), and not to connected to active area. Cumulative Metal antenna ratio is relative to total effective metal layer area.

Note: if the metal area is connected to the poly which is cut from active poly gate by using P2 layer, that is, the metal area is not electrically connected to active poly gate. It will not take into account for metal antenna ratio calculation.

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•In case of n-level metal (I)**•In case of n-level of metal (II)**

E. The definition of the effective diode area is:
(SN OR SP) AND AA NOT poly

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7.2.48 SRAM marking layer design rules

Customers must use SMIC provided standard SRAM bit cells, customer-designed SRAM bit cells are not allowed to tape-out in SMIC.

SRAM related marking layer INST and other bit cell marking layers must follow the design rules in this section.

Rules Number	Description	Operation	Design Value	Unit
SRAM.1a^[NC]	INST (60;0) is the DRC marking layer of SP127/SP155/DP315/2P240 SRAM area.			
SRAM.1b^[NC]	RFSRAM(60;9) is the DRC marking layer of RF10T SRAM area.			
SRAM.2a^[NC]	INST is required to enclose SP127/SP155/DP315/2P240 SRAM cells which include bit cells, strap cells, edge cells (or dummy cells) and tracking cells.			
SRAM.2b^[NC]	RFSRAM is required to enclose RF10T SRAM cells which include bit cells, strap cells, edge cells (or dummy cells) and tracking cells.			
SRAM.3a^[NC]	Edges of INST layer must be aligned with the boundary of SP127/SP155/DP315/2P240 SRAM cell arrays.			
SRAM.3b^[NC]	Edges of RFSRAM layer must be aligned with the boundary of RF10T SRAM cell arrays.			
SRAM.4^[NC]	The area covered by INST, RFSRAM is required to follow SRAM rules.			
SRAM.5^[NC]	The area covered by INST, RFSRAM is required to follow the general rules if it isn't defined in SRAM rules.			
SRAM.6^[NC]	Bit cell marking layer (STSRAM, DPSRAM, LRSRAM, 2PSRAM, RFSRAM) for each type SRAM cell is must for LVS purpose. Those marking layers (STSRAM, DPSRAM, LRSRAM, 2PSRAM, RFSRAM) must enclose all SRAM cells which include bit cells, strap cells, edge cells (or dummy cells) and tracking cells (see Figure1 below).			
SRAM.7	Edges of bit cell marking layer (STSRAM, DPSRAM, LRSRAM, 2PSRAM) are required to be aligned with INST layer edges.			
SRAM.8	(Purposely blank)			
SRAM.9	If the gate is enclosed by INST layer, it should be also covered by bit cell marking layers (STSRAM, DPSRAM, LRSRAM,			

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Rules Number	Description	Operation	Design Value	Unit
	2PSRAM).			
SRAM.10	If the area is enclosed by bit cell marking layers (STSRAM, DPSRAM, LRSRAM, 2PSRAM), it should be also covered by INST layer.			
SRAM.11	HPBL is the marking layer for low leakage SRAM, the edge of HPBL layer must be aligned with the boundary of STSRAM, DPSRAM, LRSRAM, 2PSRAM.			
SRAM.12	(INST OR RFSRAM) width	\geq	0.16	um
SRAM.13	Space between (INST OR RFSRAM) and (INST OR RFSRAM)	\geq	0.16	um
SRAM.14	Space between INST/RFSRAM and (GATE NOT INTERACT (INST OR RFSRAM))	\geq	0.115	um
SRAM.15	(INST OR RFSRAM) enclosure GATE along source/drain direction	\geq	0.115	um
SRAM.16	(INST OR RFSRAM) enclosure GATE along poly length direction	\geq	0.065	um
SRAM.17	(INST OR RFSRAM) extension outside of NW (NW interact AA). Extension=0um is allowed.	\geq	0.16	um
SRAM.18	Overlap of (INST OR RFSRAM) and NW (NW interact AA). Overlap=0um is allowed.	\geq	0.16	um
SRAM.19	It's not allowed (AA, CT and V1) cut (INST OR RFSRAM).			
SRAM.20	It's not allowed P2 cut (INST OR RFSRAM).			
SRAM.21	GATE direction must be same in (INST OR RFSRAM) region.			

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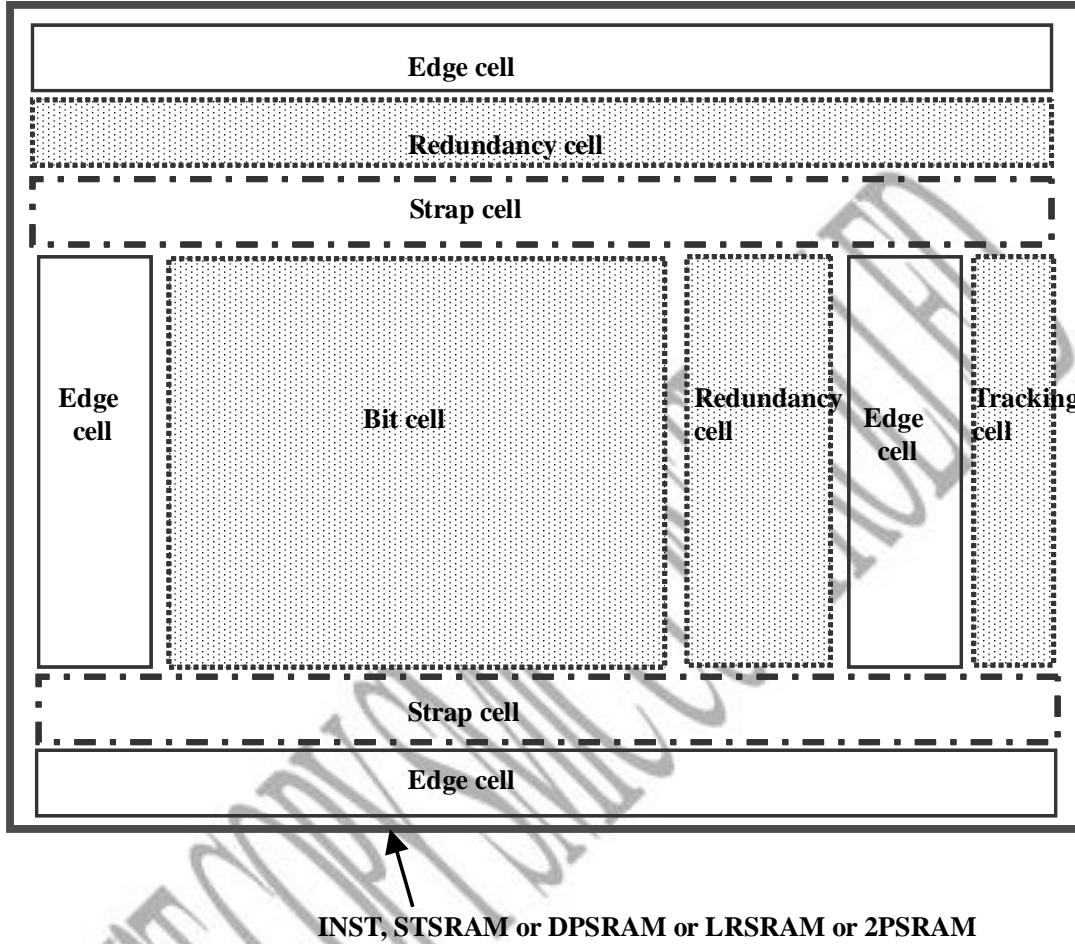
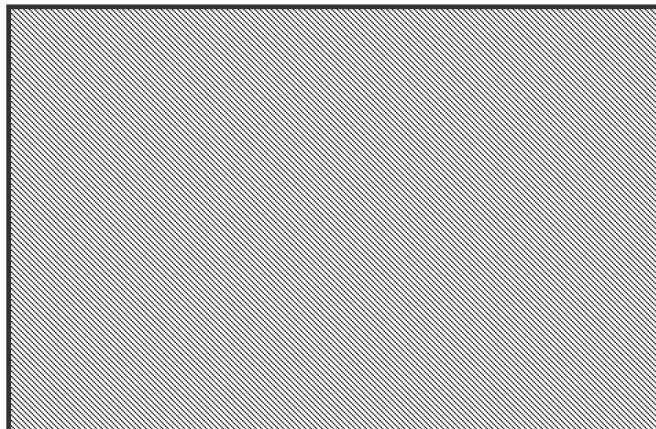


Figure1 SRAM INST marking layer figure for SP127, SP155, DP315, 2P240

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RFSRAM marking layer for RF10T SRAM

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According to: **SMIC** Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:1
2008-06-27

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7.3 Layout Guideline

7.3.1 Varactor layout Guidelines

VARMOS is the marking layer varactor device. RF varactor devices need to be covered by the marking layer VARMOS and RFDEV.

Rules Number	Description	Operation	Design Value	Unit
VAR.1a ^[G]	Channel length of core varactor MOS excluding RF device	≥	0.2	um
		≤	1	um
VAR.1b ^[G]	Channel length of core varactor MOS for RF device	≥	0.2	um
		≤	3.2	um
VAR.2a ^[G]	Channel length of I/O varactor MOS excluding RF device	≥	0.2	um
		≤	2	um
VAR.2b ^[G]	Channel length of I/O varactor MOS for RF device	≥	0.2	um
		≤	3.2	um
VAR.3 ^[G]	Channel width of varactor MOS	≥	0.4	um
VAR.4 ^[G]	Space between (poly or POLY_DMY) and neighboring GATE for core device in VARMOS	≥	0.12	um
		≤	0.6	um
VAR.5 ^[G]	Space between (poly or POLY_DMY) and neighboring GATE for VARMOS IO device	≥	0.18	um
		≤	0.6	um
VAR.6 ^[G]	(Purposely blank)			
VAR.7 ^[G]	Space between VARMOS and GATE	≥	0.16	um
VAR.8 ^[G]	VARMOS enclosure AA	≥	0.16	um
VAR.9 ^[G]	SN fully enclosure (GATE AND VARMOS) AND NW) along the channel length direction	≥	0.32	um
VAR.10 ^[G]	SN fully enclosure (GATE AND VARMOS) AND NW) along channel width direction	≥	0.13	um
VAR.11 ^[G]	SP fully enclosure (GATE AND VARMOS) NOT NW) along the channel length direction	≥	0.32	um
VAR.12 ^[G]	SP fully enclosure (GATE AND VARMOS) NOT NW) along channel width direction	≥	0.13	um

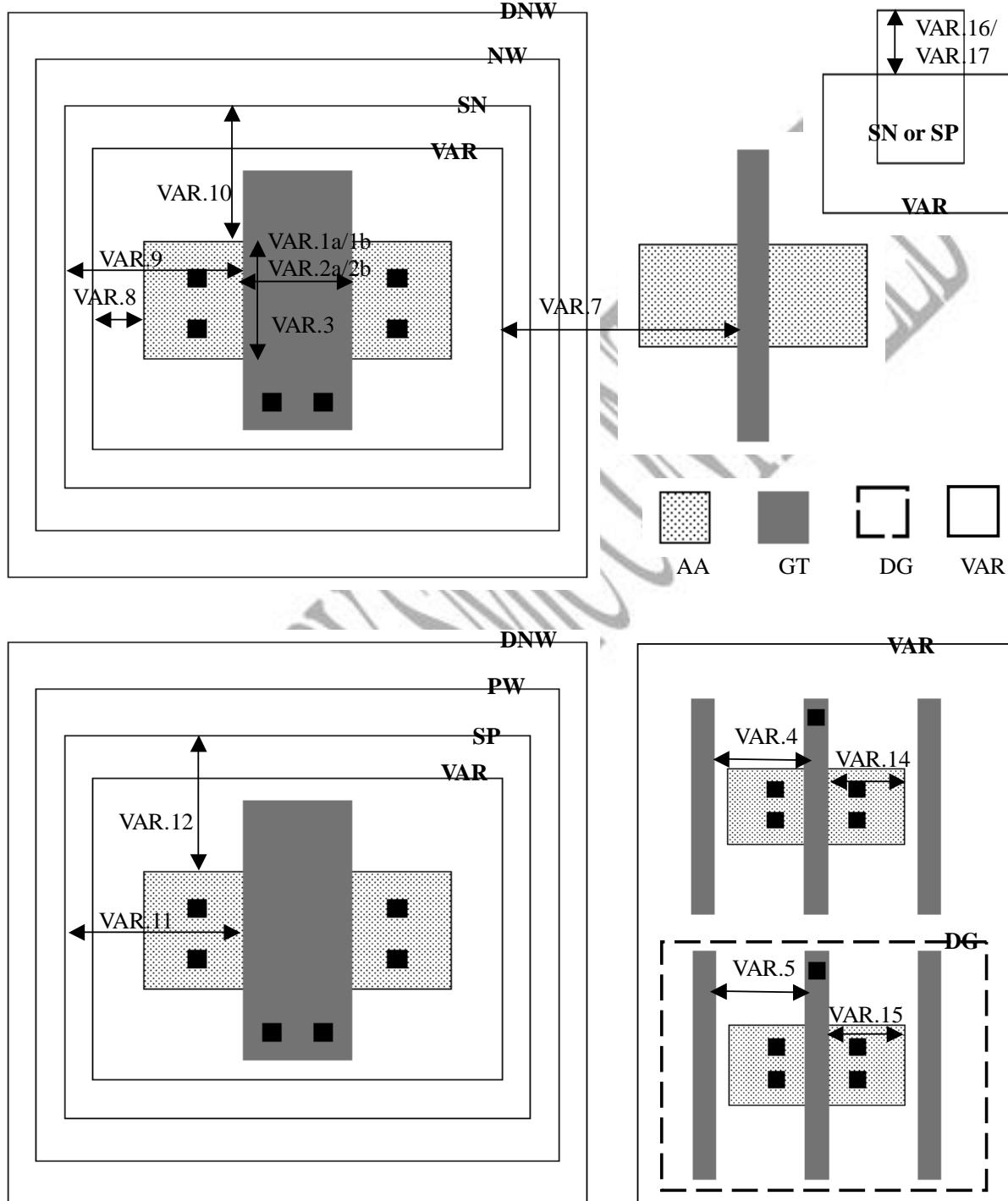
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Rules Number	Description	Operation	Design Value	Unit
VAR.13 ^[G]	(Purposely blank)			
VAR.14 ^[G]	AA extension outside of (poly or POLY_DMY) for VARMOS core device	≥	0.095	um
		≤	0.6	um
VAR.15 ^[G]	AA extension outside of (poly or POLY_DMY) for VARMOS IO device	≥	0.155	um
		≤	0.6	um
VAR.16 ^[G]	SN extension outside of VARMOS. Extension = 0um is allowed.	≥	0.16	um
VAR.17 ^[G]	SP extension outside of VARMOS. Extension = 0um is allowed.	≥	0.16	um
VAR.18 ^[G]	VARMOS marking layer must be drawn to fully cover the varactor devices.			
	Definition of varactor devices: GATE NOT OUTSIDE VARMOS.			
VAR.19 ^[G]	It's not allowed VARMOS overlap LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, UHVT_N, UHVT_P, PSUB, SAB.			
VAR.20 ^[G]	It's not allowed SP overlap (GATE AND NW) AND VARMOS).			
VAR.21 ^[G]	It's not allowed SN overlap (GATE NOT NW) AND VARMOS).			

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7.3.2 Metal E-Fuse layout guidelines

For the fuse component, it must be drawn EFUSE (81;2), MTFUSE (81;3), **FUSEAD(81;4)**; FUSEMK1 (81;152) marker layer.

E-fuse element is covered by EFUSE (81;2).

E-fuse fuse link (function area) is marked with MTFUSE (81;3).

E-fuse anode is marked with FUSEAD (81;4).

All fuse component must be fully covered by FUSEMK1 (81;152).

Rules Number	Description	Operation	Design Value	Unit
EFU.1^{[NC][G]}	FUSEMK1(81;152) must fully cover all fuse component, including EFUSE (81;2) region, program transistor, etc.			
EFU.1b^[G]	FUSEMK1 (81;152) must interact with EFUSE (81;2) region.			
EFU.1c^[G]	FUSEMK1 (81;152) must fully cover EFUSE (81;2) region.			
EFU.2a^{[NC][G]}	EFUSE (81;2) must fully cover the whole fuse element and related dummy region.			
EFU.2b^[G]	EFUSE (81;2) must interact with MTFUSE(81;3) and FUSEAD(81;4) .			
EFU.2c^[G]	EFUSE (81;2) must fully cover MTFUSE(81;3) and FUSEAD(81;4) .			
EFU.3^{[NC][G]}	(MTFUSE AND M2) is just the EFUSE function area.			
EFU.4^[G]	MTFUSE (81;3) region must exclude M1~M4 dummy pattern.			
EFU.5^{[NC][G]}	It is strongly recommended to adopt SMIC standard efuse element, including program transistor.			
EFU.6^{[NC][G]}	If designers plan to adopt customer own design, designers must provide efuse layout to SMIC for risk assessment before design start.			

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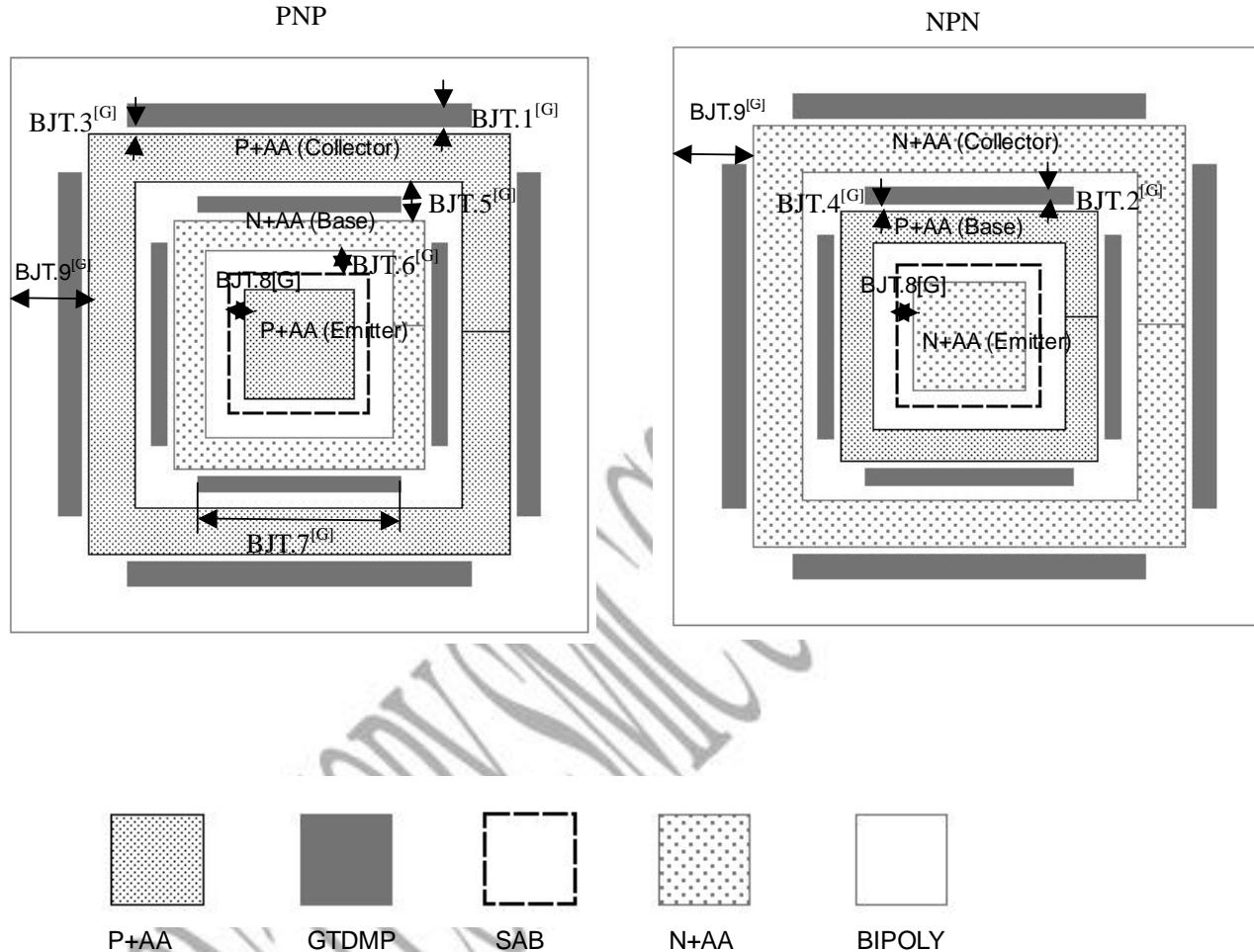
7.3.3 BIPOLA layout guidelines

SMIC provide two kinds of vertical bipolar, PNP bipolar (P+/NW) and NPN bipolar (N+/PW/DNW).
Emitter AA definition: (N+AA INSIDE BIPOLA) for NPN bipolar or (P+ AA INSIDE BIPOLA) for PNP bipolar
Collector AA definition: (N+ pickup AA INSIDE BIPOLA) for NPN bipolar or (P+ pickup AA INSIDE BIPOLA) for PNP bipolar
Base AA definition: (P+ pickup AA INSIDE BIPOLA) for NPN bipolar or (N+ pickup AA INSIDE BIPOLA) for PNP bipolar

Rules Number	Description	Operation	Design Value	Unit
BJT.1 ^[G]	(GTDM ^P INSIDE BIPOLA) width between BIPOLA edge and collector AA	=	0.5	um
BJT.2 ^[G]	GTDM ^P width between base AA and collector AA	=	0.15	um
BJT.3 ^[G]	Space between ((GTDM ^P OUTSIDE Collector AA) INTERACT BIPOLA) and Collector AA	≥	0.1	um
		≤	0.25	um
BJT.4 ^[G]	Space between GTDM ^P and Base AA when GTDM ^P is located between Base AA and Collector AA	=	0.035	um
BJT.5 ^[G]	Space between Collect AA and Base AA	=	0.22	um
BJT.6 ^[G]	Space between Base AA and SAB	=	0.22	um
BJT.7 ^[G]	GTDM ^P length in BIPOLA region	≥	1	um
BJT.8 ^[G]	SAB enclosure Emitter AA	=	0.3	um
BJT.9 ^[G]	BIPOLA enclosure of Collector AA	≥	1	um
BJT.10 ^[G]	BIPOLA overlap of PSUB, poly, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, UHVT_N, UHVT_P, VARMOS, and INST is prohibited.			

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7.3.4 Inductor design rules

SMIC provide inductor spice model and PDK, to have better device characterization prediction and LVS check, it is recommended to use SMIC PDK.

The inductor devices must be covered by inductor marking layer IND MY (212;0). IND MY should not be used for other purpose than inductor device.

Dummy block layer DUMBA/ DUMB P/DUMB M are applied in SMIC inductor designs. So SMIC dummy script will block out inductor region for auto dummy insertion.

Rules number	Description	Operation	Design Value	Unit
IND.1 ^{[G][NC]}	Inductor components (including inductor circuit, guard ring, dummy patterns.) must be covered by IND MY layer.			
IND.2 ^[G]	MTT2 and MTT2DM/ STMn and STMnDM (n=1~2) (10x metal) / TMn and TMnDUM (n=1~2) (8x metal) / ALPA and ALDUM maximum width within IND MY (for inductor application only)	≤	30	um
IND.3 ^[G]	Space between MTT2/TMn (n=1~2)/STMn (n=1~2)/ ALPA (as Inductor) and other MTT2/TM2/STM2/ALPA outside of IND MY.	≥	30	um
IND.4 ^[G]	Extension of dummy layer “IND MY” beyond inductor MTT2/TMn (n=1~2) /STMn (n=1~2) / ALPA coil metal designs.	≥	15	um
IND.5 ^{[G][NC]}	Space between active device and IND MY. Active device is all devices in device truth table.	≥	10	um
IND.6 ^[G]	All devices listed in device table inside IND MY region are prohibited.			
IND.7 ^{[G][NC]}	1xV _n (n=1~8)/2xV _n (n=1~2) are not allowed within inductor coil metal area to reduce parasitic capacitance			
IND.8 ^{[G][NC]}	Do not allow non-inductor related layouts within IND MY. Only the patterns been put into inductor characterization allowed.			
IND.9 ^{[G][NC]}	Make the inductor regions within chip to be evenly spread to have balanced pattern density.			
IND.10 ^{[G][NC]}	MGBL layer is must for inductor device with shielding to reserve poly during process, it is forbidden to draw MGBL under inductor device without shielding.			

Note:

1. For all device DRC check in IND.6^[G], DRC follows device marking layer to check diode, MOM, Bipola, VARMOS, resistor, etc. For MOS device, the definition is for DRC identify as below:

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GATE0 = (poly AND AA)

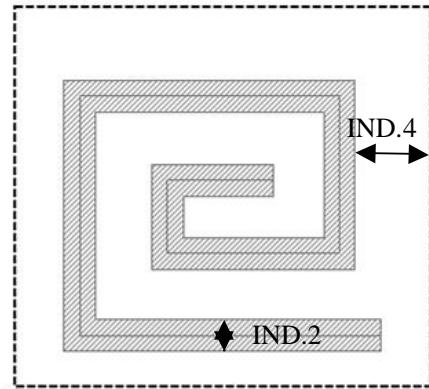
AA1 = (AA INTERACT GATE0) NOT GATE0

MOS = GATE0 TOUCH AA1 == 2

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7.3.5 Seal ring layout guideline

A. Use of the scribe lane seal ring (guard ring) to protect test chip is recommended

A continuous scribe lane and seal ring is required on all sides of a chip that is intended for dicing and packaging. The seal ring provides both a low resistance path to ground for surge currents and a metal seal against ionic contaminations. 45 degree bent is expected around every die corner. Multiple stacked via/Metal trench are considered to suppress crack risk during dicing saw operation in assembly.

B. Typical structure of scribe lane seal ring (guard ring)

For products less than 10 metal layers, please skip the metal and via layers that are not used in the product.

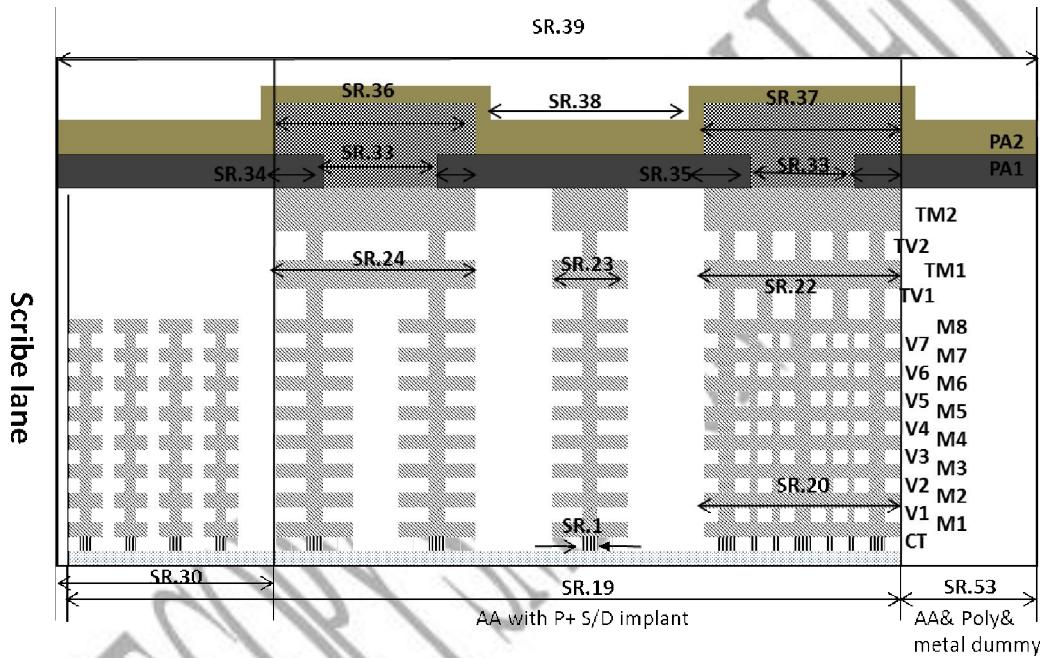
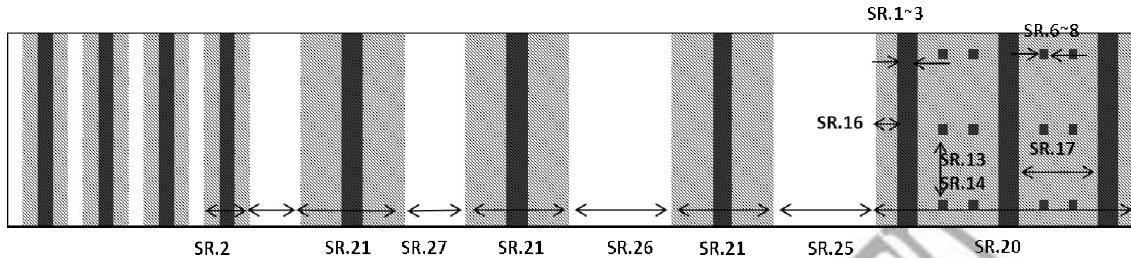


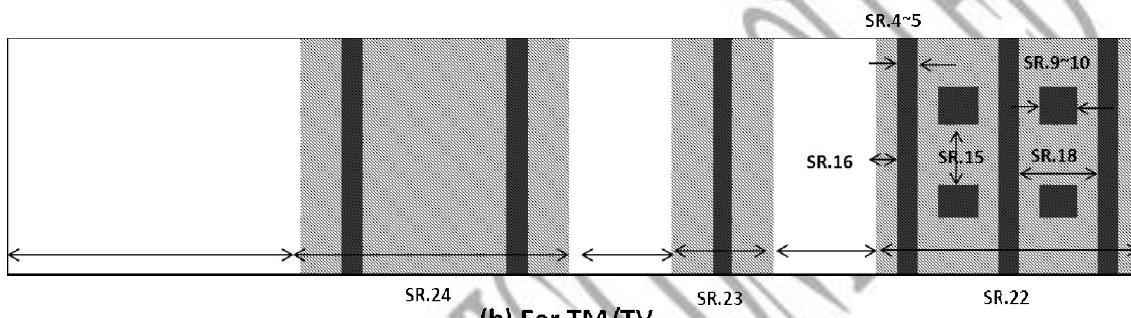
Figure.1 Cross sectional schematic of 10 metal seal ring structure

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(a) For CT, M1-M8, V1-V8



(b) For TM/TV

Figure2 Schematic top view of the seal ring structure

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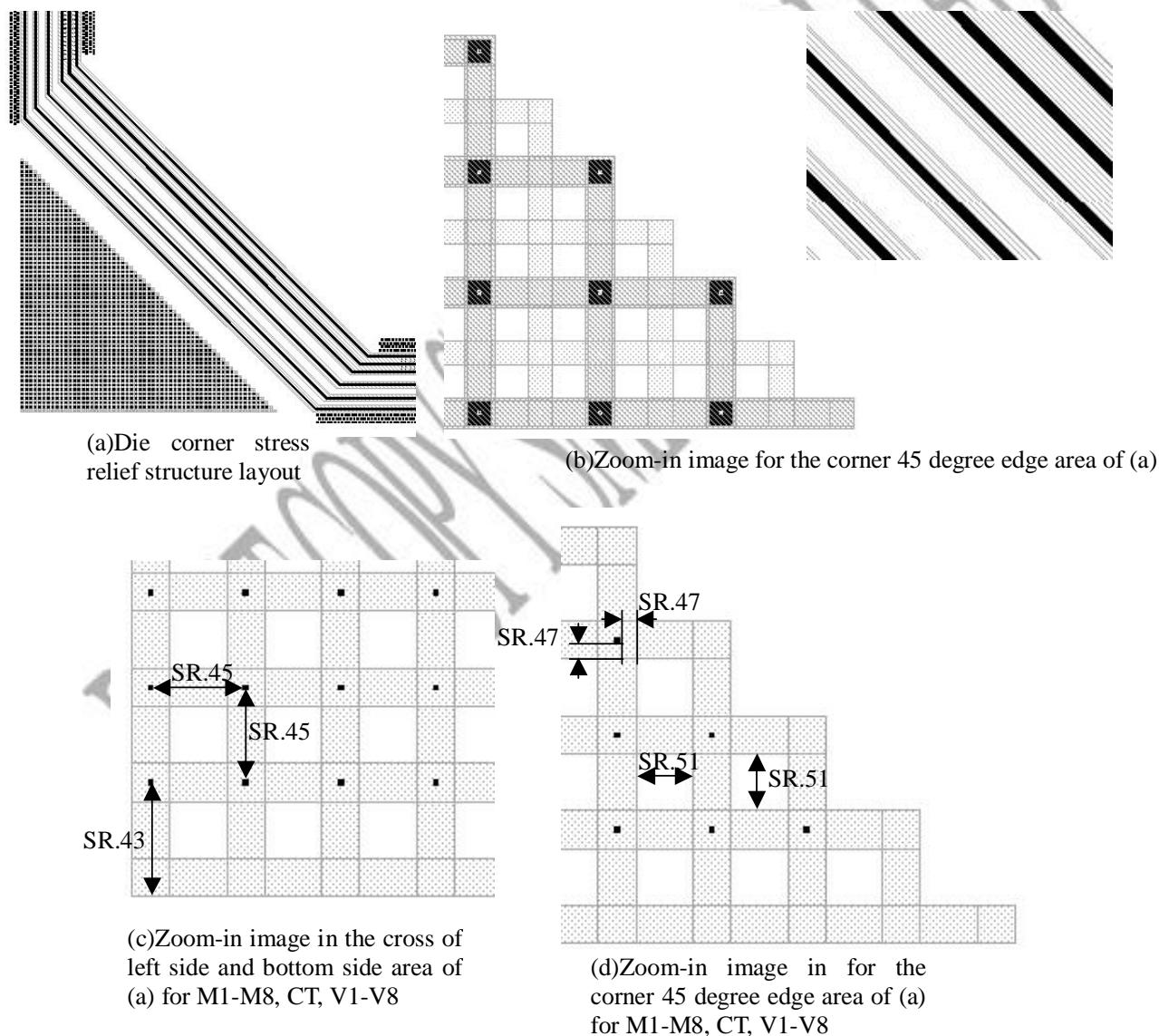
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C. Die Corner Layout

The chamfer region is required for all chips for process robustness. A chamfer or corner bevel of more than 82.2um is required to be cut from each corner of the chip. The chamfer area is triangular and has an area of more than half of 82.2 um x 82.2 um square.

The seal ring corner layout in Figure.3~Figure.5 is recommended to SMIC's customers to manage local stress at each die corner. Metal & via dummy pattern is recommended at each corner of seal ring. The dimension of each segment in the corner layout is given in Figure.3~4.

Please customer follows SMIC standard of seal ring corner rule (figure.4, figure.5) both for the situations that seal ring design and layout implemented in SMIC and customer sides.



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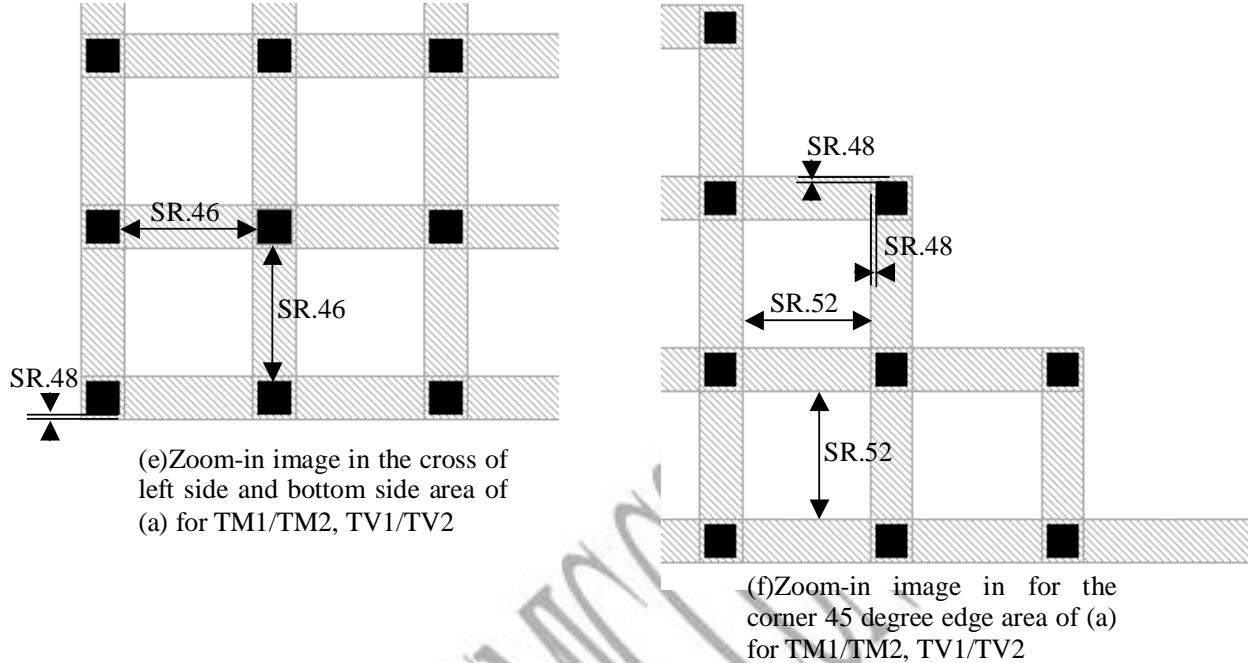


Figure3 Die corner stress relief structure layout

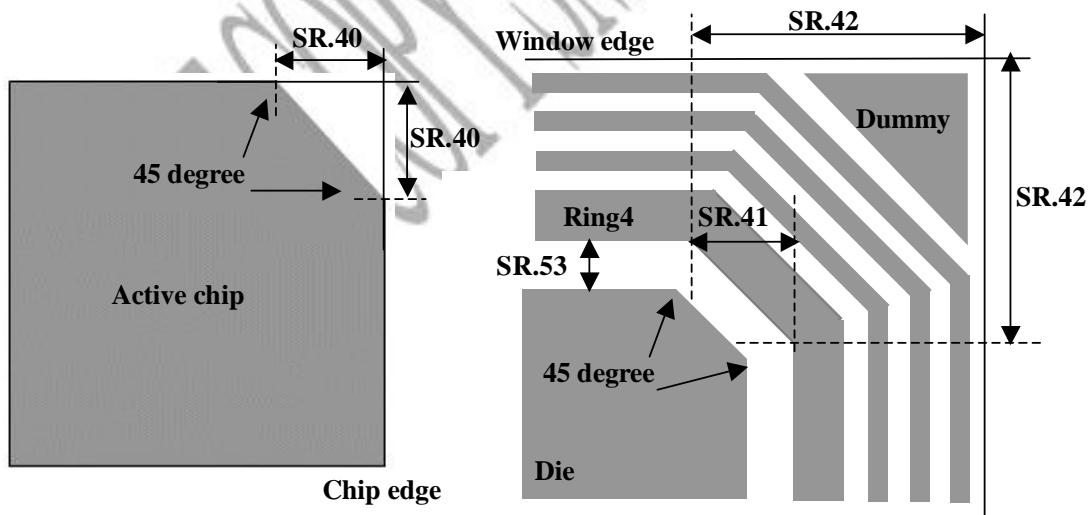


Figure4 Chamfer area at chip corner

Figure5 Seal ring corner if applied by SMIC

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Table 1 Dimension of Seal ring structure

Rule number	Description	Operation	Design Value	Unit
SR.1^[G]	Fixed width of CT slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.06	um
SR.2^[G]	Fixed width of 1x Vn slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56 or 0.1	um
SR.3^[G]	Fixed width of 2x Vn slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56 or 0.1	um
SR.4^[G]	Fixed width of 8x TV slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56	um
SR.5^[G]	Fixed width of 10x TV slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56	um
SR.6^[G]	Fixed square CT size	=	0.065	um
SR.7^[G]	Fixed width of square 1xVn size	=	0.1	um
SR.8^[G]	Fixed width of square 2xVn size	=	0.1	um
SR.9^[G]	Fixed width of square 8x TV size	=	0.51	um
SR.10^[G]	Fixed width of square 10x TV size	=	0.51	um
SR.11^[G]	CT enclosure by M1	\geq	0.1	um
SR.12^[G]	Via slot enclosure by metal	\geq	0.05	um
SR.13^[G]	Space between square CTs in metal ring along the direction of seal ring	=	1.045	um
SR.14^[G]	Space between square 1xVns in metal ring along the direction of seal ring	=	1.01	um
SR.15^[G]	Space between square 10x TVs in metal ring along the direction of seal ring	=	0.6	um
SR.16^[G]	Space between 1xVn/10xTV slot and the metal ring edge	\geq	0.5	um
SR.17^[G]	Space between 1xVn/10xTV slots	\geq	1.38	um
SR.18^[G]	Space between 1xVn/10xTV slot and 1xVn/10xTV	\geq	0.4	um

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Rule number	Description	Operation	Design Value	Unit
SR.19^[G]	Width of P+ AA beneath CT in seal ring	=	19.5	um
SR.20^[G]	M1/1x Mn width of ring4	=	5.56	um
SR.21^[G]	M1/1x Mn width of ring1,ring2, ring3	=	1.67	um
SR.22^[G]	10x TM width of ring3	=	5.56	um
SR.23^[G]	10x TM width of ring2	=	1.67	um
SR.24^[G]	10x TM width of ring1	=	4.45	um
SR.25^[G]	Space between M1/1x Mn ring4 and ring3	=	1.67	um
SR.26^[G]	Space between M1/1x Mn ring3 and ring2	=	1.67	um
SR.27^[G]	Space between M1/1x Mn ring2 and ring1	=	1.11	um
SR.28^[G]	Space between 10x TM ring3 and ring2	=	1.67	um
SR.29^[G]	Space between 10x TM ring2 and ring1	=	1.67	um
SR.30^[G]	Space between M1/1x Mn /10x TM ring1 and window edge	=	5	um
SR.31^[G]	Space between M1/1x Mn ring4 and layout edge	=	0	um
SR.32^[G]	Space between 10x TM ring3 and layout edge	=	0	um
SR.33^[G]	PA slot width	=	2.4	um
SR.34^[G]	Space between PA slot and M1/1x Mn /10x TM ring1 edge	=	1.025	um
SR.35^[G]	Space between PA slot and M1/1xMn ring4 (or 10x TM ring 3) edge	=	1.58	um
SR.36^[G]	Al ring1 width	=	4.44	um
SR.37^[G]	Al ring2 width	=	5.56	um
SR.38^[G]	Space between Al ring1 and Al ring2	=	5	um
SR.39^[G]	Total seal ring width	=	26.7	um
SR.40^[G]	Chamfer area size at the chip corner	\geq	70	um
SR.41^[G]	Chamfer length of ring4 of seal ring in the bevel corner. This rule is for customer layout and chip	\geq	70	um

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Rule number	Description	Operation	Design Value	Unit
	design. This rule is for SMIC to apply seal rings for customer.			
SR.42^[G]	Distance from window edges to the point that ring4 start to bend 45 degree at seal ring corner. This rule is for SMIC to apply seal rings for customer.	=	94	um
SR.43^[G]	Space between first column square 1x Vn and dummy area edge in the die corner dummy relief area	=	2.23	um
SR.44^[G]	Space between first column10x TV and dummy area edge in the die corner dummy relief area.	=	2.025	um
SR.45^[G]	Space between 1x Vns in dummy relief area.	=	1.9	um
SR.46^[G]	Space between 10x TVs in dummy relief area.	=	1.49	um
SR.47^[G]	Space between 1x Vn and metal edge in the dummy relief area	=	0.23	um
SR.48^[G]	Space between 10x TV and metal edge in the dummy relief area	=	0.025	um
SR.49^[G]	M1/1x Mn width in the dummy relief area	=	0.56	um
SR.50^[G]	10x TM width in the dummy relief area	=	0.56	um
SR.51^[G]	Space between M1s or 1xMns in the dummy relief area	=	1.44	um
SR.52^[G]	Space between 10TMs in the dummy relief area	=	1.44	um
SR.53^[G]	Space between seal ring layout edge and chip edge(BORDER layer)	=	6.667	um
SR.54^[G]	Chip corner chamfer area should be covered by NODMF			
SR.55^[G]	NODMF layer size at chip corner chamfer area	≥	70	um
SR.56^[G]	Seal ring must be a close ring.			
SR.57^[G]	CT slot, 1xVn slot, 2xVn slot and 8xVn slot are be drawn in seal ring region (slot pattern is NOT square pattern).			

Note: The numbers in the above table are gds drawn dimension for 28nm design (pre 10% shrinkage).

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Table 2 Key Dimension of Seal ring structure for DRC

Rule number	Description	Operation	Design Value	Unit
SR.1^[G]	Fixed width of contact slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.06	um
SR.2^[G]	Fixed width of 1x Vn slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56 or 0.1	um
SR.3^[G]	Fixed width of 2x Vn slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56 or 0.1	um
SR.4^[G]	Fixed width of 8x TV slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56	um
SR.5^[G]	Fixed width of 10x TV slot, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.56	um
SR.6^[G]	Fixed square CT size	=	0.065	um
SR.7^[G]	Fixed width of square 1xVn size	=	0.1	um
SR.8^[G]	Fixed width of square 2x Vn size	=	0.1	um
SR.9^[G]	Fixed width of square 8x TV size	=	0.51	um
SR.10^[G]	Fixed width of square 10x TV size	=	0.51	um
SR.11^[G]	CT slot, 1xVn slot, 2xVn slot, 8x TVn and 10x TVn slot are be drawn in seal ring region (slot pattern is NOT square pattern).			
SR.12^[G]	CT slot enclosure by M1	\geq	0.1	um
SR.13^[G]	Via slot enclosure by metal	\geq	0.05	um
SR.14^[G]	Space between square vias	\leq	6	um

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7.3.6 ESD design rules and guideline

The ESD guidelines are targeted to meet HBM-2KV(Human Body Mode) and MM-200V (Machine mode) spec according to EIA/JEDEC standard and EIA/JESD22 test standard, SMIC does not guarantee the final ESD device performance. If designers do not follow SMIC ESD guideline, chip level ESD test should be done for ESD verification.

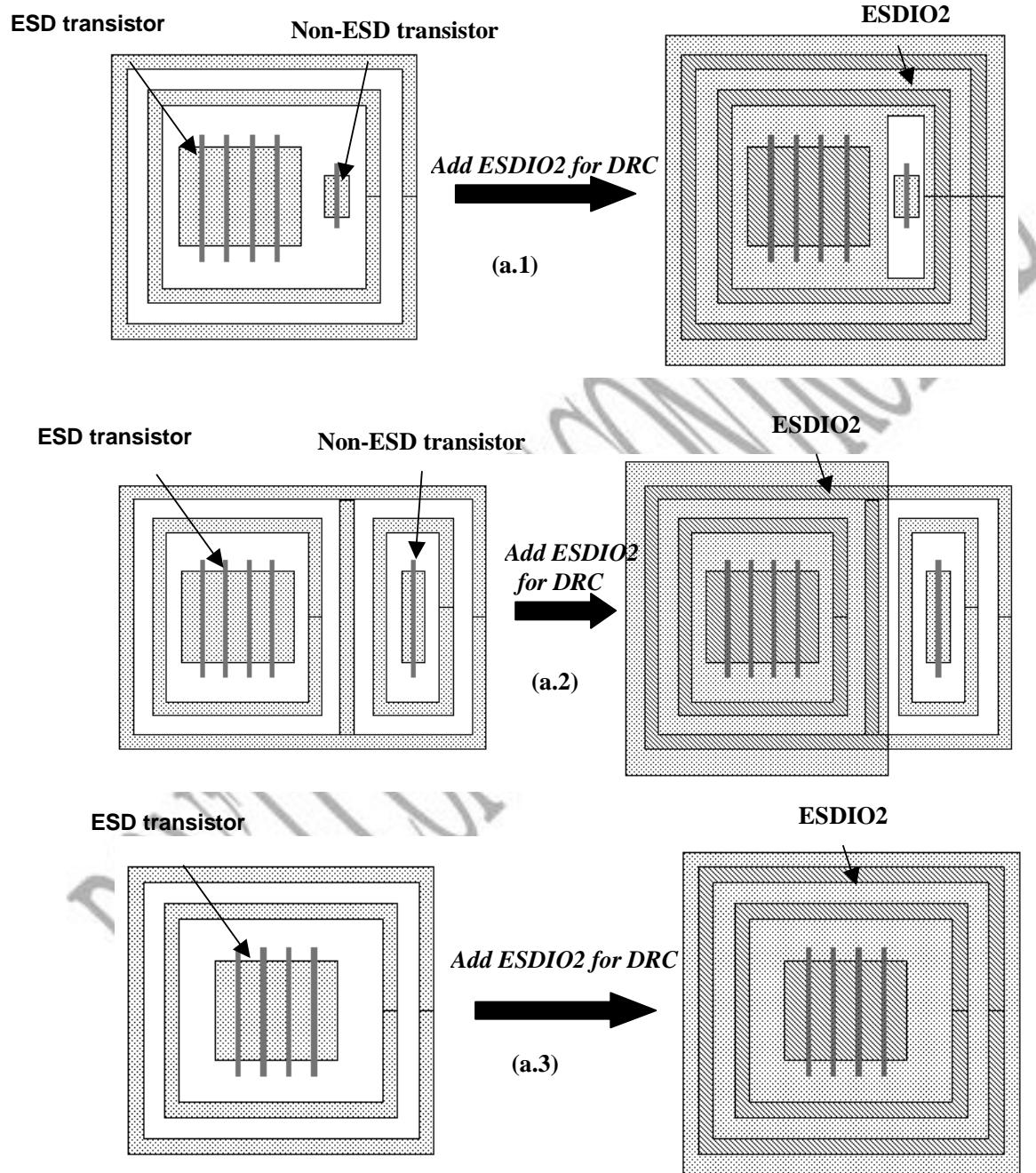
7.3.6.1 ESDIO2 (DRC marker layer for ESD component)

ESDIO2 (GDS No: 133;3) is DRC marking layer for I/O ESD **N/PMOS** including power clamp big MOS protection devices and circuits identification. This layer should cover ESD transistors and its N and P guard rings, but non-ESD transistor inside the same guard ring should be excluded. Otherwise, all the devices and circuits inside ESDIO2 will be regarded as ESD transistors and may induce false DRC alarms. ESDIO2 should be drawn at each individual ESD protection device.

ESDHV (GDS: 133;1) is DRC marking layer for HV tolerant ESD protection devices using cascaded **N/PMOS**. Please refer to the examples in Fig.1.

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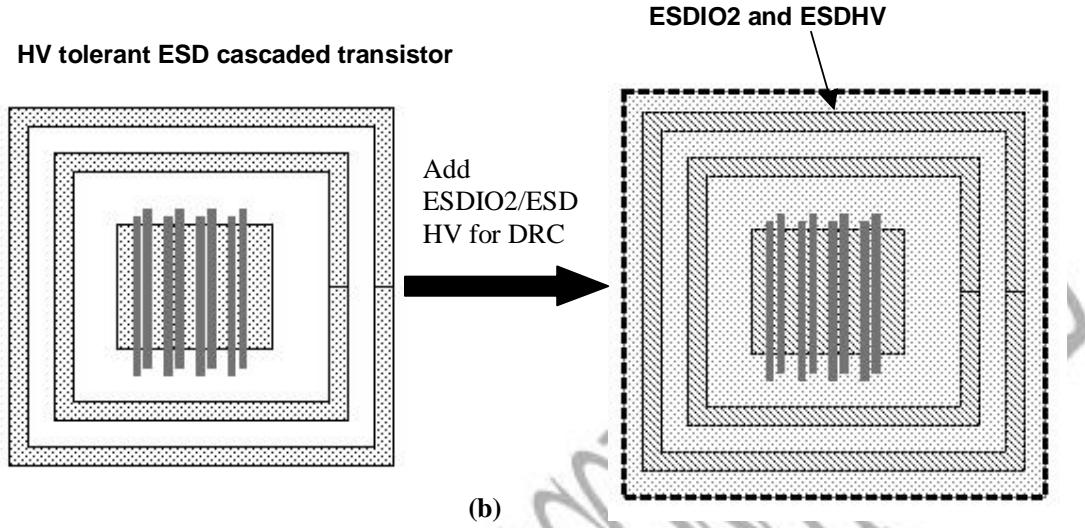


Fig.1 Examples of ESDIO2/ESDHV for ESD DRC

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7.3.6.2 ESD design and layout guideline

The guideline provided layout structure and dimension for N/P MOS ESD protection device design. SAB on drain side is essential for ESD protection devices.

Rule Number	Description	Operation	Design Value	Unit
ESD.1 ^[NC]	Finger-type structure with uniform finger width is suggested for N/P MOS ESD protection design			
ESD.2 ^[G]	Unit finger width (F) of NMOS and PMOS for ESD protection device (Fig.2)	≥	5	um
		≤	30	um
ESD.3 ^[G]	ESD.3a ^[G] and ESD.3b ^[G] are defined for total channel width of ESD N/PMOS. The total channel width is calculated by the ESD MOS in the same Drain connection. The connectivity can be formed by all metal, via, ALPA, PA and MD but not broken by resistors. SAB is used for drain recognition in DRC runset.			
ESD.3a ^[G]	Channel width (W) of NMOS for ESD protection device (Channel width=Finger width x Finger No.)	≥	360	um
ESD.3b ^[G]	Channel width (W) of PMOS for ESD protection device (Channel width=Finger width x Finger No.)	≥	450	um
ESD.4a ^[G]	Channel length of core N/PMOS for protection device	≥	0.08	um
ESD.4b ^[G]	Channel length of 1.8V/1.5V (under drive) I/O N/PMOS for protection device	≥	0.15	um
ESD.4c ^[G]	Channel length of 2.5V/1.8V (under drive) I/O N/PMOS for protection device	≥	0.27	um
ESD.4d ^[G]	Channel length of 2.5V overdrive 3.3V I/O NMOS for protection device	≥	0.55	um
ESD.4e ^[G]	Channel length of 2.5V overdrive 3.3V I/O PMOS for protection device	≥	0.44	um
ESD.5 ^[G]	Space from poly edge to CT edge on source side (SCP) for NMOS and PMOS (Fig. 4 and Fig.6).	≥	0.2	um
ESD.6 ^[G]	Space from poly edge to CT edge on drain side (DCP) (Fig. 4 and Fig.6)	≥	1	um
ESD.7 ^[G]	SAB should block on drain side of NMOS and PMOS (contact region should be kept silicided.)			

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Rule Number	Description	Operation	Design Value	Unit
	SAB drawn on source side is not necessary.			
ESD.8^[G]	Width of SAB on the drain side (A) for 1.0/1.2/1.8 NMOS and PMOS, note: A does not include the overlap of SAB area and GT(Fig. 4 and Fig.6)	\geq	0.8	um
ESD.9^[G]	ESD protection devices should be surrounded by guard ring, this guard ring also can be designed as the pickup of the ESD device. (Fig.2)			
ESD.10^[NC]	The NMOS/PMOS should be added after the input resistor R as the secondary ESD protection for better ESD immunity if there is no conflict with circuit operation.			
ESD.11^[NC]	value of input resister R. (Fig. 3)	\geq	200	Ω
ESD.12^[NC]	The suggested channel width for secondary ESD protection device	$=$	20	um
ESD.13a^[NC]	Channel length of core N/PMOS for secondary protection device	$=$	0.08	um
ESD.13b^[NC]	Channel length of 1.8V/1.5V (under drive) I/O N/PMOS for secondary protection device	$=$	0.15	um
ESD.13c^[NC]	Channel length of 2.5V/1.8 (under drive) I/O N/PMOS for secondary protection device	$=$	0.27	um
ESD.13d^[NC]	Channel length of 2.5V overdrive 3.3V NMOS for secondary protection device	$=$	0.55	um
ESD.13e^[NC]	Channel length of 2.5V overdrive 3.3V PMOS for secondary protection device	$=$	0.44	um
ESD.14a^[G]	The overlap (Sd) of SAB and poly for all I/O ESD N/PMOS (Fig. 4)	\geq	0.05	um
ESD.14b^[G]	The overlap (Sd) of the SAB and poly for core ESD N/PMOS	\geq	0.02	um
ESD.15^[G]	For high voltage tolerant I/O using Cascoded NMOS, ESD implant is required. (refer to Fig.5& 6)			
ESD.16a^[G]	Channel length for 2.5V tolerant I/O using 1.8V cascoded N/PMOS	\geq	0.15	um
ESD.16b^[G]	Channel length for 3.3V tolerant I/O using 2.5V cascoded N/PMOS	\geq	0.27	um

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Rule Number	Description	Operation	Design Value	Unit
ESD.16c^[G]	Channel length for 5V tolerant I/O using 3.3V (2.5V overdrive) cascoded N/PMOS	\geq	0.55	um
ESD.17^[G]	The space (S) between active poly gate and inactive poly gate of cascaded NMOS should be (Fig.6)	\leq	0.3	um
ESD.18^[G]	For high voltage tolerant I/O designed by cascoded N/PMOS , SAB should cover all top poly gates and extend to overlap the second poly gate by (Fig. 6)	\geq	0.05	um
ESD.19^[NC]	Contacts should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of contact drawn on rule is	\geq	370	count
ESD.20^[NC]	Vias should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of via drawn on rule is	\geq	650	count
ESD.21a^[NC]	Total width (W2) of each individual inter metal(M1~M8) lines of the nearest current path between ESD devices and bonding pad	\geq	15	um
ESD.22b^[NC]	Total width (W2) of each individual top metal(TM1,TM2) line of the nearest current path between ESD devices and bonding pad	\geq	3	um
ESD.23^[NC]	In Chip level ESD guideline, the poly gate of N/PMOS of internal and I/O circuit is not allowed to connect to power/ground or input/output pad directly. Please refer to ESD.21a, ESD.21b, ESD.21c rules below.			
ESD.23a^[NC]	Secondary ESD protection or tie-high/tie-low cell is strongly recommended to insert between poly gate and power/ground pad or input/out pad.			
ESD.23b^[NC]	N/PMOS used for capacitor is not recommended to connect power/ground or input/output pad directly.			
ESD.23c^[NC]	Poly resistor and ESD protection N/PMOS (including primary and secondary ESD protection) can be exempt for this rule.			

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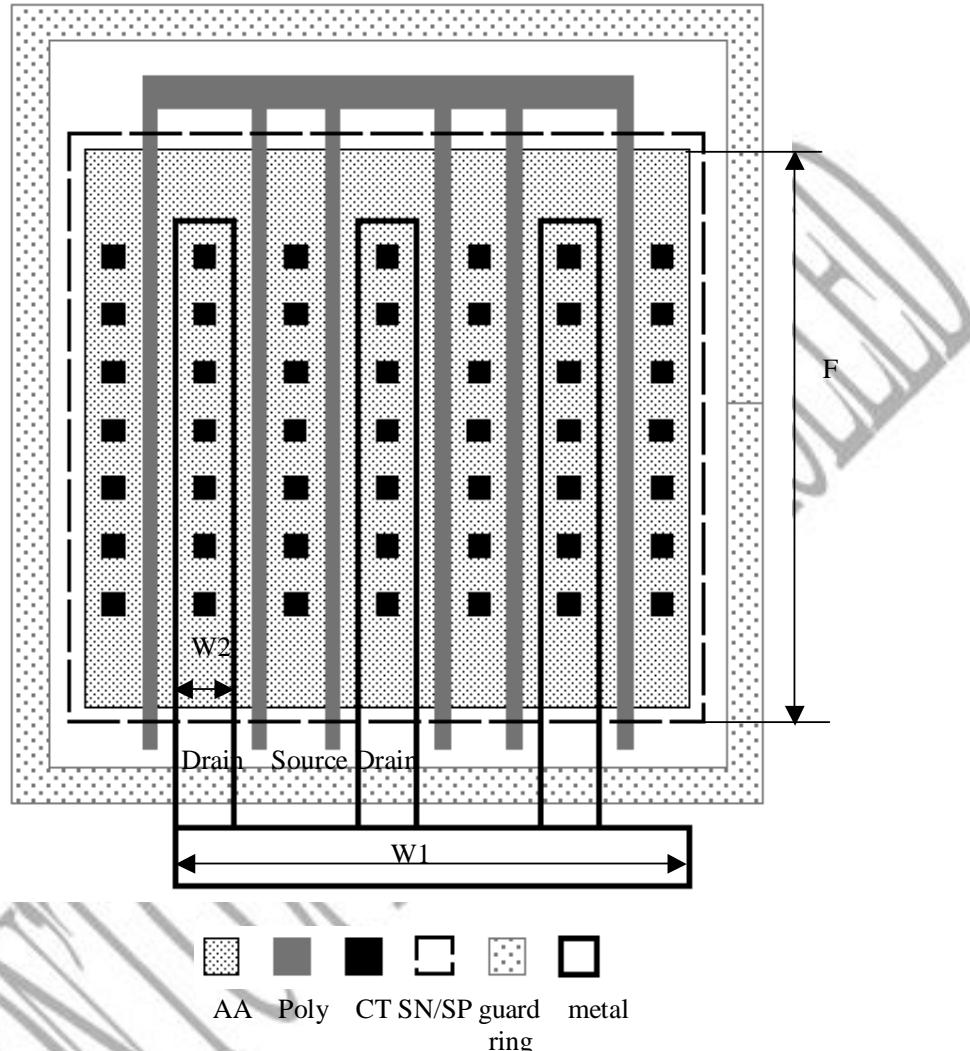


Fig.2 ESD Cell Layout Example

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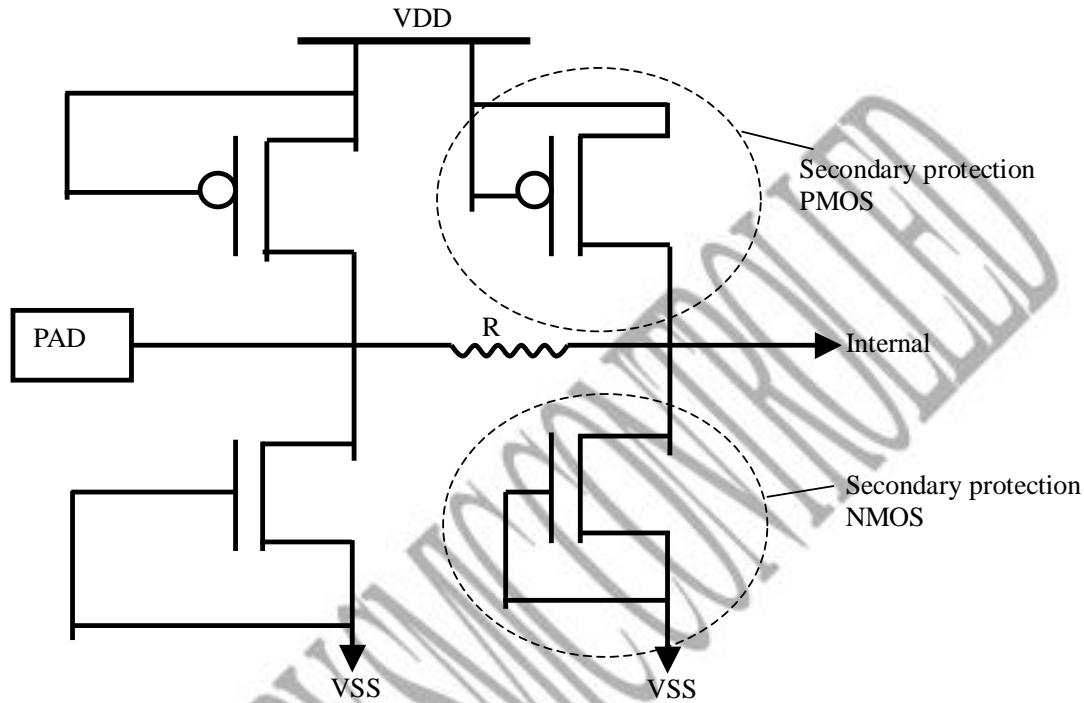


Fig. 3 ESD Protection Scheme

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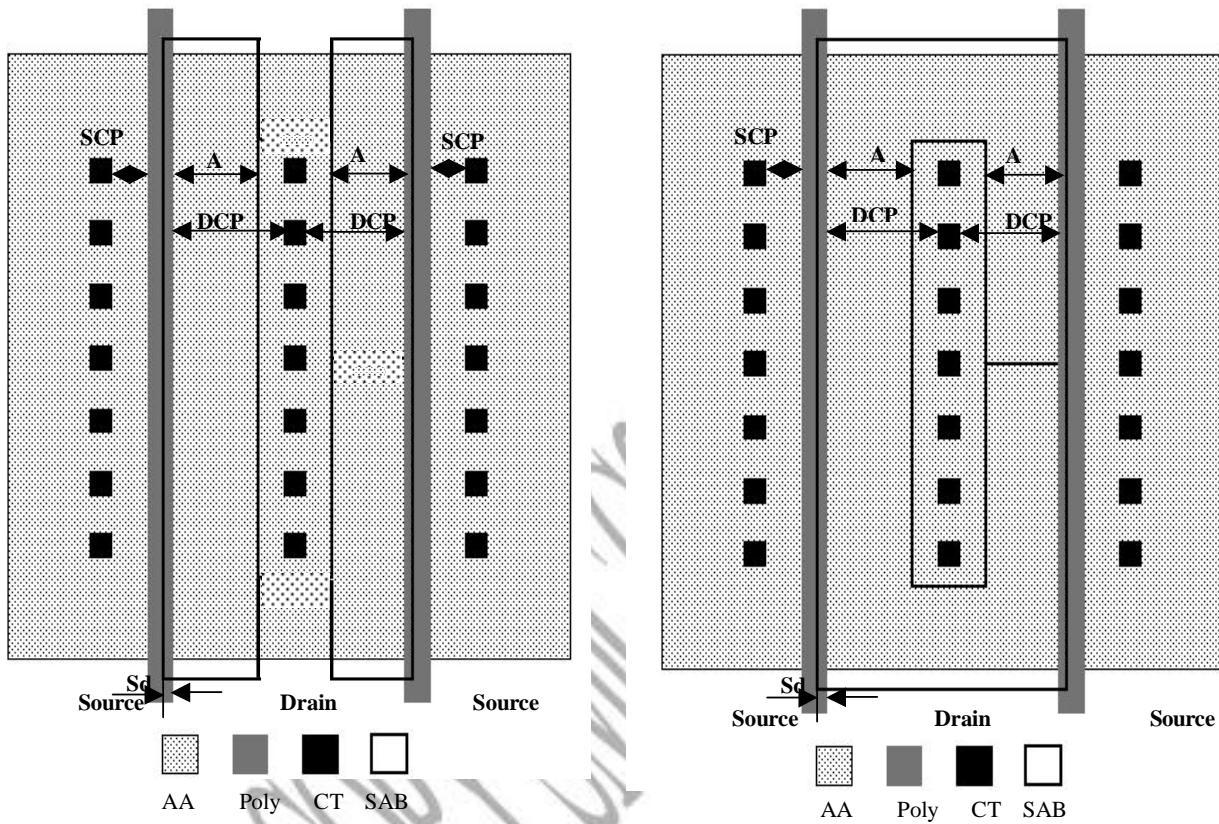


Fig.4 NMOS/PMOS I/O for ESD Protection with two layout styles of SAB

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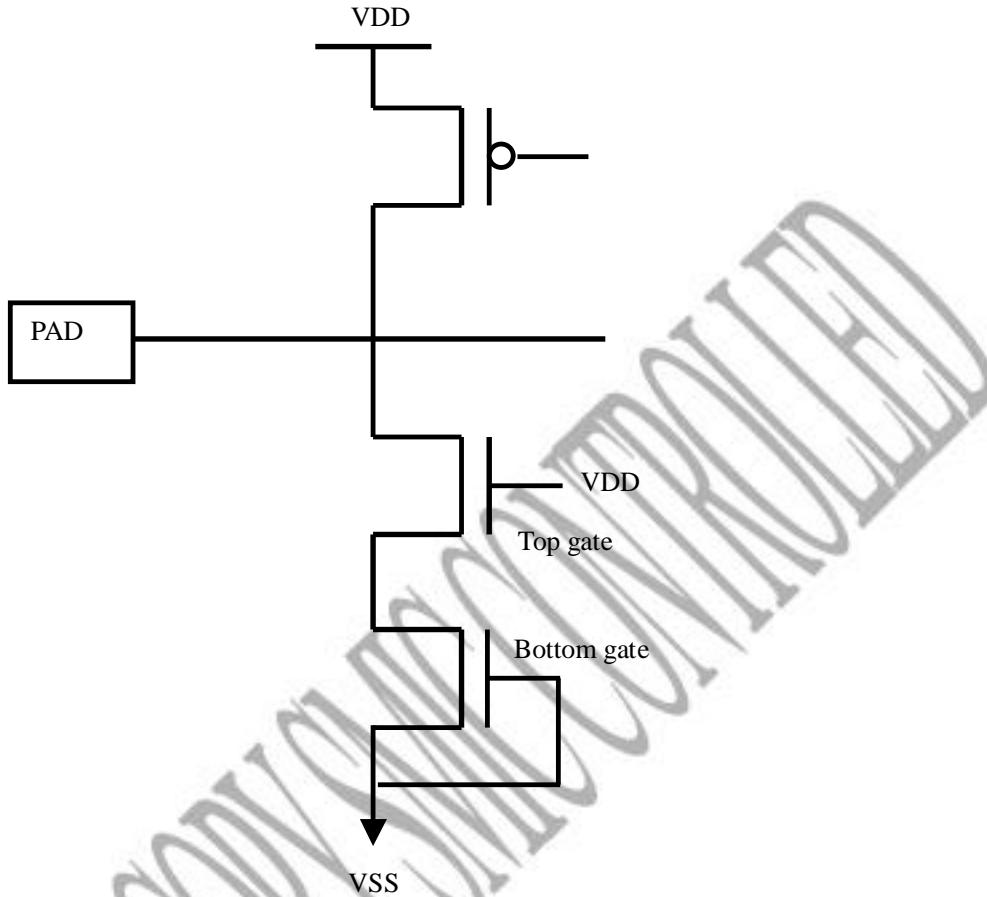


Fig. 5 HV Tolerant I/O ESD protection using cascaded NMOS

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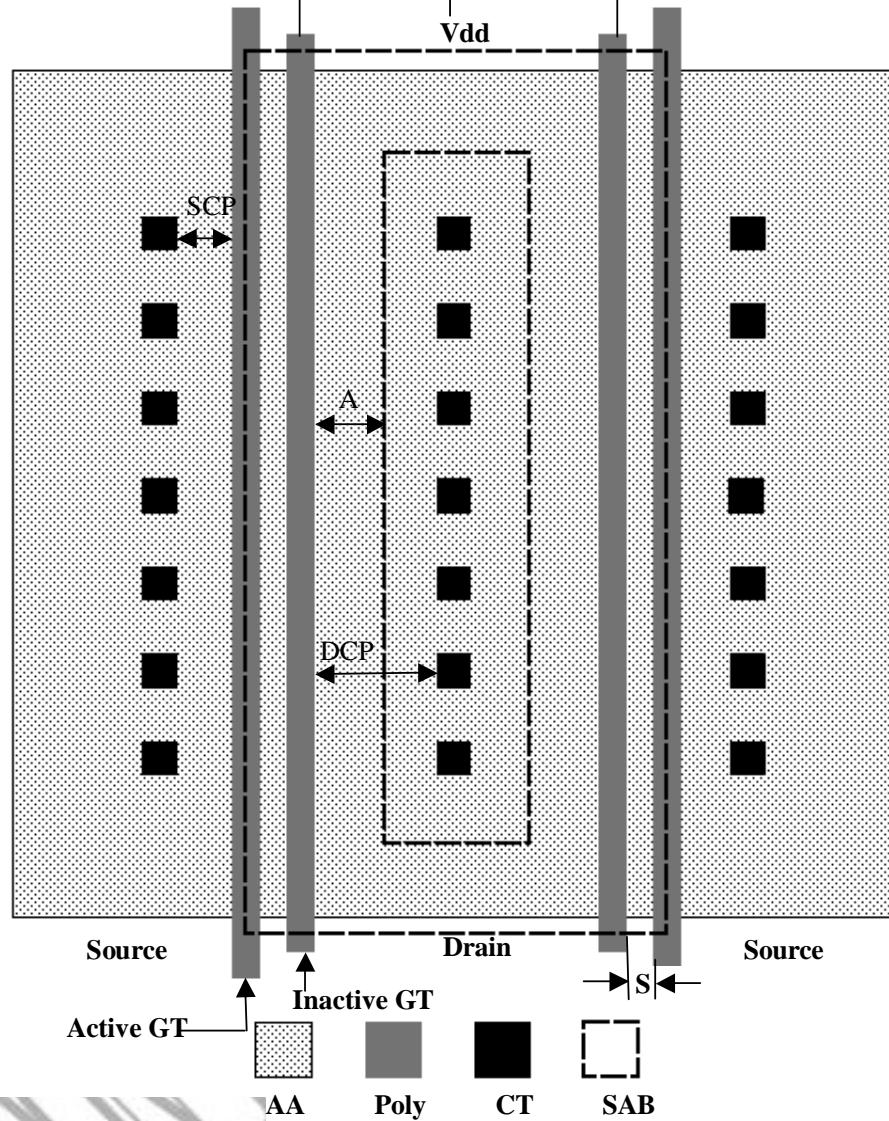


Fig.6 Cascoded NMOS for HV Tolerant I/O (two layout styles of SAB as Fig.4 are allowed)

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7.3.6.3 ESD1 implant layer rules

ESD1 implant layer is an optional layer to define ESD implant location for N type ESD device to improve ESD performance. The implant layer must be drawn in the area that needs ESD implant.

Rule Number	Description	Operation	Design Value	Unit
ESD1.1	ESD1 width.	\geq	0.5	um
ESD1.2	Space between two ESD1s. Merge if space is less than this value.	\geq	0.5	um
ESD1.3	ESD1 area.	\geq	1	um ²
ESD1.4	ESD1 enclosed area.	\geq	1	um ²
ESD1.5	CT enclosure by ESD1.	\geq	0.2	um
ESD1.5a^[R]	The recommended CT enclosure by ESD1.	\geq	0.4	um
ESD1.6	Space between an ESD1 implant to an N-channel Poly gate.	\geq	0.2	um
ESD1.7	ESD1 must be fully covered by AA at least.	\geq	0.2	um
ESD1.8	ESD1 implant region is not allowed to overlap with SP.			
ESD1.9^[NC]	ESD1 must be a drawn layer if there is need of ESD implant.			
ESD1.10	ESD1 isn't allowed to interact with poly in drain side.			

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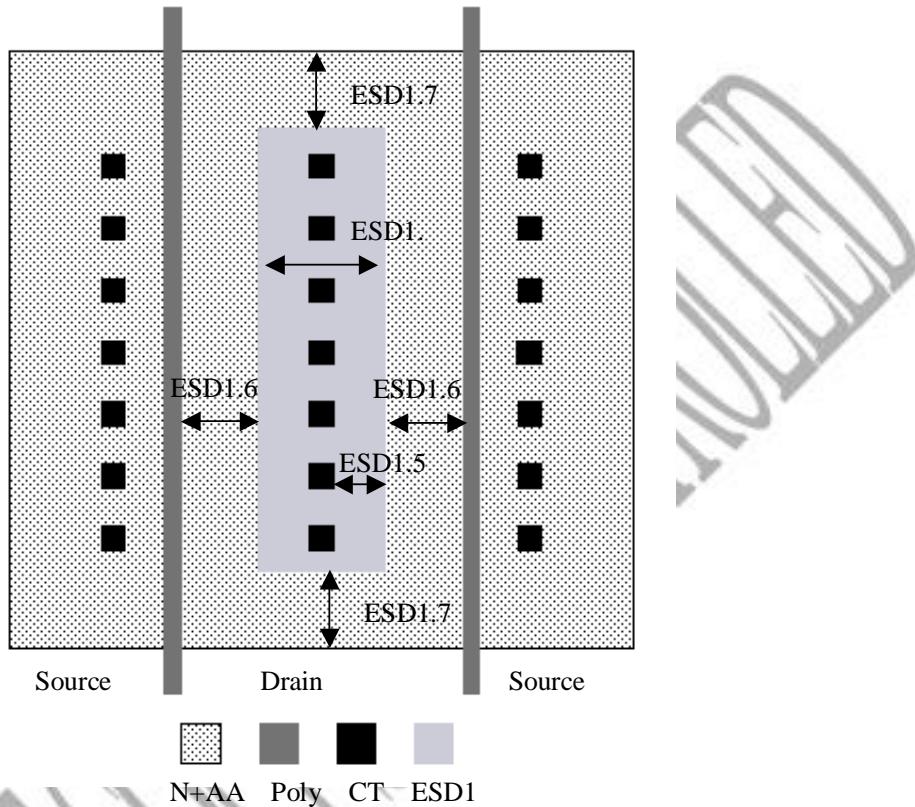


Fig. 7 ESD1 in N type ESD device

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7.3.6.4 Power Clamp guidelines

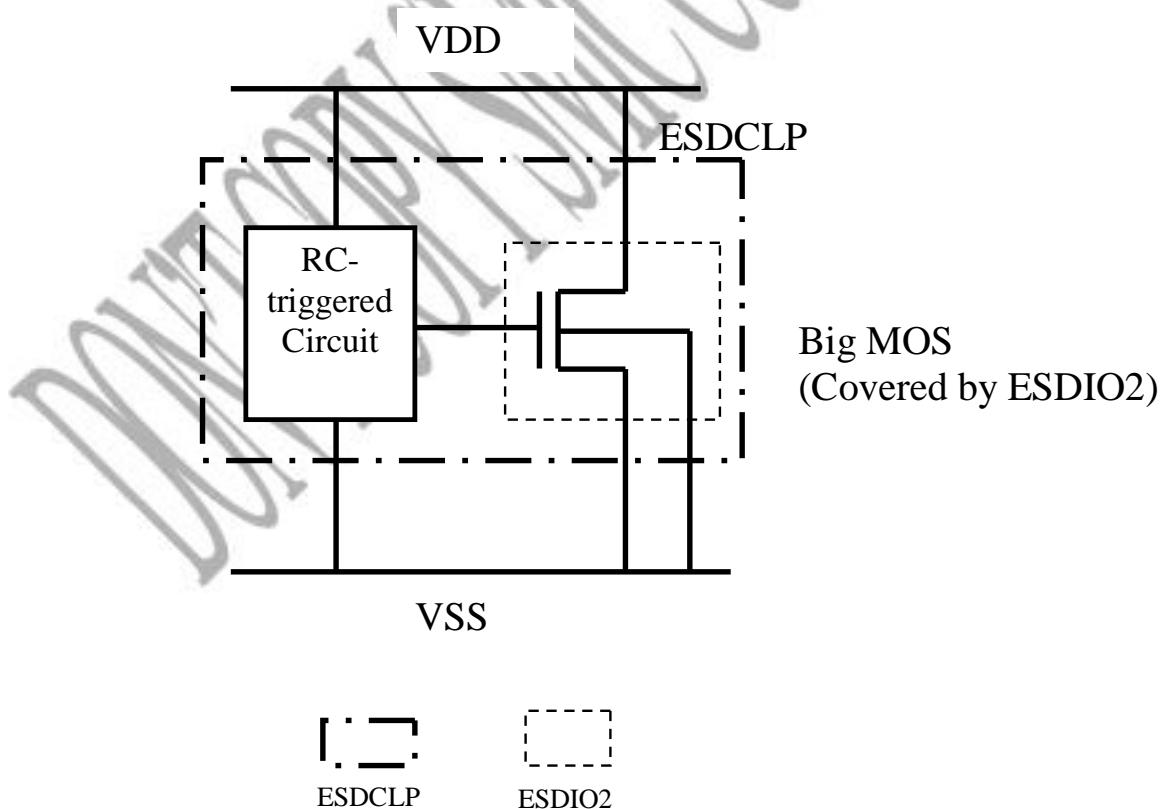
- ESDCLP (41; 2) is the marking layer for ESD RC-triggered power clamp structures connected to a power supply pad.
- Power clamp includes one RC trigger circuit and one big MOS. The trigger circuit will turn on the big MOS during ESD even and keep the big MOS off at normal operation.
- There are two kinds of power clamp devices: one is with SAB using snapback current to discharge (SAB type) and the other is without SAB using the normal turn-on current of MOS to discharge (non-SAB type).
- DRC uses ((N+ AA and ESDCLP and ESDIO2) NOT INTERACT SAB) to recognize non-SAB type power clamp NMOS and ((P+ AA and ESDCLP and ESDIO2) NOT INTERACT SAB) to recognize non-SAB type power clamp PMOS.
- DRC uses ((N+ AA and ESDCLP and ESDIO2) AND INTERACT SAB) to recognize SAB type power clamp NMOS and ((P+ AA and ESDCLP and ESDIO2) AND INTERACT SAB) to recognize SAB type power clamp PMOS.

Rule Number	Description	Operation	Design Value	Unit
ESD.30^[NC]	Finger-type structure with uniform finger width is suggested for both SAB type and non-SAB type Power Clamp.			
ESD.31^[G]	ESD.31a ^[G] , ESD.31b ^[G] and ESD.31c ^[G] are defined for total channel width of non-SAB and SAB type of Power Clamp N/PMOS. For non-SAB type (ESD.31a ^[G] and ESD.31b ^[G]), the total channel width is calculated by the ESD MOS in the same Source or Drain connection. With either one of calculated total channel width with the same source or drain connection larger than the defined value, DRC does not flag the violation. The connectivity can be formed by all metal, via, ALPA, PA and MD but not broken by resistors. For SAB type (ESD.31c ^[G]), the total channel width is calculated by the ESD MOS in the same Drain connection. The connectivity can be formed by all metal, via, ALPA, PA and MD but broken by resistors. SAB is used for drain recognition in DRC runset.			
ESD.31a^[G]	Channel width (W) of core non-SAB type power clamp N/PMOS (Channel width=Finger width x Finger No.)	\geq	1500	um
ESD.31b^[G]	Channel width (W) of 1.8V/2.5V (and all underdrive or overdrive) I/O non-SAB type power clamp N/PMOS (Channel width=Finger width x Finger No.)	\geq	1000	um
ESD.31c^[G]	Channel width (W) of 1.8V/2.5V (and all underdrive or overdrive) I/O SAB type power clamp N/PMOS	\geq	1000	um

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Rule Number	Description	Operation	Design Value	Unit
	(Channel width=Finger width x Finger No.)			
ESD.32^[G]	For non-SAB type power clamp, the spacing of source/drain CT to poly	\geq	0.2	um
ESD.33^[G]	For SAB type power clamp, ESD.2, ESD.4~ESD.10 must follow.			
ESD.34^[G]	For non-SAB type power clamp, ESD.4, ESD.9, ESD.10 must follow			
ESD.35^{[G][NC]}	For core and 1.8V application, non-SAB type power clamp is recommended to use. For 2.5V or higher application voltage, SAB-type power clamp is recommended to use.			



The information contained here: **Fig.8 Power Clamp schematic**
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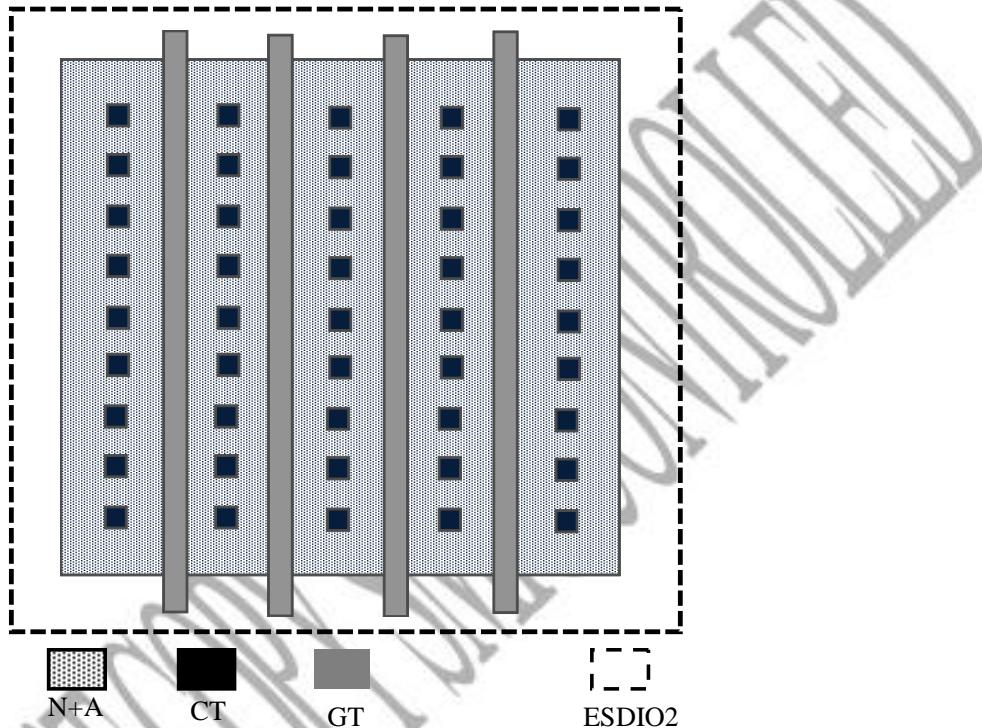


Fig.9 Non-SAB type Power Clamp NMOS (ESDIO2 drawing follow 7.3.5.1)

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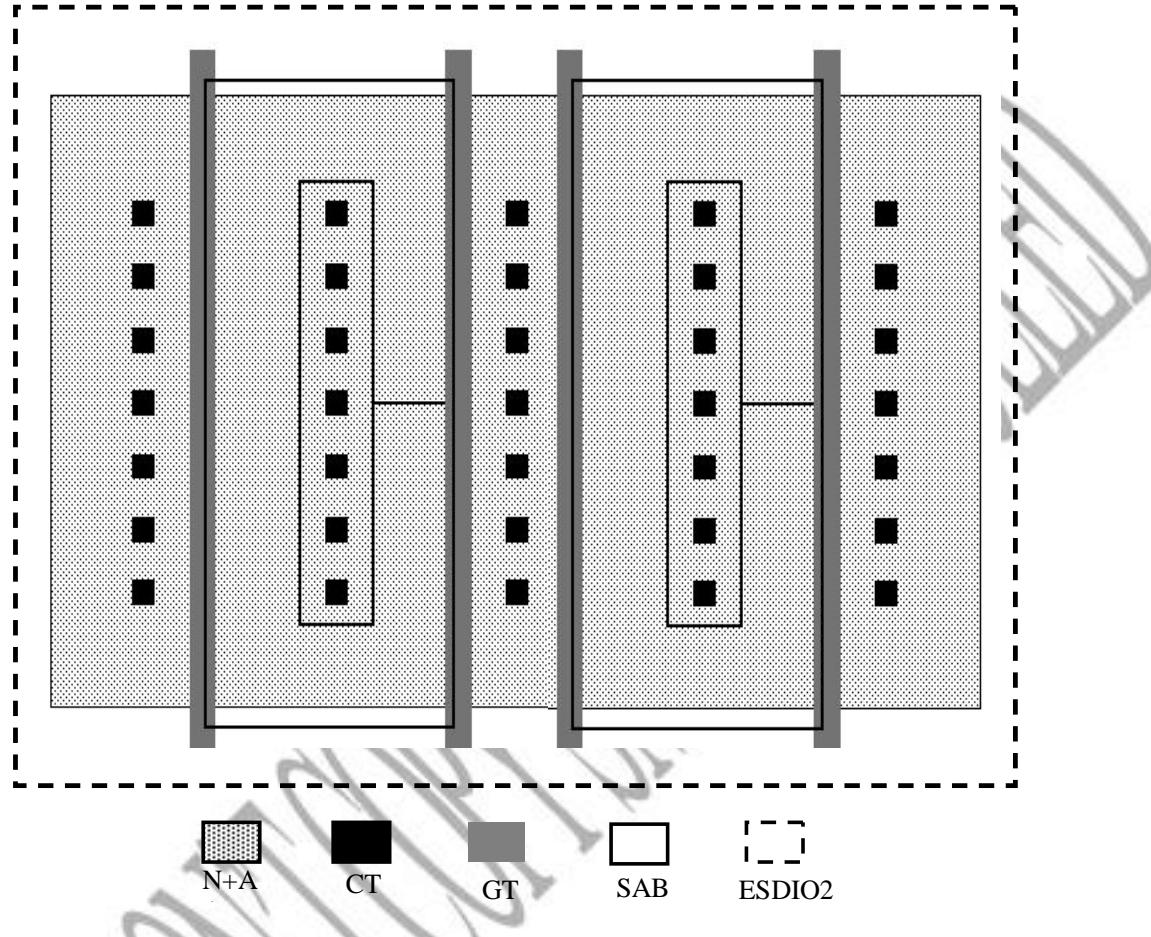


Fig.10 SAB type Power Clamp NMOS (ESDIO2 drawing follows 7.3.5.1; two layout styles of SAB as Fig.4 are allowed)

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7.3.6.5 ESD Diode guidelines

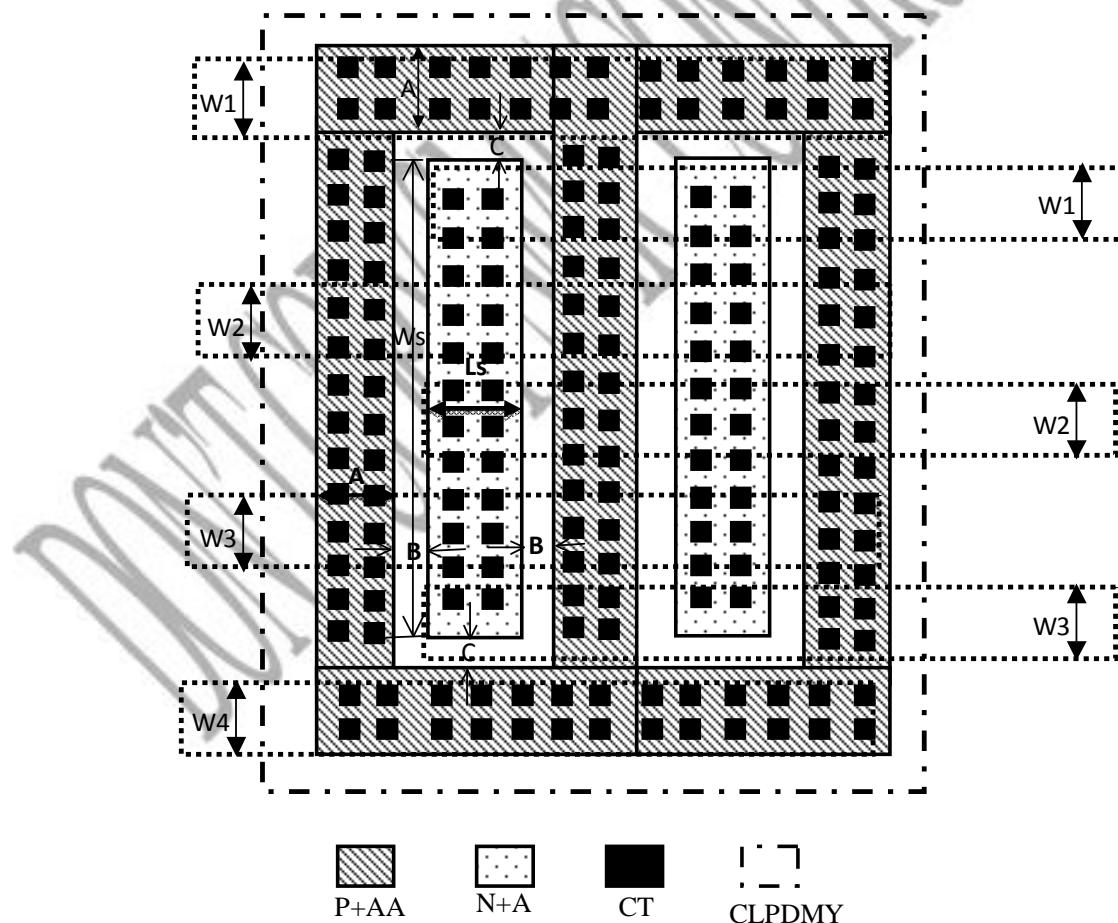
- ESD diode can be used for logic or RF ESD protection.
- ESD level is proportional to the diode perimeter; however, the parasitic capacitance increase at the same time.
- CLPDMY (87; 2) is the marking layer for STI ESD bounded diode; ESDPOB (41; 8) is the marking layer for poly bounded (gated) ESD diode.
- The values in the ESD diode guidelines are the suggested number for design reference; customer can adjust the layout parameters according to the spec/capacitance need.

Rule Number	Description	Operation	Design Value	Unit
ESD.40^{[G][NC]}	Finger-type structure with uniform finger width is suggested for both STI bounded ESD diode and poly bounded ESD diode.			
	ESD.41~ESD.46 are defined for STI ESD diode			
ESD.41^{[G][NC]}	Unit finger length of STI ESD diode (Ls)	\geq	0.5	um
		\leq	1.5	
ESD.42^{[G][NC]}	Unit finger width of STI ESD diode (Ws)	\geq \leq	5 30	um
ESD.43^{[G][NC]}	Total perimeter of STI ESD diode [(L+W)*2]	\geq	400	um
ESD.44^{[G][NC]}	The PW/NW pickup width (A) should be larger than N+AA/P+AA width (L)			
ESD.45^{[G][NC]}	The AA spacing of the longer side of N+AA/P+AA between N+AA/P+AA and PW/NW pickup AA (C)	\geq \leq	0.3 0.4	um
ESD.46^{[G][NC]}	The AA spacing of the shorter side of N+AA/P+AA between N+AA/P+AA and PW/NW pickup AA (B)	\geq \leq	0.6 0.8	um
ESD.47^{[G][NC]}	Only I/O gated diode is allowed, that is gated diode must be covered by DG			
	ESD.48~ESD.50 are defined for gated ESD diode			
ESD.48^{[G][NC]}	Unit finger length of gated ESD diode (Lg)	\geq	0.16	um

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Rule Number	Description	Operation	Design Value	Unit
ESD.49^{[G][NC]}	Unit finger width of gated ESD diode (Wg)	\geq \leq	5 30	um
ESD.50^{[G][NC]}	Total finger width of gated ESD diode (Wg*N)	\geq	360	um
	ESD.48~ESD.50 are defined for both STI ESD diode and gated ESD diode			
ESD.51^{[G][NC]}	Contacts and Vias should be as many as possible			
ESD.52^{[G][NC]}	Total metal width (W1+W2+W3+...) of anode or cathode connected to pad	\geq	20	um



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Fig.11 Multi-finger STI bounded ESD Diode

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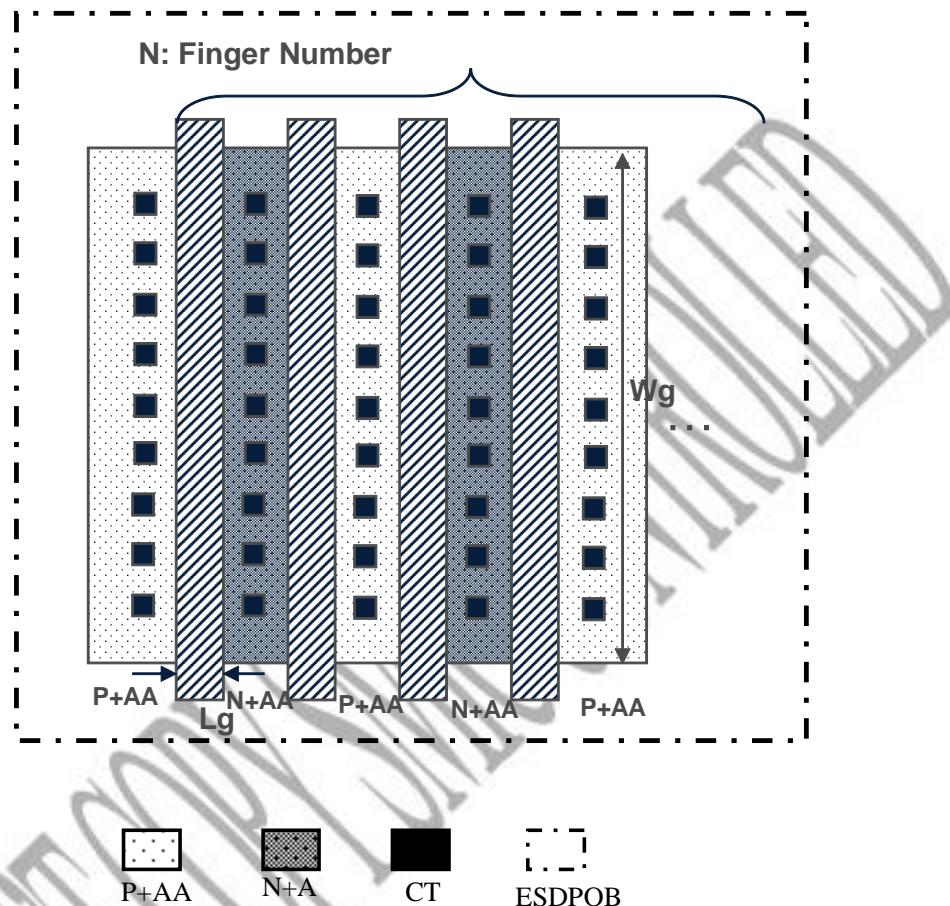


Fig.12 Multi-finger Poly bounded (gated) Diode

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7.3.7 Latch-Up prevention layout guidelines

Rule Number	Description	Operation	Design Value	Unit
LU.1 ^[G]	A double guard ring structure* should be used to surround the NMOS or PMOS AA which connected to an I/O pad and ESD devices. DRC doesn't check OCCD region.			
LU.2 ^[G]	Guard-ring width for NMOS or PMOS with AA connected to an I/O pad and ESD device	\geq	0.2	um
LU.3 ^[G]	LU.3a-LU.3d define minimum space (S1) between NMOS and PMOS with either one of NMOS or PMOS AA connected to I/O pad. The connectivity can be formed by all metal, via, ALPA, PA and MD but not broken by resistors by default. (Fig.1).			
LU.3a ^[G]	For core N/PMOS AA connected to an I/O pad Spacing between NMOS and PMOS.	\geq	2	um
LU.3b ^[G]	For 1.8V N/PMOS AA connected to an I/O pad Spacing between 1.8V NMOS and 1.8V/Core PMOS and Spacing between 1.8V PMOS and 1.8V/Core NMOS.	\geq	2.3	um
LU.3c ^[G]	For 2.5 V N/PMOS AA connected to an I/O pad Spacing between 2.5V NMOS and 2.5V/Core PMOS and Spacing between 2.5V PMOS and 2.5V/Core NMOS.	\geq	3.2	um
LU.3d ^[G]	For 3.3 V N/PMOS (2.5V overdrive) AA connected to an I/O pad Spacing between 3.3V NMOS and 3.3V/Core PMOS and Spacing between 3.3V PMOS and 3.3V/Core NMOS.	\geq	5	um
LU.4 ^[G]	Space (S2) from any point within the Source/Drain region to the nearest pickup AA region inside the same well for I/O and internal circuits. (Fig.2). DRC doesn't check OCCD region.	\leq	35	um
LU.5 ^[NC]	Space between I/O buffer and internal circuit region. (Fig.3).	\geq	15	um
LU.6 ^[NC]	All the guard rings and pickups should be connected to VDD/VSS with low series resistance. That is, NW should be tied together with N+AA, and AA should be tied together with contacts and metals of VDD/VSS. Contacts			

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and Via's should be used as many as possible.

*Double guard ring definition:

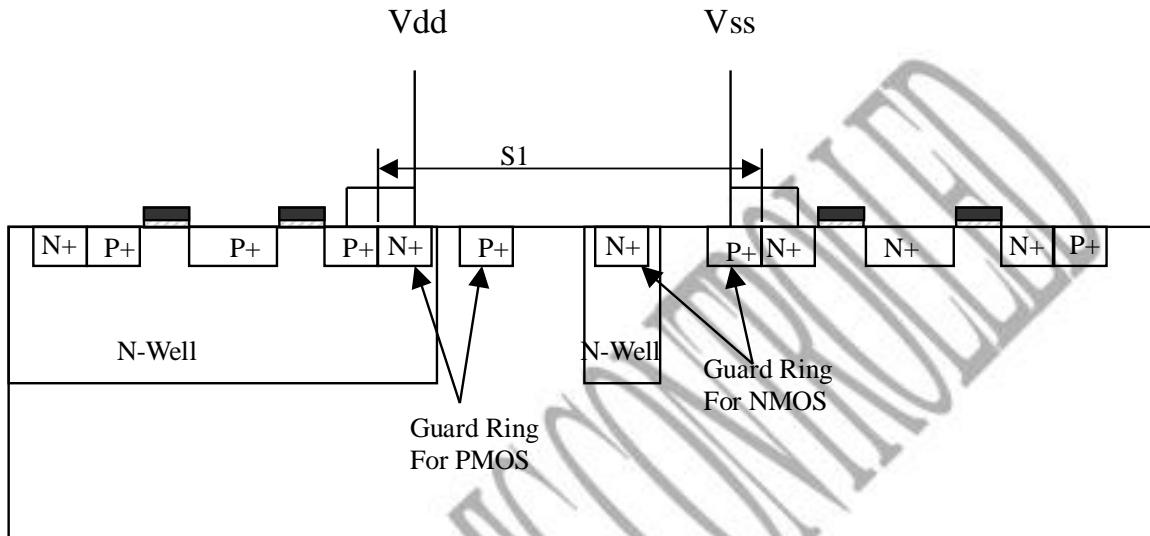
For NMOS, double guard ring includes P+ pickup (tied to Vss) and N+ in NW (tied to Vdd).

For PMOS, double guard ring includes N+ pickup (tied to Vdd) and P+ in PW (tied to Vss).

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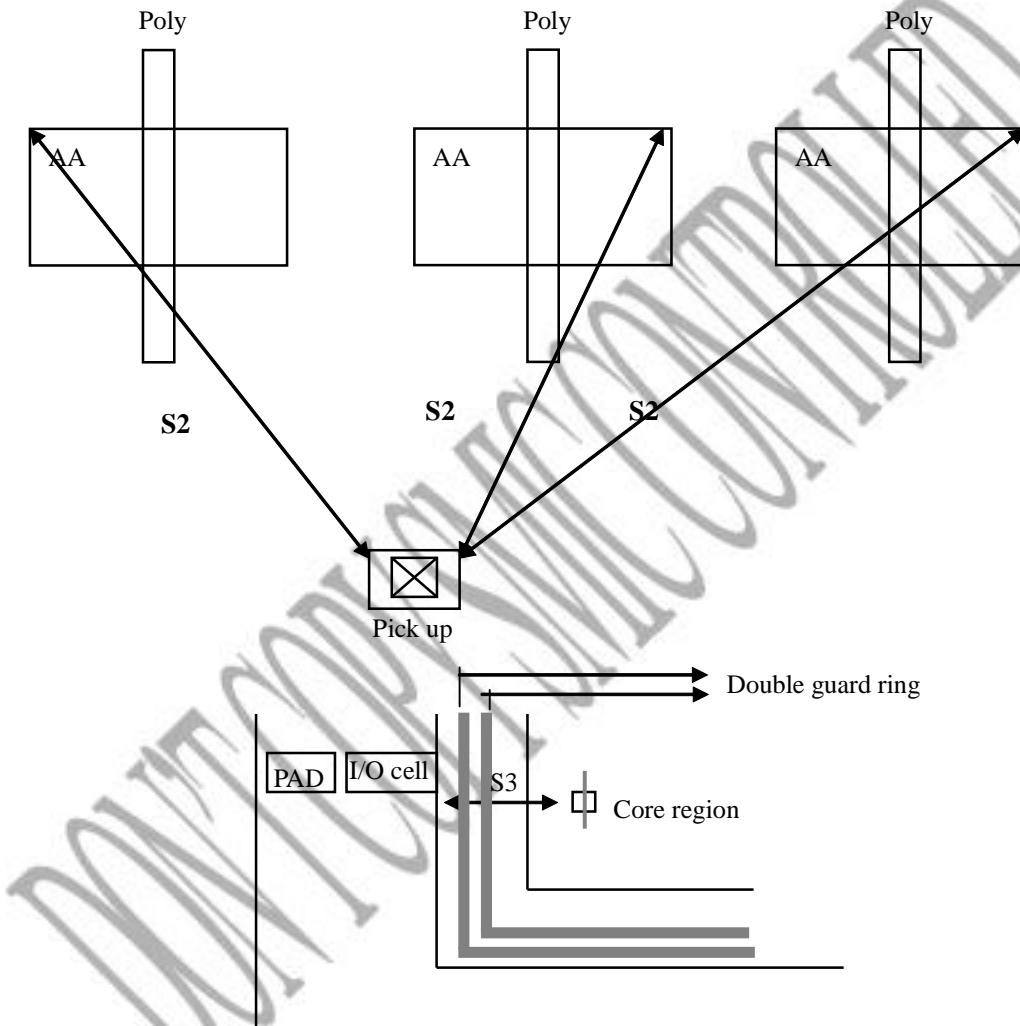
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7.3.7 Fig.2 space (S1) between NMOS and PMOS connected to I/O pad

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7.3.7 Fig.3 illustration of the spacing of MOS AA to pickup AA (S2)

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7.3.8 Redundant Via Insertion Guidelines

For better yield and reliability, it is strongly recommended to utilize SMIC offered qualified Redundant via Auto Insertion utilities to do redundant via insertion wherever the layout and design rules permit. Application notice please refer to redundant via utilities; designers can download the utilities from SMIC NOW.

Features of this utility:

1. The utility strictly follows design rules for these layers Mn, Vn, TMn, TVn and MTT.
2. The new generated redundant vias will be marked by VnRM (n=1-7), TVnRM (n=1-2)
3. For putting redundant vias as required by design rules, metal lines can be extended. Therefore, designers should ensure timing result after using redundant via utilities. Designers also can refer to SMIC offered design reference flow and Placement & Routing for timing analysis.
4. Designers can choose just clean redundant via DRC error or do via layout yield enhancement by switch.
5. There is a configuration for the counts of inserted redundant via, which default value is 1, for reliability and yield enhanced.

The following layers will prevent the utility from redundant via insertion:

1. VnRB (n=1 – 7), TVnRB (n= 1, 2) are the block layers for redundant via auto insertion. User can draw these layers where the DFM Via layout enhancement is not desired, especially for timing or resistance sensitive circuit area.
2. INDMY(212;0), LOGO(26;0), MARKS/MARKG(189;151/189;0), MOMDMY(211;1), MnR(n=1 – 8), TMnR (n=1, 2), DUMBMB(90;0), MnDUB (n=1 – 8), TMnDUB (n= 1, 2), INST/RFSRAM(only follow main rule 1xRVn.5a/1xRVn.5b to insert) , are also redundant via block layers.

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7.3.9 AA/GT/P2/PSR/Metal/Via/ALPA Dummy insertion method selection guideline

- a. This is to guide designers about how to select dummy AA/POLY/P2/PSR/METAL/VIA/ALPA (AADUM, AADOP, GTDUM, GTDOP, P2DUM, PSRDUM, PSRNDUM, M1DUM~M8DUM, M1DOP~M8DOP, B1DUM, B2DUM, B1DOP, B2DOP, TM1DUM, TM2DUM, STM1DM, STM2DM, MTT2DM, ALDUM, V1DUM~V7DUM) insertion method in the utility provided by SMIC. Auto fills dummy is .1 and .7 data type.
- b. SMIC auto dummy fills insertion utility now supports both FEOL and BEOL insertion design manual.
- c. It's strongly recommended designers to use SMIC model based dummy insertion utility to do dummy insertion which has better performance to comply with density rules. Application notice please refer dummy insertion utility; designers can download these utilities from SMIC NOW. In order to get layout uniform and friendly globally for process control, you must to use SMIC's auto dummy insertion utility (document: TD-LO28-DT-2010).
- d. If designers still found DRC violations after use SMIC-provided dummy insertion utilities, SMIC will review the results and take proactive steps to close the DRC violation issues. If you use non-SMIC-provided dummy fill scripts, you must ensure DRC clean, and consult with SMIC.
- e. Please designers ensure timing closure post dummy insertion. It is strongly recommended design to check timing with dummy fillings.
- f. It is recommended to fill on the whole chip again; even dummy fill is done in blocks or chip. It is high risky to use dummy utility only on the instance blocks. We supposed STD cell block area is well defined with dummy fillers because STD cell block area cannot be inserted dummy by SMIC current auto filling dummy utilities.
- g. For RF device or the other concerning circuits with dummy auto insertion, you can draw dummy block layers to prevent dummy auto fill. It is suggest to manually drawing dummy using manual draw dummy rules (.8 data type) but you should make sure this areas are meet DRC density requirement. Please refer to 7.1.11 Device table for dummy insertion.
- h. Need evaluate dummy fills related mask revision, please refer to 7.3.10 Mask Re-tooling Guidelines Related with Dummy Insertion.
- i. It is recommended to fill Metal/VIA dummy using SMIC P&R Metal/VIA Dummy utilities.

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7.3.10 Mask Re-tooling guidelines

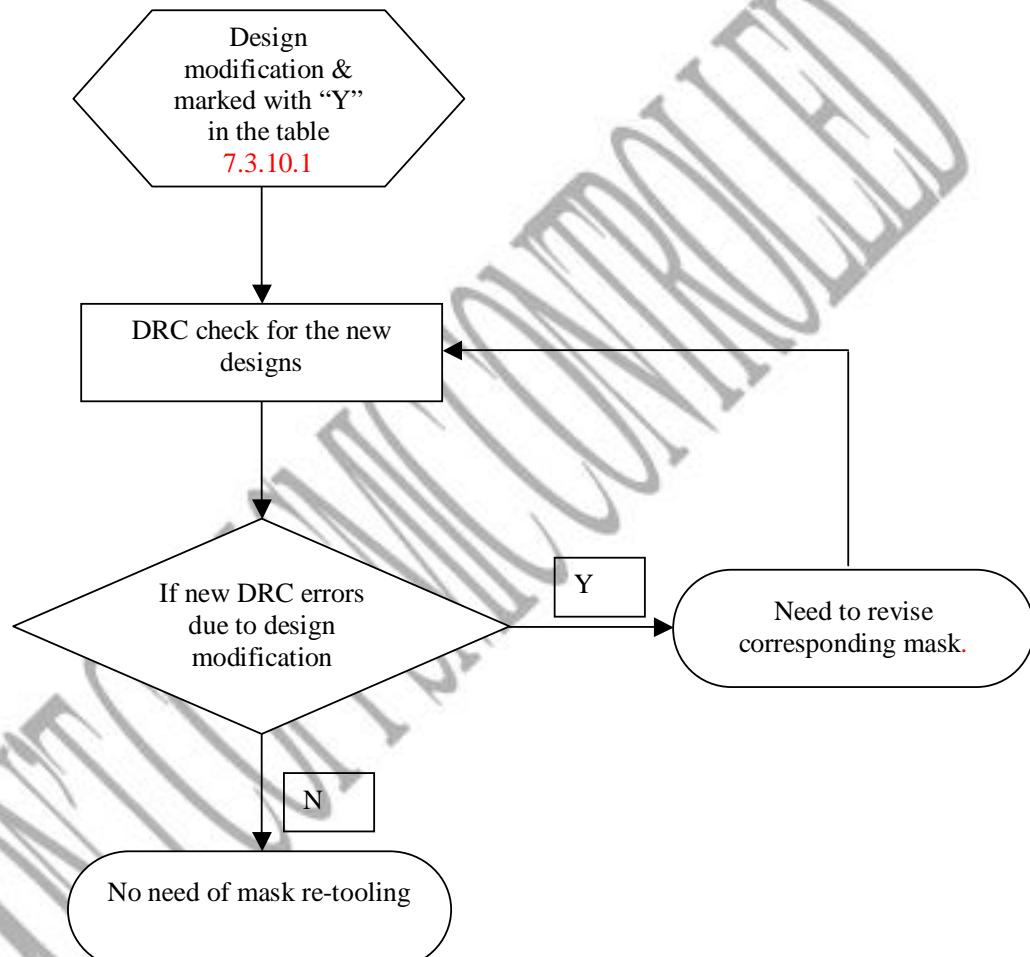
This section provides guidelines to judge which masks related with dummy insertion need to re-tool in case of GDS modification. Table 7.3.10.1 is the GDS and Mask relationship through dummy pattern interaction. The “Y” and “N” stands for impact level in this table: “Y” is high risk of mask re-tooling; need to run DRC to evaluate if need mask re-tooling, follow flow chart of 7.3.10.2; “N” is no need of re-tooling

7.3.10.1 Table of GDS and Mask relationship through dummy pattern interaction

Related Mask ->	AA	GT	Mx (x=1~8)	Vy (y=1~7)	TMn	MTT2	ALPA
Related Dummy Layer ->	AADUM ,AADOP	GTDUM, GTDOP	MxDUM, MxDOP	VyDUM	TMnDUM	MTT2DM	ALDUM
Modified GDS Layer	AA	Y	Y	N	N	N	N
	AADMP	Y	Y	N	N	N	N
	GT	Y	Y	N	N	N	N
	GTDMP	Y	Y	N	N	N	N
	Mn	N	N	Y	Y	N	N
	TMn	N	N	N	Y	N	N
	Vn	N	N	Y	Y	N	N
	MTT2	N	N	N	N	Y	N
	ALPA	N	N	N	N	N	Y
	DUMB	Y	Y	N	N	N	N
	DUMB	Y	Y	N	N	N	N
	DUMB	N	N	Y	Y	Y	Y
	MnDUB(n=1~8)	N	N	Y	Y	N	N
	VnDUB (n=1~7)	N	N	Y	Y	N	N
	TMnDUB(n=1~2)	N	N	N	N	Y	N
	MTT2DB	N	N	N	N	Y	N
	ALDUB	N	N	N	N	N	Y
	NODMF	Y	Y	Y	Y	Y	Y
	LOGO	Y	Y	Y	Y	Y	Y
	RESAA	Y	Y	N	N	N	N
	RESNW	Y	Y	N	N	N	N
	RESP2	Y	Y	N	N	N	N
	INDMY	N	N	Y	Y	N	Y
	INST/RFSRAM	Y	Y	N	N	N	N
	MARKS/MARKG	Y	Y	Y	Y	Y	Y
	P4	Y	Y	N	N	N	N

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7.3.10.2 Flow chart of dummy related re-tooling evaluation procedures.

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7.3.11 Inline OCCD and OCOVL monitor cell guidelines

7.3.11.1 OCCD On chip CD cell guidelines

The purpose of on chip CD (CAD layer OCCD: 91;4) structure is to enable FEOL AA, Poly and BEOL metal layers' CD uniformity measurement and control within a large chip. This section describes the guidelines of OCCD structure placement.

SMIC provides OCCD GDS files for insertion. The CAD layer OCCD (91;4) is must for both FEOL and BEOL OCCD GDS cell. Two types of FEOL OCCD GDS are provided for different direction, one is horizontal direction FEOL OCCD cell, using CAD layer OCCDFH (91;6); another is vertical direction FEOL OCCD cell, using CAD layer OCCDFV (91;7). The Polys in OCCDFH or OCCDFV are all in vertical direction, which is same with the GATE direction of core device region. One BEOL OCCD GDS is provided, using CAD layer OCCDB (91;10). OCCD (91;4) layer drawn size is identical to each OCCD cell marker layer: OCCDFH, OCCDFV, OCCDB..

FEOL horizontal OCCD gds: IDCD_SMIC_FEOL_H0.gds

FEOL vertical OCCD gds: IDCD_SMIC_FEOL_V0.gds

BEOL OCCD gds: 28nm_OCCD_SMIC_BEOL.gds (SMIC provide 8 layers for 1xMn GDS sample, it needs designer to modify GDS based on own metal layers)

SMIC also provides the OCCD block layer to exclude OCCD cell insertion, so if designers don't want to insert OCCD cell in certain design region, please draw OCCD block layers below:

FEOL OCCD cell block layer: OCCDFDB (91;8); BEOL OCCD cell block layer: OCCDBDB (91;9).

OCCD structures can be placed with following design rule or using SMIC auto insertion utility (xxx) to achieve suggested distribution.

Rule Number	Description	Operation	Design Value	Unit
OCCD.1 ^{[G][NC]}	Insert one OCCD structure in each 2000um ² x2000um ² window of chip. No insertion of OCCD if window size smaller than 1000um x 1000um. It needs insert OCCD when chip window size is >1000um x 1000um, and <2000um x 2000um.			
OCCD.2 ^[G]	Space between two OCCD structures, which each OCCD structure in each 2000um x 2000um window.	≥	150	um
OCCD.3 ^[G]	Space between OCCDFH/OCCDFV to AA, poly, SN, SP, P4 LOGO, MARKS, MARKG, DUMBA, DUMB _P outside of OCCD	≥	2	um
OCCD.4 ^[G]	At least insert one OCCD structure in two neighboring 2000um x 2000um window of chip.			
OCCD.5 ^[G]	OCCDFH/OCCDFV overlap of DG, PSUB, EFUSE, SAB, RESAA, RESP1, RESP2, VARMOS, LVT_N, LVT_P, INST, ESDIO1, ESDIO2, ESDCLP,			

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Rule Number	Description	Operation	Design Value	Unit
	ESDPOB, CLPDMY, BIPOLA, INDMY, MOMDMY is not allowed.			
OCCD.6 ^[G]	OCCDB can't overlap with CT, MnDUM(n=1~8), MnDOP(n=1~8), VnDUM(n=1~7), or INDMY			
OCCD.7 ^[G]	OCCDFH and OCCDFV can't overlap each other			
OCCD.8 ^[G]	OCCDFH and OCCDFV can't interact with OCOVL			
OCCD.9 ^[G]	Poly in OCCDFH/OCCDFV must be in vertical direction.			
OCCD.10 ^{[G][INC]}	Mirror or 180° rotation on OCCD structure in X,Y is allowed, 90° or 270° rotation is not allowed			
OCCD.11 ^{[G][INC]}	OCCD(91;4) must cover all OCCD cell structures, Following rules can be waived inside OCCD:			

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7.3.11.2 OCOVL On chip cell guidelines

The purpose of on chip OVL (CAD layer, OCOVL: 91;5) structure is to enable the overlay measurement and control within a big chip. It will rationalize the overlay target distribution in field and enable high order correction modeling.

SMIC provides two types of on chip OVL marks, OVL mark of Poly to AA (OVL_GT_AA), and OVL mark of CT to Poly (OVL_CT_GT).

One OCOVL cell GDS is offered combined OVL_GT_AA and OVL_GT_AA in both horizontal and vertical direction. The CAD layer OCOVL (91;5) is must for on chip OVL cell.

OCOVL cell GDS: !DOVSMIC_N.gds

OCOVL structures can be placed with following design rule or using SMIC auto insertion utility (xxx) to achieve suggested distribution.

Rule number	Description	Operation	Design value	Unit
OCOVL.1 ^[G] ^[NC]	Insert one OCOVL structure in each 2000x2000 um ² window of chip. No insertion of OCOVL if window size smaller than 1000um x 1000um. It needs insert OCCD when chip window size is >1000um x 1000um, and <2000um x 2000um.			
OCOVL.2 ^[G]	Space between two OCOVL structures DRC check methodology for the maximum space: (((NOT (OCOVL) sd 6500um) su 6500um)	≥	2000	um
		≤	13000	um
OCOVL.3 ^[G]	Space between OCOVL to AA, Poly, SN, SP, P4, CT, M1, LOGO, MARKS, MARKG, DUMBA, DUMB, DUMB, DUMB outside of OCOVL	≥	2	um
OCOVL.4 ^[G] ^[NC]	Mirror or 180o rotation on OCOVL structure in X,Y is allowed, 90o or 270o rotation is not allowed			
OCOVL.5 ^[G] ^[NC]	OCOVL (91;5) must cover OCOVL cell structures. Following rules can be waived inside OCOVL:			

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7.4 Dummy Check Rule

Dummy AA include layer AADUM (10; 1) and AADOP (10; 7).

Dummy GT include layer GTDUM (30; 1) and GTDOP (30; 7).

Dummy P2 include layer P2DUM (31; 1).

Dummy 1x Metal include layer MnDUM (6n; 1) and MnDOP (6n; 7), n=1~8.

Dummy 2x Metal include layer BnDUM (14n; 1), n=1~2.

Dummy 8x Metal include layer TM1DUM (120; 1) and TM2DUM (122; 1).

Dummy 10x Metal include layer STM1DM (228; 1) and STM2DM (229; 1).

Dummy 1x Via include layer VnDUM (7n; 1), n=0~6.

Dummy MTT2 include layer MTT2DM (231; 1).

Dummy ALPA include layer ALDUM (83; 11).

AA dummy check rules

Rule No.	Description	Operation	Design Value	Unit
DUMC_AA.00	DRC also check the poly dummy and flag the violations on main rules: AA.1, AA.4, AA.5, AA.7, AA.11, AA.31, AA.32, AA.33, AA.34, AA.39			
DUMC_AA.01	(AADUM or AADOP) width.	\geq	0.1	um
DUMC_AA.02	Space between AADUM and AADUM.	\geq	0.19	um
DUMC_AA.03	Space between AADUM and AADOP.	\geq	0.2	um
DUMC_AA.04	Space between AADUM and GTDUM.	\geq	0.025	um
DUMC_AA.05	Space between AADUM and GTDOP.	\geq	0.2	um
DUMC_AA.06	Space between AADOP and AADOP outside DG/TG	\geq	0.13	um
DUMC_AA.07	Space between AADOP and AADOP not outside DG/TG	\geq	0.15	um
DUMC_AA.08	Space between AADOP and GTDOP.	\geq	0.025	um
DUMC_AA.09	Space between AADOP and GTDUM.	\geq	0.2	um
DUMC_AA.10	(AADUM or AADOP) area (in um ²).	\geq	0.03	um ²
DUMC_AA.11	(AADUM or AADOP) must not interact (AA, Poly, AADMP, GTDMP, P2, DUMBA, NODMF, RESNW, RESP2, MARKG, MARKS, INST, RFSRAM) layers.			
DUMC_AA.12	Space between (AADUM or AADOP) and (DUMBA, NODMF, RESP2, MARKG, MARKS, INST, RFSRAM) layers.	\geq	0.4	um
DUMC_AA.13	Space between (AADUM or AADOP) and (AA, poly, AADMP, GTDMP).	\geq	0.15	um

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DUMC_AA.14	(AADUM or AADOP) overlap with CT is not allowed.			um
DUMC_AA.15	Space between (AADUM or AADOP) and SAB.	≥	0.22	um
DUMC_AA.16	(AADUM or AADOP) enclosed by SAB, (AADUM or AADOP) cut SAB is not permitted	≥	0.22	um
DUMC_AA.17	Space between (AADUM or AADOP) and P2	≥	0.04	um
DUMC_AA.18	Space between (AADUM or AADOP) and RESNW	≥	0.6	um
DUMC_AA.19	Space between AADUM and NW.	≥	0.16	um
DUMC_AA.20	AADUM enclosed by NW, AADUM cut NW is not permitted.	≥	0.16	um
DUMC_AA.21	Space between AADOP and NW.	≥	0.1	um
DUMC_AA.22	AADOP enclosed by NW, AADOP cut NW is not permitted.	≥	0.1	um
DUMC_AA.23	Space between 45-degree AA and (AADUM or AADOP).	≥	0.45	um
DUMC_AA.24	Space between AADOP and PSUB.	≥	0.15	um
DUMC_AA.25	Space between AADUM and DUMBA.	≥	0.6	um
DUMC_AA.26	Space between (AADUM or AADOP) and DG/TG.	≥	0.08	um
DUMC_AA.27	(AADUM or AADOP) enclosed by DG/TG, (AADUM or AADOP) cut DG/TG is not permitted.	≥	0.08	um
DUMC_AA.28	Space between (AADUM or AADOP) and SP.	≥	0.07	um
DUMC_AA.29	(AADUM or AADOP) enclosed by SP, (AADUM or AADOP) cut SP is not permitted.	≥	0.07	um
DUMC_AA.30	Space between (AADUM or AADOP) and INDMY.	≥	1.2	um
DUMC_AA.31	AADUM extension GTDUM	≥	0.095	um
DUMC_AA.32	AADOP extension GTDOP	≥	0.075	um
DUMC_AA.33	Space between (AADUM or AADOP) and (OCCDFH, OCCDFV, OCOVL) mark layer.	≥	0.6	um
DUMC_AA.34	Space between (AADUM or AADOP) and CT	≥	0.05	um

Poly dummy check rules

DUMC_GT.00	DRC also check the poly dummy and flag the violations on main rules: GT.1, GT.4, GT.12, GT.43, GT.40, GT.45, GT.46, GT.48.			
DUMC_GT.01	(GTDUM or GTDOP) width.	~	0.02	~

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DUMC.GT.02	(GTDUM or GTDOP) length.	≥	0.3	um
DUMC.GT.03	Space between (GTDUM or GTDOP) and (GTDUM or GTDOP) if at least one (GTDUM or GTDOP) width $\geq 0.03\text{um}$, and $\leq 0.09\text{um}$, and the parallel run length $>0.09\text{um}$.	≥	0.1	um
DUMC.GT.04	Space between (GTDUM or GTDOP) and (GTDUM or GTDOP) if at least one (GTDUM or GTDOP) width $> 0.09\text{um}$, and the parallel run length $>0.09\text{um}$.	≥	0.12	um
DUMC.GT.05	Space between GTDOP and GTDOP.	≥	0.1	um
DUMC.GT.06	Space between GTDUM and GTDOP.	≥	0.2	um
DUMC.GT.07	(GTDUM or GTDOP) area (in um^2).	≥	0.0138	um^2
DUMC.GT.08	(GTDUM or GTDOP) must not interact (AA, Poly, AADMP, GTDMP, P2, SAB, DUMBP, NODMF, RESAA, RESNW, RESP2, MARKG, MARKS, INST, RFSRAM) layers.			
DUMC.GT.09	Space between (GTDUM or GTDOP) and (DUMBP, NODMF, RESAA, RESNW, RESP2, MARKG, MARKS, INST, RFSRAM) layers.	≥	0.4	um
DUMC.GT.10	Space between (GTDUM or GTDOP) and (AA, poly, AADMP, GTDMP).	≥	0.15	um
DUMC.GT.11	Space between (AADUM or AADOP) and (GTDUM or GTDOP) on field oxide (On STI).	≥	0.025	um
DUMC.GT.12	Space between (GTDUM or GTDOP) and P4.	≥	0.04	um
DUMC.GT.13	(GTDUM or GTDOP) overlap with CT is not allowed.			
DUMC.GT.14	(GTDUM or GTDOP) enclosed by P4, (GTDUM or GTDOP) cut P4 is not permitted.	≥	0.04	um
DUMC.GT.15	Space between (GTDUM or GTDOP) and SAB	≥	0.38	um
DUMC.GT.16	Space between GTDOP and P2	≥	0.04	um
DUMC.GT.17	Space between GTDUM and P2.	≥	0.3	um
DUMC.GT.18	Space between (GTDUM or GTDOP) and INDMY	≥	1.2	um
DUMC.GT.19	Space between (GTDUM or GTDOP) and CT	≥	0.08	um
DUMC.GT.20	Space between (GTDUM or GTDOP) and Poly_JOG	≥	0.17	um
DUMC.GT.21	GTDUM extension AADUM	≥	0.085	um
DUMC.GT.22	GTDOP extension AADOP	≥	0.08	um

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DUMC.GT.23	Space between (AADUM or AADOP) and (OCCDFH, OCCDFV, OCOVL) mark layer.	≥	0.6	um
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P2 dummy check rules

DUMC.P2.00	DRC also check the poly dummy and flag the violations on main rules: P2.2, P2.4, P2.13, P2.15, P2.16			
DUMC.P2.01	P2DUM width.	≥	0.08	um
DUMC.P2.02	P2DUM length.	≥	0.15	um
DUMC.P2.03	Space between P2DUM and (P2, P2DUM).	≥	0.09	um
DUMC.P2.04	Space between P2DUM and ((poly or GTDMP) or (GTDUM or GTDOP)). Overlap between P2DUM and ((poly or GTDMP) or (GTDUM or GTDOP)) is not allowed.	≥	0.04	um
DUMC.P2.05	Space between P2DUM and ((AA or AADMP) or (AADUM or AADOP)).	≥	0.035	um
DUMC.P2.06	Space between P2DUM and CT (overlap is not allowed).	≥	0.02	um
DUMC.P2.07	Space between P2DUM and (DG or PSUB or TG).	≥	0.06	um
DUMC.P2.08	P2DUM must not interact (AA, Poly, GTDMP, AADMP, GTDUM, AADUM, GTDOP, AADOP, P2, DG, PSUB, TG) layers.			
DUMC.P2.09	Area of P2DUM.	≥	0.01	um ²
DUMC.P2.10	(P2 or P2DUM) full chip density	≥	5%	
DUMC.P2.11	Space between P2DUM and (OCCDFH, OCCDFV, OCOVL) mark layer.	≥	0.6	um

M1 dummy check rules

DUMC.M1.00	DRC also check the M1 dummy and flag the violations on main rules: M1.1, M1.3, M1.5a, M1.5b, M1.5c, M1.5d, M1.5e, M1.5f, M1.5g, M1.6a, M1.6b, M1.8, M1.9, M1.17, M1.18			
DUMC.M1.01	(M1DUM or M1DOP) width.	≥	0.07	um
DUMC.M1.02	Space between two (M1DUM or M1DOP).	≥	0.08	um
DUMC.M1.03	Dummy M1 area (um2).	≥	0.0238	um ²
DUMC.M1.04	Space between (M1DUM or M1DOP) and (M1, V1).	≥	0.16	um

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DUMC.M1.05	(M1DUM or M1DOP) can not interact MTFUSE ; Space between dummy M1 and MTFUSE .	≥	1	um
DUMC.M1.06	(M1DUM or M1DOP) must not interact (M1, V1, DUMBMB, NODMF, M1DUB, MARKG, MARKS) layers.			
DUMC.M1.07	Space between (M1DUM or M1DOP) and (DUMBMB, NODMF, M1DUB, MARKG, MARKS, OCCDB) layers.	≥	0.6	um

1x Mn: 1x Metal (M2~ M8) dummy check rules

DUMC.Mn.00	DRC also check the 1x Mn dummy and flag the violations on main rules: 1xMn.1, 1xMn.3, 1xMn.4a, 1xMn.4b, 1xMn.4c, 1xMn.4d, 1xMn.4e, 1xMn.4f, 1xMn.4g, 1xMn.4h, 1xMn.5a, 1xMn.5b, 1xMn.6, 1xMn.7, 1xMn.15, 1xMn.16, 1xMn.17			
DUMC.Mn.01	(MnDUM or MnDOP (n=2~8)) width.	≥	0.07	um
DUMC.Mn.02	Space between two (MnDUM or MnDOP (n=2~8)).	≥	0.08	um
DUMC.Mn.03	(MnDUM or MnDOP (n=2~8)) area (um2).	≥	0.0238	um ²
DUMC.Mn.04	Space between (MnDUM or MnDOP (n=2~8)) and Mn ((M2~M8), Vn (n=2~7), Vn-1 (n=2~8)).	≥	0.16	um
DUMC.Mn.05	(MnDUM or MnDOP (n=2~4)) can not interact MTFUSE ; Space between (MnDUM or MnDOP (n=2~4)) and MTFUSE .	≥	1	um
DUMC.Mn.06	(MnDUM or MnDOP (n=2~8)) must not interact (Mn (M2~M8), Vn (V2~V7), Vn-1 (n=2~8), DUMBMB, NODMF, MnDUB (n=2~8), MARKG, MARKS) layers.			
DUMC.Mn.07	Space between (MnDUM or MnDOP, n=2~8) and (DUMBMB, NODMF, MnDUB (n=2~8), MARKG, MARKS, OCCDB) layers.	≥	0.6	um

2x Bn: 2x Metal (B1, B2) dummy check rules

DUMC.Bn.00				
DUMC.Bn.01	Dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) width.	≥	0.20	um
DUMC.Bn.02	Space between two dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP).	≥	0.20	um
DUMC.Bn.03	Dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) area (um2).	≥	0.16	um ²
DUMC.Bn.04	Space between dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) and Bn (B1, B2) pattern.	≥	0.30	um

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DUMC.Bn.05	Dummy Bn (B1DUM, B1DOP, B2DUM, B2DOP) must not interact (Bn (B1, B2), BnDUB (B1DUB, B2DUB), DUMB, NODMF, MARKG, MARKS) layers.			
DUMC.Bn.06	Space between dummy Bn (B1DUM, B1DOP, B2DUM, and B2DOP) and (BnDUB (B1DUB, B2DUB), DUMB, NODMF) layers.	≥	0.50	um
DUMC.Bn.07	Space between dummy Bn (B1DUM, B1DOP, B2DUM, and B2DOP) and (MARKG, MARKS) layers.	≥	1.00	um

8x TMn: 8x Metal (TM1, TM2) dummy check rules

DUMC.TMn.0	DRC also check the 10xMn dummy and flag the violations on main rules: 8xTMn.1, 8xTMn.2a, 8xTMn .2b, 8xTMn .2c, 8xTMn .3, 8xTMn .4			
DUMC.TMn.1	Dummy TMn (TM1, TM2) width.	≥	0.75	um
DUMC.TMn.2	Space between two dummy TMn (TM1, TM2).	≥	0.75	um
DUMC.TMn.3	Dummy TMn (TM1, TM2) area (um2).	≥	1.5	um ²
DUMC.TMn.4	Space between dummy TMn (TM1, TM2) and TMn (TM1, TM2) pattern.	≥	0.75	um
DUMC.TMn.5	Dummy TMn (TM1, TM2) must not interact (TMn (TM1, TM2), TVn (TV1, TV2), DUMB, NODMF, TMnDUB (n=1, 2), MARKG, MARKS) layers.			
DUMC.TMn.6	Space between dummy TMn (TM1, TM2) and (DUMB, NODMF, TMnDUB (n=1, 2), MARKG, MARKS) layers.	≥	0.7	um

10x STMn: 10x Metal (STM1, STM2) dummy check rules

DUMC.STMn.00	DRC also check the 10x TMn dummy and flag the violations on main rules: 10xTMn .1, 10xTMn .2a, 10xTMn .2b, 10xTMn .2c, 10xTMn .3, 10xTMn .4			
DUMC.STMn.01	Dummy STMn (STM1DM, STM2DM) width.	≥	0.75	um
DUMC.STMn.02	Space between two dummy STMn (STM1DM, STM2DM).	≥	0.75	um
DUMC.STMn.03	Dummy STMn (STM1DM, STM2DM) area (um2).	≥	1.5	um ²
DUMC.STMn.04	Space between dummy STMn (STM1DM, STM2DM) and STMn (STM1DM, STM2DM) pattern.	≥	0.75	um
DUMC.STMn.05	Dummy STMn (STM1DM, STM2DM) must not interact (STMn (STM1, STM2), STVn (STV1, STV2), DUMB, NODMF, STMnDB (n=1, 2), MARKG, MARKS) layers.			

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DUMC.STMn.06	Space between dummy STMn (STM1DM, STM2DM) and (DUMBM, NODMF, STMnDB (n=1, 2), MARKG, MARKS) layers.	≥	0.7	um
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V1 dummy check rules

DUMC.V1.00	DRC also check the V1 dummy and flag the violations on main rules: 1xVn.2a, 1xVn.2b, 1xVn.3, 1xVn.3a , 1xVn.3b, 1xVn.3c , 1xVn.3d , 1xVn.4, 1xVn.4a , 1xVn.4b , 1xVn.4c , 1xVn.4d , 1xVn.8			
DUMC.V1.01	V1DUM exact width (square shape).	=	0.05	um
DUMC.V1.02	Space between two V1DUM.	≥	0.35	um
DUMC.V1.03	Enclosure by M1DUM; overlap with M1DOP is not permitted; and must be fully cover by M1DUM.	≥	0.055	um
DUMC.V1.04	Enclosure by M2DUM; overlap with M2DOP is not permitted; and must be fully cover by M2DUM.	≥	0.055	um
DUMC.V1.05	V1DUM must not interact (V1, M1, M2, V1DUB, MARKG, MARKS, NODMF, DUMBM, INDMY, OCCDB) layers.			

1x Vn: 1x Via (V2~ V7) dummy check rules

DUMC.1xVn.00	DRC also check the V1 dummy and flag the violations on main rules: 1xVn.2a, 1xVn.2b, 1xVn.3, 1xVn.3a , 1xVn.3b, 1xVn.3c , 1xVn.3d , 1xVn.4, 1xVn.4a , 1xVn.4b , 1xVn.4c , 1xVn.4d , 1xVn.8			
DUMC.1xVn.01	VnDUM (n=2~7) exact width (square shape).	=	0.05	um
DUMC.1xVn.02	Space between two VnDUM (n=2~7).	≥	0.35	um
DUMC.1xVn.03	Enclosure by MnDUM (n=2~7) and MnDUM (n=2~7) is the metal layer directly underneath VnDUM (n=2~7); overlap with MnDOP (n=2~7) is not permitted; and must be fully cover by MnDUM (n=2~7).	≥	0.055	um
DUMC.1xVn.04	Enclosure by MnDUM (n=3~8) and MnDUM (n=3~8) is the metal layer directly above VnDUM (n=2~7); overlap with MnDOP (n=2~7) is not permitted; and must be fully cover by MnDUM (n=3~8).	≥	0.055	um
DUMC.1xVn.05	VnDUM (n=2~7) must not interact (1x Vn, 1x Mn, 1x Mn+1, VnDUB (n=2~7), MARKG, MARKS, NODMF, DUMBM, OCCDB, INDMY) layers.			

MTT2 dummy check rules

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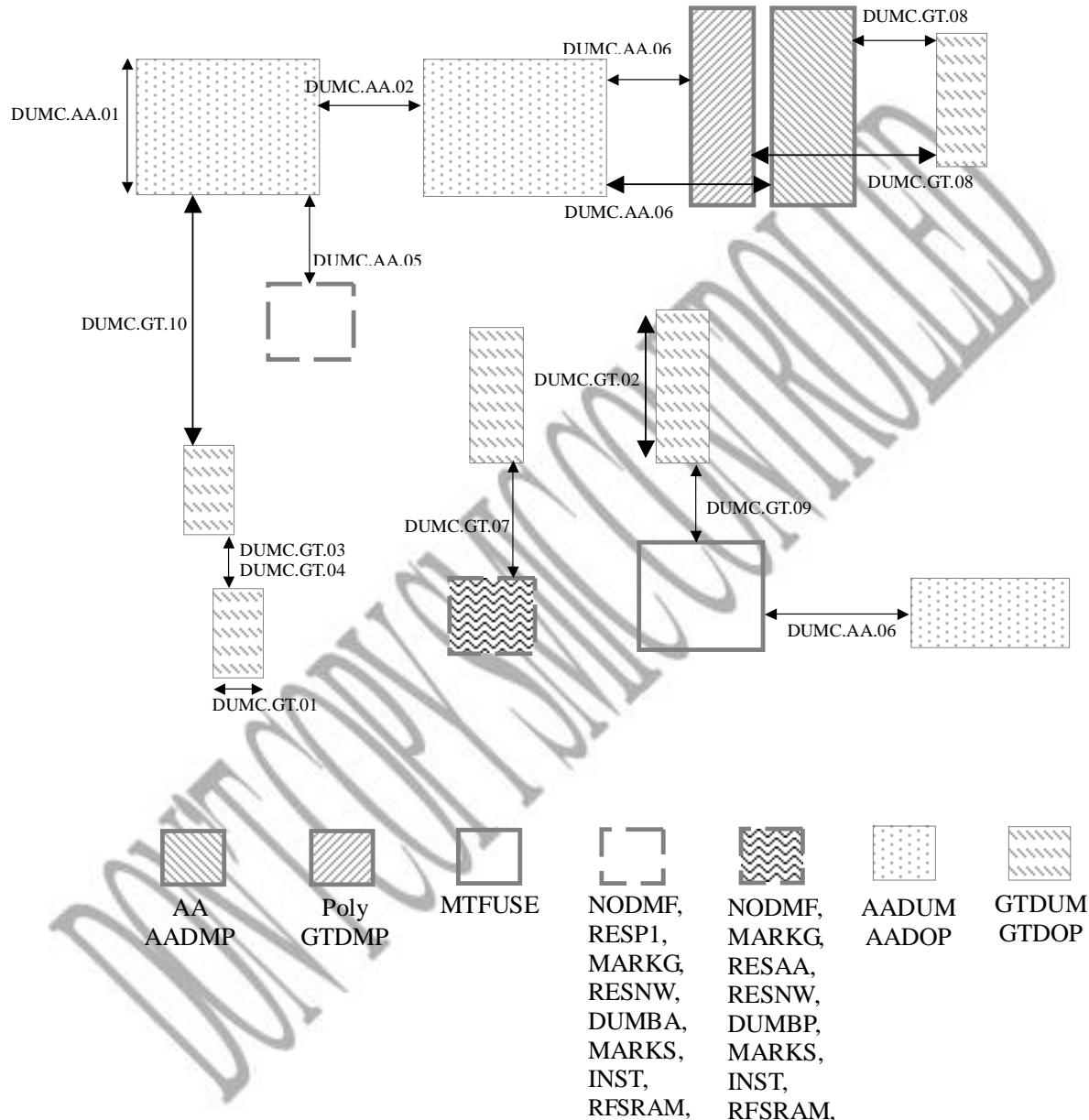
DUMC.MTT2.00	DRC also check the MTT2 dummy and flag the violations on main rules: MTT2.1, MTT2.2a, MTT2.2b, MTT2.6, MTT2.7, MTT2.14			
DUMC.MTT2.01	MTT2DM width.	\geq	3.6	um
DUMC.MTT2.02	Space between MTT2DM and MTT2DM.	\geq	1.78	um
DUMC.MTT2.03	MTT2DM must not interact (MTT2, DUMB, NODMF, MTT2DB, MARKG, MARKS) layers.			
DUMC.MTT2.04	Space between d MTT2DM and (MTT2, DUMB, NODMF, MTT2DB, MARKG, MARKS) layers.	\geq	1.78	um

ALPA dummy check rules

DUMC.ALPA.00	DRC also check the ALPA dummy and flag the violations on main rules: ALPA.1, ALPA.2			
DUMC.ALPA.01	ALDUM width.	\geq	7	um
DUMC.ALPA.02	Space between ALDUM and ALDUM.	\geq	3.6	um
DUMC.ALPA.03	ALDUM must not interact (ALPA, DUMB, NODMF, ALDUB, MARKG, MARKS) layers.			
DUMC.ALPA.04	Space between ALDUM and (ALPA, DUMB, NODMF, ALDUB, MARKG, MARKS,) layers.	\geq	2.85	um

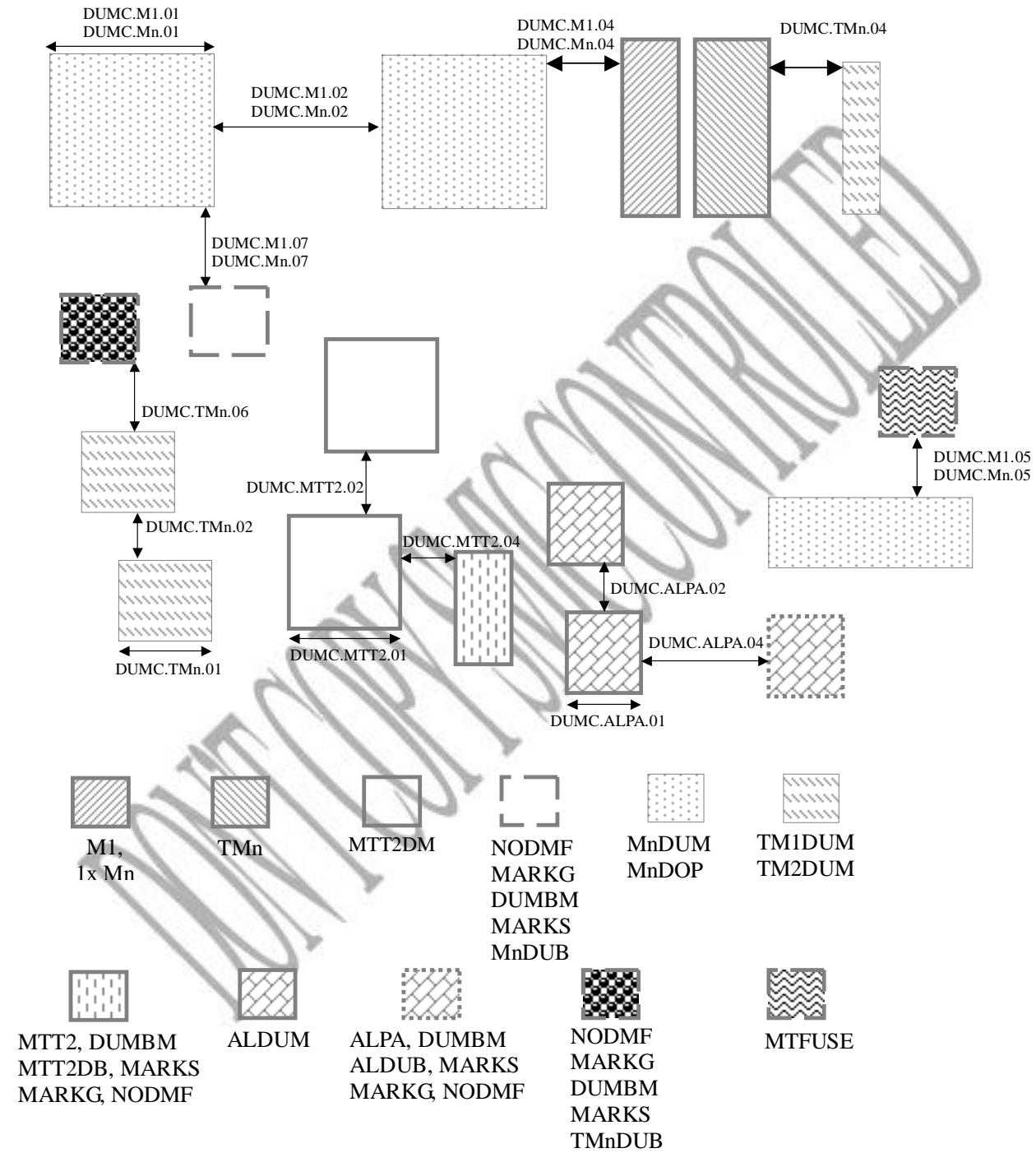
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7.5 DFM (Design for Manufacturability) Rules

7.5.1 Introduction

All the recommendations have been listed in the following DFM rules' section, it is recommended to follow them as much as possible, which can achieve large process window, better device and reliability performance, and higher yield.

DFM rules have been grouped with different priority levels. Higher priority indicates higher risk of manufacturability and yield loss when the rule is not obeyed. Users should follow DFM priority 1 and priority 2 rules strictly, DRC clean of DFM priority 1 and priority 2 rules is must for tape-out, if users intend to waive a violation of a priority 1 and priority 2 rules for any reason, need to review with SMIC before waiver. Priority 3 rules also impact manufacturability and yield, but they are not the gating items for tape-out.

DRC check methodology for DFM rules: there are two switches in DRC deck related with DFM rules. One switch is for DFM priority 1 and priority 2 rules which is turn on by default; another switch is only for priority 3 DFM rules, users can turn on it to check DFM priority 3 rules' DRC results.

7.5.2 DFM Rules

Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
AA.1a ^[R]	Recommended AA width. DRC doesn't check INST and RFSRAM region.	3	Device	≥	0.06	off
AA.1b ^[R]	Recommended AA width.	2	Process	≤	30	on
AA.2 ^[R]	Width of (((AA or AA_DMY) sizing up 0.39um) sizing down 0.39um) NOT (poly or POLY_DMY)) DRC doesn't check BIPOLA and DSTR region.	2	Process	≤	7	on
AA.5 ^[R]	Recommended space between two AAs to prevent AA bridge. DRC doesn't check INST and RFSRAM region.	3	Process	≥	0.075	off
AA.14 ^[R]	(AA or AA_DMY) space which (AA or AA_DMY) space is covered by DUMBA. DRC check maximum STI width in DUMBA.	2	Process	≤	5	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
AA.15 ^[R]	Space between (AA or AA_DMY) DRC check maximum STI width. DRC don't check: chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.	2	Process	\leq	5	on
AA.30 ^[R]	(AA or AA_DMY) density inside of the dummy block area(DUMBA), Density check window size: 20um*20um, step size: 10um DRC need check the design if DUMBA width is >5um and <20um, where density ratio= AA area/DUMBA area.	2	Process	\geq	20%	on
AA.42 ^[R]	Recommended length of horizontal edge between convex corners of T-shape (AA INTERACT poly) This check doesn't check LOGO, INST and RFSRAM region.	3	Device	\geq	0.32	on
NW.3 ^[R]	Space between NWs if at least one NW width<0.28um	2	Process	\geq	0.28	on
PSUB.3 ^[R]	Space of PSUBs if at least one PSUB width<0.28um	2	Process	\geq	0.28	on
LVT_N.3 ^[R]	Space between LVT_Ns with parallel run length >0.24um, when one LVT_N width >0.22um.	2	Process	\geq	0.18	on
LVT_P.3 ^[R]	Space between LVT_Ps with parallel run length >0.24um, when one LVT_P width >0.22um.	2	Process	\geq	0.18	on
HVT_N.3 ^[R]	Space between HVT_Ns with parallel run length >0.24um, when one HVT_N width >0.22um.	2	Process	\geq	0.18	on
HVT_P.3 ^[R]	Space between HVT_Ps with parallel run length >0.24um, when one HVT_P width >0.22um.	2	Process	\geq	0.18	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
ULVT_N.3^[R]	Space between ULVT_Ns with parallel run length >0.24um, when one ULVT_N width >0.22um.	2	Process	≥	0.18	on
ULVT_P.3^[R]	Space between ULVT_Ps with parallel run length >0.24um, when one ULVT_P width >0.22um.	2	Process	≥	0.18	on
UHVT_N.3^[R]	Space between UHVT_Ns with parallel run length >0.24um, when one UHVT_N width >0.22um.	2	Process	≥	0.18	on
UHVT_P.3^[R]	Space between UHVT_Ps with parallel run length >0.24um, when one UHVT_P width >0.22um.	2	Process	≥	0.18	on
GT.10^[R]	Width of 1st POLY_DMY neighboring GATE for I/O NMOS/PMOS. 1st poly (or POLY_DMY) is must when the space between 1st poly (or POLY_DMY) and neighboring GATE <0.51um. This rule doesn't check the neighboring GATE in ESDIO1, ESDIO2, ESDCLP, ESDPOB, CLPDMY region.	3	Process	≥	0.1 um	
GT.16^[R]	Space between (poly or POLY_DMY) in DUMBP region. DRC check maximum (NOT (poly or POLY_DMY)) width in DUMBP. DRC doesn't check OCOVL region.	2	Process	≤	3	on
GT.17^[R]	Space between (poly or POLY_DMY). DRC check the maximum (NOT (poly or POLY_DMY)) width. DRC doesn't check 1. OCOVL, DSTR and BIPOLA region. 2. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	2	Process	≤	3	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
GT.29a ^[R]	Extension of AA outside of (poly INTERACT CT) for core device with channel length $\leq 0.09\mu m$. This rule isn't applicable for PSUB, VARMOS, ESDIO2, ESDCLP, ESDPOB, CLPDMY, EFUSE region.	3	Device	\geq	0.205	off
GT.35 ^[R]	((Poly or POLY_DMY) NOT P2) density. Density check window: Window size: 10um*10um, step size: 5um. For low density , DRC don't check : <ol style="list-style-type: none">1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.2. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer.3. MOMDMY, BIPOLA, RESAA, LOGO, (DSTR AND AA), (INDMY sizing up 2um) region For high density, DRC doesn't check H-R resistor region: ((poly AND RESP2) INTERACT SAB).	3	Process	\geq	15%	off
		3	Process	\leq	55%	off
GT.36 ^[R]	((Poly or POLY_DMY) NOT P2) density. Density check window: Window size: 20um*20um, step size: 10um. For low density , DRC don't check : <ol style="list-style-type: none">1. Chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC.2. Seal ring (MARKS) sizing up 0.4um if seal ring is added by customer. For high density, DRC doesn't check H-R resistor region: ((poly AND RESP2) INTERACT SAB).	3	Process	\geq	15%	off
		3	Process	\leq	55%	off

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
GT.37 ^[R]	((Poly or POLY_DMY) NOT P2)) density inside of the dummy block area(DUMBP).Density check window size: 10um*10um, step size: 5um DRC need check the design if DUMBP width is >3um and <10um, where density ratio= ((poly or POLY_DMY) NOT P2) area/DUMBP area. DRC doesn't check OCOVL region.	2	Process	≥	10%	on
GT.44 ^[R]	Maximum ((poly or POLY_DMY) NOT P2) area. This rule doesn't check the area below: 1) H-R resistor region (((poly or POLY_DMY) AND RESP2) INTERACT SAB), BIPOLA and (GTDMP AND RESAA); 2) All (poly or POLY_DMY) width ≤ 0.2um in check window and density ≤ 50%, density check window is 10um*10um, stepping is 5um.	3	Process	≤	2	off
GTDM.P32 ^[R]	CT is not allowed to land on GTDMP	2	Device			on
P2.22 ^[R]	Recommended (P2 or P2DUM or P2DOP) density in full chip	2	Process	≥	5%	on
SN.3 ^[R]	Space between SNs with parallel run length >0.24um, when one SN width >0.22um.	2	Process	≥	0.18	on
SP.3 ^[R]	Space between SPs with parallel run length >0.24um, when one SP width >0.22um	2	Process	≥	0.18	on
P4.3 ^[R]	Space between P4s with parallel run length >0.24um, when one P4 width >0.22um.	2	Process	≥	0.18	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
P4.7a ^[R]	Recommended enclosure of PMOS GATE along poly length direction in core device region. DRC doesn't check INST and RFSRAM region.	2	Device	\geq	0.065	on
CT.6a ^[R]	CT enclosure by AA for a CT landed on AA when channel length > 0.09um to avoid high resistance.	3	Process	\geq	0.015	off
CT.6b ^[R]	CT enclosure by AA for a CT landed on AA when enclosure by AA on either perpendicular direction \geq 0.005um to avoid high resistance.	3	Process	\geq	0.04	off
CT.7e ^[R]	Recommended enclosure by poly when enclosure by poly on either perpendicular direction \geq 0um, and poly width > 0.09um.	3	Process	\geq	0.03	off
CT.9a ^[R]	Recommended enclosure by M1. DRC doesn't check INST and RFSRAM region.	3	Process	\geq	0.01	off
CT.9b ^[R]	Recommended enclosure by M1 when enclosure by M1 on either perpendicular direction \geq 0.01um and < 0.02um. DRC doesn't check INST and RFSRAM region.	3	Process	\geq	0.035	off
CT.9c ^[R]	Recommended enclosure by M1 in the four sides. DRC doesn't check INST and RFSRAM region.	3	Process	\geq	0.02	off
CT.9d ^[R]	Recommended enclosure by M1 (M1 width \geq 0.08um, M1 and M1 space < 0.06um) This rule doesn't check two CTs (when CTs space < 0.08um)	3	Process	\geq	0.015	off

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
CT.9e ^[R]	Enclosure by M1 (metal width \geq 0.33um and \leq 0.7um) when enclosure by M1 on either perpendicular direction \geq 0.015um. DRC violation is allowed if only one CT meets this rule for the redundant CTs pattern.	2	Process	\geq	0.02	on
CT.10 ^[R]	Recommended inner vertex AA enclosure of CT. This rule doesn't check the N+/P+ pickup regions	3	Process	$>$	0.04	off
CT.16 ^{[NC][R]}	Recommend put more CTs avoid high resistance wherever layout allows.	3	Device			off
M1.4 ^[R]	Recommended M1 width, when 1. Space between M1 and two side-wall M1 is 0.05 um, with parallel run length $>0.16\mu m$; 2. CT/V1 enclosure by this M1: $0.02\mu m \leq E1 \leq 0.03\mu m$; 3. Space between this M1 line end and M1: $0.07\mu m \leq S \leq 0.08\mu m$.	2	Process	\geq	0.06	on
M1.7 ^[R]	Space between (M1 or dummy M1). DRC check maximum width of (NOT (M1 or dummy M1)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LÖGO.	2	Process	\leq	4.5	on
M1.17a ^[R]	Recommended M1 area. DRC doesn't check INST and RFSRAM region.	3	Process	\geq	0.023	off
M1.21 ^[R]	M1 density (including dummy) in DUMBMB and M1DUB region. Density check window size: 125um*125um, step size: 62.5um.	2	Process	\geq	10%	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
	DRC need check the design if DUMBMB/M1DUB width is >5um and<125um, where density ratio= M1 area/(DUMBMB or M1DUB)area.	2	Process	≤	85%	on
1xMn.6^[R]	Space between (1xMn or dummy 1xMn). DRC check maximum width of (NOT (1xMn or dummy 1xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LOGO.	2	Process	≤	4.5	on
1xMn.15a^[R]	Recommended 1xMn area. DRC doesn't check OCOVL, INST and RFSRAM region.	3	Process	≥	0.023	off
1xMn.20^[R]	1xMn density (including dummy) in DUMBMB and MnDUB region. Density check window size: 125um*125um, step size: 62.5um. DRC need check the design if DUMBMB/MnDUB width is >5um and<125um, where density ratio= 1xMn area/(DUMBMB or MnDUB)area.	2	Process	≥	10%	on
1xVn.3^[R]	1x Vn must be fully covered by M1 or 1xMn. Enclosure by 1xMn must follow (1x Vn.3a^[R] and 1x Vn.3b^[R]) or 1x Vn.3d^[R], and 1x Vn.3e^[R], and 1x Vn.3f^[R] as below.	3	Device			off
1xVn.3a^[R]	Enclosure by M1 or 1xMn, where 1xMn is the metal layer directly underneath 1x Vn.	3	Device	≥	0.01	off
1xVn.3b^[R]	Enclosure by M1 or 1xMn when enclosure by 1xMn on either perpendicular direction ≥0.01 and <0.025um um and 1xMn is the metal layer directly underneath 1x Vn.	3	Device	≥	0.05	off

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xVn.3d^[R]	Enclosure by M1 or 1xMn in four sides, and 1xMn is the metal layer directly underneath 1x Vn.	3	Device	\geq	0.025	off
1xVn.3e^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width \geq 0.33um and \leq 0.7um, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.03	on
1xVn.3f^[R]	Enclosure by M1 or 1xMn in the four sides when 1xMn width >0.7 um, 1xMn is the metal layer directly underneath 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.04	on
1xVn.4^[R]	1x Vn must be fully covered by 1xMn+1. 1xMn+1 enclosure 1x Vn must follow (1x Vn.4a ^[R] and 1x Vn.4b ^[R]) or 1x Vn.4d ^[R] , and 1x Vn.4e ^[R] , and 1x Vn.4f ^[R] as below.	3	Device			off
1xVn.4a^[R]	Enclosure by 1xMn+1, where 1xMn+1 is the metal layer directly above 1x Vn.	3	Device	\geq	0.01	off
1xVn.4b^[R]	Enclosure by 1xMn+1 when enclosure by 1xMn+1 on either perpendicular direction \geq 0.01um and $<$ 0.025um and 1xMn+1 is the metal layer directly above 1x Vn.	3	Device	\geq	0.05	off
1xVn.4d^[R]	Enclosure by 1xMn+1 in four sides and 1xMn+1 is the metal layer directly above 1x Vn.	3	Device	\geq	0.025	off

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xVn.4e^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width \geq 0.33um and \leq 0.7um, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.03	on
1xVn.4f^[R]	Enclosure by 1xMn+1 in the four sides when 1xMn+1 width >0.7um, 1xMn+1 is the metal layer directly above 1x Vn. DRC violation is allowed if only one 1xVn or rectangular 1x Vn meets this rule for the redundant 1xVn pattern.	2	Device	\geq	0.04	on
1xVn. 9^[R]	Recommended consecutive stacked 1x Vn layer, which has only one 1x Vn for each 1x Vn layer to avoid high Rc. This rule doesn't check MARKS and DUPMK1 region.	3	Process	\leq	4	off
1xVn. 10^[R]	Recommended space between 1x Vn and 1xVn+1, where 1xVn and 1xVn+1 at different net and parallel run length > 0.02um	3	Device	\geq	0.06	off
1xRVn.3e^[R]	Enclosure by M1 or 1x Mn (1x Mn width \geq 0.33um and \leq 0.7um), when enclosure by 1xMn on either perpendicular direction \geq 0.01um. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.02	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xRVn.3f^[R]	Enclosure by M1 or 1x Mn (1x Mn width $>0.7\text{um}$), when enclosure by 1x Mn on either perpendicular direction $\geq 0.03\text{um}$. 1xMn is the metal layer directly underneath rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.03	on
1xRVn.4e^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width $\geq 0.33\text{um}$ and $\leq 0.7\text{um}$), when enclosure by 1x Mn+1 on either perpendicular direction $\geq 0.015\text{um}$. 1x Mn+1 is the metal layer directly above rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.02	on
1xRVn.4f^[R]	Enclosure by 1x Mn+1 (1x Mn+1 width $>0.7\text{um}$), when enclosure by 1x Mn+1 on either perpendicular direction $\geq 0.03\text{um}$. 1x Mn+1 is the metal layer directly above rectangular 1x Vn. DRC violation is allowed if only one 1xVn or one rectangle 1xVn meets this rule for the redundant rectangle 1xVn pattern.	2	Device	\geq	0.03	on
1xRVn. 12^[R]	Recommended consecutive stacked rectangular 1x Vn layer, which has only one rectangular 1x Vn for each rectangular 1x Vn layer to avoid high R_c. This rule doesn't check MARKS and DUPMK1 region.	3	Process	\leq	4	off

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
1xRVn. 13 ^[R]	Recommended space between rectangular 1x Vn and 1xVn+1, where rectangular 1xVn and 1xVn+1 at different net and parallel run length > 0.02um	3	Device	≥	0.06	off
2xMn.6 ^[R]	Space between (2xMn or dummy 2xMn). DRC check maximum width of (NOT (2xMn or dummy 2xMn)) in chip region. DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um and LOGO.	2	Process	≤	4.5	on
2xMn.13 ^[R]	2xMn density (including dummy) in DUMBMB and 2xMnDUB region. Density check window size: 125um*125um, step size: 62.5um.	2	Process	>	10%	on
	DRC need check the design if DUMBMB/2xMnDUB width is >5um and <125um, where density ratio= 2xMn area/(DUMBMB or 2xMnDUB)area.	2	Process	≥	85%	on
8xTMn .2d ^[R]	Space between (8x TMn or dummy 8x TMn) DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	2	Process	≤	12	on
8xTMn .5 ^[R]	8xTMn density (including dummy) in DUMBMB and TMnDUB. Density check window size: 125um*125um, step size: 62.5um (exclude DUPMK1 region). DRC need check the design if DUMBMB/TMnDUB width is >5um and <125um, where density ratio= 8xTMn area/(DUMBMB or TMnDUB)area.	2	Process	≥	10%	on
		2	Process	≤	85%	on
8xTMn .6 ^[R]	TMn density (including dummy) in full chip	2	Process	≥	20%	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
10xTMn .2d^[R]	Space between (10xTMn or dummy 10xTMn) DRC doesn't check chip corner triangle region (NODMF) sizing up 0.4um if seal ring is added by SMIC	2	Process	\leq	12	on
10xTMn .6^[R]	10xTMn density (including dummy) in DUMB M and TMnDUB. Density check window size: 125um*125um, step size: 62.5um (exclude DUPMK1 region). DRC need check the design if DUMB M/TMnDUB width is >5um and <125um, where density ratio= 10xTMn area/(DUMB M or TMnDUB)area.	2	Process	\geq	10%	on
		2	Process	\leq	85%	on
ALPA.3^[R]	ALPA density (including dummy) with 100um*100um window, with exemption of interacting inductor.	2	Process	\geq	10%	on
ALPA.4^[R]	Space between ALRDL and L mark (or LOGO) window.	2	Process	\geq	10	on
MD.4^[R]	MD must be within BORDER (chip edge)	2	Process	\geq	8	on
RESAA.5b^[R]	The length of GTDMP projection along AA silicide resistor width direction must be same as the length of ((AA AND RESAA) INTERACT DIFRES)	2	Process			on
RESAA.9^[R]	It's strongly recommended space between CT and SAB for non-silicidized AA resistor for spice model accuracy	2	Process	$=$	0.12	on
RESNWAA.15^[R]	Recommended space between SAB and CT	3	Device	$=$	0.3	off
RESNWST.8^[R]	It's strongly recommended AA enclosure of CT (AA INTERACT RESNW)	3	Device	$=$	0.3	off

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
HR.6^{[NC][R]}	It's recommended to manually draw AADMP in H-R resistor array region when H-R resistor array can't meet AA density rule(AA.26) and max (AA or AA_DMY) space rule (AA. 14, AA.15). Pls refer HR.7 ^[R] , HR.8 ^[R] , HR.16 ^[R] , HR.17 ^[R] for AADMP drawing in HR resistor region.	2	Device			
HR.7^[R]	Width of AADMP within RESP2	2	Device	\geq	0.05	on
HR.8^[R]	The length of AADMP projection along H-R resistor width direction must be same as the length of ((poly AND RESP2) INTERACT SAB) for H-R resistor array.	2	Device			on
HR.12^[R]	Space between H-R resistor and SN	2	Device	\geq	0.1	on
HR.14^[R]	Space between CT and SAB in RESP2 region	2	Device	$=$	0.12	on
HR.16^[R]	Space between AADMP and neighboring H-R resistor within RESP2 along H-R resistor width direction	2	Device	\geq	0.055	on
HR.17^[R]	Space between AADMP and GTDMP within RESP2 along H-R resistor width direction (AADMP and GTDMP overlap is not allowed.).	2	Device	\geq	0.055	on
HR.25^[R]	The length of (RESP1 AND ((Poly INTERACT CT) AND SAB)) should be same with (RESP2 AND ((Poly INTERACT CT) AND SAB))	3	Device			off
MR.5^{[R][NC]}	AADMP is must to be drawn beside each in metal gate resistor array region. Metal gate resistor array definition: metal gate resistor (poly AND RESP2) number >1 along resistor width direction within one RESP2	2	Device			
MR.6^[R]	Width of AADMP within RESP2	2	Device	\geq	0.05	on

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Rule No	Rule description	Prior ity	Concerned Area	op.	DFM rule (um)	DRC switch default
MR.7 ^[R]	The length of AADMP projection along metal gate resistor width direction must be same as the length of ((poly AND RESP2) INTERACT RESP1) for metal resistor array.	2	Device			on
MR.11 ^[R]	Space between MG resistor and (SN or SP)	2	Device	\geq	0.1	on
MR.13 ^[R]	Space between AADMP and neighboring metal gate resistor within RESP2 along metal gate resistor width direction	2	Device	\geq	0.055	on
MR.14 ^[R]	Space between AADMP and GTDMP within RESP2 along metal gate resistor width direction (AADMP and GTDMP overlap is not allowed.).	2	Device	\geq	0.055	on
LDNMK1.15 ^[R]	Recommended dummy metal not to insert between guard rings or in the breach of guard ring. Please use DUMB to avoid dummy metal insertion.					
ESD1.5a ^[R]	The recommended CT enclosure by ESD1.	2	Device	\geq	0.4	on

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7.6 Current Density Guidelines

7.6.1 Metal line/CT/Vn/PA Current Density

Rule Number	Description	Operation	Design Value	Unit
Jmax is maximum DC current allowed per um of metal line width or per via/contact.				
Metal Line (metal line width: Wx0.9)				
CDR.1	Jmax of M1 line at 110°C	≤	1	mA/um
CDR.2	Jmax of 1xMn line at 110°C	≤	1	mA/um
CDR.3	Jmax of 2xMn line at 110°C	≤	1.9	mA/um
CDR.4	Jmax of 8xMn line at 110°C	≤	8.8	mA/um
CDR.5	Jmax of 10xMn line at 110°C	≤	12	mA/um
CDR.6	Jmax of MTT2 line at 110°C	≤	32	mA/um
CDR.7	Jmax of ALPA(14K) line at 110°C	≤	2.8	mA/um
CDR.8	Jmax of ALPA(28K) line at 110°C	≤	5.6	mA/um
CT and Via				
CDR.9	Jmax of CT at 110°C	≤	0.083	mA/CT
CDR.10	Jmax of 1xVn at 110°C	≤	0.04	mA/via
CDR.11	Jmax of 2xVn at 110°C	≤	0.16	mA/via
CDR.12	Jmax of 8xVn at 110°C, for the 8xVn landing on 1xMn	≤	1	mA/via
CDR.13	Jmax of 8xVn at 110°C, for the 8xVn landing on 2xMn	≤	1.9	mA/via
CDR.14	Jmax of 8xVn at 110°C, for the 8xVn landing on 8xMn	≤	3	mA/via
CDR.15	Jmax of 10xVn at 110°C, for the 10xVn landing on 1xMn	≤	1.2	mA/via
CDR.16	Jmax of 10xVn at 110°C, for the 10xVn landing on 2xMn	≤	2.7	mA/via
CDR.17	Jmax of 10xVn at 110°C, for the 10xVn landing on 8xMn	≤	5.4	mA/via
CDR.18	Jmax of UTV(LT) at 110°C, for the UTV(LT) landing on 1xMn	≤	1	mA/via

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Rule Number	Description	Operation	Design Value	Unit
CDR.19	Jmax of UTV(LT) at 110°C, for the UTV(LT) landing on 2xMn	≤	1.9	mA/via
CDR.20	Jmax of UTV(LT) at 110°C, for the UTV(LT) landing on 8xMn	≤	3	mA/via
CDR.21	Jmax of PA(size=3um) line at 110°C	≤	7	mA/PA
CDR.22	Jmax of PA(size=2um) line at 110°C	≤	5.4	mA/PA

Note:

1. Suggest use as much as CT/Via numbers in layout design for reliability margin agreement.
2. Minimal required metal width and CT/Via numbers are determined by allowed design current.
3. Preferentially use maximal CT/Via design numbers for perpendicular current

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7.6.2 Metal line Irms definition

$$I_{rms} = \sqrt{\frac{1}{t_w} \int_0^{t_w} i^2(t) dt}$$

Tw=Irms check period. Typically, current period.

i(t)= current

W(in um): the width of the metal line

ΔT (°C): the temperature rise due to Joule heating

Conduction Layer	Operation	Irms	Unit
M1	≤	SQRT[ΔT * (11.06 * (w*0.9)^2 + 8.44 * (w*0.9))]	mA
M2	≤	SQRT[ΔT * (5.11 * (w*0.9)^2 + 7.73 * (w*0.9))]	mA
M3	≤	SQRT[ΔT * (3.55 * (w*0.9)^2 + 4.47 * (w*0.9))]	mA
M4	≤	SQRT[ΔT * (3.52 * (w*0.9)^2 + 6.17 * (w*0.9))]	mA
M5	≤	SQRT[ΔT * (3.15 * (w*0.9)^2 + 4.91 * (w*0.9))]	mA
M6	≤	SQRT[ΔT * (3.03 * (w*0.9)^2 + 5.22 * (w*0.9))]	mA
M7	≤	SQRT[ΔT * (2.78 * (w*0.9)^2 + 4.14 * (w*0.9))]	mA
M8	≤	SQRT[ΔT * (6.67 * (w*0.9)^2 + 3.3 * (w*0.9))]	mA
8xTM	≤	SQRT[ΔT * (9.81 * (w*0.9)^2 + 51.04 * (w*0.9))]	mA
10xTM	≤	SQRT[ΔT * (11.96 * (w*0.9)^2 + 62.84 * (w*0.9))]	mA
MTT2	≤	SQRT[ΔT * (62.83 * (w*0.9)^2 + 267.4 * (w*0.9))]	mA
ALPA(14K)	≤	SQRT[ΔT * (12.86 * (w*0.9)^2 + 43.03 * (w*0.9))]	mA
ALPA(28K)	≤	SQRT[ΔT * (24.19 * (w*0.9)^2 + 116.38 * (w*0.9))]	mA

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7.6.3 Temperature coefficient

7.6.3.1 Cu Temperature coefficient

Temperature C	100	105	110	115	120	125
Factor	2.149	1.459	1	0.692	0.484	0.341

7.6.3.2 Contact(CT) temperature coefficient

CT temperature coefficient is the same as Cu.

7.6.3.3 Aluminum temperature coefficient

Temperature C	70	85	100	110	125
Factor	3.443	2.097	1.329	1	0.6707

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8. Attachment:

[32RULE_SMICsealring_20140430.gds.](#)

[IDOVSMIC_N.gds](#)

[IDCD_SMIC_FEOL_H0.gds](#)

[IDCD_SMIC_FEOL_V0.gds](#)

[28nm_OCCD_SMIC_BEOL.gds](#)

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