



Semiconductor Manufacturing International Corporation

Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev: 4	Tech Dev Rev: 1.10	Page No.: 1/299
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Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0T	0.0	2009-12-17	Feng Ji	Initiate
1T	0.0	2011-09-13	Meng Feng Tsai	Modify 40nm Logic Design Rule as below according to 40LL process review results and customer feedback: (Simplify change description(dsc), detailed refer to DR last section) 1.Modify Doc Title; “note” before title page; purpose dsc; Grid Size dsc; And add related references in item5; 2.Modify 7.3 all 3. Modify AA.1-AA.11 dsc or value, AA fig; Add AA.12-AA.15. Delete AA note 4.Modify RESAA.2, 2R,3,3R,7 dsc or value, RESAA fig; Add RESAA.11-13 5.Modify AA.C.1-5 dsc or value; Modify AA density rule note 1-3 dsc 6.Modify DNW.5-6 dsc, table head, fig 7. Modify NW.1-4. dsc or value, fig. Add NW.9.D NW.5-6, note 1-3 8.Add NW resister rule sect 9. Modify PSUB.1-5b dsc or value. Add PSUB.3d,note#8. Delete PSUB.8 10.Delete SDOP, NC, PC sect 11. Modify TG title dsc. Modify TG.1-6 dsc and value. Add TG.9-15. Modify TG fig 12. Modify DG title dsc. Modify DG.1-6 dsc and value. Add DG.9-14. Modify DG fig 13.Add BORDER sect 14. Rename POLY rule no. head to GT. Modify GT.1-23, GT fig. Add GT.24-25a. Delete Note 1. Add Note 3. 15. Modify RESP1.1-3a, 6-7 dsc or value, RESP1 fig. Delete RESP1.10. Add RESP1.11-14 16.Add LVT, HVT sects post RESP1 17. Delete generated layer sections: NLL, LVN, VTNH, NLH, NLHT, PLL, LVP, VTPH, PLH, PLHT 18. Modify SP.1-16, 20 dsc or value, fig. Delete SP.11,19. SP.3,7 divide to a,b parts 19. Modify SN.1-16, 20 dsc or value, fig. Delete SN.11, 19. SN.3, 7 divide to a,b parts. Add SN.22. 20. Modify SAB.1-8, 10, 11 dsc or value. Delete SAB.9. Add SAB.15 21. Modify CT.1-11 dsc or value. Delete CT.2R. Add CT.2a, 3a, 6a, 6b, 7a, 7b, 14-18. Delete note on CT array.

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				<p>22. Modify BEOL rule summary table via and metal no. 23. Modify M1.4, 6-8 dsc or value. Delete 7c, 7d; Modify fig 24. Modify V1.3, 4,6, 6d, 7, 7a, 14 dsc or value. Add V1.7d. Delete V1.11-15. 25. Modify Mn.4,6,6a,6b,6c,7,7a,7d,7e dsc or value 26. Modify Vn.3,4,6a,6d,7,7a,7d dsc or value.Delete Vn.11-15 27. Add TM1.11 value. 28. Modify MD.4, 5,6 dsc. Modify Fig, Delete MD.7,9, Add MD.10,11 29. Modify ALPA all sect: delete original all rules, insert ALPA.1-12 and note 1-4. Delete ALRDL rules 30. Modify PA.2, 10 dsc or value. Modify PA, ALPA fig 31. Modify EXCLU rule 32.Add 7.4.38 Dummy check rule sect 33.Add 7.4.39 Current density rules 34.Add 7.4.40 corner rules 35. Add 7.5 DFM rule section 36. Add item 9: detail change note 37. Add 7.1.1 section on dummy pattern data type 38. Add 7.4.41 ESD rules 39.Delete TV1.8-12, TV2.8-12, PA.5-9. 40.Add Ref doc in Reference section. 50.Modify TM2.12,TM1.13 value, TM2.10 description 51.Modify TV1.2,TV1.3,TV2.2,TV2.3 rule values. Modify TV1.3, TV2.3 description. Add TV1.13.Delete TV1 note.</p>
2R	0.0	2011-12-28	Amy Wong	<p>Modify/Delete/Add 40nm Logic Design Rules as below according to 40LL process review results and customer feedback:</p> <ol style="list-style-type: none">1. Modify Titles, remove “1P10M”. Follow DR meeting requirement.2. Modify Purpose section description3. Modify Reference section: remove SRAM DR, Add dummy insertion DR4. Modify 7.1.1 description5. Modify 7.1.2 description6. Add TCD(91;4), ICOVL(91;5) layers definition in the table 7.3.1-2 40LL layer table.7. Revise Table 7.3.1-2 and 7.3.3-2 1) seal ring marker layer of MARKG → MARKS; 2) GDS number: 189;0→189;1511; 3) Delete guard ring in the layer description8. Correct table Table 7.3.2 1.8V nfet typo9. Add section 7.3.8 design check flow before tape out

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				<ul style="list-style-type: none">10. Table 7.3.6.13 add def of [NC]11. Delete RESAA.8, RESAA.11. Add one note12. Modify rule values of RESAA.12, RESAA.1313. Modify GT.3 description14. Delete GT.1315. Modify GT.2b description16. Modify TG.3, DG.3 description17. Modify SAB.11 description18. Delete LVT.3, HVT.3,LVT.14, HVT.1419. Modify SP.10. Correct typo20. Delete SN.20, SP.2021. Modify CT.1,CT.6,CT.6a,CT.6b,CT.7,CT.7a,CT.7b,CT.10 descriptions22. Modify description of M1.6, M1.6a, M1.6b, M1.6c, Mn.6, Mn.6a, Mn.6b, Mn.6c23. Modify M1.7, M1.7a, M1.7b description, rule value24. Add M1.7c25. Modify V1.3, Vn.3 description26. Delete V1.4, Vn.427. Modify description of V1.6, V1.6d, Vn.6, Vn.6d, V1.7, V1.7d, Vn.7,Vn.7d28. Modify TM1.13, TM2.12 descriptions29. Modify PA.1, PA.3, PA.4,PA.10 description, rule value, schematic30. Modify MD.11 description31. Modify description of DUMC.2,DUMC.1232. Revise DUMC.2, DUMC.6, DUMC.12, DUMC.16, DUMC.18, DUMC.20, DUMC.22, DUMC.26, DUMC.27, DUMC.28: seal ring marker layer: MARKG → MARKS33. Modify rule value of DUMC.2334. Delete DUMCN.535. Modify DUMCN.13 rule value36. Add DFM.2837. Modify DFM.26 description38. 7.4.40 chip corner rule note.1 add “MTT2”39. Add 7.4.42 HRP section40. Add 7.4.43 MTT section for UTM41. Add 7.6 SRAM section42. Add section 9.2 for v.2R detail change item description

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3R	1.0	2012-09-28	Charles_Yin	<p>A. Modify item 5 Reference: del. TD-LO40-DR-2004/5/8, reason: content merged into the file, refer to 7.4.46/47, 7.7.5/6.</p> <p>B. 1)Follow design rule general template to re-organize original 7.2 &7.3 to 7.1 and update the content. 2)Add 7.1.3~5 3)7.1.9: add table 2~5 4)7.1.11: Add definition of enclosure, extension, (not) outside</p> <p>C. Modify 7.4 due to process capability improve and customer feedback:</p> <ol style="list-style-type: none">1. Modify AA.4b/4c, AA.11/12, add AA.4d, AA.16~192. Rename AA.5~8 to NW.13~163. Modify AA.14 value: 75% ->80%, add AA.14a.4. AA.C.5: restrict gate width<0.06.5. Modify RESAA.2 rule value: 0.2->0.4, add RESAA.146. Delete DNW.5/6 for rule cancel, add DNW.77. Add 7.4.1.3, 7.4.8.2: AA/Poly silicide resistor rule8. Add NW.10~129. Revise NW resistor to under STI/AA.10. Add PSUB.3e, delete PSUB note#4; rename note#1-3,5 to PSUB.10~1311. Modify TG.3/5 value: 0.176->0.2, TG.4/6: 0.35->0.25. So does DG.12. Modify BORDER.1, add Border.4.13. Modify GT.1e value: 0.45 ->0.44, add GT.1h.14. GT.2b: change to [R] rule, relax value: 0.07->0.06.15. GT.3: delete “on STI” in desc.16. Add GT.3c/8a/9/10, GT.6a^[R], GT.20c/20d/27/28, delete GT.16.17. Modify GT.5~8, 22 to reduce unnecessary DRC alarm.18. Relax GT.20, GT.20b value: 35%->40%.19. Modify RESP1.2 value: 0.15->0.4,add RESP1.1520. Modify LVT.6 value: 0.16->0.18; LVT.9/10: 0.1->0.19. So does HVT.21. SN.7b: add “out of SRAM area”.22. Add SP.7c/8c, delete SP.8a/8b for rule optimize. So does SN.23. Add CT.1a; Modify CT.2a value:0.08->0.11.24. Delete “at least one CT(V1,Vn)” in CT.6/CT.7/M1.7/V1.6/7, Vn.6/7 for large process window.25. Modify CT.6a/6b, add CT.6c.

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				<p>26. Modify CT.7b/10, M1.7b/7c, add CT.19^[R].</p> <p>27. Modify M1.5, Mn.5 value: 0.078->0.2; Update M1.6a/6b/6c. So does Mn.</p> <p>28. Add M1.7e.</p> <p>29. Modify M1.8, Mn.7 value: 20%->10%, M1.8a, Mn.7a:80%->85%</p> <p>30. Relax M1.8b, Mn.7b, TM1.12, TM2.11 value:40%->50%.</p> <p>31. Modify M1.9, Mn.8, Mn.9 value: 0.3->0.17, M1.10: 0.15->0.17</p> <p>32. Add M1.11a/11b/13/14, Mn.10a/10b/11/12 to check metal line end space.</p> <p>33. Add M1.8d, Mn.7f, TM1.10a, TM2.10a, MTT2.7a/7b to check metal density.</p> <p>34. V1.3, TV1.3, TV2.3: add “equal to 3”, and modify V1.3 rule desc.</p> <p>35. Modify V1.5 value: 0.09->0.10, add V1.5a.</p> <p>36. Modify V1.6b/7b, V1.6c/7c</p> <p>37. Delete V1.6d/7d, add V1.16/17. So does Vn. Modify TV1.13, TV2.13/14 for redundant via rules.</p> <p>38. Relax Mn.7d/7e value:56%->70%.</p> <p>39. Relax TM1.5/7, del. TM1.6 due to process improvement</p> <p>40. Modify TM1.8 value: 0.42->0.56; Relax TM1.10 value: [30%, 80%]->[20%, 85%]. So does TM2.</p> <p>41. Relax TM1.12, TM2.11 value: 40%->50%.</p> <p>42. Modify TM1.13, TM2.12 value: 30->12.</p> <p>43. Relax ALPA.1 value: 4->2.</p> <p>44. Relax ALPA.9 value: 25%->10%, ALPA.10: 55%->70%.</p> <p>45. Relax PA.3 value: 1->0.5.</p> <p>46. Modify MD.4/6 to [R] rule, relax MD.1& MD.11</p> <p>47. Delete 7.4.37, forbid using EXCLU.</p> <p>48. 7.4.38: Add dummy insertion table, update dummy checking rules.</p> <p>49. Add CDR.3a/11/12 & Irms section.</p> <p>50. Add CORN.2.</p> <p>51. Add 7.4.44 Poly Efuse rule.</p> <p>52. Add 7.4.45 ULVT rule.</p> <p>D. Modify 7.5</p> <p>1. Change DFM.1/2 des. &Pri. to 2, add DFM.1a/2a</p> <p>2. Modify DFM.3/5/9 to reduce DRC alarm.</p> <p>3. Modify DFM.13/20/21/24/25 to align main rules.</p> <p>4. Delete DFM.11/27, add DFM.29.</p>

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				<p>E. Modify 7.6 follow current actual need and update 7.6.5, add SRAM dimension& marker layer check rules.</p> <p>F. Add 7.7 design guideline: mask retool check, OCCD/OCOVL, redundant via, BEOL dummy metal&Via insertion, ESD/latch up prevention, LDMOS, BUMP pad, DUP pad, BJT, Inductor, MOM.</p> <p>G. 8. Attachment: add seal ring, OCCD/OCOVL GDS sample.</p>



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4	1.10	2015-08-28	Kelpy Pan	<ol style="list-style-type: none">1. 7.4.1: Loose AA.4d/AA.13/AA.14/AA.14a/AA.19. Add AA.4e[R]/AA.13a[R]/AA.20~AA.23[R]. Add [R] for AA.10/AA.12/AA.15. Add AA.20~21 sketch map.2. 7.4.1.2 AA.C.5 downgrade to recommended rule.3. 7.4.2: Loose DNW.7. Add DNW.2a/DNW.4a/DNW.8~9. Update sketch map.4. 7.4.4: Optimize PSUB.5~9, PSUB.12. Delete PSUB.13. Add PSUB.14~16. Update PSUB note and sketch map.5. 7.4.3: Loose NW.3/NW.7. Add [R] for NW.11~12. Add NW.1a/NW.17[R] and sketch map. Optimize NW.12.6. 7.4.5/7.4.6: Loose TG.1~6/TG.11, DG.3~6/DG.11. Add [R] for TG.11/ DG.11. Add TG.16~20. Update sketch map.7. Delete 7.4.7, 7.4.11~7.4.20 (purposely blank). Re-arrange the following Sequence No., as well as the related cited No.8. 7.4.35: Loose ULVT.3~6.9. 7.4.7: Loose GT.3c/GT.20/GT.20b. Add GT.3d/GT.3e/GT.17a[R]/GT.18a[R]/GT.29~GT.35[R]/GT.6b[R]/GT.24b[R]/GT.24c[R]/GT.25b[R]/GT.25c[R]/GT.1a[R]/GT.5a[R].Delete GT.7~8/GT.20c/GT.20d/GT.23. Optimize GT.1a~GT.1h/GT.5/GT.6a/GT.9/GT.10/GT.21/GT.28. Update sketch map.10. 7.4.11: Loose SP.5/SP.9/SP.14/SP.20a. Delete SP.13/SP.21/SP.21a. Optimize SP.6/SP.7/SP.7a/SP.7b/SP.7c/SP.10. Update sketch map.11. 7.4.12: Loose SN.5/ SN.6/SN.7a/SN.7b/SN.9/SN.10/ SN.14/SN.20a. Delete SN.13/SN.21/SN.21a/SN.22. Update sketch map.12. 7.4.8/7.4.9: Optimize LVT.1/ LVT.4/LVT.4a/LVT.5/LVT.5a /LVT.13/HVT.1/HVT.4/HVT.4a/HVT.5/HVT.5a/HVT.13.13. 7.4.13: Optimize SAB.4~6/SAB.11. Loose SAB.4/SAB.6~8/SAB.11. Add [NC] for SAB.13~14.Delete SAB.15. Add SAB.16.14. 7.4.1.1/7.4.7.1: Loose RESP1.5~6/RESP1.11, RESAA.5~6.15. 7.4.14: Optimize CT.1a/ CT.3/CT.3a /CT.5~10/CT.13.Delete CT.9/CT.11/CT.19. Add CT.20/CT.21/CT.3[R]~CT.5[R]. Update sketch map.16. 7.4.16: Add M1.7a[R]/M1.1[R]/M1.3[R]/M1.6[R]/M1.15~16. Optimize M1.3/ M1.8/M1.8a. Delete M1.11a/M1.11b.
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			<p>Update sketch map.</p> <p>17. 7.4.18: Add Mn.1[R]/Mn.3[R]/Mn.6[R]/Mn.13[R]~Mn.16. Optimize Mn.2/Mn.7/Mn.7a. Delete Mn.10a/Mn.10b. Add [R] for Mn.7d/Mn.7e/Mn.12. Update sketch map.</p> <p>18. 7.4.17: Optimize V1.3/V1.6/7/8/9/V1.17. Add V1.17a~V1.22/ V1.5[R]. Update sketch map.</p> <p>19. 7.4.19: Optimize Vn.3/Vn.6~7/Vn.9/Vn.16~17. Add Vn.17a~Vn.21/Vn.24/Vn.5[R]/Vn.22[R]/Vn.23[R].</p> <p>20. 7.4.20: Optimize TV1.4~5. Delete TV1.6~7. Add TV1.15~ 19. Update sketch map.</p> <p>21. 7.4.22: Optimize TV2.4~5. Delete TV2.6~7. Add TV2.15~ 19. Update sketch map.</p> <p>22. 7.4.21/7.4.23: Optimize TM1.9~10/TM1.12/TM2.9~10/TM2.12.</p> <p>23. 7.4.25: Add PA.11~12.</p> <p>24. 7.4.24: Delete ALPA.5/ALPA.7/ALPA.11due to no concern. Add ALPA.13. Update sketch map.</p> <p>25. 7.4.33: Delete MTT2.4. Add MTT2.6a/MMT2.13.Modify MTT2.2/MMT2.6~7/MMT2.7b/MMT2.11. Add [R] for MTT2.2a/MMT2.5/MMT2.7b/MMT2.9. Update sketch map.</p> <p>26. 7.5: Update DFM section design rule.</p> <p>27. 7.7.5.2/7.7.5.3: Optimized description and rule.</p> <p>28. 7.7.6: Update whole section design rule.</p> <p>29. Move 7.4.7 into 7.4.27. Optimize BORDER.1/BORDER.4. Add BD.5~BD.8 and note3.</p> <p>30. Move 7.1.7 content into 7.1.6, and update the following sequence No., as well as the cited No.</p> <p>31. Update 7.1.6/7.1.6.4/7.1.8 table.</p> <p>32. Move the Figure 7.1.9.13-1 and Figure 7.1.9.13-2 to 7.1.9</p> <p>33. Modify attachment 8.3 OCOVL sample GDS to optimize OCOVL structure.</p> <p>34. 7.4.29.2: Add bracket for "AC current density Irms formula".</p> <p>35. Update design rule title and 7.3/7.1.3, and correct the flowchart template</p> <p>36. Delete 7.4.28.2 and merge into 7.4.28.1 dummy pattern check rules.</p> <p>37. Update 7.7.12 DUP (Device Under Pad) Pad Guidelines. Add 7.7.12.1/7.7.12.2.</p> <p>38. 7.7.9/7.7.10: Add IND.R.6~10. Add [G] for all the rule numbers.</p> <p>39. 7.1.5: Update DRC checking guideline.</p> <p>40. Update 5 Reference content.</p>	
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				<p>41. Optimize 7.1.9: GATE, real GATE, N+AA, P+AA, N+ PICKUP AA, P+ PICKUP AA, N+ butted AA, P+ butted AA/7.4.34.Poly E-Fuse Layout guideline.</p> <p>42. Add 7.1.10.13~7.1.10.17 for CUT, NOT INTERACT, COVER, INSIDE, ,and NOT INSIDE definition , 7.1.11 DRC connectivity definition, 7.7.12 DUP PAD Guideline, 7.4.31 Conventional Rule.</p> <p>43. Update 7.4.3:RESNWAA.7/7.4.1.1:RESAA.7/7.4.1.3:DIFRES.7/7.4.7.2:PLRES.7/ PLRES.8/ 7.4.7.1:RESP1.7.</p> <p>44. 7.6.5.1/7.6.5.4: Optimize SRDOP.105/SRGT.5/SRGT.10.</p> <p>45. 7.7.5.1: Optimize ESD.5.Add [NC] for ESD.8.</p> <p>46. 7.6.6: Update all the rules “Gate” to “Real Gate”.</p> <p>47. 7.7.7: Update LD.10[G]. Add LD.11[G].</p> <p>48. 7.4.35: Delete ULVT.3/ULVT.5 due to no concern. Modify ULVT.4/ULVT.6 rule value.</p> <p>49. 7.4.36: Optimize seal ring design rule.</p> <p>50. 7.7.3: Update description and 7.7.13 add Logo Design Guideline.</p> <p>51. 7.4.29: update Current Density Rule.</p> <p>52. Add CAD layers MOMCOL,MOMROW, MOMMK1~MOMMK8</p> <p>53. Update 7.7.11 MOM descriptions, add MOMMKn table, and add rules MOM.4[G] [NC] , MOM.5[G] , MOM.6[G]</p>

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Note: The value in the design rules comes from 45nm design rules, and after customer tape out, SMIC will do 10% shrink.



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INTERNATIONAL CORPORATION**

**40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic
Design Rule**

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1. Title

40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule

2. Purpose

Patterns Design Guideline for 40nm Logic Process.

3. Scope

All SMIC Fabs

4. Nomenclature

NA

5. Reference

Item	Reference documents No	Reference documents title	Reference documents version	Reference part
Dummy Insertion Rule	TD-LO40-DR-2009	40nm Logic Salicide 0.9/1.0/1.1/1.2/1.8/2.5V Low leakage and Generic AA/Poly/Metal/Via layers Dummy Insertion Rule	3R	All

6. Responsibility

Technology Development Center

7. Subject Content**7.1 User Guide****7.1.1 Dummy pattern data type requirements**

The dummy pattern related layers are AA, GT, Mn (n=1-8), Vn(n=1-7), TMn(n=1-2), ALPA, MTT2

a. The SMIC dummy insertion script inserted dummy should be assigned to data type 1 and data type 7. Except for ALPA, the dummy pattern to be put to ALDUM (83;11).

b. Designers are required to put their purposely added dummy into data type 0 as the main circuit. These dummies should follow design rules as the main circuit.

7.1.2 Grid size

Minimum layout grid size is 0.001 μm.



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7.1.3 Layout requirement

Designers should follow design requirement guidelines in this section in order to reduce the OPC loading and then enhance the OPC efficiency.

Guidelines number	Description
DGR.1 ^[NC]	All the geometry design must be an integer multiple of 0.001 um.
DGR.2 ^[NC]	Design geometry shape must be polygons.
DGR.3	Only shapes of geometry that are orthogonal or 45-degree angle are allowed.
DGR.4 ^{[R][NC]}	Recommended to design simple rectangular shape geometry as possible, avoid L, U, H, or O shapes.
DGR.5 ^[NC]	All line-end are must be rectangular.
DGR.6 ^[NC]	Self-intersecting shapes are not allowed.
DGR.7 ^[NC]	All the text or labels in the chip must be covered by the marker layer LOGO (26;0).
DGR.8 ^[NC]	Make sure the designs are DRC clean.
DGR.9 ^[NC]	Recommended use greater or equal half of the minimum width of each layer to avoid small jogs of geometry.
DGR.10 ^[NC]	The layout of designs should have the well-organized hierarchical structures.
DGR.11 ^[NC]	The layout of auto dummy insertion designs should be put in a separate hierarchy from the main designs, and try to avoid the flattened dummy insertion designs.



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7.1.4 Non-DRC checking guideline

1. No DRC for the design rules with the superscript of [NC].
2. No DRC for Notes which are below design rules tables.

7.1.5 DRC checking guideline

1. The rules with the superscript of [R] are recommended rules which require performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow recommended rules which purpose is to ensure better performance for process. Customers can waive violations based on their own judgment, and please consult with integration engineers if customers feel the need.

2. The rules with the superscript of [G] are layout guidelines which require performing a DRC runset, but DRC gating is not needed for them. It's strongly recommended customers to follow layout guidelines which are to ensure better performance for process and device. SMIC spice model and PDK must strictly follow SMIC design rule guidelines. And SMIC don't provide spice model and PDK if customers don't follow the SMIC layout guidelines. Customers can consult with SMIC integration engineers if necessary.

3. The design rules in this document are not applicable for seal ring area (marked with MARKS layer). For seal ring constrains and dimensions, please refer to section 7.4.36.

4. The area covered by INST should follow section 7.6 SRAM rules requirements. If the rule is not re-defined in SRAM rules, the layout should follow this design rule section 7.4 Layout rule description.

5. DRC switch setting for design rule guideline, recommended rule and DFM rules.

Category	Rule	DRC switch setting by default
Guideline (Rule number with [G])	AA resistor guideline	Turn-on
	NW resistor guideline	Turn-on
	Poly resistor guideline	Turn-on
	ESD guideline	Turn-off
	Latch Up	Turn-on
	LDMOS	Turn-off
	BJT	Non-DRC check
	Inductor	Turn-on
	BUMP	Turn-off
	DUP	Turn-on
Recommended Rule/DFM Rule	LOGO	Turn-on
	MOM	MOM.5 ^[G] , MOM.6 ^[G] : Turn-on
Refer DFM section 7.5.2		



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7.1.6 SMIC layer mapping table

7.1.6.1 SMIC drawn layer mapping table

These drawn layers below listed are related with mask making.

Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
1	AA	10	0	Active Area
2	AADUM	10	1	AA Dummy pattern
3	NLDB	12	150	Mark layer for N+ LDD and pocket implant
4	PLDB	13	150	Mark layer for P+ LDD and pocket implant
5	NW	14	0	Nwell
6	PC	16	0	P-Cell Implant
7	DNW	19	0	Deep N well imp for substrate noise suppression
8	NC	21	0	N-Cell Implant
9	DG	29	0	IO1 medium gate OX area
10	GT	30	0	Poly Gate
11	GTDUM	30	1	GT Dummy pattern
12	HRP	39	0	High Resistant Poly Imp
13	SN	40	0	N+ S/D Implant
14	ESD1	41	0	ESD1 implant
15	SP	43	0	P+ S/D Implant
16	SAB	48	0	Salicide Block
17	CT	50	0	Contact Hole (Metal to Si/Poly)
18	INST	60	0	SRAM bitcell ,edge cell, strap cell or Instance Outline;SRAM bitcell ,edge cell ,strap cell area Block layer
19	DNSRAM	60	2	Marker shape to allow LVS to identity Q299 and H299 ,Q62,1.15 SRAM cells;
20	DPSRAM	60	4	Marker shape to allow LVS to identity DP576 and DPH576 ,DP974 ,DP1.994 dualport SRAM cells;
21	LRSRAM	60	5	Marker shape to allow LVS to identity Q556,Q374 and H374 SRAM cells
22	RFSRAM	60	9	Marker shape to allow LVS to identity F741 and F1158 SRAM cells;
23	D2SRAM	60	11	Marker shape to allow LVS to identity DP589 SRAM cells;
24	2PSRAM	60	12	Marker layer for LVS or logic operation to identity 2P563 SRAM cell
25	HPBL	60	150	MARK layer to block high performance sram
26	6TMK	60	151	Marker layer for 2P SRAM 7T SRAM transistor
27	M1	61	0	Metal-1
28	M1DUM	61	1	Metal-1 Dummy pattern
29	M1DOP	61	7	Metal 1 Dummy pattern layer is referenced in OPC engineering
30	M2	62	0	Metal-2

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Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
31	M2DUM	62	1	Metal-2 Dummy pattern
32	M2DOP	62	7	Metal 2 Dummy pattern layer is referenced in OPC engineering
33	M3	63	0	Metal3
34	M3DUM	63	1	Metal-3 Dummy pattern
35	M3DOP	63	7	Metal 3 Dummy pattern layer is referenced in OPC engineering
36	M4	64	0	Metal4
37	M4DUM	64	1	Metal-4 Dummy pattern
38	M4DOP	64	7	Metal 4 Dummy pattern layer is referenced in OPC engineering
39	M5	65	0	Metal5
40	M5DUM	65	1	Metal-5 Dummy pattern
41	M5DOP	65	7	Metal 5 Dummy pattern layer is referenced in OPC engineering
42	M6	66	0	Metal 6
43	M6DUM	66	1	Metal-6 Dummy pattern
44	M6DOP	66	7	Metal 6 Dummy pattern layer is referenced in OPC engineering
45	M7	67	0	Metal 7
46	M7DUM	67	1	Metal-7 Dummy pattern
47	M7DOP	67	7	Metal 7 Dummy pattern layer is referenced in OPC engineering
48	M8	68	0	Metal 8
49	M8DUM	68	1	Metal-8 Dummy pattern
50	M8DOP	68	7	Metal 8 Dummy pattern layer is referenced in OPC engineering
51	V1	70	0	Via-1 Hole
52	V1DUM	70	1	via-1 Dummy Layer (For dummy via insertion)
53	V2	71	0	VIA-2
54	V2DUM	71	1	via-2 Dummy Layer(For dummy via insertion)
55	V3	72	0	VIA-3
56	V3DUM	72	1	via-3 Dummy Layer(For dummy via insertion)
57	V4	73	0	VIA-4
58	V4DUM	73	1	Via-4 Dummy Layer (For dummy via insertion)
59	V5	74	0	Via 5
60	V5DUM	74	1	Via-5 Dummy Layer(For dummy via insertion)
61	V6	75	0	Via 6
62	V6DUM	75	1	Via-6Dummy Layer (For dummy via insertion)
63	V7	76	0	Via 7
64	V7DUM	76	1	via-7 Dummy Layer (For dummy via insertion)
65	PA	80	0	Passivation 1

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Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
66	FUSE	81	0	Fuse Window
67	ALPA	83	0	Al bonding pad & RDL
68	ALDUM	83	11	ALPA Dummy Layer
69	PSUB	85	0	Psub area(NN)
70	VARMOS	93	0	Block Layer to cover all MOS-type varactor(previous name :Var_MOS)
71	NCAP	93	1	Dummy for mos varactor in nwell
72	PCAP	93	2	Dummy for mos varactor in pwell.
73	RESP1	96	0	Dummy Pattern for Poly-1 Resistor(previous layer name:Res_P1)
74	RESAA	97	0	DRC/LVS mark layer for AA resistor
75	SDOP	99	0	SRAM PASS GATE
76	TM1	120	0	Top Metal 1
77	TM1DUM	120	1	TM-1 Dummy pattern
78	TV1	121	0	Top Via 1
79	TM2	122	0	Top Metal 2
80	TV2	123	0	Top via 2
81	TG	125	0	IO2 thick gate OX area
82	TGV	125	1	Marking layer for 1.5V or 1.8V TG device
83	OVERDR	125	3	Marking layer for 3.3V TG device
84	BORDER	127	0	Top Structure's Border
85	MD	130	0	Passivation 2
86	DSTR	138	0	Diode Marker (identifies a diode, for LVS only)
87	HVT	159	11	Marking layer for high-Vt devices
88	LVT	159	12	Marking layer for low-Vt devices
89	ULVT	159	152	Marker layer for Ultra low Vth device of 1.0V
90	BUMP	168	0	BUMP UBM marking layer for BUMP process opening.
91	LDBK	216	150	LDMOS function area
92	MTT2	231	0	Second Ultra Thick Top Metal (RF production application)
93	MTT2DM	231	1	MTT2(UTM) dummy pattern

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7.1.6.2 SMIC CAD layers mapping table

All the CAD layers are drawn layer and used for DRC, LVS special recognition marking layer.

Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
1	DNWTR	19	2	LVS six terminal DNW MOS
2	LOGO	26	0	LOGO
3	DGV	29	1	Marking layer for 1.2V high-speed I/O devices
4	M1PIN	61	251	Metal-1 pin layer
5	M1NET	61	253	Metal-1 net layer
6	M1LABEL	61	254	Metal-1 label layer
7	M2PIN	62	251	Metal-2 pin layer
8	M2NET	62	253	Metal-2 net layer
9	M2LABEL	62	254	Metal-2 label layer
10	VSIA	63	63	VSIA tagging layer(Text Only)
11	M3PIN	63	251	Metal-3 pin layer
12	M3NET	63	253	Metal-3 net layer
13	M3LABEL	63	254	Metal-3 label layer
14	M4PIN	64	251	Metal-4 pin layer
15	M4NET	64	253	Metal-4 net layer
16	M4LABEL	64	254	Metal-4 label layer
17	M5PIN	65	251	Metal-5 pin layer
18	M5NET	65	253	Metal-5 net layer
19	M5LABEL	65	254	Metal-5 label layer
20	M6PIN	66	251	Metal-6 pin layer
21	M6NET	66	253	Metal-6 net layer
22	M6LABEL	66	254	Metal-6 label layer
23	M7PIN	67	251	Metal-7 pin layer
24	M7NET	67	253	Metal-7 net layer
25	M7LABEL	67	254	Metal-7 label layer
26	M8PIN	68	251	Metal-8 pin layer
27	M8NET	68	253	Metal-8 net layer
28	M8LABEL	68	254	Metal-8 label layer
29	V1BAR	70	2	Via12 blockage for PR
30	V1DUB	70	6	Via-1 Dummy Blockage.
31	V1DOP	70	7	Via 1 Dummy pattern layer is referenced in OPC engineering
32	V1RB	70	8	V1 redundant via insertion blockage
33	V1RM	70	10	V1 mark layer to identify redundant via
34	V2BAR	71	2	Via23 blockage for PR
35	V2DUB	71	6	Via-2 Dummy Blockage
36	V2DOP	71	7	Via 2 Dummy pattern layer is referenced in OPC engineering
37	V2RB	71	8	V2 redundant via insertion blockage
38	V2RM	71	10	V2 mark layer to identify redundant via

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Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
39	V3BAR	72	2	Via34 blockage for PR
40	V3DUB	72	6	Via-3 Dummy Blockage
41	V3DOP	72	7	Via 3 Dummy pattern layer is referenced in OPC engineering
42	V3RB	72	8	V3 redundant via insertion blockage
43	V3RM	72	10	V3 mark layer to identify redundant via
44	V4BAR	73	2	Via45 blockage for PR
45	V4DUB	73	6	Via-4 Dummy Blockage
46	V4DOP	73	7	Via 4 Dummy pattern layer is referenced in OPC engineering
47	V4RB	73	8	V4 redundant via insertion blockage
48	V4RM	73	10	V4 mark layer to identify redundant via
49	V5BAR	74	2	Via56 blockage for PR
50	V5DUB	74	6	Via-5 Dummy Blockage
51	V5DOP	74	7	Via 5 Dummy pattern layer is referenced in OPC engineering
52	V5RB	74	8	V5 redundant via insertion blockage
53	V5RM	74	10	V5 mark layer to identify redundant via
54	V6BAR	75	2	Via67 blockage for PR
55	V6DUB	75	6	Via-6 Dummy Blockage
56	V6DOP	75	7	Via 6 Dummy pattern layer is referenced in OPC engineering
57	V6RB	75	8	V6 redundant via insertion blockage
58	V6RM	75	10	V6 mark layer to identify redundant via
59	V7BAR	76	2	Via78 blockage for PR
60	V7DUB	76	6	Via-7 Dummy Blockage
61	V7DOP	76	7	Via 7 Dummy pattern layer is referenced in OPC engineering
62	V7RB	76	8	V7 redundant via insertion blockage
63	V7RM	76	10	V7 mark layer to identify redundant via
64	GTFUSE	81	1	mark layer for EFUSE gate
65	EFUSE	81	2	mark layer Efuse
66	ALPAR	83	1	ALPA resistor layer
67	ALPATXT	83	2	ALPA text layer
68	ALDUB	83	6	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of LBFILL shapes.
69	SM	84	0	Stress memorization layer
70	TTXT	87	0	Text for Top Structure
71	CTXT	89	0	Text for Cell name
72	DUPMK1	89	156	Marking layer for pad with device underneath
73	OTPMK1	89	160	OTP mark layer 1
74	DUMBMB	90	0	Block Layer for Dummy operation on all Metal

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Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
75	DUMBA	91	0	Block Layer for Dummy operation on AA
76	OCCD	91	4	on chip CD check mark layer
77	OCOVL	91	5	on chip overlay check mark layer
78	DUMBP	92	0	Block Layer for Dummy operation on GT
79	VARJUN	94	0	DRC/LVS mark layer for junction varactor
80	RESNW	95	0	DRC/LVS mark layer for NW resistor
81	RESP3T	96	1	Dummy layer for Poly-1 Resistor with 3 terminal
82	PLRES	96	3	Dummy silicide poly resistor layer
83	DIFRES	97	3	Dummy silicide diffusion resistor layer
84	TM1TXT	120	3	TM1 text layer
85	TM1DOP	120	7	TOP Metal 1 Dummy pattern layer is referenced in OPC engineering
86	TM1PIN	120	251	Top metal 1 pin layer
87	TM1NET	120	253	Top metal 1 net layer
88	TM1LABEL	120	254	Top metal 1 label layer
89	TV1DUM	121	1	TV-1 Dummy Layer(For dummy via insertion)
90	TV1BAR	121	2	top via 1 Blockage for P&R
91	TV1DOP	121	7	TOP Via 1 Dummy pattern layer is referenced in OPC engineering
92	TV1RB	121	8	TV1 redundant via insertion blockage
93	TV1RM	121	10	TV1 mark layer to identify redundant via
94	TM2DUM	122	1	TM2 Dummy pattern
95	TM2TXT	122	3	TM2 text layer
96	TM2DOP	122	7	TOP Metal 2 Dummy pattern layer is referenced in OPC engineering
97	TM2PIN	122	251	Top metal 2 pin layer
98	TM2NET	122	253	Top metal 2 net layer
99	TM2LABEL	122	254	Top metal 2 label layer
100	TV2DUM	123	1	TV-2 Dummy Layer(For dummy via insertion)
101	TV2BAR	123	2	top via 2 Blockage for P&R
102	TV2DOP	123	7	TOP Via 2 Dummy pattern layer is referenced in OPC engineering
103	TV2RB	123	8	TV2 redundant via insertion blockage
104	TV2RM	123	10	TV2 mark layer to identify redundant via
105	PRBOUN	127	1	Pr Boundary layer,whole memory instance area
106	SUBD	131	1	LVS substrate separation layer
107	RESCKT	131	3	LVS dummy layer for subckt resistor
108	PLDMK	131	4	LVS marking layer for device dummy poly
109	NFDMK	131	5	LVS marking layer for mos multiple fingers
110	EXCLU	132	0	unDRC area
111	ESDIO1	133	0	DRC mark layer for SMIC I/O ESD protection devices and circuits identification. This layer should cover SMIC IO ESD transistors.

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Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
112	ESD5V	133	1	DRC dummy layer for high voltage tolerate stacked NMOS
113	POWRING	133	2	DRC dummy layer for power ring identification
114	ESDIO2	133	3	DRC mark layer for I/O ESD protection devices and circuits identification. This layer should cover ESD transistors and their N and P guard rings, but non-ESD transistors inside the same guard ring should be excluded, otherwise all the devices and circuits inside ESDIO2 will be regarded as ESD transistors and may induce false DRC alarm
115	DMPNP	134	0	LVS mark layer for BJT
116	CAPBP	137	0	Capacitor Bottom Plate
117	DCTY	139	0	Area with no Extraction for LVS
118	M1TXT	141	0	M1 text layer
119	M2TXT	142	0	M2 text layer
120	M3TXT	143	0	M3 text layer
121	M4TXT	144	0	M4 text layer
122	M5TXT	145	0	M5 text layer
123	M6TXT	146	0	M6 text layer
124	M7TXT	147	0	M7 text layer
125	M8TXT	148	0	M8 text layer
126	M1B	151	0	Blocking M1
127	M1DUB	151	1	Metal-1 Dummy Blockage (For dummy metal insertion) and exclude dummy insertion
128	M2B	152	0	Blocking M2
129	M2DUB	152	1	Metal-2 Dummy Blockage (For dummy metal insertion) and exclude dummy insertion
130	M3B	153	0	Blocking M3
131	M3DUB	153	1	Metal-3 Dummy Blockage (For dummy metal insertion) and exclude dummy insertion
132	M4B	154	0	Blocking M4
133	M4DUB	154	1	Metal-4 Dummy Blockage (For dummy metal insertion)and exclude dummy insertion
134	M5B	155	0	metal 5 blockage (for dummy insertion or P&R)[used by abstract/LEF]
135	M5DUB	155	1	Metal-5 Dummy Blockage(For dummy metal insertion)and exclude dummy insertion
136	M6B	156	0	metal 6 blockage (for dummy insertion or P&R)[used by abstract/LEF]
137	M6DUB	156	1	Metal-6 Dummy Blockage (For dummy metal insertion)and exclude dummy insertion
138	M7B	157	0	metal 7 blockage (for dummy insertion or P&R)[used by abstract/LEF]
139	M7DUB	157	1	Metal-7 Dummy Blockage (For dummy metal insertion)and exclude dummy insertion

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Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
140	M8B	158	0	metal 8 blockage (for dummy insertion or P&R)[used by abstract/LEF]
141	M8DUB	158	1	Metal-8 Dummy Blockage (For dummy metal insertion)and exclude dummy insertion
142	BIPOLA	159	1	Placed over NPN and PNP emitters.It's used to generated PH and eliminate halos to improve performance
143	PTCT	159	7	Used during the automatic kerf merge process during mask assembly of CP masks; associated with preventing mask back-ground overwrite.
144	WELTXT	162	0	Wells Pin Text Layer
145	DIFTXT	163	0	Diffusion Pin Text Layer
146	POLYTXT	164	0	Poly Pin Text Layer
147	M1R	171	0	M1 resistor layer
148	M1SLOTB	171	1	metal 1 slot blockage
149	M2R	172	0	M2 resistor layer
150	M2SLOTB	172	1	metal 2 slot blockage
151	M3R	173	0	M3 resistor layer
152	M3SLOTB	173	1	metal 3 slot blockage
153	M4R	174	0	M4 resistor layer
154	M4SLOTB	174	1	metal 4 slot blockage
155	M5R	175	0	M5 resistor layer
156	M5SLOTB	175	1	metal 5 slot blockage
157	M6R	176	0	M6 resistor layer
158	M6SLOTB	176	1	metal 6 slot blockage
159	M7R	177	0	M7 resistor layer
160	M7SLOTB	177	1	metal 7 slot blockage
161	M8R	178	0	M8 resistor layer
162	M8SLOTB	178	1	metal8 slot blockage
163	RFDEV	181	0	DRC/LVS mark layer for RF device
164	RFSD	181	3	RF MOS of even finger with S/D permute for LVS
165	RFBL	181	5	LVS mark layer for RF large signal MOS
166	RFMOSD	182	0	DRC/LVS mark layer for RF mos drain terminal
167	RF3T	183	2	DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM
168	MARKG	189	0	Guard ring mark for DRC check
169	MARKS	189	151	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage
170	TM1B	193	0	metal top 1 blockage (for dummy insertion or P&R)[used by abstract/LEF]
171	TM1DUB	193	1	First Top Metal Dummy Blockage(For dummy metal inserdion)and exclude dummy insertion
172	TM2B	194	0	metal top 2 blockage (for dummy insertion or P&R)[used by abstract/LEF]

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Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
173	TM2DUB	194	1	Second Top Metal Dummy Blockage(For dummy metal inserdion)and exclude dummy insertion
174	MTT2DB	194	2	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of MTT2FILL shapes.
175	TM1R	201	0	TM1 resistor layer
176	TM2R	202	0	TM2/MTT2 resistor layer
177	HRPDMY	210	0	HRP Dummy Layer
178	MOMDMY	211	1	DRC/LVS mark layer for MOM
179	INDMY	212	0	DRC/LVS mark layer for inductor
180	MTT2TXT	231	3	MTT2 text layer
181	MTT2PIN	231	251	Ultra thick top metal 2 pin layer
182	MTT2NET	231	253	Ultra thick top metal 2 net layer
183	MTT2LABEL	231	254	Ultra thick top metal 2 label layer
184	MOMP1	211	3	MOM capacitor mesh terminal one
185	MOMP2	211	4	MOM capacitor mesh terminal two
186	MOMMES	211	5	MOM capacitor mesh LVS mark layer
187	INDR	212	1	LVS layer to calculate inductor radius
188	RFDN5T	181	7	LVS mark layer for 5T MOS
189	RFDN6T	181	4	6-terminal RF MOS in deep NWELL for LVS,the sixth terminal is psub.
190	System reserved layers	187	0~255	Reserved for ICC P&R techfile layer mapping only. It is not allowed to define this layer in any other tech file.
191	CL	18	0	Cell Implant / Code Implant
192	INDTEM	212	3	LVS marking layer for inductor inter via
193	MOMCOL	211	7	LVS mark layer for MOM capacitor column number
194	MOMROW	211	8	LVS mark layer for MOM capacitor row number
195	MOMMK1	211	11	Marking layer for M1 MOM
196	MOMMK2	211	12	Marking layer for M2 MOM
197	MOMMK3	211	13	Marking layer for M3 MOM
198	MOMMK4	211	14	Marking layer for M4 MOM
199	MOMMK5	211	15	Marking layer for M5 MOM
200	MOMMK6	211	16	Marking layer for M6 MOM
201	MOMMK7	211	17	Marking layer for M7 MOM
202	MOMMK8	211	18	Marking layer for M8 MOM

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7.1.6.3 40G process only used layers

Below table listed layers are used for 40G process only

Sequence number	Design layer name	GDS layer No.	GDS data type	Layer description
1	PSR	6	0	PMOS recess/eSiGe PFET Si recess(GS)
2	PSRBL	6	239	Block layer for non-SiGe PFET Si recess(GS)
3	TP	15	0	PMOS VT imp for 0.9V Low Vt/Stand Vt device
4	TN	24	0	NMOS VT imp for 0.9V Low Vt/Stand Vt device
5	CTBAR	50	1	Rectangular stud contact; CTBAR is used only in the chip guard ring and part number/label field.
6	PABAR	80	2	Rectangular via used in the chip guard ring and inductor.
7	NWHT	110	0	N-Well Vt implant for 2.5V device
8	WN	203	0	PFET area open to the etching away of tensile nitride
9	WNBL	203	239	marking layer for area blocked to etch tensile nitride
10	WP	204	0	Areas blocked in PFET for compressive nitride etch
11	WPBL	204	239	marking layer for area blocked to etch compressive nitride

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7.1.6.4 40LL mask layer mapping table

Below table listed layers are used for mask making. In column “Drawn”, “Generated” means logical operation used for mask making. “Drawn” means no logical operation used for mask making.

From Top Tier Table LCMO40-V00.

Mask ID	Process Name	Dig. Area Tone	Drawn	Description
120	AA	D	Generated	Active area
292	DNW	C	Generated	Deep N well imp for substrate noise suppression
192	NW	C	Generated	N well
191	PW	C	Generated	P well
492	NWH	C	Generated	1.8V N well
491	PWH	C	Generated	1.8V P well
494	PWHT	C	Generated	PW IO2
145	TG	D	Generated	IO2 thick gate OX area
131	DG	D	Generated	IO1 medium gate OX area
245	UG	D	Generated	Ultra Thin Gate Oxide Device
412	HR	C	Generated	N+ Polysilicon pre-doping layer
130	GT	D	Generated	Poly
214	NLHT	C	Generated	IO2(2.5V) NMOS LDD implant
215	PLHT	C	Generated	IO2 PMOS LDD implant
114	NLH	C	Generated	IO1(1.8V) NMOS LDD implant
115	PLH	C	Generated	IO1(1.8V) PMOS LDD implant
194	PC	C	Generated	P-Cell Implant
193	NC	C	Generated	N-Cell Implant
295	MVP	C	Generated	HP P-cell implant
296	MVN	C	Generated	HP N-cell implant
593	ULVP	C	Generated	Ultra low VT PMOS
594	ULVN	C	Generated	Ultra low VT NMOS
595	LVP	C	Generated	Low VT PMOS implant
113	PLL	C	Generated	SVT PMOS LDD Implant
395	VTPH	C	Generated	High Vt PMOS implant
596	LVN	C	Generated	Low VT NMOS implant
116	NLL	C	Generated	SVT NMOS LDD Implant
396	VTNH	C	Generated	High Vt NMOS implant
197	SP	C	Generated	P+ S/D Implant
198	SN	C	Generated	N+ S/D Implant
413	HRP	C	Drawn	High Resistant Poly Imp
301	SM	D	Generated	Stress memorization layer
155	SAB	D	Generated	Salicide Block
110	ESD1	C	Drawn	ESD1 implant
156	CT	C	Drawn	Contact
160	M1	C	Generated	Metal 1
180	M2	C	Generated	Metal 2
175	V5	C	Generated	Via 5

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Mask ID	Process Name	Dig. Area Tone	Drawn	Description
183	M5	C	Generated	Metal 5
178	V1	C	Generated	Via 1
179	V2	C	Generated	Via 2
181	M3	C	Generated	Metal 3
182	M4	C	Generated	Metal 4
177	V3	C	Generated	Via 3
176	V4	C	Generated	Via 4
107	PA	C	Generated	Passivation 1
184	M6	C	Generated	Metal 6
174	V6	C	Generated	Via 6
185	M7	C	Generated	Metal 7
173	V7	C	Generated	Via 7
186	M8	C	Generated	Metal 8
142	TV1	C	Generated	Top Via 1
141	TM1	C	Generated	Top Metal 1
144	TV2	C	Generated	Top via 2
143	TM2	C	Generated	Top Metal 2
108	ALPA	D	Generated	Al bonding pad & RDL
163	MD	C	Drawn	Passivation 2
543	MTT2	C	Generated	Second Ultra Thick Top Metal (RF production application)
	MARKS		Drawn	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage
	INDMY		Drawn	DRC/LVS mark layer for inductor
	BFMOAT		Drawn	Used to block p-well implants from BFMOAT regions that isolate regions to create a resistive path
	PTCT		Drawn	Used during the automatic kerf merge process during mask assembly of CP masks; associated with preventing mask back-ground overwrite.
	HRPDMDY		Drawn	HRP Dummy Layer
	DIFRES		Drawn	Dummy layer for diffusion silicide resistor
	PLRES		Drawn	Dummy layer for poly silicide resistor
	PLRES		Drawn	Dummy layer for poly silicide resistor
	MARKG		Drawn	Guard ring mark for DRC check
	GTFUSE		Drawn	mark layer for EFUSE gate
	V7DUB		Drawn	Via-7 Dummy Blockage
	V6DUB		Drawn	Via-6 Dummy Blockage
	V5DUB		Drawn	Via-5 Dummy Blockage
	V4DUB		Drawn	Via-4 Dummy Blockage
	V3DUB		Drawn	Via-3 Dummy Blockage
	V2DUB		Drawn	Via-2 Dummy Blockage
	V1DUB		Drawn	Via-1 Dummy Blockage.

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Mask ID	Process Name	Dig. Area Tone	Drawn	Description
	MTT2DB		Drawn	Ultra Thick top Metal2 dummy blockage mark layer
	M8DUB		Drawn	Block Layer for Dummy operation on M8 (For dummy-fill utility only)
	M7DUB		Drawn	Block Layer for Dummy operation on M7 (For dummy-fill utility only)
	M6DUB		Drawn	Block Layer for Dummy operation on M6 (For dummy-fill utility only)
	M5DUB		Drawn	Block Layer for Dummy operation on M5 (For dummy-fill utility only)
	M4DUB		Drawn	Block Layer for Dummy operation on M4 (For dummy-fill utility only)
	M3DUB		Drawn	Block Layer for Dummy operation on M3 (For dummy-fill utility only)
	M2DUB		Drawn	Block Layer for Dummy operation on M2 (For dummy-fill utility only)
	M1DUB		Drawn	Block Layer for Dummy operation on M1 (For dummy-fill utility only)
	MTT2DM	C	Drawn	MTT2(UTM) dummy pattern
	M8DOP	C	Drawn	Metal 8 Dummy pattern layer is referenced in OPC engineering
	M7DOP	C	Drawn	Metal 7 Dummy pattern layer is referenced in OPC engineering
	M6DOP	C	Drawn	Metal 6 Dummy pattern layer is referenced in OPC engineering
	M5DOP	C	Drawn	Metal 5 Dummy pattern layer is referenced in OPC engineering
	M4DOP	C	Drawn	Metal 4 Dummy pattern layer is referenced in OPC engineering
	M3DOP	C	Drawn	Metal 3 Dummy pattern layer is referenced in OPC engineering
	M2DOP	C	Drawn	Metal 2 Dummy pattern layer is referenced in OPC engineering
	M1DOP	C	Drawn	Metal 1 Dummy pattern layer is referenced in OPC engineering
	TM2DUM	C		TM2 Dummy pattern
	TM1DUM	C		TM-1 Dummy pattern
	M8DUM	C		Metal-8 Dummy pattern
	M7DUM	C		Metal-7 Dummy pattern
	M6DUM	C		Metal-6 Dummy pattern
	M5DUM	C		Metal-5 Dummy pattern
	M4DUM	C		Metal-4 Dummy pattern
	M3DUM	C		Metal-3 Dummy pattern
	M2DUM	C		Metal-2 Dummy pattern
	M1DUM	C		Metal-1 Dummy pattern
	INST		Drawn	SRAM bitcell mark layer
	RESAA		Drawn	AA resistor mark layer

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Mask ID	Process Name	Dig. Area Tone	Drawn	Description
	DUMBA		Drawn	Dummy AA blockage
	AADUM			AA Dummy pattern
	ALDUM			ALPA Dummy Layer
	PLDB		Drawn	Mark layer for P+ LDD and pocket implant
	VARMOS		Drawn	Mark Layer to cover all MOS-type varactor
	HVT		Drawn	Marking layer for high-Vt devices
	LVT		Drawn	Marking layer for low-Vt devices
	NCAP		Drawn	Mark layer for NFET in n-well capacitors
	RESP1		Drawn	Poly resistor mark layer
	NLDB		Drawn	Mark layer for N+ LDD and pocket implant
	PCAP		Drawn	Mark layer for PFET in p-well capacitors
	EFUSE		Drawn	Mark layer for an electrical fuse
	PSUB		Drawn	Native device
	DUMB		Drawn	Dummy poly blockage
	GTDUM		Drawn	GT Dummy pattern
	TM1DUB		Drawn	Block Layer for Dummy operation on TM1 (For dummy-fill utility only)
	DUMBM		Drawn	Dummy metal blockage
	TM2DUB		Drawn	Block Layer for Dummy operation on TM2 (For dummy-fill utility only)
	ALDUB		Drawn	ALPA dummy blockage
	HPBL		Drawn	Marker layer to Block High Performance SRAM bitcell
	6TMK		Drawn	Marker layer for 2P SRAM 6T SRAM transistor
	DNSRAM		Drawn	Marker layer for LVS or logic operation to identity SP299 SRAM cell
	LRSRAM		Drawn	Marker layer for LVS or logic operation to identity SP374 SRAM cell
	D2SRAM		Drawn	Marker layer for LVS or logic operation to identity DP589 SRAM cell
	RFSRAM		Drawn	Marker layer for LVS or logic operation to identity DP741 SRAM cell
	2PSRAM		Drawn	Marker layer for LVS or logic operation to identity 2P562 SRAM cell
	RESNW		Drawn	N well resistor mark layer
	LDBK		Drawn	Identify LDMOS function area and do related logic operation in IMP layers
	SDOP		Drawn	SRAM pass gate
	OVERDR		Drawn	Marking layer for 3.3V TG device
	ULVT		Drawn	Marking layer for Ultra low-Vt devices
	V1DUM			via-1 Dummy Layer (For dummy via insertion)

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Mask ID	Process Name	Dig. Area Tone	Drawn	Description
	V2DUM			via-2 Dummy Layer(For dummy via insertion)
	V3DUM			via-3 Dummy Layer(For dummy via insertion)
	V4DUM			via-4 Dummy Layer(For dummy via insertion)
	V5DUM			Via-5 Dummy Layer(For dummy via insertion)
	V6DUM			via-6 Dummy Layer(For dummy via insertion)
	V7DUM			via-7 Dummy Layer(For dummy via insertion)
	TGV		Drawn	Marking layer for 1.5V or 1.8V TG device

Note: Please refer DCC document **PM-DATA-02-2001** layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.



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7.1.6.5 40G mask layer name mapping table

Mask ID	Layer name	Mask tone	GDS No	GDS data type	Mask Generation Formula	Description
120	AA	D	10	0	To be filled	Active area
192	NW	C	14	0		N-Well for 0.9/1.8V/2.5V device
191	PW	C	20	0		P-Well for 0.9/1.8V/2.5V device
292	DNW	C	19	0		Deep N well imp for substrate noise suppression
495	NWHT	C	110	0		N-Well Vt implant for 2.5V device
494	PWHT	C	109	0		P-Well Vt imp for 2.5V device
492	NWH	C	106	0		N-well for 1.8V device
491	PWH	C	105	0		P-well for 1.8V device
395	VTPH	C	46	0		PMOS VT imp for 0.9V high Vt device
396	VTNH	C	47	0		NMOS VT imp for 0.9V high Vt device
195	TP	C	15	0		PMOS VT imp for 0.9V Low Vt/Stand Vt device
196	TN	C	24	0		NMOS VT imp for 0.9V Low Vt/Stand Vt device
146	SDOP	C	99	0		SRAM pass gate
145	TG	D	125	0		Triple-gate: Thick gate oxide area
131	DG	D	29	0		Dual-gate: Medium gate oxide area
412	HR	C	34	0		N+ Polysilicon pre-doping layer
130	GT	D	30	0		Polysilicon layer
201	PSR	C	6	0		eSiGe recess PFET
595	LVP	C	218	0		PMOS LDD implantation for 0.9V low Vt device
113	PLL	C	38	0		PMOS LDD implantation for 0.9V stand Vt/high Vt device
194	PC	C	16	0		P SRAM implant
193	NC	C	21	0		N SRAM implant
296	MVN	C	45	0		HP N-cell implant
114	NLH	C	36	0		NMOS LDD implantation for 1.8V device

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Mask ID	Layer name	Mask tone	GDS No	GDS data type	Mask Generation Formula	Description
115	PLH	C	37	0		PMOS LDD implantation for 1.8V device
214	NLHT	C	114	0		NMOS LDD implantation for 2.5V device
215	PLHT	C	115	0		PMOS LDD implantation for 2.5V device
596	LVN	C	219	0		NMOS LDD implantation for 0.9V low Vt device
116	NLL	C	35	0		NMOS LDD implantation for 0.9V stand Vt/high Vt device
197	SP	C	43	0		P+ S/D implantation
198	SN	C	40	0		N+ S/D implantation
301	SM	D	84	0		Area open to the removal of stress nitride
155	SAB	D	48	0		Salicide Block
398	WN	C	203	0		NFET Tensile SiN film Cap
397	WP	D	204	0		PFET Compressive SiN film Cap
156	CT	C	50	0		Contact
	CTBAR	C	50	1		Rectangular stud contact; CTBAR is used only in the chip guard ring and part number/label field.
160	M1	C	61	0		Metal-1
	M1DUM	C	61	1		Metal-1 Dummy Layer (For dummy metal insertion)
178	V1	C	70	0		VIA-1
	V1BAR	C	70	2		Rectangular via for connection M1 to M2
181	M2	C	62	0		Metal-2
	M2DUM	C	62	1		Metal-2 Dummy Layer (For dummy metal insertion)
179	V2	C	71	0		VIA-2
	V2BAR	C	71	2		Rectangular via for connection M2 to M3
181	M3	C	63	0		Metal-3
	M3DUM	C	63	1		Metal-3 Dummy Layer (For dummy metal insertion)

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Mask ID	Layer name	Mask tone	GDS No	GDS data type	Mask Generation Formula	Description
177	V3	C	72	0		VIA-3
	V3BAR	C	72	2		Rectangular via for connection M3 to M4
182	M4	C	64	0		Metal-4
	M4DUM	C	64	1		Metal-4 Dummy Layer (For dummy metal insertion)
176	V4	C	73	0		VIA-4
	V4BAR	C	73	2		Rectangular via for connection M4 to M5
183	M5	C	65	0		Metal-5
	M5DUM	C	65	1		Metal-5 Dummy Layer (For dummy metal insertion)
175	V5	C	74	0		VIA-5
	V5BAR	C	74	2		Rectangular via for connection M5 to M6
184	M6	C	66	0		Metal-6
	M6DUM	C	66	1		Metal-6 Dummy Layer (For dummy metal insertion)
174	V6	C	75	0		VIA-6
	V6BAR	C	75	2		Rectangular via for connection M6 to M7
185	M7	C	67	0		Metal-7
	M7DUM	C	67	1		Metal-7 Dummy Layer (For dummy metal insertion)
173	V7	C	76	0		VIA-7
	V7BAR	C	76	2		Rectangular via for connection M7 to M8
186	M8	C	68	0		Metal-8
	M8DUM	C	68	1		Metal-8 Dummy Layer (For dummy metal insertion)
142	TV1	C	121	0		Top Via 1
	TV1BAR	C	121	2		Rectangular via used in the chip guard ring and inductor.

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Mask ID	Layer name	Mask tone	GDS No	GDS data type	Mask Generation Formula	Description
141	TM1	C	120	0		Top Metal 1
	TM1DUM	C	120	1		TM-1 Dummy Layer (For dummy metal insertion)
144	TV2	C	123	0		Top Via 2
	TV2BAR	C	123	2		Rectangular via used in the chip guard ring and inductor.
143	TM2	C	122	0		Top Metal 2
	TM2DUM	C	122	1		TM2 Dummy Layer (For dummy metal insertion)
107	PA	C	80	0		Passivation
	PABAR	C	80	2		Rectangular via used in the chip guard ring and inductor.
108	ALPA	D	83	0		AlCu Bonding Pad
	ALDUM	D	83	11		AlCu dummy
163	MD	C	130	0		Passivation 2
106	FUSE	C	81	0		Fuse window
	WN		203	0		PFET area open to the etching away of tensile nitride/HV N-BODY implant for power P type device
	WP		204	0		Areas blocked in PFET for compressive nitride etch/HV P-BODY implant for power n type device
	NFDMK		131	5		LVS marking layer for mos multiple fingers
	BIPOLA		159	1		Placed over NPN and PNP emitters. It is used to generate PH and eliminate halos to improve bipolar performance

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7.1.7 Metal Option Table

Metal options definition scheme is denoted in this section for metal layer, and is limited only to those options present in the table.

The scheme uses the following naming: xPyM_(y-z-w)Ic_zTMC_wMTTc_ALPAu

Where:

P = poly layers,

M = total metal layers excluding AL pad/Al RDL,

Ic= Cu inter metal layers (included M1),

TMC= Cu top metal layers,

MTTc=Cu Ultra thick metal,

ALPA = AL bonding pad/Al RDL

x = number of poly layers,

y = number of total metal layers,

z = number of top metal layers,

w = number of Ultra thick metal layers.

u = type of ALPA, 1 type AL14.5k, 2 type AL28k .

For z=0 or w =0 process, the naming of metallization table don't include TM or MTT2.

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Table 7.1.7-1 Metal Option Table 4-6 Cu metal

Metallization Options table			IP4M_3lc_ITMC_ALPA1	IP4M_3lc_IMTTc_ALPA1	IP4M_3lc_ITMC_ALPA2	IP4M_3lc_IMTTc_ALPA2	IP5M_4lc_ITMC_ALPA1	IP5M_4lc_IMTTc_ALPA1	IP5M_3lc_2TMC_ALPA1	IP5M_3lc_ITMC_1MTTc_ALPA1	IP5M_3lc_ITMC_1MTTc_ALPA1	IP5M_4lc_ITMC_ALPA2	IP5M_4lc_IMTTc_ALPA2	IP5M_3lc_2TMC_ALPA2	IP5M_3lc_ITMC_1MTTc_ALPA2	IP5M_3lc_ITMC_1MTTc_ALPA2	IP6M_5lc_ITMC_ALPA1	IP6M_5lc_ITMC_ALPA1	IP6M_4lc_2TMC_ALPA1	IP6M_4lc_ITMC_1MTTc_ALPA1	IP6M_5lc_ITMC_ALPA2	IP6M_5lc_IMTTc_ALPA2	IP6M_4lc_2TMC_ALPA2	IP6M_4lc_ITMC_1MTTc_ALPA2	IP6M_4lc_ITMC_1MTTc_ALPA2	
total metal layers	4	4	4	4	5	5	5	5	5	5	5	5	5	5	5	5	6	6	6	6	6	6	6	6	6	
Mn (n = 1 ~ 8) wiring level in BD metal minium m pitch W / S = 0.07 /0.07 um	160	M1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
	178	V1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
	180	M2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
	179	V2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
	181	M3	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
	177	V3					x	x			x	x			x	x	x	x	x	x	x	x	x	x	x	
	182	M4				x	x			x	x			x	x	x	x	x	x	x	x	x	x	x	x	
	176	V4													x	x			x	x						
	183	M5													x	x			x	x						
	175	V5													x	x			x	x						
	184	M6													x	x			x	x						
	174	V6													x	x			x	x						
	185	M7													x	x			x	x						
	173	V7													x	x			x	x						
	186	M8													x	x			x	x						
Top metal min pitch W / S = 0.40/ 0.40um	142	TV1							x	x			x	x			x	x			x	x				
	141	TM1							x	x			x	x			x	x			x	x				
	144	TV2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
	143	TM2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
Ultra Thick Metal	144	TV2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
	543	MTT2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
	107	PAS1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
Al RDL W/S=2/2um	108	AL14.5k	x	x			x	x	x	x					x	x	x	x								
	108	AL28k			x	x					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
	163	PAS2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		

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Table 7.1.7-2 Metal Option Table 7-10 Cu metals

Metallization Options table									
		total metal layers							
Mn (n = 1 ~ 8) wiring level in BD metal minimum pitch W / S = 0.07 / 0.07 um	160	M1	x	x	x	x	x	x	IP7M_6lc_1TMC_ALPA1
	178	V1	x	x	x	x	x	x	IP7M_5lc_2TMC_ALPA1
	180	M2	x	x	x	x	x	x	IP7M_5lc_1TMC_1MTTC_ALPA1
	179	V2	x	x	x	x	x	x	IP7M_6lc_1TMC_ALPA2
	181	M3	x	x	x	x	x	x	IP7M_5lc_2TMC_ALPA2
	177	V3	x	x	x	x	x	x	IP8M_7lc_1TMC_ALPA1
	182	M4	x	x	x	x	x	x	IP8M_5lc_2TMC_ALPA2
	176	V4	x	x	x	x	x	x	IP8M_7lc_1TMC_ALPA1
	183	M5	x	x	x	x	x	x	IP8M_6lc_2TMC_ALPA1
	175	V5	x	x		x	x	x	IP8M_6lc_1TMC_1MTTC_ALPA1
	184	M6	x	x		x	x	x	IP8M_7lc_1TMC_ALPA2
	174	V6				x	x	x	IP8M_6lc_2TMC_ALPA2
	185	M7				x	x	x	IP8M_7lc_1TMC_ALPA1
	173	V7					x	x	IP8M_8lc_1TMC_ALPA1
	186	M8					x	x	IP8M_8lc_2TMC_ALPA1
	142	TV1		x	x		x	x	IP9M_7lc_1TMC_1MTTC_ALPA1
	141	TM1		x	x		x	x	IP9M_7lc_2TMC_ALPA2
	144	TV2	x	x	x	x	x	x	IP9M_8lc_1TMC_ALPA1
	143	TM2	x	x	x	x	x	x	IP9M_8lc_2TMC_ALPA2
Ultra Thick Metal	144	TV2	x	x	x	x	x	x	IP9M_8lc_1TMC_ALPA1
	543	MTT2	x	x	x	x	x	x	IP9M_8lc_2TMC_ALPA2
		107	PAS1	x	x	x	x	x	x
Al RDL W/S=2/ 2um	108	AL14.5k	x	x	x	x	x	x	x
	108	AL28k			x	x	x	x	x
		163	PAS2	x	x	x	x	x	x

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7.1.8 Device layout truth table

The layer marked in “1” denotes this layer is a must for the device.

The layer marked in “0” denotes this layer is must not for the device.

The layer marked in “*” denotes this layer is uncaring for the device structures or is based on circuit level design requirement.

For MOS SAB/ESD1/ESDIO2/ESD5V layers setting “0/*”, the “0”denotes SAB/ESD1/ESDIO2/ESD5V layers are must not for typical MOS device;

The “*” denotes the special usage for ESD MOS only. LVS will treat “0/*” as “*”.



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Drawing Layer Name		SPICE Name	AA	10	0	0	19	DNW	NW	0	0	14	PSUB	SDOP	TG	DG	GT	LVT	HVT	ULVT	DGV	TGV	OVERDR	SP	SN	PLRES	RESNW	INST	LRSRAM	DPSRAM	RFSRAM	D2SRAM	DNSRAM	2PSRAM	HPBL	EFUSE	GIFUSE	LDBK	BIPOLA	VARMOS	HRP	INDMY	MOMDMY	ESDI	ESDIO2	ESDSV	PCAP	NCAP
Drawing Layer GDS No.			0	10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
Drawing Layer GDS Data Type			1	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
MOS	1.1v Regular -VT (RVT) NMOS	n11ll_ckt	1	*	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
	1.1v Regular -VT (RVT) PMOS	p11ll_ckt	1	*	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
	1.1v Low -VT NMOS	nlvt11ll_ckt	1	*	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
	1.1v Low -VT PMOS	plvt11ll_ckt	1	*	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
	1.1v Ultra Low-VT NMOS	nulvt11lll_ckt	1	*	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
	1.1v Ultra Low-VT PMOS	pulvt11lll_ckt	1	*	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
	1.1v High-VT NMOS	nhvt11ll_ckt	1	*	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									
	1.1v High-VT PMOS	phvt11ll_ckt	1	*	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0								
	1.8v IO1 NMOS	---	1	*	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									
	1.8v IO1 PMOS	---	1	*	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									

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Drawing Layer Name		SPICE Name	AA	10	0	19	DNW	NW	PSUB	SDOP	TG	DG	GT	LVT	HVT	ULVT	DGV	TGV	OVERDR	SP	SN	SAB	RESAA	DIFRES	RESP1	PLRES	RESNW	INST	LRSRAM	DPSRAM	RFSRAM	D2SRAM	DNSRAM	2PSRAM	HPBL	EFUSE	GTFUSE	LDBK	BIPOLA	VARMOS	HRP	INDMY	MOMDMY	ESDI	ESDIO2	ESDSV	PCAP	NCAP
Drawing Layer GDS No.			---	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
Drawing Layer GDS Data Type			1.8v UD 1.5v IO1 NMOS	---	1	*	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
1.8v UD 1.5v IO1 PMOS		---	1	*	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v IO2 NMOS		n25ll_ckt	1	*	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v IO2 PMOS		p25ll_ckt	1	*	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v UD 1.8v IO2 NMOS		nud18ll_ckt	1	*	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v UD 1.8v IO2 PMOS		pud18ll_ckt	1	*	1	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v OD 3.3v IO2 NMOS		nod33ll_ckt	1	*	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v OD 3.3v IO2 PMOS		pod33ll_ckt	1	*	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
1.1v zero-Vt NMOS		nt11ll_ckt	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
1.8v IO1 zero-Vt NMOS		---	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v IO2 zero-Vt NMOS		nt25ll_ckt	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
2.5v OD 3.3V IO2 zero-Vt NMOS		ntod33ll_ckt	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					



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Note: For the drawn layers don't be listed in the device layout truth table, all of them are uncaring layers for the device list in above table.



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7.1.9 Design Rules Nomenclatures and Abbreviations

Abbreviation	Definition
PW	Any chip area not (NW OR PSUB)
GATE	Poly AND AA
Real gate	Type 1: <ul style="list-style-type: none">a. the same AA separated by polyb. the separated AA parts both have CT on itc. The GT has CT on it. Type 2: Figure 7.1.9.13-3's style by (GT AND AA) Type 3: LDMOS' (GT AND AA) Gate may be possibly defined by following script to cover above 3 types: <pre>GATE0 = (GT INTERACT CT) AND AA // poly gate with CT AA1 = (AA INTERACT GATE0) NOT GATE0 // S/D AA AA2 = AA1 TOUCH GATE0 => 2 // for those S/D AA like traditional transistor AA3 = AA1 INTERACT CT //S/D AA with CT AA4 = AA2 OR AA3 // std transistor(S/D AA OR AA with CT). use OR to include fig 7.19.13-3 case GATE1 = GATE0 TOUCH AA4 == 2 // define std transistor gate GATE2 = GATE0 AND LDBK // define gate in LDMOS gate = GATE1 OR GATE2</pre>
Gate side	The edge of the gate that is abutting (AA NOT GT)
Gate end	The edge of the gate that is abutting (GT NOT AA)
N+AA	(AA AND SN) NOT NW
N+ PICKUP AA	(AA AND SN) AND NW
P+AA	(AA AND SP) AND NW
P+ PICKUP AA	(AA AND SP) NOT NW
N+ butted AA	SNx = SN edge cross AA N+ butted AA = SNx AND AA
P+ butted AA	SPx = SP edge cross AA P+ butted AA = SPx AND AA
Floating AA or GT	AA or GT not interact with CT
Non-floating AA or GT	AA or GT interact with CT. AA or GT has CT on it.
Different or same net	Electrically based connectivity using all conducting layers (unless otherwise noted), including diffusion, polysilicon, and all back-end-of-line (BEOL) metal and via layers in the stack (M1 through last metal). It also includes connectivity through the substrate, through n-wells and p-wells and between n-wells through the deep n-band (for triple-well

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Abbreviation	Definition
	designs).
Field OX, STI	(BORDER/bounding box extending to all data) NOT (AA OR AADUM)
Line End extension &Line Corner	See Figure 7.1.9.13-1 line end and Figure 7.1.9.13-2 for line corner definition
Corner via, corner contact	The vias or contacts which have the nearest distance to the related said AA, GT or metal corner
Line end	ANGLE1 A1==90 deg LENGTH1 L1 >=0.08um, ANGLE2 A2 ==90 deg, LENGTH2 L2 >=0.08um, WITH LENGTH W <=0.11um. See fig 7.1.9.13-4 If the rule specifies waive extrusion with a number F < 0.08. L1 and L2 should use the specified number F identify line end. For example, if the rule specifies waive extrusion F < 0.04, then L1 and L2 should be larger or equal than 0.04 for line end detection.

- Line end extension to Via along the direction of length: A
- Line enclosure by Via along the direction of width: C and D.

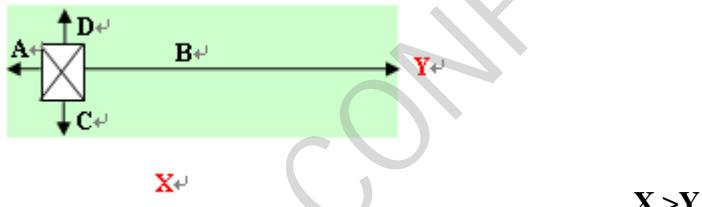


Figure 7.1.9.13-1 line end

- **Via at line corner when A < C, B < D**

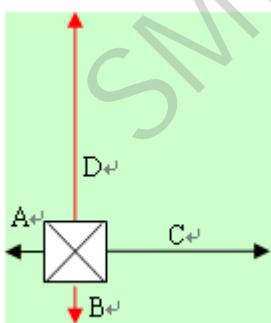


Figure 7.1.9.13-2 line corner

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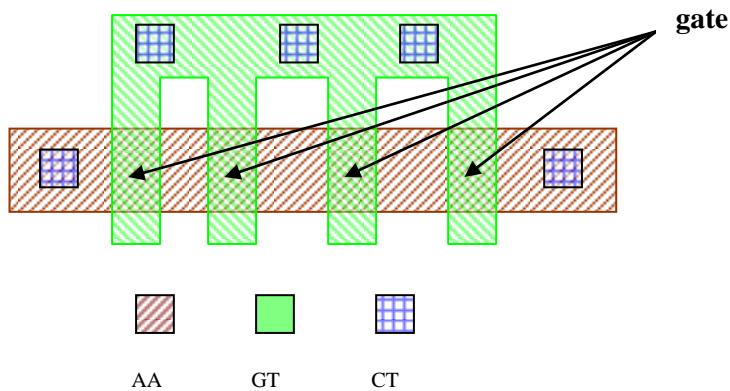
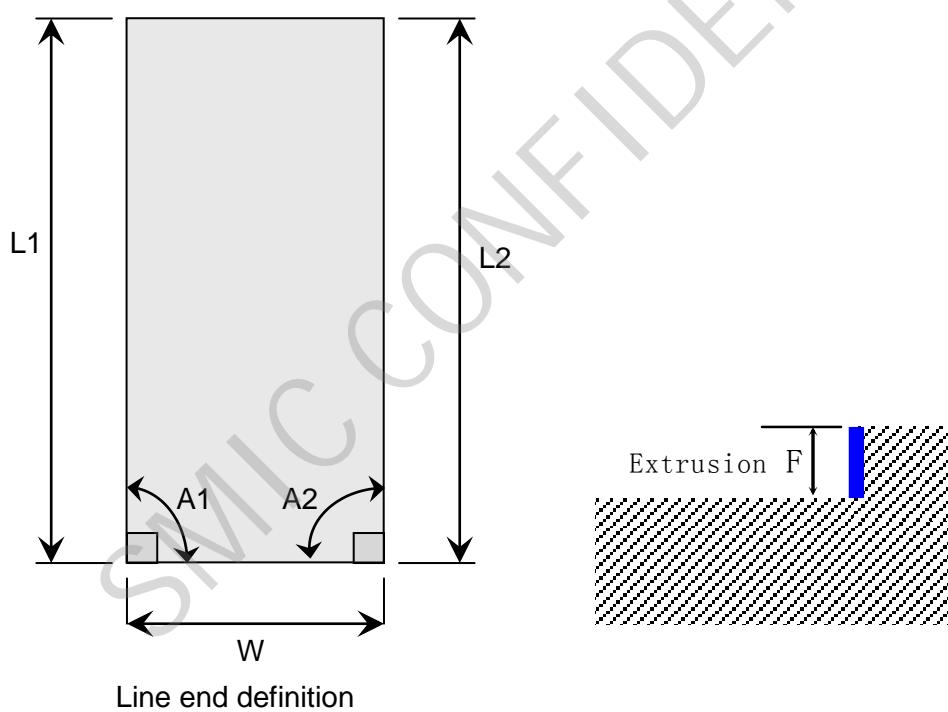


Figure 7.1.9.13-3 one type of gate definitions



Line end definition

Fig. 7.1.9.13-4

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7.1.10 Definition of terminology used in these design rules

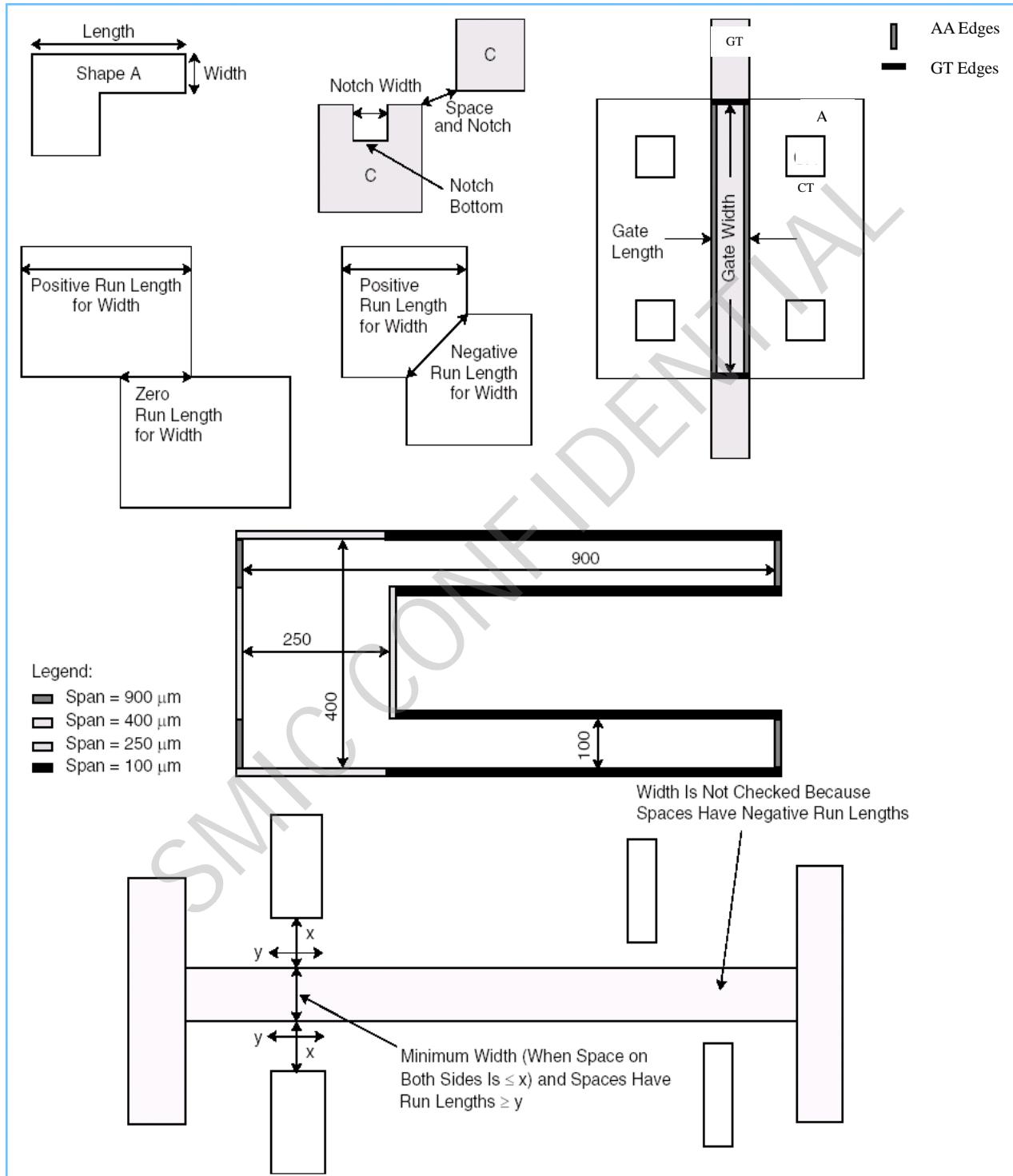
The single-letter abbreviation denoted in boldfaced type represents a shape on the corresponding design level. For example, **A** refers to a shape on design level “A”.

7.1.10.1 Dimensions

Length	The distance between the inside edges of an individual shape. Length is the longer side of the shape measured between parallel edges or edges that form an angle of less than 90°
Width	The distance between the inside edges of an individual shape. Width is the shorter side of the shape measure between parallel edges or edges that from an angle of less than 90°
A width with run length	The distance between two inside edges running in parallel; used for measuring the width between two parallel edges. This syntax applies to one or two shapes only.
A minimum width (when space on both sides is \leq x) and spaces have run lengths \geq y	Distance between the inside edges of an individual shape, when the space on both sides of the shape is constrained to value x and spaces have run lengths constrained to value y. Qualifiers can be added after “space.” For example: <ul style="list-style-type: none">• GT minimum width (when space on both sides is \leq 0.125 μm) and spaces have run lengths $>$ 0.• M1 minimum width (when space to M1_end on both sides is \leq 0.070 μm) and spaces have run lengths $>$ 0.
A Length and Width	Shape A is a square with equal length and width
Gate Length	The distance (from GT edge to GT edge) over AA
Gate Width	The distance (from AA edge to AA edge) over GT
C Notch	The distance between outside edges of the individual shape
C notch between parallel edges	The distance between parallel outside edges of an individual shape.
C Space	The distance between all outside edges of shape on level C to another shape on level C
C space and notch	The distance between all outside edges of all shapes on level C.

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Figure 7.1.10.1-1 Dimension Definitions

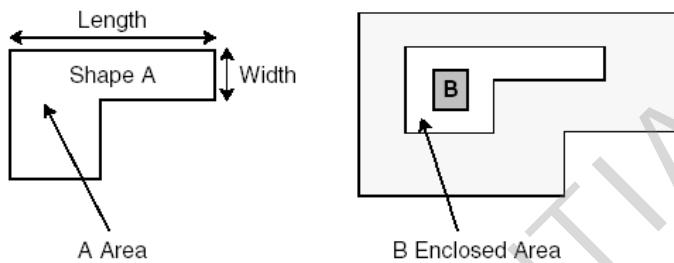


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7.1.10.2 Area

Area	The area of the shape
Enclosed Area	The space between the outside edges of one or more shape

Figure 7.1.10.2-1 Area Definitions



7.1.10.3 Density

Density	The ratio of the area of all shapes on level A within the window divided by the area of the window
A density with tiling within B	<p>Pattern density checks use the following tiling components:</p> <ul style="list-style-type: none"> <i>Box size.</i> The dimensions of the tile. <i>Step increment.</i> Tiles are stepped in increments equal to half the tile dimension. <i>Step-back requirement.</i> For (least-enclosing rectangle B) width \geq box size, incomplete tiles at the edge of B must be stepped back within the least-enclosing rectangle B. For (least-enclosing rectangle B) width $<$ box size, the density must be calculated as the ratio of the total area of A within the intersection of the checking box and B divided by the area of the intersection of the checking box and B. <i>Irregular edges.</i> For checking boxes not completely covered by B that meet the step-back requirement, the density must be calculated as the ratio of the total area of A within the intersection of the checking box and B divided by the area of the intersection of the checking box and B.

7.1.10.4 Geometry and Orientation

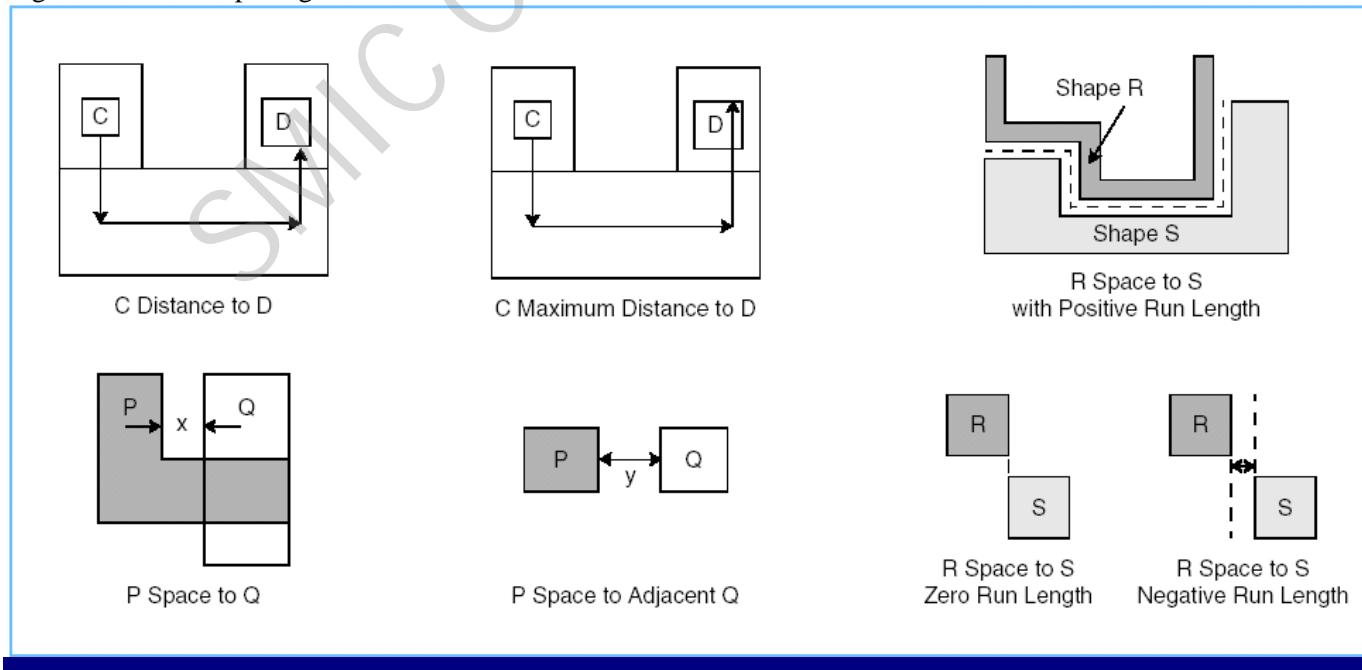
The shape A must be orthogonal	All edges of shapes on level A must be parallel to the X and Y axis
A must be orthogonal	All edges of shapes on level A must be parallel to the x and y axes.
A must be an orthogonal rectangle	Shape A is a rectangle with all edges parallel to the x and y axes. rectangle

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7.1.10.5 Spacing

C distance to D	The distance from any portion of C to the nearest edge or corner of D.
C maximum distance to D	The distance from any portion of C to the farthest edge or corner of D.
C space to D with abutting permitted when run length is $\geq n \mu m$	See “P space to Q”; zero spacing is permitted. Abutting of outside edges is permitted if the run length is greater than or equal to $n \mu m$.
P space to Q	Distance between all outside edges of shape P and outside edges of shape Q; abutting is prohibited. If P and/or Q are specified as an edge (gate side) instead of shapes, distance is checked with run length > 0 unless otherwise specified. Note: “Space to” does not prevent shapes P and Q from intersecting; “prohibited over” prevents this.
P space to adjacent Q	The distance between all outside edges of shapes on level P and outside edges of shapes on level Q. This distance is only checked between nonintersecting shapes on levels P and Q.
R space to S run length	The distance between two outside edges running in parallel; used for measuring the space between two parallel edges. This applies even if the shapes turn, as long as the minimum space between them does not effectively change. An “unbent common run” refers to the distance of run segments that do not turn. This syntax applies to one or two shapes only.

Figure 7.1.10.5-1 Spacing Definitions



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7.1.10.6 Overlap

J overlap past K	The spacing of all inside edges of shapes on level J to the outside edges of shapes on level K if the shapes intersect; coinciding of inside and outside edges is prohibited.
J overlap past K with coinciding permitted	See "J overlap past K" above; zero spacing (coinciding of inside and outside edges) is also permitted.
L overlap of M	The distance from all inside edges of shape L to the inside edges of M when L intersects M.
O Enclosure by P (P enclosure of O)	O enclosed by P: The layer O shape is completely within the layer P shape. The minimum distance from the outside edge of O to the inside edge of P in all directions.
R Extension outside of S	Layer R shape extends outside layer S shape in one direction, with no restriction on the other directions. The minimum distance from the outside edge of the layer S shape to the inside edge of the layer R shape.

Figure 7.1.10.6-1 Overlap Definitions

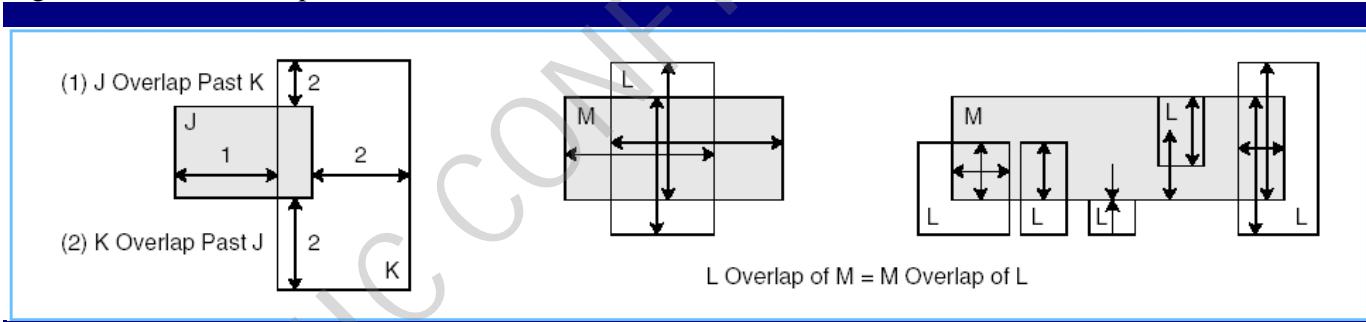
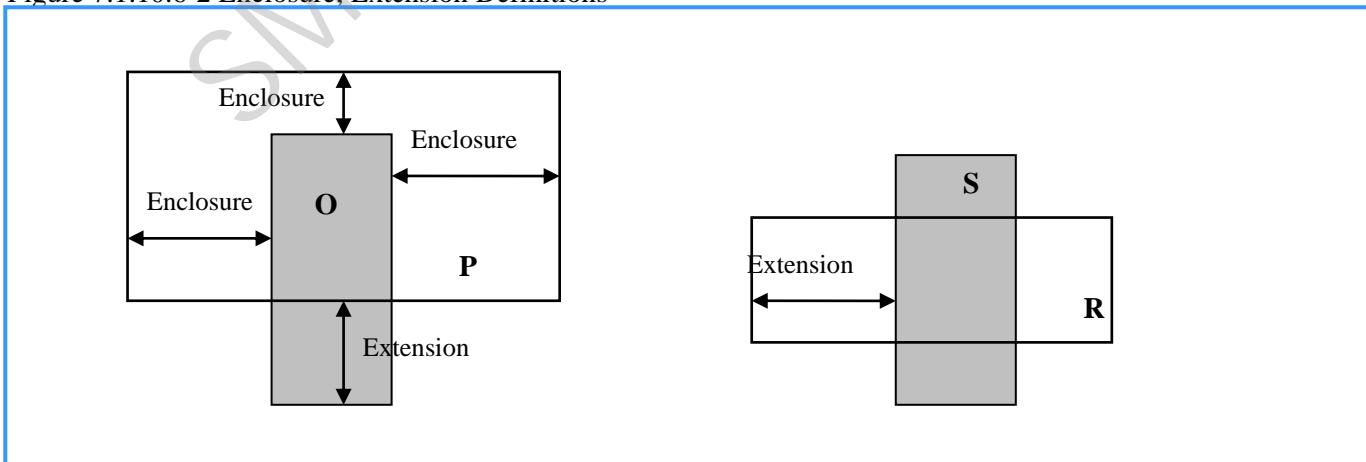


Figure 7.1.10.6-2 Enclosure, Extension Definitions

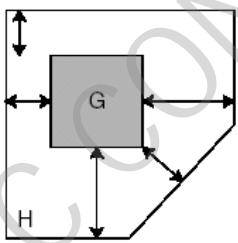


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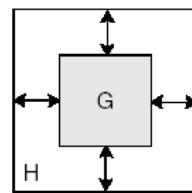
7.1.10.7 Containment

B must surround A	B does not touch A, but the enclosed area formed by B covers A.
G must be within H	All shapes on level G must be completely covered by shapes on level H. In addition, all outside facing edges of shapes on level G must have a minimum spacing greater than zero (unless the checked value is zero) to all inside facing edges of shapes on level H; G straddling H is prohibited. If G is specified as an edge (for example, the gate side) instead of shapes, distance is checked with run length > 0 unless otherwise specified.
G within H	Same as “G must be within H” if G can exist outside of H with straddling prohibited. If G is specified as an edge (gate side) instead of shapes, distance is checked with run length > 0 unless otherwise specified.
G within H with coinciding permitted	See “G within H” above; zero spacing (coinciding of inside and outside edges) is also permitted.
G minimum within H (rectangular enclosure)	See <i>Figure 7.1.10.7-1</i>

Figure 7.1.10.7-1 Containment Definitions



G Must Be Within H
G Within H



G Minimum Within H
(Rectangular Enclosure)

7.1.10.8 Conditions

C must abut D	Shapes on level C must abut shapes on level D. Abutting is defined as sharing the same edges without having a common area greater than zero.
C must touch D	Shapes on level C must intersect or abut shapes on level D. Shapes on level D are not required to touch shapes on level C.
C must not straddle D	Shapes on level C must be either completely inside or outside shapes on level D. Coincident edges are permitted.
C can only straddle D at 90°	Edges of shapes on level C can only intersect edges of shapes on level D at a 90 °angle.
C prohibited over D	Shapes on level C must not intersect shapes on level D. Abutting is permitted.
M must cover L	All vertices of shape L must be completely contained within the inside edges of shape M,

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	and every shape M must contain every shape L.
C outside D	C polygons with areas lie completely outside all D polygons. "C Abut D" is also treated as "outside". See Figure 7.1.10.8-2.
C not outside D	C polygons with areas intersect with D polygons, or completely inside D. See Figure 7.1.10.8-3.

Figure 7.1.10.8-1 Condition Definition

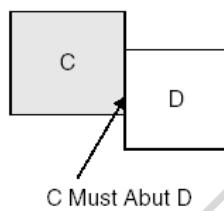


Figure 7.1.10.8-2 C outside D Definition

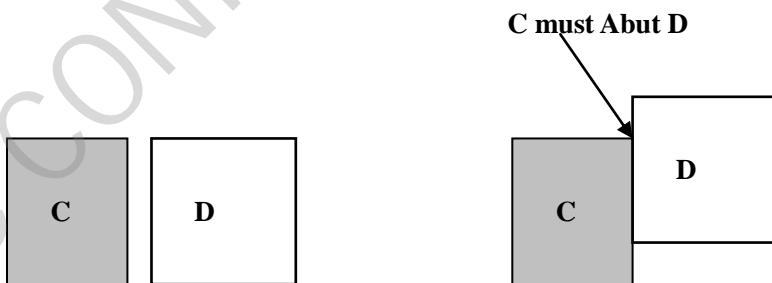
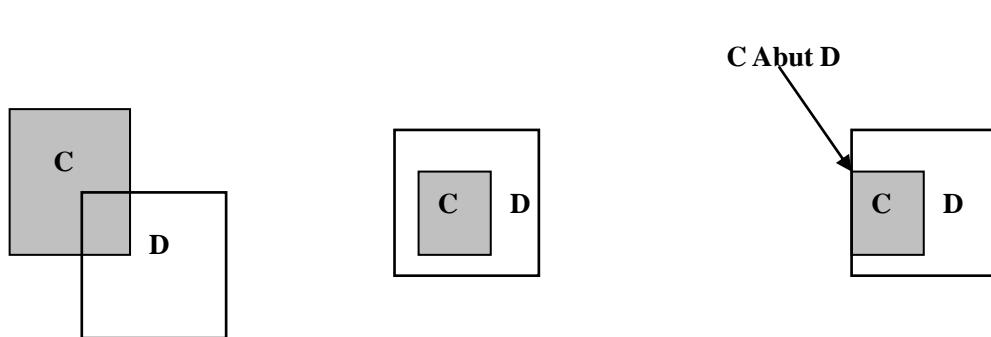


Figure 7.1.10.8-3 C not outside D Definition

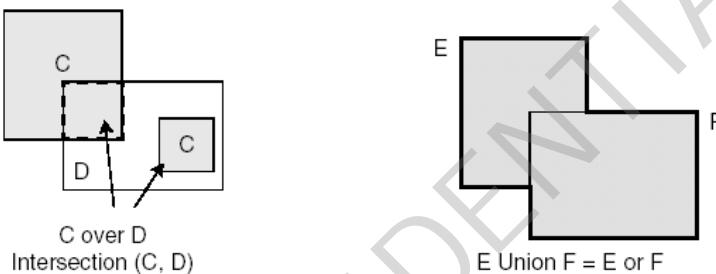


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7.1.10.9 Logical Function

C not D	The geometrical Boolean-logic “NOT” intersection of shapes on level C with the complement of shapes on level D. Same as difference (C, D).
C over D	The geometrical Boolean-logic “AND” intersection of shapes on level C and shapes on level D. Same as intersection (C, D), D under C, or (C and D).
E union F	The geometrical Boolean-logic “OR” union of shapes on level E and shapes on level F (see Figure 7.1.10.9-1).

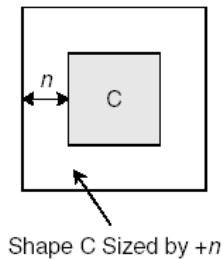
Figure 7.1.10.9-1 Logical Function Definitions



7.1.10.10 Sizing Function

C sized by n μm	All shapes on level C sized by n μm per edge, where n is either positive (expanded) or negative (shrunk).
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Figure 7.1.10.10-1 Sizing Function Definition

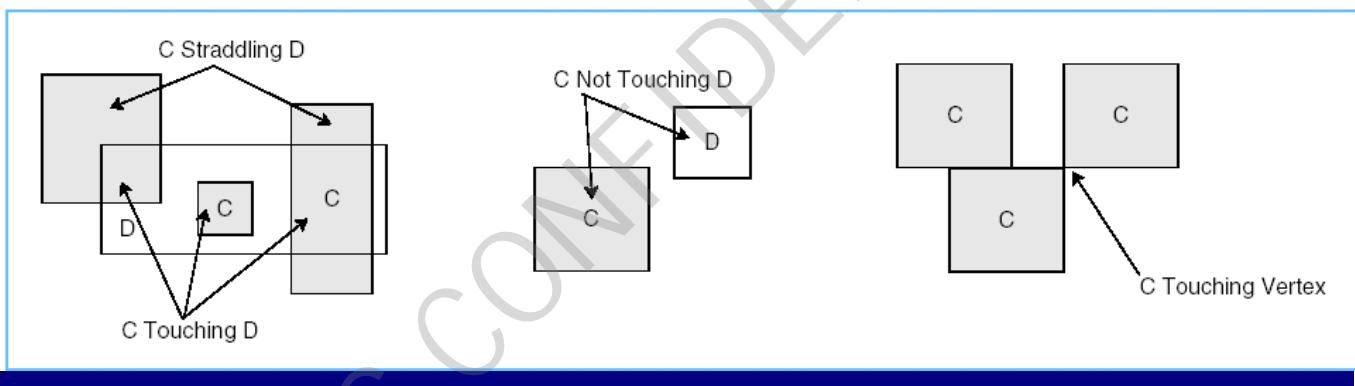


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7.1.10.11 Relational Selection Function

C coinciding with D	Shape C having inside or outside edges in common with shape D.
C incurring D	All shapes on level C that have a common area with any shapes on level D.
C straddling D	Shape C crossing the border of shape D. For example, “C straddling D” means that part of shape C overlaps D and part of shape C extends beyond the edge of D.
C touching D	All shapes on level C that are abutting or intersecting shapes on level D.
C not touching D	All shapes on level C that do not have a common area with any shapes on level D. Shapes on level C that have common edges with shapes on level D are not included in the result.
C touching vertex	Points where either two inside or two outside corners touch.

Figure 7.1.10.11-1 Relational Selection Function Definitions

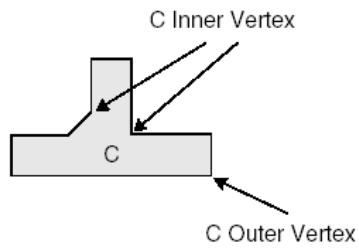


7.1.10.12 Geometrical Selection Function

A with width = n μm , A with width > n μm , A with width > n μm and $\leq m \mu\text{m}$	All shapes on level A that have widths in the valid range.
C vertex	The point at which shape edges on level C form an angle.
C inner vertex	All vertices that have angles greater than 180 ° when measured from inside the shape (concave). Same as inner corner.
C outer vertex	All vertices that have angles less than 180 ° when measured from inside the shape (convex). Same as outer corner.
C at 45 °	All shapes on level C that have edges at a 45 ° angle with respect to the x or y axis.

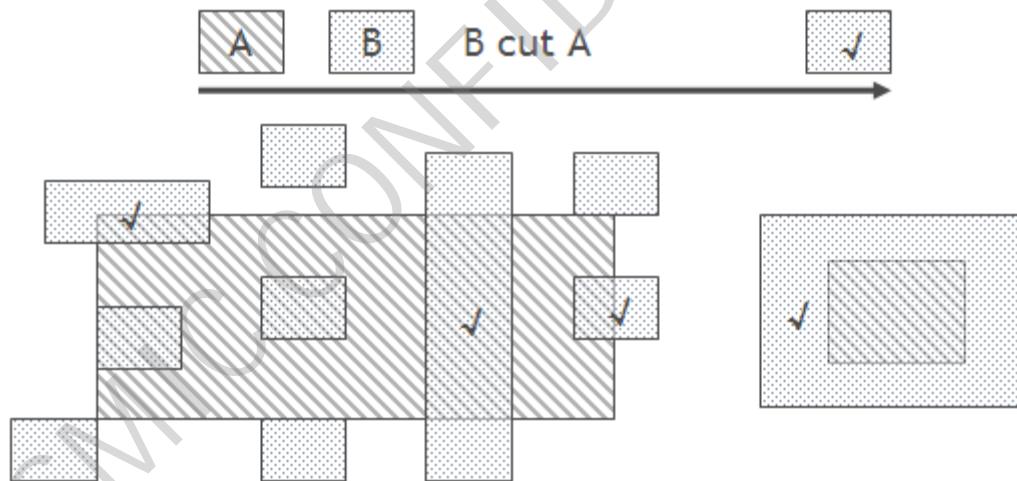
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Figure 7.1.10.12-1 Geometrical Selection Function Definitions



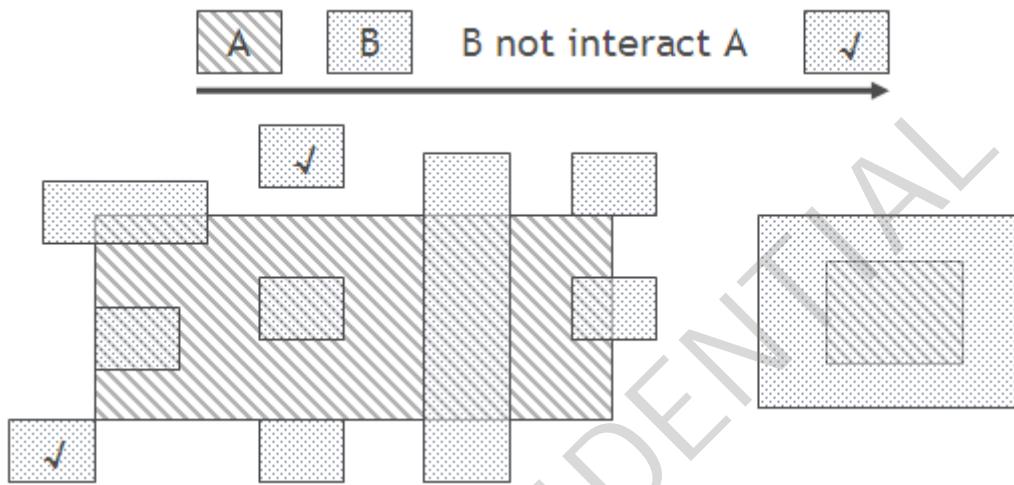
7.1.10.13 Cut definition:

- A cut B: A share part (not all) of area with B;
- B cut A: B share part (not all) of area with A.



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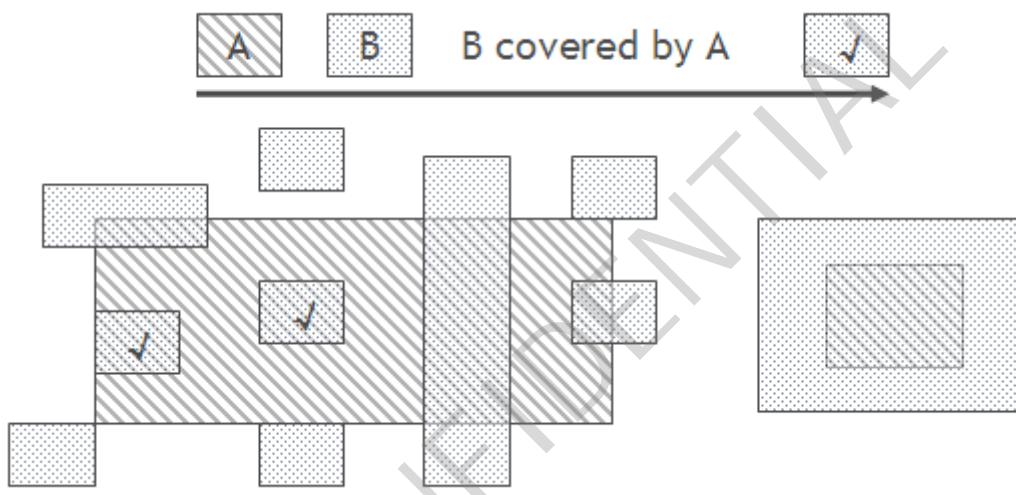
7.1.10.14 Not Interact definition:



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7.1.10.15 Cover definition:

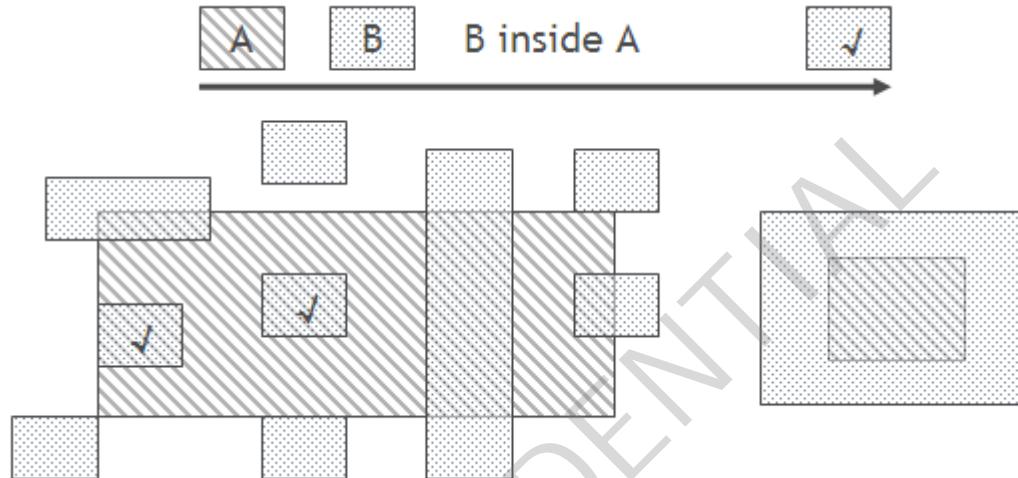
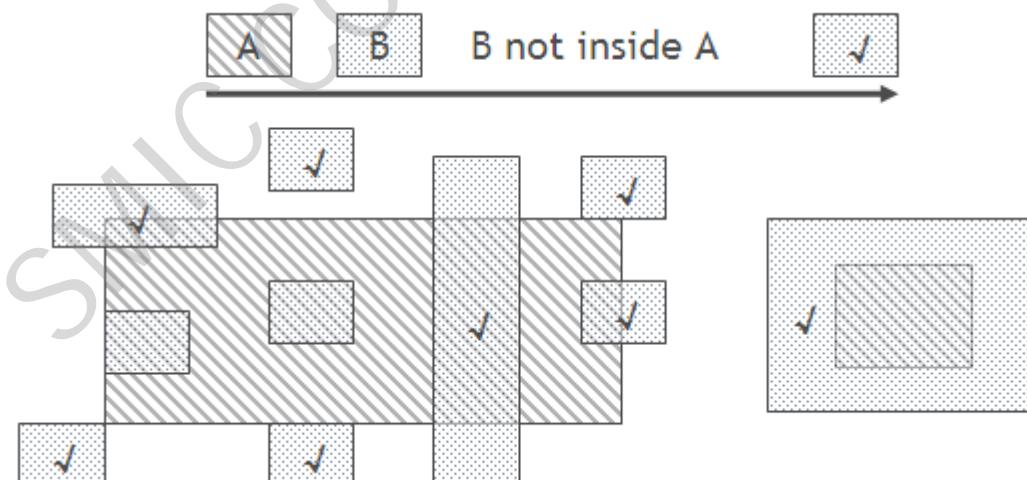
- A covered by B: A share all area with B;
- B covered by A: B share all area with A;



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7.1.10.16 Inside definition:

- A inside B (A covered by B): A share all area with B;
- B inside A (B covered by A): B share all area with A.

**7.1.10.17 Not inside definition:**



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7.1.11 DRC Connectivity Definition

1. Poly connectivity:
 - Interconnect non-resistor silicided poly, dummy poly is excluded
 - Interconnect poly = (GT NOT (SAB OR (RESP1 OR HRPDMY)))
2. NW and DNW connectivity:
 - NW interact with DNW
3. Pickup connectivity:
 - N+ pickup interact with NW; P+ pickup interact with (NOT NW)
 - N+ pickup butted P+ silicided S/D; P+ pickup butted N+ silicided S/D
4. BEOL connectivity:
 - Silicided S/D, interconnect poly, pickup connected with M1 by CT.
 - BEOL metal (NOT metal slot), via are defined as conducting layers by default, metal dummy is exclude
 - Metal resistors and inductors are treated as conducting metal

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7.2 Mask generation with GDS

7.2.1 40LL masks layers and their related GDS layers

This table content is based on 40LL LOTA table SMICLC40LL0. The masks listed are some generated masks that often reference.

Mask Code	Mask Name	Related GDS
120	AA	AA, LSRAM, 2PSRAM, RFSRAM, SN, NW, AADUM
292	DNW	DNW
192	NW	NW, TG, DG, RESAA, INST, LDBK
191	PW	NW, PSUB, TG, DG, RESAA, INST
492	NWH	NW,DG,RESAA
491	PWH	NW, PSUB, DG, RESAA
495	(purposely blank)	(purposely blank)
494	PWHT	NW, PSUB, TG, RESAA
146	(purposely blank)	(purposely blank)
145	TG	DG
131	DG	DG, TG
412	HR	SN, INST, NW, EFUSE
130	GT	GT, SDOP, LSRAM, 2PSRAM, RFSRAM, D2SRAM, 6TMK, GTDUM, OVERDR, SN, AA
214	NLHT	SN, NW, TG, RESP1, RESAA, PCAP, VARMOS, NLDB
215	PLHT	SP, NW, TG, RESP1, RESAA, NCAP, VARMOS, PLDB
114	NLH	SN, NW, DG, RESP1, RESAA, PCAP, VARMOS, NLDB
115	PLH	SP, NW, DG, RESP1, RESAA, NCAP, VARMOS, PLDB
194	PC	SP, NW, INST, HPBL
295	MVP	SP, NW, HPBL
193	NC	SN, NW, HPBL, INST
296	MVN	SN, NW, HPBL
595	LVP	SP, NW, LVT, PLDB
113	PLL	SP, NW, INST, DG, TG, RESP1, RESAA, NCAP, LVT, HVT, VARMOS, PLDB

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395	VTPH	SP, NW, HVT, PLDB
596	LVN	SN, NW, LVT, NLDB
116	NLL	SN, NW, INST, DG, TG, RESP1, RESAA, PCAP, LVT, HVT, VARMOS, NLDB
396	VTNH	SN, NW, HVT, NLDB
197	SP	INST, SP, NW
198	SN	SN, INST,NW
413	HRP	HRP
110	ESD1	ESD1
301	SM	NW, RESAA, PCAP, EFUSE, RESP1
155	SAB	SAB

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7.2.2 40LL GDS relation with mask layers

GDS no	Data type	GDS no; data type	GDS name	Related masks
10	0	10;0	AA	AA, GT
10	1	10;1	AADUM	AA
12	150	12;150	NLDB	NLL, NLH, NLHT, LVN, VTNH
13	150	13;150	PLDB	PLL, PLH, PLHT, LVP, VTPH
14	0	14;0	NW	AA, NW, NWH, PW, PWH, PWHT, HR, NC, PC, MVN, MVP, NLL, PLL, NLH, PLH, NLHT, PLHT, LVN, LVP, VTNH, VTPH, SM, SN, SP
19	0	19;0	DNW	DNW
29	0	29;0	DG	NW, PW, NWH, PWH, DG, TG, NLL, PLL, NLH, PLH
30	0	30;0	GT	GT
30	1	30;1	GTDUM	GT
39	0	39;0	HRP	HRP
40	0	40;0	SN	AA, GT, HR, NC, MVN, NLL, NLH, NLHT, LVN, VTNH, SN
41	0	41;0	ESD1	ESD1
43	0	43;0	SP	PC, MVP, PLL, PLH, PLHT, LVP, VTPH, SP
48	0	48;0	SAB	SAB
60	0	60;0	INST	NW, PW, HR, NC, PC, NLL, PLL, SN, SP
60	5	60;5	LRSRAM	AA, GT
60	9	60;9	RFSRAM	AA, GT
60	11	60;11	D2SRAM	GT
60	12	60;12	2PSRAM	AA, GT
60	150	60;150	HPBL	MVN, MVP, NC, PC
60	151	60;151	6TMK	GT
81	2	81;2	EFUSE	HR, SM
85	0	85;0	PSUB	PW, PWH, PWHT
93	0	93;0	VARMOS	NLL, PLL, NLH, PLH, NLHT, PLHT

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93	1	93;1	NCAP	PLL, PLH, PLHT
93	2	93;2	PCAP	NLL, NLH, NLHT, SM
96	0	96;0	RESP1	NLL, NLH, NLHT, PLL, PLH, PLHT, SM
97	0	97;0	RESAA	NW, NWH, PW, PWH, PWHT, NLL, NLH, NLHT, PLL, PLH, PLHT, SM
99	0	99;0	SDOP	GT
125	0	125;0	TG	NW, PW, PWHT, DG, NLL, PLL, NLHT, PLHT
125	3	125;3	OVERDR	GT
159	11	159;11	HVT	NLL, PLL, VTNH, VTPH
159	12	159;12	LVT	NLL, PLL, LVN, LVP
216	150	216;150	LDBK	NW

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7.2.3 Dummy layer mapping and mix signal related layer map table

Layer Name	GDSII No.	GDSII Data Type	Description
DUMBA	91	0	Dummy AA blockage
DUMBP	92	0	Dummy poly blockage
DUMBM	90	0	Dummy metal blockage
AADUM	10	1	AA Dummy Layer(For dummy AA insertion)
GTDUM	30	1	GT Dummy Layer(For dummy GT insertion)
TM1DUM	120	1	TM-1 Dummy Layer (For dummy metal insertion)
TM2DUM	122	1	TM2 Dummy Layer (For dummy metal insertion)
M8DUM	68	1	Metal-8 Dummy Layer (For dummy metal insertion)
M7DUM	67	1	Metal-7 Dummy Layer (For dummy metal insertion)
M6DUM	66	1	Metal-6 Dummy Layer (For dummy metal insertion)
M5DUM	65	1	Metal-5 Dummy Layer (For dummy metal insertion)
M4DUM	64	1	Metal-4 Dummy Layer (For dummy metal insertion)
M3DUM	63	1	Metal-3 Dummy Layer (For dummy metal insertion)
M2DUM	62	1	Metal-2 Dummy Layer (For dummy metal insertion)
M1DUM	61	1	Metal-1 Dummy Layer (For dummy metal insertion)
ALDUM	83	11	ALPA Dummy Layer
V1DUM	70	1	Via-1 Dummy Layer (For dummy via insertion)
V2DUM	71	1	Via-2 Dummy Layer (For dummy via insertion)
V3DUM	72	1	Via-3 Dummy Layer (For dummy via insertion)
V4DUM	73	1	Via-4 Dummy Layer (For dummy via insertion)
V5DUM	74	1	Via-5 Dummy Layer (For dummy via insertion)
V6DUM	75	1	Via-6 Dummy Layer (For dummy via insertion)
V7DUM	76	1	Via-7 Dummy Layer (For dummy via insertion)
M1DUB	151	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M1FILL shapes.
M2DUB	152	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M2FILL shapes.



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Layer Name	GDSII No.	GDSII Data Type	Description
M3DUB	153	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M3FILL shapes.
M4DUB	154	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M4FILL shapes.
M5DUB	155	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M5FILL shapes.
M6DUB	156	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M6FILL shapes.
M7DUB	157	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M7FILL shapes.
M8DUB	158	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of M8FILL shapes.
TM1DUB	193	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of TM1FILL shapes.
TM2DUB	194	1	Optional level placed over specific areas of the chip at the customer's discretion to prevent the generation of TM2FILL shapes.
V1DUB	70	6	Via-1 Dummy Blockage.
V2DUB	71	6	Via-2 Dummy Blockage.
V3DUB	72	6	Via-3 Dummy Blockage.
V4DUB	73	6	Via-4 Dummy Blockage.
V5DUB	74	6	Via-5 Dummy Blockage.
V6DUB	75	6	Via-6 Dummy Blockage.
V7DUB	76	6	Via-7 Dummy Blockage.
ALDUB	83	6	ALPA Dummy Blockage.
PTCT	159	7	Used during the automatic kerf merge process during mask assembly of CP masks; associated with preventing mask back-ground overwrite.
(blank)	10	7	(blank)
(blank)	30	7	(blank)
M1DOP	61	7	M1 dummy data type 7
V1DOP	70	7	V1 dummy data type 7

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Layer Name	GDSII No.	GDSII Data Type	Description
M2DOP	62	7	M2 dummy data type 7
V2DOP	71	7	V2 dummy data type 7
M3DOP	63	7	M3 dummy data type 7
V3DOP	72	7	V3 dummy data type 7
M4DOP	64	7	M4 dummy data type 7
V4DOP	73	7	V4 dummy data type 7
M5DOP	65	7	M5 dummy data type 7
V5DOP	74	7	V5 dummy data type 7
M6DOP	66	7	M6 dummy data type 7
V6DOP	75	7	V6 dummy data type 7
M7DOP	67	7	M7 dummy data type 7
V7DOP	76	7	V7 dummy data type 7
M8DOP	68	7	M8 dummy data type 7
MTT2DM	231	1	MTT2(UTM) dummy
MTT2DB	194	2	MTT2(UTM) dummy blockage mark layer
V1RM	70	10	V1 mark layer to identify redundant via
V2RM	71	10	V2 mark layer to identify redundant via
V3RM	72	10	V3 mark layer to identify redundant via
V4RM	73	10	V4 mark layer to identify redundant via
V5RM	74	10	V5 mark layer to identify redundant via
V6RM	75	10	V6 mark layer to identify redundant via
V7RM	76	10	V7 mark layer to identify redundant via
TV1RM	121	10	TV1 mark layer to identify redundant via
TV2RM	123	10	TV2 mark layer to identify redundant via

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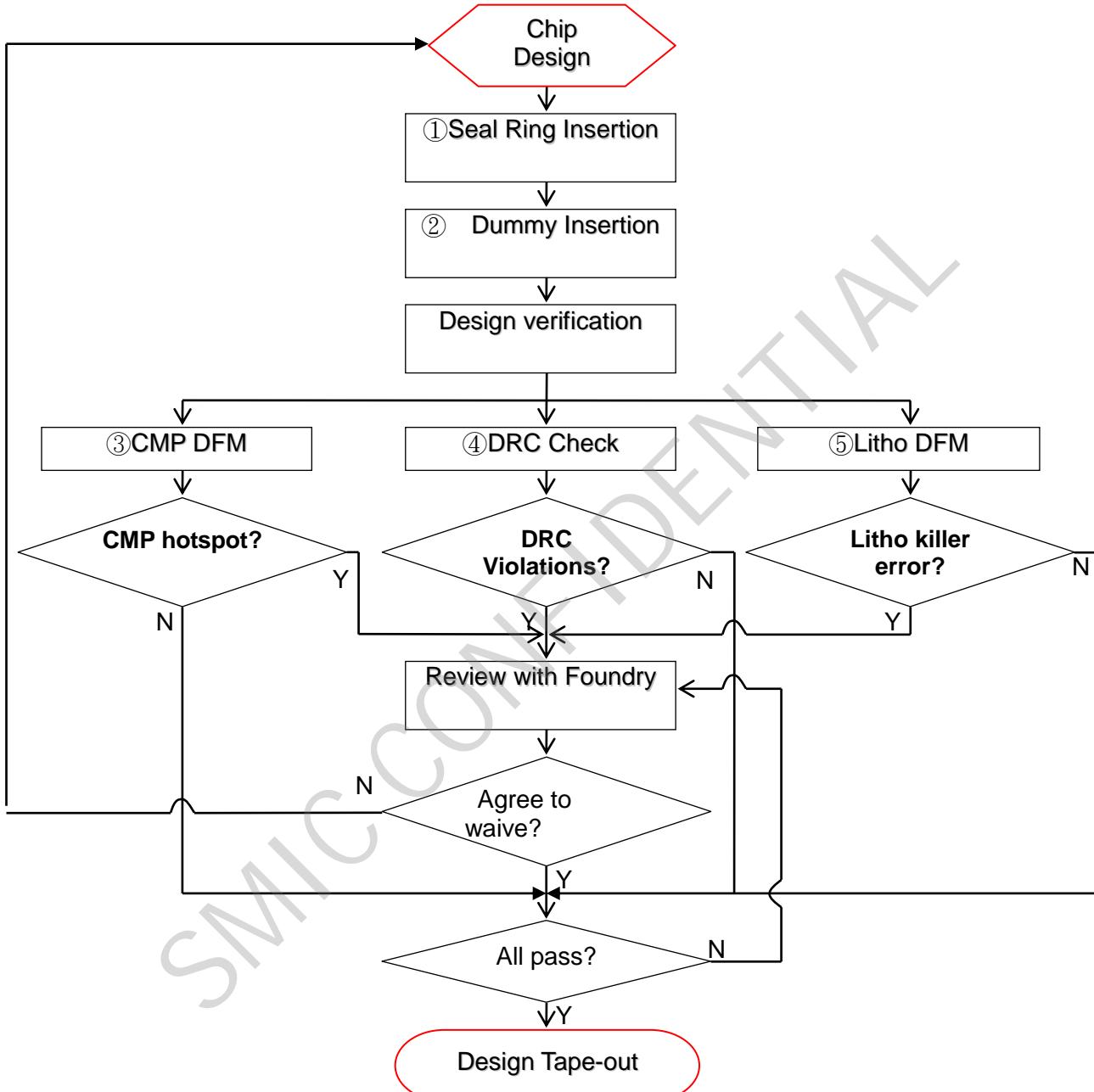


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Layer Name	GDSII No.	GDSII Data Type	Description
V1RB	70	8	V1 redundant via insertion blockage
V2RB	71	8	V2 redundant via insertion blockage
V3RB	72	8	V3 redundant via insertion blockage
V4RB	73	8	V4 redundant via insertion blockage
V5RB	74	8	V5 redundant via insertion blockage
V6RB	75	8	V6 redundant via insertion blockage
V7RB	76	8	V7 redundant via insertion blockage
TV1RB	121	8	TV1 redundant via insertion blockage
TV2RB	123	8	TV2 redundant via insertion blockage

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7.3 Design check Flow before tape out



Notes:

1. Designer must clean DRC and DFM litho killer errors before tape-out. Non-cleans can not be waived unless SMIC does so after reviews.
2. Recommend designers to do dummy insertions (Step ②) before DRC and DFM check. Without dummy inserted, design verification, CMP DFM, and DRC results related to dummy patterns will not be accurate.
3. Recommend designers to do the steps of ③, ④ and ⑤ by themselves. SMIC can help to do the work before tape out if designers have concerns or difficulties.

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7.4 Layout Rule Description

7.4.1 AA: Active Area Rules

Rule number	Description	Operation	Design Value	Unit
AA.1	AA width (The INST connected area apply SRAM design rule)	\geq	0.06	μm
AA.1a	AA width of NMOS/PMOS for 0.9/1.1/1.2V transistor	\geq	0.12	μm
AA.1b^[R]	(purposely blank)			
AA.2	AA (enclosure by TG or DG) width for 1.8/2.5V transistor	\geq	0.32	μm
AA.3	(purposely blank)	\geq		μm
AA.4a	AA space	\geq	0.08	μm
AA.4b	The space between two AA with gate along source/drain direction, if one of AA width (W2) $\geq 0.14 \mu\text{m}$, and AA to AA run length $Y1 \geq 0.14 \mu\text{m}$	\geq	0.1	μm
AA.4c	The space between two AA with gate along gate poly direction, if one of AA width (W3) $\geq 0.14 \mu\text{m}$, and AA to AA run length $Y2 \geq 0.14 \mu\text{m}$	\geq	0.1	μm
AA.4d	Space between two AAs inside (DG OR TG)	\geq	0.13	μm
AA.4e^[R]	Space between (AA or AADUM) DRC check maximum STI width. DRC don't check: chip corner DUMBA region as defined in rule CORN.2 if seal ring is added by SMIC.	\leq	10	μm
AA.5	(purposely blank)			
AA.6	(purposely blank)			
AA.7	(purposely blank)			
AA.8	(purposely blank)			
AA.9	AA area except floating AA. (The INST connected area apply SRAM design rule)	\geq	0.02	μm^2
AA.9a	AA area at floating AA(The INST connected area apply SRAM design rule)	\geq	0.015	μm^2
AA.10^[R]	DG, TG or core transistors mixed in the same AA are prohibited			
AA.11	It is not allowed to draw AA straddle on boundary of NW (exclude LDMOS area, the AA within LDBK layer; waive the AA interact with RESNW)			
AA.12^[R]	AA channel width of NMOS/PMOS for 0.9/1.1/1.2V transistor. Waive transistor inside VARMOS	\leq	50	μm
AA.13	AA enclosed area	\geq	0.0395	μm^2
AA.13a^[R]	Enclosed area when AA all of inner edge length $< 0.21 \mu\text{m}$.	\geq	0.077	μm^2

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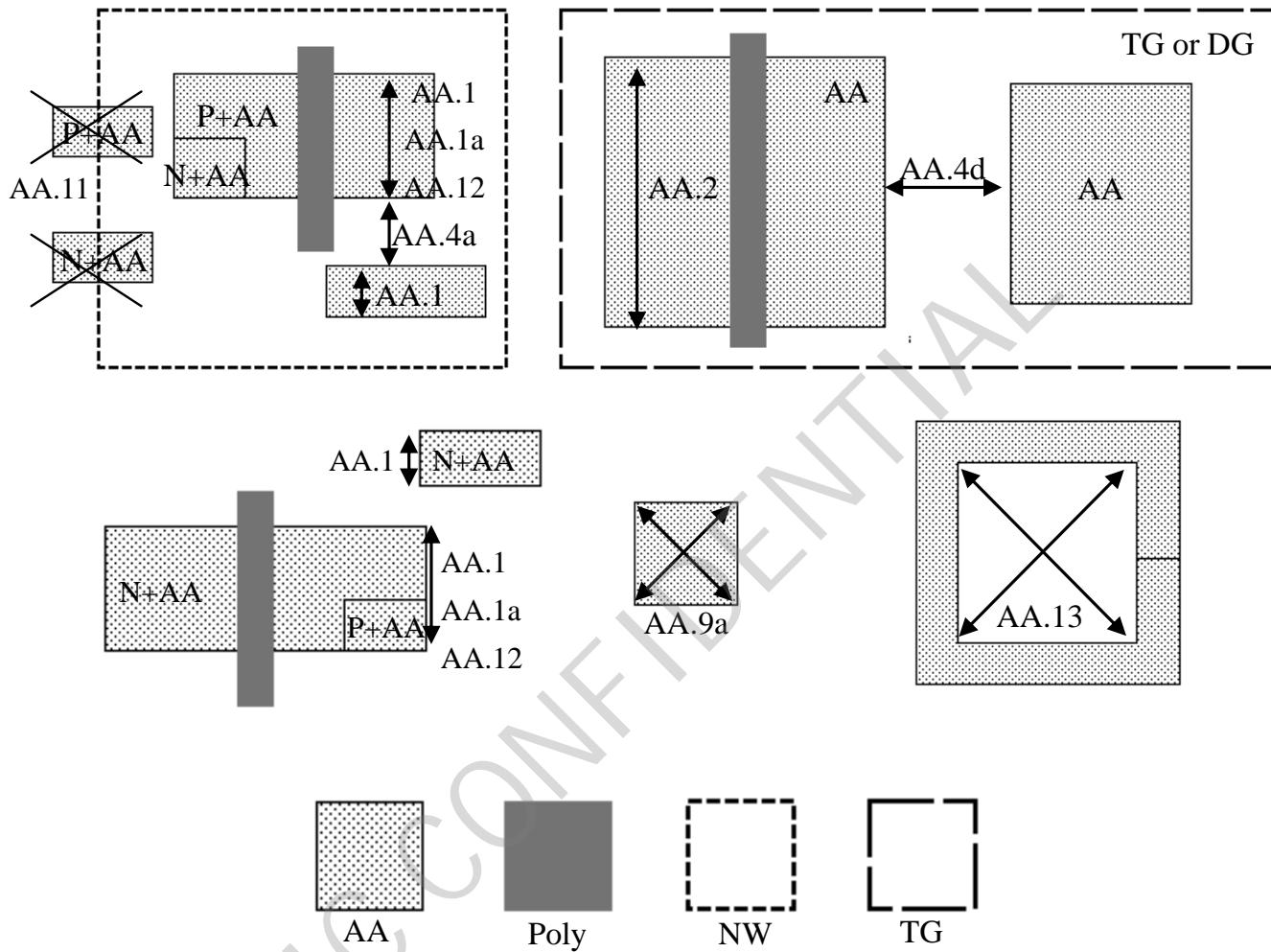
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Rule number	Description	Operation	Design Value	Unit
	This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM OR RFSRAM) covered region.			
AA.14	For area excluding (DG or TG), AA density (including dummy). Density check window size: 200 μm *200 μm with step size: 100 μm . Waive RESNW, LOGO, seal ring(MARKS) areas DRC check with the said window size and rule number and highlight as X. $Y = X$ not (DG or TG), $Z = (Y \text{ area})/(100*100)$ If $Z > 25\%$, highlight Y for AA density inside of Y that cannot meet of rule value requirement.	\geq	20%	
		\leq	82%	
AA.14a	For area in of (DG or TG), AA density (including dummy). Density check window size: 200 μm *200 μm with step size 100 μm DRC check with the said window size and rule number and highlight as X. $Y = X$ and (DG or TG), $Z = (Y \text{ area})/(100*100)$ If $Z > 25\%$, highlight Y for AA density inside of Y outside of rule value requirement	\geq	20%	
		\leq	90%	
AA.15 ^[R]	AA density overlap by DUMBA. Density check window size 200 μm *200 μm with step size 100 μm	\geq	20%	
		\leq	80%	
AA.16	Bent 45 degree AA width	\geq	0.16	μm
AA.17	45 degree AA space to parallel AA	\geq	0.16	μm
AA.18	AA space of U shape (notch) (outside of SRAM) Waive for extrusion E ≤ 0.03 , or U shape bottom AA width W0 $> 0.08 \mu\text{m}$	\geq	0.15	μm
AA.19	AA must be fully covered by (SN OR SP). Waive the violations in AA interact RESNW, LOGO, OCOVL region.			
AA.20	Maximum length of (AA NOT pickup AA) when AA width $< 0.12 \mu\text{m}$ and butted with pickup AA	\leq	0.4	μm
AA.21	Maximum AA length between two contacts, or between one contact and AA line end when AA width $< 0.12 \mu\text{m}$	\leq	60	μm
AA.22	AA density over the whole chip	\geq	25%	
		\leq	75%	
AA.23 ^[R]	For any geometry on AA, NW, GT, M1, or Mn (n=2~8), an edge of length $< 1.0 \times W_{\min}$ cannot have any adjacent edge with length $< 1.0 \times W_{\min}$			

Note:

For AA.4a, the shape cross areas with sharp angle are not applicable for this space rule. It is depicted in Fig. 7.4.1-3.

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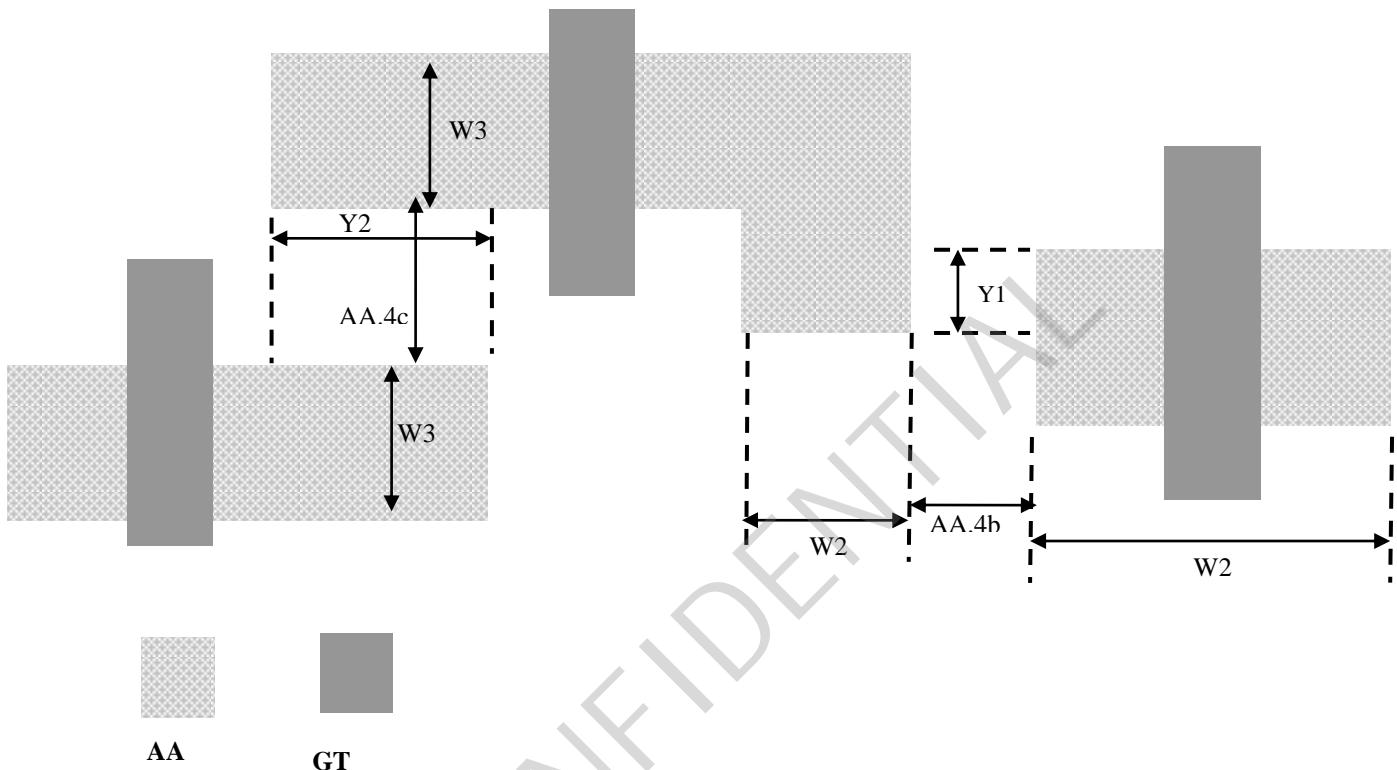


Fig. 7.4.1-2

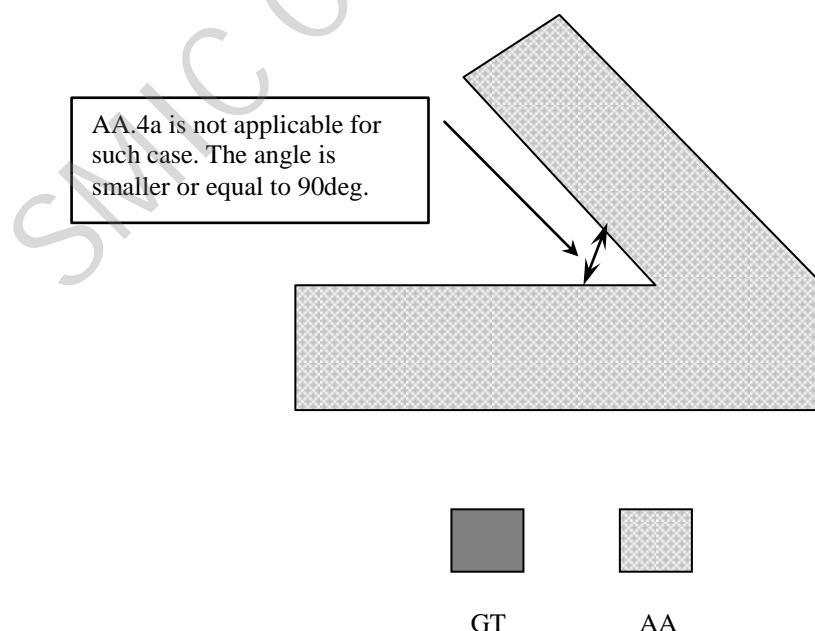


Fig. 7.4.1-3

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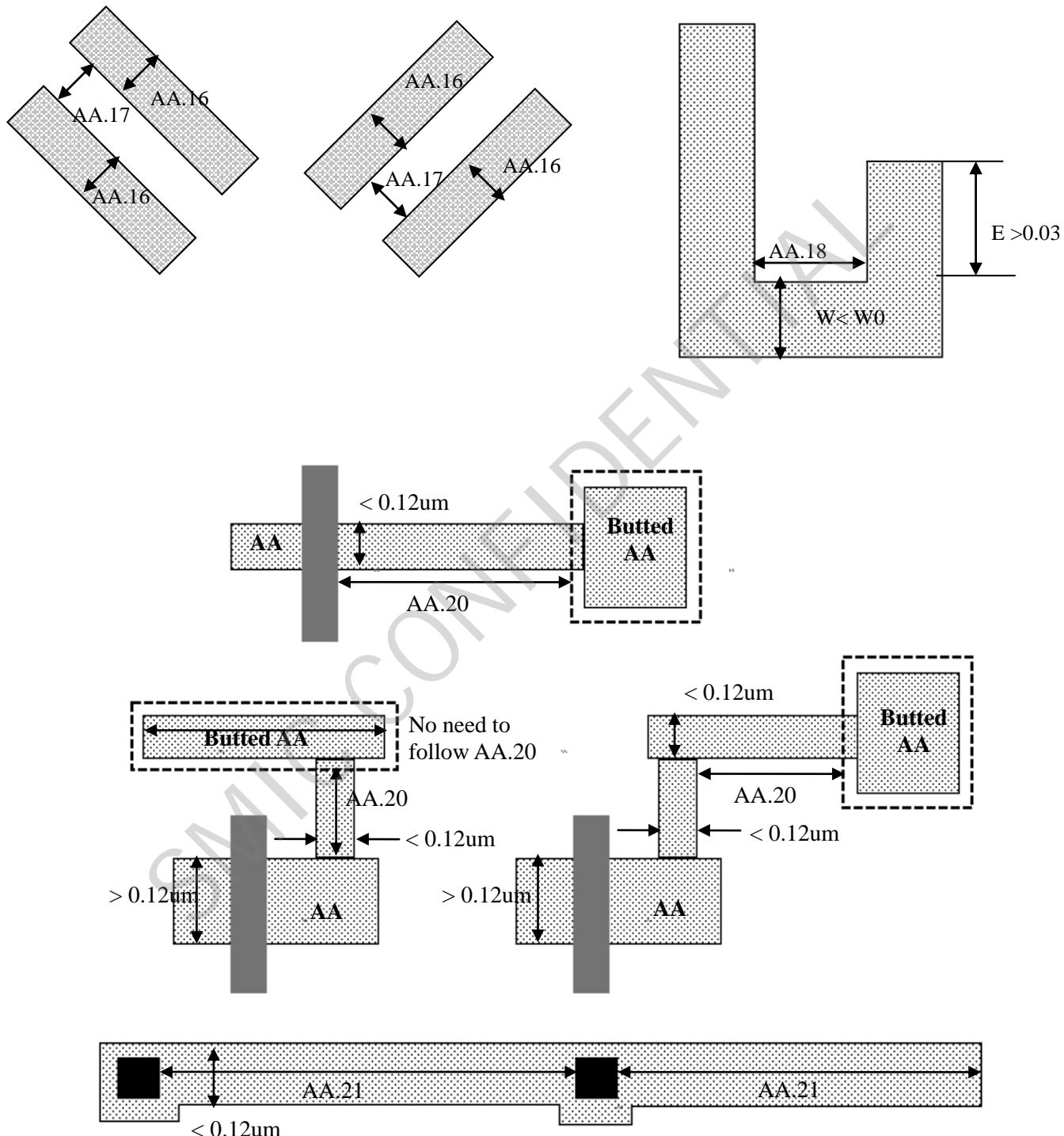


Fig. 7.4.1-4

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7.4.1.1 AA Resistor Rules (AA resistor block layer RESAA)

AA resistor means AA within RESAA overlap SAB region.

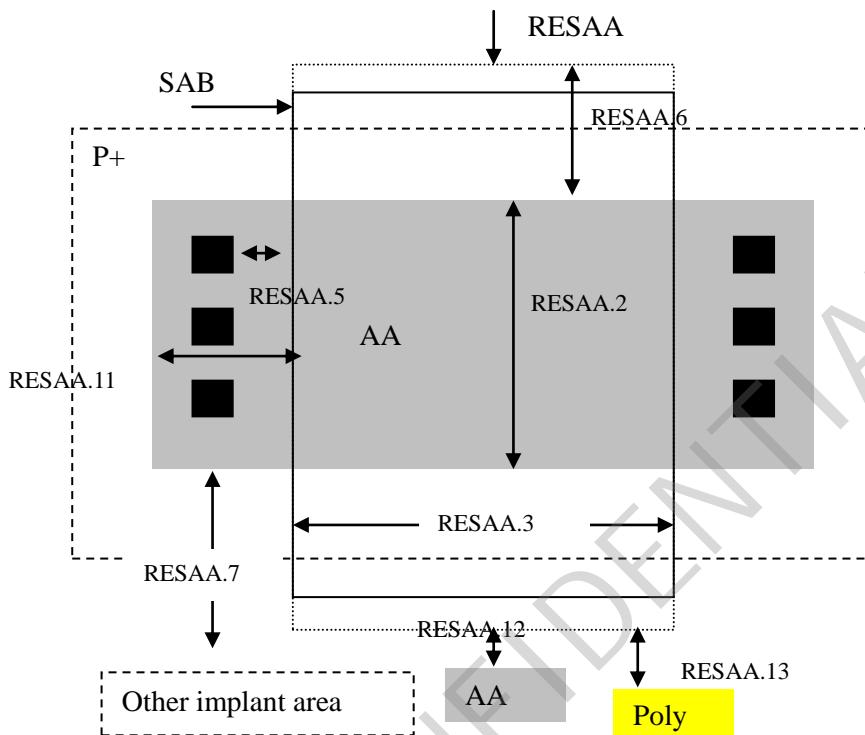
AA resistor = AA AND RESAA

Rule number	Description	Operation	Design Value	Unit
RESAA.1^[NC]	AA resistor must be within RESAA layer			
RESAA.2	AA resistor width	\geq	0.4	μm
RESAA.2a^[R]	(purposely blank)			
RESAA.3	AA resistor length	\geq	0.400	μm
RESAA.3a^[R]	(purposely blank)			
RESAA.4	AA resistor must be orthogonal			
RESAA.5	CT to SAB space	\geq	0.18	μm
RESAA.6	Extension of RESAA outside of AA	\geq	0.15	μm
RESAA.7	The separation between resistors with un-related implant region Un-related implant region: NW, LVT, HVT, SN, SP, ESD1. These regions don't interact with resistors.	\geq	0.16	μm
RESAA.8	(purposely blank)			
RESAA.9	For AA resistor, make sure the AA be covered by SAB and implanted by either SN or SP.			
RESAA.10	AA SAB resistor with SP must lay on NW			
RESAA.11	(purposely blank)	\geq	0.4	μm
RESAA.12	Space RESAA to non-related AA	\geq	0.08	μm
RESAA.13	Space RESAA to non-related Poly	\geq	0.08	μm
RESAA.14	RESAA and SAB on AA should have coincident edge			

Note:

- Dog-bone design at the end of AA resistor for contact pick-up is not suggested

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7.4.1.2 AA Density design rules

Rule number	Description	Operation	Design Value	Unit
AA.C.1	Containing rectangle of HDA	\leq	250*250	μm
AA.C.2	(purposely blank)			
AA.C.3	Containing rectangle of LDA	\leq	50*50	μm
AA.C.4	Containing rectangle of MDA	\leq	125*125	μm
AA.C.5 ^[R]	Space between Real Gate and minimum 50*50um LDA Waive if the gate channel length $\geq 0.06 \mu\text{m}$	\geq	20	μm

Note:

1. HDA is defined as regions with the AA pattern density over 85% after insertion of dummy AA, which is generated by checking **250 μm *250 μm** blocks, beginning at the origin and stepping by 25 μm after each check until the design has been checked. If the density of AA within the **250 μm *250 μm** area is above 85%, it is called HDA.
2. LDA is defined as regions with the AA pattern density less than 10% after insertion of dummy AA, which is generated by checking 25 μm *25 μm blocks, beginning at the origin and stepping by 25 μm after each check until the design has been checked. If the density of AA within the 25 μm *25 μm area is below 10%, it is called LDA.
3. MDA is defined as regions with the AA pattern density less than **20%** after insertion of dummy AA, which is generated by checking 25 μm *25 μm blocks, beginning at the origin and stepping by 25 μm after each check until the design has been checked. If the density of AA within the 25 μm *25 μm area is below **20%**, it is called MDA.

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7.4.1.3 AA Silicide Resistor Rules

AA Silicide resistor mark layer is DIFRES.

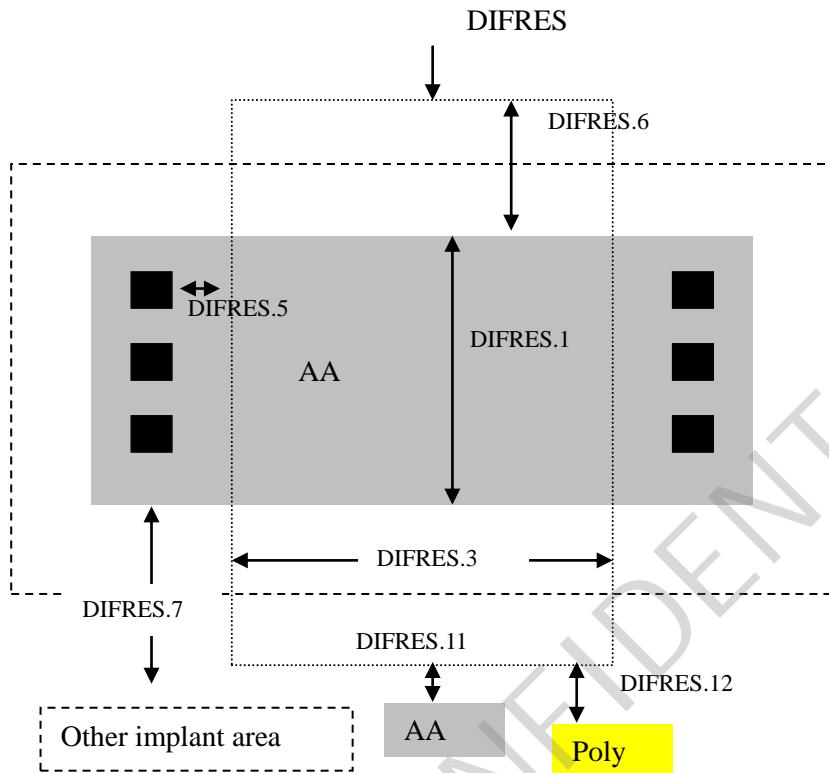
AA Silicide resistor: (AA AND DIFRES)

RULE NO.	DESCRIPTION	Operation	Design Value	Unit
DIFRES.1	AA Silicide resistor width	\geq	0.2	μm
DIFRES.2	DIFRES can not overlap with RESAA			
DIFRES.3	AA Silicide resistor square number	\geq	1	
DIFRES.4	AA Silicide resistor must be orthogonal			
DIFRES.5	CT to DIFRES space	$=$	0.01	μm
DIFRES.6	Extension of DIFRES outside of AA	\geq	0	μm
DIFRES.7	The separation between AA resistors and un-related implant region Un-related implant region: NW, LVT, HVT, SN, SP, ESD1. These regions don't interact with resistors.	\geq	0.16	μm
DIFRES.8	For AA Silicide resistor, make sure the AA be implanted by either SN or SP. Minimum enclosure by (SN or SP)	\geq	0.18	μm
DIFRES.9	AA Silicide resistor with SP must lay on NW			
DIFRES.10	AA Silicide resistor with SN must lay on PW			
DIFRES.11	Space between DIFRES and non-related AA	\geq	0.08	μm
DIFRES.12	Space between DIFRES and non-related Poly	\geq	0.08	μm

Note:

1. Dog-bone design at the end of AA resistor for contact pick-up is not suggested.

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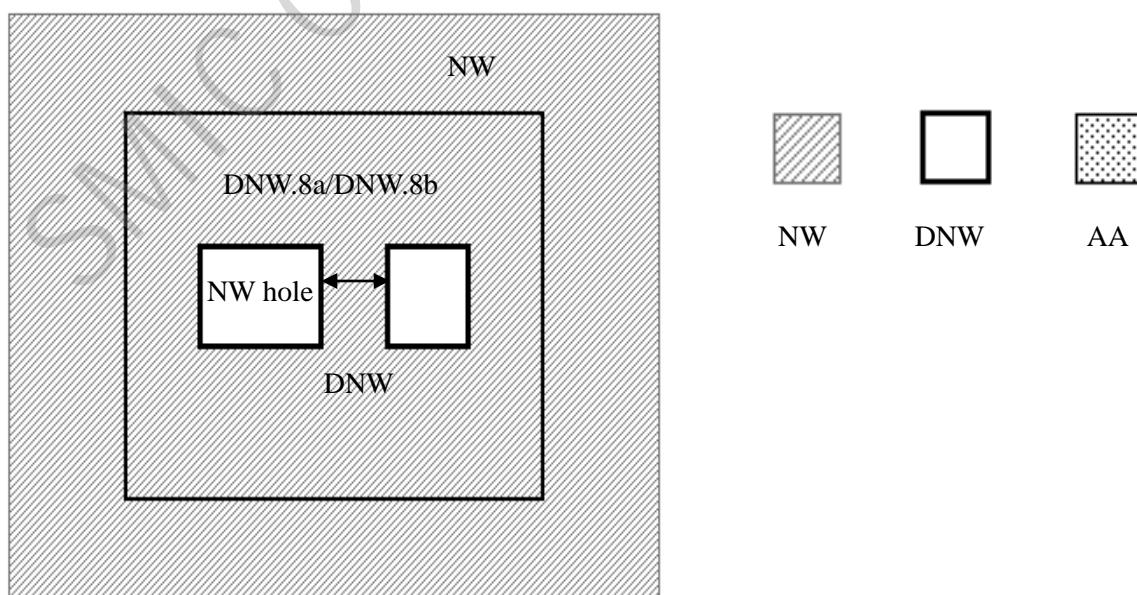
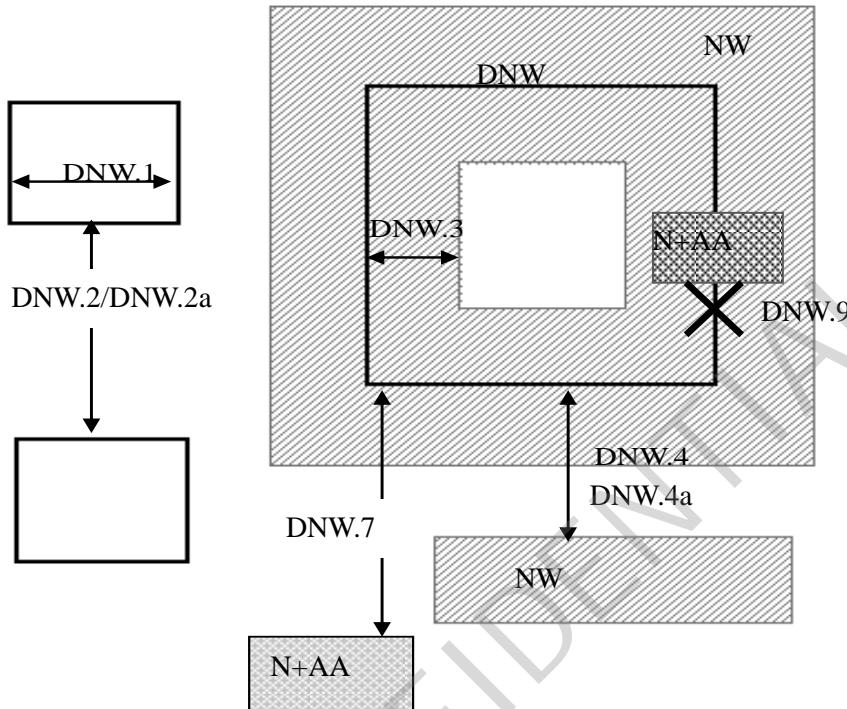


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7.4.2 DNW Design Rules

Rule number	Description	Operation	Design Value	Unit
DNW.1	DNW width	\geq	0.520	μm
DNW.2	Space between two DNW regions	\geq	0.8	μm
DNW.2a	Space between two DNW regions at different net	\geq	1.8	μm
DNW.3	Overlap of NW and DNW region.	\geq	0	μm
DNW.4	Space between a DNW and a NW	\geq	0.565	μm
DNW.4a	Space between a DNW and a NW at different net	\geq	1.5	μm
DNW.5	(Purposely blank)			
DNW.6	(Purposely blank)			
DNW.7	Space between DNW and N+AA outside of DNW	\geq	1.4	μm
DNW.8	Space between (NW hole INSIDE DNW) and ((NW hole INSIDE DNW) or ((PW NOT DNW) at different nets.	\geq	0.6	μm
DNW.9	It is not allowed that N+AA CUT DNW			

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7.4.3 NW: N-Well Implant Layer Rules

Rule number	Description	Operation	Design Value	Unit
NW.1	NW width. (parallel side to side width. The INST connected area apply SRAM design rule)	\geq	0.330	μm
NW.1a	NW width for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) connected area.	\geq	0.27	μm
NW.2	(purposely blank)			
NW.3	Space between two NW regions of the same net. (with run length > 0, skip to check jog $\leq 0.005\mu\text{m}$ pattern)	\geq	0.330	μm
NW.4	Space between two NW regions of different net.	\geq	0.600	μm
NW.5	(purposely blank)			
NW.6	(purposely blank)			
NW.7	NW area	\geq	0.64	μm^2
NW.8	NW enclosed area	\geq	0.7	μm^2
NW.9	NW space to N+AA (enclosure by TG or DG)	\geq	0.22	μm
NW.10	NW enclosure of P+AA (enclosed by TG or DG)	\geq	0.22	μm
NW.11^[R]	N+AA adjacent both two edges space opposite to NW. Both of two adjacent edges space to NW smaller than rule value is not permitted. In schematic rule check method, E = 0.08, D=0.16	\geq	0.16	μm
NW.12^[R]	NW enclosure opposite of P+AA adjacent both two edges. Both of two adjacent edges enclosed by NW smaller than rule value is not permitted. In schematic rule check method, E = 0.08, D=0.16 This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region.	\geq	0.16	μm
NW.13	N+ AA enclosure by NW. Exclude LDMOS region (within LDBK). Waive ((AA interact RESNW) and SN)	\geq	0.08	μm
NW.14	Space between NW and N+AA	\geq	0.08	μm
NW.15	P+AA enclosure by NW. Exclude LDMOS region(within LDBK)	\geq	0.08	μm
NW.16	Space between NW and P+AA inside PW. Exclude LDMOS region(within LDBK)	\geq	0.08	μm

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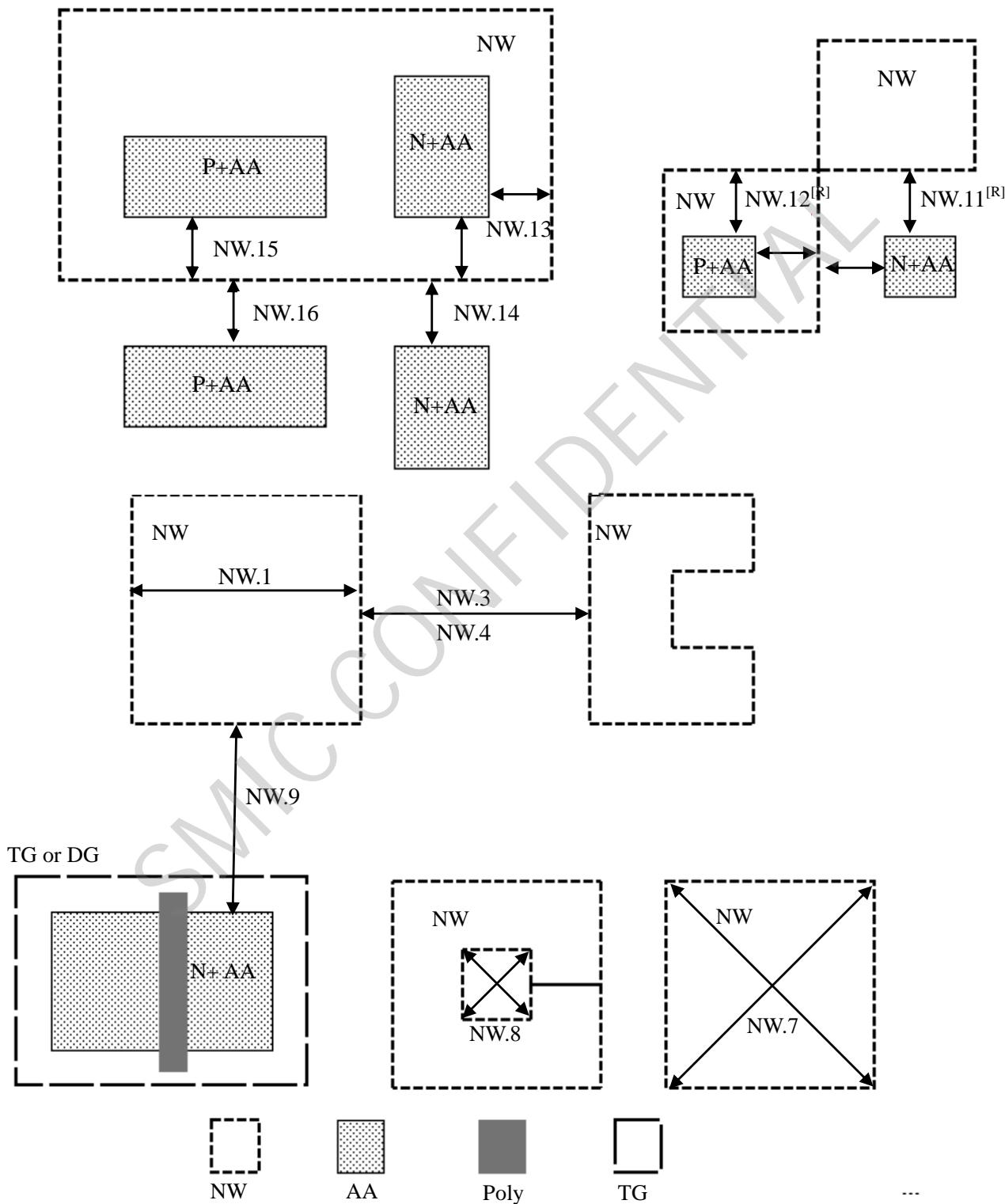
Semiconductor Manufacturing International Corporation

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NW.17 ^[R]	For parallel long NW (length > 50 μm), must make NW width larger than 0.89 μm or NW to NW space larger than 0.89 μm. If this area passed AA density DRC check, this rule can be waived. This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM OR RFSRAM covered region.	≥	0.89	μm
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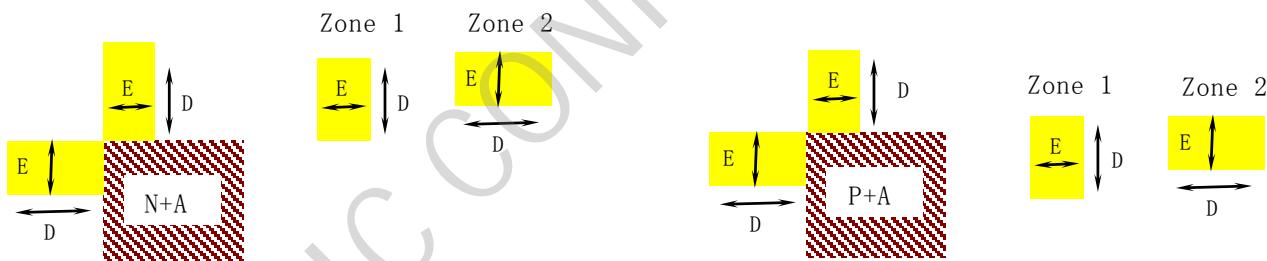
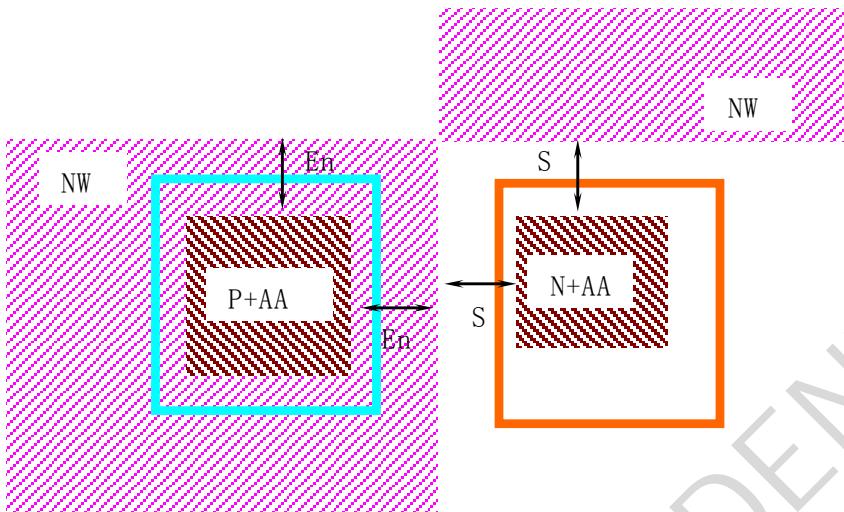
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NW. 11, NW. 12



NW.11 check method:

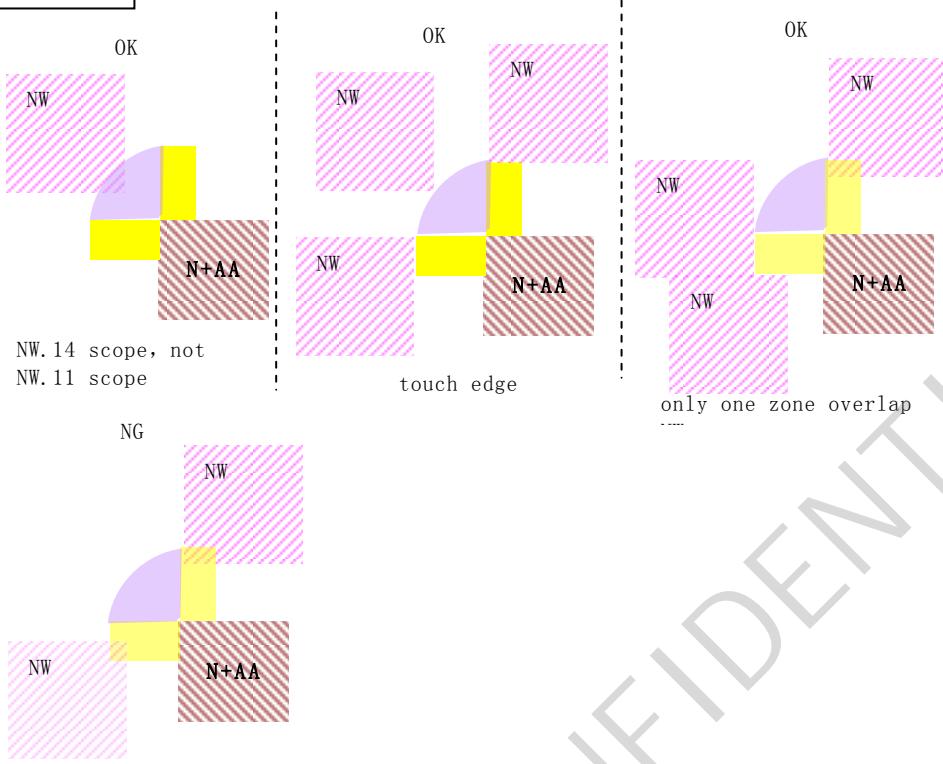
Zone 1 and Zone 2 are started from the outer vertex of N+AA. Zone 1 and Zone 2 should not overlap with NW simultaneously. Touch edge is not overlap.

NW.12 check method:

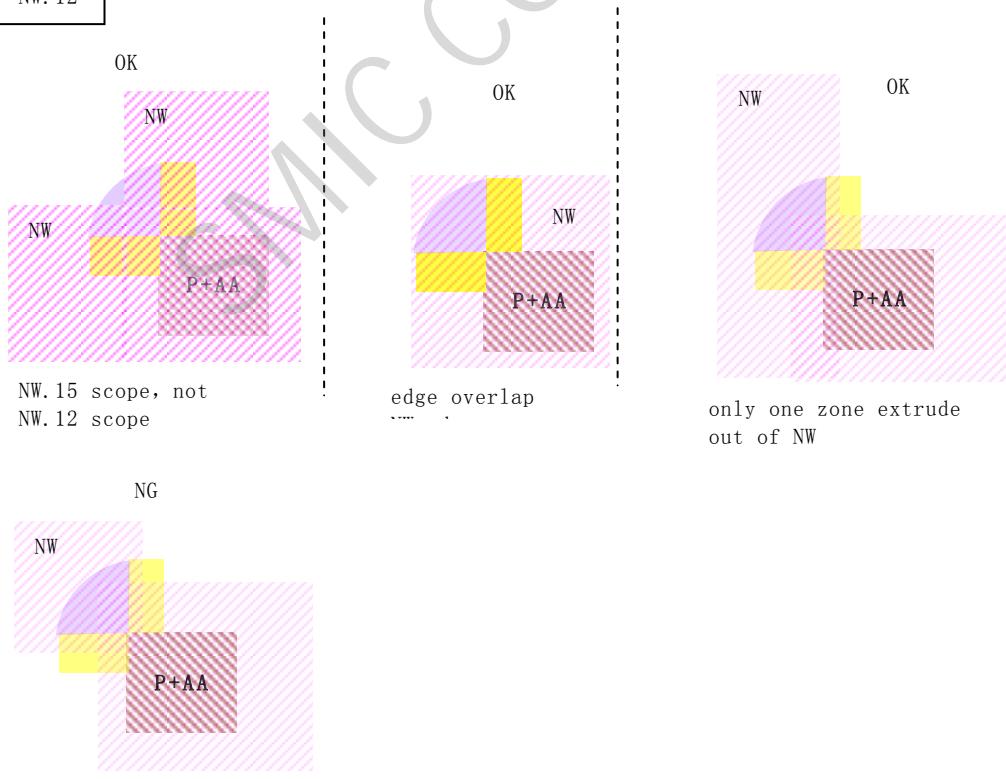
Zone 1 and Zone 2 are started from the outer vertex of P+AA. Zone 1 and Zone 2 should not extrude out of NW simultaneously. Touch NW edge is not extrude out.

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NW. 11

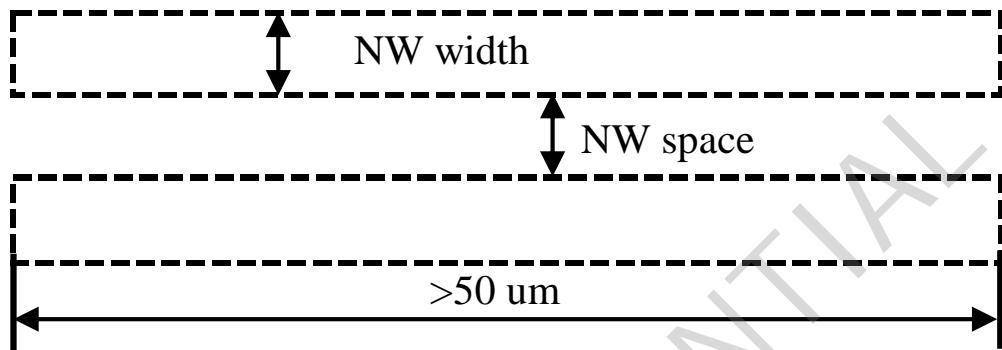


NW. 12



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NW.17^[R] : For parallel long NW (length > 50um), must make NW width larger than 0.89um or NW to NW space larger than 0.89um





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RESNW layer is to define the NW resistor area where no other implantation layer except for NW; NW resistor is the overlapped area of NW and RESNW. NW resistor under AA should have SAB on top except the contact region.

NW resistor on AA: RESNWAA= (NW AND RESNW) AND AA

NW resistor under STI= (NW AND RESNW) NOT AA

RESNW is a mark layer for LVS and DRC check..

7.4.3.1. NW resistor under STI Rules

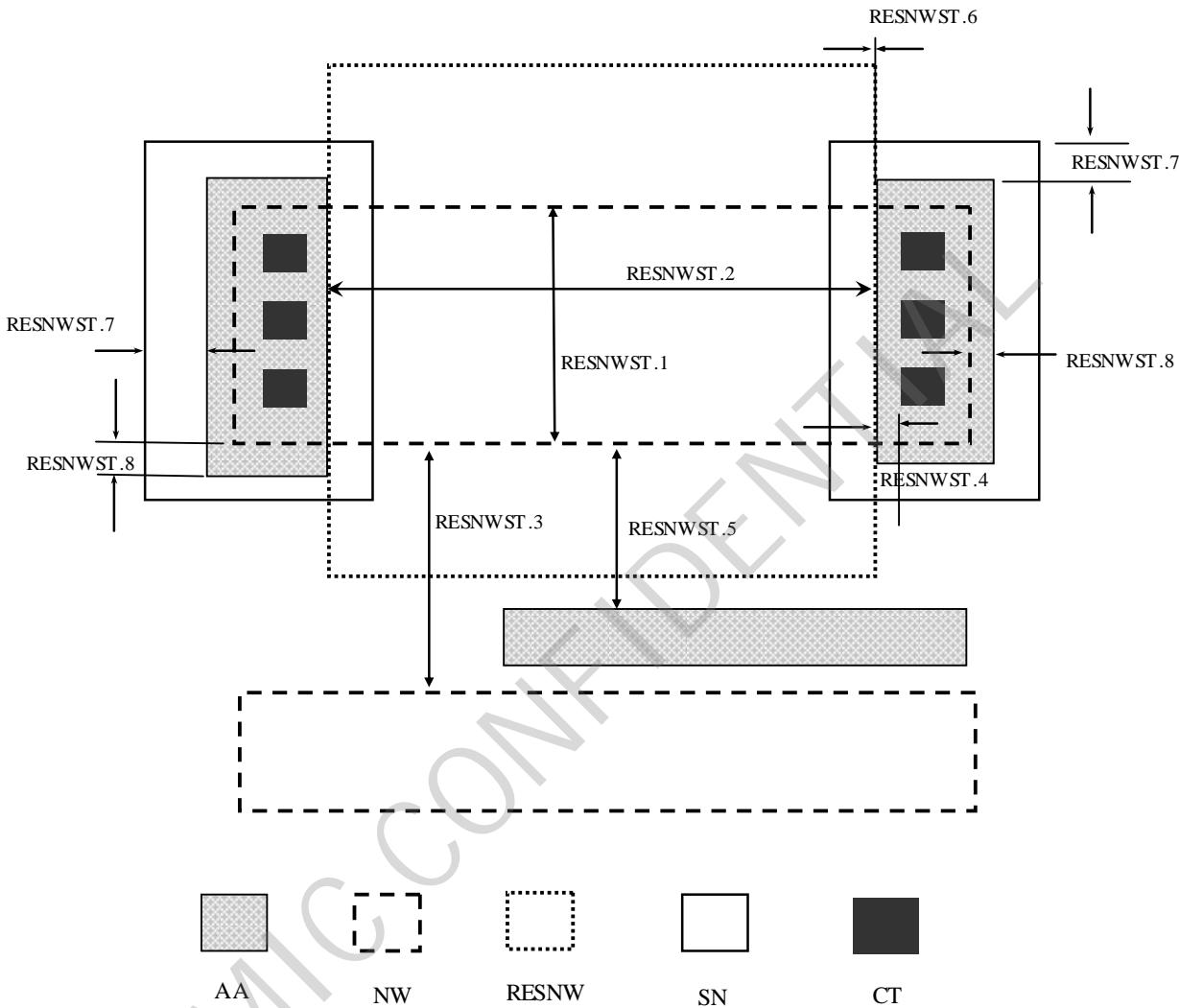
The NW Resistor in this section means NW resistor under STI

Rule item	Description	Lbl	Op	Design Value	Unit
RESNWST.1	NW-Resistor width	W1	\geq	1.2	μm
RESNWST.2	NW-Resistor length	L1	\geq	10	μm
RESNWST.3	NW-Resistor and NW space	S1	\geq	1	μm
RESNWST.4	The nearest CT space to (AA edge touch RESNW)	S2	$=$	0.3	
RESNWST.5	Space between NW resistor and adjacent AA	S3	\geq	0.44	μm
RESNWST.6	Space between RESNW to silicided AA area. DRC check by (RESNW AND NW) touch AA edge with count 2.	S4	$=$	0.00	μm
RESNWST.7	SN enclosure of AA	EN1	\geq	0.4	
RESNWST.8	AA enclosure of NW(the NW interacted with RESNW)	EN2	\geq	0.3	
RESNWST.9	CT should be in (NW AND (pick up AA))	R1			
RESNWST.10	NW resistor under STI must not overlap with AADUM	R2			
RESNWST.11	(RESNW AND NW) must be an orthogonal rectangle shape to have good simulation accuracy	R3			

Note:

1. DR check of R1: highlight CT and ((AA touch RESNW) not NW)
2. NW resistor length L1 calculation: (AA edge touch RESNW) space inside of RESNW
3. RESNW to AA space S4 check: a. AA should not straddle RESNW edge; b. One RESNW allow exact two AA TOUCH with its edge.
4. Check method of S2 CT space to AA edge: (CT inside ((NW interact RESNW) AND AA)) space to the (AA touch RESNW edge) where the AA this CT within.

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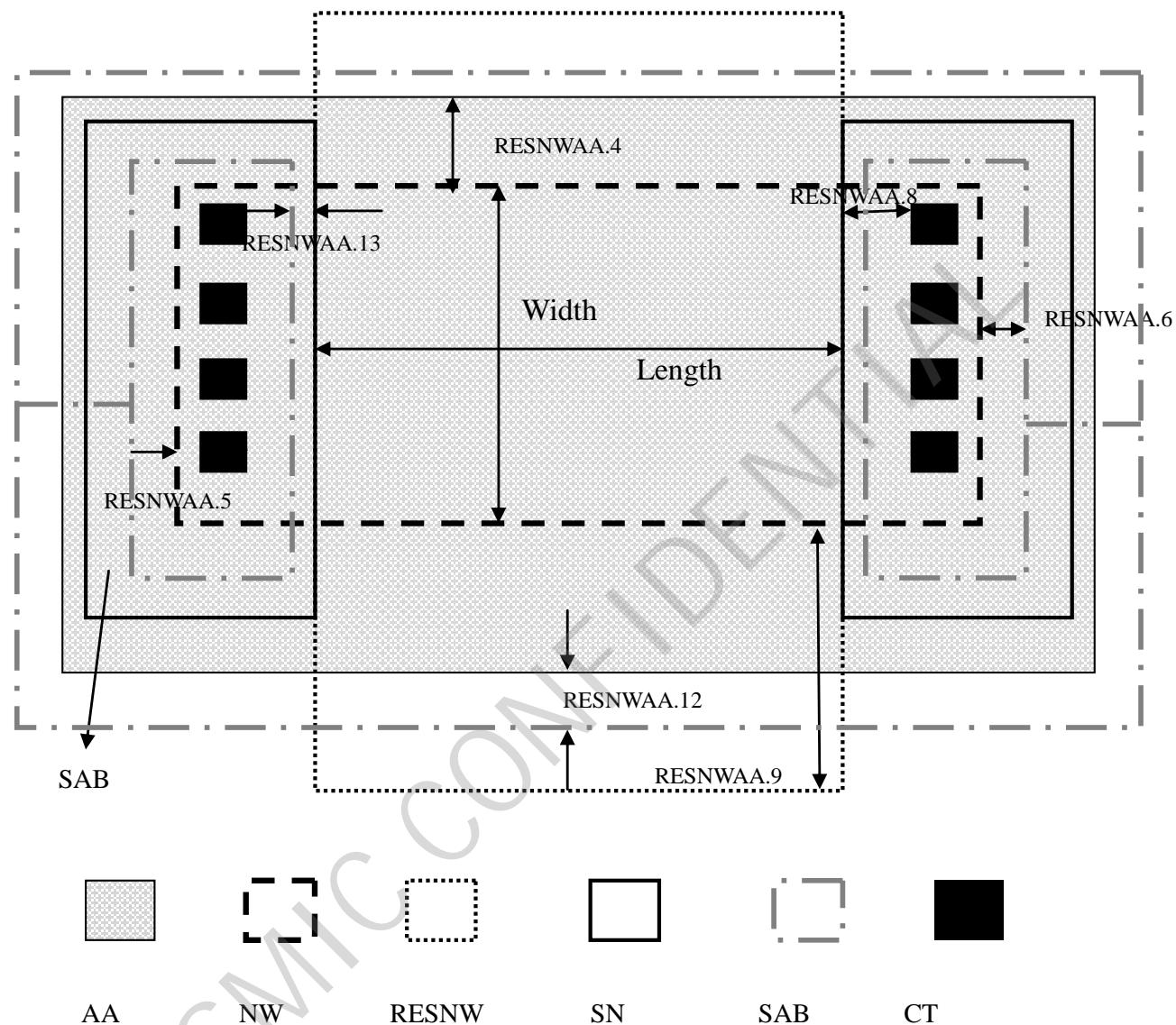
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7.4.3.2. NW resistor on AA Rules

NW resistor in this section is NW resistor on AA

Rules number	Description	Operation	Design Value	Unit
RESNWAA.1	RESNW must be an orthogonal rectangle			
RESNWAA.2	NW-Resistor length	\geq	10	μm
RESNWAA.3	NW-Resistor width	\geq	1.2	μm
RESNWAA.4	AA enclosure of RESNWAA	\geq	0.3	μm
RESNWAA.5	NW enclosure of CT	\geq	0.20	μm
RESNWAA.6	Enclosure of SAB beyond related NW	\geq	0.20	μm
RESNWAA.7	RESNW must not overlap with other implant layers (except NW) in the NW-Resistor area. Other implant layers: LVT, HVT, SN, SP, ESD1. These layers don't interact with resistors.			
RESNWAA.8	Space between RESNW and CT inside (AA interact RESNW)	=	0.70	μm
RESNWAA.9	Extension of RESNW outside of NW	\geq	0.00	μm
RESNWAA.10	SAB must include NW resistor except CT area			
RESNWAA.11	Space between RESNW to SN	=	0.00	μm
RESNWAA.12	SAB enclosure of AA	\geq	0.18	μm
RESNWAA.13	SAB overlap of SN. Use exact value on sides touch RESNW.	=	0.4	μm

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7.4.4 PSUB: Native NMOS Implant Block Layer Rules

Rules number	Description	Operation	Design Value	Unit
PSUB.1	PSUB width	\geq	0.330	μm
PSUB.2	AA width of native NMOS for 0.9/1.1/1.2/1.8/2.5V transistors	\geq	0.400	μm
PSUB.3a	0.9/1.1/1.2V gate length enclosed by PSUB	\geq	0.300	μm
PSUB.3b	1.8V gate length enclosed by PSUB(enclosed by DG)	\geq	0.8	μm
PSUB.3c	2.5V gate length enclosed by PSUB(enclosed by TG)	\geq	1.2	μm
PSUB.3d	2.5V overdrive 3.3V gate length enclosed by PSUB (enclosed by TG)	\geq	1.2	μm
PSUB.3e	2.5V underdrive 1.8V gate length enclosure by PSUB(enclosed by TG)	\geq	1.2	μm
PSUB.4	Space between two PSUB	\geq	0.330	μm
PSUB.5	PSUB enclosure of AA. <i>DRC doesn't check IND MY region.</i>	\geq	0.200	μm
		\leq	0.260	μm
PSUB.6	Space between PSUB and unrelated AA. <i>DRC doesn't check IND MY region.</i>	\geq	0.08	μm
PSUB.7	Space between PSUB and NW. <i>DRC doesn't check IND MY region.</i>	\geq	0.63	μm
PSUB.8	(purposely blank)			
PSUB.9	Space between a PSUB and an unrelated Gate region. <i>DRC doesn't check IND MY region.</i>	\geq	0.370	μm
PSUB.10	PSUB inside or cross over a NW area is not allowed			
PSUB.11	PSUB inside or cross over a DNW area is not allowed			
PSUB.12	Only one AA region is allowed to exist in one PSUB region, except for the NMOS capacitor, IND MY and pickup region.			
PSUB.13	(purposely blank)			
PSUB.14	PSUB area	\geq	0.7	μm^2
PSUB.15	PSUB enclosed area	\geq	0.64	μm^2
PSUB.16^[R]	It's not allowed (SP AND GATE) in PSUB. <i>DRC doesn't check IND MY region.</i>			

Note:

1. (purposely blank)

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2. (purposely blank)
3. (purposely blank)
4. (purposely blank)
5. (purposely blank)
6. The PW mask is generated from NW and PSUB patterns if Native NMOS exists in circuitry.
7. It is recommended that PSUB should be conformal to AA edge. For example, in the case of dog-bone AA, PSUB should draw like Fig.1 and avoid PSUB like Fig.2. When the distance X between AA, as shown in Fig.2, is too short (so that PSUB.4 is violated), it is recommended to increase X to make PSUB conform to AA edge.

This note is not used for IND MY region.

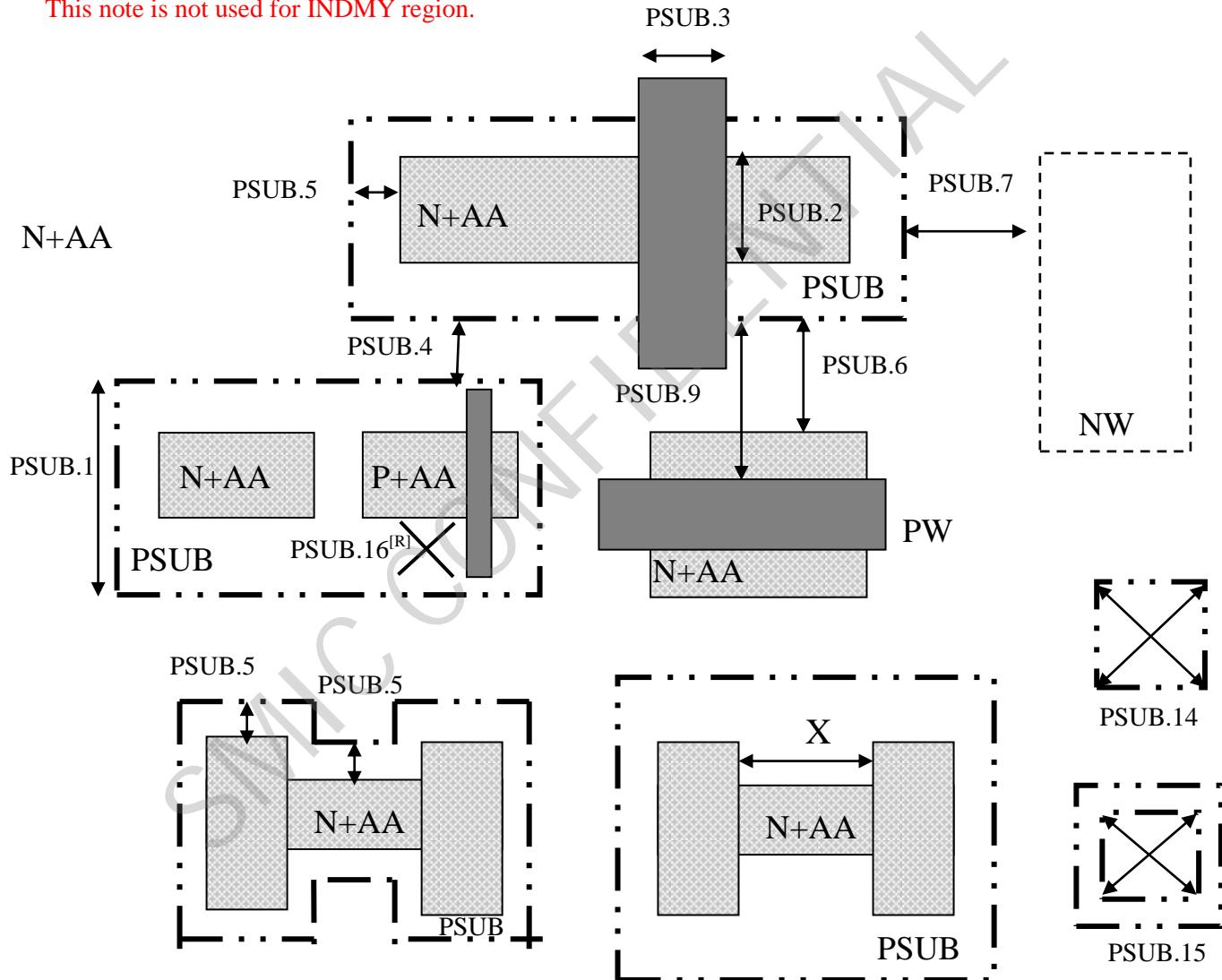
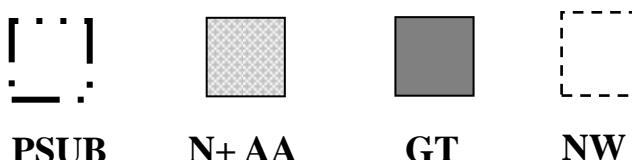


Fig.1 Recommended

Fig.2 Not recommended



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7.4.5 TG: Triple Gate Rules (Define 2.5 IO2 region)

Rules number	Description	Operation	Design Value	Unit
TG.1	TG width (Single-point-interaction is allowed.)	\geq	0.33	μm
TG.2	Space between two TGs (Single-point-interaction is allowed.)	\geq	0.33	μm
TG.3	AA with transistor enclosure by TG(include AA area not under poly)	\geq	0.20	μm
TG.4	Real gate enclosure by TG	\geq	0.20	μm
TG.5	Space between TG and AA with device (include all the devices described in the design truth table 7.1.8). Prohibit overlap of TG and other voltage AA with transistor.	\geq	0.19	μm
TG.6	Space between TG and Real gate (Don't be necessary for pick-up to follow these rules)	\geq	0.19	μm
TG.7	TG area	\geq	0.463	μm^2
TG.8	TG enclosed area	\geq	0.463	μm^2
TG.9	(purposely blank)			
TG.10	(purposely blank)			
TG.11^[R]	Extension of AA in TG outside of Real Gate . Exclude gate within LDMOS region(within LDBK) and within inductor area(layer INDMDY)	\geq	0.15	μm
TG.12	Space between TG and DG	\geq	0.33	μm
TG.13	TG overlap past NW with abutting permitted	\geq	0.33	μm
TG.14	TG overlap of NW with abutting permitted	\geq	0.33	μm
TG.15	NW overlap past TG with abutting permitted	\geq	0.33	μm
TG.16	((DG OR TG) OR NW) width. DRC only check opposite side. This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) connected region.	\geq	0.33	μm
TG.16a	((DG OR TG) OR NW) width for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) connected area.	\geq	0.27	μm
TG.17	Space between (DG OR TG) and NW. (with run length > 0). Space= 0um is allowed. DRC waive: a) The violated region doesn't interact with AA.	\geq	0.33	μm

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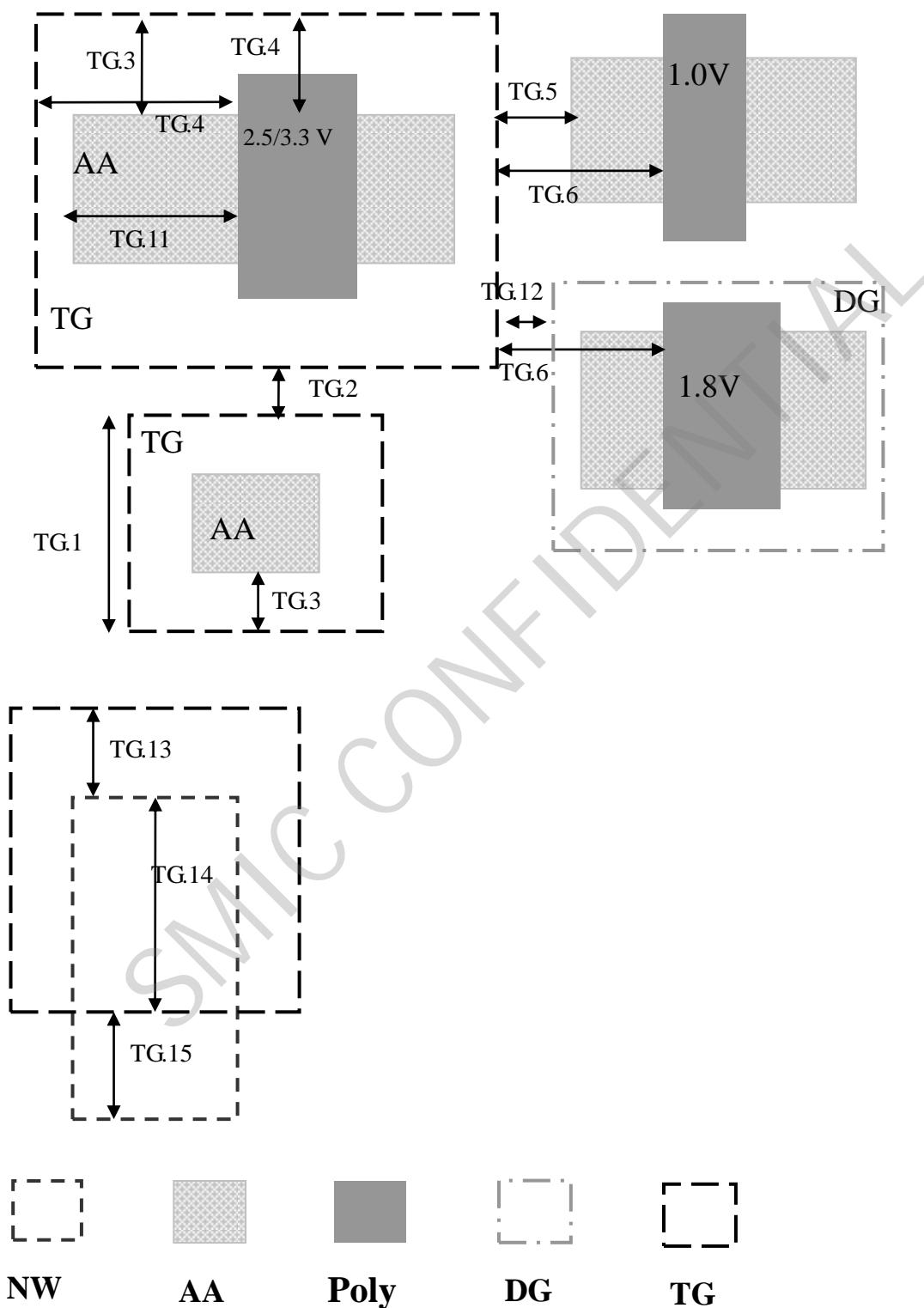
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	b) The violated region interacts with AA, but the AA is pickup AA.			
TG.18	Space between (NW NOT (DG OR TG)) and (NW NOT (DG OR TG)). (With run length > 0, skip to check jog <=0.01um pattern.)	\geq	0.33	μm
TG.19	Space between ((DG OR TG) AND NW) and ((DG OR TG) AND NW). (With run length > 0).	\geq	0.33	μm
TG.20	Space between ((DG OR TG) NOT (NW OR PSUB)) and ((DG OR TG) NOT (NW OR PSUB)). (With run length > 0).	\geq	0.33	μm

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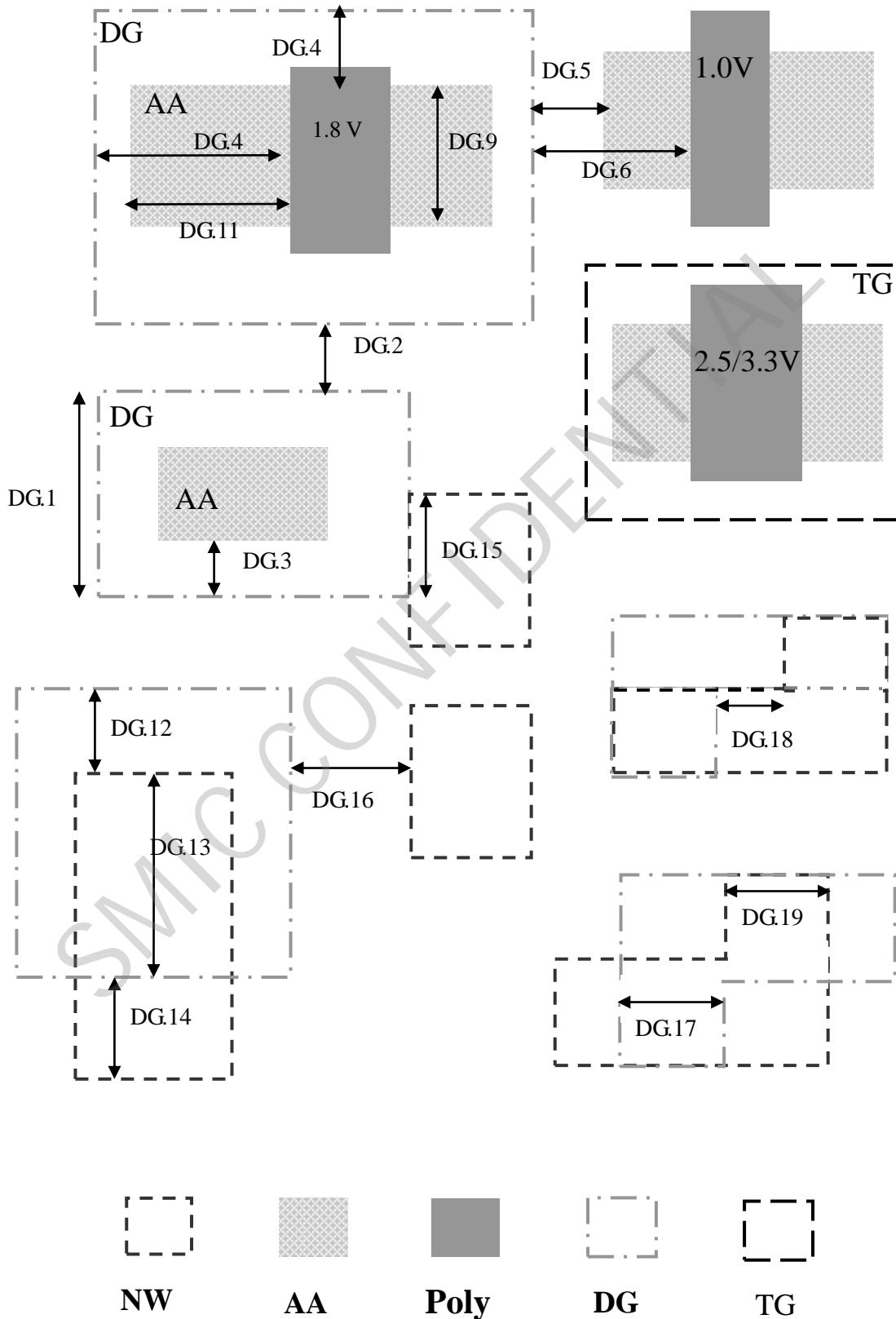


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7.4.6 DG: Dual Gate Rules (Define 1.8V IO1 region)

Rules number	Description	Operation	Design Value	Unit
DG.1	DG width	\geq	0.33	μm
DG.2	Space between two DGs	\geq	0.33	μm
DG.3	AA with transistor enclosure by DG(include AA area not under poly)	\geq	0.20	μm
DG.4	Real gate enclosure by DG	\geq	0.20	μm
DG.5	Space between DG and AA with device (include all the devices described in the design truth table 7.1.8). Prohibit overlap of DG and other voltage AA with transistor.	\geq	0.19	μm
DG.6	Space between DG and Real gate (Don't be necessary for pick-up to follow these rules)	\geq	0.19	μm
DG.7	DG area	\geq	0.463	μm^2
DG.8	DG enclosed area	\geq	0.463	μm^2
DG.9	(purposely blank)			
DG.10	(purposely blank)			
DG.11^[R]	AA (enclosed by DG) overlap past poly	\geq	0.15	μm
DG.12	DG overlap past NW with abutting permitted	\geq	0.33	μm
DG.13	DG overlap of NW with abutting permitted	\geq	0.33	μm
DG.14	NW overlap past DG with abutting permitted	\geq	0.33	μm

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7.4.7 GT: Poly Rules

Rules number	Description	Operation	Design Value	Unit
GT.1a	Real Gate channel length for 0.9/1.1/1.2V N/P MOS transistors (std, high, or low VT)	\geq	0.04	μm
GT.1a ^[R]	Real Gate channel length for 0.9/1.1/1.2V N/P MOS transistors (std, high, or low VT)	\geq	0.044	μm
GT.1b	Real Gate channel length for 1.8V N/P MOS transistors	\geq	0.15	μm
GT.1c	Real Gate channel length for 2.5V N/P MOS transistors	\geq	0.27	μm
GT.1d	Real Gate channel length for 2.5V overdrive 3.3V NMOS transistors	\geq	0.55	μm
GT.1e	Real Gate channel length for 2.5V overdrive 3.3V PMOS transistors	\geq	0.44	μm
GT.1f	Real Gate channel length for 2.5V underdrive 1.8V NMOS transistors	\geq	0.24	μm
GT.1g	Real Gate channel length for 2.5V underdrive 1.8V PMOS transistors	\geq	0.24	μm
GT.1h	Real Gate channel length for 1.8V underdrive 1.5V N/P MOS transistors	\geq	0.125	μm
GT.2a	Poly width	\geq	0.04	μm
GT.2b ^[R]	Non-floating poly outside of (extend AA W \geq 2.5 μm) region width. This rule is not applicable for GT interacting with EFUSE (81;2).	\geq	0.06	μm
GT.3	Space between two GTs	\geq	0.1	μm
GT.3b	(Purposely blank)			
GT.3c	GT to GT space if one GT's width $>$ 0.12 μm , parallel run length of the two GT $>$ 0.14 μm	\geq	0.14	μm
GT.3d	Space between two GATEs when L-shape AA and L-shape poly enclosed area $<$ 0.011 μm^2	\geq	0.105	μm
GT.3e	Space between large GT and GATE when the GATE channel length \leq 0.08 μm . The large GT definition: GT area \geq 630 μm^2 and within regions of density $>$ 70% in window 30 μm x 30 μm , stepping 15 μm . Dummy poly isn't included in the density check.	\geq	0.93	μm
GT.4	Space between AA and poly on field oxide	\geq	0.03	μm
GT.5	Extension of AA outside of Real Gate. Exclude gate within	\geq	0.06	μm

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Rules number	Description	Operation	Design Value	Unit
	LDMOS region(within LDBK) and within inductor area(layer: INDMDY)			
GT.5a ^[R]	Extension of AA outside of Real Gate. Exclude gate within LDMOS region (layer: LDBK) and within inductor area (layer: INDMDY).	≥	0.07	μm
GT.6	Extension of poly outside of AA to form poly end-cap Waive within LDBK area.	≥	0.09	μm
GT.6a ^[R]	Extension E of GT outside of AA to form poly end-cap. The GT to L shape AA (in the same MOS) space S < 0.1 μm. The L shape AA height h > 0.02 μm. This rule is not applied for (DNSRAM OR LRSRAM) OR D2SRAM) OR RFSRAM) covered region.	≥	0.11	μm
GT.6b ^[R]	Extension of poly outside of AA to form poly end-cap. Exclude inside inductor (layer: INDMDY) and exclude inside LDMOS (layer: LDBK).	≥	0.10	μm
GT.7	(Purposely blank)			
GT.8	(Purposely blank)			
GT.8a	Space between GT line end to line (Dh) or GT line to line (Ds) when the layout structures meet the conditions of below: (Waive the GT small extrusion F<0.04 μm) 1. GT line end definition: GT width W<0.065 μm 2. Run length of GT line to line or GT line to end: E1>=-0.03 μm 3. Any one edge distance from the corner of the two edges: K1 <0.065 μm Any one of Dh or Ds meet this rule value is ok. This rule is not applicable for SRAM region check.	≥	0.11	μm
GT.9	For GT channel length < 0.06, range of Real Gate space to (GT or GTDUM) The (GT or GTDUM) parallel to Real Gate for (GT.9) covers channel width >= 67%. GT.9 not applicable for SRAM area.	≥	0.12	μm
GT.10	For GT channel length ≥ 0.06, Real Gate space to (GT or GTDUM)	≥	0.13	μm
GT.11	(Purposely blank)			
GT.12	(Purposely blank)			

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Rules number	Description	Operation	Design Value	Unit
GT.13	(Purposely blank)			
GT.14	(Purposely blank)			
GT.15	(Purposely blank)			
GT.16	(Purposely blank)			
GT.17	GT area	\geq	0.012	μm^2
GT.17a ^[R]	GT area when GT all of edge length $< 0.21 \mu\text{m}$	\geq	0.055	μm^2
GT.18	Poly enclosed area	\geq	0.04	μm^2
GT.18a ^[R]	Enclosed area when GT all of inner edge length $< 0.21 \mu\text{m}$	\geq	0.077	μm^2
GT.19	(Purposely blank)			
GT.20	Poly density(including dummy)(full chip)	\geq	13%	
		\leq	40%	
GT.20b	Poly density overlap by DUMBP. Exclude OCCD, OCOVL region.	\geq	13%	
GT.20c	(purposely blank)			
GT.20d	(purposely blank)			
GT.21	No bent Real Gate on AA is allowed. All Real Gate patterns on AA have to be orthogonal to AA edge.			
GT.22	GT must be enclosed by (SN or SP) except the MOM, GTFUSE and (HRP AND GT). Exclude floating GT Fail to comply with silicide poly may have up to 10% Rs difference between with and without (SN or SP) implant.			
GT.23	(purposely blank)			
GT.24	L-shape poly space to AA	\geq	0.04	μm
GT.24a	(purposely blank)			
GT.24b ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $\leq 0.45 \mu\text{m}$, and L-shape GT length ($L \geq 0.055 \mu\text{m}$), space between L-shaped GT to AA in the same MOS. (Waive the violations in SRAM area)	\geq	0.05	μm
GT.24c ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $> 0.45 \mu\text{m}$, and L-shape GT length ($L \geq 0.055 \mu\text{m}$), space between L-shaped GT to AA in the same MOS	\geq	0.05	μm

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Rules number	Description	Operation	Design Value	Unit
GT.25	L-shape AA space to poly(in the same transistor)	\geq	0.03	μm
GT.25a	(purposely blank)			
GT.25b ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $\leq 0.45 \mu\text{m}$, space between L-shaped AA to GT in the same MOS. (Waive the violations in SRAM area)	\geq	0.05	μm
GT.25c ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $> 0.45 \mu\text{m}$, space between L-shaped AA to GT in the same MOS	\geq	0.05	μm
GT.26	All memory cell transistor(transistors within INST layer), gate GT direction should be unidirectional in one chip			
GT.27	Bent 45 degree GT width	\geq	0.16	μm
GT.28	Space between GT to bent 45 degree GT. This rule is not applied for LOGO region.	\geq	0.16	μm
GT.29	The poly length between two CTs (the two CTs on same poly), when the poly width $< 0.08\mu\text{m}$. This rule isn't applicable for ESDIO2, ESDHV region.	\leq	20	μm
GT.30	The length from the any point inside poly GATE to the nearest CT on GATE poly, when the poly width $< 0.08\mu\text{m}$. This rule isn't applicable for ESDIO2, ESDHV region.	\leq	65	μm
GT.31	(AA or poly) local density (including dummy). 1. Checked window size: $20 \mu\text{m} \times 20 \mu\text{m}$, stepping $10 \mu\text{m}$. Excluded: DUMBA/DUMBPF/RESNW/LOGO/INDMY region. 2. The rule is applied while the checked region width $\geq 5 \mu\text{m}$.	\geq	0.05%	
GT.32 ^[R]	Poly interacting AA must separate at least two AA diffusions (exclude dummy pattern). DRC doesn't check: 1. (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM), LDBK, LOGO and INDMY covered region. 2. When AA or poly not interact with CT.			
GT.33 ^[R]	Floating Real Gate is not allowed if the effective source/drain is not connected together. Definition of floating Real Gate: 1. Real Gate without CT on poly. 2. Real Gate with CT on poly but not connect to MOS AA, pickup or PAD. 3. It is not a floating Real Gate if the Real Gate is connected to			

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Rules number	Description	Operation	Design Value	Unit
	<p>AA by butted CT in (DNSRAM OR LRSRAM) OR D2SRAM OR RFSRAM) covered region.</p> <p>Definition of effective source/drain:</p> <p>Source/drain is connected to different (MOS AA NOT poly), pickup, Real Gate or PAD.</p> <p>This rule is only used to check chip level GDS.</p>			
GT.34 ^[R]	Distance from poly to a perpendicular AA "U" inside vertex, where the AA vertex distance is $\leq 0.210 \mu\text{m}$.	\geq	0.09	μm
GT.35 ^[R]	Poly overlap past AA when poly to AA inner vertex distance $< 0.040 \mu\text{m}$.	\geq	0.13	μm

Note:

1. Poly_end with length means the poly end extension outside of AA.
2. GT.26 DRC check may possibly report memory cell GT direction to be all horizontal or all vertical. If there are both horizontal and vertical GT direction cells exist in one chip, the layout should be corrected to fulfill GT.26's requirement.
3. For GT.3, GT.4, the shapes cross areas with sharp angle are not applicable for the two space rules. It is depicted in Fig. 7.4.7-2.
4. GT.6 is not applicable when the GT and AA are inside inductor (layer: INDMY).

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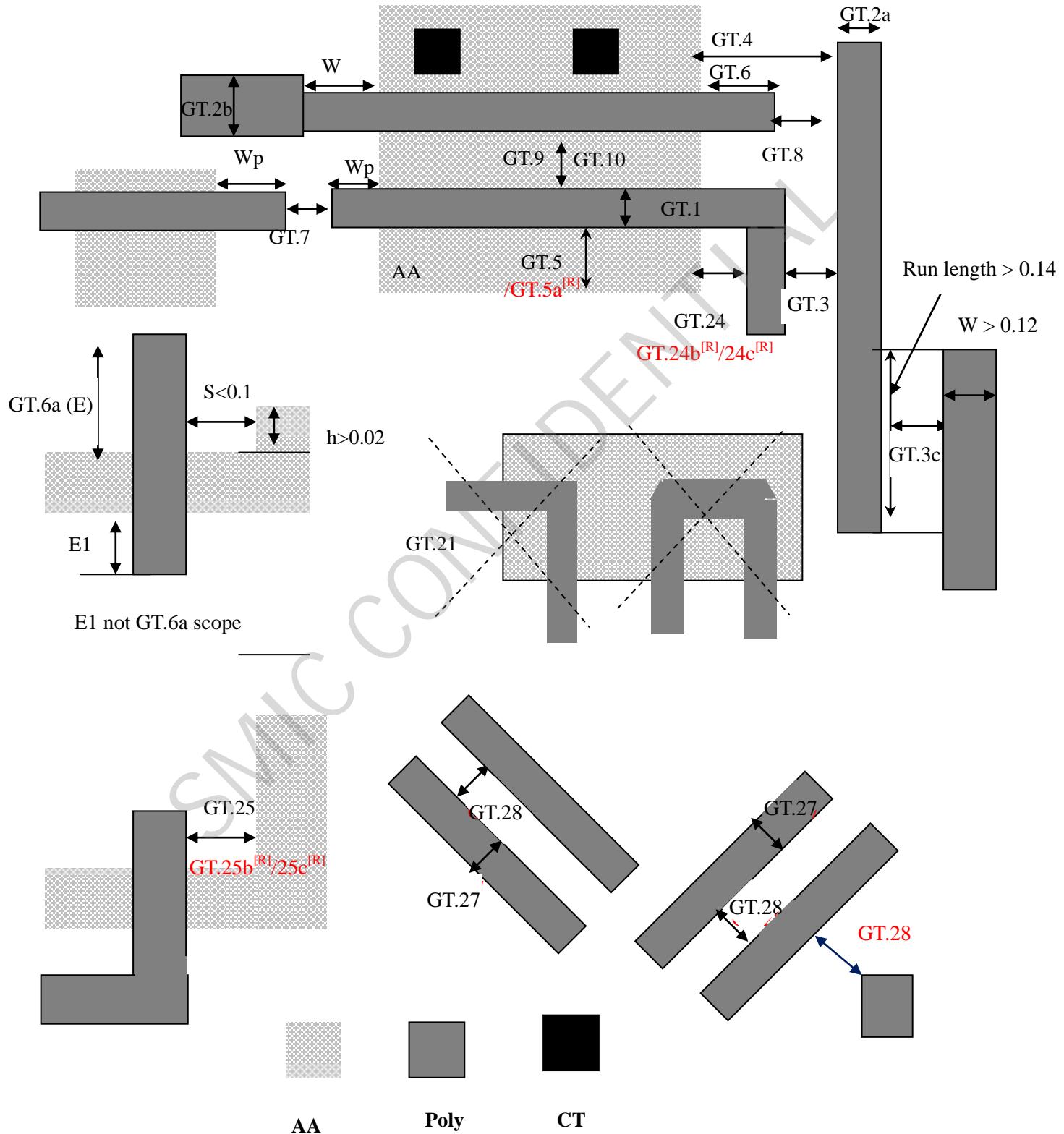


Fig. 7.4.7-1

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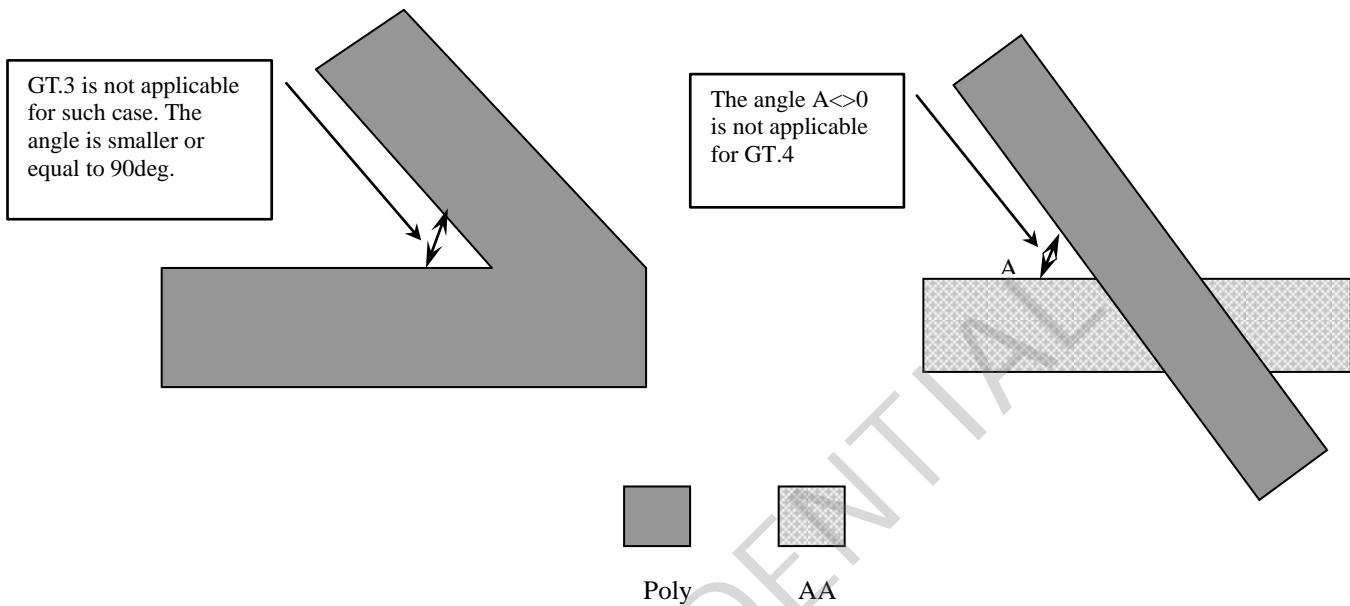


Fig. 7.4.7-2

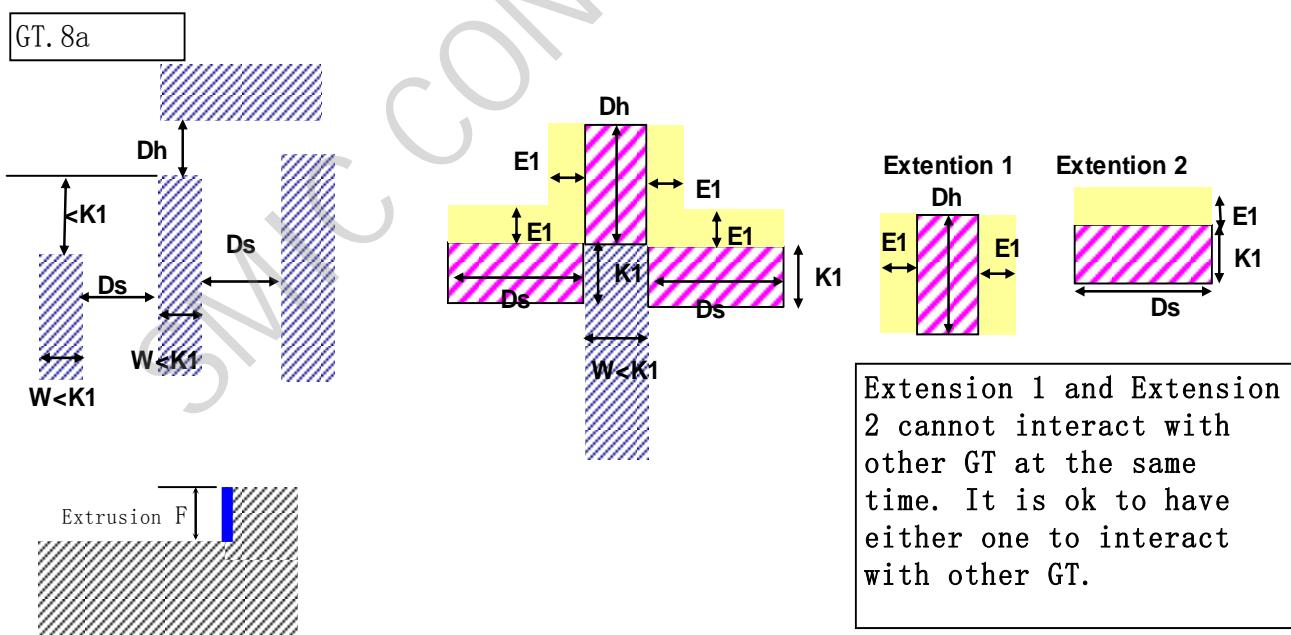


Fig 7.4.7-3

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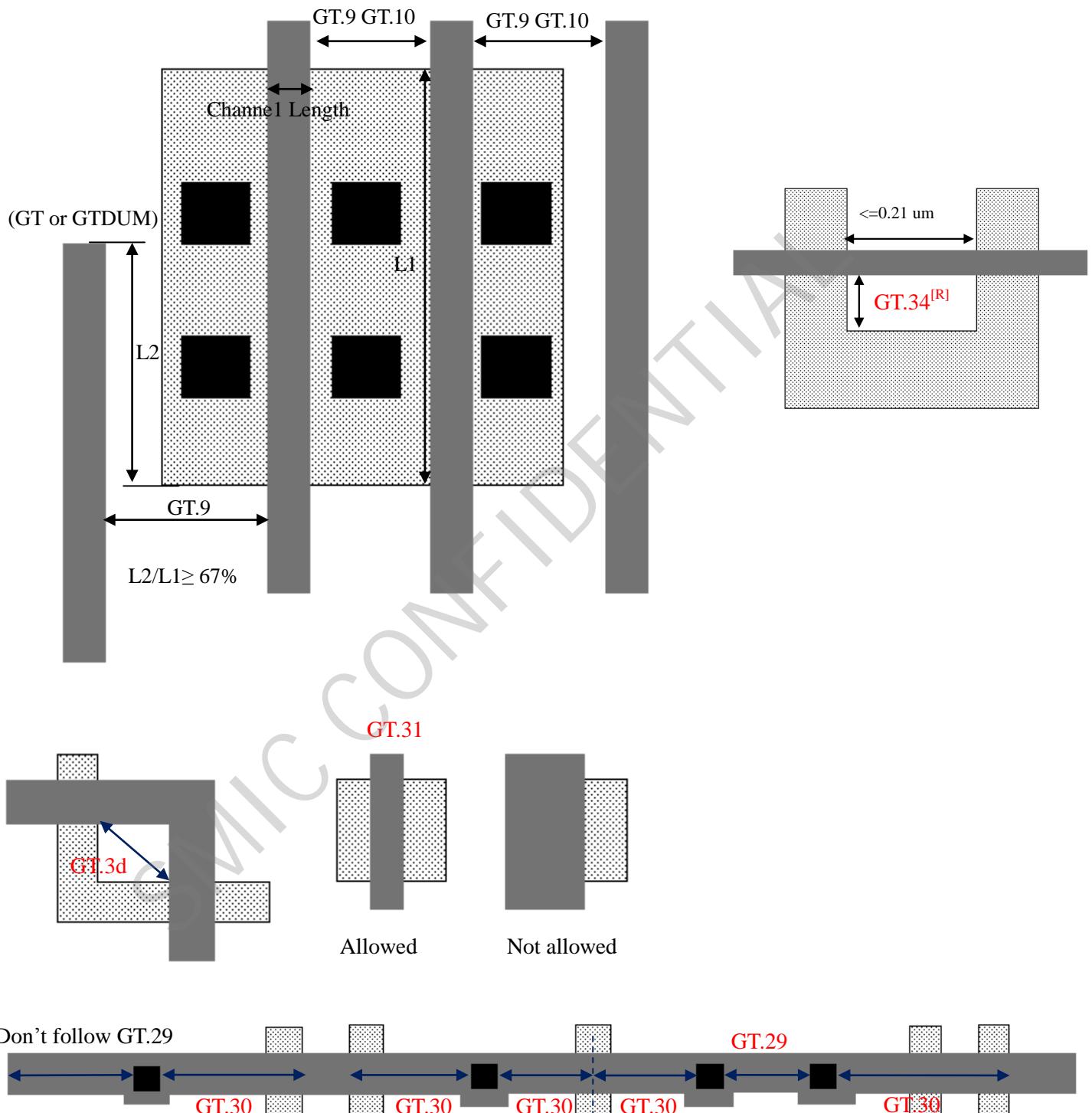


Fig. 7.4.7-4

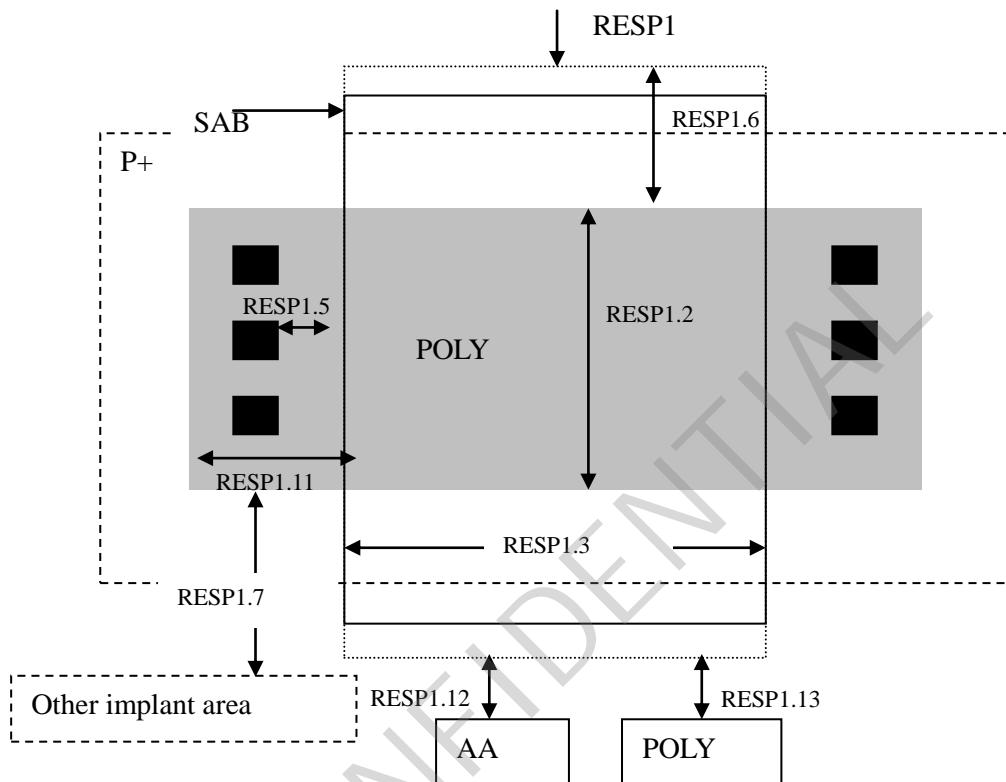
Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 112/299
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7.4.7.1 Poly Resistor Rules (Poly resistor block layer RESP1)

Poly resistor = GT AND RESP1

Rules number	Description	Operation	Design Value	Unit
RESP1.1	POLY resistor must within RESP1 layer			
RESP1.2	POLY resistor width	\geq	0.4	μm
RESP1.2 a^[R]	((purposely blank)			
RESP1.3	POLY resistor length	\geq	0.4	μm
RESP1.3a^[R]	(purposely blank)			
RESP1.4	POLY resistor must be orthogonal			
RESP1.5	CT to SAB space	\geq	0.18	μm
RESP1.6	Extension of RESP1 outside of POLY	\geq	0.15	μm
RESP1.7	The separation between resistors with un-related implant region Un-related implant region: LVT, HVT, SN, SP, ESD1. These regions don't interact with resistors.	\geq	0.16	μm
RESP1.8^[NC]	Dog-bone design at the end of POLY resistor for contact pick-up is not suggested			
RESP1.9	For POLY resistor, make sure the POLY be covered by SAB and implanted by either SN or SP.			
RESP1.10	(purposely blank)			
RESP1.11	Extension Poly to SAB	\geq	0.3	μm
RESP1.12	RESP1 space to non-related AA	\geq	0.16	μm
RESP1.13	RESP1 space to non-related Poly	\geq	0.24	μm
RESP1.14	(purposely blank)			
RESP1.15	RESP1 and SAB on GT should have coincident edge			

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7.4.7.2 Poly silicide Resistor rule

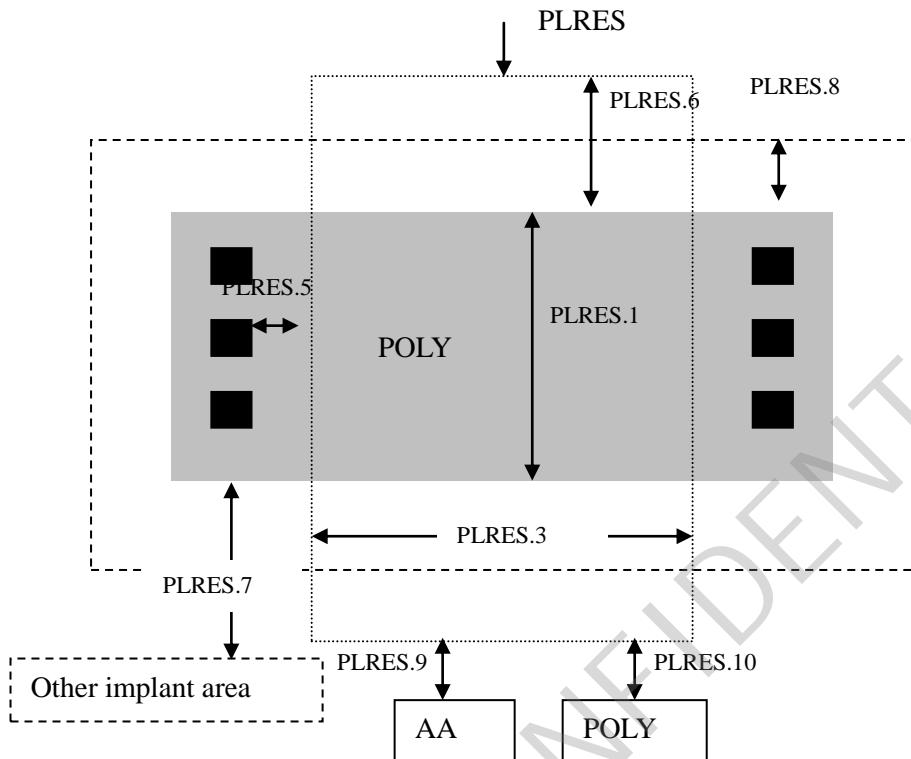
Poly resistor mark layer PLRES.

Poly Silicide resistor: (GT AND PLRES)

Rules number	DESCRIPTION	Operation	Design Value	Unit
PLRES.1	POLY silicide resistor width;	\geq	0.15	μm
PLRES.2	PLRES can not overlap with RESP1			
PLRES.3	POLY silicide resistor square number	\geq	1	
PLRES.4	POLY silicide resistor must be orthogonal			
PLRES.5	CT space to PLRES (Fixed-value)-	$=$	0.01	μm
PLRES.6	Extension of PLRES outside of POLY	\geq	0	μm
PLRES.7	The separation between resistors with un-related implant region Un-related implant region: LVT, HVT, SN, SP, ESD1. These region don't interact with resistors.	\geq	0.16	μm
PLRES.8	For POLY silicide resistor, make sure the POLY resistor be implanted by either SN or SP. Minimum enclosure by SN or SP.	\geq	0.18	μm
PLRES.9	PLRES space to non-related AA	\geq	0.16	μm
PLRES.10	PLRES space to non-related Poly	\geq	0.24	μm

Note: 1. Dog-bone design at the end of POLY resistor for contact pick-up is not suggested

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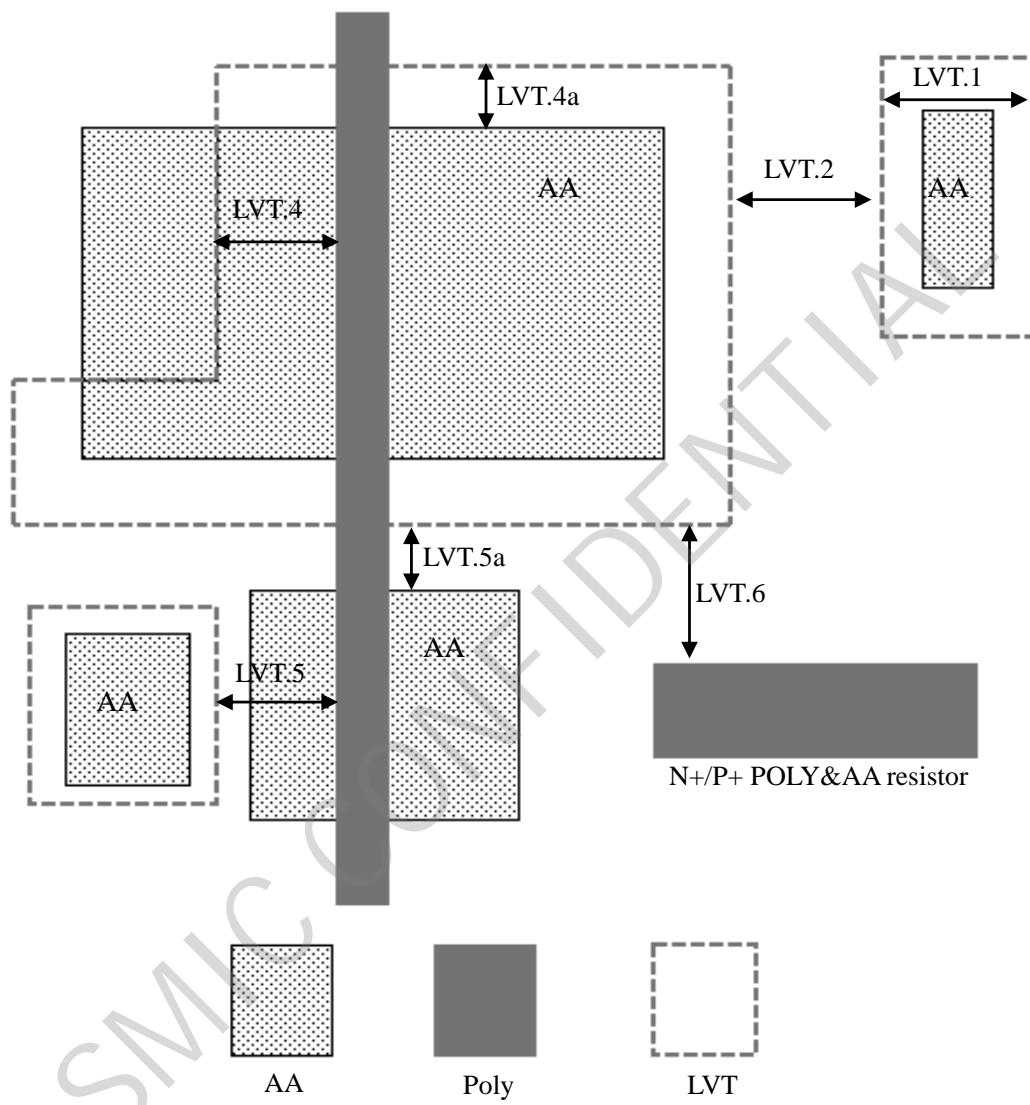


Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 116/299
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7.4.8 LVT: Low Vt devices Rules

Rules number	Description	Operation	Design Value	Unit
LVT.1	LVT width DRC only check opposite side.	\geq	0.18	μm
LVT.2	Space between two LVT. (with run length > 0)	\geq	0.18	μm
LVT.3	(purposely blank)			μm
LVT.4	LVT extension outside of Real Gate along source drain direction	\geq	0.14	μm
LVT.4a	LVT extension outside of Real Gate along poly direction	\geq	0.08	μm
LVT.5	Space between LVT and Real Gate along source drain direction	\geq	0.14	μm
LVT.5a	Space between LVT and Real Gate along poly direction	\geq	0.08	μm
LVT.6	Space between LVT to (poly SAB resistor(GT AND RESP1) or AA SAB resistor(AA AND RESAA))	\geq	0.18	μm
LVT.7	(purposely blank)			
LVT.8	(purposely blank)			
LVT.9	LVT area	\geq	0.19	μm^2
LVT.10	LVT enclosed area	\geq	0.19	μm^2
LVT.11	(purposely blank)			
LVT.12	(purposely blank)			
LVT.13	(LVT overlap AA) overlapping DG, VARMOS, PSUB and HVT is prohibited.			
LVT.14	(purposely blank)			

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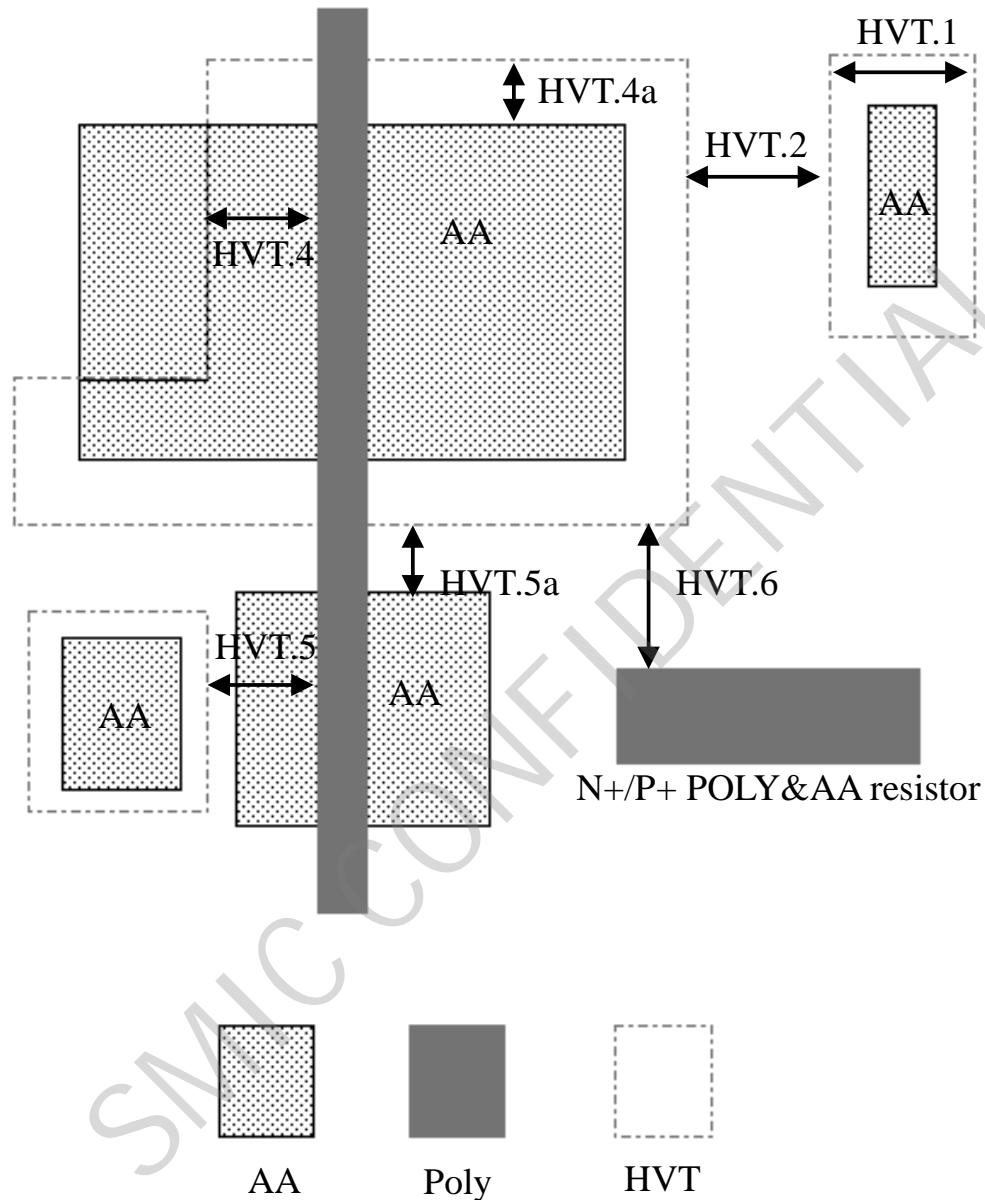


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7.4.9 HVT High Vt devices Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
HVT.1	HVT width DRC only check opposite side.	≥	0.18	μm
HVT.2	Space between two HVT. (with run length > 0)	≥	0.18	μm
HVT.3	(purposely blank)			
HVT.4	HVT extension outside of Real Gate along source drain direction	≥	0.14	μm
HVT.4a	HVT extension outside of Real Gate along poly direction	≥	0.08	μm
HVT.5	Space between HVT and Real Gate along source drain direction	≥	0.14	μm
HVT.5a	Space between HVT and Real Gate along poly direction	≥	0.08	μm
HVT.6	Space between HVT to (poly SAB resistor(RESP1 AND GT) or AA SAB resistor(RESAA AND AA))	≥	0.18	μm
HVT.7	(purposely blank)	≥		
HVT.8	(purposely blank)	≥		
HVT.9	HVT area	≥	0.19	μm ²
HVT.10	HVT enclosed area	≥	0.19	μm ²
HVT.11	(purposely blank)			
HVT.12	(purposely blank)			
HVT.13	(HVT overlap AA) overlapping DG, VARMOS, PSUB and LVT is prohibited.			
HVT.14	(purposely blank)			

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7.4.11 SP: P+ S/D Implant Layer Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
SP.1	SP width (with run length > 0)	≥	0.18	μm
SP.2	Space between two SP (with run length > 0)	≥	0.18	μm
SP.3a	Space between SP and N+ AA inside PW, except AA resistor (RESAA AND AA). (run length > 0.1 μm)	≥	0.08	μm
SP.3b	Space between SP and N+ AA inside PW, except AA resistor (RESAA AND AA). (run length ≤ 0.1 μm)	≥	0.05	μm
SP.4	Space between SP and N+ pick-up AA	≥	0.02	μm
SP.5	Space between a SP and a butted N+ AA	=	0	μm
SP.6	SP extension outside of Real Gate for PMOS along source drain direction	≥	0.16	μm
SP.7a	Space between SP and S/D direction N-channel Real Gate	≥	0.16	μm
SP.7b	Space between SP and non-S/D direction N-channel Real Gate This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region.	≥	0.08	μm
SP.7c	A butted N+ pick-up AA space to PMOS Real Gate in the same AA.	≥	0.23	μm
SP.8a	(purposely blank)			
SP.8b	(purposely blank)			
SP.8c	A butted N+ pick-up AA (in L shape AA) space to PMOS Real Gate in the same AA, when this butted N+ pick-up AA extrusion: $0 < h < 0.1 \mu\text{m}$	≥	0.23	μm
SP.9	Space between a SP and a N+ AA resistor or N+POLY resistor (SN AND ((RESAA AND AA) OR (RESP1 AND GT)))	≥	0.14	μm
SP.10	P+AA enclosure by SP	≥	0.08	μm
SP.11	(purposely blank)			
SP.12	SP enclosure of P+ pickup AA	≥	0.02	μm
SP.13	(purposely blank)			
SP.14	(P+ AA resistor or P+ Poly resistor) enclosure by SP The resistor here: (SP AND ((RESAA AND AA) OR (RESP1 AND GT)))	≥	0.14	μm

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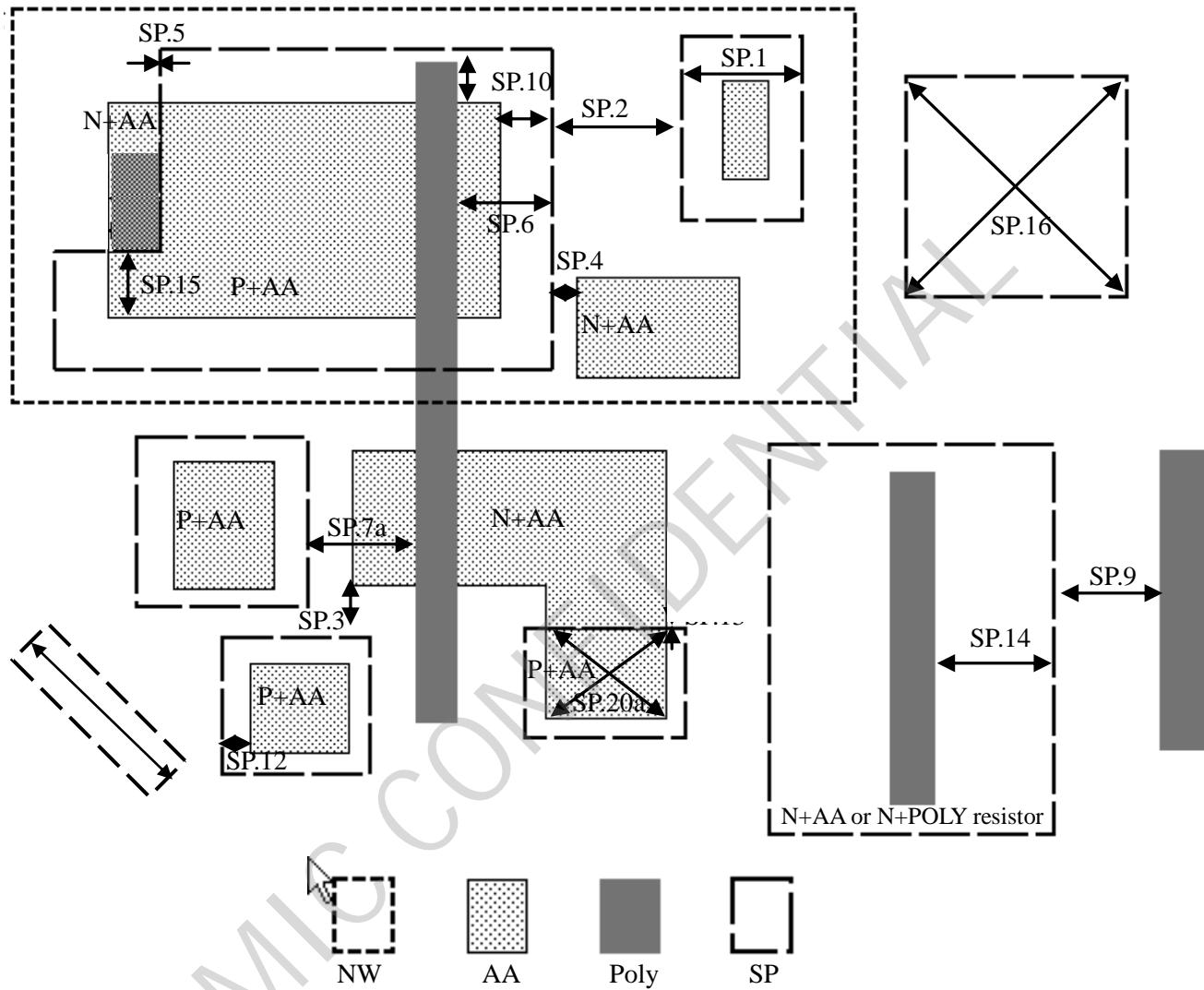
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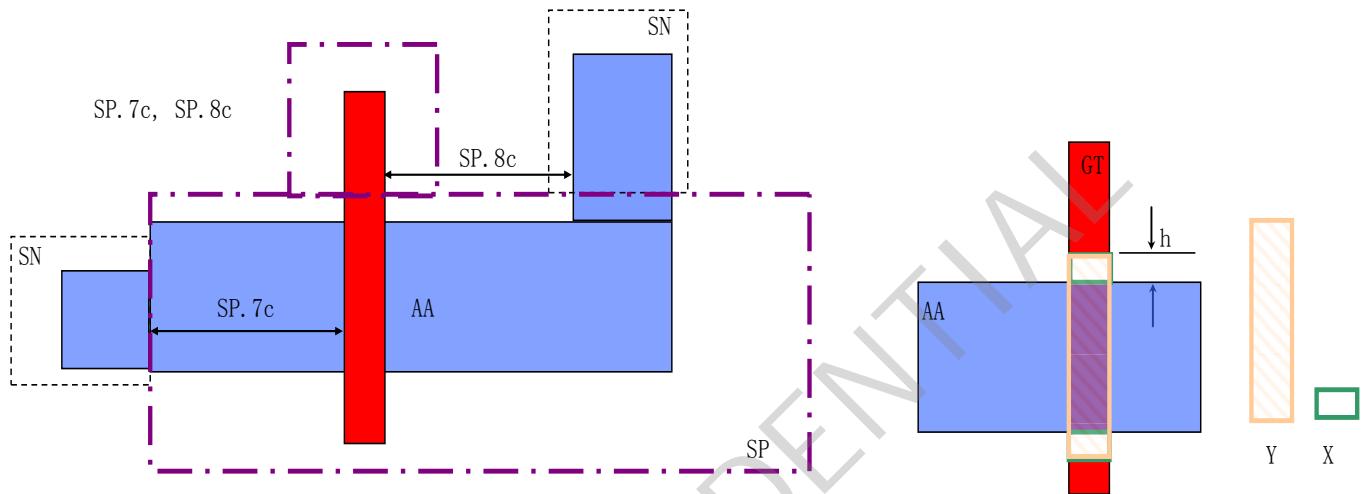
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SP.15	SP and AA overlap.	\geq	0.1	μm
SP.16	SP area (μm^2) The INST connected area apply SRAM design rule	\geq	0.11	μm^2
SP.17	SN and SP overlap is forbidden			
SP.18	Enclosed area by SP	\geq	0.11	μm^2
SP.19	(purposely blank)			
SP.20	(purposely blank)			
SP.20a	P+ butted AA in P-well area(the area interact with CT)	\geq	0.021	μm^2
SP.21	(purposely blank)			
SP.21a	(purposely blank)			

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X =AA edge in GT expand h
 SP. 7c, SP. 8c highlight Y space OPPOSITE to
 N+AA connected with the same AA PMOS S/D
 area smaller than rule value

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7.4.12 SN: N+ S/D Implant Layer Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
SN.1	SN width (run length > 0)	≥	0.18	μm
SN.2	Space between two SN. (with run length > 0)	≥	0.18	μm
SN.3a	Space between SN and P+ AA inside NW, except AA resistor (RESAA AND AA). (run length > 0.1 μm)	≥	0.08	μm
SN.3b	Space between SN and P+ AA inside NW, except AA resistor(RESAA AND AA). (run length <= 0.1 μm)	≥	0.05	μm
SN.4	Space between SN and P+ pick-up AA	≥	0.02	μm
SN.5	Space between a SN and a butted P+ AA	=	0	μm
SN.6	SN extension outside of Real Gate for NMOS along source drain direction	≥	0.16	μm
SN.7a	Space between SN and S/D direction P-channel Real Gate	≥	0.16	μm
SN.7b	Space between SN and Non-S/D direction P-channel Real Gate . This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM OR RFSRAM covered region.	≥	0.08	μm
SN.7c	A butted P+ pick-up AA space to NMOS Real Gate in the same AA.	≥	0.23	μm
SN.8a	(purposely blank)			
SN.8b	(purposely blank)			
SN.8c	A butted P+ pick-up AA (in L shape AA) space to NMOS Real Gate in the same AA, when this butted P+ pick-up AA extrusion: $0 < h < 0.1 \mu\text{m}$	≥	0.23	μm
SN.9	Space between a SN and a P+AA resistor or P+POLY resistor(SP AND ((RESAA AND AA) OR (RESP1 AND GT)))	≥	0.14	μm
SN.10	N+AA enclosure by SN Waive for (AA interact RESNW)	≥	0.08	μm
SN.11	(purposely blank)			
SN.12	N+ pickup AA enclosure by SN Waive for (AA interact RESNW)	≥	0.02	μm
SN.13	(purposely blank)			
SN.14	N+AA resistor or N+POLY resistor enclosure by SN The resistor here: (SN AND ((RESAA AND AA) OR (RESP1 AND GT)))	≥	0.14	μm
SN.15	SN and AA overlap.	≥	0.1	μm

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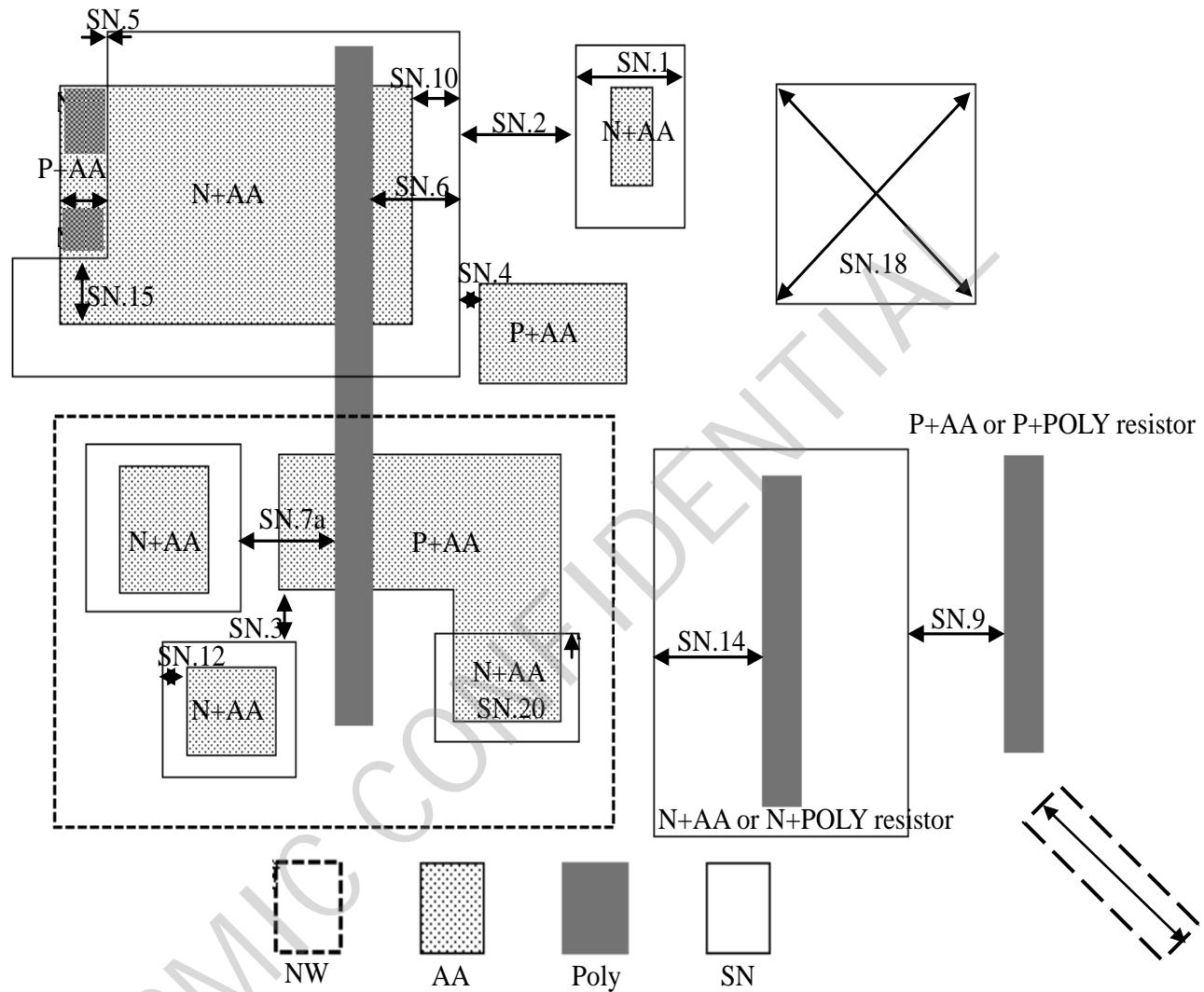
SN.16	SN area (The INST connected area apply SRAM design rule)	\geq	0.11	μm
SN.17	SN and SP overlap is forbidden			
SN.18	Enclosed area of SN (μm^2)	\geq	0.11	μm^2
SN.19	(purposely blank)			
SN.20	(purposely blank)			
SN.20a	N+ butted AA in NW minimum area(the area interact with CT)	\geq	0.021	μm^2
SN.21	(purposely blank)			
SN.21a	(purposely blank)			
SN.22	(purposely blank)			

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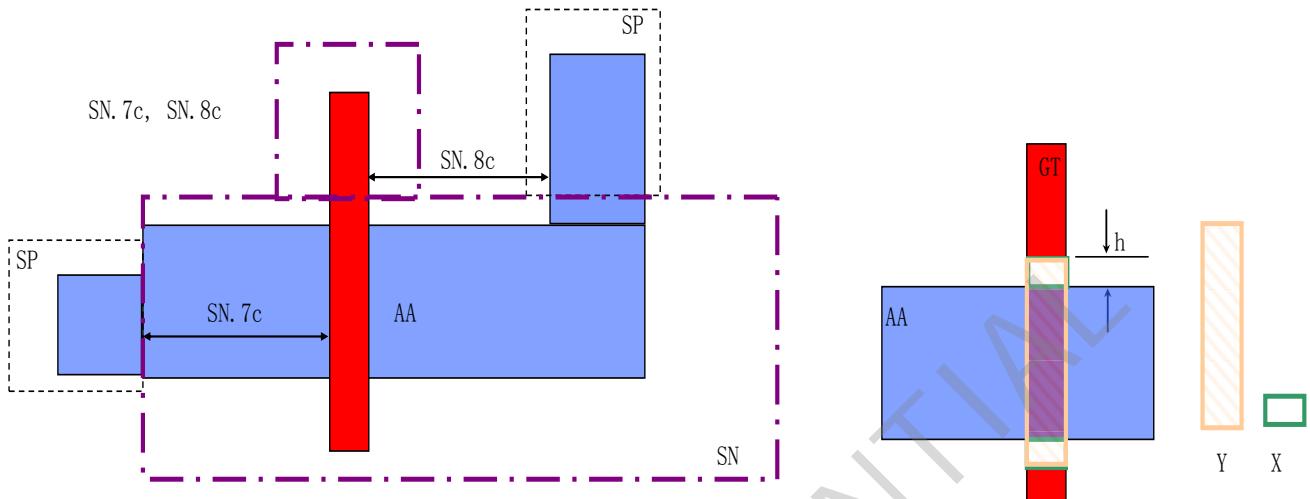
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X = AA edge in GT expand h
 SN. 7c, SN. 8c highlight Y space OPPOSITE to P+AA connected with the same AA NMOS S/D area smaller than rule value

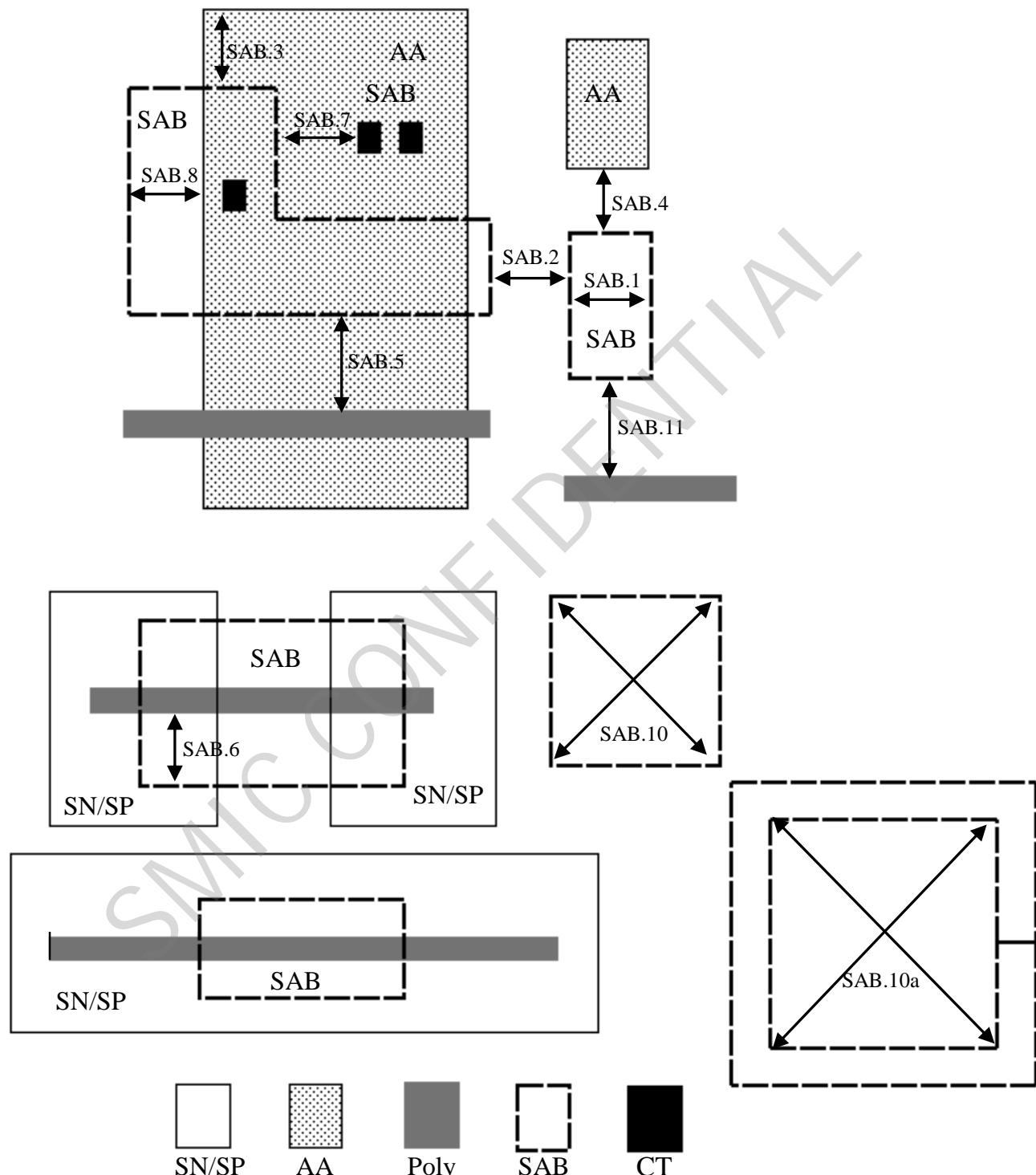


Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 128/299
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7.4.13 SAB: Salicide Block Layer Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
SAB.1	SAB width	≥	0.200	μm
SAB.2	Space between two SABs	≥	0.200	μm
SAB.3	Extension of related AA outside of SAB	≥	0.200	μm
SAB.4	Space between SAB and AA	≥	0.150	μm
SAB.5	Space between SAB and poly Real Gate	≥	0.240	μm
SAB.6	Extension of SAB outside of poly	≥	0.150	μm
SAB.7	Space between SAB and CT	≥	0.180	μm
SAB.8	Extension of SAB outside of AA	≥	0.150	μm
SAB.9	(purposely blank)			
SAB.10	SAB area	≥	0.200	μm ²
SAB.10a	SAB enclosed area	≥	0.370	μm ²
SAB.11	Space between SAB and ((GT not interacting with SAB) on STI).	≥	0.200	μm
SAB.13 ^[NC]	Follow poly resistor guideline, if poly resistor is used.			
SAB.14 ^[NC]	Follow ESD guideline, if SAB is used in ESD.			
SAB.15	(purposely blank)			
SAB.16 ^[R]	SAB overlap of GATE is not allowed (except ESDIO1, ESDIO2, ESDHV, OCOVL region).			

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7.4.14 CT: Contact Layer Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
CT.1	Fixed CT size (square shape).	=	0.060	μm
CT.1a	Non-square CT only allowed inside of [EFUSE, OCOVL, SRAM(INST)]			
CT.2	Space between two contacts	≥	0.080	μm
CT.2a	Space between two contacts on different net	≥	0.11	μm
CT.2R	(purposely blank)			
CT.3	CT array space to CT array for run length > 0.34 μm CT array is formed by logic operation (((all CTs su0.09) sd0.3) su0.21) This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region.	≥	0.110	μm
CT.3 ^[R]	CT array space to CT array for run length > 0.34μm. CT array is formed by logic operation (((all CTs su0.09) sd0.3) su0.21).	≥	0.180	μm
CT.3a	Space between two contacts in CT array: contact array is larger or equal to 4x4 CT. Two contact regions whose space is within 0.12 μm at same M1 are considered to be in the same array. This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region	≥	0.08	μm
CT.4	Space between AA region and contact overlap poly	≥	0.04	μm
CT.4 ^[R]	Space between AA region and contact overlap poly	≥	0.05	μm
CT.5	0.9/1.0/1.1/1.2V device space between Real Gate and contact overlap AA	≥	0.040	μm
CT.5 ^[R]	0.9/1.0/1.1/1.2V device space between Real Gate and contact overlap AA	≥	0.05	μm
CT.5a	1.8/2.5V device space between Real Gate (enclosure by TG or DG) to contact overlap AA	≥	0.080	μm
CT.6	CT must be within AA (if CT touches AA), and must meet rule (CT.6a or (CT.6b, CT.6c)) and CT.6d. CT.6 CT.6a, CT.6b, CT.6c and CT.6d are not applicable for CT interacts with EFUSE(81;2) The CT here is interacted with M1 and AA intersection. This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region			
CT.6a	CT enclosure by AA (four sides)	≥	0.01	μm

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CT.6b	CT enclosure by AA (exclude pick-up AA) for two opposite sides when either opposite sides<0.01 μm, >=0.005 μm.	≥	0.03	μm
CT.6c	CT enclosure by pick-up AA for two opposite sides when either opposite sides<0.01 μm, >=0.005 μm.	≥	0.02	μm
CT.6d	CT enclosure by AA	≥	0.005	μm
CT.7	CT must be within Poly (if CT touches GT) CT.7, CT.7a, CT.7b not applicable for CT interacts with EFUSE(81;2). Per M1 and Poly intersection containing a CT, must meet rule CT.7a or CT.7b. This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region.			
CT.7a	CT enclosure by Poly	≥	0.01	μm
CT.7b	CT enclosure by Poly for two opposite sides when either opposite sides<0.01 μm, >=0 μm.	≥	0.02	μm
CT.8	CT(on AA) must be fully enclosed by SP or SN. This rule is not applied for OCOVL region.	≥	0.03	μm
CT.9	(purposely blank)			
CT.10	CT overlap (poly and AA) or (STI not GT) region is forbidden. Waive the CT overlap gate in (LOGO, INDMY, MOMDMY). Waive the CT overlap STI for (CT straddles STI in INST). Waive rectangle CT in (INST or EFUSE) violation of this rule.			
CT.11	(purposely blank)			
CT.12	Non-silicided contacts are not allowed			
CT.13	45 degree rotated contacts are not allowed. This rule is not applied for OCOVL region.			
CT.14	(purposely blank)			
CT.15	(purposely blank)			
CT.16	(purposely blank)			
CT.17	(purposely blank)			
CT.18	(purposely blank)			
CT.19^[R]	(purposely blank)			
CT.20	CT must be fully covered by M1 and (AA OR GT). This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region.			
CT.21	It's not allowed CT overlap with NW, AA, Poly and M1			

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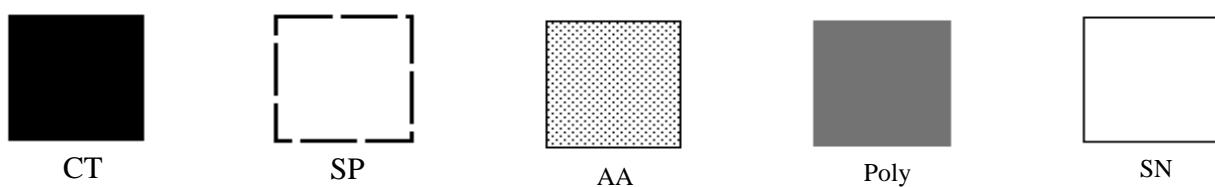
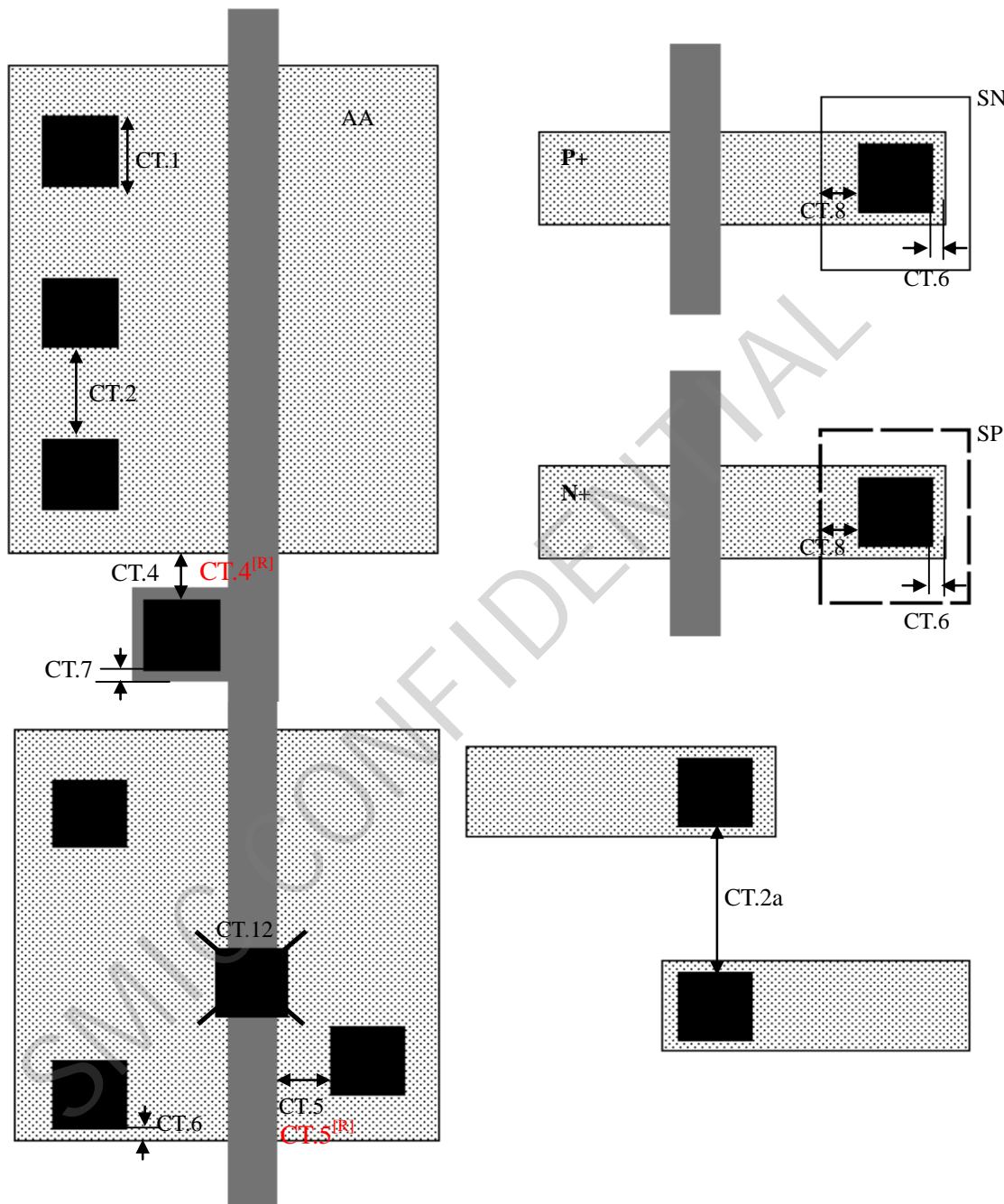
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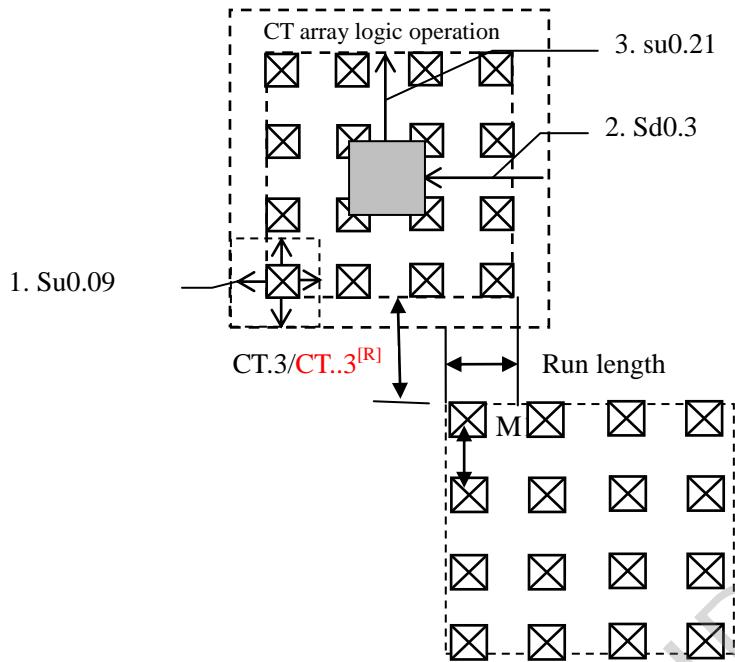
	<p>resistor.</p> <p>For NW, AA, silicide poly resistor, please refer each resistor section definition.</p> <p>Non-silicide poly resistor definition: ((GT AND RESP1) AND SAB)</p> <p>M1 resistor definition: (M1 AND M1R).</p>			
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7.4.15 SMIC 0.04 μm BEOL Design Rule Summary

Layer	Parameter	Minimum dimension	Unit	Remark
M1	Pitch	0.14	μm	
	Width	0.07	μm	Max allowed 4.5
	Space	0.07	μm	
	Enclosure of CT	0.015	μm	
	Enclosure of V1	0.015	μm	
V1-7	Pitch	0.14	μm	
	Width	0.07	μm	
	Space	0.07	μm	
M2-8	Pitch	0.14	μm	
	Width	0.07	μm	Max allowed 4.5
	Space	0.07	μm	
	Enclosure of Vn	0.015	μm	
	Enclosure of Vn-1	0.015	μm	
TM1, TM2	Pitch	0.800	μm	
	Width	0.400	μm	Max allowed 12
	Space	0.400	μm	
	Enclosure of TV2	0.010	μm	
TV1, TV2	Pitch	0.700	μm	
	Width	0.360	μm	
	Space	0.340	μm	

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7.4.16 Metal 1 Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
M1.1	M1 width.	≥	0.07	μm
M1.1 ^[R]	M1 width.	≥	0.08	μm
M1.2	M1 width.	≤	4.5	μm
M1.3	M1 space This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region.	≥	0.07	μm
M1.3 ^[R]	M1 space This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region.	≥	0.08	μm
M1.4	M1 area (The INST connected area apply SRAM design rule)	≥	0.0196	μm ²
M1.5	M1 enclosed area	≥	0.2	μm ²
M1.6	Space between two (run length > 0.3 μm) parallel metal lines with both metal line width is > 0.22 μm.	≥	0.08	μm
M1.6 ^[R]	Space between two (run length > 0.3 μm) parallel metal lines with one or both metal line width is > 0.22 μm.	≥	0.12	μm
M1.6a	Space between two (run length > 0.6 μm) parallel metal lines with one or both metal line width is > 0.7 μm.	≥	0.12	μm
M1.6b	Space between two (run length > 0.6 μm) parallel metal lines with one metal line width is > 0.22 μm and other metal line width is >0.7 μm.	≥	0.14	μm
M1.6c	Space between two (run length > 1.5 μm) parallel metal lines with one or both metal lines width is >1.5 μm.	≥	0.3	μm
M1.7	CT must be within M1; Per ((AA not gate) or GT) and M1 intersection containing a CT must meet rule ((M1.7a and (M1.7b or M1.7c)) and M1.7e)			
M1.7a	CT enclosed by M1 This rule is not applied for OCOVL covered region.	≥	0	μm
M1.7a ^[R]	CT enclosed by M1	≥	0.025	μm
M1.7b	M1 overlap past CT for two opposite sides with either side ≥0μm and <0.015μm	≥	0.025	μm
M1.7c	M1 overlap past CT for two opposite sides with either side ≥0.015μm	≥	0.015	μm

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M1.7d	(purposely blank)			
M1.7e	CT enclosed by M1(M1 width > 0.7 μm)	≥	0.03	μm
M1.8	M1 density (%) in 125 μm * 125 μm window with step size 62.5 μm	≥	10%	
M1.8a	M1 density (%) in 125 μm * 125 μm window with step size 62.5 μm	≤	85%	
M1.8b	M1 density difference (%) between any two 200μm adjacent windows (stepped without overlapping)	≤	50%	
M1.8c	M1 density (%) with 840 μm*840μm window	≤	70%	
M1.8d	M1 density over the whole chip	≥	20%	
M1.9	(M1 at 45 °) width (run length > 0 μm)	≥	0.17	μm
M1.10	(M1 at 45 °) space to parallel M1 (run length > 0 μm)	≥	0.17	μm
M1.11a	(purposely blank)			
M1.11b	(purposely blank)			
M1.11c	(purposely blank)			
M1.12	(purposely blank)			
M1.13	Space X between CT(in M1[A]) to adjacent M1[B] when M1[A] and M1[B] meet the following conditions: 1.M1[A] to adjacent M1[B] space S <= 0.08 μm 2. M1[A] width W > 0.12 μm 3. The projected parallel run length R of M1[A] to M1[B]. R > 0.27 μm Waive if there is redundant CT in the same {(M1[A] and AA intersection) or (M1[A] and GT intersection)} M1.13 is not applicable for SRAM area.	≥	0.085	μm
M1.14	Minimum M1 to M1 space S at M1 line-end. Width W < W0. The minimum space can be line end head to other M1 or line end side to other M1. Rule check: S >= (Dh or Ds). E1 = 0.02, K1=0.065, W0=0.09 μm, Dh=Ds=0.08 in the illustration. Schematic's Extension 1, Extension 2, and Extension 3: 1 Three extensions overlaps with other M1=> NG 2. When Extension 1 and one of the (extension 2 or extension 3) overlap with other M1. The remaining side extension's Ds need to size up from 0.08 to 0.11um. If this remaining extension interact with other M1(include touch edge), NG.	≥	0.08	μm

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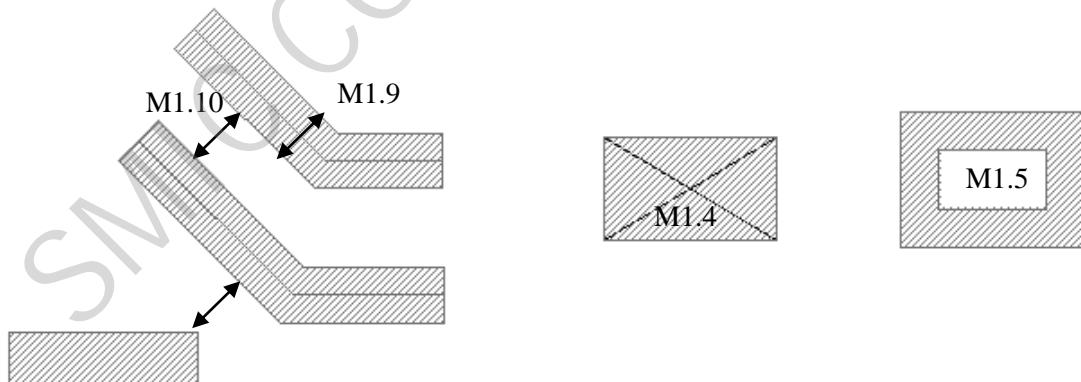
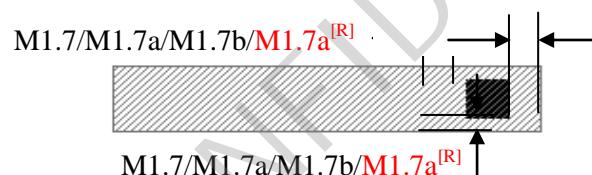
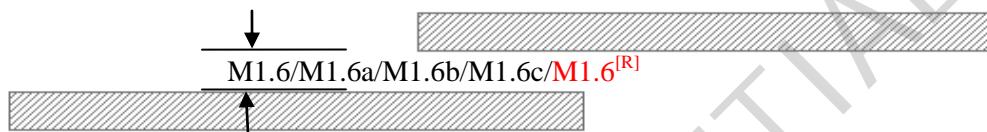
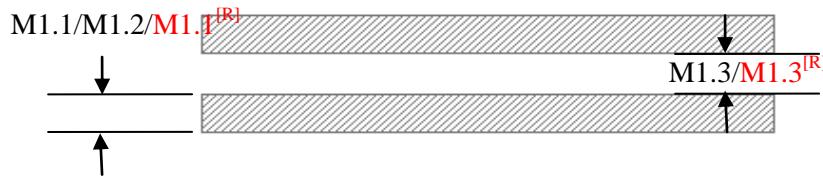
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	Outside of SRAM(INST) area. Waive extrusion F < 0.07. Only Highlight either one of the situations: 1) There is only one CT in the same {(M1[A] and AA intersection) or (M1[A] and GT intersection)} and CT space to M1[B] Sh < 0.10 μm. 2) there is only one V1 in the M1[A] and M2 intersection, and V1 space to M1[B] Sh < 0.10 μm			
M1.15	M1 density (including dummy). Density check window size: 80um*80um, step size 40um DRC only check the region with width of checking window \geq 40um	\geq	1%	
M1.16	Maximum M1 area of merged low density windows must follow item (1) and (2). The definition of low density window: window size 10um*10um, step size: 5um, density < 1% (1) Maximum area of merged low density window \leq 6500um ² , except merged low density windows width \leq 30um. (2) Maximum area of merged low density window \leq 18500um ² . DRC only check the region with width of (checking window NOT above excluding region) \geq 5um			

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M1



CT

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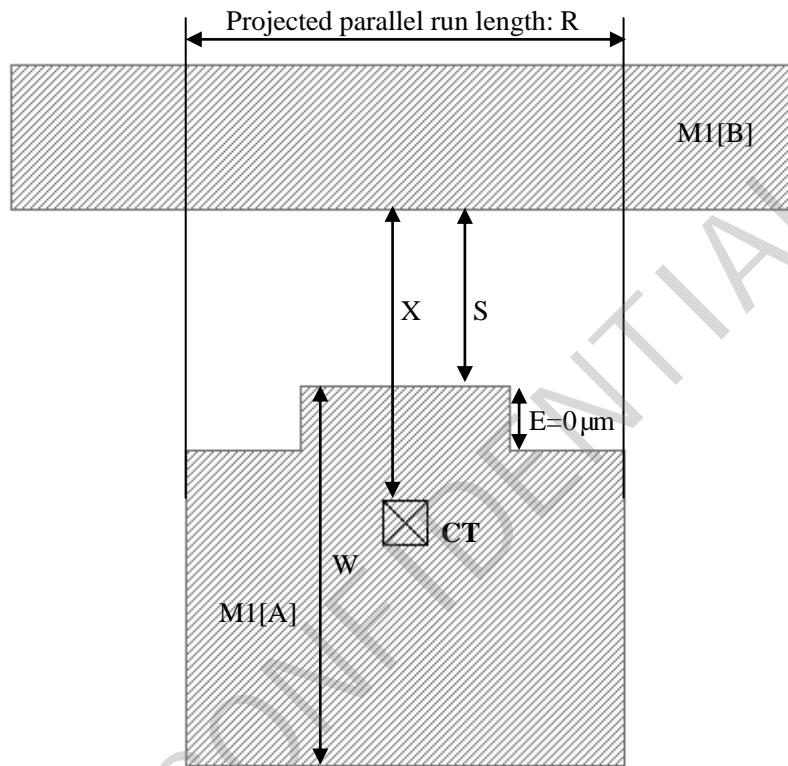
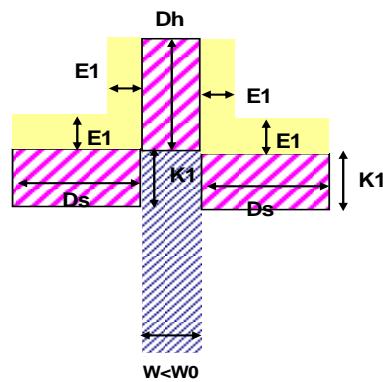
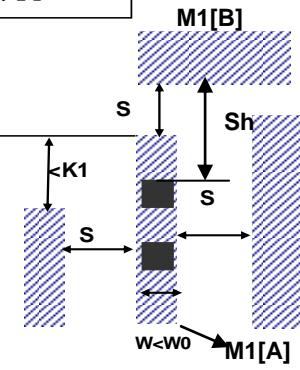


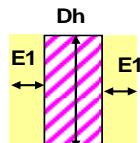
Figure for M1.13

Doc. No.: TD-LO40-DR-2001	Doc. Title: 40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 141/299
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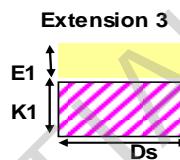
M1. 14



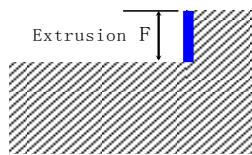
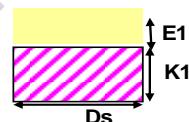
Extension 1



Extension 3



Extension 2



Extension 1, Extension 2, and Extension 3 cannot overlap with other M1 at the same time.

1. One extension overlaps with other M1 is ok.
2. Only Extension 2 and extension 3 overlap with other M1 is ok
3. Three extensions overlaps with other M1=> NG
4. When Extension 1 and one of the (extension 2 or extension 3) overlap with other M1. The remaining side extension's Ds need to size up from 0.08 to 0.11um. If this remaining extension interact with other M1(include touch edge), NG.

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7.4.17 Via 1 Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
V1.1	Fixed V1 size (square shape)	=	0.07	μm
V1.2	V1 space	≥	0.07	μm
V1.3	Space between V1s (with run length ≥ 0) at least two sides, when array equal to or greater than 3x3. Two Via areas whose space is within 0.10 μm are considered to be in the same array. An array does not have both row and column greater than or equal to 3 can apply smaller spacing “V1.2” instead of “V1.3”. (In a given via array, for via located at the corner or at the edge side of the via array, only need to check the inner side via to via spacing, since there are no via located at the outer side, which means via to via spacing is big enough to meet the V1.3 rule.)	≥	0.09	μm
V1.4	(purposely blank)			
V1.5	V1 (different net) (outside of SRAM) space for run length > 0μm	≥	0.10	μm
V1.5 ^[R]	V1 (different net) (outside of SRAM) space for run length > 0μm	≥	0.11	μm
V1.5a	V1 space in different net	≥	0.09	μm
V1.5b	(purposely blank)			
V1.6	V1 must be fully covered by M1 Per M1 and M2 intersection containing a V1, must meet rule V1.6a, V1.6b or V1.6c.			
V1.6a	V1 minimum within M1	≥	0.015	μm
V1.6b	M1 overlap past V1 for two opposite sides with either side ≥ 0.01 μm, and < 0.015 μm	≥	0.02	μm
V1.6c	M1 overlap past V1 for two opposite sides with either side ≥ 0 μm, and < 0.01 μm.	≥	0.03	μm
V1.6d	(purposely blank)			
V1.7	V1 must be fully covered by M2 Per M1 and M2 intersection containing a V1, must meet rule V1.7a, V1.7b or V1.7c.			
V1.7a	V1 minimum within M2	≥	0.015	μm
V1.7b	M2 overlap past V1 for two opposite sides with either side ≥ 0.01 μm, and < 0.015 μm	≥	0.02	μm
V1.7c	M2 overlap past V1 for two opposite sides with either side ≥ 0 μm, and < 0.01 μm.	≥	0.03	μm

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V1.7d	(purposely blank)			
V1.8	At least two V1 vias must connect M1 to M2 when the M1 or M2 width is > 0.26 μm . (This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM) OR RFSRAM) covered region)			
V1.9	At least three V1 vias must connect M1 to M2 when the M1 or M2 width is > 0.55 μm			
V1.10	At least four V1 vias must connect M1 to M2 when the M1 or M2 width is > 0.645 μm			
V1.11	(purposely blank)			
V1.12	(purposely blank)			
V1.13	(purposely blank)			
V1.14	(purposely blank)			
V1.15	(purposely blank)			
V1.16	At least two V1s with space $\leq 0.16 \mu\text{m}$ or three V1s with space $\leq 0.65 \mu\text{m}$ when one of M1 or M2 with both length and width $> 0.24 \mu\text{m}$. (exclude SRAM area to check)			
V1.17	At least two V1s when either wide metal of M1 or M2 with both length $L > 0.24 \mu\text{m}$ and width $W > 0.24 \mu\text{m}$, and the distance $D \leq 1.1 \mu\text{m}$ away from this wide metal. Exclude SRAM area to check.			
V1.17a	At least two V1s when either wide metal of M1 or M2 with both length $L > 1.4 \mu\text{m}$ and width $W > 1.4 \mu\text{m}$, and the distance $D \leq 2.8 \mu\text{m}$ away from this wide metal. Exclude SRAM area to check.			
V1.17b	At least two V1s when either wide metal of M1 or M2 with both length $L > 7 \mu\text{m}$ and width $W > 2.1 \mu\text{m}$, and the distance $D \leq 7.1 \mu\text{m}$ away from this wide metal. Exclude SRAM area to check.			
V1.18	45-degree rotated V1 is not allowed.			
V1.19	Single V1 is not allowed in "H-shape" M2 when: 1. The M2 has "H-shape" interact with two metal holes: both two metal holes length $\leq 4.5 \mu\text{m}$ (L_2) and two metal hole area $\leq 4.5 \mu\text{m}^2$. 2. The V1 overlaps on the center metal bar of this "H-shape" M2. 3. The center metal bar length $\leq 1 \mu\text{m}$ (L) and the metal bar width $\leq 0.2 \mu\text{m}$.			

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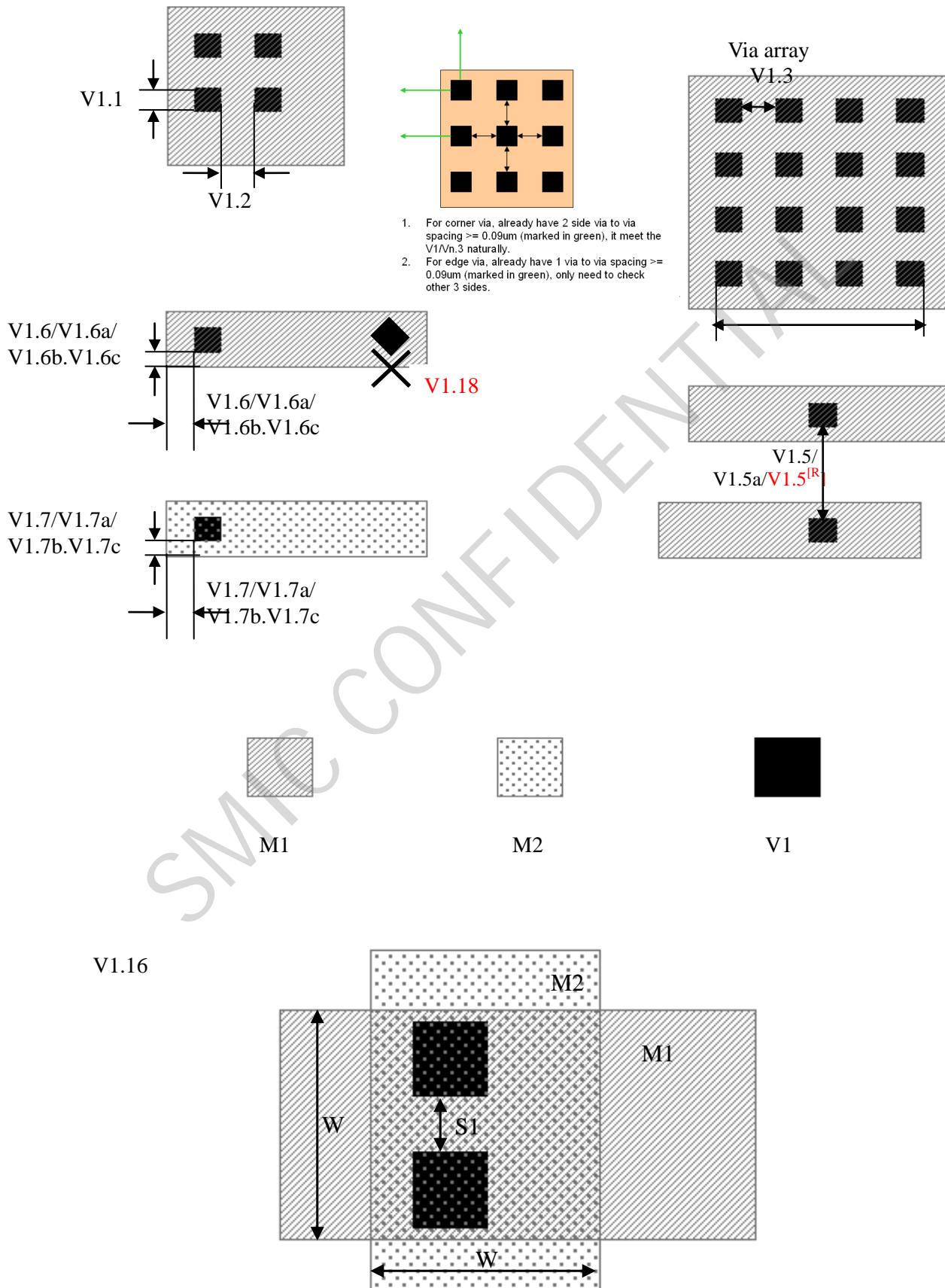


Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 144/299
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V1.20	V1 connected to M1DUM, M2DUM is not allowed. This rule is not applied for LOGO covered region.			
V1.21	V1 must be fully covered by M1 and M2.			
V1.22	It's not allowed V1 overlap with M1 and M2 resistor. M1 resistor definition: (M1 AND M1R). M2 resistor definition: (M2 AND M2R).			

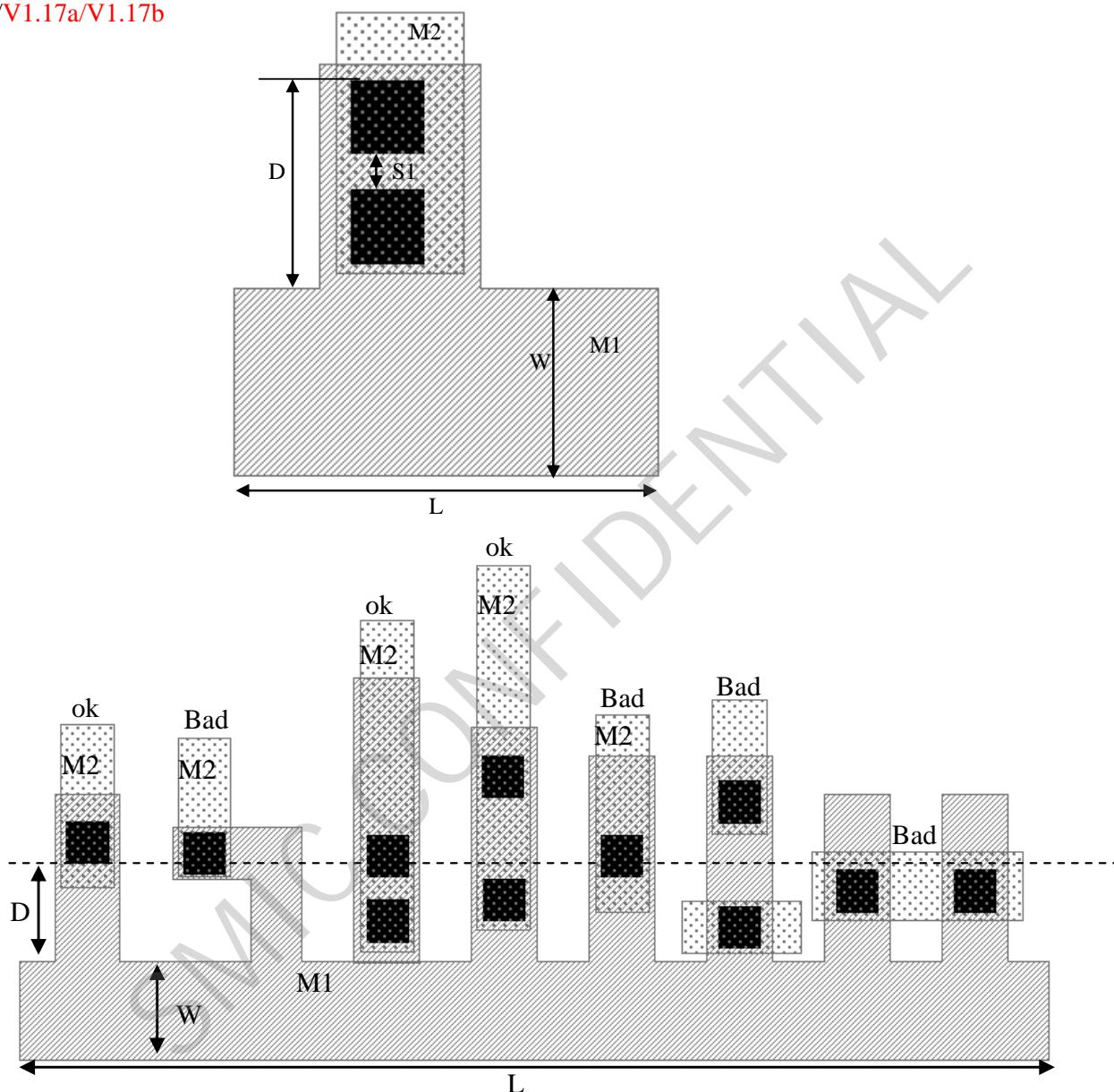
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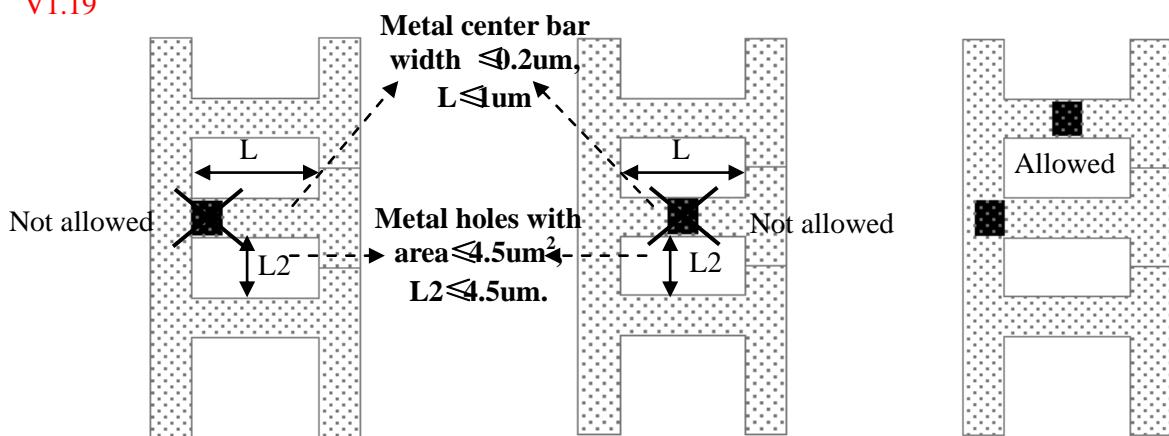


Doc. No.: TD-LO40-DR-2001	Doc. Title: 40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 146/299
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V1.17/V1.17a/V1.17b



V1.19



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7.4.18 Metal n (n=2~8) Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
Mn.1	Mn width.	≥	0.07	μm
Mn.1 ^[R]	Mn width.	≥	0.08	μm
Mn.2	Mn width. When Mn used for TM-1, DRC waive the (Mn AND DUPMK1) region.	≤	4.5	μm
Mn.3	Mn space	≥	0.07	μm
Mn.3 ^[R]	Mn space	≥	0.08	μm
Mn.4	Mn area (For n=2, The INST connected area apply SRAM design rule)	≥	0.0196	μm ²
Mn.5	Mn enclosed area	≥	0.2	μm ²
Mn.6	Space between two (run length > 0.3 μm) parallel metal lines with both metal line width is > 0.22 μm.	≥	0.1	μm
Mn.6 ^[R]	Space between two (run length > 0.3 μm) parallel metal lines with one or both metal line width is > 0.22 μm.	≥	0.12	μm
Mn.6a	Space between two (run length > 0.6 μm) parallel metal lines with one or both metal line width is > 0.7 μm.	≥	0.12	μm
Mn.6b	Space between two (run length > 0.6 μm) parallel metal lines with one metal line width is > 0.22 μm and other metal line width is >0.7 μm.	≥	0.14	μm
Mn.6c	Space between two (run length > 1.5 μm) parallel metal lines with one or both metal lines width is > 1.5 μm	≥	0.3	μm
Mn.7	Mn density (%) in 125 μm x 125 μm window with step size 62.5 μm	≥	10%	
Mn.7a	Mn density (%) in 125 μm x 125 μm window with step size 62.5 μm	≤	85%	
Mn.7b	Mn density difference (%) between any two 200μm adjacent windows (stepped without overlapping)	≤	50%	
Mn.7c	Mn density (%) with 840μm*840 μm window	≤	70%	
Mn.7d ^[R]	[(Mn with width > 2.8μm) over M(n-1)] density (%) with 200μm*200 μm step size 100 μm where n = 2-8 and (n-1) = metal level below.	≤	70%	
Mn.7e ^[R]	[M(n + 1) over [Mn with width > 2.8μm] density (%) with 200μm*200 μm step size 100 μm, where n = 1-7 and n + 1 = metal level above	≤	70%	
Mn.7f	Mn density over the whole chip	≥	20%	
Mn.8	45 °Mn width	≥	0.17	μm
Mn.9	(Mn at 45 ° space to parallel Mn (run length > 0 μm)	≥	0.17	μm
Mn.10a	(purposely blank)			
Mn.10b	(purposely blank)			

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Rules number	DESCRIPTION	Operation	Design Value	Unit
Mn.10c	(purposely blank)			
Mn.11	<p>Space S_h between V_{n-1} (V_{n-1} is enclosed by $Mn[A]$) to neighbouring metal line $Mn[B]$, when the layout structures meet the following conditions:</p> <ol style="list-style-type: none"> 1. $Mn[A]$ line end definition: line width $W < 0.1 \mu m$. 2. V_{n-1} enclosure by $Mn[A]$ line end: $E < 0.05 \mu m$ 3. The parallel run length of $Mn[A]$ and $Mn[B]$: $\geq -0.03 \mu m$ 4. Space S_s between $Mn[A]$ to the neighbouring parallel metal line: $S_s < 0.08 \mu m$; 5. Any one edge distance from the corner of the two edges of $Mn[A]$: $< 0.095 \mu m$ <p>At least one V_{n-1} in the $Mn[A]$ and $Mn[B]$ intersection meet this rule is ok.</p> <p>This rule is not applicable for SRAM region DRC check.</p> <p>Rule check:</p> <p>$S_h \geq Dh$, $S_s < Ds$, $E1 = 0.03$, $K1 = 0.095$, $Dh=0.12$, $Ds = 0.08$ in the illustration</p> <p>Waive extrusion $F < 0.07$.</p>	\geq	0.12	μm
Mn.12 ^[R]	<p>Minimum Mn to Mn space S at Mn line-end. Width $W < 0.1 \mu m$. The minimum space can be line end head to other Mn or line end side to other Mn. Rule check:</p> <p>$S \geq (Dh \text{ or } Ds)$. $E1 = 0.03$, $K1=0.095$, $Dh=Ds=0.1$ in the illustration.</p> <p>Outside of SRAM (INST) area.</p> <p>Waive extrusion $F < 0.07$.</p> <p>Waive the violation for MOM (within MOMDMY).</p>	\geq	0.1	μm
Mn.13 ^[R]	<p>It is not allowed to have local density $> 85\%$ of all 3 consecutive metal ($M1/Mn$, $Mn+1$ and $Mn+2$) over any window size $62.5*62.5\mu m$ (stepping size $31.25\mu m$).</p> <ul style="list-style-type: none"> a) The metal layers include $M1/Mn$ and dummy metals. b) This rule doesn't check DUMB, MARKS and (TM2 and PA) region. 			
Mn.14	<p>Mn density (including dummy). Density check window size: $80\mu m * 80\mu m$, step size $40\mu m$.</p> <p>DRC only check the region with width of checking window $\geq 40\mu m$.</p>	\geq	1%	
Mn.15	<p>Maximum Mn area of merged low density windows must follow item (1) and (2).</p> <p>The definition of low density window: window size $10\mu m * 10\mu m$, step size: $5\mu m$, density $< 1\%$.</p> <p>(1) Maximum area of merged low density window $\leq 6500\mu m^2$, except merged low density windows width $\leq 30\mu m$.</p> <p>(2) Maximum area of merged low density window $\leq 18500\mu m^2$. DRC only check the region with width of (checking window NOT above excluding region) $\geq 5\mu m$.</p>			
Mn.16	It is not allowed to have local density $< 5\%$ of all 3 consecutive			

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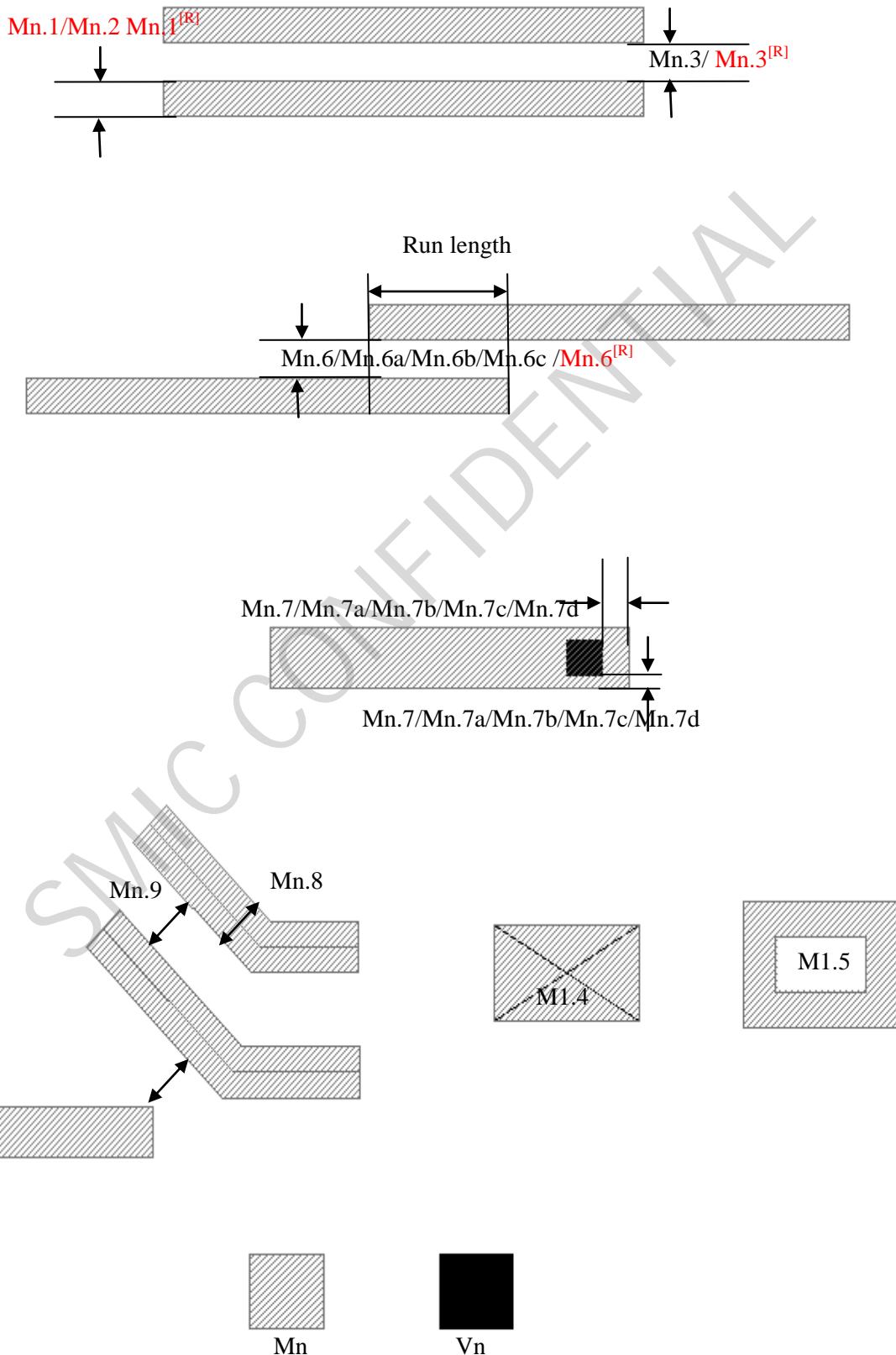


Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 149/299
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Rules number	DESCRIPTION	Operation	Design Value	Unit
	<p>metal (M1/Mn, Mn+1 and Mn+2) over any window 30*30um (stepping 15um).The metal layers include M1/Mn and dummy metals.</p> <p>DRC only check the region with width of (checking window NOT above excluding region) \geq 15um.</p>			

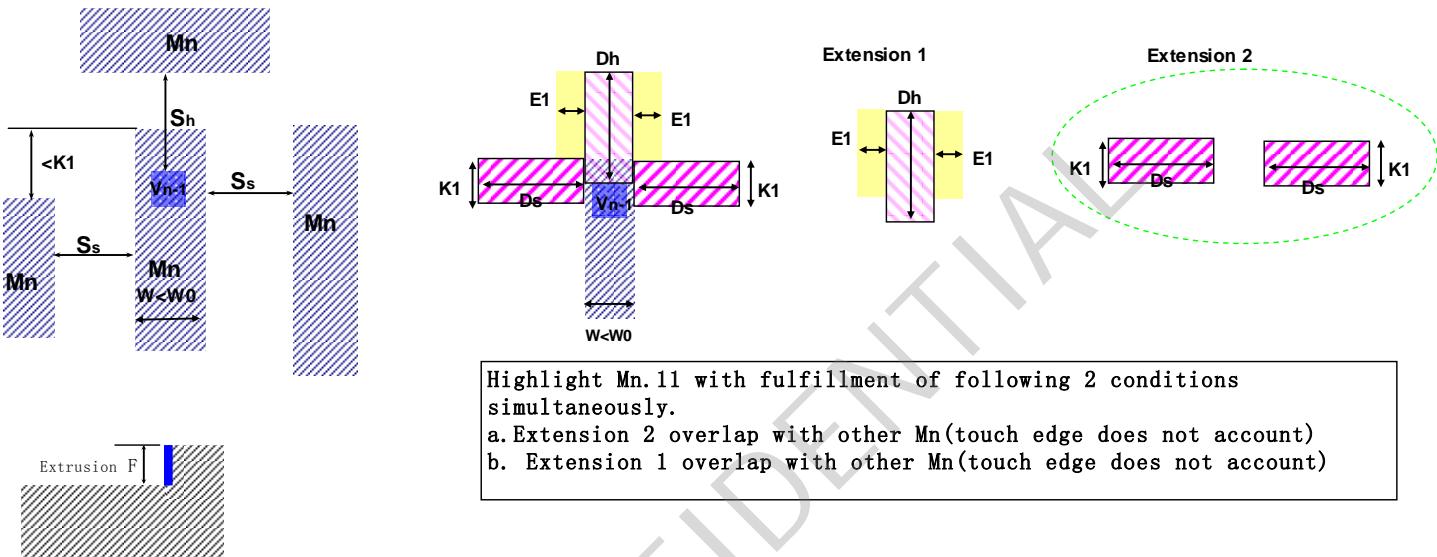
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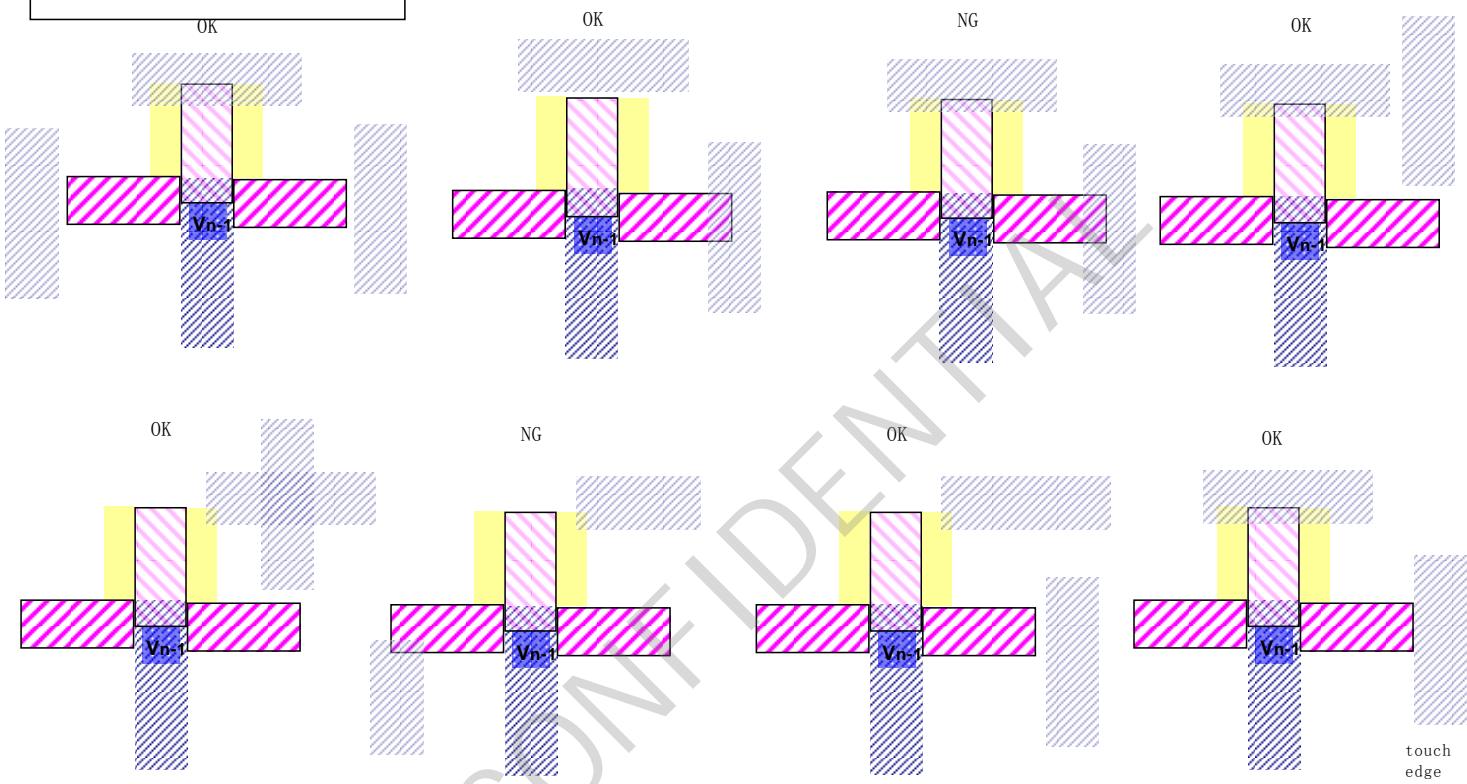
Doc. No.: TD-LO40-DR-2001	Doc. Title: 40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 151/299
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Mn. 11

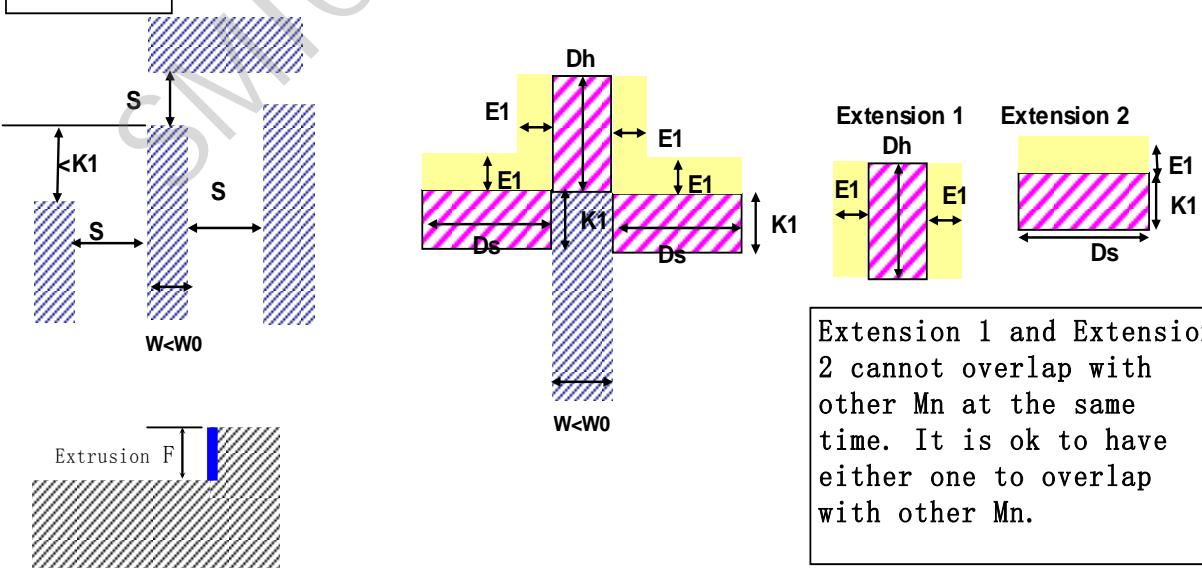


Doc. No.: TD-LO40-DR-2001	Doc. Title: 40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 152/299
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Mn. 11 explanation samples



Mn. 12



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7.4.19 Vian (n=2~7) Rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
Vn.1	Vn exact length and width	=	0.07	μm
Vn.2	Vn space	≥	0.07	μm
Vn.3	Space between Vns (with run length ≥ 0) at least two least two sides, when array equal to or greater than 3x3. Two Via areas whose space is within 0.10 μm are considered to be in the same array. An array does not have both row and column greater than or equal to 3 can apply smaller spacing “Vn.2” instead of “Vn.3”. (In a given via array, for via located at the corner or at the edge side of the via array, only need to check the inner side via to via spacing, since there are no via located at the outer side, which means via to via spacing is big enough to meet the Vn.3 rule.)	≥	0.09	μm
Vn.4	(purposely blank)			
Vn.5	Vn space in different net for run length $>0\mu m$ (outside of SRAM)	≥	0.10	μm
Vn.5^[R]	Vn space in different net for run length$>0\mu m$ (outside of SRAM)	≥	0.11	μm
Vn.5a	Vn space in different net	≥	0.09	μm
Vn.5b	(purposely blank)			
Vn.6	Vn must be fully covered by within Mn Per Mn and Mn+1 intersection containing a Vn, must meet rule Vn.6a, Vn.6b or Vn.6c.			
Vn.6a	Vn minimum within Mn	≥	0.015	μm
Vn.6b	Mn overlap past Vn for two opposite sides with either side $\geq 0.01\mu m$, and $< 0.015\mu m$	≥	0.02	μm
Vn.6c	Mn overlap past Vn for two opposite sides with either side $\geq 0\mu m$, and $< 0.01\mu m$	≥	0.03	μm
Vn.6d	(purposely blank)			
Vn.7	Vn must be fully covered by within Mn+1 Per Mn and Mn+1 intersection containing a Vn, must meet rule Vn.7a, Vn.7b or Vn.7c.			



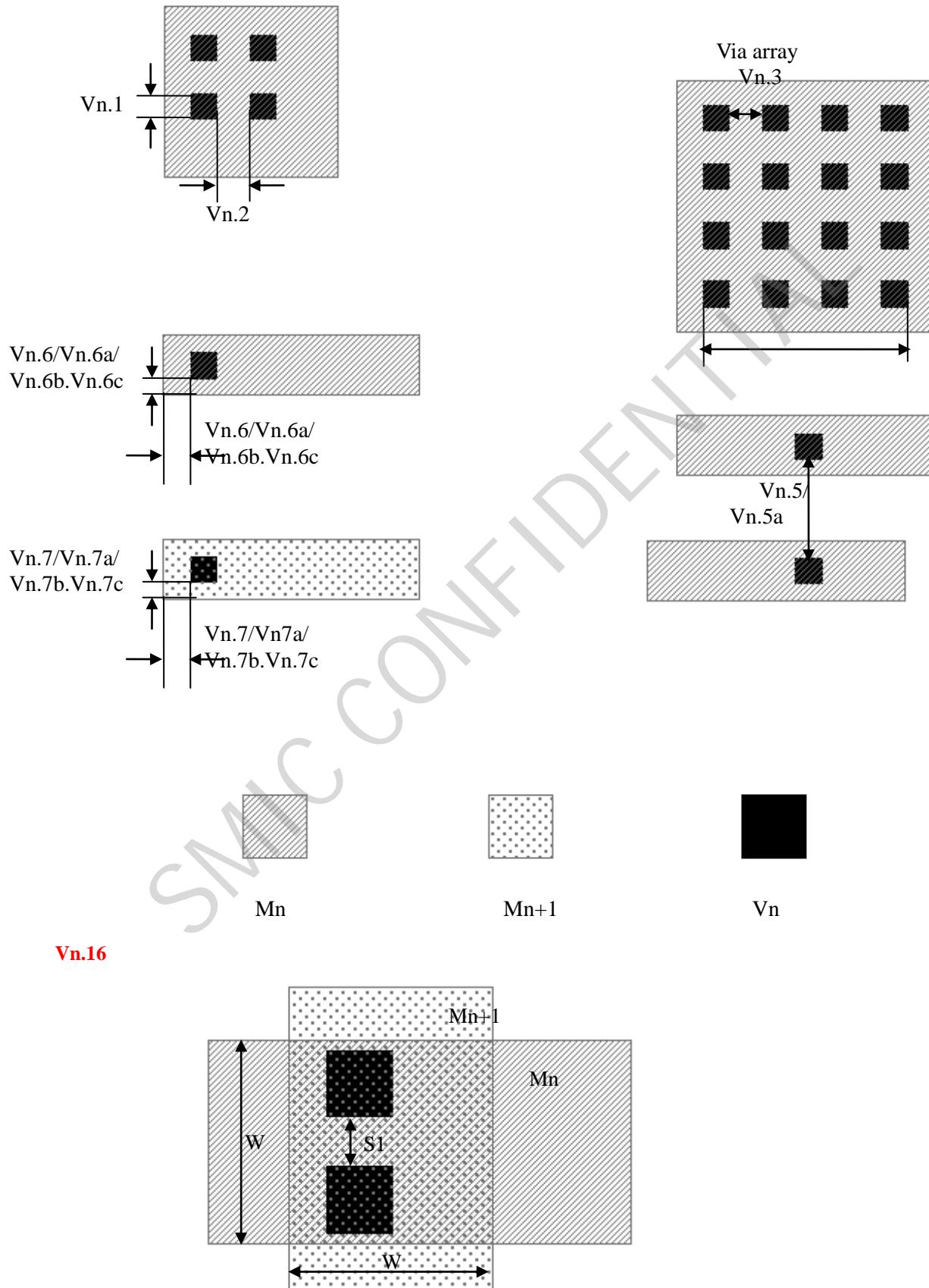
Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 154/299
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Vn.7a	Vn minimum within Mn+1	≥	0.015	μm
Vn.7b	Mn+1 overlap past Vn for two opposite sides with either side ≥0.01 μm, and < 0.015 μm	≥	0.02	μm
Vn.7c	Mn+1 overlap past Vn for two opposite sides with either side ≥0 μm, and < 0.01 μm	≥	0.03	μm
Vn.7d	(purposely blank)			
Vn.8	At least two Vns must connect Mn to M(n + 1) when the Mn or M(n + 1) width is > 0.26μm			
Vn.9	At least three Vns must connect Mx to M(n + 1) when the Mn or M(n + 1) width is > 0. 55μm,			
Vn.10	At least four Vn vias must connect Mn to M(n + 1) when the Mn or M(n + 1) width is > 0.645 μm			
V1.11	(purposely blank)			
V1.12	(purposely blank)			
V1.13	(purposely blank)			
V1.14	(purposely blank)			
V1.15	(purposely blank)			
Vn.16	At least two Vns with space <=0.16 μm or three Vns with space <= 0.65um when one of Mn or Mn+1 with both length and width >0.24 μm. Exclude SRAM area to check.			
Vn.17	At least two Vns when either wide metal of Mn or Mn+1 with both length L>0.24 μm and width W>0.24 μm, and the distance D<=1.1 μm away from this wide metal. Exclude SRAM area to check.			
Vn.17a	At least two Vns when either wide metal of Mn or Mn+1 with both length L>1.4 μm and width W>1.4 μm, and the distance D<=2.8 μm away from this wide metal. Exclude SRAM area to check.			
Vn.17b	At least two Vns when either wide metal of Mn or Mn+1 with both length L>7 μm and width W>2.1 μm, and the distance D<=7.1 μm away from this wide metal. Exclude SRAM area to check.			

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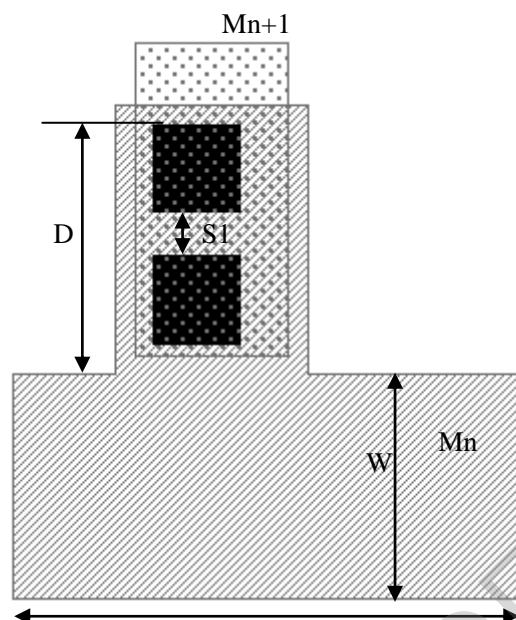
Vn.18	45-degree rotated Vn is not allowed.			
Vn.19	Single Vn is not allowed in "H-shape" Mn+1 when: 1. The Mn+1 has "H-shape" interact with two metal holes: both two metal holes length $\leq 4.5\text{um}$ (L2) and two metal hole area $\leq 4.5\text{um}^2$. 2. The Vn overlaps on the center metal bar of this "H-shape" Mn+1. 3. The center metal bar length $\leq 1\text{um}$ (L) and the metal bar width $\leq 0.2\text{um}$.			
Vn.20	Vn connected to MnDUM, Mn+1 Dummy is not allowed. This rule is not applied for LOGO covered region.			
Vn.21	Vn must be fully covered by Mn and Mn+1.			
Vn.22 ^[R]	Via (Vn, TV1) insertion, n=1~7. Insert one Vn if single Vn and (Wn \geq =5Wn+1, or Wn+1 \geq =5Wn) at enclosure. (Reference condition is continuous heating 168hours, and temperatures 200°C,.)			
Vn.23 ^[R]	At least two vias (Vn, TV1, TV2, n=1~7) in Mn and Mn+1 (M1, Mn, n=2~8, TM1, TM2) intersection area. (This rule is not applicable for SRAM region, but SRAM region should follow main rule: V1.17, Vn.17, TV1.13, TV2.13, TV2.14)			
Vn.24	It's not allowed Vn overlap with Mn and Mn+1 resistor. Mn resistor definition: (Mn AND MnR). Mn+1 resistor definition: (Mn+1 AND Mn+1R).			

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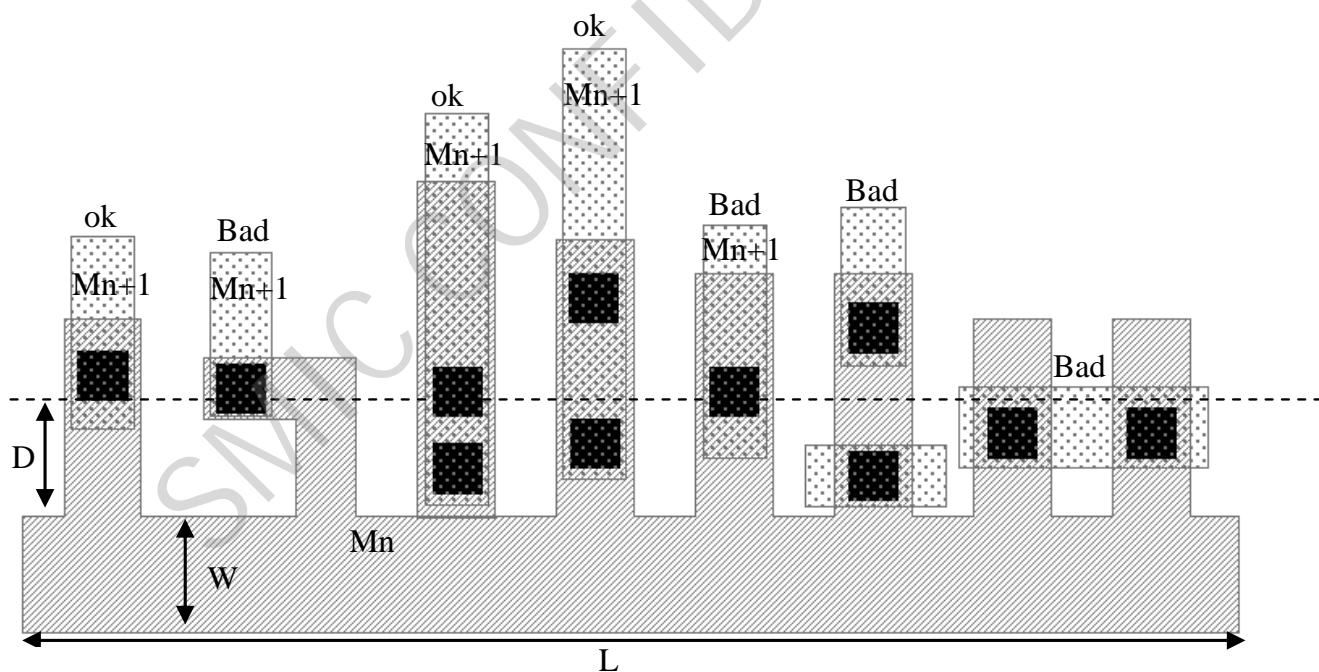


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Vn.17



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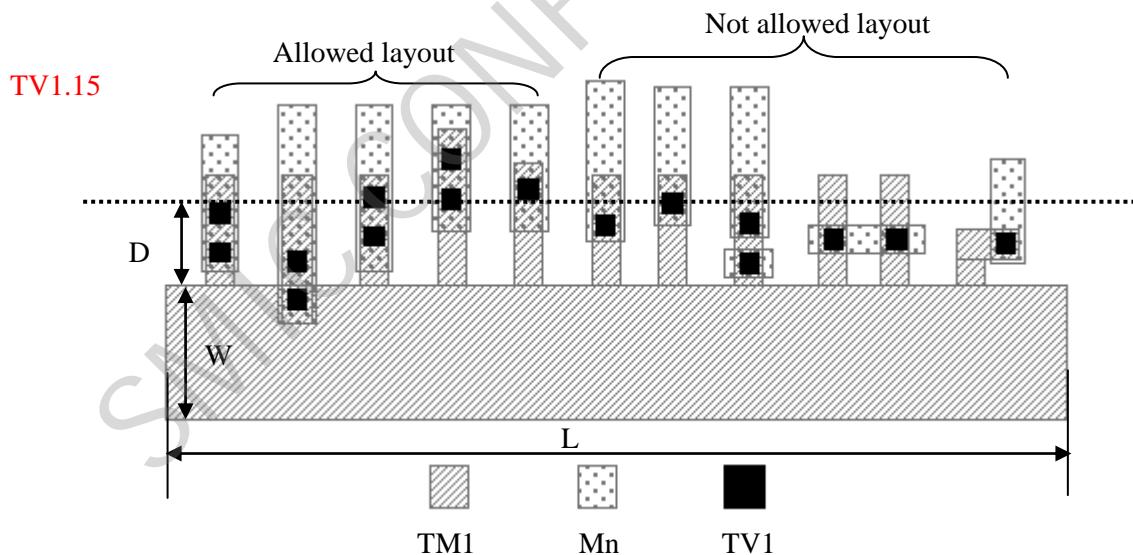
Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 158/299
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7.4.20 TV1 Rules (top via 1)

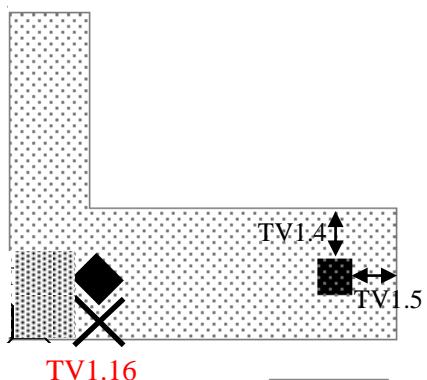
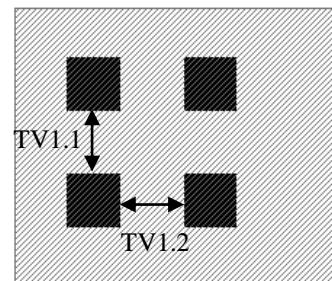
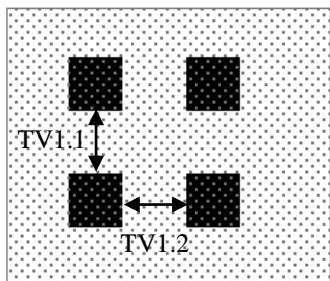
Rules number	DESCRIPTION	Operation	Design Value	Unit
TV1.1	Fixed TV1 size (square shape)	=	0.36	μm
TV1.2	Space between two TV1s	≥	0.34	μm
TV1.3	Space between top vias, in case TV1 array is larger than or equal to 3x3. Two Via areas whose space is within 0.56 μm are considered to be in the same array. An array does not have both row and column greater than or equal to 3 can apply smaller spacing “TV1.2” instead of “TV1.3”.	≥	0.50	μm
TV1.4	TV1 enclosure by Mn. Mn is Metal layer directly underneath TV1	≥	0.01	μm
TV1.5	TV1 enclosure by Mn at least two opposite sides. Mn is Metal layer directly underneath TV1	≥	0.05	μm
TV1.6	(purposely blank)			
TV1.7	(purposely blank)			
TV1.8	(purposely blank)			
TV1.9	(purposely blank)			
TV1.10	(purposely blank)			
TV1.11	(purposely blank)			
TV1.12	(purposely blank)			
TV1.13	At least 2 TV1 connect Mx to TM1 intersection area if either TM1 or Mx width>1.8 μm			
TV1.14	(purposely blank)			
TV1.15	At least two TV1s when either wide metal of Mn or TM1 with both length L>10 μm and width W>3 μm, and the distance D<=5 μm away from this wide metal. Exclude SRAM area to check.			
TV1.16	45-degree rotated TV1 is not allowed.			

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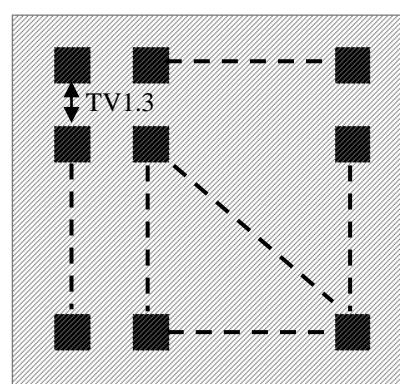
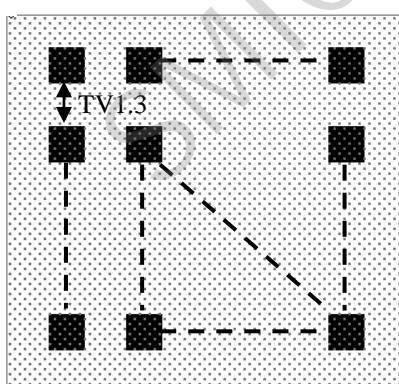
TV1.17	TV1 connected to MnDUM, TM1DUM is not allowed. This rule is not applied for LOGO covered region.			
TV1.18	TV1 must be fully covered by Mn and TM1.			
TV1.19	It's not allowed TV1 overlap with Mn and TM1 resistor. Mn resistor definition: (Mn AND MnR). TM1 resistor definition: (TM1 AND TM1R).			



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TV1.16



TM1



Mn



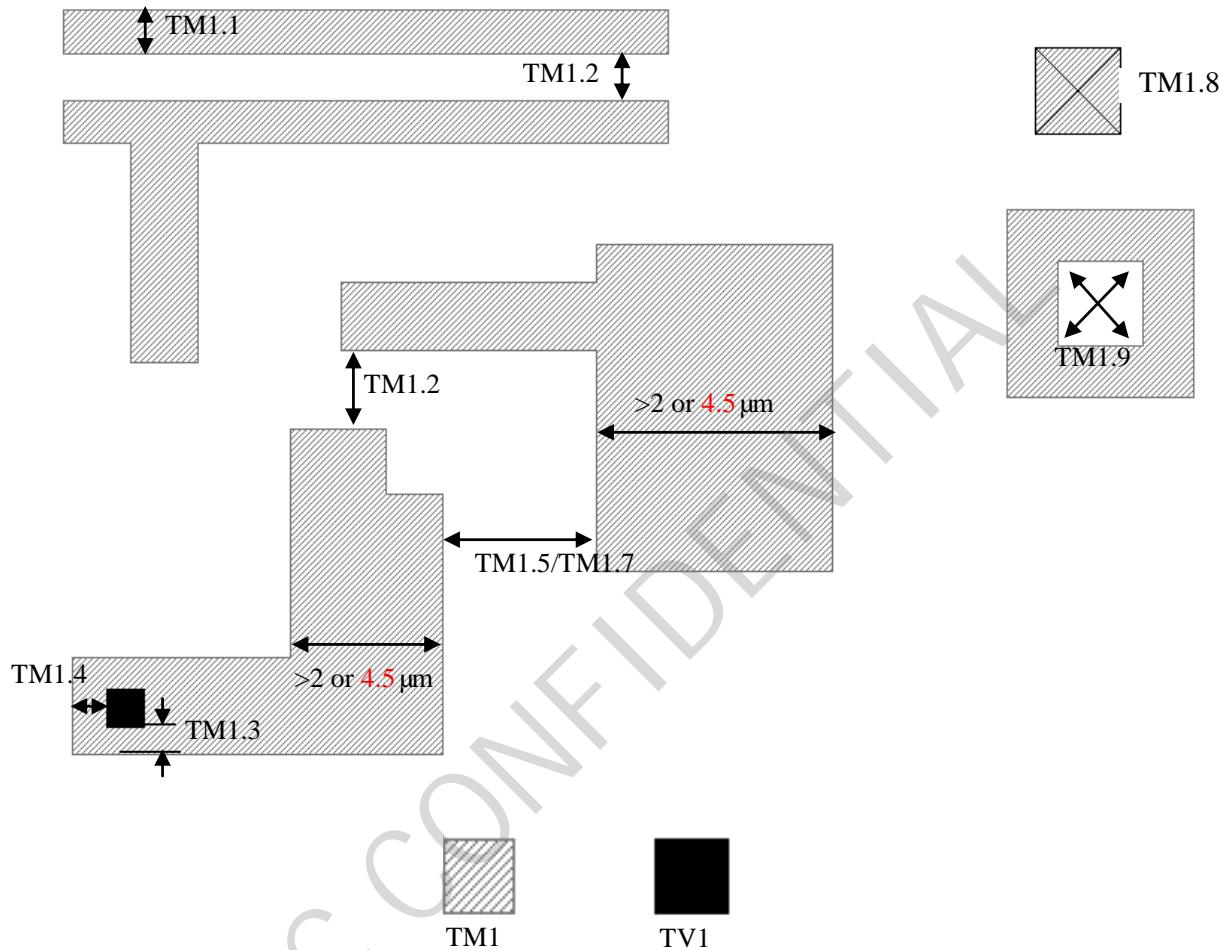
TV1

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7.4.21 TM1 Rules (top metal 1)

Rules number	DESCRIPTION	Operation	Design Value	Unit
TM1.1	TM1 width	\geq	0.40	μm
TM1.2	Space between two TM1s	\geq	0.40	μm
TM1.3	TV1 enclosure by TM1	\geq	0.020	μm
TM1.4	Extension of TM1 line end outside of TV1	\geq	0.030	μm
TM1.5	Space between two length $> 1.5 \mu\text{m}$ parallel metal lines with one or both metal line width is $> 2 \mu\text{m}$.	\geq	0.500	μm
TM1.6	(purposely blank)			
TM1.7	Space between two length $> 4.5 \mu\text{m}$ parallel metal lines with one or both metal line width is $> 4.5 \mu\text{m}$	\geq	1.2	μm
TM1.8	TM1 area	\geq	0.56	μm^2
TM1.9	Enclosed dielectric area by TM1	\geq	0.78	μm^2
TM1.10	Dummy pattern is required in case TM1 density is less than 20%. Density check window: Window size: $200 \mu\text{m} \times 200 \mu\text{m}$, step size: $100 \mu\text{m}$ (INDMY or MARKG or MARKS) are excluded for this rule check	\geq	15%	
		\leq	85%	
TM1.10a	TM1 density over the whole chip	\geq	20%	
TM1.11	TM1 density with $840 \mu\text{m} \times 840 \mu\text{m}$ area	\leq	70%	
TM1.12	TM1 density difference between 2 adjacent $200 \mu\text{m} \times 200 \mu\text{m}$ area	\leq	50%	
TM1.13	TM1 line width; This rule is not applicable for TM1 underneath of MD opening region.	\leq	12	μm

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7.4.22 TV2 Rules (top via 2)

Rules number	DESCRIPTION	Operation	Design Value	Unit
TV2.1	Fixed TV2 size (square shape)	=	0.360	μm
TV2.2	Space between two TV2s	≥	0.34	μm
TV2.3	Space between top vias, in case TV2 array is larger than or equal to 3x3. Two Via areas whose space is within 0.56 μm are considered to be in the same array. An array does not have both row and column greater than or equal to 3 can apply smaller spacing “TV2.2” instead of “TV2.3”.	≥	0.50	μm
TV2.4	TV2 enclosure by TM1/Mn, where TM1/Mn is the Metal layer directly underneath TV2	≥	0.01	μm
TV2.5	TV2 enclosure by TM1/Mn at least two opposite sides, where TM1/Mn is the metal layer directly underneath TV2.	≥	0.05	μm
TV2.6	(purposely blank)			
TV2.7	(purposely blank)			
TV2.8	(purposely blank)			
TV2.9	(purposely blank)			
TV2.10	(purposely blank)			
TV2.11	(purposely blank)			
TV2.12	(purposely blank)			
TV2.13	At least 2 TV2 within TM1 and TM2 intersection area. One of the TMx width > 1.8 μm. x = 1, 2			
TV2.14	For TM2 without TM1, and TV2 landing on the highest inter-metal Mx, at least 2 TV2 connect Mx to TM2 intersection area, if either TM2 or Mx width > 1.8 μm			
TV2.15	At least two TV2s when either wide metal of TM1 or TM2 with both length L>10 μm and width W>3 μm, and the distance D<=5 μm away from this wide metal. Exclude SRAM area to check.			
TV2.16	45-degree rotated TV2 is not allowed.			
TV2.17	TV2 connected to TM1DUM/MnDUM or TM2DUM/MTT2DUM is not allowed, where TM1DUM/MnDUM is the metal layer directly underneath TV2.			

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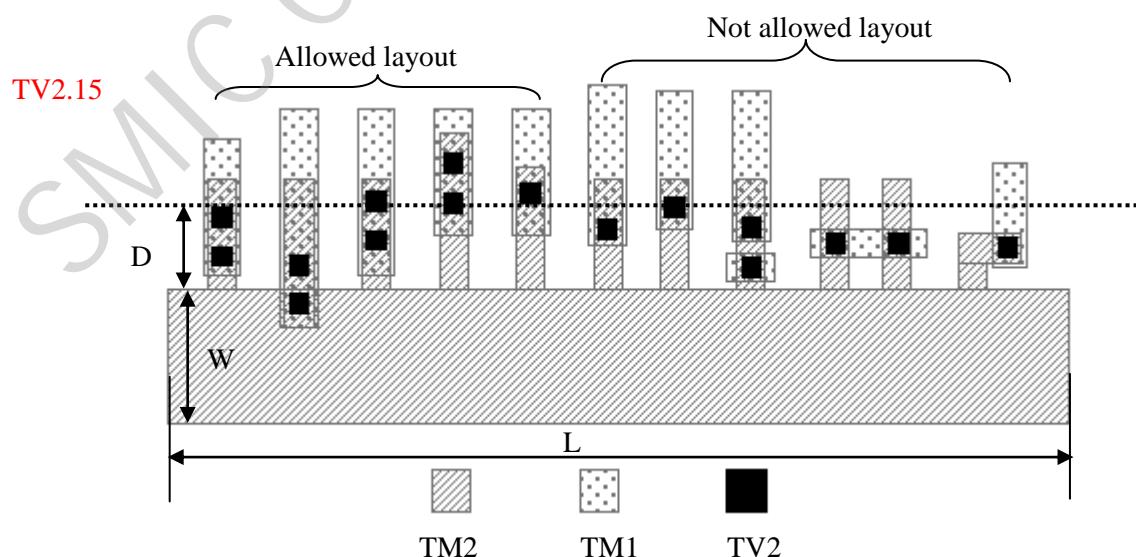
According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:1

2008-06-27

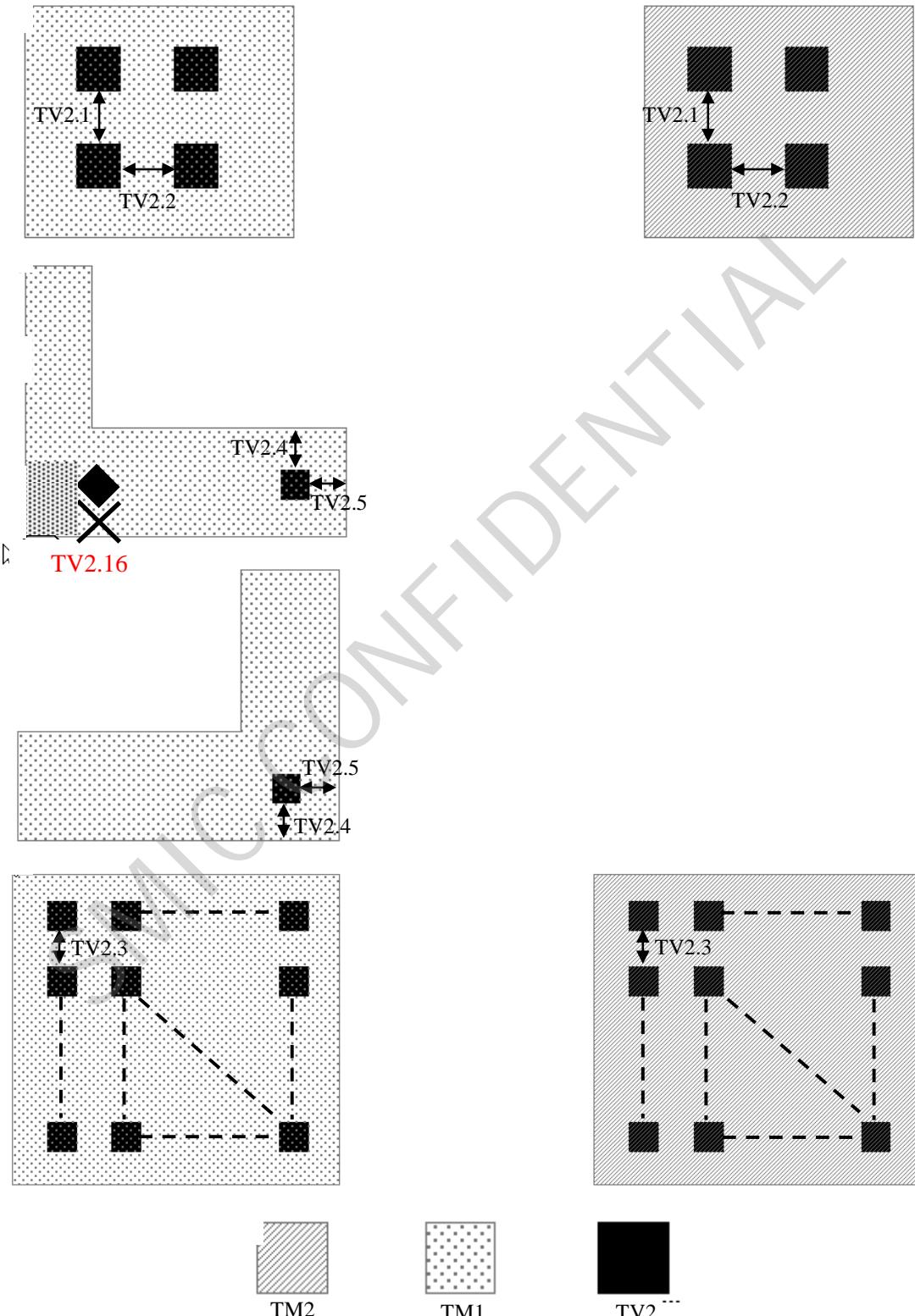
Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 164/299
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	This rule is not applied for LOGO covered region.			
TV2.18	TV2 must be fully covered by TM1/Mn and TM2/MTT2, where TM1/Mn is the metal layer directly underneath TV2.			
TV2.19	<p>It's not allowed TV2 overlap with Mn/TM1 resistor when Mn/TM1 directly underneath TV2. And It's not allowed TV2 overlap with TM2/MTT2 resistor when TM2/MTT2 directly above TV2.</p> <p>Mn resistor definition: (Mn AND MnR).</p> <p>TM1 resistor definition: (TM1 AND TM1R).</p> <p>TM2 resistor definition: (TM2 AND TM2R).</p> <p>MTT2 resistor definition: (MTT2 AND TM2R)</p>			

Note: For reposition process from Mn to TV2, the TV2 enclosure size by Mn should follow rule TV1.5.



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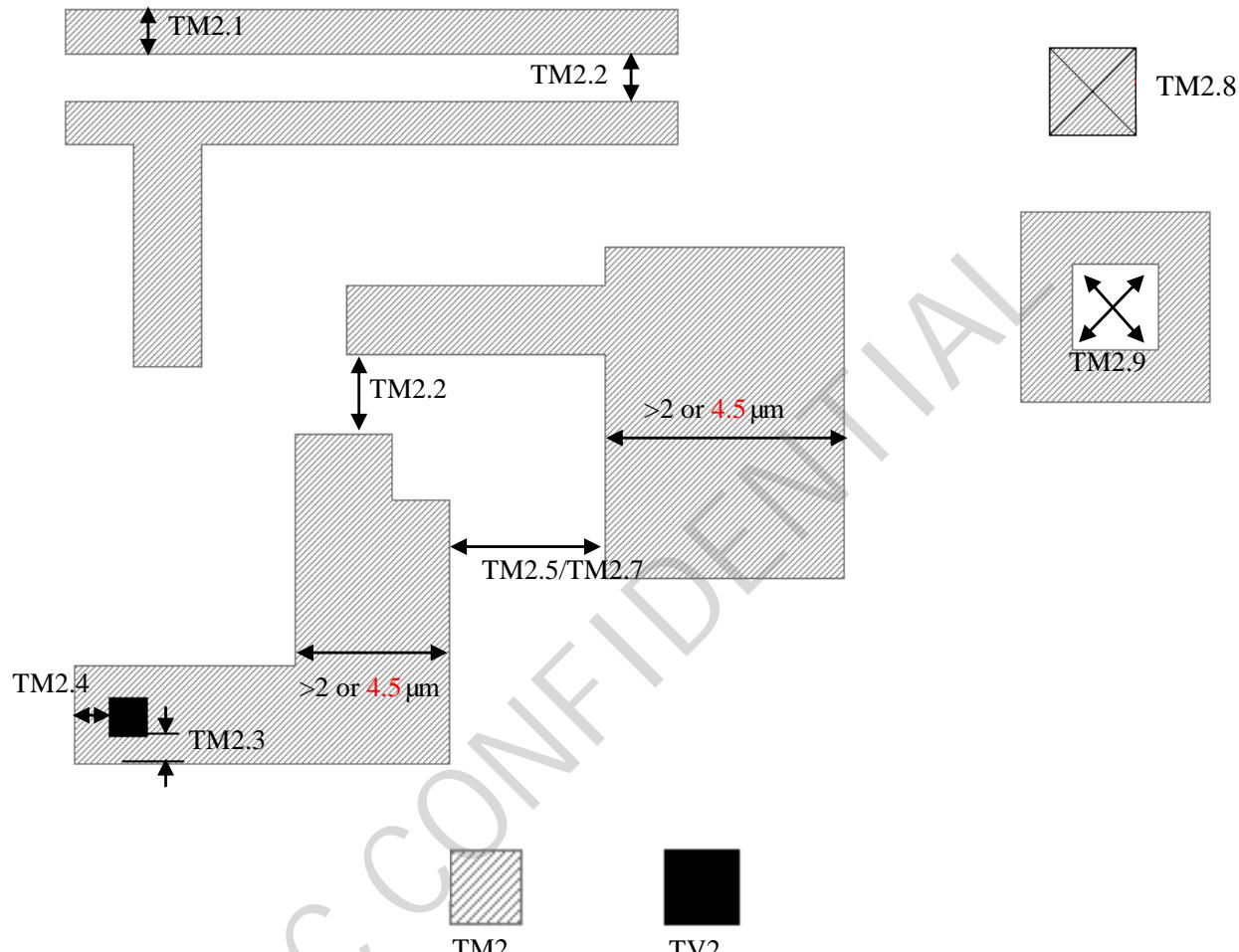


Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 166/299
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7.4.23 TM2 Rules (top metal 2): TM2 rule for connection

Rules number	DESCRIPTION	Operation	Design Value	Unit
TM2.1	TM2 width	\geq	0.40	μm
TM2.2	Space between two TM2s	\geq	0.40	μm
TM2.3	TV2 enclosure by TM2	\geq	0.020	μm
TM2.4	Extension TM2 line end outside TV2	\geq	0.030	μm
TM2.5	Space between two length $> 1.5 \mu\text{m}$ parallel metal lines with one or both metal line width is $> 2 \mu\text{m}$.	\geq	0.500	μm
TM2.6	(purposely blank)			
TM2.7	Space between two length $> 4.5 \mu\text{m}$ parallel metal lines with one or both metal line width is $> 4.5 \mu\text{m}$.	\geq	1.2	μm
TM2.8	TM2 area	\geq	0.56	μm^2
TM2.9	Enclosed dielectric area by TM2	\geq	0.78	μm^2
TM2.10	Dummy pattern is required in case TM2 density is less than 20%. Density check window: Window size: $200 \mu\text{m} \times 200 \mu\text{m}$, step size: $100 \mu\text{m}$ (INDMY or MARKG or MARKS) are excluded for this rule check	\geq	15%	
		\leq	85%	
TM2.10a	TM2 density over the whole chip	\geq	20%	
TM2.11	TM2 density difference between 2 adjacent $200 \mu\text{m} \times 200 \mu\text{m}$ area	\leq	50%	
TM2.12	TM2 line width. This rule is not applicable for TM2 underneath of MD opening region.	\leq	12	μm

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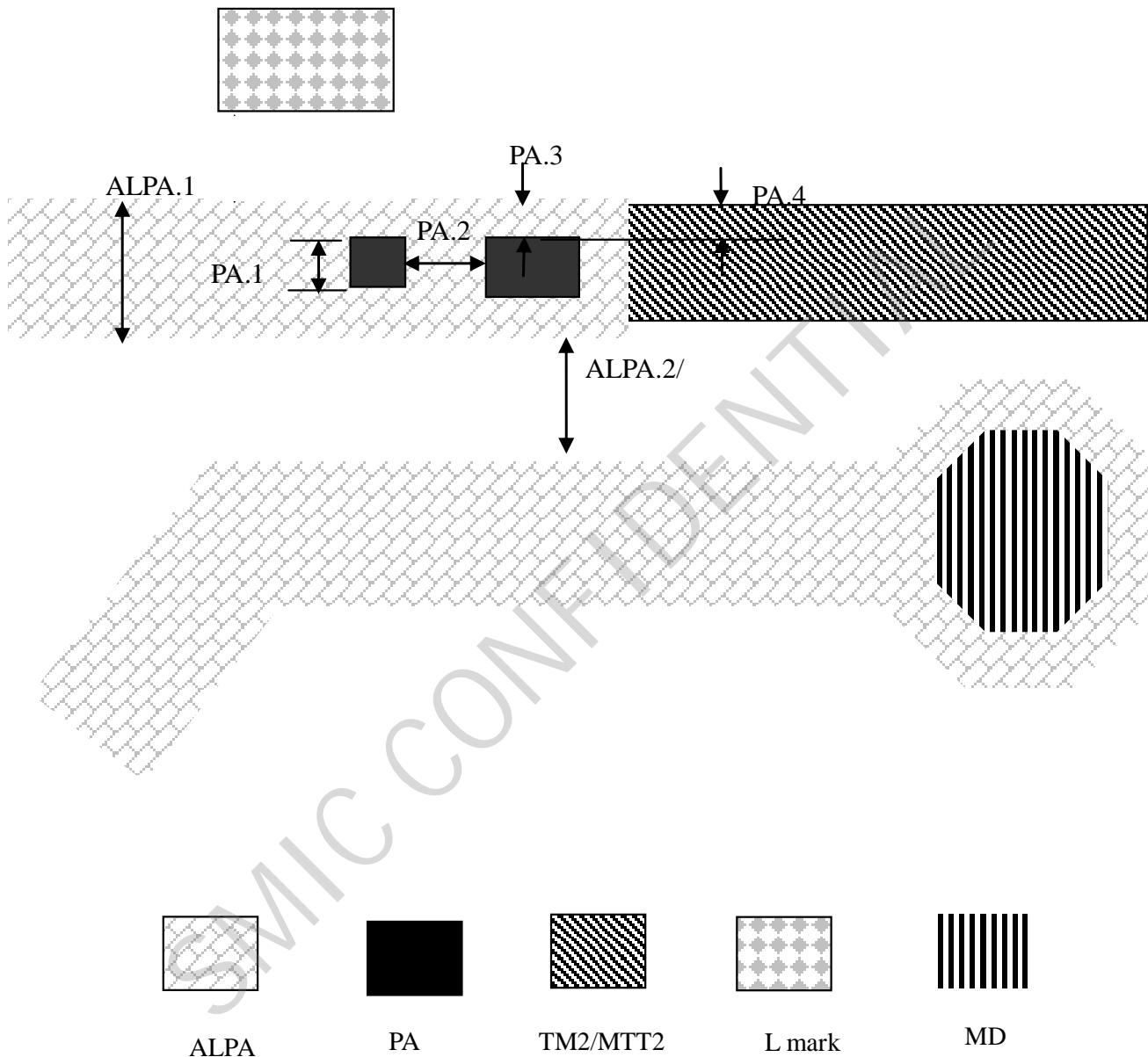
7.4.24 ALPA Rules (Alpa bonding pad, and RDL: redistribution layer)

Rules number	DESCRIPTION	Operation	Design Value	Unit
ALPA.1	ALPA width	\geq	2	μm
ALPA.2	ALPA space	\geq	2	μm
ALPA.3	(purposely blank)			
ALPA.4	(purposely blank)			
ALPA.5	(purposely blank)			
ALPA.6	(purposely blank)			
ALPA.7	(purposely blank)			
ALPA.8	(purposely blank)			
ALPA.9	ALPA density	\geq	10%	
ALPA.10	ALPA density	\leq	70%	
ALPA.11	(purposely blank)			
ALPA.12	ALPA must be drawn layer			
ALPA.13	ALPA.1 and ALPA.2 allow 0.002um tolerance on 45-degree bent ALPA in INDMY.			

Note:

1. ALPA including Alpa Pad and ALRDL.
2. ALRDL is defined as ALPA layer width equal or smaller than 35 μm .
3. ALPA pad is defined as ALPA layer width larger than 35 μm .
4. In addition to the design rules above, the PA design rules must be observed.

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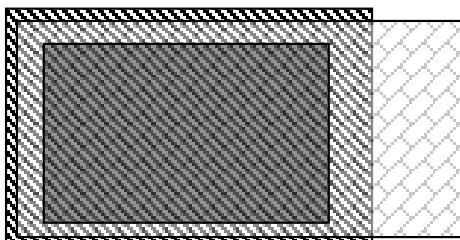
7.4.25 PA (passivation-1) rules

Rules number	DESCRIPTION	Operation	Design Value	Unit
PA.1	PA size	\geq	2	μm
PA.2	Space between two PAs	\geq	2	μm
PA.3	PA enclosed by ALPA	\geq	0.5	μm
PA.4	PA enclosed by TM2, MTT2	\geq	0.5	μm
PA.5	(purposely blank)			
PA.6	(purposely blank)			
PA.7	(purposely blank)			
PA.8	(purposely blank)			
PA.9	(purposely blank)			
PA.10	PA without ALPA above it is not allowed.		-	
PA.11	45-degree rotated PA is not allowed. (Octagon shape PA is allowed.) This rule is not applicable for INDMY region.			
PA.12	PA.1, PA.2, and PA.4 allow 0.002um tolerance on 45-degree rotated PA in INDMY.			

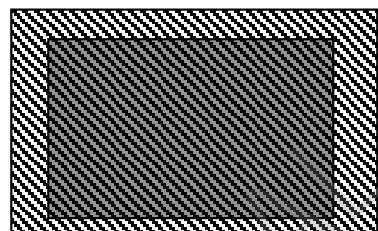
Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 171/299
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PA.10

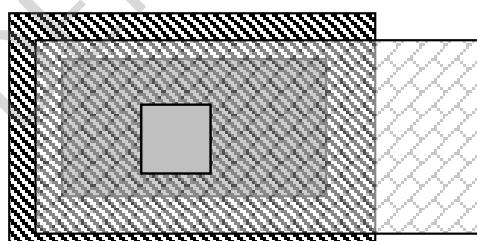
Correct layout:



Not allowed for no ALPA on PA



Not allowed for ALPA hole within PA



TM2



PA opening



Alpa

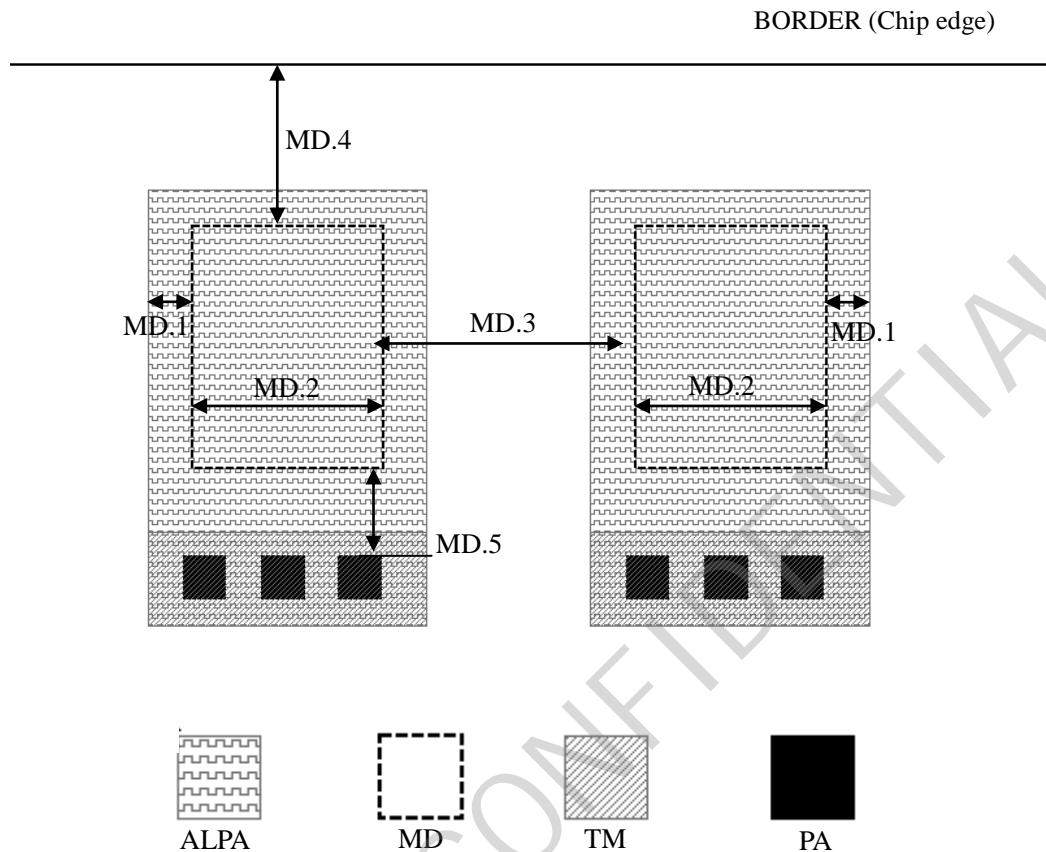


Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 172/299
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7.4.26 MD Rules (passivation-2)

Rules number	DESCRIPTION	Operation	Design Value	Unit
MD.1	MD (PA2) enclosure by Alpa	\geq	1	μm
MD.2	MD (PA2) width	\geq	14	μm
MD.3	MD (PA2) space	\geq	6	μm
MD.4^[R]	MD (PA2) must be within BORDER (CHIP EDGE)	\geq	8	μm
MD.5	MD (PA2) space to PA, if MD not touch with PA	\geq	1.7	μm
MD.6^[R]	MD (PA2) wire-bond pad opening, MD edge space to BORDER (CHIPEDGE).	\leq	200	μm
MD.7	(purposely blank)			
MD.8	Inductor is prohibited under MD (PA2) wire-bond pad opening		-	
MD.9	(purposely blank)			
MD.10	MD(passivation-2) must be a drawn layer			
MD.11	MD(PA2) is prohibited to overlap or touch with PA(PA size <3 μm)			

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7.4.27 BORDER (CHIPEDGE)

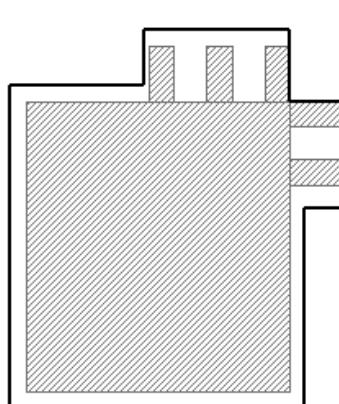
Chip edge BORDER layer and layout pattern rule is defined to avoid any layout pattern extend out to scribe lane region

Rules number	Description	Operation	Design Value	Unit
BORDER.1	Designers must to add BORDER layers (127;0) to define chip boundary and have all chip layout patterns inside BORDER, except DUMBA, DUMB, DUMB in corner as defined in rule CORN.2			
BORDER.2	BORDER enclosure of following layers AA, GT, CT, Mn, Vm. n = 1-8, m = 1-7.	\geq	0.36	μm
BORDER.3	DNW enclosure by BORDER	\geq	0.8	μm
BORDER.4	All designs should place a BORDER at the most outermost edge with straight lines from chip corner area to corner area. The BORDER shape for chip with seal ring is rectangle shape. Without seal ring, octagonal shape (with the corner area fixed 74um)			
BD.5^[NC]	BORDER layer size should be exact same with the seal ring window edge if seal ring has been added by designers.			
BD.6	Enclosure of seal ring outer ring outline edge by BORDER layer if seal ring has been added by designers.	\geq	5	um
BD.7^[NC]	BORDER layer size should be exact same with chip window size in LDDI form (chip window size when tape-out).			
BD.8^[NC]	BORDER layer rules BD.1~ BD.7 are only for chip level design rules. DRC does not check IP level BORDER.			

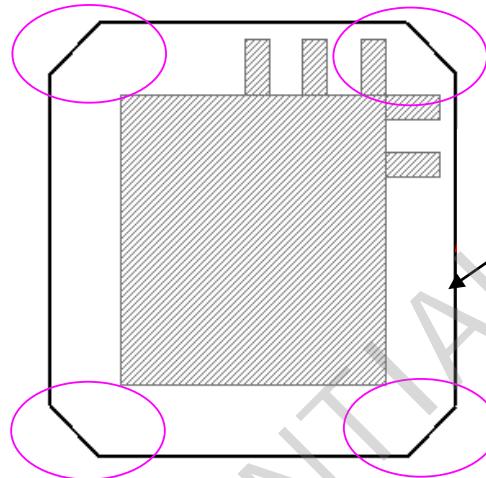
Note:

1. To reduce DRC run time, BORDER.1 DRC script checks following layers: AA, GT, CT, Mn(n = 1-8), TMi(i=1-2), ALPA.
2. For DRC, BORDER is to OR all BORDERs within chip, and include the region holes enclosed by BORDER.
3. DRC runset provides switch for BORDER rule DRC check, which is turn-on by default, this switch can be turn-off for IP level DRC check.

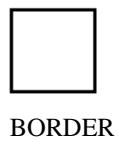
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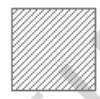
N.G. for BORDER.4



O.K. for BORDER.4



BORDER



CIRCUIT



Chip corner area

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7.4.28 Dummy Check Rules

This section describes the dummy related GDS DRC (design rule check) items. For dummy insertion, please refer to SMIC dummy insertion rule (indicated in Reference section). Designers can refer to below device table for dummy pattern insertion and need add dummy block layers to avoid dummy patterns insertion.

Dummy patterns Device Category	Marker Layer	GDS No.	AA Dummy	Poly Dummy	Inter Metal Dummy	Inter Via Dummy	Top Metal dummy	ALPA Dummy	Remark
LDMOS	LDBK	216;150	Y	Y	Y	Y	Y	Y	
SRAM	INST	60; 0	Y	Y	Y	Y	Y	Y	
AA Resistor	RESAA	97; 0	Y	N	Y	Y	Y	Y	
	DIFRES	97;3	Y	N	Y	Y	Y	Y	
NW Resistor	RESNW	95; 0	N	N	Y	Y	Y	Y	
Poly Resistor	RESP1	96; 0	N	Y	Y	Y	Y	Y	
	PLRES	96;3	N	Y	Y	Y	Y	Y	
HRP	HRPDMDY	210; 0	N	Y	Y	Y	Y	Y	
Diode	DSTR	138; 0	Y	Y	Y	Y	Y	Y	
BJT	BIPOLA	159;1	Y	Y	Y	Y	Y	Y	
MOS Varactor	VARMOS	93; 0	Y	Y	Y	Y	Y	Y	
Junction Varactor	VARJUN	94; 0	Y	Y	Y	Y	Y	Y	
e-Fuse	EFUSE	81;2	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
	GTFUSE	81;1	Y	Y	Y	Y	Y	Y	M1 and M2 dummy should be "N" for GTFUSE
MOM	MOMDMY	211;1	Y	Y	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
Inductor	INDMY	212; 0	Y	Y	Y	N	Y	Y	Designers can draw dummy block layer

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									based on their requirement
Seal Ring	MARKS	189;151	N	N	N	N	N	N	
Guard Ring	MARKG	189; 0	N	N	N	N	N	N	
LOGO	LOGO	26; 0	N	N	N	N	N	N	
Y: do dummy filling by script automatically.									
N: block dummy filling by marker layer of device, and will be defined in the dummy insertion rules to avoid dummy filling.									

The following section's "SMIC dummy" rule refers to the dummy inserted under the SMIC dummy insertion rule. The "non-SMIC dummy" refers to the dummy inserted by rules other than SMIC dummy insertion rule. DRC default option is set to check "SMIC dummy".

7.4.28.1 Dummy pattern Check Rules for SMIC dummy and customer dummy

The dummy checking rules as below are used for the dummy patterns checking.

1. If the GDS passes all the dummy checking rules as below, it means that the dummy pattern followed SMIC dummy insertion script.
2. If the GDS passes DUMC.41~DUMC.50 rule checking but fails the rules of DUMC.1~DUMC.40, it means that the dummy pattern did not follow SMIC dummy insertion script. SMIC integration engineer and customer engineer should be informed.
3. If the dummy pattern can't pass DUMC.41~DUMC.50 rule checking, this GDS is not allowed for tape-out.

Rules number	DESCRIPTION	Operation	Design Value	Unit
DUMC.1	(Purposely blank).			
DUMC.2	Dummy AA must not touch (AA, GT, CT, LOGO, PTCT, MARKS, RESP1, RESNW, PLRES, HRPDMY).			
DUMC.3	(Purposely blank).			
DUMC.4	(Purposely blank).			
DUMC.5	Dummy AA space to AA.	≥	0.710	μm
DUMC.6	Dummy AA space to (GT, PTCT, RESP1, RESNW, PLRES, HRPDMY).	≥	0.220	μm
DUMC.7	Dummy AA space to GTFUSE.	≥	3.330	μm
DUMC.8	Dummy AA space to NW.	≥	0.260	μm
DUMC.9	(purposely blank)			
DUMC.10	Dummy AA cannot insert at RESNW area			

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Rules number	DESCRIPTION	Operation	Design Value	Unit
DUMC.11	Dummy AA should not be larger than 20x20 μm			
DUMC.12	Dummy GT must not touch (AA, GT, CT , LOGO, PTCT, MARKS, RESAA, RESNW, DIFRES).			
DUMC.13	Dummy GT width	\geq	0.044	μm
DUMC.14	Dummy GT space	\geq	0.110	μm
DUMC.15	Dummy GT space to GT on AA	\geq	0.150	μm
DUMC.15a	Dummy GT space to GT on field OX	\geq	0.110	μm
DUMC.16	Dummy GT space to (AA, PTCT, RESAA, RESNW, DIFRES, HRPDMY).	\geq	0.220	μm
DUMC.16a	(Purposely blank)			
DUMC.17	Dummy GT space to GTFUSE.	\geq	3.330	μm
DUMC.18	M _x Dummy must not touch (CT , M _x , V _x , V _{x-1} , TV1 , TV2 , LOGO, PTCT, MARKS), where M _x =M1-M8, TM1, TM2, MTT2. x=1~8. V ₈ and V ₋₁ are not applicable.			
DUMC.19	M _x Dummy space to GTFUSE with touching prohibited, where M _x =M1, M2.	\geq	3.33	μm
DUMC.20	M _x Dummy space to (MxDUB, DUMB, PTCT), where M _x =M1-M8.	\geq	0.6	μm
DUMC.21	M _x Dummy space to M _x (when M _x Dummy not touching INDMY), where M _x =M1-M8.	\geq	0.6	μm
DUMC.21a	M _x Dummy space to M _x (when M _x Dummy touching INDMY), where M _x =M1-M8.	\geq	0.53	μm
DUMC.22	V _x Dummy must not touch (V _x , M _x , M _{x+1} , LOGO, PTCT, INDMY, MARKS), where V _x =V1-V7, x=1-7			
DUMC.23	V _x Dummy exact width, where V _x =V1-V7.	=	0.077 or 0.07 or 0.12	μm
DUMC.24	xx Dummy must be square, where xx=V1-V7			
DUMC.25a	V _x Dummy must be within M _x Dummy, where V _x =V1-V7 and M _x = metal level below V _x .	\geq	0.06	μm
DUMC.25b	V _x Dummy must be within M _y Dummy, where V _x =V1-V7 and M _y = metal level above V _x .	\geq	0.06	μm



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Rules number	DESCRIPTION	Operation	Design Value	Unit
DUMC.26	TMx Dummy space to (TMx, TMxDUB, PTCT), where TMx=TM1, TM2	\geq	0.6	μm
DUMC.26a	MTT2 Dummy(MTT2DM) space to (MTT2, MTT2DB, PTCT)	\geq	1.77	μm
DUMC.27	ALPA Dummy must not touch (ALPA, LOGO, PTCT,MARKS)			
DUMC.28	ALPA Dummy space to (ALPA, ALDUB, PTCT).	\geq	2.84	μm
DUMC.29	ALPA Dummy space to INDMY with touching prohibited.	\geq	2.84	μm
DUMC.30	xx Dummy density within INDMY. (Where xx=M1~M8, TM1, TM2, MTT2. Only check dummy metal density)	\leq	12%	
DUMC.31	xx Dummy must be within BORDER, where xx=all metal and via levels, AA, GT			
DUMC.32	Width of Mx Dummy, where Mx=M1-M8.	\geq	0.22	μm
DUMC.33	Space of Mx Dummy, where Mx=M1-M8.	\geq	0.22	μm
DUMC.34	Width of TMx Dummy, where TMx=TM1-TM2.	\geq	0.44	μm
DUMC.34a	Width of MTT2 Dummy	\geq	1.5	μm
DUMC.35	Space of TMx Dummy, where TMx=TM1-TM2.	\geq	0.6	μm
DUMC.35a	Space of MTT2 Dummy	\geq	1.0	μm
DUMC.36	Width of ALPA Dummy.	\geq	4.44	μm
DUMC.37	Space of ALPA Dummy.	\geq	2.84	μm
DUMC.38	(Purposely blank)			
DUMC.39	(Purposely blank)			
DUMC.40	Vx Dummy to Vx Dummy space	\geq	0.13	μm
DUMC.41	Dummy AA must follow AA.1, AA.4a, AA.9a, AA.11, AA.13, AA.13a, AA.16, AA.17 rules.			
DUMC.42	Dummy GT must follow GT.2a, GT.3,GT.3c,GT.3e,GT.4,GT.8a,GT.17,GT.17a,GT.18,GT.18a, GT.27,GT.28 rules.			
DUMC.43	Dummy M1 must follow M1.1, M1.2, M1.3, M1.4, M1.4a, M1.5, M1.6, M1.6a, M1.6b, M1.6c, M1.9, M1.10, M1.14 rules.			

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Rules number	DESCRIPTION	Operation	Design Value	Unit
DUMC.44	Dummy Mx must follow Mn.1, Mn.2, Mn.3, Mn.4, Mn.4a, Mn.5, Mn.6, Mn.6a, Mn.6b, Mn.6c, Mn.8, Mn.9, Mn.12, Mn.13, Mn.16 rules. Where Mx=M2-M8.			
DUMC.45	Dummy V1 must follow V1.2, V1.5, V1.5a, V1.6, V1.6a, V1.6b, V1.6c, V1.7, V1.7a, V1.7b, V1.7c, V1.18, V1.21 rules.			
DUMC.46	Dummy Vx must follow Vn.2, Vn.5, Vn.5a, Vn.6, Vn.6a, Vn.6b, Vn.6c, Vn.7, Vn.7a, Vn.7b, Vn.7c, Vn.18, Vn.21 rules. Where Vx=V2-V7, x=2-7.			
DUMC.47	Dummy TM1 must follow TM1.1, TM1.2, TM1.5, TM1.7, TM1.8, TM1.9, TM1.13 rules.			
DUMC.48	Dummy TM2 must follow TM2.1, TM2.2, TM2.5, TM2.7, TM2.8, TM2.9, TM2.12 rules.			
DUMC.49	Dummy MTT2 must follow MTT2.1, MTT2.2, MTT2.6, MTT2.6a, MTT2.11 rules.			
DUMC.50	Dummy ALPA must follow ALPA.1, ALPA.2 rules.			

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7.4.29 Current Density Rule

Jmax is maximum DC current allowed per um of metal line width or per via/contact. The junction temperature is at 110°C.

Rules number	DESCRIPTION	Operation	Design Value	Unit
CDR.5	Jmax of CT line at 110°C	≤	0.2	mA/ μm

Layer	Width(um)	Length(um)	Jmax
M1	<0.5um	L>10um	1.2mA/um (current/width)
		10um≥L>5um	1.2x2mA/um (current/width)
		L≤5um	1.2x4mA/um (current/width)
	≥0.5um	L>5um	1.2x2mA/um (current/width)
		L≤5um	1.2x4mA/um (current/width)
Mn	<0.5um	L>10um	1.3mA/um (current/width)
		10um≥L>5um	1.3x2mA/um (current/width)
		L≤5um	1.3x4mA/um (current/width)
	≥0.5um	L>5um	1.3x2mA/um (current/width)
		L≤5um	1.3x4mA/um (current/width)
TM	<0.5um	L>10um	8.8mA/um (current/width)
		10um≥L>5um	8.8x2mA/um (current/width)
		L≤5um	8.8x4mA/um (current/width)
	≥0.5um	L>5um	8.8x2mA/um (current/width)
		L≤5um	8.8x4mA/um (current/width)
ALPA(14.5K)	Any Width	Any Length	2.8mA/um (current/width)
ALPA(28K)	Any Width	Any Length	5.6mA/um (current/width)
UTM	Any Width	Any Length	32mA/um (current/width)
Vn	<0.5um	L>10um	0.07mA/via
		10um≥L>5um	0.07x1.5mA/via
		L≤5um	0.07x4mA/via
	≥0.5um	L>5um	0.07x2mA/via
		L≤5um	0.07x4mA/via
TV	<0.5um	L>10um	3mA/via
		10um≥L>5um	3x1.5mA/via
		L≤5um	3x4mA/via
	≥0.5um	L>5um	3x2mA/via
		L≤5um	3x4mA/via
PA(size=3um)	Any Width	Any Length	7mA/PA
PA(size=2um)	Any Width	Any Length	5.4mA/PA

Note:

1. Suggest use as much as CT/Via numbers in layout design for reliability margin agreement.
2. Minimal required metal width and CT/Via numbers are determined by allowed design current.
3. Preferentially use maximal CT/Via design numbers for perpendicular current flow direction.



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7.4.29.1 Temperature coefficient

* Cu Temperature coefficient

Temperature C (degree)	100	105	110	115	120	125
Factor	2.149	1.459	1	0.692	0.484	0.341

* Contact (CT) temperature coefficient

CT temperature coefficient is the same as Cu.

* Aluminum temperature coefficient

Temperature C(degree)	70	85	100	110	125
Factor	3.443	2.097	1.329	1	0.6707

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7.4.29.2 AC current density Irms

Irms definition:

$$I_{rms} = \sqrt{\frac{1}{t_w} \int_0^{t_w} i^2(t) dt}$$

tw= Irms check period. Typically, current period.

i(t)= current

W (in μm) : the width of the metal line

ΔT ($^{\circ}\text{C}$): the temperature rise due to Joule heating

Conduction layer	Operation	Irms	Unit
M1	\leq	SQRT[$\Delta T * (10.82 * w^2 + 11.73 * w)$]	mA
M2	\leq	SQRT[$\Delta T * (3.49 * w^2 + 3.93 * w)$]	mA
M3	\leq	SQRT[$\Delta T * (3.38 * w^2 + 4.25 * w)$]	mA
M4	\leq	SQRT[$\Delta T * (3.33 * w^2 + 4.16 * w)$]	mA
M5	\leq	SQRT[$\Delta T * (3.12 * w^2 + 3.67 * w)$]	mA
M6	\leq	SQRT[$\Delta T * (3.06 * w^2 + 4.55 * w)$]	mA
M7	\leq	SQRT[$\Delta T * (2.23 * w^2 + 2.90 * w)$]	mA
M8	\leq	SQRT[$\Delta T * (2.12 * w^2 + 2.79 * w)$]	mA
TM1	\leq	SQRT[$\Delta T * (9.72 * w^2 + 33.46 * w)$]	mA
TM2	\leq	SQRT[$\Delta T * (7.01 * w^2 + 30.31 * w)$]	mA
MTT2	\leq	SQRT[$\Delta T * (6.70 * w^2 + 83.39 * w)$]	mA
ALPA	\leq	SQRT[$\Delta T * (4.41 * w^2 + 42.13 * w)$]	mA

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7.4.30 Chip Corner Rules

This section applies for the chips that need seal ring insertion and before seal ring insertion. This section describes the chip corner requirements to prevent the chip design interferes with seal ring. For seal ring detail design, please refer to seal ring insertion rule (doc number described in Reference section).

Rules number	DESCRIPTION	Operation	Design Value	Unit
CORN.1	Chamfer area size at the chip corner. The chip edge is defined to be the maximum boundary of all chip layers. All layers include BORDER (127; 0) should not interact with area A in the figure. This rule is applicable for chips before seal ring insertion.	\geq	74	μm
CORN.2	For the chips needs SMIC mask shop insert dummy and seal ring, the corner area A(see this section figure) should be covered with (DUMBA, DUMBP, DUMBMB).			

Note:

- c) The DRC executes this section rule check on following layers: AA, GT, CT, SP, SAB, Mn (n=1-8), MnDUM (n=1-8), TM1, TM2, MTT2, BORDER.
- d) This rule section only applies for those chips that need to have seal ring insertion. The chip corner rule check option is default turned on in DRC script.
- e) In case for the building block level design, or the chip level design with seal ring already inserted, please turn off the chip corner rule check option.

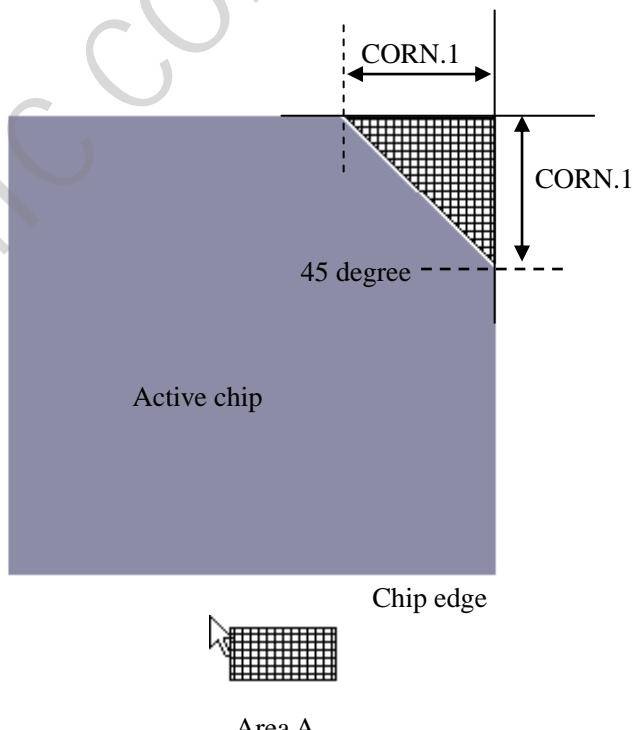


Fig.7.4.30-1



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7.4.31 Conventional Rule

Rules number	DESCRIPTION	Operation	Design Value	Unit
Convention.1	NW not interacting with N+ pickup is not allowed.			
Convention.2	(SP AND (AA AND GT)) in PW is not allowed, except LDMOS, VARMOS and OCCD region.			
Convention.3	(SN AND (AA AND GT)) in NW is not allowed, except LDMOS and VARMOS region. This rule is not applied for (DNSRAM OR LRSRAM) OR D2SRAM) OR RFSSRAM) covered region.			

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7.4.32 HRP Rules (high resistance poly layer)

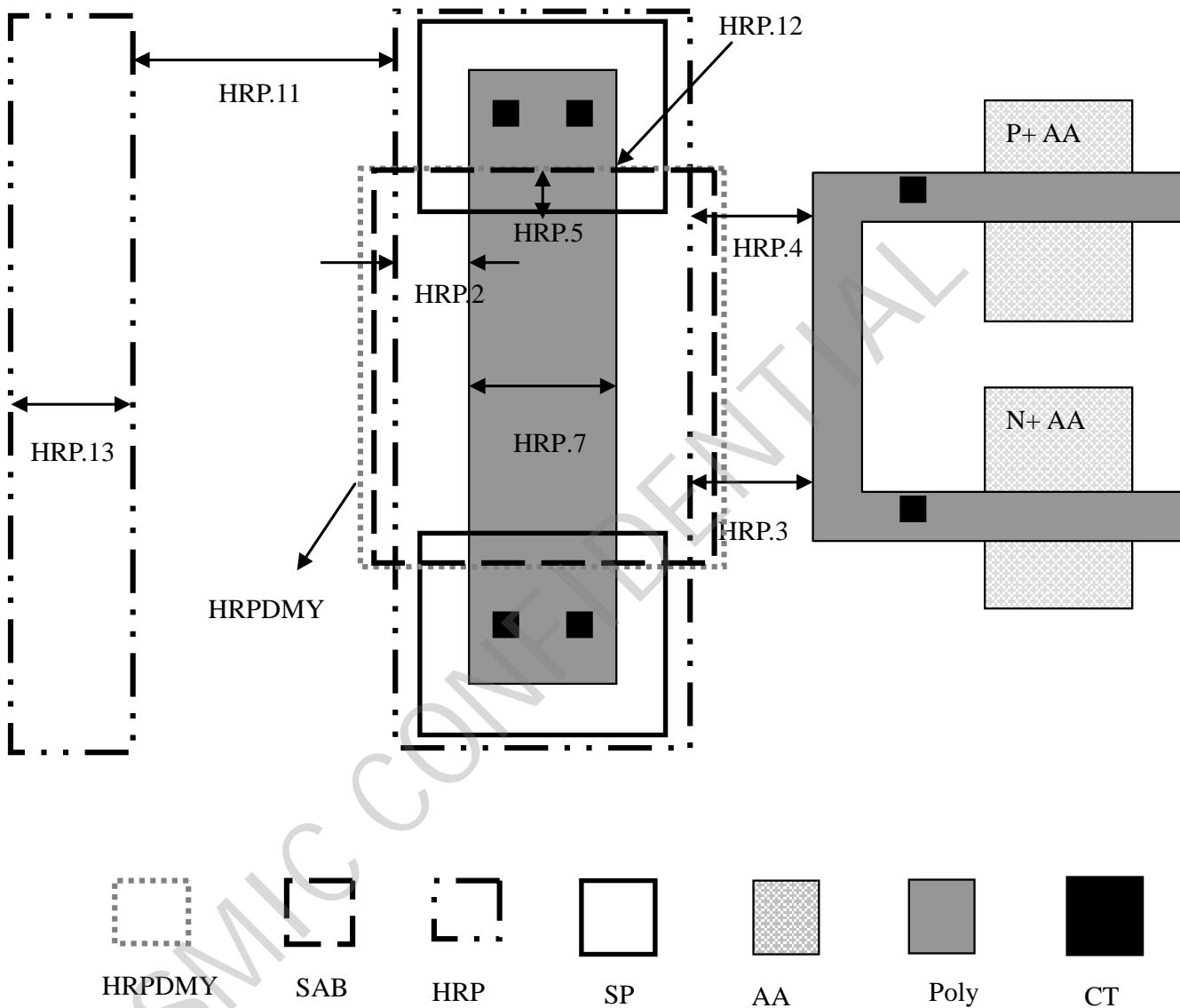
HRPDMY(210;0) is the marker layer for high resistance Poly, high resistance Poly resistors is the overlapped area of Poly and HRPDMY, high resistance Poly resistor must within HRP and HRPDMY layer.

Layer HRP(39;0): HRP implant area

HRP resistor or resistor in this section stands for (HRPDMY AND GT)

Rules number	DESCRIPTION	Operation	Design Value	Unit
HRP.1 ^[NC]	It is strongly suggested that resistor square number ≥ 1 for precision Rs			
HRP.2	HRP extension outside of poly resistor region	\geq	0.22	μm
HRP.3	Space from HRP region to Poly gate of NMOS	\geq	0.20	μm
HRP.4	Space from HRP region to Poly gate of PMOS	\geq	0.20	μm
HRP.5	P+ region for pickup overlap with SAB	$=$	0.30	μm
HRP.6	(purposely blank)			
HRP.7	Width of Poly region for high resistance poly resistor	\geq	2.00	μm
HRP.8 ^[NC]	Dummy layer “HRPDMY” is needed for LVS, DRC to define high resistance poly resistor body in model			
HRP.9	(SN, SP) layers are not allowed in the HRPDMY region (when check the rule, size down the HRPDMY by 0.3 μm along the current direction)			
HRP.10	For contact rule, please follow Logic baseline rule			
HRP.11	HRP space	\geq	0.18	μm
HRP.12	HRPDMY and SAB on GT should have coincident edge			
HRP.13	HRP Width	\geq	0.18	μm

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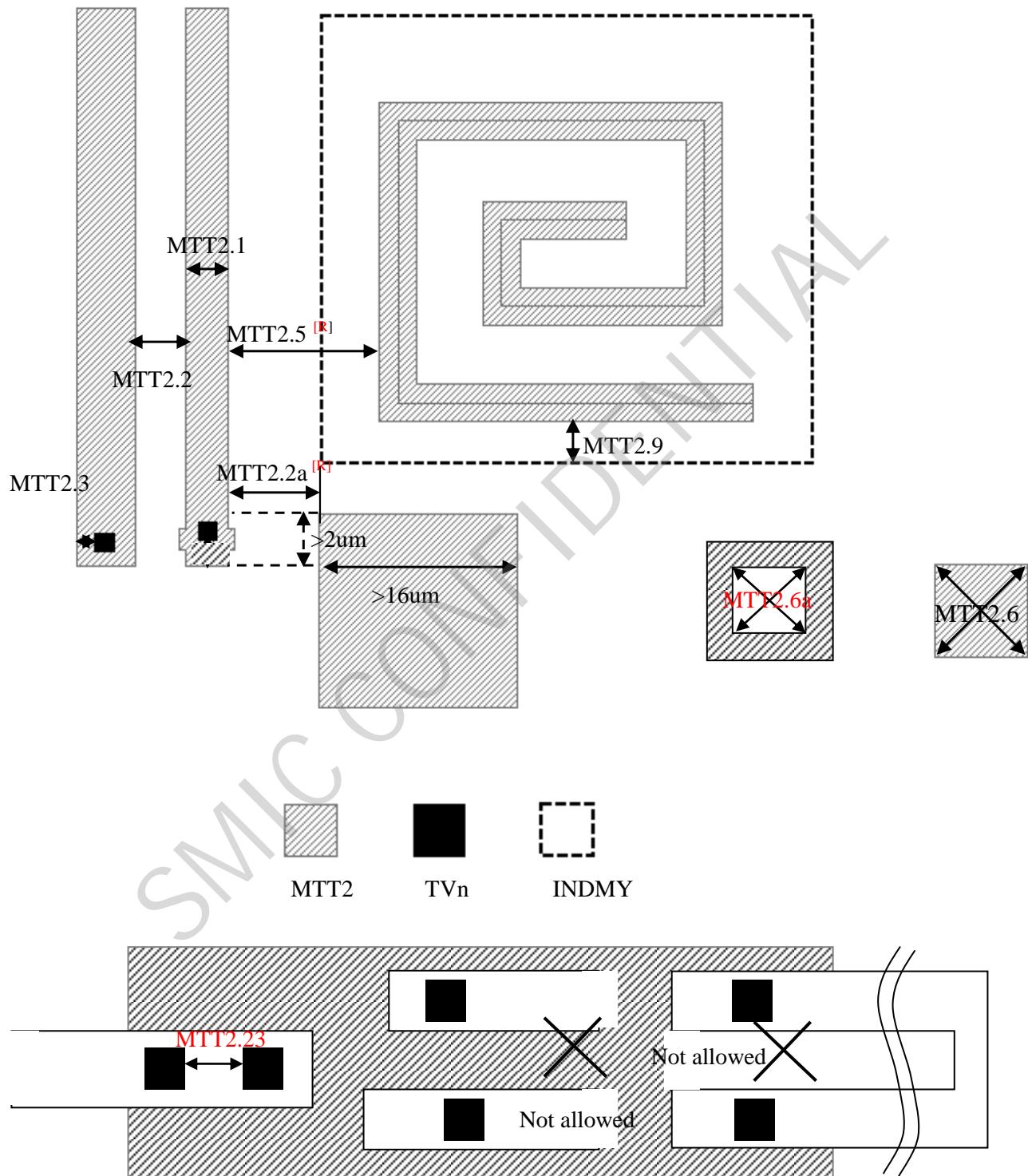


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7.4.33 MTT2 Rules (ultra thick top metal layer, metal thickness 3.4 μm)

Rules number	DESCRIPTION	Operation	Design Value	Unit
MTT2.1	MTT2 Width	\geq	1.5	μm
MTT2.2	Space between two MTT2 regions	\geq	1.0	μm
MTT2.2a [R]	Space between two MTT2s having parallel segment larger than 2 μm with one or both MTT2 width larger than or equal to 16 μm	\geq	2.00	μm
MTT2.3	Extension of MTT2 region beyond top Via	\geq	0.30	μm
MTT2.4	(purposely blank)			
MTT2.5 [R]	Space from MTT2 used as Inductor to other MTT2 region	\geq	30	μm
MTT2.6	MTT2 area	\geq	9	μm^2
MTT2.6a	Enclosed area	\geq	9	μm^2
MTT2.7	Density of MTT2 area. Window size:200 μm *200 μm with step size:100 μm	\geq	15%	
		\leq	85%	
MTT2.7a	MTT2 density over the whole chip	\geq	20%	
MTT2.7b [R]	INDMY area density in window size 840 μm *840 μm with step 420um	\leq	20%	
MTT2.8	All devices listed in device table inside Inductor region are prohibited			
MTT2.9 [R]	Extension of dummy layer "INDMY" beyond MTT2 region used as Inductor	\geq	15	μm
MTT2.10 ^[NC]	Inductor components (including inductor circuit, guard ring, dummy patterns) should be covered by INDMY layer			
MTT2.11	MTT2 line width allowed. MTT2 underneath of MD does not follow this rule	\leq	17	μm
MTT2.12	MTT2 pattern density on the whole chip(including dummy patterns)	\leq	55%	
MTT2.13 [R]	At least 2 TVs with space \leq 1.7 μm are required to connect MTT2. (Please add vias as many as possible which is for reliability concern and RF application)			

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7.4.34 Poly E-Fuse Layout guideline

For the fuse component, it must be drawn EFUSE (81;2), GTFUSE (81;1), FUSEMK1 (81;152) marker layer.

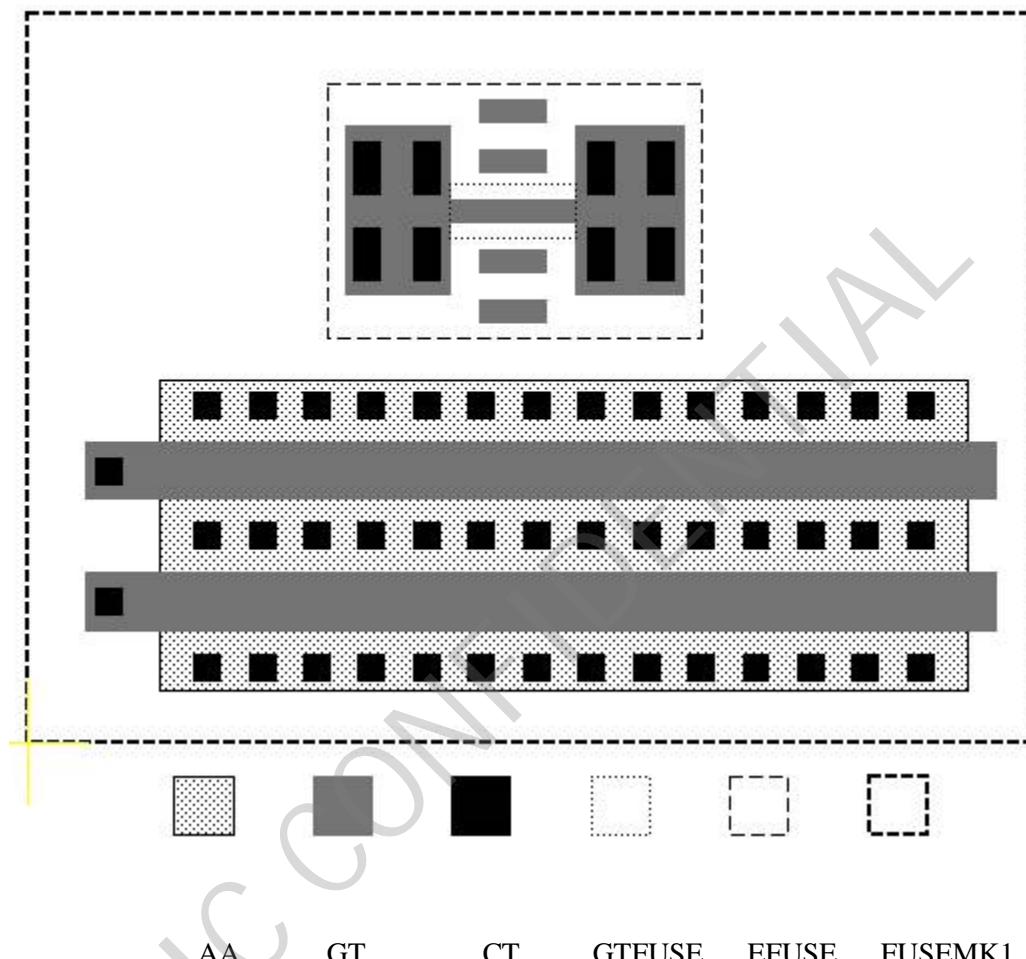
E-fuse element is covered by EFUSE (81;2).

E-fuse function area is marked with GTFUSE (81;1).

All fuse component must be fully covered by FUSEMK1 (81;152).

Rules number	Description	Operation	Design Value	Unit
EFU.1a ^{[G][NC]}	FUSEMK1 (81;152) must fully enclose all fuse component, including EFUSE (81;2) region, program transistor, etc.			
EFU.1b ^[G]	FUSEMK1 (81;152) must interact with EFUSE (81;2) region.			
EFU.1c ^[G]	FUSEMK1 (81;152) must fully cover EFUSE (81;2) region.			
EFU.2a ^{[G][NC]}	EFUSE (81;2) must fully enclose the whole fuse element and related dummy region.			
EFU.2b ^[G]	EFUSE (81;2) must interact with GTFUSE(81;1).			
EFU.2c ^[G]	EFUSE (81;2) must fully cover GTFUSE(81;1).			
EFU.3 ^{[G][NC]}	(GTFUSE AND GT) is just the EFUSE function area.			
EFU.4 ^{[G][NC]}	It is strongly recommended to adopt SMIC standard efuse element, including program transistor.			
EFU.5 ^{[G][NC]}	If designers plan to adopt customer own design, designers must provide efuse layout to SMIC for risk assessment before design start.			

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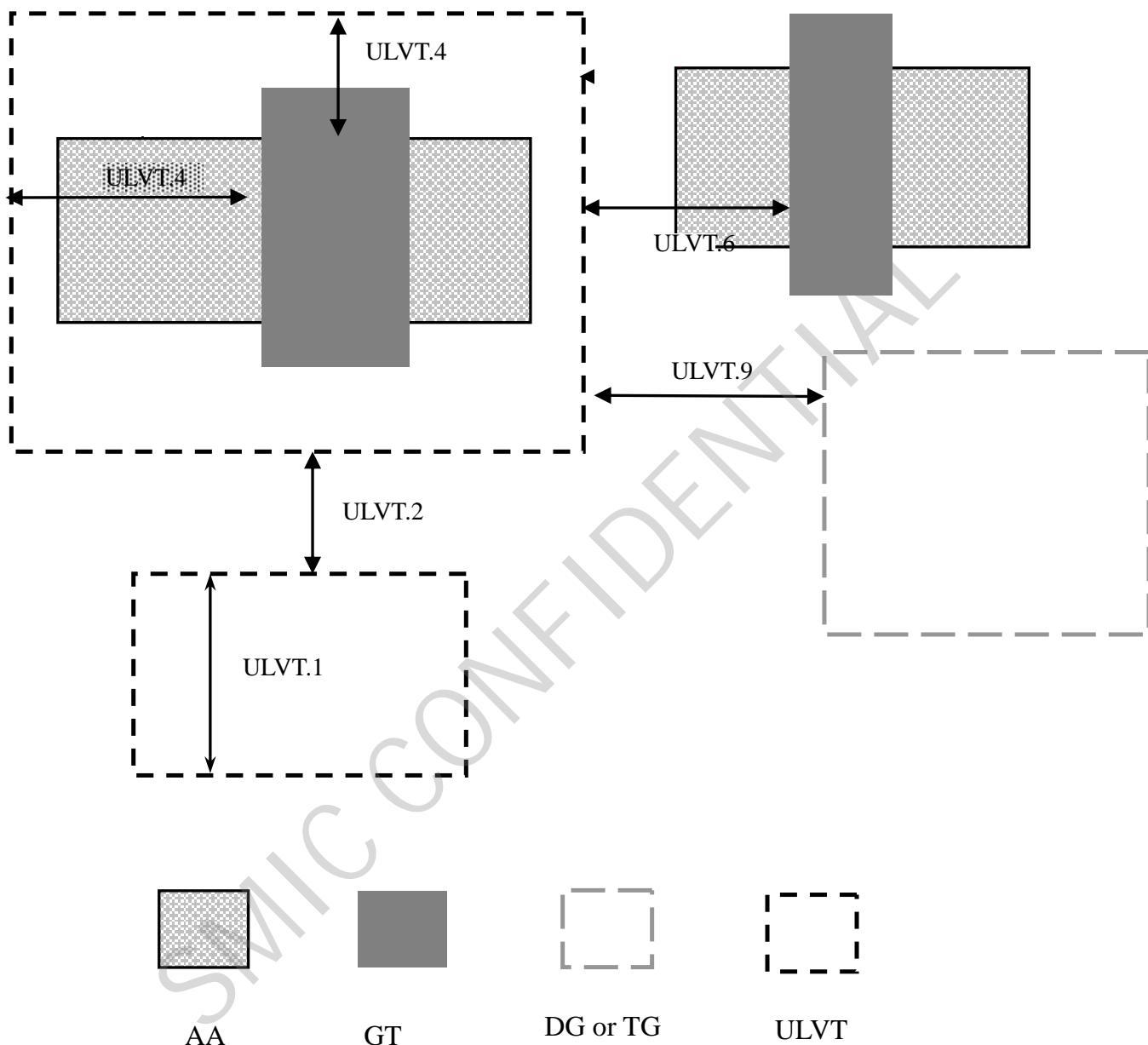
Doc. No.: TD-LO40-DR-2001	Doc. 40nm Logic Salicide Title: 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 192/299
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7.4.35 ULVT: Ultra Low Vt devices Rules

Ultra low Vt device is one of core voltage devices. Ultra low Vt devices are inside ULVT. ULVT transistor minimum channel length and minimum channel width is the same as core voltage transistor.

Rules number	Description	Operation	Design Value	Unit
ULVT.1	ULVT width (Parallel side to side width)	≥	0.33	μm
ULVT.2	Space between two ULVTs (with run length>0)	≥	0.33	μm
ULVT.3	(purposely blank)			
ULVT.4	Gate enclosure by ULVT	≥	0.14	μm
ULVT.5	(purposely blank)			
ULVT.6	Space between ULVT and Real Gate	≥	0.14	μm
ULVT.7	ULVT area	≥	0.463	μm ²
ULVT.8	ULVT enclosed area	≥	0.463	μm ²
ULVT.9	Space between ULVT and (DG or TG)	≥	0.33	μm

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7.4.36 Seal Ring insertion Rules and Checking Rules

Seal ring is the structure to protect circuit from mechanical damage during die saw. A continuous scribe line and seal ring is required on all sides of a chip that is intended for dicing and packaging. The dimensions given in Figs. 1- 4 and in the tables in this section are used by SMIC. **Generally, it's strongly recommended designers to follow SMIC seal ring GDS sample structure. If designers use their owned seal ring structure, SMIC can't guarantee the seal ring quality.**

The seal ring provides both a low resistance path to ground for surge currents and a metal seal against ionic contaminations.

The seal ring rule has been revised from previous generation of technology for more robust protection. 45 degree bend is expected around every die corner. Multiple stacked via/Metal trench are considered to suppress crack risk during dicing saw operation in assembly.

Fig.-1 shows the typical structure of scribe line seal ring.

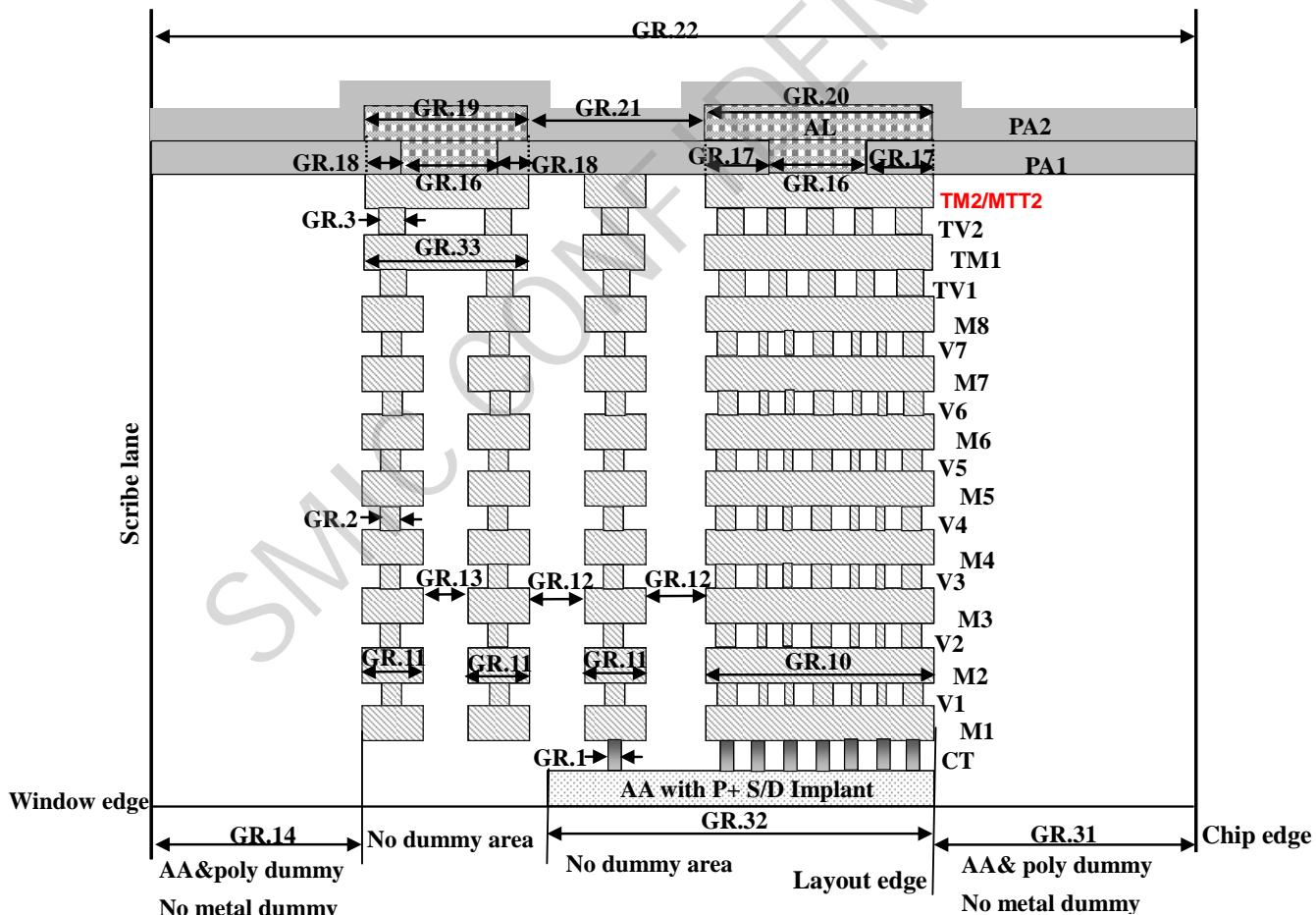
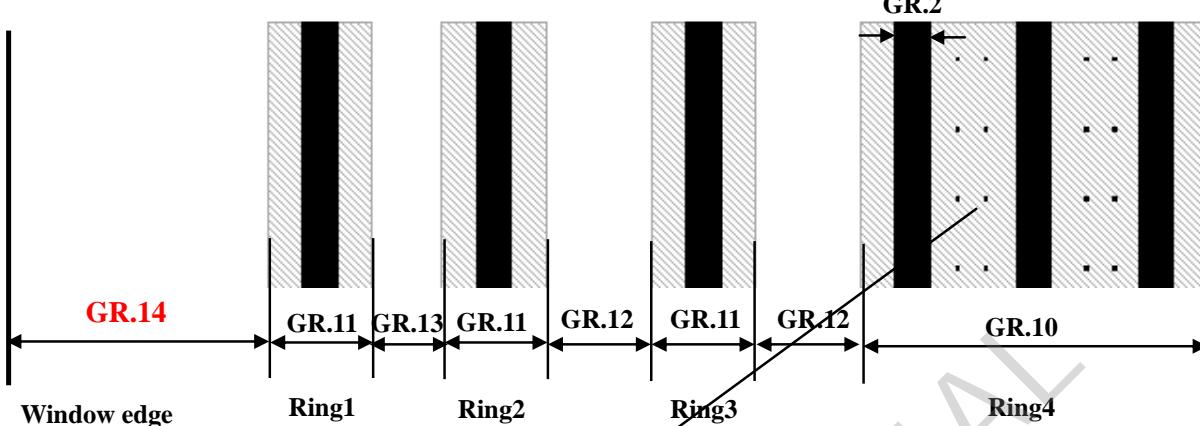


Fig1. Cross sectional schematic of 10 metal seal ring structure

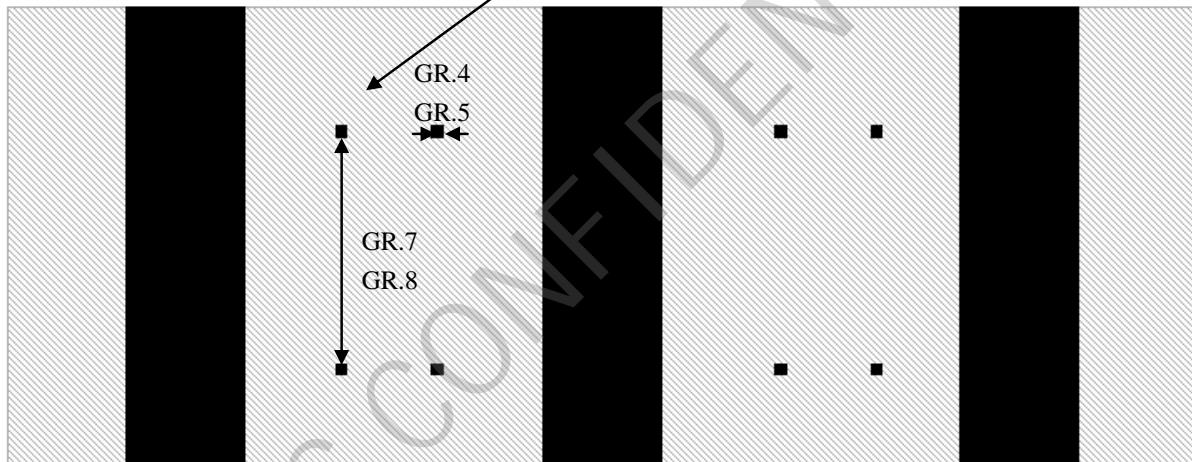
For products less than 10 metal layers, please skip the metal and via layers that are not used in the product.

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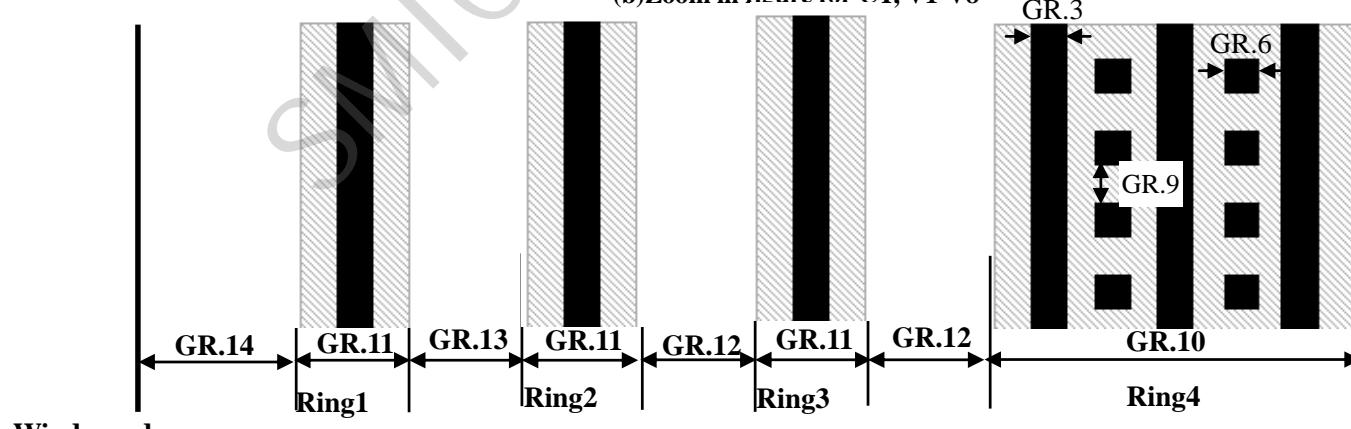


(a) For CT, M1-M8, V1-V8

Ring1 and Ring2 will be merged into one Ring at top metal



(b) Zoom in figure for CT, V1-V8



(c) For TMx, TVx (x=1.2) , MTT2

Figure2 Schematic top view of the seal ring structure

Ring1 and Ring2 will be merged into one ring at top metal

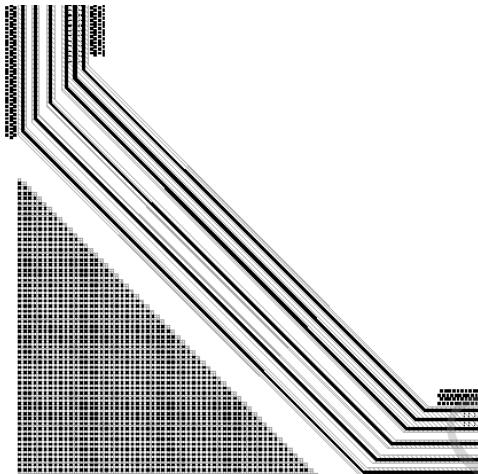
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7.4.36.1 Seal Ring Insertion Rules

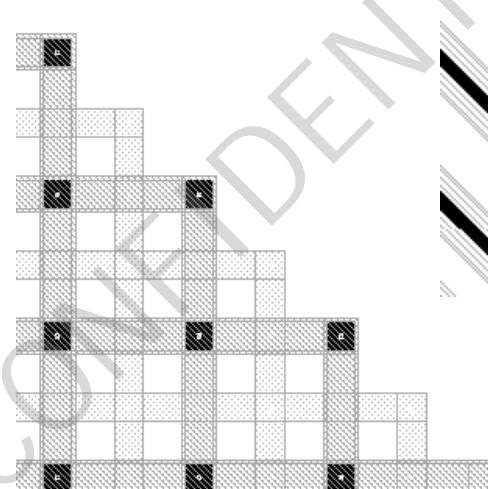
The chamfer region is required for all chips for process robustness. A chamfer or corner bevel of more than 74 um is required to be cut from each corner of the chip. The chamfer area is triangular and has an area of more than half of 74 um x 74 um square.

The seal ring corner layout in Fig.3~Fig.5 is recommended to SMIC's customers to manage local stress at each die corner. Metal & via dummy pattern is recommended at each corner of seal ring. The dimension of each segment in the corner layout is given in Fig. 3~4.

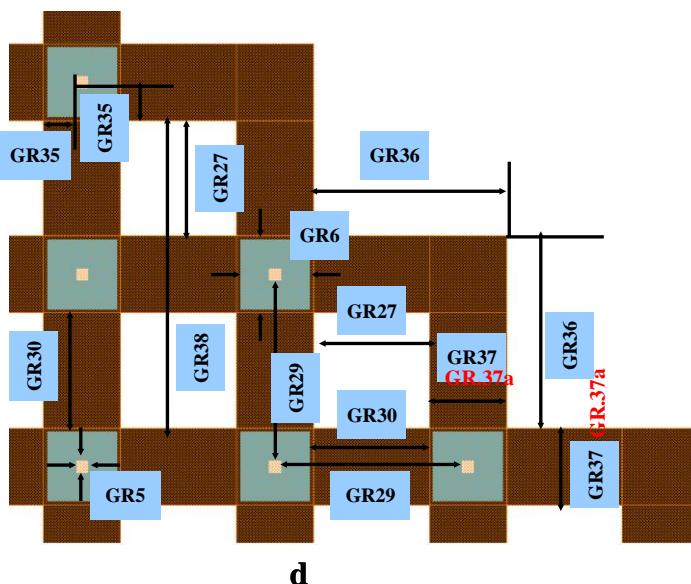
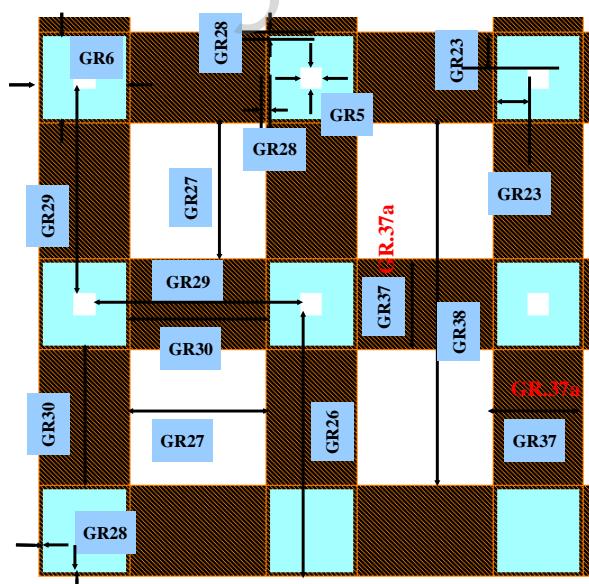
Fig3, Fig. 4 and Fig.5 show the schematic of the chip corner and seal ring corner design for the customers who want SMIC to add the seal rings for them. In summary, Fig. 5 is SMIC internal standard.



(a) Die corner stress relief structure layout



(b)Zoom-in image for the corner 45 degree edge area of (a)



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Fig. 3. Die corner stress relief structure layout

- (a) for M1~M8, V1~V7
- (b) zoom in images for the corner 45 degree edge area of (a)
- (c) zoom in images for the cross of left side and bottom side area of (a)
- (d) zoom in images for the corner 45 degree edge area of (b)

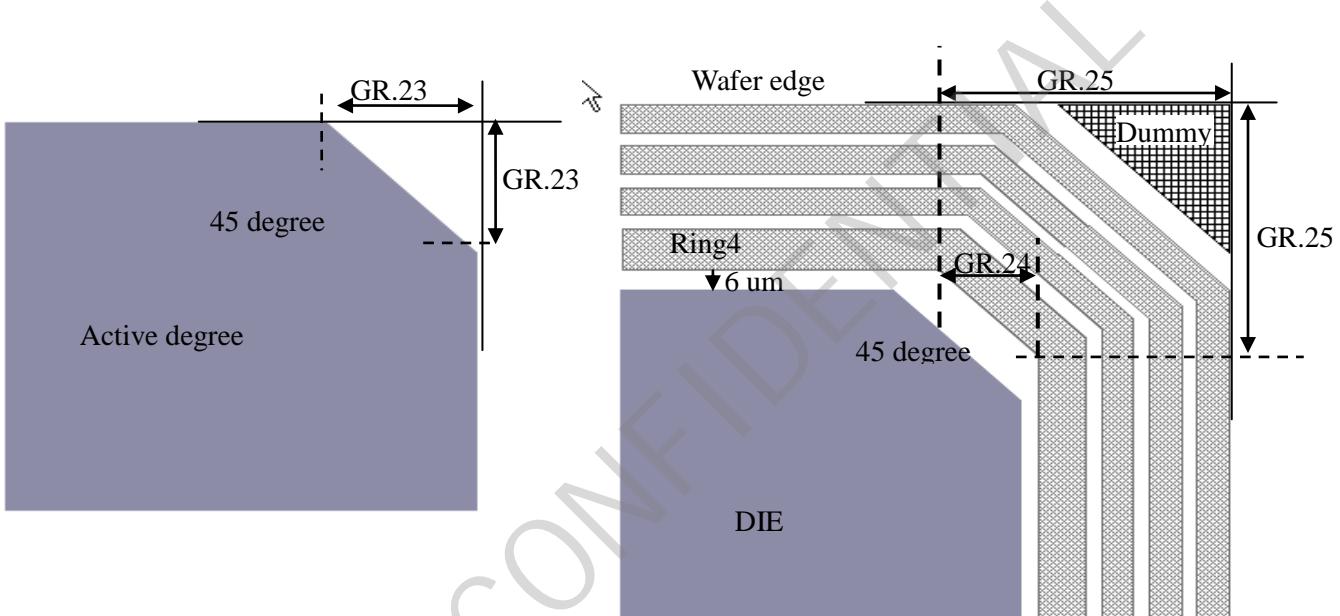


Fig.4 Chamfer area at chip corner

Fig.5 Seal ring corner if applied by SMIC

Table 1 Dimension of Seal ring structure

Rule Number	Description	Operation	Design Value	Unit
GR.1^[NC]	Contact slot width (fixed), it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.06	μm
GR.2^[NC]	V1-V7 slot width (fixed), it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.07	μm
GR.3^[NC]	TV1, TV2 slot width (fixed), it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.36	μm
GR.4^[NC]	Square CT size (fixed)	=	0.06	μm
GR.5^[NC]	Square V1-V7 size (fixed)	=	0.07	μm

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GR.6^[NC]	Square TV1, TV2 size (fixed)	=	0.36	μm
GR.7^[NC]	Space between square CT along the direction of seal ring	≥	1.051	μm
GR.8^[NC]	Space between square Vn (n=1~7) along the direction of seal ring	≥	1.041	μm
GR.9^[NC]	Space between square TVn (n=1~2,) along the direction of seal ring	≥	0.711	μm
GR.10^[NC]	M1-M8 width of ring4, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	≥	5.556	μm
GR.11a^[NC]	M1-M8 width of ring1, ring2, ring3, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	≥	1.666	μm
GR.11b^[NC]	TM1, TM2, MTT2 width of ring1. It is allowed $\sqrt{2}$ variation at 45 degree angle area.	≥	4.445	μm
GR.11c^[NC]	TM1, TM2, MTT2 width of ring 2 and ring3. It is allowed $\sqrt{2}$ variation at 45 degree angle area.	≥	1.666	μm
GR.12^[NC]	Space between ring4 and ring3, space between ring3 and ring2	≥	1.667	μm
GR.13^[NC]	Space between ring1 and ring2	≥	1.111	μm
GR.14^[NC]	Space between metal ring1 and window edge	≥	5.0	μm
GR.15^[NC]	Space between metal ring4 and layout edge	≥	0.0	μm
GR.16^[NC]	Passivation1 slot width, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	≥	2.444	μm
GR.17^[NC]	Space between passivation slot and layout edge	≥	1.556	μm
GR.18^[NC]	Space between passivation slot and Metal ring1 edge	≥	1.0	μm
GR.19^[NC]	Al width above ring1 and ring2, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	≥	4.444	μm
GR.20^[NC]	Al width of ring4, it is allowed $\sqrt{2}$ variation at 45 degree angle area.	≥	5.556	μm
GR.21^[NC]	Space between Al ring	≥	5.0	μm
GR.22^[NC]	Total seal ring width.	≥	26.667	μm
GR.23^[NC]	Chamfer area size at the chip corner, This rule is for customer layout and chip design and apply seal ring by customer	≥	74	μm

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	themselves			
GR.24^[NC]	Chamfer length of ring4 of seal ring in the bevel corner. This rule is for customer layout and chip design. Apply seal ring by SMIC.	≥	74	μm
GR.25^[NC]	Distance from window edges to the point that metal ring4 of seal ring start to bend 45 degree at seal ring corner. This rule is for SMIC to apply seal rings for customer.	≥	94	μm
GR.26^[NC]	Space between first row square via1~via7 and dummy area edge in the die corner dummy relief area	≥	1.299	μm
GR.27^[NC]	Space between metal for die corner dummy pattern for M1 to M8 in the die corner dummy relief area.	≥	0.667	μm
GR.28^[NC]	Space between first column TV1, TV2 and dummy area edge in the die corner dummy relief area.	≥	0.042	μm
GR.29^[NC]	Via distance from each other in dummy relief area.	≥	1.044	μm
GR.30^[NC]	TV1/TV2 distance from each other in dummy relief area.	≥	0.711	μm
GR.31^[NC]	Space between seal ring and chip edge (assembly isolation)	≥	6.667	μm
GR.32^[NC]	Width of P+ beneath CT in seal ring	≥	12.221	μm
GR.33^[NC]	(purposely blank)			
GR.34^[NC]	Space between via slot to the metal ring edge	≥	0.333	μm
GR.35^[NC]	Space between via1~via7 and metal edge in the dummy relief area	≥	0.189	μm
GR.36^[NC]	Space between TM1/TM2/ MTT2 and the dummy pattern edge in the dummy relief area	≥	2.223	μm
GR.37^[NC]	M1~TM2 width in the dummy relief area	≥	0.444	μm
GR.37a^[NC]	MTT2 width in the dummy relief area	≥	1.666	μm
GR.38^[NC]	Space between metal for die corner dummy pattern for TM1, TM2 and MTT2 layer in the die corner dummy relief area	≥	1.778	μm
GR.39^[NC]	Seal ring must be a close ring except RF device.			

Note: The numbers in the above table are GDS drawn dimension before 10% shrink and before OPC. Post OPC data is shown in table-2.

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Table 2 Post OPC key dimension of Seal ring structure

Post OPC Dimension shown below table is used for SMIC maskshop reference. Designers don't need to follow the table.

Rule Number	Description	Operation	Post OPC Dimension	Unit
GRC.1	Contact slot width (fixed) , it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.097	μm
GRC.2	V1-V7 slot width (fixed) , it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.1	μm
GRC.3	TV1, TV2 slot width (fixed) , it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.36	μm
GRC.4	Square CT size (fixed)	=	0.090	μm
GRC.5	Square V1-V7 size (fixed)	=	0.092	μm
GRC.6	Square TV1, TV2 size (fixed)	=	0.36	μm

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7.4.36.2 Seal Ring Check Rules

Rule Number	Description	Operation	Design Value	Unit
GRC.1	Contact slot width (fixed) , it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.06	μm
GRC.2	V1-V7 slot width (fixed) , it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.07	μm
GRC.3	TV1, TV2 slot width (fixed) , it is allowed $\sqrt{2}$ variation at 45 degree angle area.	=	0.36	μm
GRC.4	Square CT size (fixed)	=	0.06	μm
GRC.5	Square V1-V7 size (fixed)	=	0.07	μm
GRC.6	Square TV1, TV2 size (fixed)	=	0.36	μm
GRC.7	M1-M8 width of ring4.	≥	5.556	μm
GRC.8a	M1-M8 width of ring1, ring2 and ring3.	≥	1.666	μm
GRC.8b	TM1, TM2, MTT2 width of ring1.	≥	4.445	μm
GRC.8c	TM1, TM2, MTT2 width of ring 2 and ring3.	≥	1.666	μm
GRC.9	M1~TM2 width in the dummy relief area	≥	0.444	μm
GRC.10	MTT2 width in the dummy relief area	≥	1.666	μm
GRC.11	Space between metal for die corner dummy pattern for M1 to M8 in the die corner dummy relief area.	≥	0.666	μm
GRC.12	Space between metal for die corner dummy pattern for TM1, TM2 and MTT2 layer in the die corner dummy relief area along the vertical direction.	≥	1.777	μm

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7.4.37 Antenna Ratio Effect rules

The "Antenna Ratio Effect" is a common name for the effects of charge accumulation in isolated nodes of an integrated circuit during its processing. This effect is also sometimes called "Plasma Induced Damage"(PID) or "charging effect". In those cases that the discharging of the isolated nodes is done through the thin gate oxide of the transistor, it might cause damage to the transistors and degrade their performance.

Antenna Ratio effect generic prevention rules are intended to reduce gate oxide damage, which was caused when exposed polysilicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler-Nordheim tunneling current to flow through the oxide during high density plasma processing in chip fabrication. Given the known process charge influence, a figure of exposed conductor area to transistor gate area ratio is determined which guarantees Gate Oxide Integrity (GOI) reliability requirements. Failure to consider antenna rules in a design may lead to either reduced performance in transistors exposed to process induced damage, or may lead to total failure if the antenna rules are seriously violated.

Rule No.	DESCRIPTION	Op.	Design Value	Unit
ANT.GT.1	Drawn ratio of field poly perimeter area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V IO1 and 2.5V IO2) connected directly to it	\leq	500	
ANT.GT.2	Drawn ratio of field poly top area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V IO1 and 2.5V IO2) connected directly to it	\leq	250	
ANT.CT.1	Drawn ratio of CT area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V IO1 and 2.5V IO2) connected directly to it	\leq	10	
ANT.MN.1	When a protection diode is not used, the ratio of cumulative metal area to the active poly gate area (0.9/1.1/1.2V Core, 2.5V IO2) from M1 to TM (if double TM used, TM layer defined as TM2 layer)	\leq	5000	
ANT.MN.2	When a protection diode is not used, the ratio of cumulative metal area to the active poly gate area (1.8V IO1) from M1 to TM (if double TM used, TM layer defined as TM2 layer)	\leq	1000	
ANT.MN.3	When a protection diode is used, the ratio of cumulative M1 to Mn (Mn is inter metal layer directly underneath TM2) area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V IO1 and 2.5V IO2) connected directly to it	\leq	diode area*500+ 44000	
ANT.MN.4	When a protection diode is used, the ratio of single TM _n (n=1,2) area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V/2.5V IO) connected directly to it	\leq	diode area*9984+ 55000	
ANT.VN.1	When the protection diode is not used, the drawn ratio of single layer Via area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V/2.5V IO) connected directly to it	\leq	20	
ANT.VN.2	When the protection diode is not used, the drawn ratio of cumulative Via area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V/2.5V IO) connected directly to it	\leq	50	



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Rule No.	DESCRIPTION	Op.	Design Value	Unit
ANT.VN.3	When the protection diode is used, the drawn ratio of cumulative Via area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V IO1 and 2.5V IO2) connected directly to it.	\leq	diode area * 200 + 1000	
ANT.PA.1	When the protection diode is not used, the drawn ratio of PA area to the active poly gate area (1.8V/2.5V IO) connected directly to it	\leq	20	
ANT.PA.2	When the protection diode is not used, the drawn ratio of PA area to the active poly gate area (0.9/1.1/1.2V Core) connected directly to it	\leq	200	
ANT.PA.3	When the protection diode is used, the drawn ratio of PA area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V/2.5V IO) connected directly to it	\leq	diode area * 100 + 400	
ANT.AL.1	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the active poly gate area (1.8V/2.5V IO) connected directly to it	\leq	1000	
ANT.AL.2	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the active poly gate area (0.9/1.1/1.2V Core) connected directly to it	\leq	2000	
ANT.AL.3	When the protection diode is used, the drawn ratio of ALPA side-wall area to the active poly gate area (0.9/1.1/1.2V Core, 1.8V/2.5V IO) connected directly to it	\leq	diode area * 8500 + 30000	

Note:

1. Designer should select proper ALPA thickness in antenna rule DRC execution. At present there are 2 kinds of ALPA thickness for selection: 14.5k A and 28k A. The default selection is 14.5k A.

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A. The definition of Field Poly Perimeter antenna ratio

$$\text{Ratio} = 2[(L+W1)x t] / (W2 \times l)$$

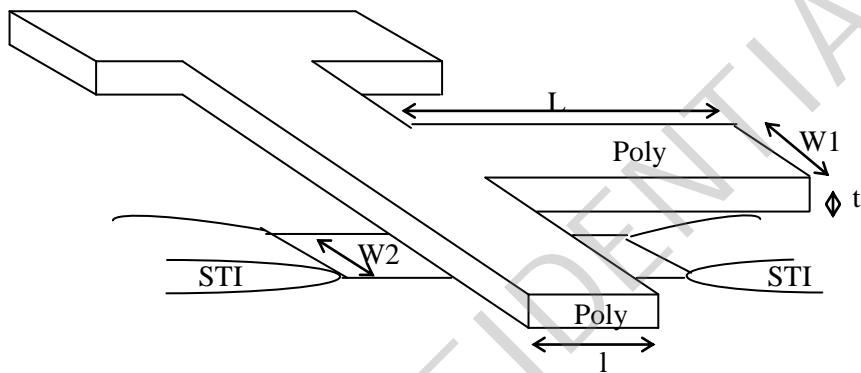
L : floating field poly length connected to gate

W1 : floating field poly width connected to gate

t : field poly thickness (poly thickness refer to document No. TD-LO40-SP-2001)

W2 : connected transistor channel width

l : connected transistor channel length



B. The definition of Field Poly Top Area antenna ratio is

$$\text{Ratio} = (\text{Apoly}) / (W2 \times l)$$

Apoly : Effective poly area that is electrically connected to gate.

C. The definition of CT, Via1-Via7 antenna ratio is

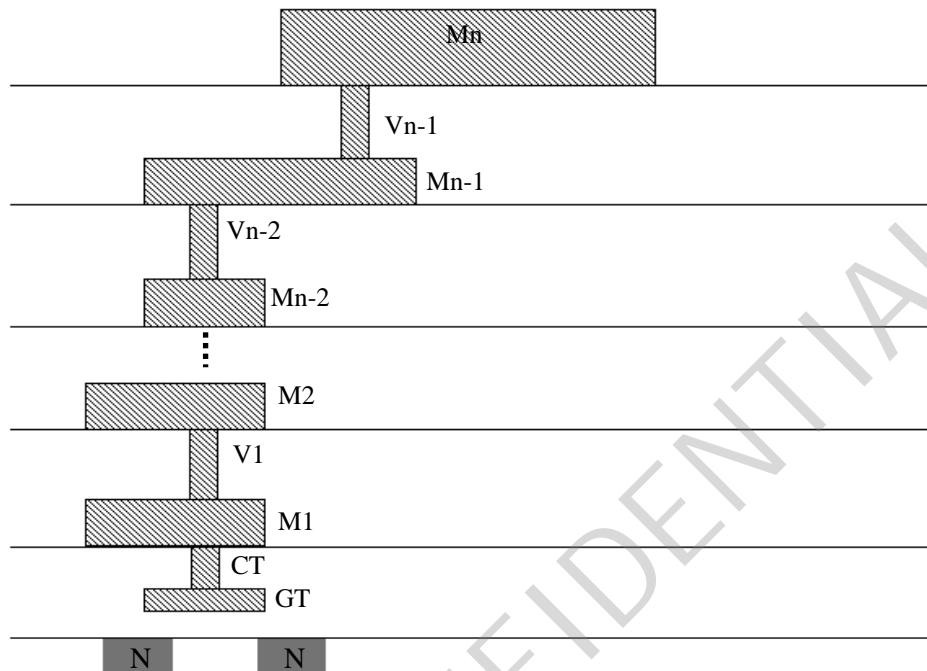
$$\text{Ratio} = \{\text{total CT (Via) area}\} / (W2 \times l)$$

D. The definition of Cumulative Metal antenna ratio is

$$\text{Ratio} = (A_{M1} + \dots) / (W2 \times l)$$

A_{Mx} : Effective metal(x) area that is electrically connected to gate without using Metal(x+1), and not to connected to active area. Cumulative Metal antenna ratio is relative to total effective metal layer area.

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•In case of n-level metal (I)

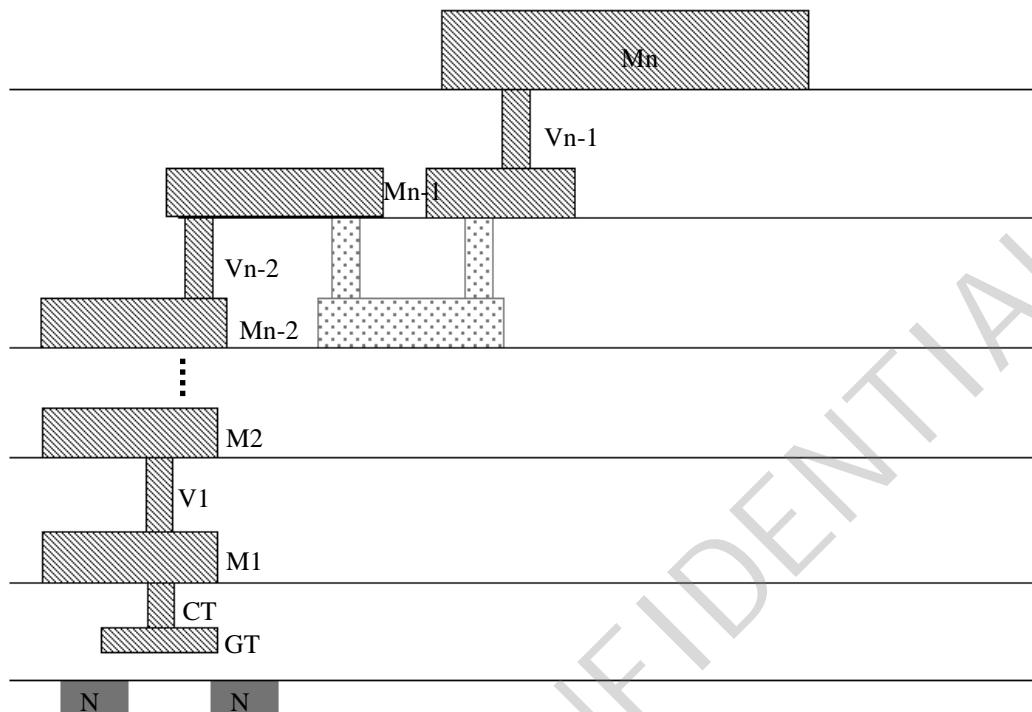
[Horizontal hatching] Antenna area without protection diode. The antenna is cumulated.

[Brick pattern] Antenna area with protection diode. The antenna is cumulated.

[Dotted pattern] Metal/via in re-route but not included in antenna calculation.

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•In case of n-level of metal (II)



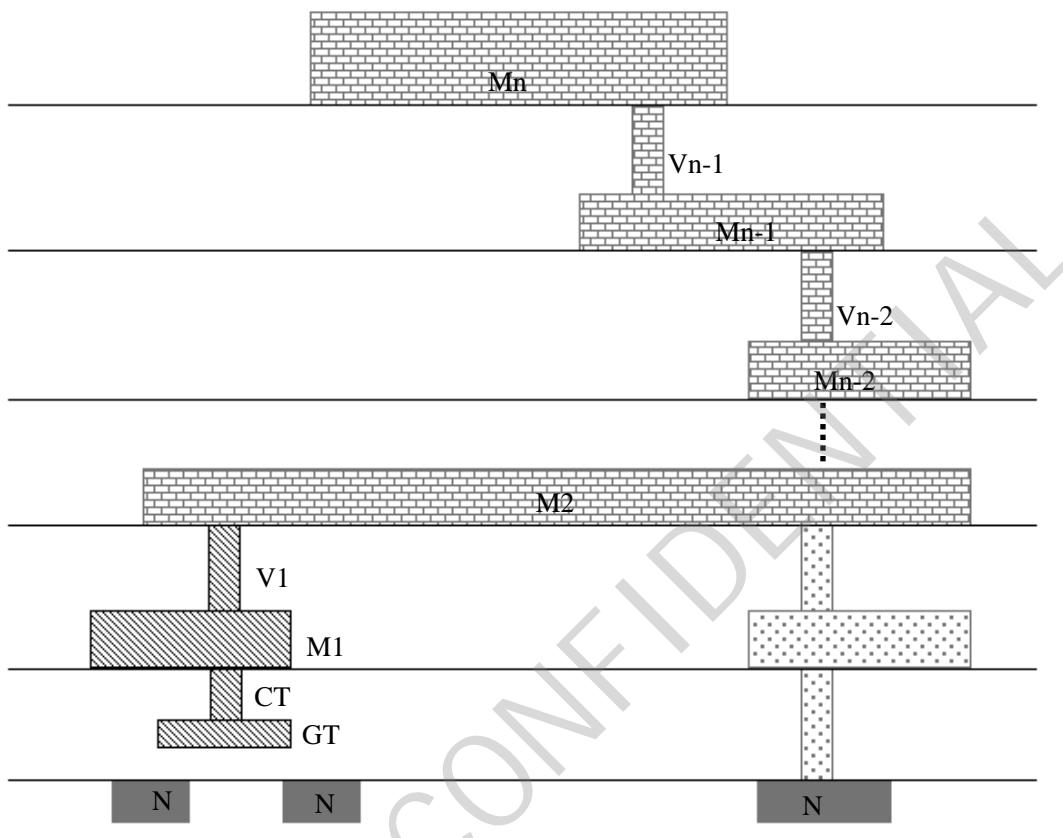
Antenna area without protection diode. The antenna is cumulated.

Antenna area with protection diode. The antenna is cumulated.

Metal/via in re-route but not included in antenna calculation.

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•In case of n-level metal (III)



[Hatched Box] Antenna area without protection diode. The antenna is cumulated.

[Brick Pattern Box] Antenna area with protection diode. The antenna is cumulated.

[Dotted Pattern Box] Metal/via in re-route but not included in antenna calculation.

E. The definition of the effective diode area is:
 $((SN \text{ OR } SP) \text{ AND } AA) \text{ NOT } GT$

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7.5 DFM Rules

7.5.1 Introduction:

All the recommendations have been listed in the following DFM rules' section, it is recommended to follow them as much as possible, which can achieve large process window, better device and reliability performance, and higher yield.

DFM rules have been grouped with different priority levels. Higher priority indicates higher risk of manufacturability and yield loss when the rule is not obeyed. Users should follow DFM priority 1 and priority 2 rules strictly, DRC clean of DFM priority 1 and priority 2 rules is must for tape-out, if users intend to waive a violation of a priority 1 and priority 2 rules for any reason, need to review with SMIC before waiver. Priority 3 rules also impact manufacturability and yield, but they are not the gating items for tape-out.

7.5.2 DFM Rules Description

Rule number	Description	Priority	Concern	Operation	Design Value	DRC switch default setting
NW.11 ^[R]	N+AA adjacent both two edges space opposite to NW. Both of two adjacent edges space to NW smaller than rule value is not permitted.	3	Process	≥	0.16	on
NW.12 ^[R]	NW enclosure opposite of P+AA adjacent both two edges. Both of two adjacent edges enclosed by NW smaller than rule value is not permitted.	3	Process	≥	0.16	on
NW.17 ^[R]	For parallel long NW (length > 50 μm), must make NW width larger than 0.89 μm or NW to NW space larger than 0.89 μm. If this area passed AA density DRC check, this rule can be waived This rule is not applied for (DNSRAM OR LRSRAM) OR D2SRAM) OR RFSRAM) covered region.	3	Process	≥	0.89	off
PSUB.16 ^[R]	It's not allowed P+ GATE in PSUB. DRC doesn't check INDMY region.	3	Device			on
AA.4e ^[R]	Space between (AA or AADUM) DRC check maximum STI width. DRC don't check: chip corner DUMBA region as defined in rule CORN.2 if seal ring is added by SMIC.	3	Process	≤	10	on
AA.10 ^[R]	DG, TG or core transistors mixed in the same AA are prohibited	3	Device			on
AA.12 ^[R]	AA channel width of NMOS/PMOS for 0.9/1.1/1.2V transistor. Waive transistor inside VARMOS	3	Device	≤	50	on
AA.13a ^[R]	Enclosed area when AA all of inner edge length < 0.21 μm. This rule is not applied for (DNSRAM OR LRSRAM) OR D2SRAM) OR RFSRAM) covered region.	3	Process	≥	0.077	off
AA.15 ^[R]	AA density overlap by DUMBA. Density check window size 200 μm*200 μm with step size 100 μm	3	Process	≥	20%	off
				≤	80%	
AA.23 ^[R]	For any geometry on AA, NW, GT, M1, or Mn (n=2~8), an edge of length < 1.0xWmin cannot have any adjacent edge with length < 1.0xWmin	3	OPC	<	Wmin (minimum width)	off



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Rule number	Description	Priority	Concern	Operation	Design Value	DRC switch default setting
A.A.C.5 ^[R]	Space between gate and minimum 50*50um LDA Waive if the gate channel length $\geq 0.06 \mu\text{m}$	3	Process	\geq	20	off
GT.1a ^[R]	GT channel length for 0.9/1.1/1.2V N/P MOS transistors (std, high, or low VT)	3	Process	\geq	0.044	off
GT.2b ^[R]	Non-floating poly outside of (extend AA $W \geq 2.5 \mu\text{m}$) region width. This rule is not applicable for GT interacting with EFUSE (81;2).	3	Process	\geq	0.06	off
GT.5a ^[R]	Extension of AA outside of GT. Exclude gate within LDMOS region (layer: LDBK) and within inductor area (layer: INDMY).	3	OPC	\geq	0.07	off
GT.6a ^[R]	Extension E of GT outside of AA to form poly end-cap. The GT to L shape AA (in the same MOS) space $S < 0.1 \mu\text{m}$. The L shape AA height $h > 0.02 \mu\text{m}$. This rule is not applied for (DNSRAM OR LSRAM) OR D2SRAM OR RFSRAM) covered region.	3	Device	\geq	0.11	off
GT.6b ^[R]	Extension of poly outside of AA to form poly end-cap. Exclude inside inductor (layer: INDMY) and exclude inside LDMOS(layer: LDBK).	3	Device	\geq	0.1	off
GT.17a ^[R]	GT area when GT all of edge length $< 0.21 \mu\text{m}$	3	Process	\geq	0.055	off
GT.18a ^[R]	Enclosed area when GT all of inner edge length $< 0.21 \mu\text{m}$	3	Process	\geq	0.077	off
GT.24b ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $\leq 0.45 \mu\text{m}$, and L-shape GT length ($L \geq 0.055 \mu\text{m}$), space between L-shaped GT to AA in the same MOS. (Waive the violations in SRAM area)	3	Device	\geq	0.05	off
GT.24c ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $> 0.45 \mu\text{m}$, and L-shape GT length ($L \geq 0.055 \mu\text{m}$), space between L-shaped GT to AA in the same MOS.	3	Device	\geq	0.05	off
GT.25b ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $\leq 0.45 \mu\text{m}$, space between L-shaped AA to GT in the same MOS. (Waive the violations in SRAM area)	3	Device	\geq	0.05	off
GT.25c ^[R]	If channel length $< 0.2 \mu\text{m}$, channel width $> 0.45 \mu\text{m}$, space between L-shaped AA to GT in the same MOS	3	Device	\geq	0.05	off
GT.32 ^[R]	Poly interacting AA must separate at least two AA diffusions (exclude dummy pattern). DRC doesn't check: 1. (DNSRAM OR LSRAM) OR D2SRAM OR RFSRAM), LDBK, LOGO and INDMY covered region. 2. When AA or poly not interact with CT.	3	Device			off
GT.33 ^[R]	Floating Real Gate is not allowed if the effective	3	Device			off

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Rule number	Description	Priority	Concern	Operation	Design Value	DRC switch default setting
	<p>source/drain is not connected together.</p> <p>Definition of floating Real Gate:</p> <ol style="list-style-type: none"> 4. Real Gate without CT on poly. 5. Real Gate with CT on poly but not connect to MOS AA, pickup or PAD. 6. It is not a floating Real Gate if the Real Gate is connected to AA by butted CT in (DNSRAM OR LRSRAM) OR D2SRAM) OR RFSRAM) covered region. <p>Definition of effective source/drain:</p> <p>Source/drain is connected to different (MOS AA NOT poly), pickup, Real Gate or PAD.</p> <p>This rule is only used to check chip level GDS.</p>					
GT.34 ^[R]	Distance from poly to a perpendicular AA "U" inside vertex, where the AA vertex distance is $\leq 0.210\mu\text{m}$.	3	OPC	\geq	0.09	off
GT.35 ^[R]	poly overlap past AA when poly to AA inner vertex distance $< 0.040\mu\text{m}$.	3	OPC	\geq	0.13	off
DG.11 ^[R]	AA (enclosed by DG) overlap past poly	3	Device	\geq	0.17	on
TG.11 ^[R]	Extension of AA in TG outside of gate. Exclude gate within LDMOS region(within LDBK) and within inductor area(layer INDMDY)	3	Device	\geq	0.15	on
SAB.16 ^[R]	SAB overlap of GATE is not allowed (except ESDIO1, ESDIO2, ESDHV, OCOVL region).	3	Device			off
CT.3 ^[R]	CT array space to CT array for run length $> 0.34\mu\text{m}$. CT array is formed by logic operation (((all CTs su0.09) sd0.3) su0.21).	3	Process, OPC	\geq	0.18	off
CT.4 ^[R]	Space between AA region and contact overlap poly	3	Process	\geq	0.05	off
CT.5 ^[R]	0.9/1.1/1.2V device space between poly region and contact overlap AA	3	Process	\geq	0.05	off
M1.1 ^[R]	M1 width.	3	Process	\geq	0.08	off
M1.3 ^[R]	M1 space	3	Process	\geq	0.08	off
M1.6 ^[R]	Space between two (run length $> 0.3 \mu\text{m}$) parallel M1 lines with both metal lines width $> 0.22 \mu\text{m}$.	3	Process	\geq	0.12	off
M1.7a ^[R]	CT minimum within M1	3	OPC	\geq	0.025	off
V1.5 ^[R]	V1 (different net) space (outside of SRAM) for run length $> 0\mu\text{m}$	3	Process reliability	\geq	0.11	off
Mn.1 ^[R]	Mn width.	3	Process	\geq	0.08	off
Mn.3 ^[R]	Mn space	3	Process	\geq	0.08	off
Mn.6 ^[R]	Space between two (run length $> 0.3 \mu\text{m}$) parallel Mn(n=2~8) lines with both metal lines width is $> 0.22 \mu\text{m}$.	3	Process	\geq	0.12	off
Mn.7d ^[R]	[(Mn with width $> 2.8\mu\text{m}$) over M(n-1)] density (%) with $200\mu\text{m} \times 200\mu\text{m}$ step size $100\mu\text{m}$ where n = 2-8 and (n-1) = metal level below.	3	Process	\leq	70%	on

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Rule number	Description	Priority	Concern	Operation	Design Value	DRC switch default setting
Mn.7e ^[R]	[M(n + 1) over [Mn with width > 2.8μm] density (%) with 200μm*200μm step size 100μm, where n = 1-7 and n + 1 = metal level above]	3	Process	≤	70%	on
Mn.12 ^[R]	Minimum Mn to Mn space S at Mn line-end. Width W < 0.1um. The minimum space can be line end head to other Mn or line end side to other Mn. Rule check: S >= (Dh or Ds). E1 =0.03, K1=0.095, Dh=Ds=0.1 in the illustration. Outside of SRAM (INST) area. Waive extrusion F < 0.07. Waive the violation for MOM (within MOMDMY).	3	Process	≥	0.1	off
Mn.13 ^[R]	It is not allowed to have local density > 85% of all 3 consecutive metal (M1/Mn, Mn+1 and Mn+2) over any window size 62.5*62.5um (stepping size 31.25um). f) The metal layers include M1/Mn and dummy metals. g) This rule doesn't check DUMBMB, MARKS and (TM2 and PA) region.	3	Process			off
Vn.5 ^[R]	Vn(n=2~7) space in different net for run length > 0μm(outside of SRAM)	3	Process reliability	≥	0.11	off
Vn.22 ^[R]	Via (Vn, TV1) insertion, n=1~7. Insert one Vn if single Vn and (Wn>=5Wn+1, or Wn+1>=5Wn) at enclosure. (Reference condition is continuous heating 168hours, and temperatures 200°C,.)	3	Process reliability			off
Vn.23 ^[R]	At least two vias (Vn, TV1, TV2, n=1~7) in Mn and Mn+1 (M1, Mn, n=2~8, TM1, TM2) intersection area. (This rule is not applicable for SRAM region, but SRAM region should follow main rule: V1.17, Vn.17, TV1.13, TV2.13, TV2.14)	3	Process, yield			off
MTT2.5 ^[R]	Space from MTT2 used as Inductor to other MTT2 region	3	Process	≥	30	on
MTT2.2a ^[R]	Space between two MTT2s having parallel segment larger than 2 μm with one or both MTT2 width larger than or equal to 16 μm	3	Process	≥	2	on
MTT2.7b ^[R]	INDMY area density in window size 840 μm*840 μm with step 420um	3	Process	≤	20%	on
MTT2.9 ^[R]	Extension of dummy layer "INDMY" beyond MTT2 region used as Inductor	3	Device	≥	15	on
MTT2.13 ^[R]	At least 2 TVs with space ≤ 1.7 μm are required to connect MTT2. (Please add vias as many as possible which is for reliability concern and RF application)	3	Process reliability			off
MD.4 ^[R]	MD (PA2) must be within BORDER (CHIP EDGE)	3	Process	≥	8	off

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Rule number	Description	Priority	Concern	Operation	Design Value	DRC switch default setting
MD.6 ^[R]	MD (PA2) wire-bond pad opening, MD edge space to BORDER (CHIPEDGE).	3	Process	\leq	200	off
ESD.9a ^[R]	Recommended CT enclosure by ESD1	3	Device	\geq	0.4	off

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7.6 SRAM Rules

7.6.1 Guideline for SRAM rules:

The area covered by INST should follow SRAM rules if these rules are redefined in SRAM rule

The area covered by INST should follow the common rule also if this rule is not redefined in SRAM rule

7.6.2 Cell transistor Dimensions

The dimensions mentioned are layout drawn dimensions.

SP299 and DP589 are LL (low leakage) bit cells; SP374 and DP741 are HP (high performance) bit cells

Single Port SRAM

Device	Gate	PG	PD	PU
0.299(um2) SRAM	Ld (um)	0.059	0.055	0.055
	Wd (um)	0.11	0.142	0.06
0.374(um2) SRAM	Ld (um)	0.063	0.055	0.055
	Wd (um)	0.183	0.233	0.07

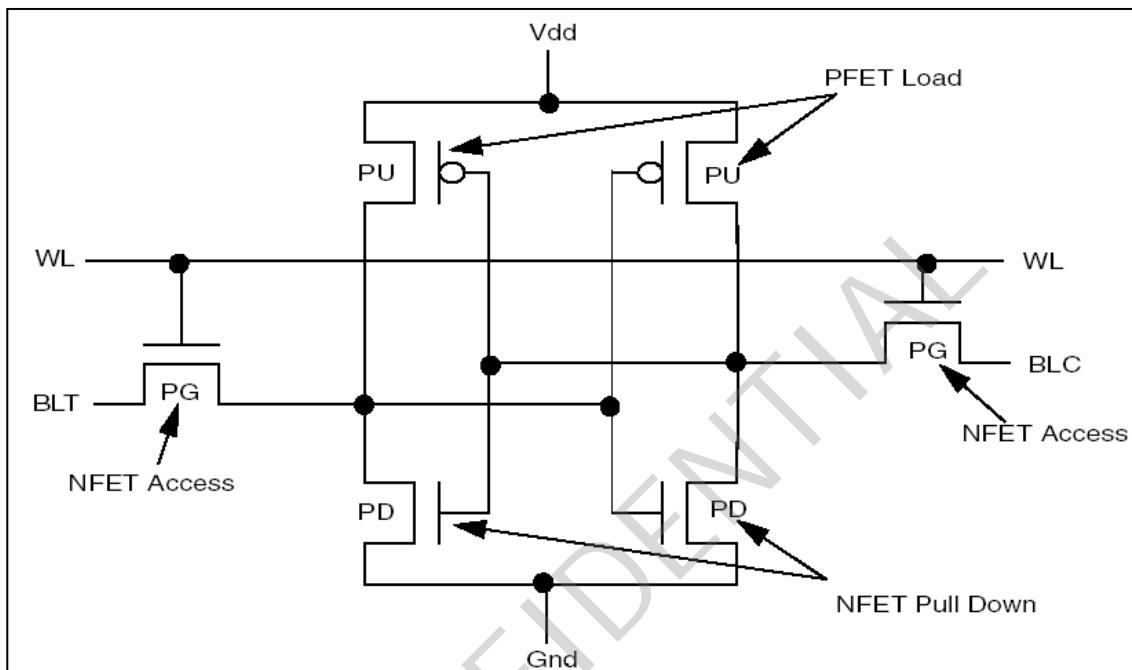
Dual Port SRAM

Device	Gate	PG	PD	PU
0.589(um2) SRAM	Ld (um)	0.067	0.055	0.055
	Wd (um)	0.154	0.305	0.06
0.741(um2) SRAM	Ld (um)	0.063	0.055	0.055
	Wd (um)	0.168	0.438	0.08

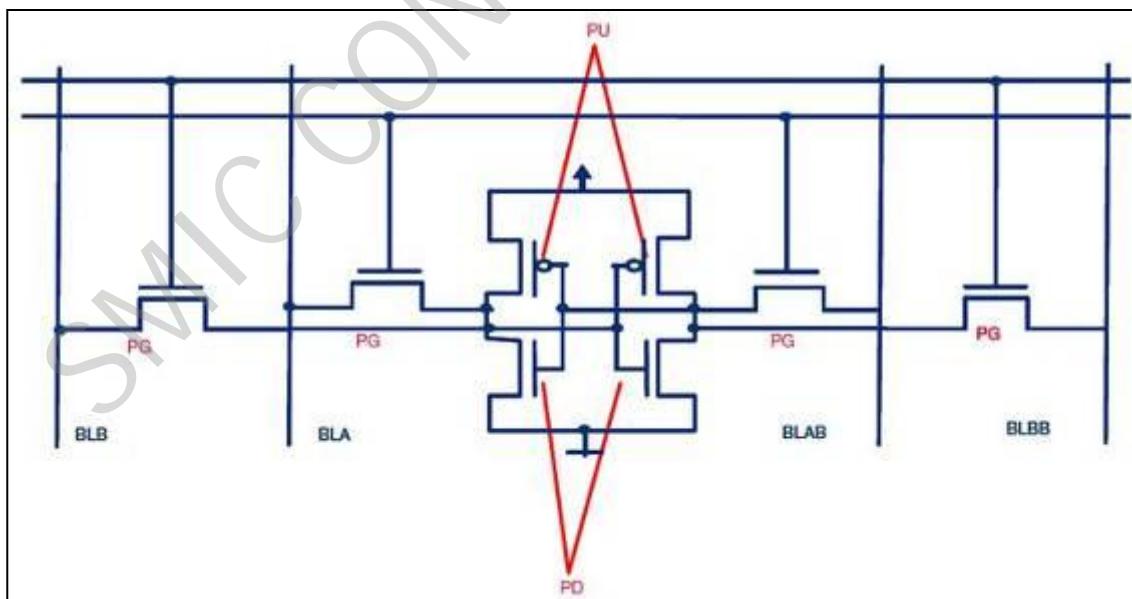
Doc. No.: TD-LO40-DR-2001	Doc. Title: 40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage And Generic Design Rule	Doc.Rev:4	Tech Dev Rev: 1.10	Page No.: 214/299
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7.6.3 Design of SRAM Cells

Single Port 6T SRAM



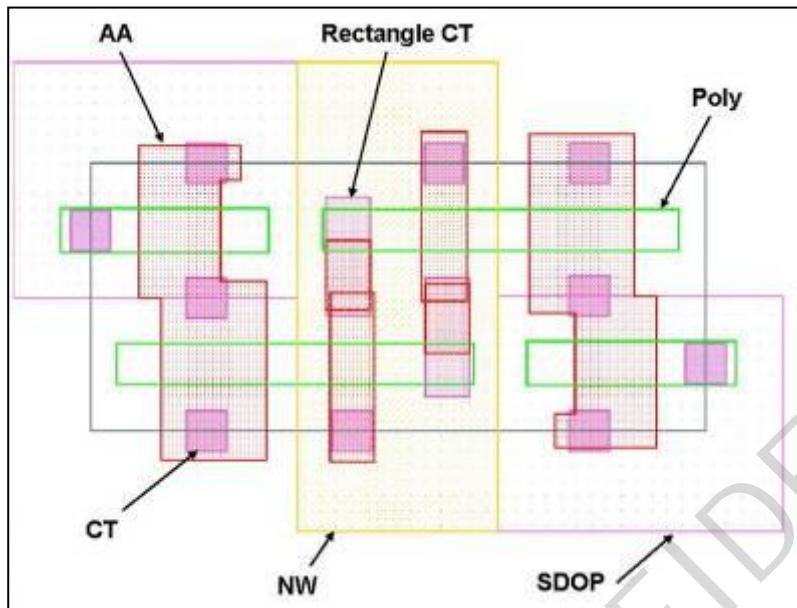
Dual Port 8T SRAM



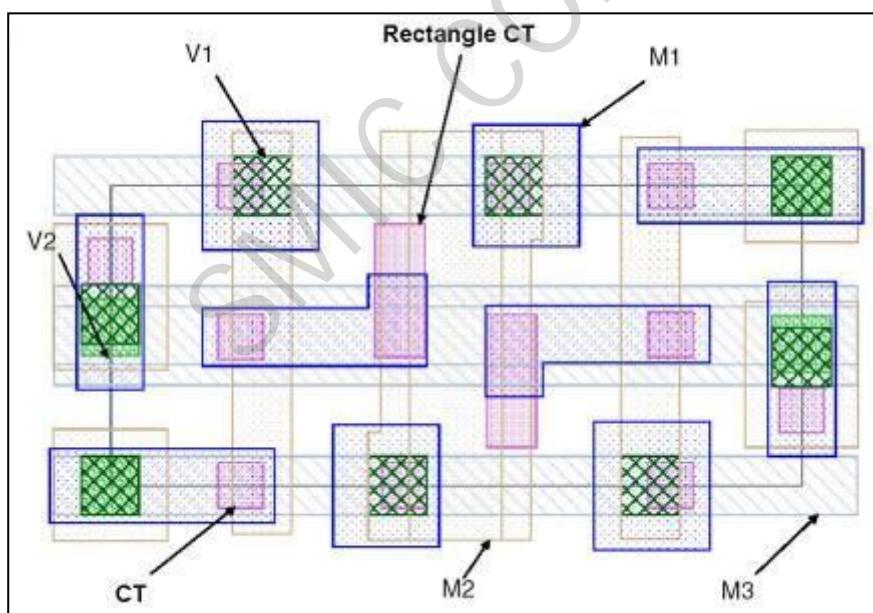
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7.6.4 Design of single port and Dual port SRAM cell

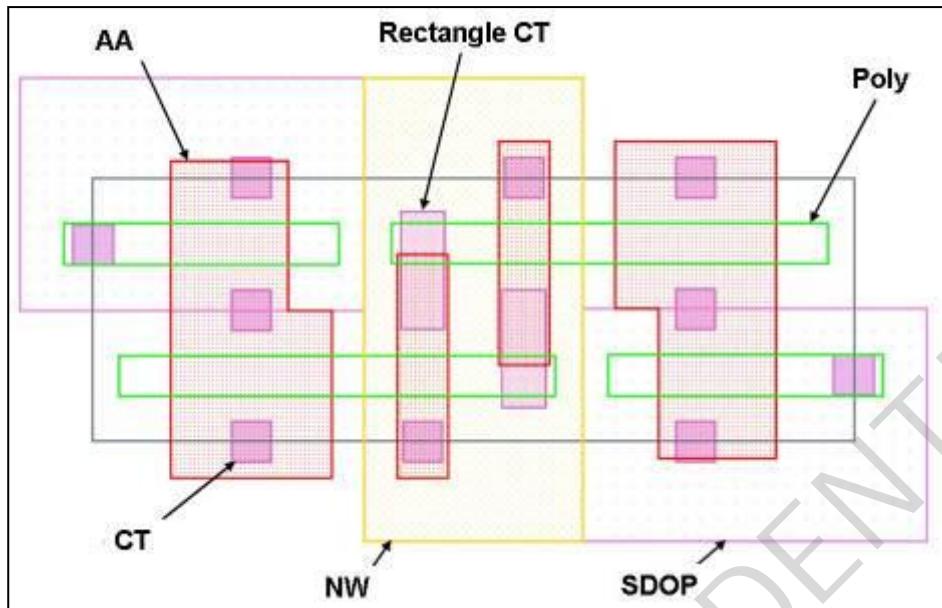
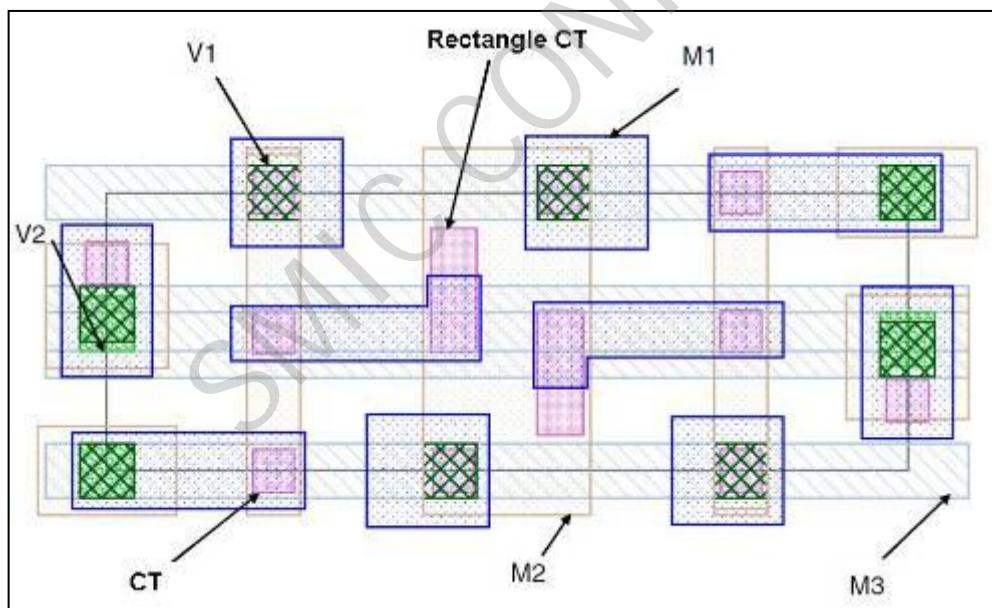
Single Port 0.299 SRAM layout (FEOL)



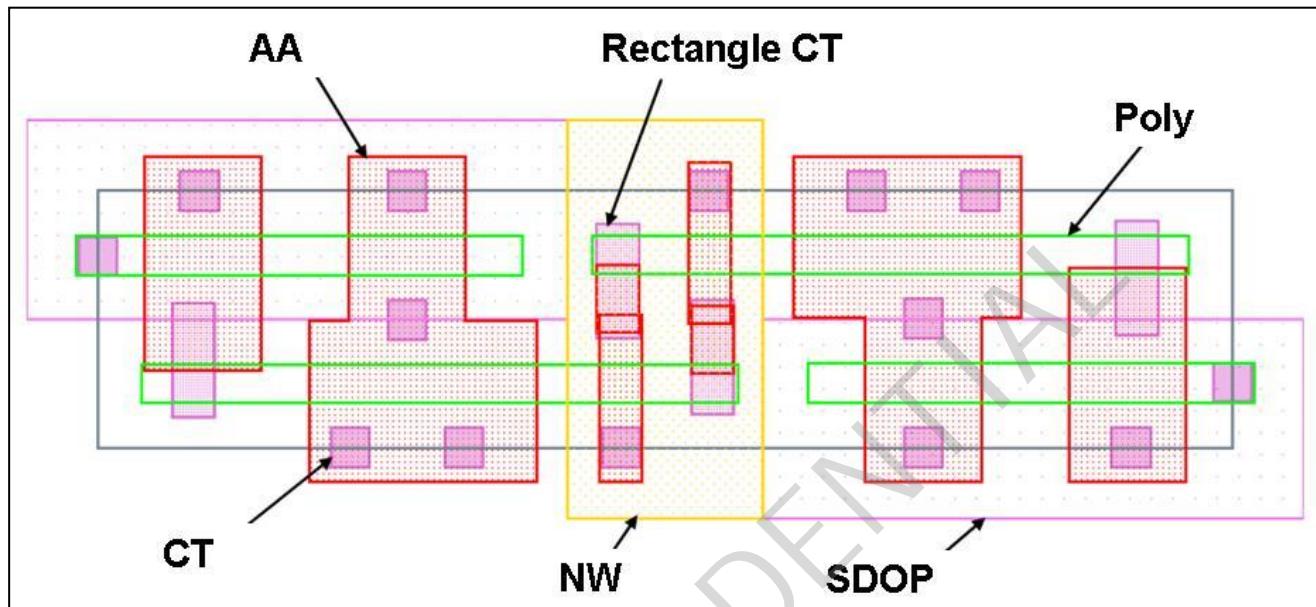
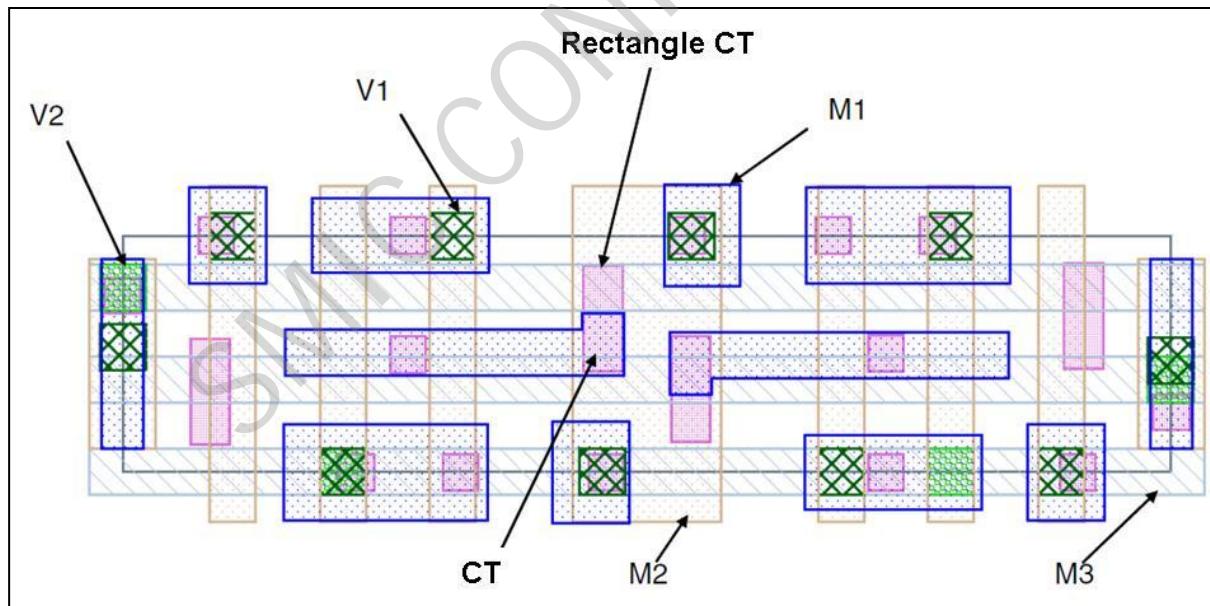
Single Port 0.299 SRAM layout (BEOL)



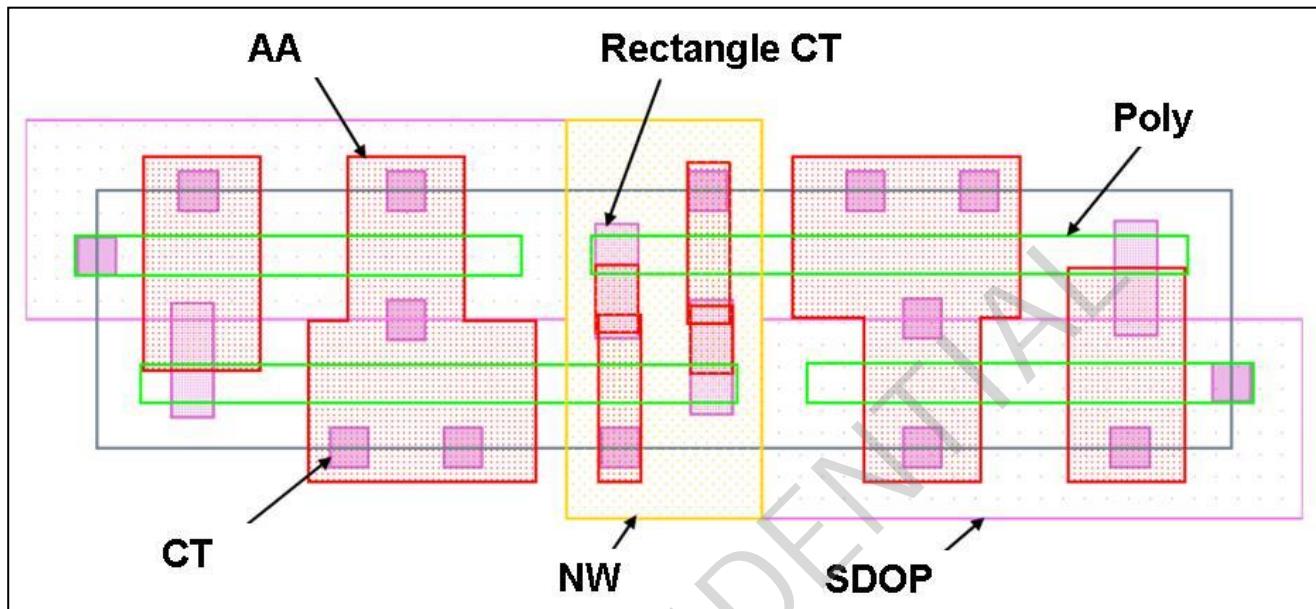
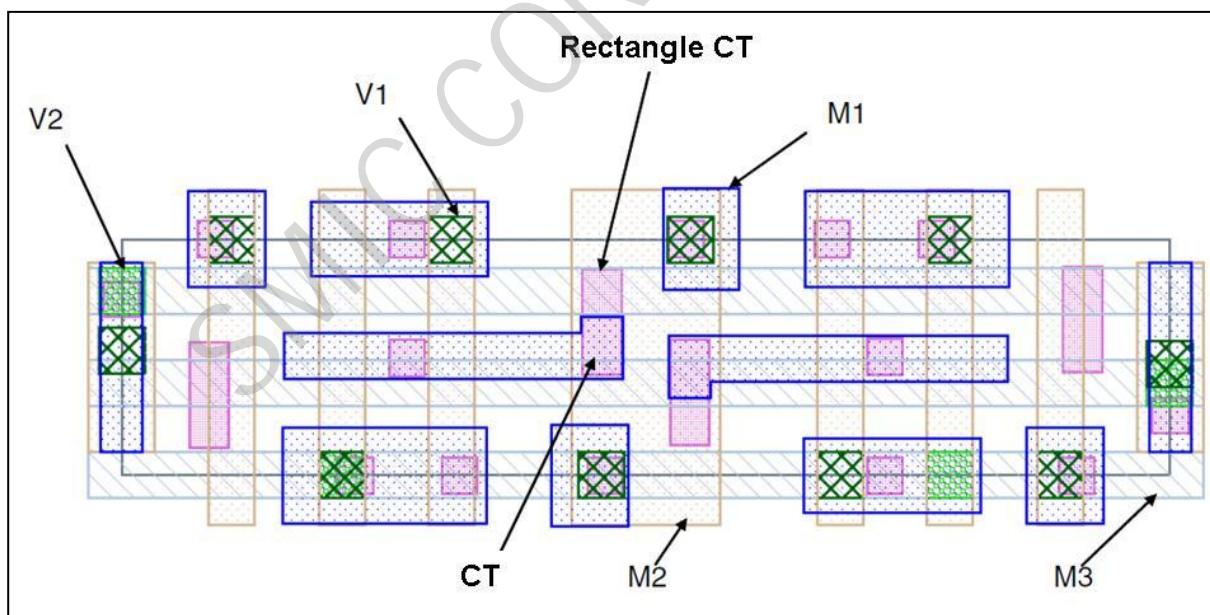
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Single Port 0.374 SRAM layout (FEOL)**Single Port 0.374 SRAM layout (BEOL)**

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Dual Port 0.589 8T SRAM (FEOL)

Dual Port 0.589 8T SRAM (BEOL)


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Dual Port 0.741 8T SRAM (FEOL)

Dual Port 0.741 8T SRAM (BEOL)




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7.6.5 SRAM Layout Rule Description**7.6.5.1 SRAM AA: Active Area Rules**

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRAA.1a	No need to follow common rule								
SRAA.1sa	AA inner vertex to inner vertex distance	\geq	NA	0.046	0.168	0.06	0.08	0.046	μm
SRAA.4	(Purposely blank)								
SRAA.4a	AA space	\geq	0.08	0.069	0.068	0.069	0.065	0.065	μm
SRAA.4b	(Purposely blank)								
SRAA.4c	AA with gate space along gate poly direction, if one of AA width $(W3) \geq 0.14 \mu\text{m}$, and AA to AA run length $Y2 \geq 0.14 \mu\text{m}$	\geq	0.1	0.085	0.086	0.09	0.104	0.085	μm
SRAA.6sa	Space between NW outer vertex and N+AA inside PW outer vertex	\geq	NA	0.037	NA	0.04	NA	0.037	μm
SRAA.9	AA area	\geq	0.02					0.015	μm^2



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7.6.5.2 SRAM NW: N-Well Implant Layer Rule

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRNW.1	NW width	\geq	0.33	0.275	0.294	0.279	0.3	0.27	μm
SRNW.3	(purposely blank)								
SRNW.13	NW enclosure of N+AA	\geq	0.08	0.042	0.042	0.027	0.027	0.027	μm
SRNW.14	Space between NW and N+AA inside PW	\geq	0.08	0.042	0.042	0.045	0.045	0.04	μm
SRNW.15	NW enclosure of P+AA	\geq	0.08	0.038	0.043	0.04	0.046	0.037	μm

7.6.5.3 SRAM SDOP: SRAM Pass Gate

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRDOP.101	Gate touching SDOP must be covered by SDOP		NA						
SRDOP.102	SDOP width	\geq	NA	0.272	0.317	0.38	0.195	0.18	μm
SRDOP.103	SDOP area	\geq	NA	0.152	0.236	0.333	0.204	0.1	μm^2
SRDOP.104	SDOP must be in INST		NA						
SRDOP.105	SDOP enclosure of Real Gate	\geq	NA	0.061	0.057	0.056	0.066	0.056	μm

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7.6.5.4 SRAM GT: Poly Rules

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRGT.3	Space between two poly on field	\geq	0.1	0.072	0.072	0.07	0.106	0.07	μm
SRGT.4	Space between AA and poly on field oxide, floating poly need not follow this rule	\geq	0.03	0	0.013	0	0	0	μm
SRGT.5	Extension of AA outside of Real Gate	\geq	0.06	0.045	0.058	0.045	0.052	0.045	μm
SRGT.6	Extension of poly outside of AA to form poly end-cap, floating poly need not follow this rule, area interacted with rectangle contact need not follow this rule.	\geq	0.09	0.06	0.061	0.055	0.078	0.055	μm
SRGT.7	(poly_end with length < 0.120 μm) space to (poly_end with length < 0.120 μm) (head to head space) must be: , excluding floating poly. The head to head with run length > 0	\geq	0.1	0.072	0.072	0.09	0.102	0.07	μm
SRGT.10	For GT channel length \geq 0.06, Real Gate space to (GT or GTDUM).	\geq	0.13	NA	0.121	0.128	0.131	0.12	μm
SRGT.1a, SRGT.8, SRGT.9, SRGT.13, SRGT.14, SRGT.17, SRGT.21, SRGT.102, SRGT.101, SRGT.103 rules are purposely blank									



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7.6.5.5 SRAM SN: N+ S/D Implant Layer Rule

RULE NO.	Description	Oper ation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRSN.3a	Space between SN and P+ AA inside NW, except AA resistor. (run length > 0.1 μm)	≥	0.08	0.043	0.043	0.045	0.046	0.043	μm
SRSN.3b	Space between SN and P+ AA inside NW, except AA resistor. (run length <= 0.1 μm)	≥	0.05	0.038	0.081	0.04	0.098	0.038	μm
SRSN.4	Space between SN and P+ pick-up AA	≥	0.02	0	0.05	0	0.03	0	μm
SRSN.10	N+AA enclosure by SN (not include pick up AA)	≥	0.08	0.042	0.041	0.045	0.053	0.041	μm
SRSN.10sa	N+AA enclosure by SN(Not apply to AA along S/D direction), N+AA outer vertex to SN inner vertex	≥	NA	0.037	NA	0.04	NA	0.037	μm
SRSN.16	SN area	≥	0.11	>0.11	0.082 ₃	>0.11	>0.11	0.0823	μm ²
SRSN.18	Enclosed area of SN	≥	0.11	0.072 ₈	0.208 ₈	0.103 ₅	0.167 ₈	0.0728	μm ²
SRSN.1, SRSN.2, SRSN.3#a, SRSN.6, SRSN.7a, SRSN.7b, SRSN.22#a are purposely blank									

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7.6.5.6 SRAM SP: P+ S/D Implant Layer Rule

RULE NO.	Description	Oper ation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRSP.3a	Space between SP and N+ AA inside PW, except AA resistor. (run length > 0.1 μm)	≥	0.08	0.042	0.041	0.045	0.053	0.041	μm
SRSP.3b	Space between SP and N+ AA inside PW, except AA resistor. (run length <= 0.1 μm)	≥	0.05	0.037	NA	0.04	NA	0.037	μm
SRSP.10	SP enclosure of P+AA (not include pick up AA)	≥	0.08	0.038	0.043	0.04	0.046	0.038	μm
SRSP.12	SP enclosure of P+ pickup AA	≥	0.02	0	0.045	0	0.03	0	μm
SRSP.16	SP area	≥	0.11	0.072 ₈	0.092 ₄	0.103 ₅	0.115 ₉	0.072	μm ²
SRSP.1, SRSP.2, SRSP.3#a, SRSP.6, SRSP.7a, SRSP.7b, SRSP.7ba, SRSP.15#a, SRSP.20, SRSP.19 are purposely blank									

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7.6.5.7 SRAM CT: Contact Layer Rules

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRCT.2a	Space between two contacts on different net	≥	0.10		0.11	0.088	>0.10	0.088	μm
SRCT.4	Space between AA region and contact overlap poly	≥	0.04	0.036	0.051	0.036	0.036	0.032	μm
SRCT.5	Space between Gate and contact overlapping AA	≥	0.04	0.031	0.028	0.033	0.035	0.028	μm
SRCT.102	CT space to V1 on different net	≥	NA	0.092	0.116	0.075	0.088	0.075	μm
SRCT.2, SRCT.3, SRCT.6aa, SRCT.7a, SRCT.10, SRCT.18, SRCT.101, SRCT.105 are purposely blank									

7.6.5.8 SRAM RCT: Rectangle contact in SRAM Layer Rule

RCT is defined as 60nm*160nm Rectangle CT in SRAM Bit cell.

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRRCT.101	Rectangle CT width	=	NA	0.06	0.06	0.06	0.06	0.06	μm
SRRCT.102	Rectangle CT length	=	NA	0.16	0.16	0.16	0.16	0.16	μm
SRRCT.103	Rectangle CT space to Rectangle CT	≥	NA	0.074	0.078	0.074	0.09	0.074	μm
SRRCT.104	(purposely blank)								
SRRCT.104c	Rectangle CT space to CT inside INST with touching prohibited	≥	NA	0.07	0.08	0.071	0.089	0.07	μm
SRRCT.106	Rectangle CT end space to AA (with run length>0)	≥	NA	0.133	0.133	0.135	0.143	0.133	μm
SRRCT.106a	Rectangle CT side space to AA	≥	NA	0.069	0.073	0.069	0.075	0.069	μm
SRRCT.107	Rectangle CT end space to Poly	≥	NA	0.037	0.039	0.055	0.045	0.037	μm
SRRCT.107a	Rectangle CT side space to Poly	≥	NA	0.082	0.087	0.105	0.189	0.082	μm
SRRCT.108	Rectangle CT space to M1	≥	NA	0.057	0.063	0.063	0.077	0.057	μm

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7.6.5.9 SRAM Metal 1 Rules

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRM1.3sa	distance between M1 outer vertex to outer vertex	\geq	0.07	0.0646	0.0689	0.08	0.08	0.064	μm
SRM1.4	M1 area	\geq	0.0196	0.0168	0.0203	0.0203	0.0222	0.0168	μm^2
SRM1.7a	CT minimum within M1, not applicable to rectangle CT	\geq	0	0	0.002	0	0.002	0	μm
SRM1.7b	M1 overlap past CT for two opposite sides with either side $\geq 0\mu\text{m}$ and $< 0.015\mu\text{m}$, not applicable to rectangle CT	\geq	0.025	0.017	0.025	0.025	0.015	0.012	μm

7.6.5.10 SRAM Via1 Rules

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap Cell	Design Value	Unit
SRV1.6a	V1 minimum within M1	\geq	0.015	0.005	0.001	0	0.003	0	μm
SRV1.6c	M1 overlap past V1 for two opposite sides with the other two sides $\geq 0\mu\text{m}$.	\geq	0.03	>0.03	>0.03	>0.03	0.015	0.015	μm
SRV1.7c, SRV1.8 are purposely blank									



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7.6.5.11 SRAM M2 Rules

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRM2.3	M2 space	\geq	0.07	0.07	0.07	0.065	0.07	0.065	μm
SRM2.4	M2 area	\geq	0.0196	0.0192	0.0205	0.0322	0.0379	0.0192	μm^2

7.6.5.12 SRAM Via2 Rules

RULE NO.	Description	Operation	Base Rule	299 Strap and Cell	374 Strap and Cell	589 Strap and Cell	741 Strap and Cell	Design Value	Unit
SRV2.6a	V2 minimum within Mn	\geq	0.015	0	0	0	0.01	0	μm
SRV2.6c	(purposely blank)								



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7.6.6 SRAM Device Dimension Check Rules

SRAM device gate definition:

Bit cell mark layer: DNSRAM (SP299), LRSRAM (SP374), D2SRAM (DP589) or RFSRAM (DP741)

PD: Inside bit cell mark layer gate, outside NW and outside SDOP. Pull down device.

PG: Inside bit cell mark layer gate, outside NW and inside SDOP. Pass gate device.

PU: Inside bit cell mark layer gate, inside NW. Pull up device.

RULE NO.	Description	Operation	Design Value	Unit
SRDevice.1	All Gates inside INST must be inside DNSRAM (SP299), LRSRAM (SP374), D2SRAM (DP589) or RFSRAM (DP741).			
SRDEV.SP299.PD.W	SP299 PD Real Gate channel width	=	0.142	μm
SRDEV.SP299.PD.L	SP299 PD Real Gate channel length	=	0.055	μm
SRDEV.SP299.PG.W	SP299 PG Real Gate channel width	=	0.11	μm
SRDEV.SP299.PGL	SP299 PG Real Gate channel length	=	0.059	μm
SRDEV.SP299.PU.W	SP299 PU Real Gate channel width	=	0.06	μm
SRDEV.SP299.PUL	SP299 PU Real Gate channel length	=	0.055	μm
SRDEV.SP374.PD.W	SP374 PD Real Gate channel width	=	0.233	μm
SRDEV.SP374.PD.L	SP374 PD Real Gate channel length	=	0.055	μm
SRDEV.SP374.PG.W	SP374 PG Real Gate channel width	=	0.183	μm
SRDEV.SP374.PGL	SP374 PG Real Gate channel length	=	0.063	μm
SRDEV.SP374.PU.W	SP374 PU Real Gate channel width	=	0.07	μm
SRDEV.SP374.PUL	SP374 PU Real Gate channel length	=	0.055	μm
SRDEV.DP589.PD.W	DP589 PD Real Gate channel width	=	0.305	μm
SRDEV.DP589.PD.L	DP589 PD Real Gate channel length	=	0.055	μm
SRDEV.DP589.PG.W	DP589 PG Real Gate channel width	=	0.154	μm
SRDEV.DP589.PGL	DP589 PG Real Gate channel length	=	0.067	μm
SRDEV.DP589.PU.W	DP589 PU Real Gate channel width	=	0.06	μm

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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:1

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SRDEV.DP589.PU.L	DP589 PU Real Gate channel length	=	0.055	µm
SRDEV.DP741.PD.W	DP741 PD Real Gate channel width	=	0.438	µm
SRDEV.DP741.PD.L	DP741 PD Real Gate channel length	=	0.055	µm
SRDEV.DP741.PG.W	DP741 PG Real Gate channel width	=	0.168	µm
SRDEV.DP741.PGL	DP741 PG Real Gate channel length	=	0.063	µm
SRDEV.DP741.PU.W	DP741 PU Real Gate channel width	=	0.08	µm
SRDEV.DP741.PU.L	DP741 PU Real Gate channel length	=	0.055	µm

Note: The gate considered in this section is gate inside (INST size by -1.5um).



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7.6.7 SRAM Marker Layer Check Rules

RULE NO.	Description	Base Rule	Check Rule
SRMarker.1^[NC]	<p>It is strongly recommended to adopt SMIC standard SRAM mini array, including pickup straps, edge dummy cells. Please contact SMIC customer engineer or sales personnel about adding dummy layout, pickup strap.</p> <p>Please download SMIC standard 0.299um², 0.374um², 0.589um² and 0.741um² layout samples through SMIC NOW.</p>	NA	
SRMarker.2^[NC]	<p>If customer plans to adopt their own cell design, customer must provide customer's SRAM cell layout to SMIC customer engineer or sales personnel for risk assessment before any tape-out.</p> <p>For customer's product tape-out with their own SRAM layout design, need Si verification for speed, function, leakage, Vccmin, and process window check.</p> <p>For Customer's own SRAM cell layout, customer shall contact SMIC customer engineer or sales personnel to define the related SRAM mark layers. Please do not assume it will be same as SMIC's existing SRAM mark layers.</p>	NA	
SRMarker.3^[NC]	<p>If Customers want to design their own cell and to use logic SPICE model to simulate chip performance, please strictly follow SMIC logic design rules. Please contact SMIC customer engineer or sales personnel for risk assessment.</p> <p>SMIC logic or SRAM SPICE model does not support bit cell not provided by SMIC. Customers have to qualify the bit cell if the bit cell is prepared by themselves. Please contact SMIC customer engineer or sales personnel for qualification methodology.</p>	NA	
SRMarker.4	Marker layer DNSRAM, LRSRAM, D2SRAM, RFSRAM must be within SRAM marker INST.	NA	
SRMarker.5	For high performance SRAM bit cell (LRSRAM (SP374), RFSRAM (DP741)), there must be high performance marker layer HPBL overlapped.	NA	
SRMarker.6	No hole or slot is permitted in one SRAM marker layer (DNSRAM, LRSRAM, D2SRAM, RFSRAM, INST).	NA	
SRMarker.7^[NC]	SRAM bit cell pass gate transistor must be covered by SDOP marker layer.	NA	
SRMarker.8	DNSRAM, LRSRAM, D2SRAM, RFSRAM should not overlap with each other(touch is permitted)	NA	
SRMarker.9	No Overlap of (DNSRAM (SP299) or D2SRAM (DP589)) with HPBL is permitted.	NA	

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7.7 Design guidelines

The rules with the superscript of [G] are layout guidelines which require performing a DRC runset, but DRC check is not gated for them. It's strongly recommended customers to follow layout guidelines which purpose is to ensure better performance for process. Customers can waive violations based on their own judgment, and please consult with integration engineers if customers feel the need.

It is strongly recommended to adopt the qualified IP at SMIC for inductor, MOM, varactor and BJT. If customer plans to adopt their own cell design, customer must provide customer's IP layout to SMIC customer engineer or sales personnel for risk assessment before any tape-out. For customer's product tape-out with their own layout design, silicon verification data and process window check data is needed.

SMIC spice model and PDK is based on SMIC design rule guidelines. And SMIC don't provide spice model and PDK if customers don't follow the layout guidelines.

7.7.1 Re-tool check

This section provides guidelines to judge which mask or masks need to re-tool in case of GDS modification.

To judge which mask or masks need to re-tool, following sequences may be referenced:

Case I: Mask re-tool due to directly related GDS layer modification

User may check table 7.3.1-4 for directly related GDS and mask layers. From the table, the modified GDS will impact the directly related masks. The directly related masks must re-tool.

Case II: Mask re-tool due to indirectly related GDS layer modification which may impact the dummy pattern of other masks

Designers may check table 7.7.1-1 for masks which can be impacted due to GDS modification through dummy pattern interaction. The usage of the table 7.7.1-1 is described in the notes under the table.

Table 7.7.1-1 GDS and Mask relationship through dummy pattern interaction

Related Mask ->	AA	GT	Mn	TMn	Vn	ALPA
Related Dummy Layer ->	AADUM	GTDUM	MnDUM, MnDOP	TMnDUM	VnDUM	ALDUM
Modified GDS Layer	AA	1	2	3	3	3
	GT	2	1	3	3	3
	Mn	3	3	1	3	3
	TMn	3	3	3	1	3
	Vn	3	3	2	3	1
	ALPA	3	3	3	3	1
	AADUM	1	2	3	3	3
	GTDUM	2	1	3	3	3
	MnDOP, MnDUM	3	3	1	3	3
	TMnDUM	3	3	3	1	3

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Related Mask ->	AA	GT	Mn	TMn	Vn	ALPA
Related Dummy Layer ->	AADUM	GTDUM	MnDUM, MnDOP	TMnDUM	VnDUM	ALDUM
DUMBA	2	3	3	3	3	3
DUMBP	3	2	3	3	3	3
DUMBM	3	3	2	2	2	2
MnDUB(n=1-8)	3	3	2	3	2	3
TMnDUB(n=1-2)	3	3	3	2	3	3
VnDUB(n=1-7)	3	3	2	3	2	3
INDMY	2	2	2	2	2	2
RESNW	2	2	3	3	3	3
PLRES	2	3	3	3	3	3
HRPDMY	2	3	3	3	3	3
RESP1	2	3	3	3	3	3
EFUSE	2	2	3	3	3	3
MARKS	2	2	2	2	2	2
RESAA	3	2	3	3	3	3
DIFRES	3	2	3	3	3	3
MOMDMY	3	3	2	2	2	3
LDBK	3	3	3	3	3	3
INST	3	3	3	3	3	3
DSTR	3	3	3	3	3	3
BIPOLA	3	3	3	3	3	3
VARMOS	3	3	3	3	3	3
VARJUN	3	3	3	3	3	3
GTFUSE	3	3	3	3	3	3

Note:

a) Meaning of the numbers in the table

The numbers stands for impact grade

1: Must re-tool

2: Evaluate. Run DRC to check, follow corresponding flow chart 7.7.1-2 in NEXT SECTION

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- 3: No need of re-tooling
b) Mn:n = 1-8; Vn: n= 1-7; TMn: n = 1, 2; MnDUM: n=1-8; MnDOP:n=1-8; TMnDUM: n=1,2;
c) When Mn/MnDUB/MnDOP/MnDUM GDS is modified, it is needed to check column 'Mn' for Mn with same n value, and check column 'Vn' for Vn and Vn-1 with same n value.
For example:

- 1) When M3 GDS layer is modified, please check column 'Mn' for M3 mask, and check column 'Vn' for V2 and V3 masks.
- 2) When TMn/TMnDUB/TMnDUM GDS is modified, it is needed to check column 'TMn' for TMn with same n value. For example 1) When TM2 GDS layer is modified, pls check column 'TMn' for TM2 mask.



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Chart 7.7.1-2 40LL dummy re-tooling check procedures

Check operation Notes:

1. The DRC should include DUMC.x and DUMCN.x both sections.

1. AA mask revision decision flow due to AADUM

1.1	AADUM level 2 revision layers revised (GT,NW,DUMBA,INDMY,GTDUM,RESP1,RESNW,PLRES,HRPDMY,EFUSE,MARKS)
1.2	Design rule check (e.g GT to AADUM space rule)
1.2.1	No violation ==> AA mask no need of revision. Go 1.4
1.2.2	Exist DRC violation (e.g GT to AADUM space rule). Go 1.3
1.3	must revise AA mask(e.g. AA impacted)
1.4	Complete decision

2. GT mask revision decision flow due to GTDUM

2.1	GTDUM level 2 revision layers revised(AA, DUMB, INDMY, AADUM, RESAA,DIFRES, RESNW, EFUSE, MARKS)
2.2	Design rule check (e.g AA to GTDUM space rule)
2.2.1	No violation ==> GT mask no need of revision. Go 2.4
2.2.2	Exist DRC violation (e.g AA to GTDUM space rule). Go 2.3
2.3	must revise GT mask(e.g. GT impacted)
2.4	Complete decision

3. Mn,TMn mask revision decision flow due to MnDUM,MnDOP,TMnDUM

3.1	(MnDUM (n=1-8)or TM1DUM or TM2DUM) level 2 revision, following layers revised[LOGO, DUMB, MnDUB(n=1-8),TMnDUB(n=1-2),VnDUB(n=1-7),INDMY, MOMDMY, MARKS]
3.2	Design rule check (e.g DUMB to M2DUM space rule)
3.2.1	No violation ==> (Mn or TMn) mask no need of revision. Go 3.4
3.2.2	Exist DRC violation(e.g DUMB to M2DUM space rule). Go 3.3
3.3	must revise (Mn or TMn) mask (e.g. M2 impacted)
3.4	Complete decision

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7.7.2 Inline process control cells

7.7.2.1 OCCD On chip CD monitor cell guidelines

The purpose of OCCD (within chip CD, layer OCCD(91;4)) structure is to enable the GT or AA's CD uniformity measurement and control within a big chip. This section describes the guideline of OCCD structure placement.

Rules number	Description	Operation	Design Value	Unit
OCCD.1 ^[INC]	OCCD structures are to be placed in floor plan arrange stage or by dummy insertion utility to achieve suggested distribution	≥	0.330	μm
OCCD.2 ^[INC]	Insert one OCCD structure in each 2x2 mm ² window.(OCCD window hereafter) No insert of OCCD if window size smaller than 1mm x 1mm.			
OCCD.3 ^[INC]	OCCD window percentage: window 2mm x 2mm is one unit. 50% window units with OCCD structure. Recommend 70% window units with OCCD structure.			
OCCD.4 ^[INC]	Space between OCCD structures	≥	150	μm
OCCD.5 ^[INC]	Other structures outside of OCCD space to OCCD Other structures means: AA, GT, SN, SP, LOGO, seal ring(MARKS), guard ring(MARKG), DUMBA, DUMB OCCD should not straddle on NW	≥	2	μm
OCCD.6 ^[INC]	OCCD(91;4) must cover OCCD cell structures.			

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7.7.2.2 OCOVL On chip overlay monitor cell guidelines

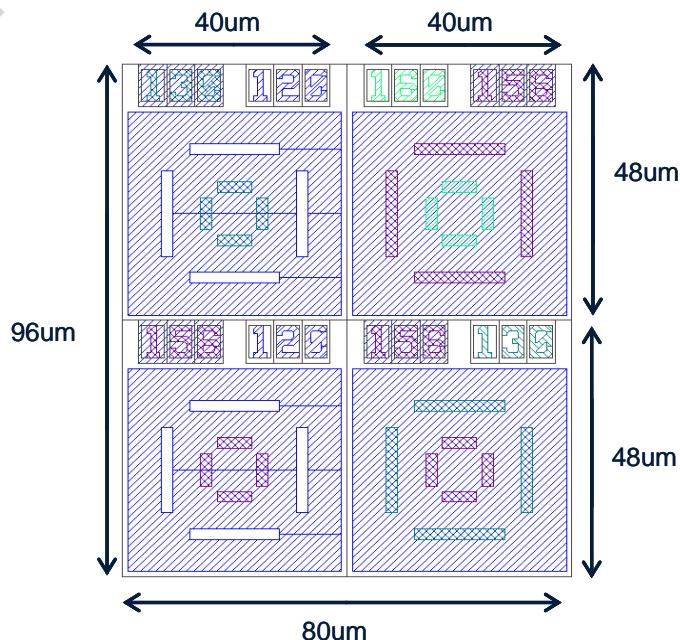
The purpose of OCOVL (within chip overlay, layer OCOVL(91;5)) is to enable the overlay measurement and control within a big chip. It will rationalize the overlay target distribution in field and enable high order correction modeling.

Rule number	Description	Operation	Design Value	Unit
OCOVL.1^[NC]	OCOVL structures are to be placed in floor plan arrange stage or by dummy insertion utility to achieve suggested distribution			
OCOVL.2^[NC]	Insert one OCOVL structure in each 4x4 mm ² window.(OCOVL window hereafter). No insert of OCOVL if window size smaller than 4x4mm ²			
OCOVL.3^[NC]	Space between OCOVL blocks(see note.1)	≥	1000	μm
OCOVL.4^[NC]	Other structures outside of OCOVL minimum space to OCOVL Other structures means: AA, GT, SN, SP, CT, M1, LOGO, seal ring (MARKS), guard ring (MARKG), DUMBA, DUMBP, DUMB OCOVL should not straddle on NW	≥	2	μm
OCOVL.5	OCOVL(91;5) must cover OCOVL cell structures. Following rules can be waived inside OCOVL: GT.21, GT.22, SAB.3, SAB.7, SAB.8, CT.1a, CT.12			

Note:

1. The OCOVL cell set contains 4 overlay structures; The 4 overlay marks are: GT_AA; CT_AA; CT_GT; M1_CT.

Fig. 7.7.2.2-1 OCOVL cell sample figure (SMIC provided OCOVL sample GDS may vary according to process monitor requirement.)





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7.7.3 Redundant Via insertion guide

For better yield and reliability, it is strongly recommended to utilize SMIC offered qualified Redundant via Auto Insertion utilities to do redundant via insertion wherever the layout and design rules permit.

For Digital design, it is recommended to do redundant via insertion at place and routing stage with the PR tech file provided by SMIC, the tech file Doc No. are DS-LO40-PR-2001(for Encounter) and DS-LO40-PR-2002(for IC Compiler). Designers can contact DS team if have questions.

For Analog design, it is recommended to do redundant via insertion using SMIC provided tech file (tech file Doc No: TD-LO40-DT-2007), and then please designers check and ensure LVS passed. The information as followed lists the solution of analog design auto redundant via insertion.

Features of this utility:

1. The utility strictly follows design rules for these layers Mn, Vn, TMn, and TVn.
2. The new generated redundant vias will be marked by VnRM (n=1-7), TVnRM (n=1-2)
3. For putting redundant vias as required by design rules, metal lines can be extended. Therefore, designers should ensure timing result&LVS passed after using redundant via utilities.
4. Designers can choose just clean redundant via DRC error or do via layout yield enhancement by switch.
5. There is a configuration for the counts of inserted redundant via, which default value is 1, for reliability and yield enhanced.

The following layers will prevent the utility from redundant via insertion:

1. VnRB (n=1 – 7), TVnRB (n= 1, 2) are the block layers for redundant via auto insertion. User can draw these layers where the DFM Via layout enhancement is not desired, especially for timing or resistance sensitive circuit area.

INDMY(212;0), LOGO(26;0), MARKS/MARKG(189;151/189;0), MOMDMY(211;1), MnR(n=1 – 8), TMnR (n=1, 2), DUMBMB(90;0), MnDUB (n=1 – 8), TMnDUB (n= 1, 2), INST(60;0, only follow main rule V1.16/V1.17/Vn.16/Vn.17 to insert) are also redundant via block layers.

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7.7.4 BEOL dummy metal & dummy Via insertion method selection guideline

This is to guide designers about how to select dummy metal & dummy via ((M1DUM~M8DUM, TM1DUM, TM2DUM, MTT2DM, ALDUM, V1DUM~V7DUM) insertion method in the utility provided by SMIC. SMIC dummy metal & dummy via insertion utility now supports both model based and rule based insertion design manual.

It's strongly recommended designers to use SMIC model based dummy metal & dummy via insertion utility to do dummy insertion which has better performance to comply with density rules. Application notice please refer dummy insertion utility; designers can download these utilities from SMIC NOW.

If designers still found DRC violations after use SMIC-provided dummy metal & dummy via insertion utilities, SMIC will review the results and take proactive steps to close the DRC violation issues. If you use non-SMIC-provided dummy fill scripts, you must ensure DRC clean. Please designers ensure timing closure post dummy insertion.

Features of these utilities:

1. Minimum space of metal dummy to active pattern is 0.6um for M1~M8, TM1, TM2, and the minimum space for MTT2 dummy to active pattern is 1.778um for both model-based dummy and rule-based dummy utilities.
2. Other features please refer to 40nm_ll_calibre_BEOL_model_based_dummy_fill_script_release_note.pdf

Following layers will prevent the dummy metal & dummy via insertion for both model-based dummy and rule-based dummy utilities:

1. INDMY(212;0), LOGO(26;0), MARKS/MARKG(189;151/189;0), DUMB(90;0), PTCT(159;7) will prevent dummy insertion for these layers: M1~M8, TM1, TM2, MTT2, ALPA, V1~V7
2. M1DUB (151;1), M2DUB (152;1), M3DUB (153;1), M4DUB (154;1), M5DUB (155;1), M6DUB (156;1), M7DUB (157;1), M8DUB (158;1), TM1DUB (193;1), TM2DUB (194;1), MTT2DB (194;2), ALDUB (83;6), V1DUB (70;6), V2DUB (71;6), V3DUB (72;6), V4DUB (73;6), V5DUB (74;6), V6DUB (75;6), V7DUB (76;6) will prevent dummy insertion for its specific dummy metal & dummy via: for example M1DUB prevents only M1 dummy insertion.
3. GTFUSE (81;1) will prevent only M1, M2 dummy insertion.

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7.7.5 ESD layout guideline

The ESD guidelines are targeted to meet HBM-2KV(Human Body Mode) and MM-200V (Machine mode) spec according to EIA/JEDEC standard and EIA/JESD22 test standard, SMIC does not guarantee the final ESD device performance. If designers do not follow SMIC ESD guideline, chip level ESD test should be done for ESD verification.

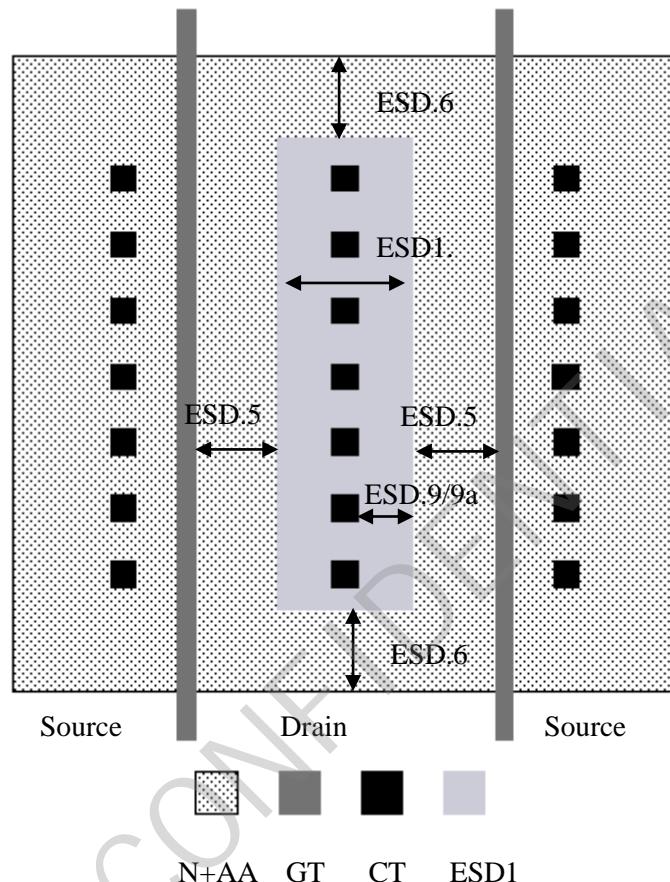
7.7.5.1 ESD1 implant drawing rules

ESD1 implant layer is an optional layer to define ESD implant location for N type ESD device to improve ESD performance.

We suggest ESD1 to be drawn at drain side of the ESD NMOS by following the drawing rules.

Rules number	DESCRIPTION	Operation	Design Value	Unit
ESD.1	ESD1 width	≥	0.33	μm
ESD.2	Space between two ESD1 implant regions. Merge if the space is less than this value.	≥	0.33	μm
ESD.3	ESD1 area	≥	0.7	μm ²
ESD.4	Enclosed area of ESD1	≥	0.7	μm ²
ESD.5	Space between an ESD1 implant to an N-channel Real Gate , ESD1 cannot touch gate.	≥	0.2	μm
ESD.6	ESD1 must be enclosed by AA at least	≥	0.2	μm
ESD.7	ESD1 implant region is not allowed to overlap with SP			
ESD.8 ^[NC]	ESD1 must be a drawn layer if there is need of ESD implant. ESD1 should be drawn directly the location to have ESD implant.			
ESD.9	CT enclosure by ESD1	≥	0.2	um
ESD.9a ^[R]	Recommended CT enclosure by ESD1	≥	0.4	um

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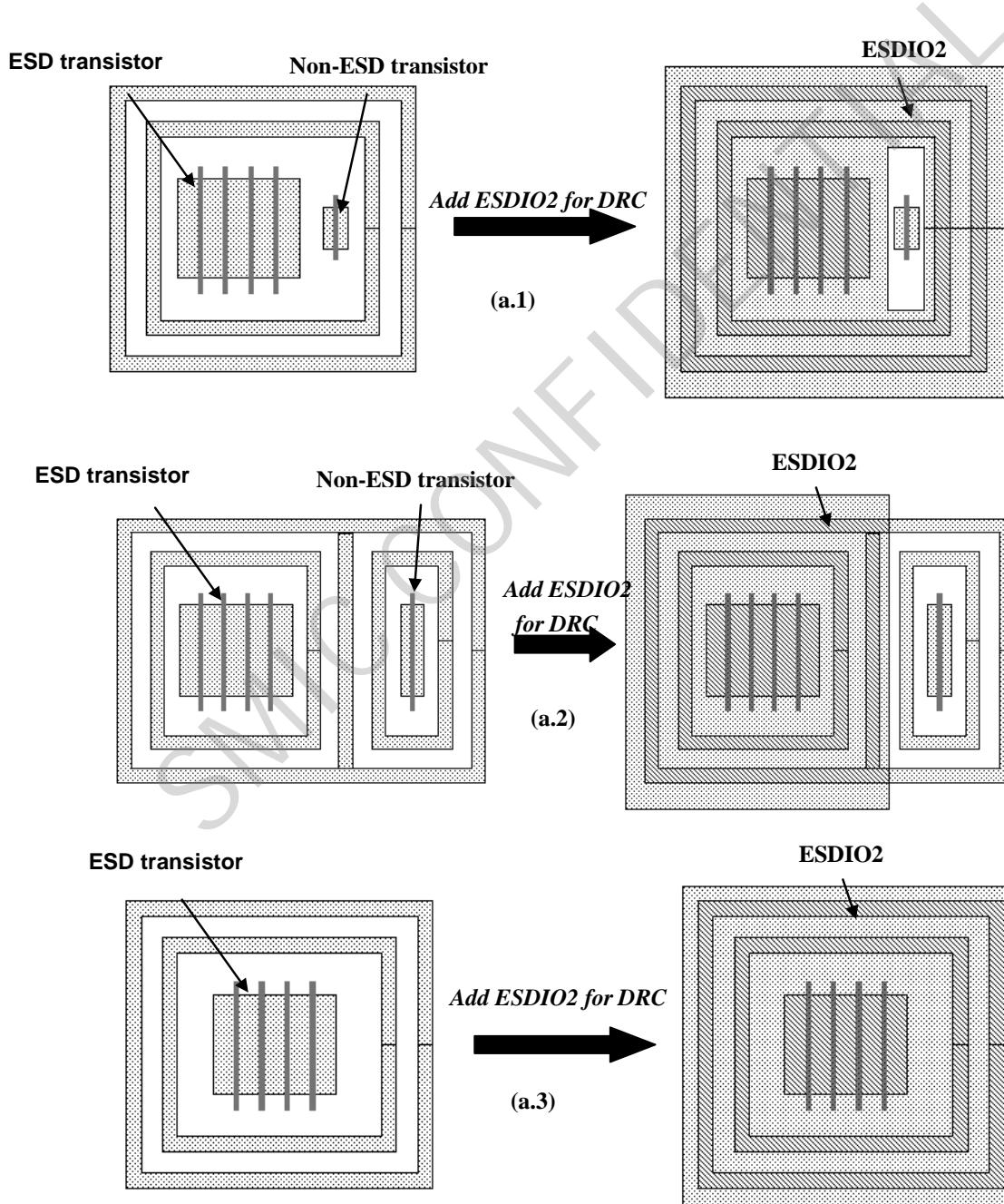


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7.7.5.2 ESDIO2 (DRC marker layer for ESD component)

ESDIO2 (GDS No.:133;3) is DRC marking layer for I/O ESD protection devices and circuits identification. This layer should cover ESD transistors (**except secondary ESD protection devices**) and its N and P guard rings, but non-ESD transistor inside the same guard ring should be excluded. Otherwise, all the devices and circuits inside ESDIO2 will be regarded as ESD transistors and may induce false DRC alarms. ESDIO2 should be drawn at each individual ESD protection device.

ESDHV (GDS: 133;1) is DRC marking layer for HV tolerant ESD protection devices using cascoded NMOS. Please refer to the examples in Fig. 7.7.5.1-1.



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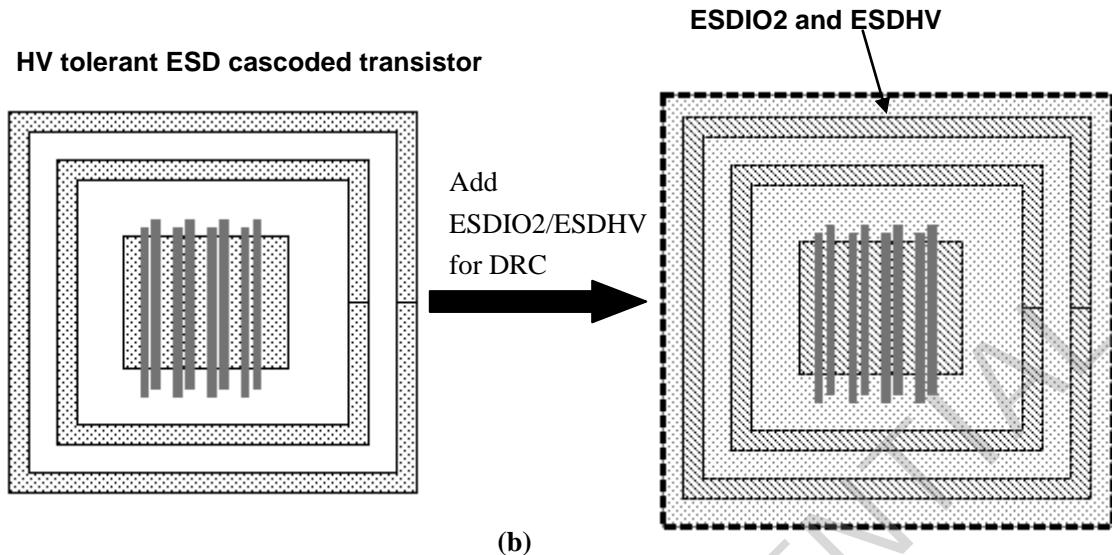


Fig.1 Examples of ESDIO2/ESDHV for ESD DRC

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7.7.5.3 ESD design and layout guideline

The guideline provided layout structure and dimension for N/P MOS ESD protection device design. SAB on drain side is essential for ESD protection devices.

Items	DESCRIPTION	Operation	Design Value	Unit
ESDLO.1^[NC]	Finger-type structure with uniform finger width is suggested for N/P MOS ESD protection design			
ESDLO.2^[G]	Unit finger width (F) of NMOS and PMOS for ESD protection device(Fig. 7.7.5.3-1)	≥	10	μm
		≤	60	μm
ESDLO.3^[G]	ESDLO.3a ^[G] and ESDLO.3b ^[G] are defined for total channel width of ESD N/PMOS. The total channel width is calculated by the ESD MOS in the same Drain connection. SAB in ESDIO2 region is used for drain recognition in DRC runset. The connectivity (not limited in ESDIO2 region) can be formed by all metal, via, ALPA, PA and MD and not broken by resistors.			
ESDLO.3a^[G]	Channel width (W) of NMOS for ESD protection device (Channel width=Finger width x Finger No.)	≥	300	μm
ESDLO.3b^[G]	Channel width (W) of PMOS for ESD protection device (Channel width=Finger width x Finger No.)	≥	450	μm
ESDLO.4a^[G]	Channel length of 2.5V I/O N/PMOS for protection device	≥	0.27	μm
ESDLO.4b^[G]	Channel length of 2.5V I/O overdrive 3.3V NMOS for protection device	≥	0.55	μm
	Channel length of 2.5V I/O overdrive 3.3V PMOS for protection device	≥	0.44	μm
ESDLO.4c^[G]	Channel length of 2.5V I/O underdrive 1.8 N/PMOS for protection device	≥	0.24	μm
ESDLO.4d^[G]	Channel length of 1.8V I/O N/PMOS for protection device	≥	0.2	μm
ESDLO.4e^[G]	Channel length of 1.1V N/PMOS for protection device	≥	0.07	μm
ESDLO.5^[G]	Space from poly edge to CT edge on source side (SCP) for NMOS and PMOS (Fig. 7.7.5.3-3 and Fig. 7.7.5.3-5).	≥	0.20	μm
ESDLO.6^[G]	(Purposely blank)			
ESDLO.7^[G]	SAB should block on drain side of NMOS and PMOS (contact region should be kept silicided.) SAB drawn on source side is not necessary.			

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Items	DESCRIPTION	Operat ion	Design Value	Unit
ESDLO.8a^[G]	Width of SAB on the drain side (A) for NMOS, note: A does not include the overlap of SAB area and GT (Fig. 7.7.5.3-3 and Fig. 7.7.5.3-5).	≥	1.0	μm
ESDLO.8b^[G]	Width of SAB on the drain side (A) for PMOS, note: A does not include the overlap of SAB area and GT(Fig. 4 and Fig.6)	≥	0.6	um
ESDLO.9^[G]	ESD protection devices should be surrounded by guard ring, this guard ring also can be designed as the pickup of the ESD device. (Fig. 7.7.5.3-1)			
ESDLO.10^[NC]	The NMOS/PMOS should be added after the input resistor R as the secondary ESD protection for better ESD immunity if there is no conflict with circuit operation.			
ESDLO.11^[NC]	value of input resister R. (Fig. 7.7.5.3-2)	≥	200	Ω
ESDLO.13^[NC]	The suggested channel width for secondary ESD protection device	=	20	μm
ESDLO.13b^[NC]	The suggested channel length of 2.5V I/O N/PMOS for secondary protection device	=	0.27	μm
ESDLO.13c^[NC]	The suggested channel length of 1.8V I/O N/PMOS for secondary protection device	=	0.2	μm
ESDLO.13d^[NC]	The suggested channel length of 1.1V N/PMOS for secondary protection device	=	0.07	μm
ESDLO.14a^[G]	The overlap (Sd) of SAB and poly for 1.8V/2.5V I/O ESD N/PMOS (Fig. 7.7.5.3-3)	≥	0.05	μm
ESDLO.14b^[G]	The overlap (Sd) of the SAB and poly for 1.1V I/O ESD N/PMOS	≥	0.02	μm
ESDLO.15^[G]	For high voltage tolerant I/O using Cascoded 1.8V/2.5V NMOS, (ESDIO2 AND ESDHV) must overlap with ESD1. (refer to Fig. 7.7.5.3-4 &5)			
ESDLO.16^[G]	The space (S) between active poly gate and inactive poly gate of Cascoded NMOS should be (Fig. 7.7.5.3-5)	≤	0.3	μm
ESDLO.17^[G]	For high voltage tolerant I/O designed by 1.8V/2.5V NMOS, SAB should cover all top poly gates and extend to overlap the second poly gate by (Fig. 7.7.5.3-5)	≥	0.05	μm
ESDLO.18^[NC]	Contacts should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of contact drawn on rule is	≥	550	count



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Items	DESCRIPTION	Operat ion	Design Value	Unit
ESDLO.19^[NC]	Vias should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of via drawn on rule is	≥	500	count
ESDLO.20a^[NC]	Total width (W2) of each individual inter metal(M1~M8) lines of the nearest current path between ESD devices and bonding pad	≥	20	μm
ESDLO.20b^[NC]	Total width (W2) of each individual top metal(TM1,TM2) line of the nearest current path between ESD devices and bonding pad	≥	3	μm
ESDLO.21^[NC]	In Chip level ESD guideline, the poly gate of N/PMOS of internal and I/O circuit is not allowed to connect to power/ground or input/output pad directly. Please refer to ESDLO.21a, ESDLO.21b, ESDLO.21c rules below.			
ESDLO.21a^[NC]	Secondary ESD protection or tie-high/tie-low cell is strongly recommended to insert between poly gate and power/ground pad or input/out pad.			
ESDLO.21b^[NC]	N/PMOS used for capacitor is not recommended to connect power/ground or input/output pad directly.			
ESDLO.21c^[NC]	Poly resistor and ESD protection N/PMOS (including primary and secondary ESD protection) can be exempt for this rule.			

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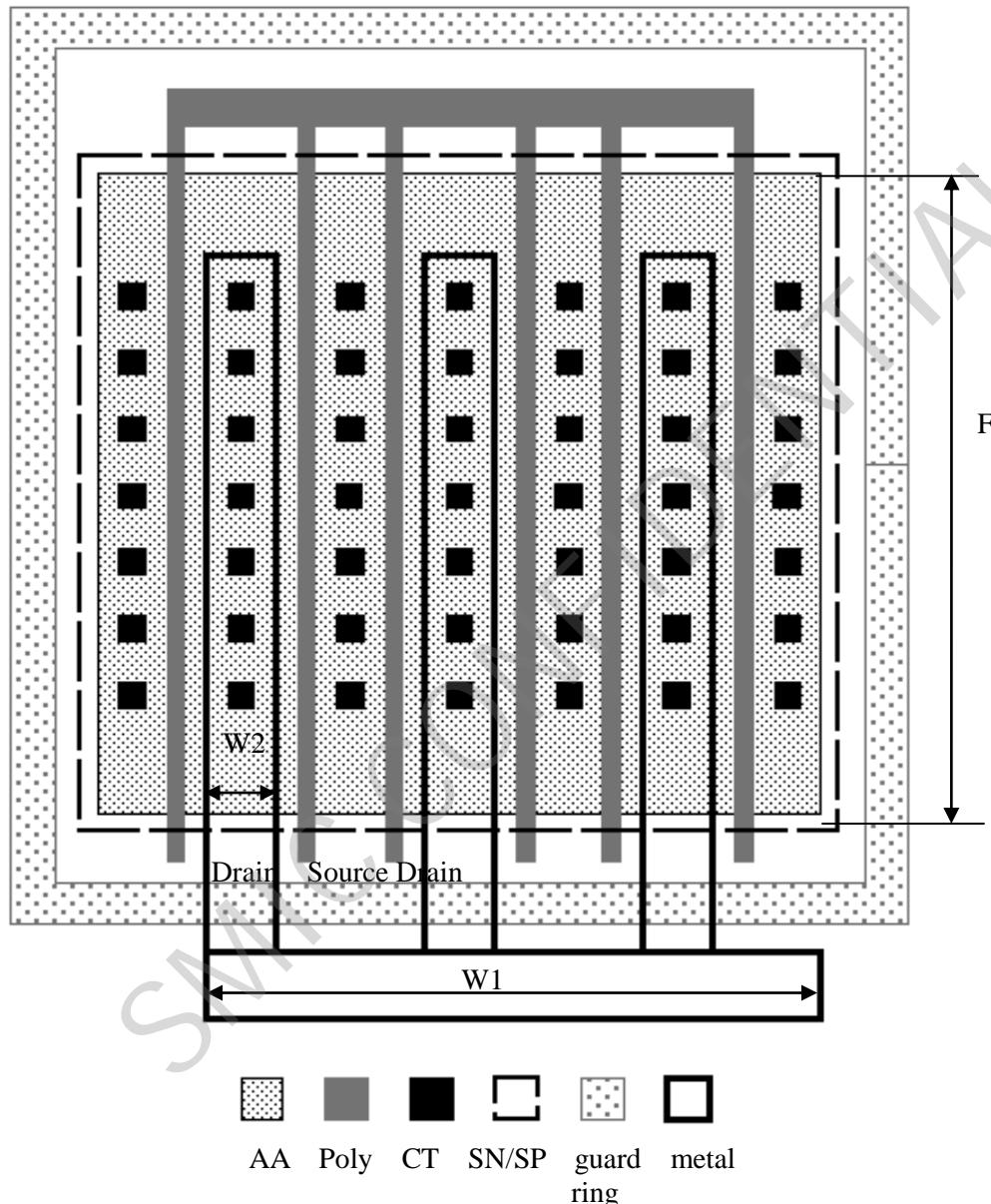


Fig. 7.7.5.3-1 ESD Cell Layout Example

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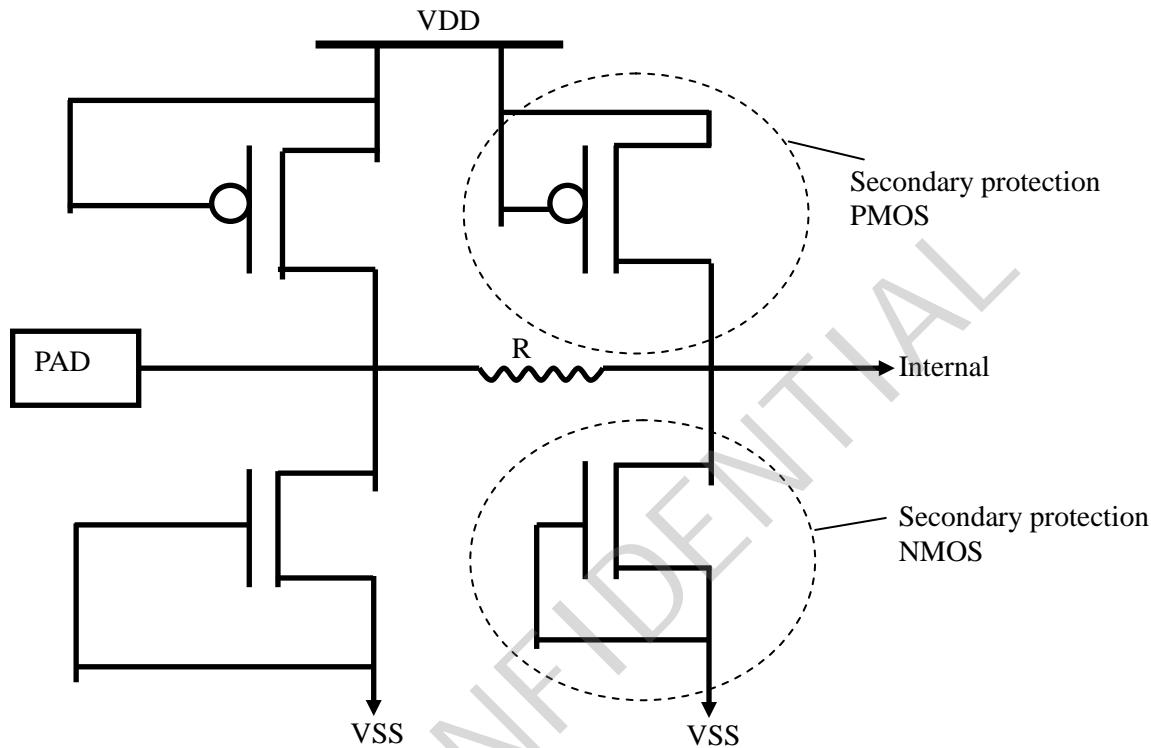
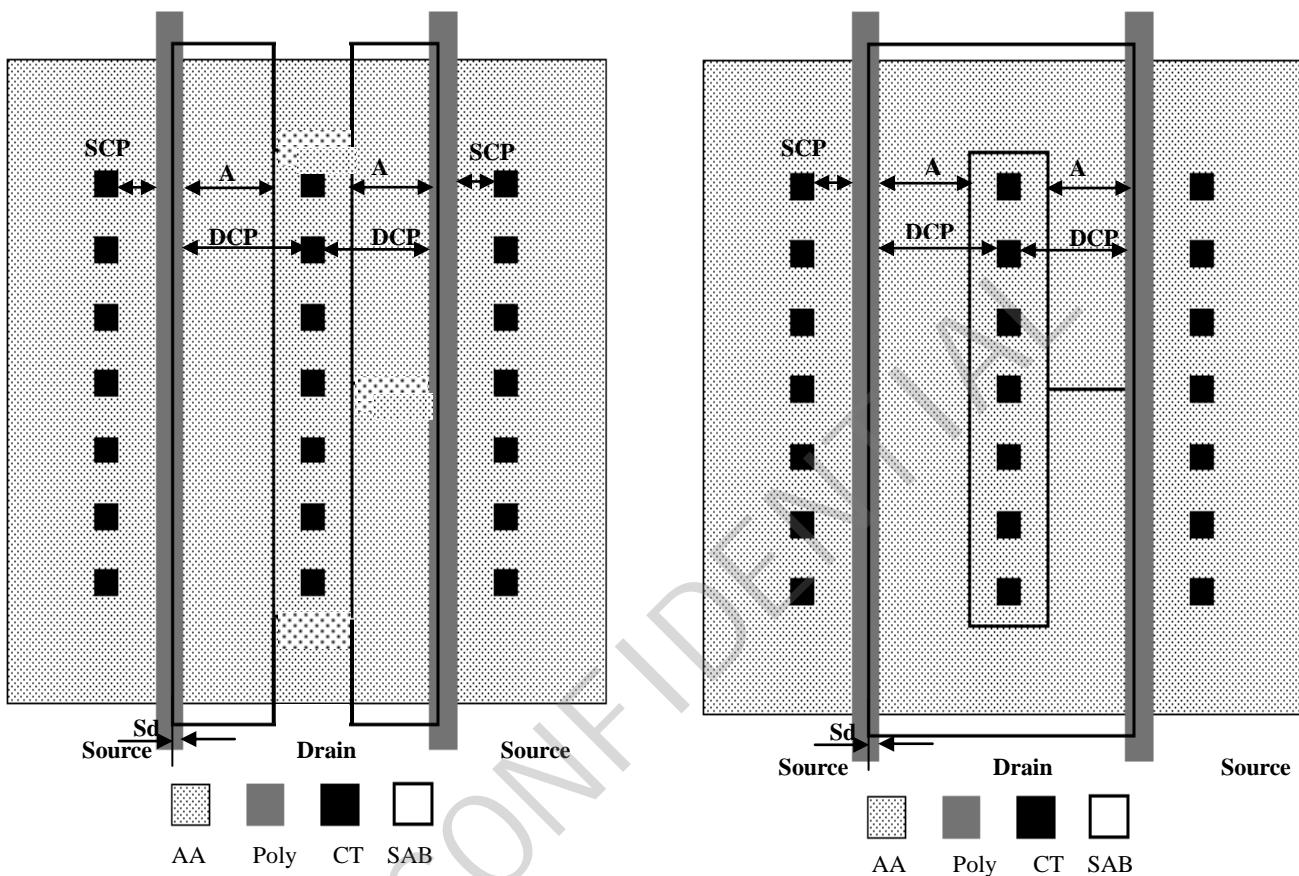


Fig. 7.7.5.3-2 ESD Protection Scheme

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7.7.5.3-3 NMOS/PMOS I/O for ESD Protection with two layout styles of SAB

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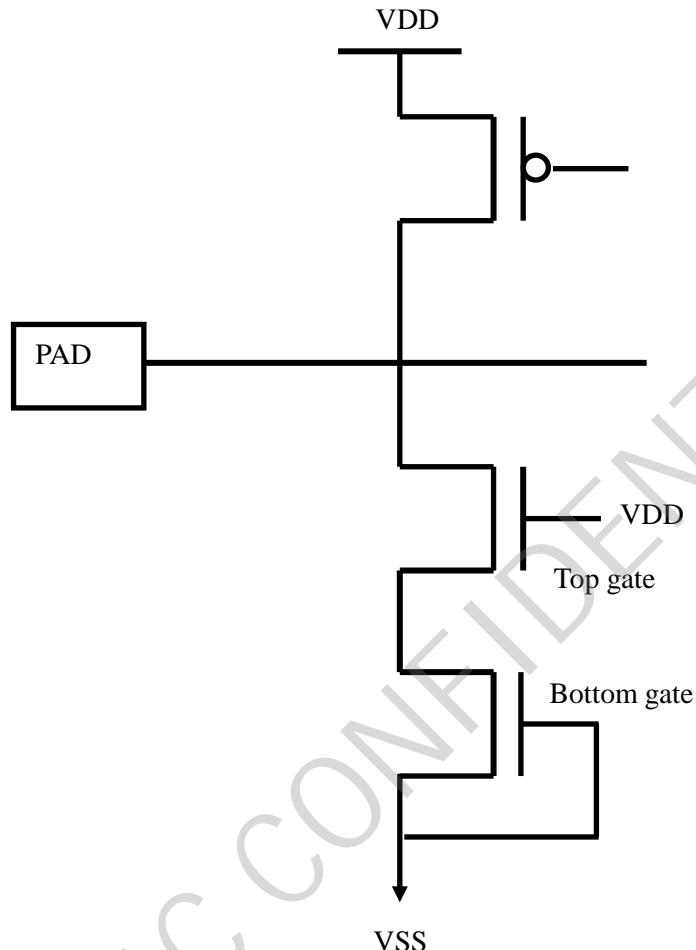


Fig. 7.7.5.3-4 HV Tolerant 2.5/3.3V I/O ESD protection using cascaded NMOS

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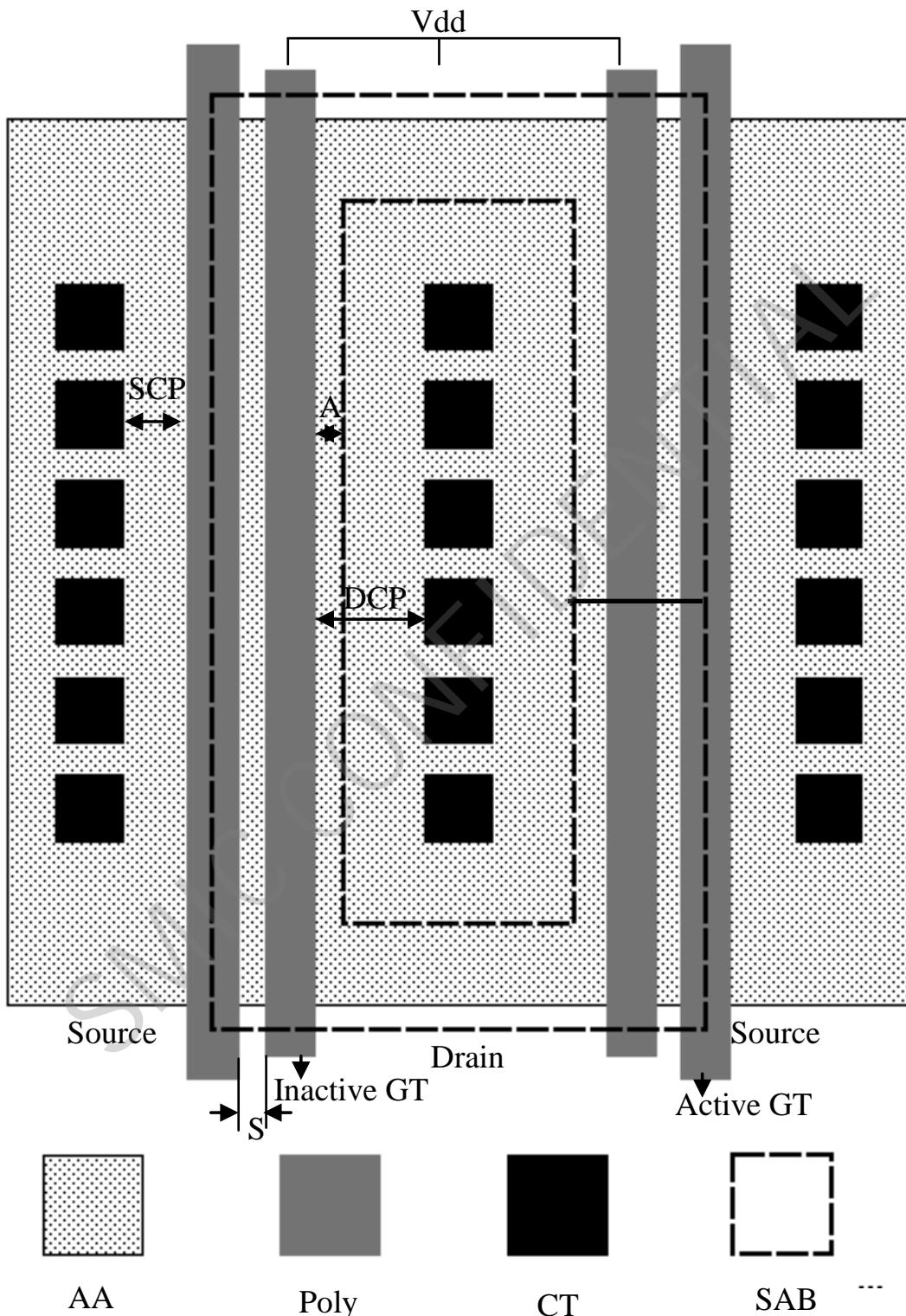


Fig. 7.7.5.3-5 Cascoded NMOS for HV Tolerant I/O (two layout styles of SAB as 7.7.5.3-3 is allowed)

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7.7.6 Latch Up Prevention Layout Guidelines

Rules Number	DESCRIPTION	Operation	Layout Value	Unit
LU.1^[G]	A double guard ring structure* should be used to surround the NMOS and PMOS for I/O buffers and ESD devices.			
LU.2^[G]	Minimum guard-ring width	\geq	0.12	μm
LU.3^[G]	LU.3a-LU.3d define minimum space (S1) between NMOS and PMOS connected to I/O pad (Fig. 7.7.6-1)			
LU.3a^[G]	For core N/PMOS connected to an I/O pad Spacing between NMOS and PMOS	\geq	2	μm
LU.3b^[G]	For 1.8V N/PMOS connected to an I/O pad Spacing between 1.8V NMOS and 1.8V/Core PMOS and Spacing between 1.8V PMOS and 1.8V/Core NMOS	\geq	2.3	μm
LU.3c^[G]	For 2.5V N/PMOS connected to an I/O pad Spacing between 2.5V NMOS and 2.5V/Core PMOS and Spacing between 2.5V PMOS and 2.5V/Core NMOS	\geq	3.2	μm
LU.4^[G]	Maximum space (S2) from any point within the Source/Drain region to the nearest pickup AA region inside the same well for I/O and internal circuits. (Fig. 7.7.6-2) DRC doesn't check OCCD region.	\leq	35	μm
LU.5^[NC]	Minimum space (S3) between I/O circuit and internal circuit region. (Fig. 7.7.6-3)	\geq	15	μm
LU.6^[NC]	All the guard rings and pickups should be connected to VDD/VSS with low series resistance. Contacts and Via's should be used as many as possible.			

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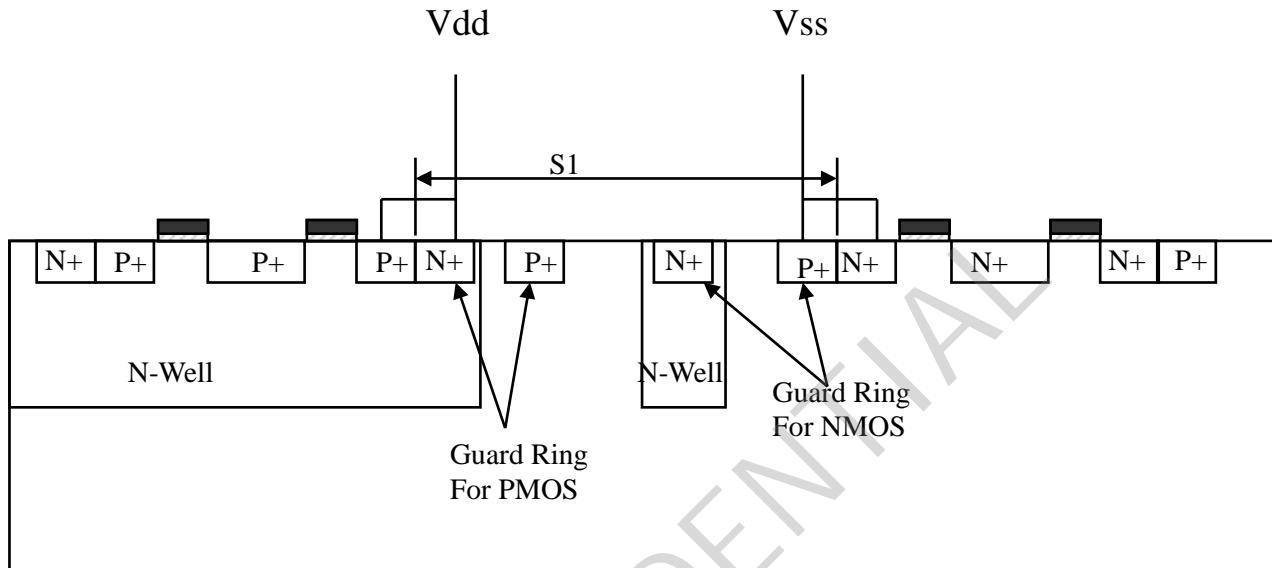


Fig. 7.7.6-1 space (S1) between NMOS and PMOS connected to I/O pad

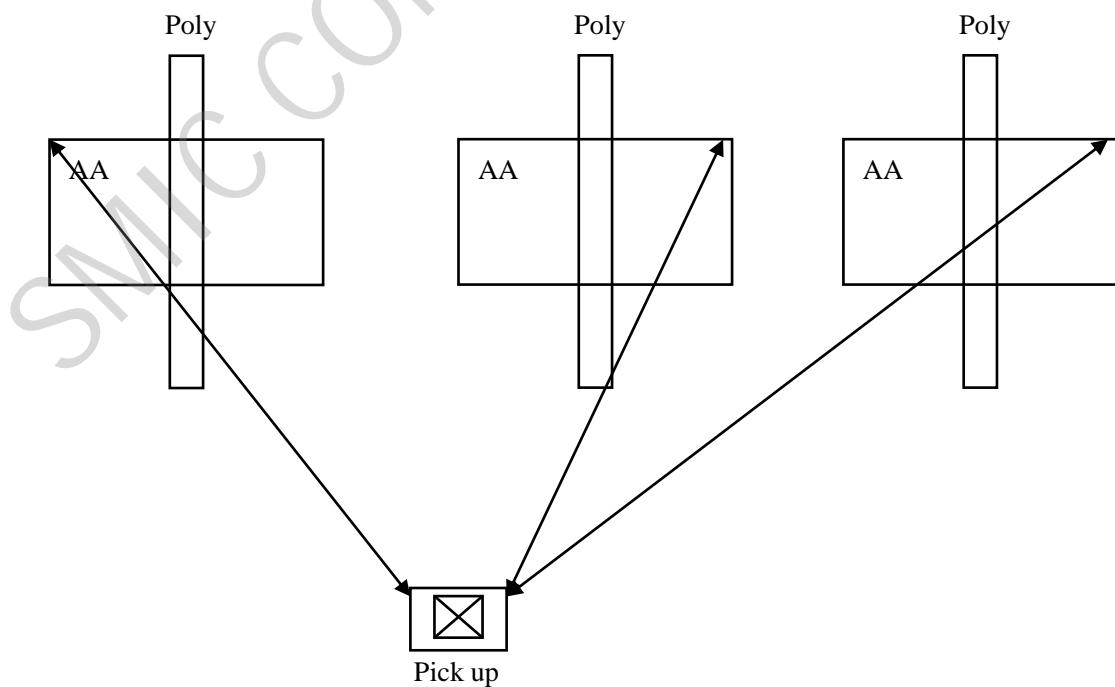


Fig. 7.7.6-2 Space (S2) between pickup AA to MOS AA

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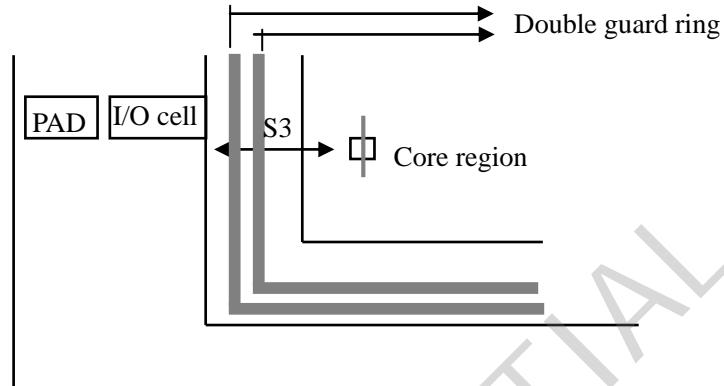


Fig. 7.7.6-3 Space (S3) I/O circuit to internal circuit

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7.7.7 LDMOS design Guideline for IO 2.5V gate OX device

LDBK layer is the mark layer to identify LDMOS area. The LDMOS described here is covered by TG and LDBK layers. It is parasitical device of 2.5V IO. The LDMOS follow 2.5V IO related design rules and the rules described below.

The drain side is for 5V operation; the gate side with 2.5V operation voltage; the source side is connected to ground.

Rule No	Description	Operation	Design value	Unit
LD.1a^[G]	Effective Channel length for NLDMOS transistors	\geq	0.28	μm
LD.1b^[G]	Effective Channel length for PLDMOS transistors	\geq	0.26	μm
LD.2^[G]	Drain AA width along source/drain direction for LDMOS transistors	\geq	0.2	μm
LD.3^[G]	STI width along source/drain direction	$=$	0.15	μm
LD.4^[G]	Overlap of GT and STI along source/drain direction	\geq	0.05	μm
LD.5^[G]	NLDMOS gate overlaps with NW in source/drain direction length. PLDMOS gate not in NW in source/drain direction length	$=$	0.22	μm
LD.6^[G]	LDMOS channel width	\geq	2	μm
LD.7a^[G]	Space between LDMOS source side AA and pickup AA along source/drain direction	\geq	0.6	μm
LD.7b^[G]	Space between LDMOS source side AA and pickup AA along gate poly direction	\geq	0.9	μm
LD.8^[G]	NW extension outside of N LDMOS AA along gate poly direction. NW space to P LDMOS AA along gate poly direction	\geq	0.25	μm
LD.9^[G]	LDBK extension outside of (gate, source, drain)'s AA	\geq	0.4	μm
LD.10^[G]	One LDMOS unit must have two polys and a common drain. Single poly structure is not allowed.			
LD.11^[G]	Common source is allowed only for one LDMOS with multi-fingers Gate structure within one LDBK region. (Drain/Source/GATE is connected together respectively.)			

Note:

1. Effective channel length(L_{eff}):

- a) NLDMOS effective channel length: GT not in NW part channel length in source/drain direction
- b) PLDMOS effective channel length: GT in NW part channel length in source/drain direction

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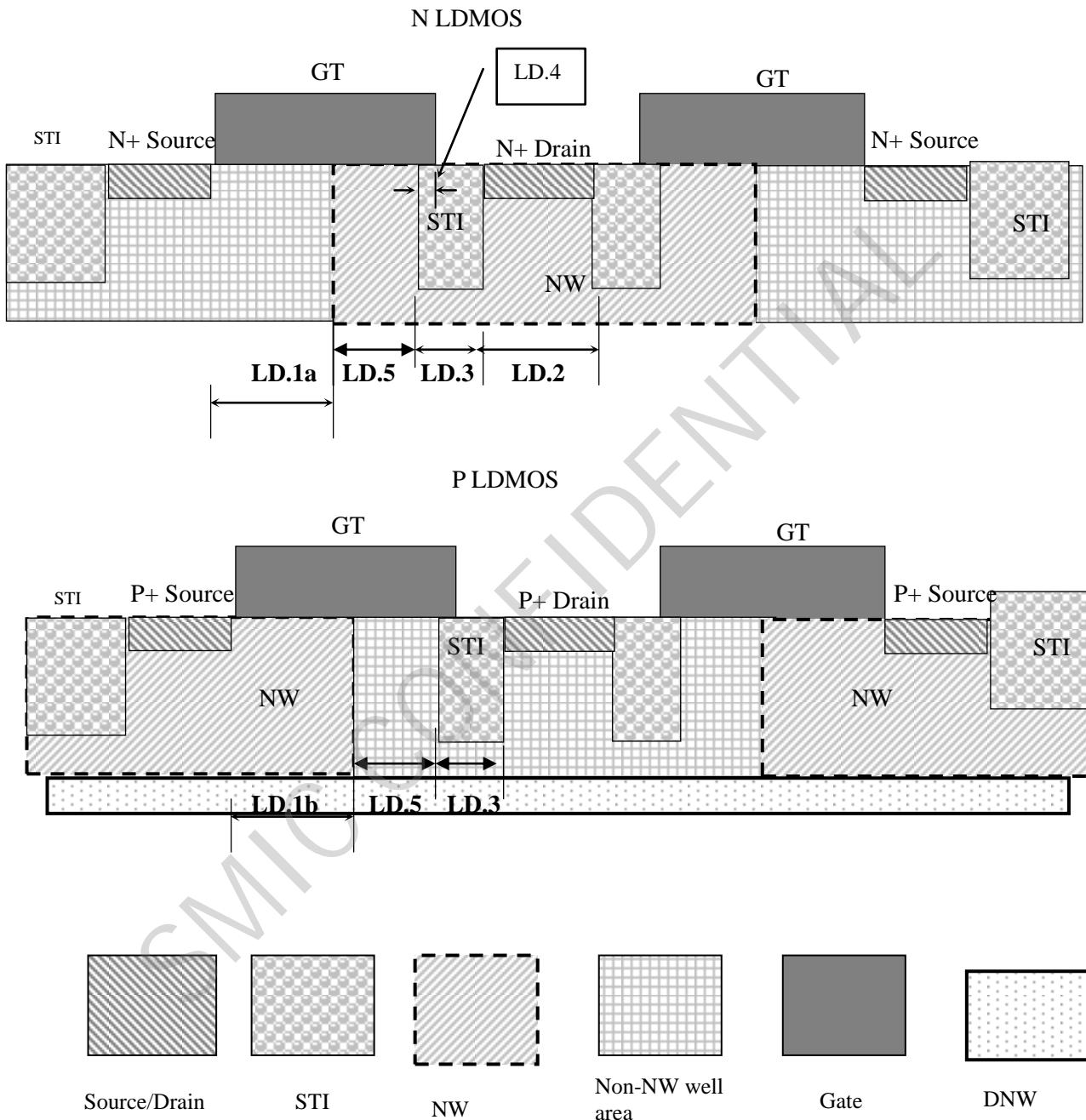


Fig. 7.7.7-1

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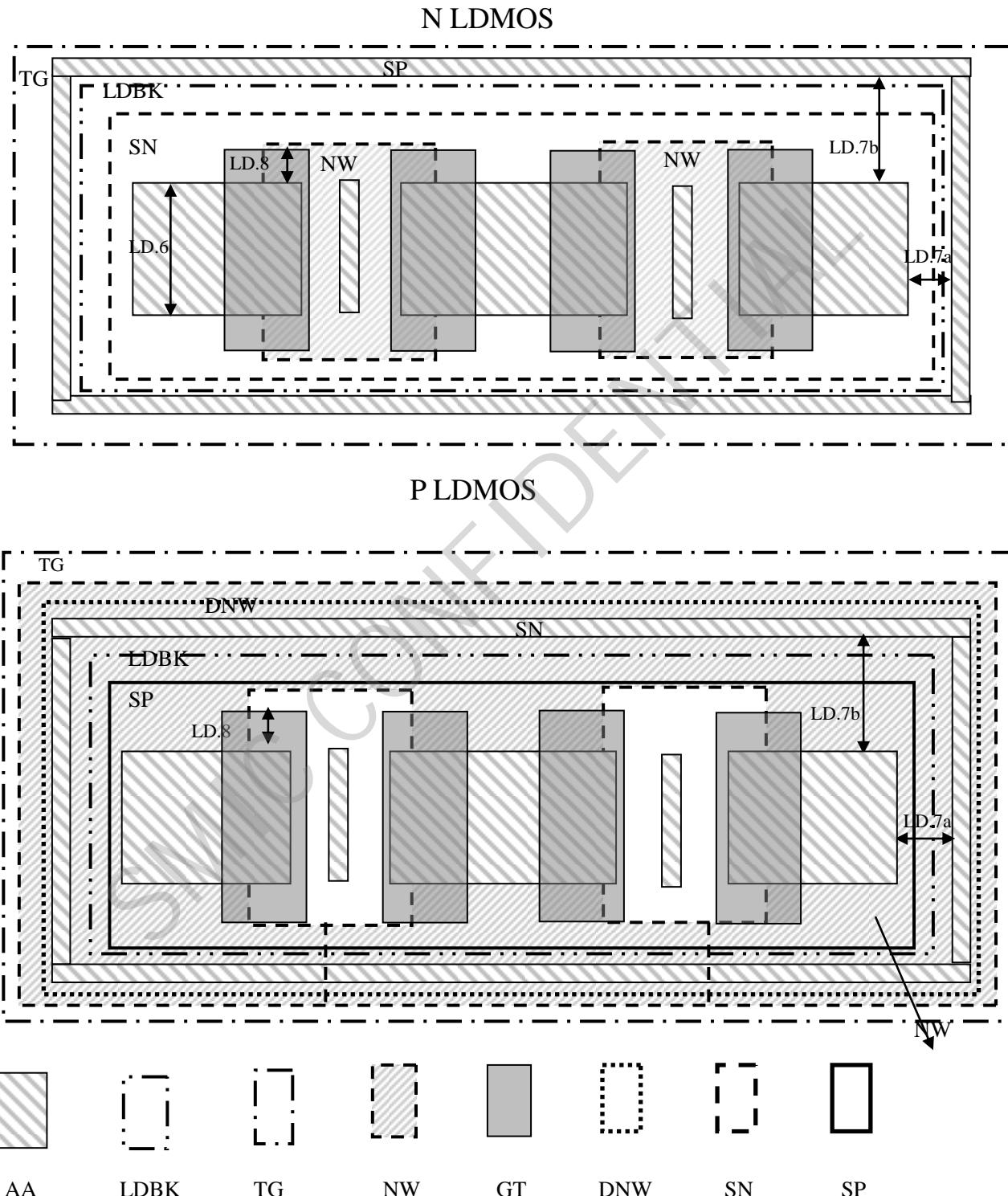


Fig. 7.7.7-2

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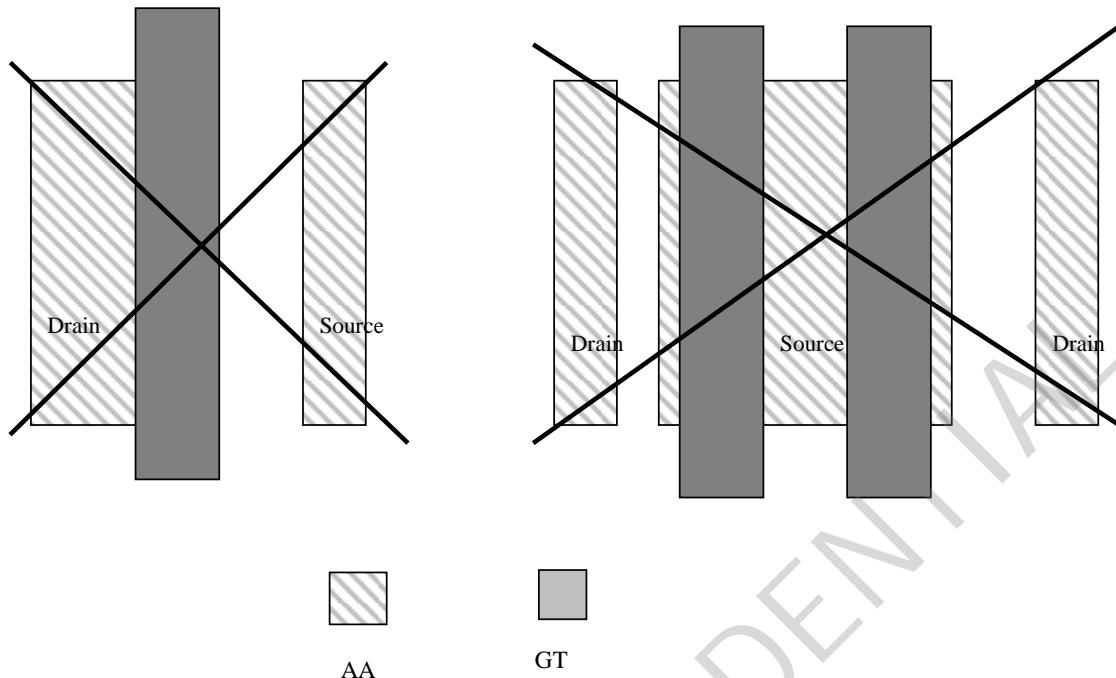


Fig. 7.7.7-3 Illustration for LD.12

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7.7.8 BUMP UBM pad design guideline

This section describes BUMP UBM (Under Bump Metal) layout guideline for designer's reference. Designers should reference the bump plant, testing plant, package plant's related design rule and requirements as final rule. SMIC is not responsible for the issue caused due to violation of the chips final bump plant, test plant, package plant's requirements.

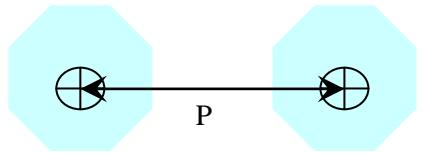
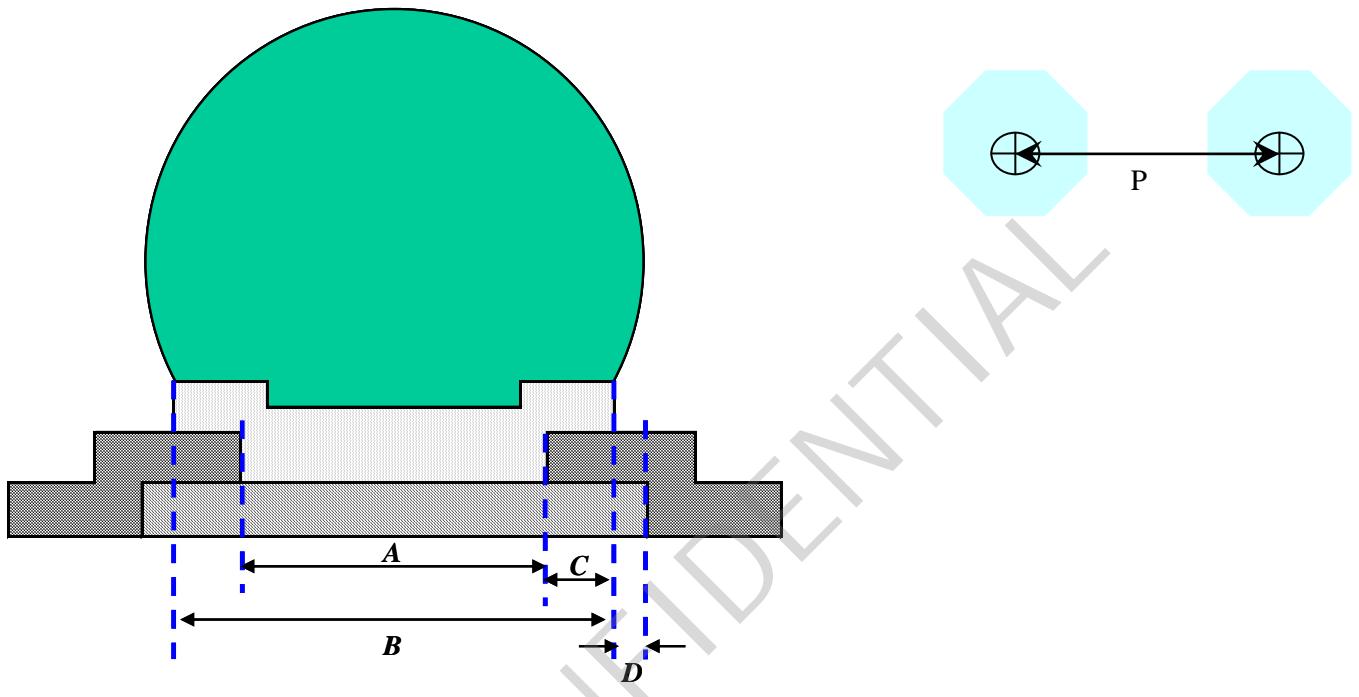
The BUMP in the guidelines stands for layer (168;0). The layer is used for BUMP process opening.

The BUMP described is assumed to have octagon shape.

The dimensions described will have 10% shrink to get to final silicon dimensions.

Rule number	Description	Symbol	Operation	Design Value	Unit
BUMP.1^[G]	BUMP Pitch (center to center space)		\geq	166.67	μm
BUMP.2^[G]	MD width(parallel edge to edge) inside BUMP	A	\geq	61.11	μm
BUMP.3^[G]	BUMP width (parallel edge to edge) Designer should consult with BUMP house the maximum BUMP width allowed.	B	\geq	88.89	μm
BUMP.4^[G]	MD enclosed by BUMP	C	\geq	15.56	μm
BUMP.5^[G]	BUMP enclosure by ALPA	D	\geq	6.67	μm
BUMP.6^[NC]	Distance from center of BUMP to edge of seal ring (MARKS)		\geq	88.89	μm
BUMP.7^[G]	BUMP space		\geq	77.78	μm

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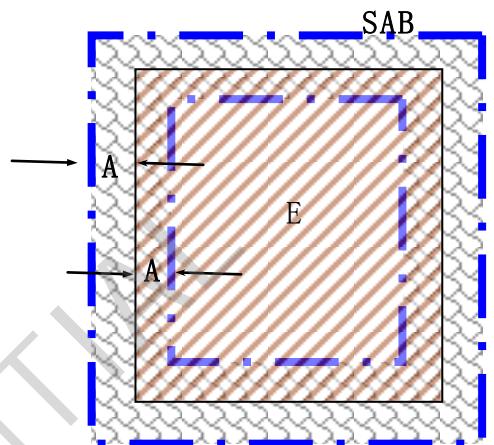
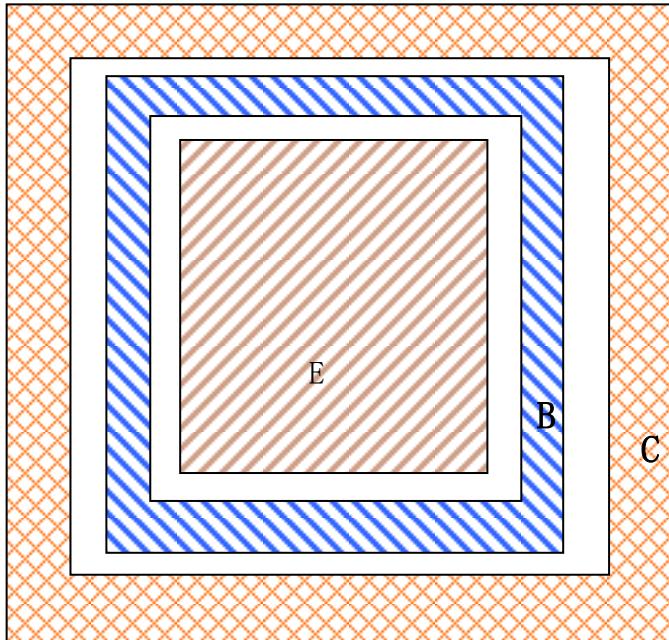
7.7.9 BJT device layout guideline

The BJT devices provided by SMIC are PNP(P+/NW/Psub) and NPN(N+/PW/DNW).

BJT device is marked with BIPOLA(159;1)(for logic operation), DMPNP(134;0)(for LVS) layer. Designer is recommended to use SMIC PDK's BJT layout to get the best prediction result and correct LVS result.

Rules number	Description	Operation	Design Value	Unit
BJT.1 ^{[G][NC]}	SAB straddle on emitter edge. SAB enclose emitter with A um. Emitter overlap SAB with A um.	A =	0.2	μm
BJT.2 ^{[G][NC]}	BJT emitter size(in um) should be either of the following 3 sizes: 2x2, 5x5, 10x10			
BJT.3 ^{[G][NC]}	Marker BIPOLA and DMPNP should cover all AA area for emitter, base and collector to have correct logic operation and LVS.			

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7.7.10 Inductor device layout guideline

The inductor devices should be marked with INDMY(212;0). INDMY should not be used for other purpose than inductor device.

Recommend designer to use the inductor provided by SMIC PDK to have better characterization prediction and LVS check.

For detail inductor model and other guides, designer may refer to TD-MM40-RM-2001.

Rules number	Description	Operation	Recommend Value	Unit
IND.W.1^{[G][NC]}	The inductor coil metal width for MTT2.	\geq	8	μm
IND.S.1^{[G][NC]}	The inductor coil metal space for MTT2.	\geq	2	μm
IND.EN.1^{[G][NC]}	INDMY enclose inductor coil metal	\geq	50	μm
IND.R.1^{[G][NC]}	V_n (n=1-8) are not allowed within inductor coil metal area to reduce parasitic capacitance			
IND.R.2^{[G][NC]}	Do not allow non-inductor related layouts within INDMY. Only the patterns been put into inductor characterization allowed.			
IND.R.3^{[G][NC]}	Active device and layouts space to INDMY	\geq	10	μm
IND.R.4^{[G][NC]}	Make the inductor regions within chip to be evenly spread to have balanced pattern density.			
IND.R.5^{[G][NC]}	SMIC dummy insertion script does not block out inductor area. Designer should add related dummy block layers.			
IND.R.6^[G]	Maximum density of INDMY in whole chip	\leq	5%	
IND.R.7^[G]	Maximum M1/Mn density within (INDDMY SIZING 16 μm) in window 125 μm x 125 μm , stepping 62.5 μm	\leq	85%	
IND.R.8^[G]	M1/Mn/TM1/TM2 metal density over the whole chip (include INDDMY)	\geq	20%	
IND.R.9^[G]	TM1/TM2/MMT2 density range in window 200 μm x 200 μm , stepping 100 μm . The following special regions are excluded while the density checking: PA,MARKS, LOGO,INDMY This rule is only applied while the width of (checking window NOT excluded region) \geq =50 μm .	\geq	15%	
		\leq	85%	
IND.R.10^[G]	Maximum density of INDMY in window 1600 μm x 1600 μm , stepping 800 μm	\leq	14%	

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7.7.11 MOM device layout guideline

MOM(metal oxide metal) capacitor is based on the capacitance between parallel same layer metal lines and different layer metal lines

MOMDMY(211;1) is a mark layer for MOM region, including terminal and capacitor area

MOMMKn(211;11~211;18) is a mark layer to identify the MOM region, only enclose finger area.

Recommend designer to use the MOM provided by SMIC PDK to have better characterization prediction and LVS check.

Layer name	GDS No	Data Type	Description
MOMDMY	211	1	LVS marking layer to identify MOM device
MOMMK1	211	11	DRC marking layer to identify M1 MOM region
MOMMK2	211	12	DRC marking layer to identify M2 MOM region
MOMMK3	211	13	DRC marking layer to identify M3 MOM region
MOMMK4	211	14	DRC marking layer to identify M4 MOM region
MOMMK5	211	15	DRC marking layer to identify M5 MOM region
MOMMK6	211	16	DRC marking layer to identify M6 MOM region
MOMMK7	211	17	DRC marking layer to identify M7 MOM region
MOMMK8	211	18	DRC marking layer to identify M8 MOM region

Rules number	Description	Operation	Design Value	Unit
MOM.1^{[G][NC]}	Use symmetrical dummy metal around the matched pairs of MOM cells instead of auto inserted dummy.			
MOM.2^{[G][NC]}	Active device underneath or above MOM cell should be put into couple capacitance consideration in design.			
MOM.3^{[G][NC]}	SMIC dummy insertion script does not block out MOM area. Designer should add related dummy block layers.			
MOM.4^{[G][NC]}	MOMDMY and MOMMKn layers are must for MOM device			
MOM.5^[G]	It is not allowed: 1) V1 in MOMMK1 2) Vn/Vn-1 in MOMMKn (n=2~8), where Vn-1 is the via underneath Mn, and Vn is the via above Mn. Vn can be inter-via or TV1 or TV2.			
MOM.6^[G]	The space between (Mn AND MOMMKn AND MOMDMY) and Vn /Vn-1 (n=1~8) outside of MOMDMY, where Vn-1 is the via underneath Mn, and Vn is the via above Mn. Vn can be inter-via or TV1 or TV2.	≥	0.08	um

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7.7.12 DUP (Device Under Pad) Pad Guidelines

DUPMK1 (89;156) is the marking layer for pad with device underneath.

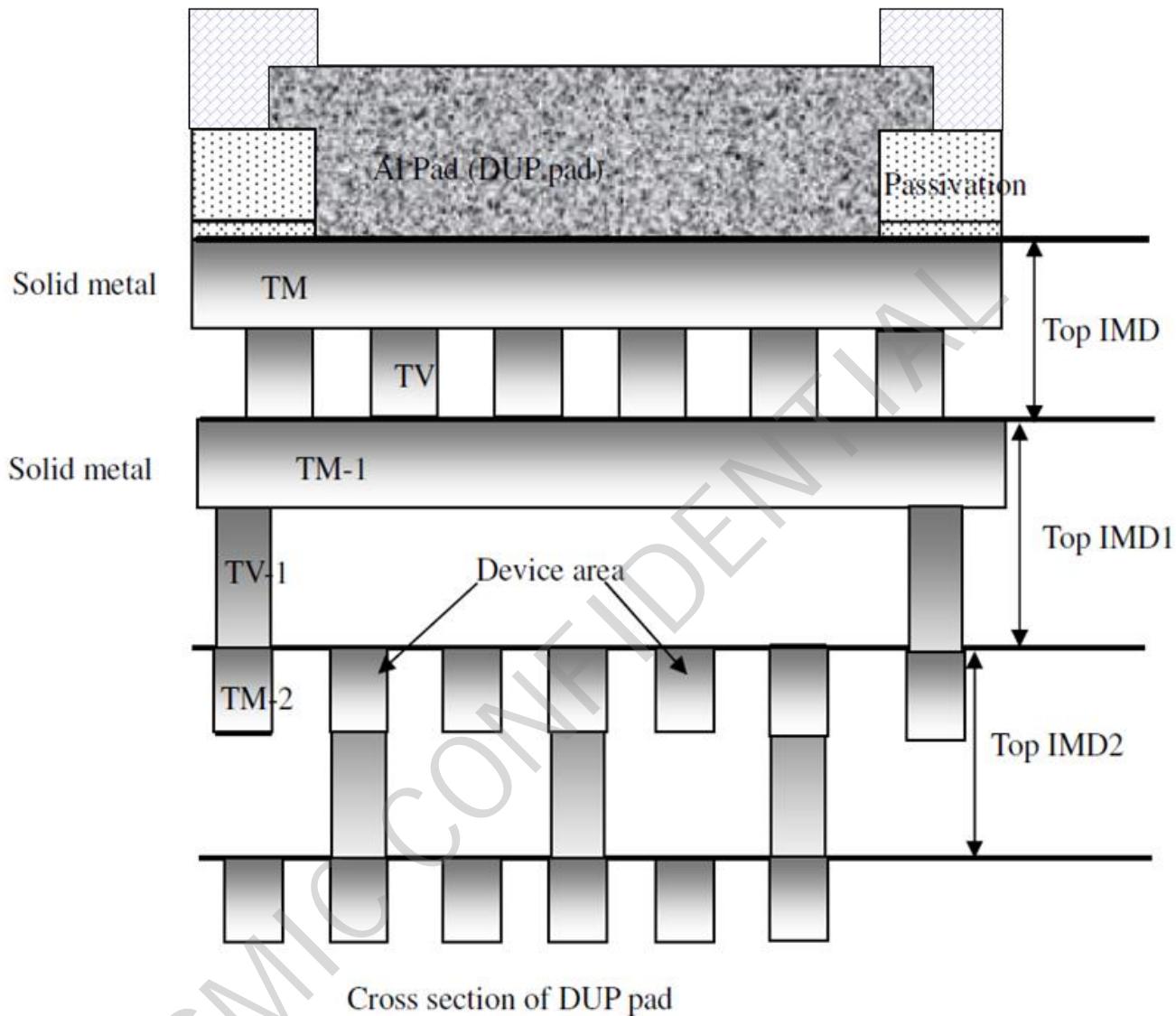
DUP pad area in below rules is ((DUPMK1 AND MD)

Rules Number	DESCRIPTION	Operation	Layout Value	Unit
DUP.1 ^[G]	For MD that interacts with DUPMK1, this piece of MD must be fully covered by DUPMK1.			
DUP.2 ^[G]	Two metal layers (TM and TM-1) are needed in DUP pad area, these two metal layers design must be solid.			
DUP.2a ^[NC]	It's not allowed to add metal slots for TM and TM-1 in the DUP pad area.			
DUP.3 ^[NC]	Device (transistor, metal resistor, BJT, etc) must be located underneath TM-1 layer.			
DUP.3a ^[G]	ALPAR, MOMDMY, INDMY, TM2R, TM-1R(TM-1 resistor mark layer) must be outside of DUP pad area.			
DUP.4 ^[G]	TV-1 pattern must be outside of DUP pad area			
DUP.5 ^[G]	DUP pad area must have TV array between TM and TM-1. Two Via areas whose space is within 0.56 μm are considered to be in the same array. TV space within array in DUP pad opening area should follow TV2.3.			

Notes:

1. TM is TM2 or MTT2.
2. TM-1 is the metal layer directly underneath TM layer. It can be inter-metal (Mn) or TM1.
3. TV is TV2. TV-1(connecting TM-1 and TM-2) is directly underneath TV layer, it can be inter-via (Vn) or TV1.

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7.7.12.1 In-line Bond Pad Design

Inline bond PAD design is shown as Fig 7.7.12.1 and table 7.7.12.1:

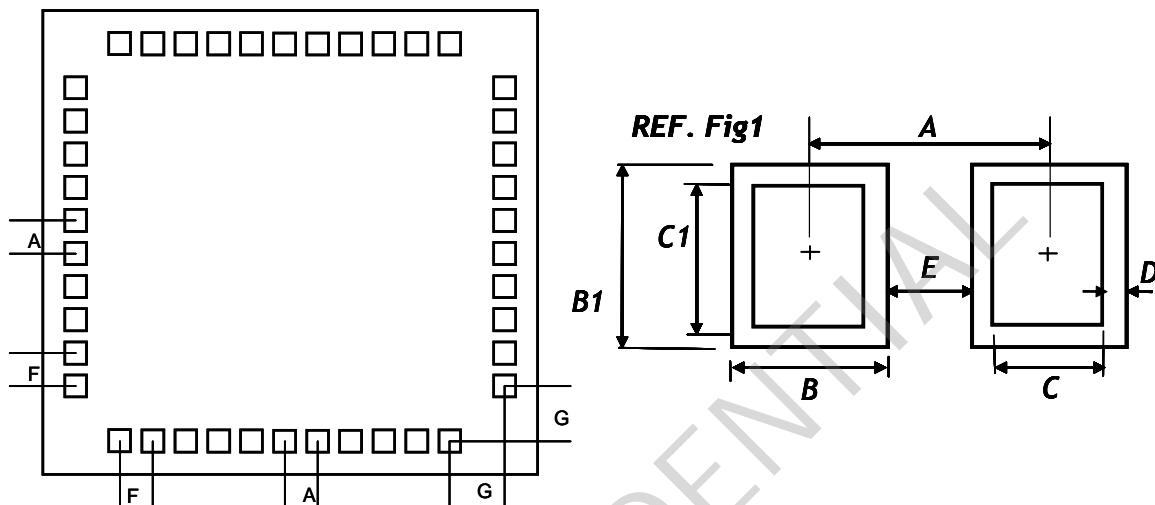


Fig 7.7.12.1 Inline bond PAD design

Table 7.7.12.1 Key items of Inline bond PAD design

RULE NO.	DESCRIPTION	Rule Min (μm)
7.7.12.1.A ^[NC]	In-line Bond Pad Pitch	55.55
7.7.12.1.B ^[NC]	Bond Pad Siz	52.77
7.7.12.1.B1 ^[NC]	Bond Pad Size	71.00
7.7.12.1.C ^[NC]	Bond Pad Opening	48.33
7.7.12.1.C1 ^[NC]	Bond Pad Opening	66.55
7.7.12.1.D ^[NC]	Passivation Area On Pad	2.225
7.7.12.1.E ^[NC]	In-line Pad to Pad Space	2.78
7.7.12.1.F ^[NC]	Bond Pad Pitch at Corner 5 Pads	96.00
7.7.12.1.G ^[NC]	Corner Pad Distance	210.00

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7.7.12.2 Stagger Bond Pad Design

Stagger bond PAD design is shown as Fig 7.7.12.2 and table 7.7.12.2:

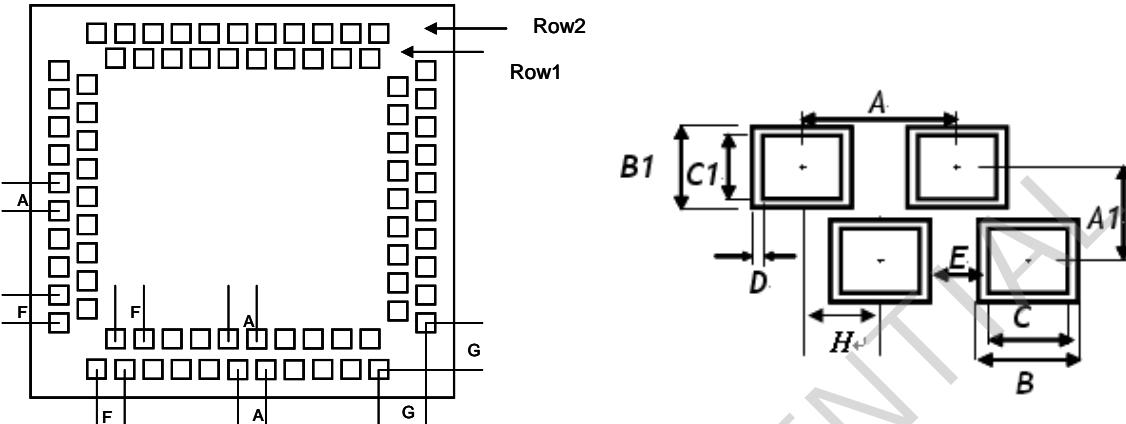


Fig7.7.12.2 Stagger bond PAD design

Table 7.7.12.2 Stagger bond PAD design

RULE NO.	DESCRIPTION	Rule Min (μm)
7.7.12.2.A ^[NC]	In-line Bond Pad Pitch	55.55
7.7.12.2.A1 ^[NC]	Staggered Pitch of ROW1–ROW2 Pad	74.00
7.7.12.2.B ^[NC]	Bond Pad Siz	52.77
7.7.12.2.B1 ^[NC]	Bond Pad Size	71.00
7.7.12.2.C ^[NC]	Bond Pad Opening	48.33
7.7.12.2.C1 ^[NC]	Bond Pad Opening	66.55
7.7.12.2.D ^[NC]	Passivation Area On Pad	2.225
7.7.12.2.E ^[NC]	In-line Pad to Pad Space	2.78
7.7.12.2.F ^[NC]	Bond Pad Pitch at Corner 5 Pads	96.00
7.7.12.2.G ^[NC]	Corner Pad Distance	210.00
7.7.12.2.H ^[NC]	Staggered Pad shift of ROW1–ROW2 Pad	27.78



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7.7.13 Logo Design Guideline

Please use rectangular or 45-degree polygons to write words, logos, and other marks that are not part of the circuit.

1. Product label region must be fully covered by LOGO (26;0) marking layer.
2. Please don't use minimum rule for LOGO pattern, except CT and Via layer.

For the minimum width and space are less than 1um rules, please use greater, or equal 1um of width and space to draw LOGO patterns.

If the minimum rule value is greater than 1um, please follow the minimum rule at least.

Rule number	Description	Operation	Rule Value	Unit
LOGO.1 ^[G]	Space between LOGO and AA, GT or Metal. DRC doesn't check dummy AA, dummy GT, dummy metal.	\geq	10	um
LOGO.2 ^[G]	LOGO overlap with PA, ALPA is not allowed.			
LOGO.3 ^[NC]	A circuit in the LOGO is not allowed.			

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8. Attachment:

1. 40NM_SEALRING_DRC_SAMPLE.gds
2. OCCD sample GDS
3. OCOVL sample GDS

9. Detail change note**9.1 Chronicle detail change note**

Doc. Rev.	Change Date	Author	Change Description
1T	2011-09-08	Sam Mao Wind He Tom Hu Feng Ji Shuai Zhang	<ol style="list-style-type: none">1. Mod Doc. Title; “note” in page 4; purpose; Grid Size des; layer mapping table and device truth table.2. Add the definition of “Gate”3. Del all notes “Note: R means “Recommended””4. Mod all “Design min(um)” to “Design (um)”5. Mod 7.3.7 Design Rules Syntax6. Del AA.1R/3, RESAA.2R/3R, AA.C.27. Add AA.1a/4c/9a/12/13/14/15, RESAA.11/12/138. Mod AA.1/2/4b/5/6/7/8/9/10, RESAA.2/7 des9. Mod AA.1/4a value10. Mod RESAA.3/7 value11. Mod AA.C.1/3/4/5 des.12. Del NW.213. Mod NW.1/3/4/5/6 des. and value.14. Add NW.915. Add 7.4.4 NW: N-Well Resistor Rule16. Mod DNW.5/6 des.17. Mod PSUB.2/3a/3b/3c/5a/5b des.18. Mod PSUB.2 value19. Del PSUB.8,20. Mod PSUB.1, PSUB.4 value.21. Del SDOP: SRAM PG Implant Layer Rules22. Mod T(D)G.1/2/3/4/5/6 des..23. Add T(D)G.10/11/12/13/14,TG.1524. Add BORDER (CHIPEDGE) rules.25. Mod GT rule name26. Mod GT.1/2/3a/4/5/6/7/16/19/21/23 des.27. Mod GT.5/7/8/9/10/13/16/17/18 value28. Add GT.2a/2b/24/24a/25/25a29. Del GT.3b/11/14/1530. Del RESP1.2R/3R.31. Mod RESP1.1/6/7 des.32. Mod RESP1.2/3/6/7 value33. Add RESP1.11/12/1334. Add LVT and HVT rules.35. Mod N(P)LL.4, LVN(P).4, VTN(P)H.4, N(P)LH.4, N(P)LHT.4, SN(P).6 value to 0.22.36. Mod N(P)LL.1/2/3/4/5/6/7/8/9/13 des.37. Mod LVN(P).1/2/3/4/5/6/7/8/9/13 des.38. Mod VTN(P)H.1/2/3/4/5/6/7/8/9/13 des.39. Mod N(P)LH.1/2/3/4/5/6/7/8/9/13 des.40. Mod N(P)LHT.1/2/3/4/5/6/7/8/9/13 des.

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Doc. Rev.	Change Date	Author	Change Description
			<ul style="list-style-type: none">41. Mod N(P)LL.3/4/5/6, LVN(P).3/4/5/6, VTN(P)H.3/4/5/6, N(P)LH.3/4/ 5/6, N(P)LHT.3/4/5/6 value42. Del N(P)LL.8, LVN(P).8, VTN(P)H.8, N(P)LH.8, N(P)LHT.8, SN (P).11.43. Add N(P)LL.14, LVN(P).14, VTN(P)H.14, N(P)LH.14, N(P)LHT. 1444. Del N(P)C: SRAM N(P)MOS Implant Layer Rules45. Mod SN(P).1/2/3/4/5/6/7/7a/8a/8b/9/10/12/13/14/15/16/20 des.46. Mod SN(P).4/7a/8a/9/12/14/16/18/19/20 value47. Add SN(P).7b,SN.2248. Mod SAB.1/2/3/4/5/6/7/8/9/11 des.49. Mod SAB.5/10 value50. Del SAB.9,SN(P).1951. Add SAB.1552. Del CT.2R53. Mod CT.1/2/3/4/5/5a/6/7/8/9/10/11 des.54. Mod CT.3/8/9 value.55. Add CT.2a/3a/6a/6b/7a/7b/14/15/16/17/1856. Mod CT array logic operation to (((all CTs su0.09) sd0.3) su0.21)57. Mod 7.4.24 "SMIC 0.04um BEOL Design Rule Summary"58. Mod M1(n).4/6 value & desc; Del M1.7c, M1.7d59. Mod V1(n).3/6/6d/7/7d/14, M1(n).4/6/6a/6b/6c/7 des; Mod V1.3, Vn.3 to 0.09 from 0.075; Mod V1(n).6a/7a from 0.017 to 0.015; Mod V1(n).6/6d/7 des.; Add V1(n).7d60. Del TV1.8 and TV2.861. Mod MD.4/6 des.62. Del ALPA.3;Add ALPA.8/9/1063. Mod PA.2 value; PA.10 wording64. Mod 7.4.39 EXCLLU Rules65. Mod 7.4.40 current density rules and 7.4.41 rules66. Rev. AA.10 desc to make it clear.
1T	2011-09-08	MengFeng	<ul style="list-style-type: none">67. del GT.12, LVN.11, LVP.11, VTNH.11, VTPH.11, LVT.11, HVT. 1168. LVT.7, LVN.7,LVP.7, HVT.7, VTNH.7, VTPH.7 change rule value to 0.0269. LVT.3a,LVN.3a,LVP.3a,HVT.3a,VTNH.3a,VTNH.3a chg rule value to 0.01, chg description.70. del LVT.3b,LVN.3b,LVP.3b,HVT.3b,VTNH.3b,VTNH.3b71. del LVT.2, HVT.272. LVT.4,HVT.4,LVN.4,LVP.4,VTNH.4,VTPH.4 chg rule value to 0.1473. del LVT.10,11,14; del HVT.10,11,1474. chg AA.13 rule value to 0.04575. SN.6,SP.6,SN.7a,SP.7a rule value chg to 0.1676. Mod GT.19 desc and rule value77. Del V1.3,Vn.3 => not correct. Did not delete them. Should not delete.(2011-08-02)78. Merge ALPA and RDL rules as ALPA rule
1T	2011-09-08	Shuai Zhang	<ul style="list-style-type: none">79. modify Vn6.d, Vn7.d description80. Modify ALPA rules
1T	2011-09-08	MengFeng	<ul style="list-style-type: none">81. del RESP1.1082. Modify values 0.18 to 0.14 for LVT.4, HVT.483. modify values 0.02 to 0.010 for LVT.7, HVT.7
1T	2011-09-08	Mengfeng	<ul style="list-style-type: none">84. Modify GT.1c IO 2.5V min poly CD from 0.26 to 0.27 um.

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Doc. Rev.	Change Date	Author	Change Description
1T	2011-09-08	Shuai Zhang, MengFeng	85. restore TV1.8, TV2.8. not delete. Correct TV1.9 mis-insert error. 86. Add DUMC.38, DUMC.39 87. change PSUB.3c rule number to 1.2 88. change NW.3 desc "potential" to "net" 89. revise NW.4 desc "potential" to "net". Del desc of 0.9/1.0/1.1/1.2V 90. Del NW.5, NW.6 91. Revise LVN.3a, LVP.3a, VTPH.3a, HVT.3a corrected from 0.02 to 0.01 92. Revise LVN.7, LVP.7, VTNH.7, VTPH.7 from 0.02 to 0.01 93. modify PLH.3b 0.08 to 0.05 94. corrected SAB.5, 9,10, 15 different from previous version issue 95. Fig 7.3.6.5-1 label corrected to make them clear 96. Fig of AA.4a W1, del "< 0.14" in the fig 97. del ALPA.8 as repeated definition in the note for ALRDL
1T	2011-09-08	MengFeng	98. Revise PSUB.3b rule value 0.45 to 0.8
1T	2011-09-08	MengFeng	99. Modify Grid size to fix only 0.001um
1T	2011-09-08	Mengfeng Shuai Zhang	100.TG.11 "poly" change to "non-floating poly" 101.del MD.7, MD.9 102.Modify TM1.5, TM1.6, TM2.5,TM2.6 des.
1T	2011-09-08	MengFeng Shuai Zhang	103.Add definition of "floating", "non-floating" in 7.3.6.6 DR nomenclatures. 104.Delete ALPA.4 for no MD(PAS2) polyimide process now.
1T	2011-09-08	MengFeng	105.BORDER section adds guide line for BORDER and circuit min space 0.36um. 106.page 95, 97 diagram NW figure correct to make it close. 107. figure 7.3.6.1-1 title changed to "Gate related definition" 108.change GT.9, GT.10 rule number from 0.14 to 0.13
1T	2011-09-08	Daniel Lu	109.Merge design rule and DFM rule TD-LO40-DR-2002 (2TV0.2) into one document because system integration, i.e. section 7 in original DFM rule document is copied to 7.5 in this document, but made some modifications list as below. (1) Delete 'design service' words in 7.5.3 and 7.5.6 (2) Modify DFM3 , DFM.9, DFM11 by replace 'POLY' with 'GT' to align with design rule document. (3) Modify DFM.8 by replace 'POLY.1' with 'GT.1a' (4) Add a diagram to describe DFM.10 (5) Add 'Designer can waive the violations if design passes sign-off level signal integrity check' in DFM.5 (6) Add a DFM rule as DFM.26 (7) Modify DFM.9 value from 0.11 to 0.07 (8) Modify DFM.13 value from 0.30 to 0.18 (9) Delete 7.2 in original DFM rule document and re-organize the sub-title numbers in 7.5 of this document Note: The DFM rule changed value had been updated in 2010-12-29 DRC script.
1T	2011-09-08	MengFeng Shuai Zhang	110. Delete 40LL and 40G mask truth table 111.LDD.4 0.14-> 0.18: LVT.4, HVT.4, LVN.4, LVP.4, VTNH.4, VTPH.4. According to org decision. 112.Add note in GT. All memory cell transistor GT direction should be aligned in one chip. 113.Add MD.10: MD must be drawn layer
1T	2011-09-08	MengFeng	114. PLL.4 description changed to similar to NLL.4 to correct edit error.
1T	2011-09-08	Daniel Lu	115.Add a DFM rule as DFM.27 in section 7.5, and related figure
1T	2011-09-08	Shuai Zhang	116. Add 7.4.38: Guidelines for Seal Ring section

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1T	2011-09-08	MengFeng	117.replace 40LL layer map table to be the same as Top Tier system's. 118.LDD.4 0.18-> 0.14: LVT.4, HVT.4, LVN.4, LVP.4, VTNH.4, VTPH.4. According to org decision. Note: The changes from 2011-1-1 till 1-31 does not need DRC script update.
1T	2011-09-08	MengFeng	119.Corrected DNW picture. DNW zone picture transparency changed from 50% to 0% for reader to have better recognition of DNW and NW separation. 120.40LL & 40G design truth table add HPBL(60:150) for SP374 and DP741 cells. 121.Remove 40LL design truth table Q242(Q299S) SRAM Cell Devices BIPOLA mark. 122.Delete seal ring section. Plan to put Seal ring into separated DR for better management.
1T	2011-09-08	MengFeng	123.Add PSUB.3d for native device 2.5V overdrive 3.3V min channel length. 124.Table 7.3.1-1 40LL layer map table filled in some layers missed option/must description 125.Table 7.3.1-2 40LL layer and nomenclature table: delete the repeated "LOGO" layer description row in the table 126.Table 7.3.3-2 40G layer and nomenclature table: delete the repeated "LOGO" layer description row in the table 127.Remove section title specification on voltage (Core 0.9/1.1/1.2V device) for 7.4.12 LVN, 7.4.13 VTNH, 7.4.17 LVP, 7.4.18 VTPH 128.Modify section tile to make it clear: 7.4.5 TG, 7.4.6 DG, 7.4.11 NLL, 7.4.14 NLH, 7.4.15 NLHT, 7.4.16 PLL, 7.4.19 PLH, 7.4.20 PLHT 129.Add 7.4.39.1 temperature coefficient sub-section in current density rule 130.Border section revised to align other section formation. Add note. 131.BORDER.1 description add "BORDER to include all chip patterns" 132.Modify AA.11 rule description to correct grammar error. 133.Modify 7.3.6.4 title to add "Orientation" 134.Add some sub sections in 7.3.6 Design rule syntax: Spacing, Overlap, Containment, Logical Function, Sizing Funcion, Relational Selection Function. Revise the syntax to align with 45nm DR.
1T	2011-09-08	MengFeng	135. BORDER.2 description modification to include dummy pattern into the BORDER space check. 136.Add MD.11 to prevent small passivation 1(PA) under MD
1T	2011-09-08	MengFeng	137. delete DUMC.4 dummy AA straddle DNW prohibition
1T	2011-09-08	MengFeng	138.Modify DUMC.15 description to constrain on AA with DR value changed from 0.64 to 0.14 139.add DUMC.15a for dummy GT to GT on field OX with the same rule number 0.1 as GT rule. 140.Modify DUMC.16 description. Remove the AA constrain. 141.Add DUMC.16a for dummy GT space to AA. Put the DR value same as GT section's GT to AA min space 0.03
1T	2011-09-08	Melody Yan	142.Modify 7.3.6 Design Rule Syntax sections to make it more comprehensive
1T	2011-09-08	Melody Yan	143.Modify SN.22 description from "SN minimum width and length if the area touch with gate" to "SN minimum width and length if there is gate within SN". To make meaning clear. 144.AA.11: add in description "(exclude LDMOS area, the AA within LDBK layer)" 145.Put LDMOS mark layer LDBK(216;150) into the layer Table 7.3.1-2 for 40LL and Table 7.3.3-2 for 40G.
1T	2011-09-08	MengFeng	146.Modify SP299 GDS layer number in Table 7.3.3-2 for 40G from 60;2 to 60;10 to comply with sample GDS layer number. 147.Modify MD.5 description with "if MD not touch with PA" to make meaning more clear.

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1T	2011-09-08	MengFeng	148. Remove AAING in DUMC.2, DUMC.5 149. Remove GTING in DUMC.12, DUMC.15,DUMC.15a 150. Remove VxING in DUMC.22 151. Remove MxING in DUMC.21 152. Remove following items in 7.3.5 dummy pattern layer map table: PCIS, BFMOAT, AAING, GTING, CTING, V1ING, V2ING, V3ING, V4ING, V5ING, M1ING, M2ING, M3ING, M4ING, M5ING, M6ING, M7ING, M8ING. 153. Change P+AA definition in 7.3.6.13 from “(AA over (SP over NW)” to “(AA over SP)” 154. Add “Field OX” definition in 7.3.6.13 Design Rules Nomenclatures and Abbreviations. 155. SN.22 description modification: remove “and length” and correct the typo “thre” to “there”.
1T	2011-09-08	Jun Zhao	156. Dummy check rules rule number modifications: DUMC.19 3.0 to 3.33, DUMC.20 0.2 to 0.22, DUMC.21 0.48 to 0.22, DUMC.25a 0.03 to 0.03, DUMC.25b 0.03 to 0.03, DUMC.26 1.6 to 1.78, DUMC.28 2.56 to 2.84, DUMC.29 2.56 to 2.84, DUMC.32 0.07 to 0.22, DUMC.33 0.2 to 0.22, DUMC.34 0.4 to 0.44, DUMC.35 1.6 to 1.78, DUMC.36 4.00 to 4.44, DUMC.37 2.56 to 2.84
1T	2011-09-08	Gorton Zhang, Melody Yan	157. Modify DUMC.5 check rule from 0.64 to 0.710 Modify DUMC.6 check rule from 0.2 to 0.220 Modify DUMC.7 check rule from 3 to 3.330 Modify DUMC.8 check rule from 0.24 to 0.260 Modify DUMC.9 check rule from 0.24 to 0.260 Modify DUMC.13 check rule from 0.04 to 0.044 Modify DUMC.14 check rule from 0.1 to 0.110 Modify DUMC.15 check rule from 0.14 to 0.150. Modify DUMC.15a check rule from 0.1 to 0.110 Modify DUMC.16 check rule from 0.2 to 0.220 Modify DUMC.16a check rule from 0.03 to 0.033 Modify DUMC.17 check rule from 3 to 3.330
1T	2011-09-08	MengFeng Tsai	158. GT.5 add “Exclude gate within LDMOS region(within LDBK)” to prevent miss alarm in LDMOS structure. 159. GT.16 modify “within BORDER” to “within whole GDS area” to better cover the layout without BORDER drawn.
1T	2011-09-08	MengFeng Tsai	160. Add in Table 7.3.2 40LL device truth table 2P562 bit cell PU, PD,PG related and add 2PSRAM(60;12) for this bit cell. Corrected SP299 cell mark layer to be DNSRAM(60;2) 161. Table 7.3.1-2 40LL layer table: correct SP299 layer from 60;10 to 60;2 DNSRAM; add SP374 layer LRSRAM(60;5); add 2P562 layer 2PSRAM(60;12). Modified the SRAM mark layer’s description to be proper. 162. Table 7.3.3-2 40G layer map table add 2P562 2PSRAM(60;12) layer
1T	2011-09-08	MengFeng Tsai	163. Add section 7.1.1 Dummy pattern data type requirements 164. Add 7.4.40 corner rules

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1T	2011-09-08	MengFeng Tsai	165.Modify AA.5, AA.7, AA.8 to exclude LDMOS region(within LDBK) 166.Delete DG.10 rule of "DG shapes must be orthogonal"
1T	2011-09-08	MengFeng Tsai	167.Added in 7.4.40 Chip corner Rules Note.1 and Note. 2 to specify the layers for rule check and specify only chips with seal ring fit for this rule. 168.Revise 7.3.5 title to contain dummy and mix signal related layers 169.Change original dummy layer table into 7.3.5.1 "dummy layer map table". 170.Add 7.3.5.2 "Mix signal related layer map table" 171.Add 7.3.6.13 item for line end and line corner and related fixtures. 172.Delete MARKF(190;0) from Table 7.3.1-2 40LL layers and Table 7.3.3-2 40G layers. It is not used in 40nm
1T	2011-09-08	MengFeng Tsai	173.Modify 7.3.5.2 layer table P2 description to fit with 40nm technology providing. 174.Add 7.3.5.2 mix signal layer tabloe MIM layer MIM (58;0) 175.Add 7.4.40 chip corner rule note.3 as reminding to turn off chip corner rule option if seal ring not needed to insert.
1T	2011-09-08	MengFeng Tsai	176.Add ALPA into 7.1.1 dummy pattern data requirement. Add into item "a" ALDUM (83;11) for ALPA's dummy. 177.Add ALDUM(83;11) into table 7.3.3-1 40G mask layer table 178.Re-organize 7.4.38 to 7.4.38.1 to "Dummy pattern Check Rules for SMIC dummy" and 7.4.38.2 "Dummy pattern check rules for non-SMIC dummy". 7.4.38.1 is the same as before. 7.4.38.2 rules are newly added. 179.Add definition of corner via and corner contact in 7.3.6.13 as "The vias or contacts which have the nearest distance to the related said AA, GT or metal corner"
1T	2011-09-08	MengFeng Tsai	180.Delete CT, Via, TV , PA BAR related rules as these only apply to seal ring, and to be defined in seal ring DR. Following BAR related rules are deleted: CT.14, CT.15, CT.16, CT.17, CT.18, V1.11, V1.12, V1.13, V1.14, V1.15, Vn.11, Vn.12, Vn.13, Vn.14, Vn.15, TV1.8, TV1.9, TV1.10, TV1.11, TV1.12, TV2.8, TV2.9, TV2.10, TV2.11, TV2.12, PA.5, PA.6, PA.7, PA.8 181.Add note after Table 7.3.1-1 for ESD mask making. "About ESD1(Mask# 110) ESD implant mask making logic operation, 40LL formula table SMICLC40LL0 for ESD1 only can be used for SMIC provided IO or ESD component. For non-SMIC designed ESD and IO, user should consult with SMIC tape out sponsors for suitable formula."
1T	2011-09-08	MengFeng Tsai	182.Delete section 7.4.40 chip corner rule 1 st paragraph sentence about eh seal ring insertion rule "For seal ring detail design, please refer to document TD-LO40-DR-2008." 183.Revise 7.4.40 chip corner rule Note 1, remove the CT, Vn, TV1, TV2 from DRC check to reduce DRC check time, as these layers can be covered by other main rules. 184.7.4.7 Border rule note wordings modified for smoother grammar. Change the original note to be note item 1. 185.Add 7.4.7 BORDER rule note 2 to specify the layers to check for BORDER.1 rule. . Purpose: reduce DRC run time. 186.Correct BORDER.2 spelling error in "BORDER" word. 187.Correct BORDER.1 description grammar error. Change "Designer" to "Designers" 188.BORDER.2 : remove "and their related dummy patterns." in description. Reason: dummy pattern do not neet that space concern. 189.Delete RESP1.14. Reason: the process had improved and no need of this rule.
1T	2011-09-08	MengFeng Tsai	190.Modify TG.5 and DG.5 description "AA with transistor (include AA area not under poly)" to "AA with device (include all the devices described in the design truth table 7.3.2, 7.3.4)". Purpose: make the meaning more clear 191.Delete PA.9. Reason: this rule belongs to seal ring and inductor scope. 192.Add section 7.4.41 ESD layout rules 193.Correct 7.4.39.1 "Temperature" spell error 194.Change DUMC.25a 25b rule values from 0.03 to 0.06 to cope with dummy insertion

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			rule's 0.065. 195.Modify GT.22 description. Remove the 2 nd sentence "Intrinsic poly lines are forbidden." to prevent meaning ambiguous."
1T	2011-09-08	MengFeng Tsai	196.Add HP SRAM cell implant mask layers MVP, MVN into table 7.3.1-1 for 40LL mask layers. 197.Add HPBL(60;150), 6TMK(60;151) in table 7.3.1-2 for 40LL layer 198.Add NWH, PWH to table 7.3.1-1 for 40LL mask layers
1T	2011-09-08	Enoch Yue	199.Add HP SRAM cell implant mask layers MVN into table 7.3.3-1 for 40G mask layers. 200.Add HPBL(60;150) ,6TMK(60;151) in table 7.3.3-2 for 40G layer
1T	2011-09-08	MengFeng Tsai	201.Modify CORN.1 rule value from 78 to 74um. 202.Modify GT.1b rule value from 0.2 to 0.15um 203.Add Ref doc in Reference section. 204.Modify 7.4.40 chip corner rule 1 st paragraph. Insert sentence "For seal ring detail design, please refer to seal ring insertion rule(doc number described in Reference section)".
1T	2011-09-08	MengFeng Tsai	205.Modify Table 7.3.3-1 40G mask layer table ALDUM(GDS#83;11) mask layer number from 180 to108. A typo correction. 206.Modify ESD layout check rules to follow 7/13 meeting conclusion. 207.Add ESDIO2(133;3) into table 7.3.1-2 and table 7.3.3-2 for 40LL and 40G layer. 208.Add 7.3.7 Metal options section
1T	2011-09-08	MengFeng Tsai	209.Modify Table 7.3.1-2 and table 7.3.3-2 ESDIO2 layer description to make it clearer. 210.Correct 7.4.41 section prologue ESDIO2(133;3) layer spelling issue. 211.Add in ESD.3, ESD.4 description "minimum" constrain
1T	2011-09-08	MengFeng Tsai	212.Add GT.26, Move original GT Note #2 item to GT.26 for restriction of SRAM GT direction to be aligned one direction in one chip. 213.Add in Table 7.3.1-2 and table 7.3.3-2 layers ESD5V(133;1) and POWERRING(133;2).
1T	2011-09-08	MengFeng Tsai	214. Revise table 7.3.1-2 ESDIO2 description to make it more reasonable. 215. Revise 7.5.2 DFM.1, DFM.2 concerned area from "device" to "Process(physical data)". A 216.Revise ESD1 whole section according to DR committee conclusion ESD1 to be drawn layer. 217. Remove table 7.3.1-1 note. The note comment about ESD1 is moved to ESD1 section 218.Modify MARKG description in table 7.3.1-2, table 7.3.3-2
1T	2011-09-08	MengFeng Tsai	219.Modify ESD1 layout section according to updated input.
1T	2011-09-08	MengFeng Tsai	220.modify table 7.3.3-2 40G ESDIO2 description align with 40LL's table. 221.remove generated layer sections(they are to move to post logic operation DR): NLL, LVN, VTNH, NLH, NLHT, PLL, LVP, VTPH, PLH, PLHT 222.Revise GT.22 description. Remove the "SAB" requirement to align with previous tech nodes.
1T	2011-09-08	MengFeng Tsai	223. Updated ESD1 section prelude wording. 224. Modify Table 7.3.1-1 ESD1 logic operation to "NA". 225.Modify GT section figure GT.2b "W >= 0.6um" to "W" to prevent the value definition different from description W value. 226.Modify GT.26 description "aligned to one direction" to "unidirectional"
1T	2011-09-08	Cindy Zhang	227.Modify Fig. 7.4.41-2 Examples of ESDIO2 mark layers drawing. To make the picture contrast better 228.Add in 7.4.41 3 rd paragraph "The ESD guideline is targeted to meet HBM-2kV, MM-0.2kV and MM-200V specification according to EIA/JEDEC standard

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			and EIA/JESD22 test standard. SMIC does not guarantee to final ESD performance.”
1T	2011-09-08	MengFeng Tsai	229.Modify TM2.12, TM1.13 max line width from 12 to 30um 230.Add 7.4.4 PSUB note #8 to exclude PSUB rules from inductor area(INDMY(212;0)). 231. Modify 7.4.9 LVT section: LVT.2 add back; LVT.3a, 3b merged to LVT.3 with rule value 0.04; LVT.4 rule value changed from 0.14 to 0.16; Add LVT.4a; LVT.5 rule value changed from 0.14 to 0.16; add LVT.5a; delete LVT.7 as LVT.4, 4a cover it; LVT.9 min area changed from 0.19 to 0.1 um^2; Modify LVT.13, TG, DG removed in the description; LVT.14 add back with rule value 0.02um.; picture modified according to rule changed. 232.Modify 7.4.10 HVT section: HVT.2 add back; HVT.3a, 3b merged to HVT.3 with rule value 0.04; HVT.4 rule value changed from 0.14 to 0.16; Add HVT.4a; HVT.5 rule value changed from 0.14 to 0.16; add HVT.5a; delete HVT.7 as HVT.4, 4a cover it; HVT.9 min area changed from 0.19 to 0.1 um^2; Modify HVT.13, TG, DG removed in the description; HVT.14 add back with rule value 0.02um.; picture modified according to rule changed. 233.Modify V1.3, Vn.3 array from 4x4 to 3x3, array row or column 4 to 3. 234.Add Table 7.3.1-3 40LL mask layers and their related GDS layers 235.Dummy check rule to check dummy not within seal ring area. Add MARG in DUMC.2, DUMC.12, DUMC.18, DUMC.26, DUMC.27 236.Added MnDOP,(n=1-8),VnDOP(n=1-7) MTT2DUM, MTT2DUB into table 7.3.5.1 dummy layer map table
1T	2011-09-08	MengFeng Tsai	237.table 7.3.1-1 ESD1 changed from “Must” to “Optional” 238.modify GT.7 description. Add “Wp” into “(poly_end with length Wp < 0.120 μm) to cope with picture. GT picture related with GT.7, the poly end with length changed to variable “Wp” 239.Delete GT.24a and GT.25a. These 2 rules are covered by DFM section. 240.revise PSUB section note#8 to “PSUB under inductor (marked by INDMY) needs not to follow the design rules of PSUB.5a,5b, 6-9” 241. Modify LVT.4, LVT.5, HVT.4, HVT.5 rule value from 0.16 to 0.14 242. Modify LVT.4a, LVT.5a, HVT.4a, HVT.5a rule value from 0.09 to 0.08
1T	2011-09-08	MengFeng Tsai	243.Modify 7.4.4 PSUB note #8, add “note#3, note#7” into inductor immune for PSUB. 244.Add DG.9, TG.9 which was skipped during TG, DG section editting. Add these blank rules to keep table integrity. 245.Correct LVT section figure mark text missed issue. 246.Modify CT.3 related figure to correct the array shape and figure mark
1T	2011-09-08	MengFeng Tsai	247.Delete TG.10 same as DG.10 reason 248.Modify PSUB.4 description to “Space between two PSUB“. Delete the “potential” constrain. 249.Add BORDER.3 for BORDER enclose DNW 0.8um 250.Modify DUMCN.11 dummy metal to other metal space rule value from Mn.2 to Mn.3 to correct the typo. 251.Add 7.1.2 on design rule applicable scope and add item a to exclude seal ring area. 252.Modify 7.1.1 dummy pattern type, add data type 7 into the scope. 253.Modify Table 7.3.1-1 40LL mask layer name and mapping table’s top tier number to version 2 as LCMO40-V00.02. Modify the table according to LCMO40-V00.02
1T	2011-09-08	MengFeng Tsai	254.Modify CT.3. Move the CT array definition logic operation from before the schematic into rule description to make it clear. 255.Modify Mn.7d, Mn.7e. Add density check step 100um. 256.Modify TM2.10 description window size and step to align with TM1.10. Density check window 200x200 step100. Previous typo window size was 25x25. 257.Delete ALPA.6. Reason: no Al fuse(FUSE area) component defined.

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			258.Add in 7.3.5.1 dummy layer table data type 1 dummy layers. And DUMBA, DUMBp, DUMBm dummy block layers
1T	2011-09-08	MengFeng Tsai	259.Modify TV1.2, TV2.2 rule values from 0.36 to 0.34
1T	2011-09-08	MengFeng Tsai	260.Add TV1.13. Move TV1 note on redundant TV1 to TV1.13. Delete TV1 note
1T	2011-09-08	Jun Zhao	261.Modify DUMC.6, DUMC.16, add MARKG 262.Modify DUMC.18, add MxDUB, DUMBm, MTT2 263.Modify DUMC.20, add MARKG 264.Modify DUMC.22, add VxDUM, MARKG in 265.DUMC.26, MARKG, MTT2 added in. Rule value change from 1.78 to 1.77 266.DUMC.27 added ALDUB 267.DUMC.28 added MARKG 268.DUMC.30, DUMC.34, DUMC.35 added MTT2 269.Delete DUMC.38. Reason: no MIM in 40nm 270.Delete DUMC.39 Reason: follow dummy insertion truth table, MOM area permit dummy insertion, designer has to put dummy block layer if needed.
1T	2011-09-08	MengFeng Tsai	271.7.4.37 EXCLU section, delete INST as DRC block layer for AA-V2. Reason: put SRAM related DRC guide in DR guide section 272.Add section 7.1.3 for SRAM design rule and check method 273.Modify following rules to make description clear: V1.6d, V1.7d, Vn.6d, Vn.7d 274.Modify CT.6 description, add constrain”(if CT touches AA)” 275.Modify CT.7 description, add constrain “(if CT touches GT)” 276.Modify table 7.3.1-3 ESD1 related GDS layer to be only ESD1 to comply with ESD1 as drawn layer rule.
1T	2011-09-08	MengFeng Tsai	277. Modify CT.5. Add 1.0V into the device. 278. Merge 7.1.3 content into 7.1.2 item b. Reason: SRAM check strategy is in design rule applicable scope. 279.Modify DUMC.31. Add AA, GT dummy to be within BORDER constrain.
1T	2011-09-08	Gorton Zhang	280.DUMC.2, DUMC.6, DUMC.12, DUMC.16 description updated to comply with Dummy insertion truth table. DUMC.2: eliminate GTFUSE, add RESP1, RESNW DUMC.6: add MARKG, RESP1, RESNW DUMC.12: eliminate GTFUSE; add RESAA, RESNW DUMC.16: add MARKG, RESAA, RESNW
1T	2011-09-08	MengFeng Tsai	281.Add DIFRES, PLRES into table 7.3.1-2 40LL layer table 282.TV1.3, TV2.3 rule values changed from 0.5 to 0.54 283.V1.4, Vn.4 description add constrain “not touching MOMDMY”
1T	2011-09-08	Gorton Zhang	284. DUMC.2, DUMC.6, DUMC.12, DUMC.16 description updated to comply with Dummy insertion truth table modification. DUMC.2: Add DIFRES, PLRES, HRPDMY into scope DUMC.6: Add DIFRES, PLRES, HRPDMY into scope DUMC.12: Add DIFRES, PLRES, HRPDMY into scope DUMC.16: Add DIFRES, PLRES, HRPDMY into scope 285. Delete DUMC.16a. Reason: DUMC.16 covers DUMC.16a.
1T	2011-09-08	Jun Zhao	286. Modify TV1.3, TV2.3 description. “space between two TV1(TV2) regions” modified to “Minimum space between top vias”
1T	2011-09-08	MengFeng Tsai	287.Modify TV1.3, TV2.3 rule value from 0.54 to 0.5. Reason: process achievable this rule value. 288.Layer tables data type not specified, modify by adding data type 0. Tables modified: table 7.3.1-1. 289.Add BORDER note #3 for BORDER to include the holes within BORDER.

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9.2 Chronicle detail change note for v.2R

Doc. Rev.	Change Date	Author	Change Description
2R	2011-12-19	MengFeng Tsai	<ul style="list-style-type: none"> 1. DUMC.2 add dummy AA not touch AA, del DIFRES part to comply with dummy insertion truth table 2. DUMC.12 remove dummy GT not touch PLRES, HRPDMY. To comply with dummy insertion truth table. 3. Correct typo:Table 7.3.2 40LL Design truth table, two 1.8v IO1 nfet, modify the one linked with SP from “nfet” to “pfet”. 4. Delete RESAA.8(rule about dog bone shape resistor AA). Move the original content to RESAA note. Reason: suggestion rule put to note area. Dog bone shape is not yet well defined in DR. 5. M1.6, M1.6a, M1.6b,M1.6c,Mn.6,Mn.6a,Mn.6b,Mn.6c modify “run length >=” to “run length >” 6. M1.6c, Mn.6c description “with one metal line” change to “with both metal lines” 7. Delete V1.4, Vn.4 max via array width rules. Reason: 2011-9-29 DR committee conclusion. 8. V1.6 description modification: delete “V1 within M1 with width > 0.14μm must meet rule V1.6a or V1.6d” 9. Delete V1.6d. Add V1.6dR. Modify the original content and put to new V1.6dR. The original M1 enclosure V1 part can be covered by V1.6c. This part does not keep. Put the redundant via part into V1.6dR as recommended rule. 10. V1.7 description modification: delete “V1 within M2 with width > 0.14μm must meet rule V1.7a or V1.7d” 11. Delete V1.7d. Add V1.7dR. Modify the original content and put to new V1.7dR. The original M2 enclosure V1 part can be covered by V1.7c. This part does not keep. Put the redundant via part into V1.6dR as recommended rule. 12. Vn.6 description modification: delete “Vn within Mn with width > 0.14μm must meet rule Vn.6a or Vn.6d” 13. Delete Vn.6d. Add Vn.6dR. Modify the original content and put to new Vn.6dR. The original Mn enclosure Vn part can be covered by Vn.6c. This part does not keep. Put the redundant via part into Vn.6dR as recommended rule. 14. Vn.7 description modification: delete “Vn within Mn+1 with width > 0.14μm must meet rule Vn.7a or Vn.7d” 15. Delete Vn.7d. Add Vn.7dR. Modify the original content and put to new Vn.7dR. The original Mn+1 enclosure Vn part can be covered by Vn.7c. This part does not keep. Put the redundant via part into Vn.6dR as recommended rule. 16. DUMC.23 rule value change from 0.07 to 0.077 to meet with dummy insertion
2R	2011-12-19	MengFeng Tsai	<ul style="list-style-type: none"> 17. CT.10 description modification to include the AADUM and GTDUM to be with AA & GT. Waive this rule for LOGO, INDMY(inductor), MOMDMY. Area.
2R	2011-12-19	Mengfeng	<ul style="list-style-type: none"> 18. DUMC.23 modify the rule value from 0.077 to (0.077 OR 0.07) to fit existing different dummy insertion set status. 19. delete DUMCN.5. Reason: found some non-std design dummy AA straddle on NW.

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2R	2011-12-19	MengFeng Tsai	20. Add TCD(91;4), ICOVL(91;5) layer definition in the table 7.3.1-2 40LL layer table. 21. SP.10 removed description one redundant left parenthesis"(“. Typo correction.
2R	2011-12-19	MengFeng Tsai	22. M1.7a description change: “within” changed to “enclosed by”. Rule value changed from 0.015 to 0 um. 23. Add DFM.28 for M1 CT enclosure enhancement. 24. revise rule number index V1.6dR back to V1.6d. Revise the enclose rectangle size from 0.07x0.21 to 0.07x0.27 25. revise rule number index Vn.6dR back to Vn.6d. Revise the enclose rectangle size from 0.07x0.21 to 0.07x0.27
2R	2011-12-19	MengFeng Tsai	26. Delete M1.7. reason:1. content can be covered by M1.7a, M1.7b; 2. reduce the confusion of “at least one” in the description. 27. add HRP section 28. add UTM section 29. separate detail change note for v.2R into new section 9.2
2R	2011-12-19	Linda_Zhuang	30. Delete RESAA.11, which can be deduced from RESAA.5, CT.1 and CT.6 rules 31. Revise RESAA.12 rule value: 0.16um → 0.08um; RESAA.13 rule from 0.24um→0.08um based on process evaluation. 32. Revise TG.3 and DG.3 rules: remove ”include AA area not under poly” to make design run description more clear 33. Delete GT.13 rule since it is a repeat of GT.6 34. Delete SN.20 and SP.20 since they are repeated with SN.12 and SP.12 respectively 35. Add M1.7c M1 and CT enclosure rule for two opposite sides with the other two sides $\geq 0.02\mu m$ and $< 0.25\mu m$ 36. Add back M1.7: at least one CT per (AA or Poly) and M1 intersection area need to meet M1.7a, M1.7b and M1.7c 37. Revise V1.7dR rule number as V1.7d. Revise the enclose rectangle size from 0.07x0.21 to 0.07x0.27 38. Revise Vn.7dR rule number as Vn.7d. Revise the enclose rectangle size from 0.07x0.21 to 0.07x0.27 39. Revise TM1.13 and TM2.12 description to add the comment “TM1/TM2 underneath of MD opening area needs not to follow this rule” 40. Revise PA.1 rule: correct typo error of “minmum” to “minimum”; change PA minimum size (square) from 3um to 2um; 41. Correct PA.3 and PA.4 typo error of “enclosure” to “enclosed” 42. Revise MD.11 rule description: MD(PA2) is prohibited to overlap or touch with PA when PA size $<= 10\mu m$, changed from 10um to 3um 43. Revise DFM28 rule description: M1 enclose CT when M1 width size $\geq 0.12\mu m$ → M1 minimum overlap past CT for the sides with M1 size $\geq 0.12\mu m$; Downgrade DFM28 from Pri. 1 to Pri. 2 rule 44. Revise Section 7.1.2 item a seal ring marker layer of MARKG → MARKS 45. Revise Table 7.3.1-2 and 7.3.3-2 1) seal ring marker layer of MARKG → MARKS; 2) GDS number: 189;0→189;151l; 3) Delete guard ring in the layer description; 46. Revise DUMC.2, DUMC.6, DUMC.12, DUMC.16, DUMC.18, DUMC.20, DUMC.22, DUMC.26, DUMC.27, DUMC.28: seal ring marker layer: MARKG → MARKS

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2R	2011-12-19	MengFeng Tsai	<p>47. Insert SRAM rule section 7.6 *Copy from SRAM rule v.0 DR. Some modifications are to prevent known no process concern alerts *Cell dimension copy from Gorton's draft 2011-12-9. SP374 and DP741 dimension different from v.0 DR *SRAA.1 rule value 0.06 chg to 0.046 to comply with re-chk result *SRPW PW rules deleted: remove generated layers *SRDOP.101 change GT to gate: to prevent edge cell alarm in DP741 *SRGT.1a: delete. The rule value is same as main rule section *SRGT.7 rule value change from 0.072 to 0.07: follow Gorton 12/9 proposal *delete SRGT.13, SRGT.14: main rule section GT.13, GT.14 deleted. *delete SRGT.17: main rule section rule value 0.012 is same as V.0 SRAM DR *delete NC, PC sections: delete generated layers *delete SM section: delete generated layers *SRCT.2 delete: same rule number as CT.2 *SRCT.6aa change rule value from -0.008 to -0.011: follow 12/9 Gorton proposal according to new check result *SRCT.7a change rule value from -0.001 to -0.003: follow 12/9 Gorton proposal according to new check result *remove SRM1.7 from SRCT section: obvious typo *SRCT.102 change rule value from 0.088 to 0.075: follow 12/9 Gorton proposal according to new check result</p> <p>48. M1.6, Mn.6, M1.6a, Mn.6a : “with one or both metal line width is \geq xx μm” change to “with both metal lines width is $>$ xxμm.</p> <p>49. DUMCN.13 rule value changed from Vn.1 to “0.070 or 0.077 or 0.120”</p> <p>50. Delete LVT.3. reason:process concern on LVT to gate space not AA.</p> <p>51. M1.7 change “(AA or poly)” to “((AA not gate) or GT)”. Remove “M1.7a” from M1.7 description.</p> <p>52. PA.1 description delete “(square)”</p> <p>53. Chip corner rule 7.4.40 note.1 check layers add “MTT2”</p> <p>54. PA.4 desciption add MTT2 with TM2</p> <p>55. PA.10 description modification: delete “PA opening landing on TM2(highest top copper metal layer), this”</p> <p>56. PA.10 schematic revised to enhance understanding</p> <p>57. MTT.7 description modified. Remove the dummy MTT related description. Add check window and step follow TM2 rule.</p> <p>58. MTT.10 revise description to a inductor drawn guide. Mark it as non-DRC chk rule.</p> <p>59. HRP.1 square number change from “>5” to “\geq1” to align with model. Change this rule as non-check rule</p> <p>60. Add definition of [NC] (no DRC check) in table 7.3.6.13 DR nomenclature and abbreviation</p> <p>61. HRP.9 modify “S/D and LDD” to “(SN, SP)”</p> <p>62. HRP.12 desc modify “edge space should be 0um” to “should have coincident edge”</p> <p>63. V1.3, Vn.3 description add “For the via spaces fully covered by both under and upper metal, then this rule does not check this space.”</p> <p>64. MTT.11: modify “width” to “line width”. Add description “MTT underneath of MD does not follow this rule”</p> <p>65. CT.1, CT.6, CT.6a, CT.6b, CT.7, CT.7a, CT.7b description modification: not</p>

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			applicable for CT interact with EFUSE(81;2) 66. Delete HVT.3. reason: process concern on HVT to gate space not AA
2R	2011-12-19	MengFeng Tsai	67. Modify Titles, remove “1P10M”. Follow DR meeting requirement. 68. Modify Purpose section description: remove SRAM not included description. Reason: SRAM section is included in this revise. 69. CT.10 modify description “gate and STI” to “(gate or STI)”. Reason: correct the mis-use of “and”. 70. Modify Reference section: remove SRAM DR. Reason: SRAM section is included in this revise. 71. 7.1.1 dummy pattern requirements: add MTT2 in the dummy related layers. 72. 7.1.2 applicable scope item b: revise SRAM rule related description to comply with this version section 7.6 SRAM rule section. Revise “40nm SRAM rule (Doc: TD-LO40-DR-2007)” to “section 7.6 SRAM rules requirements”. Revise “follow this design rule” to “follow this design rule section 7.4 Layout rule description”. 73. GT.2b description modification: not applicable for GT interact with EFUSE(81;2) 74. HRP.9: description add sizing to prevent false alarm. 75. Delete LVT.14 and HVT.14. Reason: already covered by SN/SP pickup enclosure rules
2R	2011-12-19	MengFeng Tsai	76. Add section 7.3.8 on design check flow before tape out 77. Remove SRAA.1. Reason:AA min width in main layout rule is 0.06. The 0.046 rule value is for inner vertex to inner vertex distance. Should remove this rule to prevent confusion. 78. SRAA.1#a modify rule value from 0.055 to 0.046. Reason: to comply with existing SRAM baseline design 79. Table 7.3.6.13 add def of [NC] 80. DFM.26 description add “If this area pass AA density DRC check, this rule can be waived”. Reason:provide waive criterion
2R	2011-12-19	MengFeng Tsai	81. GT.3 modify description: “poly on field” change to “poly on STI .STI here is the area outside of (AA, GT, AADUM, GTDUM).” 82. SAB.11 modify description: “unrelated poly on field oxide.”to”((GT not interact with SAB) on STI). STI here is the area outside of (AA, GT, AADUM, GTDUM).”
2R	2011-12-19	MengFeng Tsai	83. M1.7b correct typo from “with the other two sides $\geq 0\mu m$ and $< 0.20\mu m$ ” to “with the other two sides $\geq 0\mu m$ and $< 0.020\mu m$ ” 84. M1.7c correct typo from “with the other two sides $\geq 0.02\mu m$ and $< 0.25\mu m$ ” to “with the other two sides $\geq 0.02\mu m$ and $< 0.025\mu m$ ”
2R	2011-12-19	Mengfeng Tsai	85. Add into 5.Reference section TD-LO40-DR-2009 40 dummy insertion rule.
2R	2011-12-19	Mengfeng Tsai	86. M1.7b modify “M1 minimum overlap past CT for two opposite sides with the other two sides $\geq 0\mu m$ and $< 0.020\mu m$ ” to “M1 minimum overlap past CT for two opposite sides with the other two sides $\geq 0\mu m$ and $< 0.015\mu m$ ” 87. M1.7c modify “M1 minimum overlap past CT for two opposite sides with the other two sides $\geq 0.02\mu m$ and $< 0.025\mu m$ ” to “M1 minimum overlap past CT for two opposite sides with the other two sides $\geq 0.015\mu m$ and $< 0.025\mu m$ ”. M1.7c rule value changed from 0.02 to 0.015.

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9.3 Chronicle detail change note for v.3R

Doc. Rev.	Change Date	Author	Change Description
3R	2012-01-30	MengFeng Tsai	1. Add section 9.3 for Chronicle detail change for V.3 2. CT.10 description modification: add waive CT on STI for CT straddles STI within INST. Add waive rectangle CT in SRAM
3R	2012-02-03	MengFeng Tsai	3. Modify DUMC.22 description: change "Vx Dummy must not touch (Vx ,VxDUM," to "Vx Dummy must not touch (Vx ,VxDUB," 4. Modify definition of "gate" in 7.3.6.13 nomenclature to cover 3 types of "gate" concerned in the design rules. Add Figure 7.3.6.13-3 for one type of gate
3R	2012-02-22	MengFeng	5. GT.7 head to head space description modification. Add "The head to head with run length > 0." to make meaning clear
3R	2012-03-05	MengFeng	6. Delete DUMC.9 dummy space to DNW. Reason: the rule should be dummy space to PW or dummy within NW.
3R	2012-03-15	MengFeng	7. Delete PSUB note 4. Reason: a. PSUB pick up need SP implant; b. model tk diode_NW_PSUB need SP on PSUB to implement.
3R	2012-03-20	MengFeng	8. Table 7.3.1-3 40LL mask layer and GDS modification: a. table column name "Layer name" change to "Mask Name" 9. Table 7.3.1-3 Mask layer related GDS mofication: AA: del DUMBA, RESNW GT: del DUMB; add OVERDR, SN, AA; del repeated GT in related GDS. Delete mask#146 SDOP related
3R	2012-03-22	MengFeng	10. Delete SRCT.2a. Reason: CT section can cover. 11. Modify 7.6.5 SRAM rule all table head: "SMIC comment" changed to "Description"
3R	2012-03-23	MengFeng	12. Add TV2.13 for redundant TV2
3R	2012-03-26	MengFeng	13. Delete SRSN.7b. Reason: repeat of SRSN.3, delete redundant rule.
3R	2012-03-27	MengFeng	14. Add MARKG Table 7.3.1-2 40LL layers and nomenclature. Reason: as one dummy insertion rule referenced layer. 15. Add section 7.4.44 IO 2.5V gate OX LDMOS design Guidelines 16. 7.4.40 chip corner rule modification: 17. Section purpose description modified. Corner rule only suitable for the chips which need seal ring insertion and before seal ring insertion.
3R	2012-03-28	MengFeng	18. add EXDFM(239;1) rule into 7.4.37 and rename section title from EXCLU rule to "EXCLU, EXDFM rules" 19. add EXDFM(239;1) into Table 7.3.1-2 40LL layers and nomenclature
3R	2012-04-02	Mengfeng	20. Modify GT.3, SAB.11, CT.10 : delete the definition of STI. It will be defined in 7.3.6.13. 21. Define "STI" in nomenclature in 7.3.6.13 nomenclature. Revise the item "Field OX" to "Field OX, STI". The definition changed from "not AA" to "NOT (AA OR AADUM)" 22. Add figure numbers name tag to GT section: Fig.7.4.8-1, Fig. 7.4.8-2 23. Add figure in GT for GT.3, GT.4 clarification: Fig 7.4.8-3 24. Add GT note#3 to exclude the sharp cross of GT or AA in the space rule GT.3, GT.4. 25. Modify GT.5 description to exclude inductor area. 26. Add GT note#4 to clarify GT.6's non-applicable for inductor (INDMY) area. 27. Add figure numbers name tag to AA section: Fig.7.4.1-1, Fig. 7.4.1-2

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			<ul style="list-style-type: none">28. Add figure in AA for AA.4a clarification: Fig 7.4.1-329. Add AA note#1 to exclude the sharp cross of GT or AA in the space rule GT.3, GT.4.30. Add PSUB.3e for native device 1.8V UD 1.5V min L. Rule value: TBD31. Add PSUB.3f for native device 2.5V UD 1.8V min L32. Delete 7.4.44 LDMOS note #2. STI is defined in 7.3.6.13.
3R	2012-04-03	Mengfeng	<ul style="list-style-type: none">33. Move PSUB.3e, 3f from draft to “to do” list after rule value fixed then add on.
3R	2012-04-03	Mengfeng	<ul style="list-style-type: none">34. Add AA resistor DIFRES section 7.4.1.335. Add poly resistor PLRES section 7.4.8.236. Section 7.4.3.1 NW resistor section overall revised to be NW resistor under STI.37. Remove EXDFM from 7.4.3738. Add in 7.4.37 constrain usage of EXCLU: “The use of EXCLU to cover design layout should have written approval from SMIC representative.”39. Modify GT.1e 2.5V OD 3.3V PMOS min channel length from 0.45 to 0.44.40. Modify GT.1a, GT.1b, GT.1c, GT.1d, GT.1e, GT.1f, GT.1g description “minimum length” to “minimum channel length”41. Modify DFM.1 and add DFM.1a to restrict L shape AA to poly space by AA width.42. Modify DFM.2 and add DFM.2a to restrict L shape GT to AA space by AA width43. modify DFM.4: add reference test condition
3R	2012-04-13	Arthur Liu	<ul style="list-style-type: none">44. Modify TG.4 TG.6 DG.4 DG.6 minimum value from 0.35 to 0.2545. Delete CT.6 CT.7 M1.7 restriction “at least one CT”.46. Add CT.6c rule: Minimum CT enclosure by pick-up AA for at least two opposite sites47. Modify M1.8 minimum density value from 20% to 15%; M1.8a Maximum density value from 80% to 85%.48. Modify M1.9 Mn.8 minimum 45 °width from 0.3 to 0.1749. Delete V1.6 “At least one V1” restriction; Delete Vn.6 “At least one Vn” restriction50. Modify TM1.5 TM2.5 minimum space value from 0.6 to 0.551. Modify TM1.13 TM2.12 Maximum line width from 30 to 1252. Modify ALPA.1 minimum width from 4 to 253. Modify ALPA.9 min density from 25% to 10%; Modify ALPA.10 max density from 55% to 70%54. Update DFM.5 rule description to exclude MOM and Inductor device55. Modify Mn.7 rule value from 20% to 15%56. Modify Mn.7a rule value from 80% to 85%
3R	2012-04-16	MengFeng Tsai	<ul style="list-style-type: none">57. Modify CT.6: add in CT.6c with CT.6a, CT.6b.58. Modify CT.6c description to be as a CT.6b’s complementary rule for pickup AA.59. Remove EXDFM(239;1) layer from Table 7.3.1-2 layer table
3R	2012-04-17	MengFeng Tsai	<ul style="list-style-type: none">60. Modify PA.3 rule number from 1 to 0.5
3R	2012-04-17	MengFeng Tsai	<ul style="list-style-type: none">61. Modify LDMOS section fig 7.4.44-1, fig 7.4.44-2 figures to make them clear.62. Modify CT.6, CT.6a, CT.6b, CT.6c description, Add CT.6d. Reason: make the rules complete.63. Modify M1.7b, M1.7c, V1.6b, V1.6c, V1.7b, V1.7c, Vn.6b, Vn.6c, Vn.7b,

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			Vn.7c: “with the other two sides” to “with either side”. Reason: to cover the previous missed ranges.
3R	2012-04-19	MengFeng Tsai	<p>64. Modify CT.7b “when the other two opposite sides” to “when either opposite sides”</p> <p>65. Modify V1.7, Vn.7 description: delete “At least one V1”, “At least one Vn”</p> <p>66. Delete PSUB note#1,2,3,5. Move the related content to add PSUB.10, PSUB.11, PSUB.12, PSUB.13.</p>
3R	2012-04-20	MengFeng Tsai	<p>67. Modify V1.6b, V1.7b description from “with either side $\geq 0.01\mu m$”, to “with either side $\geq 0.01\mu m$, and $< 0.015\mu m$”</p> <p>68. Modify V1.6c, V1.7c description from “with either side $\geq 0\mu m$”, to “with either side $\geq 0\mu m$, and $< 0.01\mu m$”</p> <p>69. Remove DUMBA from DUMC.2, DUMC.6</p> <p>70. Remove DUMBp from DUMC.12, DUMC.16</p> <p>71. Remove DUMBm from DUMC.18, DUMC.26</p> <p>72. Modify AA.4b description for space along S/D, and rule value from 0.11 to 0.1</p> <p>73. Modify AA.4c description for space along gate poly direction, and rule value from 0.1 to 0.11</p>
3R	2012-04-20 for 4/19 mtg	MengFeng Tsai	<p>74. Modify AA.9 rule value from 0.02 to 0.035.</p> <p>75. Modify AA.12 rule value from 50 to 10. Exempt VARMOS</p> <p>76. Delete DNW.5, DNW.6</p> <p>77. Modify PSUB.6 rule value from 0.08 to 0.38</p> <p>78. Modify TG.3 rule value from 0.176 to 0.2</p> <p>79. Modify TG.5 rule value from 0.176 to 0.2</p> <p>80. Modify GT.5 rule value from 0.06 to 0.09</p> <p>81. Modify GT.6 rule value from 0.09 to 0.11</p> <p>82. Modify GT.7 rule value from 0.1 to 0.11</p> <p>83. Modify GT.17 rule value from 0.012 to 0.022</p> <p>84. Modify LVT.6 rule value from 0.16 to 0.18</p> <p>85. Modify LVT.9 rule value from 0.1 to 0.19</p> <p>86. Modify LVT.10 rule value from 0.1 to 0.19</p> <p>87. Modify HVT.6 rule value from 0.16 to 0.18</p> <p>88. Modify HVT.9 rule value from 0.1 to 0.19</p> <p>89. Modify HVT.10 rule value from 0.1 to 0.19</p> <p>90. Modify CT.2a rule value from 0.08 to 0.11</p> <p>91. Modify CT.4 rule value from 0.04 to 0.05</p> <p>92. Modify M1.4 rule value from 0.0196 to 0.055</p> <p>93. Modify M1.5 rule value from 0.078 to 0.2</p> <p>94. Add M1.7e</p> <p>95. Modify M1.7 description for consideration of M1.7e</p> <p>96. Modify M1.10 rule value from 0.15 to 0.17</p> <p>97. Modify V1.5, Vn.5 rule value from 0.09 to 0.11</p> <p>98. Add V1.5a, Vn.5a</p> <p>99. Modify Mn.4 rule value from 0.0196 to 0.027</p> <p>100. Modify Mn.5 rule value from 0.078 to 0.2</p> <p>101. Modify Mn.9 rule value from 0.3 to 0.17</p> <p>102. Modify TV1.4 rule value from 0.01 to 0.02</p> <p>103. Modify TM1.8 rule value from 0.42 to 0.565</p> <p>104. Modify 7.4.25 table’s TV1, TV2 space from 0.36 to 0.34.</p> <p>105. Modify TV2.4 rule value from 0.01 to 0.02</p>

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			106. Modify TM2.8 rule value from 0.42 to 0.565 107. Modify Vn.6b, Vn.7b description from “with either side $\geq 0.01\mu m$ ”, to “with either side $\geq 0.01\mu m$, and $< 0.015\mu m$ ” 108. Modify Vn.6b, Vn.7b description from “with either side $\geq 0\mu m$ ”, to “with either side $\geq 0\mu m$, and $< 0.01\mu m$ ” 109. Modify DG.3 rule value from 0.176 to 0.2 110. Modify DG.5 rule value from 0.176 to 0.2 111. Modify MD.6 description “opening maximum to BORDER” to “opening any edge maximum to BORDER”
3R	2012-04-23	MengFeng Tsai	112. Modify MD.6 description: change “any edge maximum to BORDER” to “whole MD enclosed area maximum space to BORDER”.
3R	2012-04-24	MengFeng Tsai	113. Modify RESAA.2 min SAB AA resistor min width from 0.2 to 0.4. Reason: better model support 114. Modify RESP1.2 min SAB poly resistor min width from 0.15 to 0.4. Reason: better model support
3R	2012-04-25	MengFeng Tsai	115. Modify CT.10 description “(gate or STI)” to “(gate or (STI not GT))” 116. Modify AA.4c rule value from 0.11 to 0.1 117. Modify AA.9 rule value from 0.035 to 0.02 118. Modify AA.12 rule value from 10 to 50 119. modify PSUB.6 from 0.38 to 0.08 120. Modify GT.5 rule value from 0.09 to 0.06 121. Modify GT.6 rule value from 0.11 to 0.09 122. Modify GT.7 rule value from 0.11 to 0.1 123. Modify GT.17rule value from 0.022 to 0.012 124. Modify CT.4 rule value from 0.05 to 0.04 125. Modify M1.4 rule value from 0.055 to 0.0196 126. Modify Vn.5a description “V1” to “Vn” 127. Modify Vn.5a,Vn.5, V1.5, V1.5a description. Add “(outside of SRAM)”. 128. Add V1.5b Vn.5b to specify Vn space different net in SRAM. 129. modify Mn_4 rule value from 0.027 to 0.0196 130. Modify TV1.4 rule value from 0.02 to 0.01 131. modify TV2.4 rule value from 0.02 to 0.01 132. Modify TM1.8, TM2.8 rule value from 0.565 to 0.56 133. Add M1.11a, M1.11b, M1.11cfor line end space. Add related picture in M1 section. 134. Add Mn.10a, Mn.10b, Mn.10c for line end space. Add related picture in Mn section 135. Modify DFM.1, DFM.1a, DFM.2, DFM.2a description
3R	2012-04-26	MengFeng Tsai	136. Add “line end” definition and related picture in 7.3.6.13 DR nomenclatures. Modify the original “line end & line Corner” to “line end extention & line corner” 137. Modify M1.11a “line end to an M1 line(the parallel run length $>0\mu m$) in perpendicular direction” to “line end to an M1 (the parallel run length $>0\mu m$)” 138. Modify M1.11b and M1.11c “M1 line end (with (CT or V1)) to an M1 line (the parallel run length $>0\mu m$) in perpendicular direction” to “M1 line end (with (CT or V1)) to an M1 (the parallel run length $>0\mu m$)” 139. Modify Mn.10a “line end to an Mn line(the parallel run length $>0\mu m$) in perpendicular direction” to “line end to an Mn (the parallel run length $>0\mu m$)” 140. Modify Mn.10b and Mn.10c “Mn line end (with Vn) to an Mn line (the parallel run length $>0\mu m$) in perpendicular direction” to “Mn line end (with Vn) to an

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			Mn (the parallel run length >0um)"
3R	2012-04-30	MengFeng Tsai	141. Modify NW section schematic: correct NW.4 schematic 142. Modify SN, SP section schematic: correct SN.14, SP.14 schematic
3R	2012-05-03	MengFeng Tsai	143. Add V1.5b for V1 different net space not outside SRAM. Reason: missed in last version. Add to meet with DR TF conclusion. Missed in 4/25 modification.
3R	2012-05-08	MengFeng Tsai	144. Modify DUMC.22, add Vx dummy must not touch M _x , M _{x+1} 145. Modify DUMC.18, add Mx dummy must not touch Vx,Vx-1 146. GT.8 rule value correct to 0.1. Previous 5/3 version mistakenly changed it to 0.11. 147. Modify CT.10 description. Add waive EFUSE area. 148. add NW.10 for NW enclosure IO P+AA 149. Revise M1.11b rule value from 0.1 to 0.09 150. Revise M1.11c rule value from 0.12 to 0.1 151. Revise Mn.10a rule value from 0.1 to 0.09 152. Revise Mn.10b rule value from 0.1 to 0.09 153. Revise Mn.10c rule value from 0.12 to 0.1
3R	2012-05-11	MengFeng Tsai	154. DUMC.6: remove DIFRES from AADUM space constrain. Reason: correct previous v.1T typo and align with dummy insertion rule dummy insertion truth table. 155. DUMC.16: remove PLRES from GTDUM space constrain. Reason: correct previous v.1T typo and align with dummy insertion rule dummy insertion truth table. 156. Modify M1.8, Mn.7 metal min density from 15% to 12%. 157. BORDER note #1 modification: delete "This section is only for the designs which designers do not put the seal ring. If designers draw seal ring following design rule, chip edge BORDER layer can be skipped.", add "All designs should place a BORDER at the outset edge with straight lines from chip corner area to corner area.". Delete "Designers must draw border layer if they do not put the seal ring in the design." 158. Add TV2.14 for double TV in only one TM2 with Mn case. 159. Modify TV1.13, change "if Mx width" to "if either TM1 or Mx width" . Reason: complete the spirit of the rule.
3R	2012-05-16	MengFeng Tsai	160. modify table 7.3.1-2 layer tbl "TCD" to "OCCD"(on chip CD), "ICOVL" to "OCOVL"(on chip overlay) 161. Add 7.7.2.1 OCCD content. 162. Add 7.7.2.2 OCOVL content 163. Modify SN.7b to be applicable only for outside of SRAM. The within SRAM part rule is covered by SRSN.3 164. Modify CT.1 desription. Remove the exception of EFUSE description. Move the part to CT.1a 165. Add CT.1a for non-square CT in EFUSE, MARKS, INST 166. Delete SRCT.101. Reason: cannot execute. Thre are many CT interact with STI instances in SRAM bit cell. 167. M1.11a, Mn.10a rule value changed from 0.08 to 0.07 168. M1.11b, Mn.10b rule value changed from 0.09 to 0.07 169. SRM1.4 rule value changed from 0.015 to 0.0168 170. SRMn.4 rule value changed from 0.013 to 0.0192 171. Modify M1.10 description for parallel M1 45 deg.

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3R	2012-05-23	MengFeng Tsai	172. TM1.10, TM2.10 description modification to exclude INDMY /MARG/ MARKS. Change rule value from 30%-80% to 20%-85% 173. GT.9 description and rule value change: changed from NFET gate min space to poly channel length < 0.06, range of gate space to poly and poly dummy 0.12-0.33um 174. GT.10 description and rule value change: change from PFET gate min space to poly channel length >= 0.06, min gate space to poly and poly dummy 0.14um 175. add GT.10a for the accompany poly to gate coverage of channel width at lease 67% 176. change 7.3.6.13 nomenclature “gate” definition: AA2 definition change from “== 2” to “>= 2” 177. AA.14 description and rule number change: change to fit for outside of DG or TG. Rule value changed from 25%-75% to 25%-80% 178. Add AA.14a for inside DG or TG pattern density 25%-90% 179. GT.20 description add “(full chip)”, rule value changed from 15-35% to 15-40%. 180. GT.20b rule value changed from 15-35% to 15-40%. 181. delete GT.16. Reason: use GT.20 to cover max GT density rule. 182. add GT.20c for core 25x25um tile min density 10% 183. add GT.20d for IO 25x25um tile min density 5%
3R	2012-05-24	MengFeng Tsai	184. GT.10 rule value changed from 0.14 to 0.13. Reason: to comply with previous version DR min gate space 0.13 185. GT.3 description change: remove STI. Reason: make GT min space rule cover both STI and AA. 186. Add M1.7f for large M1 with small adjacent M1, the M1-CT enclosure 187. Delete M1.11c. Reason: use M1.12 to cover the line end to other M1 space 188. Add M1.12 for M1 line end’s V1 to neighboring M1 line min space 189. Delete Mn.10c. Reason: use Mn.11 to cover the line end to other Mn space 190. Add Mn.11 for Mn line end’s Vn to neighboring Mn line min space
3R	2012-05-25	MengFeng Tsai	191. Modify M1.7f description and rule value from (M1 enclose CT) to (CT to M1 space) Add M1.7f related schematic. Reason: correct the way of description to meet meeting conclusion 192. Add M1.12, Mn.11 related schematics in M1 and Mn sections. 193. Merge GT.10a to GT.9. Change “gate for GT.9 or GT.10)” to “gate for (GT.9). Reason: GT.10 does not define max gate and poly spce, only GT.9 defines. 194. Add schematic for GT.9, GT.10
3R	2012-05-25	MengFeng Tsai	195. M1.7f description change to not applicable for SRAM. Reason: prevent non-necessary alert. 196. GT.9 description modification: remove “not allow more than one piece of polys” 197. Delete AA.C.5. Reason: present dummy insertion related rules can cover..
3R	2012-05-30	MengFeng Tsai	198. Modify GT.9 description. GT.9 not applicable for SRAM area 199. M1.7f fixed rule value to 0.14 200. GT.20c, GT.20d description modification “TD” changed to “TG”. Reason: correct typo 201. PSUB note#8 description modification: change “note#3” to “PSUB.12”. Reason: the original note#3 now moved to PSUB.12. 202. PLRES.3 unit changed from “square” to “”. Reason: more suitable

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			203. M1.7 description modification: change “(M1.7a and (M1.7b or M1.7c)) and M1.7e” to “((M1.7a and (M1.7b or M1.7c)) and M1.7e) and M1.7f”
3R	2012-05-31	MengFeng Tsai	204. M1.7 description change “((M1.7a and (M1.7b or M1.7c)) and M1.7e) and M1.7f” to “(M1.7a and (M1.7b or M1.7c)) and M1.7e” 205. Re-number M1.7f to M1.13 and related pictures rule item number 206. Modify M1.13 description: add waive condition that the redundant CT can fulfill M1.13 CT to M1 space requirements
3R	2012-06-04	MengFeng Tsai	207. AA.12 description: change “width” to “channel width”. Change “Exempt AA under VARMOS” to “Waive transistor inside VARMOS”. Reason: make meaning more clear
3R	2012-06-5	MengFeng Tsai	208. Add OCCD, OCOVL GDS in 8.Attachment section 209. Modify Table 7.3.1-3 40LL mask layer & GDS: delete NWHT item. Reason: mask set delete it. 210. Correct typo of repeat V1.5b between V1.6d and V1.7. Delete the redundant V1.5b. 211. Correct typo of Vn.5a, change “not outside of SRAM” to “(outside of SRAM)”.
3R	2012-06-6	MengFeng Tsai	212. M1.13 rule number add test condition 0.085 213. MD.11 rule description modification: change “PA size <= 3um” to “PA size < 3um”. Reason: to fit with process capability.
3R	2012-06-7	MengFeng Tsai	214. Delete M1.12. Reason: M1 space rule do not need to consider V1. M1 line end already considered in M1.11b, M1.11c. 215. Modify Mn.11 Vn to Vn _{n-1} . Reason: correct typo.
3R	2012-06-11	MengFeng Tsai	216. Modify Mn.11 “Mn[A] and M _{n-1} intersection” to “Mn[A] and M _{n-1} intersection”
3R	2012-06-12	MengFeng Tsai	217. Add layers into layer map table 7.3.5.1 dummy layer map table: RFDEV(181;0), VnRM & VnRB(n=1-7), TVnRM & TVnRB(n=1-2)
3R	2012-06-14	MengFeng Tsai	218. Add BORDER.4 rule with content moved from BORDER Note#1: “All designs should place a BORDER at the most outermost edge with straight lines from chip corner area to corner area.”. Reason: to prevent BORDER drawing making dummy insertion insufficient at chip edge.
3R	2012-06-15	MengFeng Tsai	219. Modify M1.8b,Mn.7b, TM1.12, TM2.11 max density difference rule value from 40 to 50%. Reason: to comply with process capability.
3R	2012-06-18	MengFeng Tsai	220. table 7.3.1-1 40LL layer HPBL description modification: change “to block” to “for”. Reason: to make meaning clear. 221. Table 7.3.2 40LL Design truth table modifications to correct typo: DP466 PD add on CT layer; add DNW “x” to DP466 PU, RF600 PU, DP589 PU, Q299S PU, Q303 HP PU; Q303 LP PU; DP466 PU add NW mark; all N+, P+ poly resistor silicide/non-silicide NW part mark “x” as optional. 222. GT.22 modify description: add exclude floating GT. Reason: prevent non-necessary alert
3R	2012-06-19	MengFeng Tsai	223. Add in 7.7.2.1 OCCD insertion related guide items: OCCD.5 added other structure explanation
3R	2012-06-21	MengFeng Tsai	224. Modify OCCD.5 other structure definition: del NW,BORDER. Add constrain not straddle on NW. 225. Vn.11-Vn.15, V1.11-V1.15 deleted rules re-arrange table to have better look 226. Add V1.16,Vn.16: redundant V1,Vn for width >0.24. Add related schematics. 227. Add V1.17, Vn.17: redundant V1,Vn connection for adjacent 0.12um of

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			0.24x0.24um plate. Add related schematics.
3R	2012-06-26	MengFeng Tsai	<p>228. Table 7.3.1-3 40LL mask-GDS table NW mask GDS add LDBK. Reason: according to LOTA ver. J change</p> <p>229. Table 7.3.1-3 40LL mask-GDS table PLHT, PLH mask's "PCAP" GDS change to "NCAP". Reason: correct typo</p> <p>230. make table 7.3.1-4 GDS to mask layer relation table complete</p>
3R	2012-06-27	MengFeng Tsai	<p>231. fig 7.4.8-3 GT.4 part notation modify the angle from "The angle is smaller or equal to 90 deg" to "The angle A <> 0 is not applicable for GT.4".</p> <p>232. SN.6 schematic modification to make it match with rule meaning.</p> <p>233. SP.6 schematic modification to make it match with rule meaning.</p>
3R	2012-06-28	MengFeng Tsai	234. Modify OCCD.5: add (DUMBA, DUMB) layers as other structure to keep off. Reason: follow dummy insertion blockage strategy.
3R	2012-06-29	MengFeng Tsai	<p>235. Add 7.7.3 Redundant via insertion guide</p> <p>236. Modify OCCD.3 description: clarify window percentage meaning.</p> <p>237. Add OCCD.6 for DRC waive OCCD items</p> <p>238. DUMC.26 rule value changed from 1.77 to 0.6. Description change remove TMx's MTT2 part. Reason: comply with dummy insertion update</p> <p>239. Add DUMC.26a for MTT2 dummy space to MTT2 and other structures</p>
3R	2012-07-03	MengFeng	240. Modify OCCD.2 description to state window size smaller than 1x1 mm^2 no insertion.
3R	2012-07-04	Howard Gan	241. add CDR.11, CDR.12 for poly silicide and non-silicide max current
3R	2012-07-05	MengFeng	242. V1.16, V1.17, Vn.16, Vn.17 description change: waive the non-square V1, Vn
3R	2012-07-05	Arthur Liu	<p>243. Modify 7.6.1 description to correct grammar error of plural and singular</p> <p>244. modify 7.6.2 description, add LL and HP related bit cell names.</p> <p>245. Modify 7.6.5.1 SRAM AA rules:</p> <p>SRAA.1#a rule item name change to SRAA.1sa.</p> <p>SRAA.1sa chg base rule value. Add each bit cell min values.</p> <p>Delete SRAA.4 Reason: no AA.4</p> <p>Modify SRAA.4a description to comply with main rule. Rule value changed from 0.064 to 0.065</p> <p>Delete SRAA.4b Reason: SRAM area can meet AA.4b</p> <p>Modify SRAA.4c description to be same as AA.4c. Add each bit cell related min values.</p> <p>Add in SRAA.5, SRAA.6 each cell related min values.</p> <p>SRAA6#a rule item name change to SRAA.6sa</p> <p>SRAA.6sa base rule value change to NA. Fill in each cell's min value.</p> <p>ARAA.7: Fill in each cell's min value.</p> <p>Delete SRAA.9. Reason: AA.9 can cover</p> <p>246. Modify 7.6.5.2 SRAM NW rules</p> <p>SRNW.1: fill in each cell's min values. Modify rule value from 0.268 to 0.27. Reason: after bit cell review.</p> <p>Delete SRNW.3. Reason: all bit cells can meet NW.3</p> <p>247. Modify 7.6.5.3 SRAM PG marker SDOP</p> <p>SRDOP.102 modify each cell min value. Rule value changed from 0.182 to 0.18. Reason: comply with bit cell geometry.</p> <p>SRDOP.103 modify each cell min value. Rule value changed from 0.09 to 0.1. Reason: comply with bit cell geometry.</p> <p>SRDOP.104 delete "is" from description. Reason: grammar correction</p>

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			<p>Add SRDOP.105</p> <p>248. Modify 7.6.5.4 SRAM GT</p> <p>SRGT.3 fill in each cell min value. Rule value changed from 0.064 to 0.07. Reason: bit cell review result.</p> <p>SRGT.4 fill in each cell min value. Rule value changed from 0.01 to 0. Reason: comply with bit cell geometry.</p> <p>SRGT.5: delete. Reason: SRAM all function gates comply with GT.5</p> <p>SRGT.6: fill in each cell min value. Rule value changed from 0.042 to 0.055 Reason: comply with bit cell geometry.</p> <p>SRGT.7: modify description to align with GT.7. Fill in each bit cell's min values.</p> <p>SRGT.8: delete. GT.8 can cover</p> <p>SRGT.9: delete. GT.9 can cover</p> <p>SRGT.10: base rule value change to 0.13 to comply with GT.10. fill in each cell's min value. Change rule value from 0.118 to 0.12. Reason: comply with bit cell dimension</p> <p>Delete SRGT.21, SRGT.101, SRGT.103. Reason: comply with main rule sections.</p> <p>249. Modify 7.6.5.5 SRAM SN</p> <p>Delete SRSN.1, SRSN.2, SRSN.3#a, SRSN.6, SRSN.7a, SRSN.22#a. Reason: main rule can cover.</p> <p>Modify SRSN.3 item name to SRSN.3a</p> <p>SRSN.3a description modify to align with SN.3a. Each cell fill in min values.</p> <p>Add SRSN.3b</p> <p>SRSN.4: fill in each cell's min value</p> <p>SRSN.10 description modification to align with SN.10. Fill in each cell's min value. Rule value changed from 0.04 to 0.041. Reason: after cell review.</p> <p>SRSN.10#a rule item name changed to SRSN.10sa</p> <p>SRSN.10sa: fill in each cell's min values.</p> <p>SRSN.16: fill in each cell's min values. Rule value changed from 0.08232 to 0.0323. Reason: after bit cell review.</p> <p>SRSN.18 fill in each cell's min values.</p> <p>250. Modify 7.6.5.6 SRAM SP</p> <p>SRSP.1 delete. Reason: SRAM bit comply with SP.1</p> <p>SRSP.2 delete. Reason: SRAM bit comply with SP.2</p> <p>SRSP.3 revise rule item name to SRSP.3a</p> <p>SRSP.3a revise description to align with SP.3a, add bit cell min value, revise rule value from 0.04 to 0.041. Reason: after bit cell review</p> <p>Add SRSP.3b</p> <p>SRSP.3#a delete. Reason: replaced by new SRSP.3a, SRSP.3b</p> <p>SRSP.6 delete. Reason: SRAM bit comply with SP.6</p> <p>SRSP.7a, SRSP.7b, SRSP.7ba delete. Reason: bit cell can meet main rule</p> <p>SRSP.10 modify description to comply with SP.1. Fill in cell's min values. Rule value changed from 0.04 to 0.038.</p> <p>SRSP.12 fill in each cell's min value</p> <p>SRSP.15#a delete. Reason: SRAM do not have SP partial overlap AA</p> <p>SRSP.20 delete. Reason: bit cell can meet SP.20</p> <p>SRSP.16 fill in bit cell min values. Rule value changed from 0.0728 to 0.072. Reason: after layout review.</p>

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			<p>SRSP.19 delete. Reason: SP.19 was deleted.</p> <p>251. Modify 7.6.5.7 SRAM CT Delete SRCT.3, SRCT.6aa, SRCT.7a, SRCT.10, SRCT.18, SRCT.105. Reason: can comply with main rule, and no need to special define.</p> <p>252. Modify 7.6.5.8 SRAM rectangle contact Modify “60nun*160nm” to “60nm*160nm”. Correct typo “SRAN” to “SRAM”</p> <p>SRRCT.104 delete. Reason: CT to CT space can cover SRRCT.104c modify description “touching” to “inside”. Fill in each cell min values. Rule value changed from 0.068 to 0.07. Reason: after bit cell review result</p> <p>SRRCT.106 modify bit cell min value. Change rule value from 0.073 to 0.133. Reason: after bit cell review result</p> <p>SRRCT.106a modify bit cell min value. Reason: after bit cell review result</p> <p>SRRCT.107 modify bit cell min value. Change rule value from 0.036 to 0.037. Reason: after bit cell review result</p> <p>SRRCT.107a modify bit cell min value. Change rule value from 0.059 to 0.082. Reason: after bit cell review result</p> <p>SRRCT.108 modify bit cell min value. Change rule value from 0.055 to 0.057. Reason: after bit cell review result</p> <p>253. Modify 7.6.5.9 SRAM M1 SRM1.3#a rule item name changed to SRM1.3sa SRM1.3sa description change from “vertex distance” to “vertex min distance”. Fill in cell’s min values.</p> <p>SRM1.4 fill in each cell min value.</p> <p>SRM1.7a fill in each cell min value. Correct base rule number. Change rule number from 0.008 to 0. Reason: result of bit cell review</p> <p>SRM1.7b description modification to align with M1.7b. Fill in each cell’s min value.</p> <p>254. Modify 7.6.5.10 SRAM V1 SRV1.6a Fill in each cell min value</p> <p>SRV1.6c Fill in each cell min value, change rule value from 0.005 to 0.015. Reason: after bit cell review</p> <p>SRV1.7 delete. Reason: after bit cell review</p> <p>255. Modify 7.6.5.11 SRAM M2 Add note wording “Mn here is M2”</p> <p>SRMn.3: delete. Reason: follow main rule</p> <p>SRMn.4 fill in each cell’s min value</p> <p>256. Modify 7.6.5.12 SRAM V2 Add note wording “Vn here is V2”</p> <p>SRVn.6a fill in each cell’s min value. Rule value changed from 0.005 to 0.</p> <p>SRVn.6c delete. Reason: use Vn.6c</p> <p>257. Add section 7.6.5.13 SRAM device dimension check rules</p> <p>258. Add section 7.6.5.14 SRAM marker layer check rules</p> <p>259. Add NW resistor definition before 7.4.3.1 NW resistor under STI</p> <p>260. Add 7.4.3.2 NW resistor on AA rules</p>
3R	2012-07-09	MengFeng	261. Add OCCD.6, OCOVL.5 for DRC waive items
			262. Revise Table 7.7.1-1 GDS and mask relation through dummy interaction
3R	2012-07-10	Mealie Zhang	263. Add 7.7.4 BEOL dummy metal & Via insertion method selection guideline.

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3R	2012-07-11	MengFeng	264. Modify 7.7.4 dummy metal & via insertion guide descriptions. Reason: wording perfection 265. Reorganize 7.6.5.13 SRAM device to 7.6.6 SRAM marker section. 7.6.5.14 to 7.6.7. Reason: DR structure more reasonable 266. HRP.8 change to [NC]. Reason: a guide rule and cannot execute script check. 267. SRDOP.105 description modification: "must enclose gate" change to "minimum enclose gate". Reason: enhance the meaning. 268. Delete 7.4.37 EXCLU rule section. Reason: follow DR mtg conclusion. 269. Delete EXCLU from Table 7.3.1-2 40LL layer tbl, 7.3.3-2 40G layer tbl. 270. RESNWAA.6 description modification: "SAB and related NW" change to "SAB beyond related NW". Reason: to make meaning clear
3R	2012-07-12	MengFeng	271. Mn.10a, Mn.10b, Mn.11 description modification: waive SRAM area
3R	2012-07-16	MengFeng	272. Add AA.15 for 45 deg AA width. Reason: mask making concern 273. Add AA.16 for 45 deg space parallel AA Reason: mask making concern 274. Add AA.17 for u-shape notch AA min space. Reason: OPC pattern concern 275. Add GT.3c for wider GT min space. Reason: litho process PR aspect ratio concern. 276. Add GT.29 for GT line end to GT rule. Reason: OPC line end sizing concern and have 0.01 larger GT to GT space. 277. Add GT.2b_test1 for GT.2b test rule number 0.04. Reason: GT litho have BARC, no concern of STI dishing impact to litho 278. Add GT.2b_test2 for GT.2b test rule number 0.06. Reason: for extreme STI dish case, may need GT PR with 20nm larger min CD. 279. M1.13 description modification: eliminate extrusion E consideration. Rule number change from 0.14 to 0.085 280. Add M1.14 and related schematic for narrow width M1 line end to M1 rule. Reason: OPC consideration the need of more sizing room at the narrow width line end.
3R	2012-07-17	MengFeng	281. V1.17 description D value changed from 1.2 to 1.1um. Reason: According to QA result 282. V1.16, V1.17 description modification: add exclusion of seal ring 283. Add Mn.12 and related schematic for narrow width Mn line end to Mn rule. Reason: OPC consideration the need of more sizing room at the narrow width line end. 284. Mn.11 rule value change from 0.14 to 0.12. Description add metal line end side distance Ds < 0.08. width <0.1 Change E<=0.08 to E < 0.05. Add line end check operation parameters E1. Reason: OPC consideration the need of more sizing room at the narrow width line end for line end side distance to other metal very small case. 285. Add Mn.11_test1 for test Ds = 0.07. 286. Mn.10b description change "extend Q" to "extend E". 287. Add AA.4d AA to AA min space inside DG or TG Reason: consideration of IO AA's isolation 288. AA.14 description modification. Add waive NWRES, LOGO, seal ring 289. Add AA.18 AA to be covered by (SN or SP) 290. Add NW.11 for N+AA at PW corner space to NW. Reason: consideration of corner double side isolation effect of wells two time of one side. Double the one side space rule

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			<p>291. Add NW.12 for P+AA enclose at NW corner. Reason: consideration of corner double side isolation effect of wells two time of one side. Double the one side enclosure rule</p> <p>292. Add GT.6a for near L shape AA, GT extension out of AA</p> <p>293. Add CT.19 to recommend redundant CT</p> <p>294. Add SP.7c, SP.8c for N+AA space to PMOS gate on the same AA. Reason: consider cross diffusion effect of butted pickup</p> <p>295. Add SN.7c, SN.8c for P+AA space to NMOS gate on the same AA. Consider cross diffusion effect of butted pickup</p> <p>296. M1.2 description modification: waive seal ring max width</p> <p>297. Mn.2 description modification: waive seal ring max width</p>
3R	2012-07-19	MengFeng	<p>298. SN.1 description modification. Delete the INST related. Change “parallel side to side width” to with run length >0”. Reason: SRAM run length > 0 can pass. “run length > 0” to prevent no concern alerts.</p> <p>299. SP.1 description modification. Delete the INST related. Reason: SRAM part run length >0 can pass “run length > 0” to prevent no concern alerts</p> <p>300. LDMOS section fig 7.4.44-1 P LDMOS schematic add DNW. Reason: comply with model tk design</p> <p>301. Add E fuse rule section 7.4.44</p> <p>302. Add 7.4.39.2 AC current density Irms</p> <p>303. SRM1.7a, SRM1.7b description wording change: “share contact” to “rectangle CT”</p> <p>304. GT.20c, GT.20d AA density check window change from “25x25 step 12.5” to “100x100 step 50”. Reason: DR meeting conclusion</p> <p>305. Add section 7.7.5 Antenna ratio effect rules</p> <p>306. M1.8, M1.8a., Mn.7, Mn.7a density rule check window change from 25x25 step12.5 to 110x110um step55um. Reason: reduce non-necessary alert within process capability</p> <p>307. Add DFM.29 for redundant via. Reason: process, yield concern.</p>
3R	2012-07-20	MengFeng	<p>308. 7.7.5 Antena section changes: Reason: correct rule’s layer RDV to PA translation error.</p> <p>a) Rule item name change:</p> <ul style="list-style-type: none">i. ANT.AL.1 to ANT.PA.1ii. ANT.AL.2 TO ANT.PA.2iii. ANT.AL.3 TO ANT.AL.1iv. ANT.AL.4 to ANT.AL.2v. ANT.AL.5 to ANT.PA.3vi. ANT.AL.6 to ANT.AL.3 <p>b) ANT.PA.1, ANT.PA.2, ANT.PA.3 description “ALPA” change to “PA”</p> <p>309. 7.7.5 Antena section add note#1 to specify the ALPA thickness 14.5k and 28k selection for DRC execution</p> <p>310. Mn.7d, Mn.7e rule value changed from 56% to 70%. Reason: process compatibility review result</p> <p>311. CT.19 :rule item add [R], description change “Suggest” to “Recommend”</p> <p>312. Add definition of “[R]” in 7.3.6.13 abbreviation table.</p>
3R	2012-07-20	Charles Yin	<p>313. Follow the general template to update all the design rules tables, add column “operation” and “Unit”. Change all “um” to “μm”.</p> <p>314. Add 7.1.2, 7.1.3, 7.1.4. sections</p> <p>315. 7.1.5.1 40LL mask layer mapping table update: 1) Generated layer delete GDS No/data type to avoid customer drawing pattern by mistake. 2) Delete</p>

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			<p>NWHT (Mask ID: 495) layer and SDOP mask ID due to process change. 3)</p> <p>Add MTT2/MTT2DM, MTT2DB and delete 7.3.5.2 Mix signal related layer map table, reason: match 40LL top tier and delete duplicated content.</p> <p>316. Delete RFDEV from original 7.3.5.1 table and rename as 7.2.3.1.</p> <p>317. Follow general template to update original 7.3.7 to 7.1.7 metal options table.</p> <p>318. Change 7.3.3 to 7.1.5.2 40G mask layer mapping table and merge 40G CAD layers with 40LL</p> <p>319. Add CAPBP, VARJUN, ALPAR, DUPMK1, RFDEV, RESP3T, SUBD, RESCKT, PLDMK in 7.1.6 CAD layers mapping table.</p> <p>320. Update original 7.3.7 section, rename to 7.1.7 metallization options table.</p> <p>321. AA.9 delete “Floating AA is defined as AA that has no CT above it”, reason: it has been defined.</p> <p>322. AA.16: change “45 degree AA to AA parallel min space” to “45 degree AA space to parallel AA”</p> <p>323. Delete 7.4.1.2 section.</p> <p>324. RESAA.6, PLRES.6: delete “minimum distance” in rule description.</p> <p>325. Change PSUB.3a~3d rule description: “enclosure” to “enclosed”.</p> <p>326. Merge PSUB.5a and PSUB.5b to PSUB.5.</p> <p>327. Change Border rule Note.1 before the rule table as description.</p> <p>328. GT.28 change to: The space between two parallel Bent 45 deg GT.</p> <p>329. Delete 7.4.3.2, 7.4.8.1 section note.</p> <p>330. Change RESP1.8 to [NC] rule.</p> <p>331. LVT.6, HVT.6: Space between LVT to (poly and AA SAB) resistor to “Space between LVT to (poly SAB resistor or AA SAB resistor)</p> <p>332. 7.4.25 table: change all “Feature” to “Width”, change TV1/TV2 pitch from 0.720 to 0.700.</p> <p>333. Change M1.8 Mn.7 rule value from 12% to10%, reason: follow meeting conclusion.</p> <p>334. Delete “exclude/waive Sear ring (MARKS)” in CT.1a, M1.2, V1.16, V1.17, Mn.2, Reason: 7.1.4 has defined to exclude MARKS area.</p> <p>335. Delete V1.6d/V1.7d, Vn.6d, Vn.7d.</p> <p>336. TM1.10 rule description: 30% -->20% to match rule value relaxation.</p> <p>337. 7.4.43 : Change all “MTT” in section to “MTT2”.</p> <p>338. EFU.10[NC]: change Dummy GT(no CT) to dummy floating GT.</p> <p>339. SRGT.6: change “share CT” to “rectangle CT”.</p> <p>340. 7.6.5.11: delete “Mn in this section is M2” and change “SRMn.*” to “SRM2”.</p> <p>341. 7.6.5.12: delete “Vn in this section is V2” and change “SRVn.*” to “SRV2”</p>
3R	2012-07-23	MengFeng	<p>342. 7.1.8 Nomenclature definition, “Line end” definition add consideration of extrusion.</p> <p>343. NW.11, NW.12 description revised to make meaning clear.</p> <p>344. GT.8a description and illustration modified. Reason: to make meaning clear.</p> <p>345. M1.13 description modification: “stand on M1[A]” change to “in M1[A]”. Reason: correct grammar issue.</p> <p>346. M1.14 description and illustration modified. Reason: to make meaning clear.</p> <p>347. Mn.11 description change, Vn-1 to line end space description modified to make meaning clear. Change “N=2-7” to “N=2-8” to correct typo.</p> <p>348. Mn.12 description and illustration modified. Reason: to make meaning clear.</p> <p>349. OCOVL.5 waive rule item modification. Reason: fit with actual waive list.</p> <p>350. Vn.3, V1.3, TV1.3, TV2.3 description modification: “An array does not have both row and column greater than 3” change to “An array does not have both</p>

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			row and column greater or equal than 3”
3R	2012-07-26	Charles Yin	<p>351. Update NW.11 and NW.12</p> <p>352. Update GT.8a.</p> <p>353. Update SN.8c, SP.8c rule description and schematic map.</p> <p>354. Update SN.7a, SN.7c, SP.7a, SP.7c schematic map.</p> <p>355. Update M1.14, Mn.11 and Mn.12.</p> <p>356. Delete SN.8a, SN.8b, SP.8a, SP.8b. Reason: follow meeting conclusion.</p> <p>357. Update M1.6a/6b/6c, Mn.6a/6b/6c metal space rules,. reason: reflect process capability to reduce DRC violations.</p> <p>358. Relax TM1.6/7, TM2.6/7, reason: same as above.</p> <p>359. Modify V1.16, V1.17, Vn.16, Vn.17 via space from “<=0.14” to “<0.16”. Reason: follow meeting conclusion.</p> <p>360. Update DUMC20, DUMC.21 rule value from 0.22 to 0.6. Reason: Timing concern.</p> <p>361. MD.4, MD.6 are changed to recommended rules.</p> <p>362. Antenna ratio guideline and LDMOS guideline add the superscript of [G].</p>
3R	2012-07-27	Charles Yin	<p>363. ANT.MN.3^[G], ANT.MN.4^[G],ANT.VN.3^[G]: delete “with area larger than 0.054um²”.</p> <p>364. ANT.VN.3 add “single via layer”.</p> <p>365. Add 7.1.3 layout requirement to forbid non 45C acute angle patterns.</p> <p>366. Rename AA.15~AA.18 to AA.16~AA.19, and delete “HRPDMY area”, reason: AA.15 already exist; AA.19: HRPDMY has no AA pattern.</p> <p>367. Optimize CT.11 wording to avoid misunderstanding. “CT overlap AA with 0 SN/SP space is forbidden” to “It is not allowed that (CT not outside AA) touches or straddles on (SN or SP) edge”.</p> <p>368. Change original 7.3.6 to 7.1.11.</p> <p>369. Follow DR Committee meeting conclusion to delete “1P10M” in title, Change Tech. Dev version to 1.0.</p> <p>370. Modify DFM.3 rule description follow GT.6.</p> <p>371. Modify DFM.4.</p> <p>372. Modify DFM.8 rule description follow GT.1a.</p> <p>373. Modify DFM.9 rule description follow GT.5.</p> <p>374. Delete DFM.11 rule referenced DR GT.13.</p> <p>375. Modify DFM.13 rule description follow CT.3.</p> <p>376. Modify DFM.15 rule description follow CT.5.</p> <p>377. Modify DFM.20 rule description follow M1.6.</p> <p>378. Modify DFM.21 rule description and rule value follow V1.5.</p> <p>379. Modify DFM.24 rule description follow Mn.6.</p> <p>380. Modify DFM.25 rule description and rule value follow Vn.5.</p> <p>381. Delete DFM.27 rule.</p> <p>382. Update DFM.29 to exclude SRAM region</p>
3R	2012-07-29	Charles Yin	<p>383. Add BUMP(168;0)in 7.1.6 CAD layer map table.</p> <p>384. Add 7.7.9 bump flip chip design guideline.</p> <p>385. Add SRCT.2a, rule value 0.088.</p> <p>386. Add SRGT.5, rule value 0.045.</p> <p>387. GT.8: Exclude SRAM area to check.</p> <p>388. SRRCT.106: Add restriction “with run length>0”: Reason: based on SMIC SRAM bitcell GDS QA result.</p> <p>389. Add SRM2_3, rule value change from 0.06 to 0.065..</p>

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			<p>390. V1.5, Vn.5 change rule value from 0.11 to 0.10. Reason: QA result and process capability verification OK.</p> <p>391. Add ULVT(159;152) in 7.1.6.1 layer mapping table.</p> <p>392. Add section 7.4.45 ULVT design rules.</p> <p>393. Delete OCCD sample figure. Reason: prevent misleading user.</p> <p>394. Delete OCOVL sample figures. Replace with new sample figure.</p> <p>395. Delete OCOVL.4. Reason: no need for only one OCOVL structure..</p> <p>396. Change OCOVL.5 rule item name to OCOVL.4</p> <p>397. OCOVL.2 add limitation on small insertion remain area no OCOVL insertion</p> <p>398. Merge seal ring rule content as section 7.4.46 and add seal ring GDS into 8.Attachment list.</p> <p>399. Delete reference document: Antenna ratio effect guideline and seal ring. Reason: they have been merged into main DR.</p> <p>400. Add CDR.3a for MTT2.</p>
3R	2012-07-31	Charles Yin	<p>401. Change 7.7.5 Antenna ratio effect from guideline to rule 7.4.46. Reason: follow meeting conclusion to change.</p> <p>402. DFM.1, DFM.2 add “waive DRC violations in SRAM area”, reason: SRAM QA.</p> <p>403. Restore section 7.1.4.2.(AA.C.5 is deleted.)</p> <p>404. GT.20c, AA.14: change “outside” to “excluding”; GT.20d, AA.14a: change “inside” to “in”. Reason: avoid miss detecting some violations across the IO boundary.</p> <p>405. GT.22: Add warning message: Fail to comply with silicide poly may have up to 10% Rs difference between with and without (SN or SP) implant.</p> <p>406. Rename AA.5~AA.8 to NW.13~NW.16, reason: merge all NW enclosure /space rules from AA into NW section.</p> <p>407. Update poly Efuse schematic map.</p> <p>408. V1.5a change rule value to 0.09, merge V1.5b as V1 space in different net.</p> <p>409. Vn.5a, Vn.5b merge as Vn.5a: Vn space in different net.</p> <p>410. Delete TM1.6, TM2.6, reason: reduce DRC violations and reflect process capability.</p> <p>411. Add dummy insertion device table in 7.4.38 dummy check rule. Reason: remind customer to draw dummy block layers to avoid dummy pattern insertion.</p> <p>412. V1.3, Vn.3 modification: only request Vn space 0.09 for at least two sides, same array space definition change from 0.11 to 0.10um, delete “For the via spaces fully covered by both under and upper metal, this rule does not check this space.” Reason: reflect process capability.</p> <p>413. Add BUMP.7[G].</p> <p>414. MD.6 wording optimization: “whole MD enclosed area maximum space to BORDER” to “MD edge space to Border”.</p> <p>415. Add “outside” and “not outside” definition in 7.1.11.8.</p> <p>416. AA.4b, AA.4c change “AA to AA overlap(run length)” to “AA to AA run length”, reason: follow general template.</p> <p>417. RESNW.10~RESNW.14 rename to RESNW.9~RESNW.13 and update related schematic map.</p> <p>418. CT.19^[R]: clear define the resistor type in the rule description.</p> <p>419. Update SP.8c and SN.8c schematic map.</p> <p>420. Update V1.17, Vn.17 schematic map.</p> <p>421. Add back AA.C.5.</p>

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			422. Add M1.8d, Mn.7f, TM1.10a, TM2.10, MTT2.7a, MTT2.7b for INDMY area density check. Reason: process limitation. 423. Change GT.2b to recommended rule and relax rule value from 0.07 to 0.06. 424. AA.18, V1.16, Vn.16 add “exclude SRAM area to check”. 425. Delete DFM.11, reason: the rule can be covered by GT.6a. 426. Add “enclosure”, “Extension” definition in 7.1.11.6. 427. Change DMUC.20 rule description: when Mx dummy not touching INDMY. 428. Add DUMC.21a rule value from 0.6 to 0.53, reason: Match dummy insertion rule 1MDUM.3c.
3R	2012-08-13	MengFeng Tsai	429. Add PSUB.3e for 2.5V UD 1.8V native transistor min channel length. 430. Add GT.1h for 1.8V UD 1.5V N/P MOS transistors min channel length 431. Modify GT.6a schematic. Reason: make the definition clear
3R	2012-08-14	MengFeng Tsai	432. M1.14 schematic extension 1 & 2 condition change from “interact with” to “overlap with”. Reason: align with QA result. 433. Mn.12 schematic extension 1 & 2 condition change from “interact with” to “overlap with”. Reason: align with QA result
3R	2012-08-23	MengFeng Tsai	434. Add waive description for NW resistor on AA for rules: AA.11: add waive the AA interact with RESNW AA.19: modify waive (RESNW AND AA) to waive (AA interact RESNW) NW.13: add in description “Waive ((AA interact RESNW) and SN)” RESNWAA.8: description add “inside (AA interact RESNW)” SN.10: add “Waive for (AA interact RESNW)” SN.12: add “Waive for (AA interact RESNW)” 435. GT.3c rule value changed from 0.155 to 0.15. Reason: Loose rule after OPC confirm
3R	2012-08-24	MengFeng Tsai	436. GT.20d description modification to re-check the within IO area highlighted part GT density. Reason: reduce non-necessary alert. 437. NW.11, NW.12 rule check method change: reduce the edge check length to 0.08um. Revise related schematic to describe the check method.
3R	2012-08-28	MengFeng Tsai	438. M1.14 description correct typo: “Waive extrusion E < 0.07” changed to “Waive extrusion F < 0.07”. To align rule and schematic.
3R	2012-08-29	MengFeng Tsai	439. ANT.VN.3 modify description: remove single via layer, only for cumulative via area. Reason: correct typo 440. Table 7.1.9.1 40LL design truth table: add 2.5V OD 3.3V zero Vt, and 2.5V UD 1.8V zero Vt devices Reason: correct missed item. 441. DUMC.18 description modification: remove MxDUB. Reason: prevent alarm after designer add dummy block after dummy insertion. 442. DUMC.22 description modification: remove VxDUB. Reason: prevent alarm after designer add dummy block after dummy insertion. 443. DUMC.27 description modification: remove ALDUB,DUMBMB. Reason: prevent alarm after designer add dummy block after dummy insertion.
3R	2012-08-31	MengFeng Tsai	444. Mn.11 description modification: add S _h , S _s . Reason: optimize description to make it clear. 445. Mn.11 schematic diagram modification. Reason: enhance rule explanation 446. Mn.12, M1.14 schematic label “extension” spelling error corrected
3R	2012-09-03	MengFeng Tsai	447. Remove ALRDL(83;3) from layer table 7.1.7. Reason: prevent confusing 448. Revise TG.11 rule description to be like GT.5’s except this rule applies to within TG. Reason: rule description optimization 449. Revise RESAA.9 description. Remove “No LDD should be implanted into

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			<p>to AA resistor.”. Reason: LDD is generated layer, no description in DR other place for LDD generation method.</p> <p>450. SP.20a description modification: change “AA butted p-well” to “P+ butted AA in P-well”. Reason: make description clear</p> <p>451. SP.21 description modification: change “AA butted n-well” to “N+ butted AA in NW”. Reason: make description clear</p> <p>452. SP.21a description modification: change “AA butted n-well” to “N+ butted AA in NW”. Reason: make description clear</p> <p>453. SN.20a description modification: change “AA butted n-well” to “N+ butted AA in NW”. Reason: make description clear</p> <p>454. SN.21 description modification: change “AA butted p-well” to “P+ butted AA in P-well”. Reason: make description clear</p> <p>455. SN.21a description modification: change “AA butted p-well” to “P+ butted AA in P-well”. Reason: make description clear</p> <p>456. Add 7.1.9 design truth table name “Table 7.1.9.1 40LL Design truth table”</p> <p>457. Add Table 7.1.9.2 Inductor, MOM device truth table</p> <p>458. Add 7.7.10 inductor layout guideline</p> <p>459. Add 7.7.11 MOM layout guideline</p> <p>460. Add 7.7.9 BJT device layout guideline</p>
3R	2012-09-06	MengFeng Tsai	<p>461. TM1.7 description modification: change “> 1.5 μm parallel metal” to “> 4.5 μm parallel metal” Reason: product verified</p> <p>462. GT.20c description modification to re-check the within non-IO area highlighted part GT density. Reason: reduce non-necessary alert</p> <p>463. AA.14 description modification to re-check the within non-IO area highlighted part GT density. Reason: reduce non-necessary alert</p> <p>464. AA.14a description modification to re-check the within IO area highlighted part GT density. Reason: reduce non-necessary alert</p>
3R	2012-09-10	MengFeng Tsai	<p>465. 7.4.41 ESD1 drawing rule prologue modification: to fit the merge of ESD separated DR merged into DR.</p> <p>466. Add ESD.9, ESD.9a for CT enclosure by ESD1 rules</p> <p>467. Add 7.7.5 ESD layout guidelines</p> <p>468. Add 7.7.6 Latch up prevention layout guidelines</p> <p>469. Add 7.7.12 DUP pad guidelines</p> <p>470. CT.19 add area constrain for sufficient large area to hold redundant CT. Reason: prevent non-necessary alert.</p> <p>471. Schematic for BORDER.4 optimized to make it clear.</p>
3R	2012-09-11	MengFeng Tsai	<p>472. DFM.1, DFM.2 priority change from 1 to 2. Reason: process improvemed.</p> <p>473. Add Table 7.1.9.3 HRP design truth table</p> <p>474. Remove MIM, MOM components from Table 7.1.9.1 design truth table</p> <p>475. V1.16, V1.17, Vn.16, Vn.17 redundant via space change from <0.16 to <= 0.16. Reason: process capable.</p> <p>476. Table 7.2.3.2 dummy layer map: delete AADOP, GTDOP</p> <p>477. 7.1.6.1 40LL mask making layer map: delete P2, MIM, IDT.</p> <p>478. GT.6a changed to be recommended rule. Reason: process variation robustness concern. Normally ok.</p> <p>479. AA.C.5 description change: add constrain of GT in gate width <= 0.06. Change “poly on AA” to “GT in gate” to address functional gate. Reason: follow GT.2b consideration to prevent non-necessary alert.</p> <p>480. DUMC.35 rule value change from 1.77 to 0.6um. Reason: dummy insertion rule change</p>

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3R	2012-09-12	MengFeng Tsai	481. BUMP.3 description modification: add max width advice. Reason: no fixed max BUMP width in BUMP rules. 482. 7.7.8 BUMP guide prolog: add assumption of BUMP layout shape to be octagon. Reason: prevent ambiguous. 483. 7.4.3.1 NW resistor under STI rules whole section change: layout style change to align PCM tk. Reason: to have better simulation accuracy 484. Add Table 7.1.9.4, 7.1.9.5 design truth table of LDMOS, ULVT
3R	2012-09-13	MengFeng Tsai	485. Mn.12 description modification: change "to other M1" to "to other Mn". Reason: correct typo. 486. TM2.7 description modification: change "> 1.5 μm parallel metal" to "> 4.5 μm parallel metal" Reason: product verified
3R	2012-09-14	MengFeng Tsai	487. GT.6 description modification: add "waive LDMOS". Reason: SMIC LDMOS GT overlap STI between gate and pickup smaller than this rule. 488. DFM.3 description modification: add "exclude LDMOS". Reason: SMIC LDMOS GT overlap STI between gate and pickup smaller than this rule. 489. DFM.29 description modification: remove V1.16 and Vn.16 from SRAM area waive list. Reason: V1.16, Vn.16 already waive SRAM area 490. Remove the GT.1a item from 7.4.9 LVT section. Reason: correct edit error. 491. RESNWST.4 description modification: change "CT space" to "The nearest CT space". Reason: make rule meaning clear. 492. RESNWST.6 description modification: add DRC check method with 2 AA edges touching. Reason: make clear. 493. RESNWST.9 description modification: NW in pickup AA description method change. Reason: make description clear. 494. RESP1.9 description change: remove "no LDD" parts. Reason: LDD layers are generated. 495. SP.20a description modification: "areas" change to "area". Reason: correct typo. 496. SP.20a, SP.21a, SN.20a, SN.21a description change: "contact area" change to "area(the area interact with CT)". Reason: make meaning clear 497. change rule item name SRAA.5 to SRNW.13, SRAA.6 to SRNW.14, SRAA.7 to SRNW.15. Reason: AA.5-8 renamed to NW.13-16 498. BORDER.4 description adds BORDER shape between with seal ring and without seal ring chip. Reason: make rule clear 499. AA.C.5 description change: "GT in gate" to "gate", "GT width" to "gate channel length" 500. Mn.9 description modification: add constrain of parallel Mn. Reason: prevent non-necessary alert. 501. AA.14, AA.14a, GT.20c, GT.20d description modification: waive if the highlight area smaller or equal than 25% of check window. Reason: prevent non-necessary highlight 502. Add AA resistor definition in 7.4.1.1 AA resistor section prolog 503. RESAA.1 change to [NC]. Reason: same as AA resistor definition 504. GT.22 description: add definition of HRP resistor. Reason: make clear 505. 7.4.8.1 poly resistor: add poly resistor definition. Reason: make clear. 506. LVT.6, HVT.6 description: make poly & AA SAB resistor definition clear 507. SP.3a, SN.3a, SP.3b, SN.3b, SP.9, SN.9, SP.14, SN.14 description modification: make AA & GT resistor def clear. 508. SAB.14 description modification: make resistor def clear. 509. 7.4.42 HRP resistor prolog: add HRP, resistor definitions

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			510. Add RESAA.14. Reason: define RESAA edge align with SAB on AA 511. Add RESP1.15. Reason: define RESP1 edge align with SAB on AA
3R	2012-09-14	Powa Yang	512. Revise 7.7.12 DUP section
3R	2012-09-17	MengFeng Tsai	513. Re-org 7.1.8 metal option tbl: separate the too large table into 2 tpls to fit in page.
3R	2012-09-18	MengFeng Tsai	514. V1.16, V1.17, Vn.16, Vn.17 add redundant via condition “or three V1s with space <= 0.65um”, “or three Vns with space <= 0.65um”. Reason: process capable.
3R	2012-09-19	MengFeng Tsai	515. Add DNW.7 for N+AA and DNW space 516. M1.13 description modification: remove the redundant CT meet M1.13 constraint. 517. M1.14 schematic check method modified. Description DRC check method add “Highlight if the schematic extension 1-3 all touch other M1.”. Reason: process permit loose. → 9/20 further update
3R	2012-09-20	MengFeng Tsai	518. M1.14 description modification: updated DRC check method. Reason: according to OPC suggestion 519. AA.18 description modification: add jog definition 0.03. Schematic add this definition Reason: after OPC suggestion. 520. V1.17, Vn.17 remove space constrain of redundant vias. Add waive SRAM area. The related schematic updated. 521. GT.22 description change: waive HRP region definition change from (HRPDMY and GT) to (HRP and GT). Reason: prevent non-necessary alert 522. Delete TD-LO40-DR-2005 from 5. reference, reason: merged as 7.7.5/6. 523. Update 8. attachment: update seal ring sample GDS, reason: DUMBA/DUMBp mark layer change, to align with DUMBm. 524. Add OCCD/OCOVl GDS sample in 8.attachment.
			525. Rename GR.1~GR.6 to GRC.1~GRC.6, reason: to distinguish with seal ring checking rule with insertion rules GR.1~GR.38. 526. M1.13 relax: R>=0.27 → R>0.27, and M1[A] width change from “>=0.11” to “>0.12um”. Reason: process capable. 527. MD.1 rule value modify from 2 to 1, reason: process capability verified. 528. M1.14: add waive condition for CT/V1 in the intersection, reason: actual process verified. 529. Mn.12: Waive for MOM. Reason: reduce unnecessary DRC alert. 530. Add OTPMK1in CAD table. Reason: for some special use after SMIC approval.