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7.3 INST marker layer design rules

INST is a drawn layer and used to define SRAM edge.

Rule number	Description	Opt.	Design Value	Unit
INST.S.1	Space between INST in S/D direction when PRL > -0.144um	\geq	0.21	um
INST.S.2	Space between INST in GATE poly direction when PRL > -0.21um	\geq	0.144	um
INST.S.3	(purposely blank)			
INST.S.4	(purposely blank)			
INST.S.5	Space between ALL_AA and INST in S/D direction when PRL > -0.24um (ALL_AA CUT INST is not allowed)	\geq	0.25	um
INST.S.5.1	Space between ALL_AA and INST in GATE poly direction when PRL > -0.25um (ALL_AA CUT INST is not allowed)	\geq	0.24	um
INST.S.6	Space between NW and INST (NW cut INST is not allowed)	\geq	0.365	um
INST.S.7	Space between SVT_N and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.8	Space between SVT_P and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.9	Space between LVT_N and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.10	Space between LVT_P and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.11	Space between ULVT_N and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.12	Space between ULVT_P and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.13a	Space between HVT_N and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.13b	Space between HVT_P and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.14a	Space between LFN_N and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.14b	Space between LFN_P and INST (space = 0um is allowed)	\geq	0.21	um
INST.S.15	Space between ALL_GT and INST (ALL_GT cut INST is not allowed)	\geq	0.118	um

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Rule number	Description	Opt.	Design Value	Unit
INST.S.16	Space between ALL_P2 and INST (ALL_P2 cut INST is not allowed) in S/D direction	\geq	0.09	um
INST.S.16a	Space between ALL_P2 and INST (ALL_P2 cut INST is not allowed) in GATE poly direction	\geq	0.15	um
INST.S.17	Space between SN and INST (space = 0 um is allowed) DRC flag opposite region.	\geq	0.21	um
INST.S.17a	Space between SN edge (inside INST) and SN edge (outside INST)	\geq	0.25	um
INST.S.18	Space between SP and INST (space = 0 um is allowed) DRC flag opposite region.	\geq	0.21	um
INST.S.18a	Space between SP edge (inside INST) and SP edge (outside INST)	\geq	0.25	um
INST.S.20	Space between ALL_M0 and INST (ALL_M0 cut INST is not allowed)	\geq	0.136	um
INST.S.22	Space between ALL_M0C and INST (ALL_M0C cut INST is not allowed)	\geq	0.18	um
INST.S.23	Space between ALL_M0G and INST (ALL_M0G cut INST is not allowed)	\geq	0.085	um
INST.S.26	Space between V0 and INST (V0 cut INST is not allowed)	\geq	0.084	um
INST.S.27	Space between RV0 and INST (RV0 CUT INST is not allowed)	\geq	0.084	um
INST.S.28	Space between ALL_M1 and INST	\geq	0.081	um
INST.EN.1	INST enclosure by CHIPB (INST cut CHIPB is not allowed)	\geq	0.5	um
INST.R.1	INST overlap (SVT_N or SVT_P or HVT_N or HVT_P or LVT_N or LVT_P or ULVT_N or ULVT_P or LFN_N or LFN_P) is not allowed.			

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7.4 DUP (Device Under Pad) for Wire bond pad structure design rules

DUPMK1 (89;156) is the marking layer for wire bond pad. The following wire bond pad rules should be followed to provide good mechanical integrity. Any violation including structure or rules, may induce yield or reliability problem during testing and assembly.

Wire bond pad definition:

- 1.(DUPMK1 AND (MD interact DUPMK1)).
- 2.(((MD not interact DUPMK1) sd 17.2um) su 17.2um)

Rule number	Description	Opt.	Design Value	Unit
WBPAD.1	DUPMK1 is must for wire bond pad region.			
WBPAD.2	DUPMK1 width DRC waive the 3um jog violation for each side.	≥	35	um
WBPAD.3	MD must be fully enclosed by DUPMK1.	≥	0	um
WBPAD.4	In wire bond pad area, MD must interact with PA. (MD AND PA) width DRC waive the 3um jog violation for each side.	≥	35	um
WBPAD.5	Wire bond pad design should include one layer of solid ALPA and two layers of solid Cu metal (TM and TM-1). It is not allowed to draw metal slot for ALPA, TM and TM-1 in wire bond pad area. For example: For two thick top metal case: TM2 and TM1 should be solid. For one thick top metal case: TM2 and M7 should be solid.			
WBPAD.6	Wire bond pad design must have dense TV between TM and TM-1. The TV density under wire bond pad. DRC check the (wire bond pad sd 1um) area where density ratio = (TV area)/(wire bond pad area), with window size 10umx10um, step 5um.	≥	10%	
WBPAD.7	TV-1 pattern must be outside of wire bond pad area. For example: For two thick top metal case: TV1 must outside of wire bond pad area. For one thick top metal case: V6 must outside of wire bond pad area.			
WBPAD.8	ALPA, TM, TM-1 should fully enclose wire bond pad area	≥	1	um
WBPAD.9^[R]	MD/ALPA/PA/TM/TM-1 patterns in wire bond pad area should have	≥	2	um

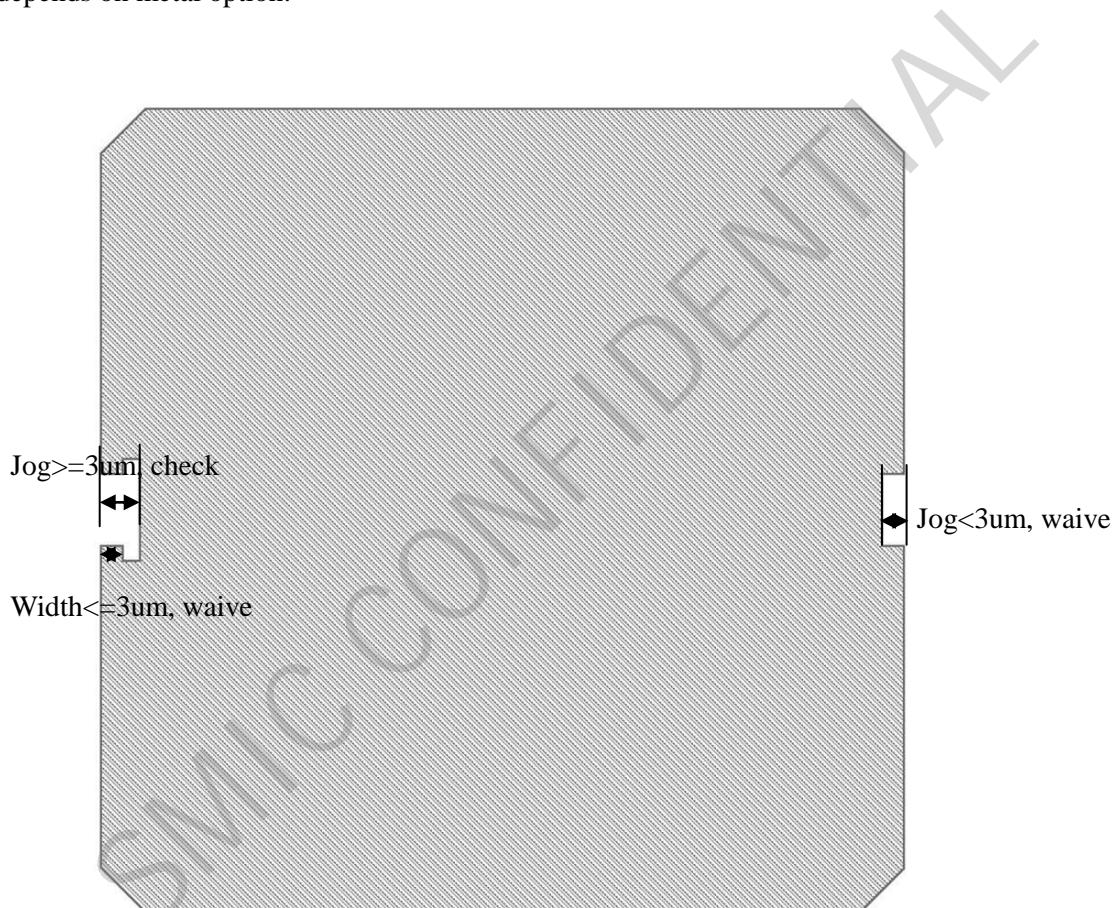
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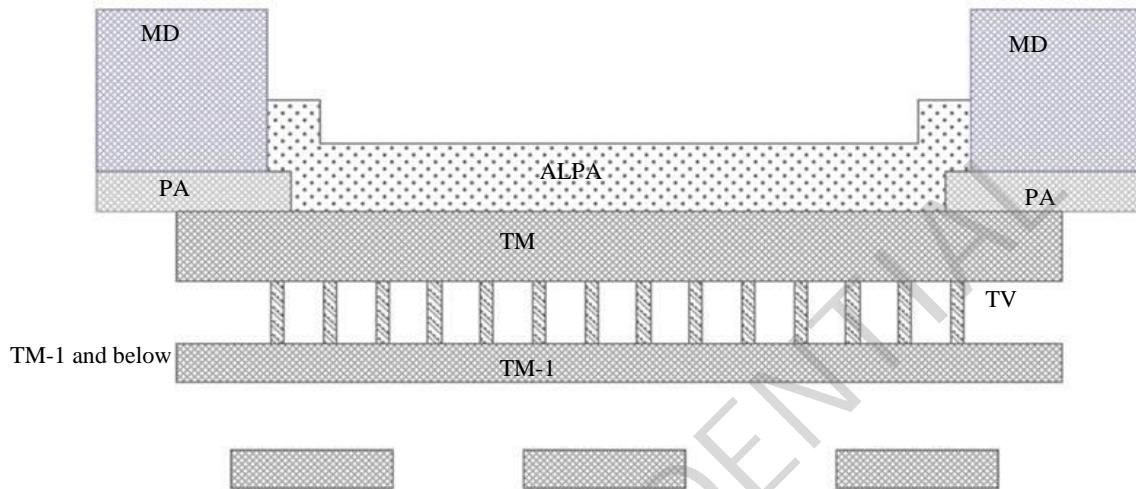
	4 corners with 45 °cut for corner stress relief. The length of corner cut	≤	5	um
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Note:

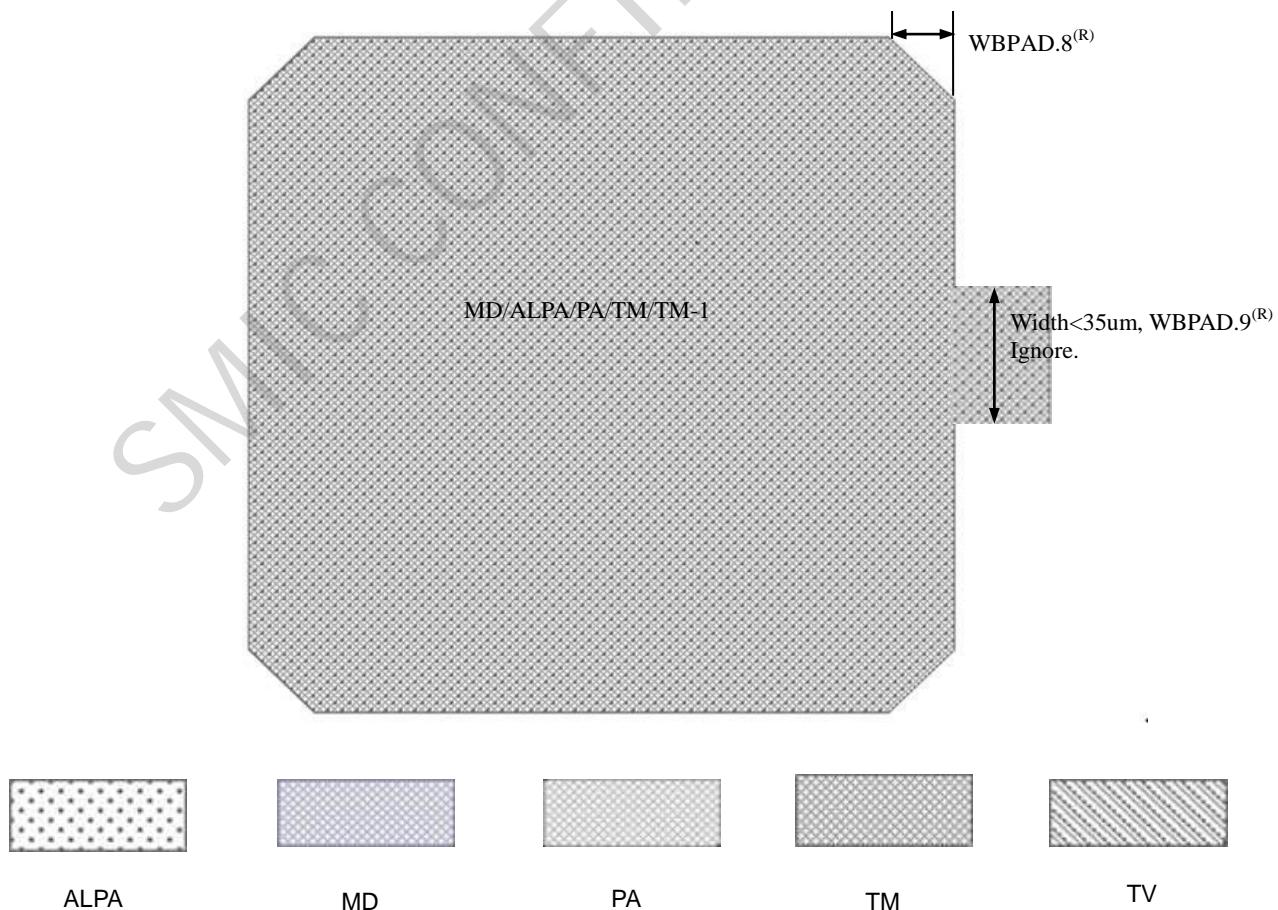
1. TM is TM2 and UTM, TM-1 is the metal layer put under TM. It may be TM1, or Mn inter-metal, which depends on metal option.



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Above is Wire Bond Pad Structure Schematic Diagram



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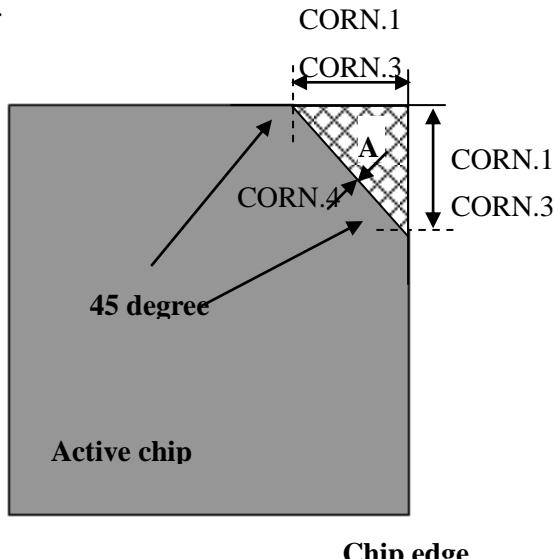
7.5 Chip corner design rules

This section describes the chip corner requirements to prevent the chip design interferes with seal ring.

Rule number	Description	Opt.	Design Value	Unit
CORN.1	NODMF is dummy block layer for chip corner chamfer area A, and must fully cover chamfer area A.			
CORN.2	Chamfer area A size at the chip corner.	=	66.6	um
CORN.3	Chamfer area A size must be same as NODMF size.			
CORN.4^[NC]	Chip corner should have 4 chamfer corners with 45 degree cut for those chips that need insert seal ring.			
CORN.5	The layers (listed in Note1) should not overlap with chamfer area A.			

Notes:

1. The CORN.5 DRC checking layers: AA ,AADMP, AR, NW, PSUB, SVT_N, SVT_P, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, GT, GTDMP, P2, P2DMP, SN, SP, M0, M0DMP, M0G, M0GDMP, M0C, M0CDMP, DIR, DIRDMP, V0, M1, Vy, Mxy, 1.25xMy, 1.25xVn, 1.25xMn, 2xVn, 2xMn, 10xTVn, 10xTMn, 14xTVn, 14xTMn, UTV, UTM, PA, ALPA, MD, MIM, CTOP.
2. This rule section only applies for those chips that need have seal ring insertion. The chip corner rule check option is default turned on in DRC script.
3. In case for the building block/IP level design or the chip level design with seal ring already inserted, please turn off the chip corner rule check option.



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7.6 Chip boundary CHIPB design rules

CHIPB is a drawn layer and used to define chip edge, designers must draw CHIPB layer following CHIPB design rules, $0.048*n$ um, $n \geq 0$ and n is an integer.

Rule number	Description	Opt.	Design Value	Unit
CHIPB.W.1	CHIPB width in GATE poly direction	=	1.056+0.096*n	um
CHIPB.EN.1	CHIPB enclosure of (CELLB OR DMCB1) in GATE poly direction (Cut is not allowed)	=	0.384+0.048*n	um
CHIPB.EN.2	CHIPB enclosure of OCCDFH in GATE poly direction	=	0.048*n	um
CHIPB.EN.3	CHIPB must enclose all chip layout patterns (all chip design, excluding MARKS, NODMF marking layer) if seal ring is inserted by SMIC. DRC waive if the chip has been added seal ring by designer. DRC check layers: AA ,AADMP, AR, NW, PSUB, SVT_N, SVT_P, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, GT, GTDMP, P2, P2DMP, SN, SP, M0, M0DMP, M0G, M0GDMP, M0C, M0CDMP, DIR, DIRDMP, V0, M1, Vy, Mxy, 1.25xMy, 1.25xVn, 1.25xMn, 2xVn, 2xMn, 10xTVn, 10xTMn, 14xTVn, 14xTMn, UTV, UTM, PA, ALPA, MD, MIM, CTOP. DRC only check AA and AADMP enclosure in S/D direction.	\geq	0.45	um
CHIPB.EN.4	CHIPB enclosure of ALL_AA in GATE poly direction, except INST region	=	0.528+0.048*n	um
CHIPB.EN.5	CHIPB enclosure of FIN in GATE poly direction, except INST region	=	0.019+0.048*n	um
CHIPB.EN.6	CHIPB enclosure of DNW if seal ring is inserted by SMIC.	\geq	3	um
CHIPB.EN.7	CHIPB enclosure of MD if seal ring is inserted by SMIC	\geq	3	um
CHIPB.EN.8	CHIPB enclosure of seal ring outer ring outline edge (except seal ring corner stress relief area) if seal ring is inserted by designers.	\geq	0.7	um
CHIPB.R.1	CELLB must be fully covered by CHIPB.			
CHIPB.R.1a	CHIPB layer (GDS No: 127;3) must be drawn.			

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Rule number	Description	Opt.	Design Value	Unit
CHIPB.R.2	CHIPB must be rectangular and orthogonal to grid.			
CHIPB.R.3	Only one CHIPB is allowed in a chip.			
CHIPB.R.4	CHIPB edge must be on an integer multiple of 0.010um.			
CHIPB.R.5^[NC]	CHIPB size should be exactly same as chip window size in Layout Design Database Information (LDDI) form when tape-out.			
CHIPB.R.6^[NC]	CHIPB layer size should be exactly same with the seal ring window edge if seal ring is inserted by designers.			

Notes:

1. The DRC executes this section rule check on following layers: AA, AADMP, AR, DNW, NW, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, DG, GT, GTDMP, P2, SN, SP, P4, M0, M0DMP, M0C, M0G, M0GDMP, V0, M1, Mxy, Vy, 1.25xMy, 1.25xVn, 1.25xMn, 10xTMn, 10xTVn, 14TMn, 14xTVn, UTM, UTV, PA, ALPA and MD.

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7.7 LOGO design rules

LOGO(26;0) is the DRC marker layer for LOGO purpose pattern, such as Product label, words, logos, and other marks that are not part of the circuit. All the LOGO patterns must be fully covered by LOGO(26;0) marking layer.

1. Please use rectangular polygons to write LOGO pattern.

2. Please don't use minimum rule for LOGO pattern.

For the minimum width and space are less than 1um rules, please use greater, or equal 1um of width and space to draw LOGO patterns.

If the minimum rule value is greater than 1um, please follow the minimum rule at least.

3. Please use AADMP to draw the LOGO pattern.

Rule number	Description	Opt.	Design Value	Unit
LOGO.1	Space between LOGO and (AA/GT/M1/Mxy/1.25xMy/1.25xMn/10xTMn/14xTMn /UTM/ALPA OUTSIDE LOGO), except OCCD, OCOVL, WTPMK region	\geq	9.0	um
LOGO.2	Metal width in LOGO region.	\geq	0.106	um
LOGO.3	Space between two metals in LOGO region.	\geq	0.106	um
LOGO.4^[NC]	A circuit in the LOGO region is not allowed.			

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7.8 Passive device layout rules

7.8.1 HR resistor design rules

Rule number	Description	Opt.	Design Value	Unit
HR.W.1	DIR width	=	0.12-1.8	um
HR.W.2	DIRDMP width	=	0.192-1.8	um
HR.W.3	GTDMF width in S/D direction	=	0.086	um
HR.S.1	Space between (DIR OR DIRDMP) (DIR overlap with DIRDMP is not allowed)	\geq	0.192	um
HR.S.1.1	Space between (DIR OR DIRDMP) at length direction when PRL \geq 0um	\geq	0.192	um
HR.S.2	Space between (DIR OR DIRDMP) and (M0G OR M0) (Overlap is not allowed, except M0G (Width = 0.06um) INTERACT DIR)	\geq	0.345	um
HR.S.3	Space between (DIR OR DIRDMP) and (M0G INTERACT DIR) with width = 0.06um. (M0G overlap with DIRDMP, DIR overlap with M0GDMP is not allowed)	\geq	0.178	um
HR.S.4	Space between (DIR OR DIRDMP) and (M0GDMP OR M0DMP) (Overlap is not allowed, except DIRDMP space to M0GDMP)	\geq	0.11	um
HR.S.6.1	Space between DIR and AOP_AA (Overlap is not allowed).	\geq	0.113	um
HR.S.6.2	Space between DIRDMP and AOP_AA (Overlap is not allowed).	\geq	0.078	um
HR.S.7.1	Space between DIR and AOP_GT (Overlap is not allowed).	\geq	0.07	um
HR.S.7.2	Space between DIRDMP and GT (Overlap is not allowed).	\geq	0.07	um
HR.S.8	Space between RESP1 and AOP_AA (Overlap with AA, cut with AADMP is not allowed).	\geq	0.065	um
HR.S.9	Space between DIRDMP and GTDMF (overlap is not allowed).	\geq	0.035	um
HR.S.10	Space between DIR and RESP1	\geq	0.257	um
HR.EX.1	M0G (width = 0.06um) extension of DIR in DIR width direction at both sides (extension \leq 0um is not allowed)	=	0.014	um

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Rule number	Description	Opt.	Design Value	Unit
HR.EX.2	DIR extension of M0G (width = 0.06um) in DIR length direction (extension \leq 0um is not allowed)	\geq	0.063	um
HR.EN.1	RESP1 enclosure of ((AADMP OR DIRDMP) OR DIR)	\geq	0.065	um
HR.EN.1a	RESP1 enclosure of DIRDMP	\leq	0.36	um
HR.L.1	Length of DIR or DIRDMP	\geq	0.61	um
HR.L.1.1	Length of high R resistor (DIR AND RESP2)	\geq	0.36	um
HR.L.2	Maximum length of high R resistor (DIR AND RESP2)	\leq	25	um
HR.A.1	Area of DIR or DIRDMP	\geq	0.092	um
HR.R.1	Square number (length/width) of high R resistor must be ≥ 1			
HR.R.2	DIRDMP must be placed 2-side beside high R resistor RESP2/RESP1 must interact two DIRDMPs within 2.3um in HR resistor width direction.			
HR.R.3	DIR, DIRDMP, and RESP2 (INTERACT DIR) must be 3 rectangle orthogonal to grid respectively.			
HR.R.4	DIR resistor can only use M0G (width = 0.06um).			
HR.R.5	RESP2 must abut with M0G edge, RESP2 must interact at least two DIRDMP.			
HR.R.6	RESP2 intersecting DIR or DIRDMP must form two or more DIRs or DIRDMPs .			
HR.R.7	DIR must be covered by RESP1, and must be uni-direction in the same RESP1.			
HR.R.8	RESP1 and RESP2 must INTERACT DIR.			
HR.R.9	M0G (INTERACT DIR) INTERACT GT is not allowed.			
HR.R.10	Maximum delta V $\geq 5.6V$ is not allowed, when: 1. Space between two DIR/DIRDMP is $< 1.6\mu m$ 2. Space between DIR/DIRDMP and (AOP_M0G OR (M0 NOT M0C)) is $< 3.6\mu m$ 3. Space between DIR and AOP_GT is $< 0.42\mu m$ 4. DIR space to (AOP_GT NOT P2) is $< 0.72\mu m$			

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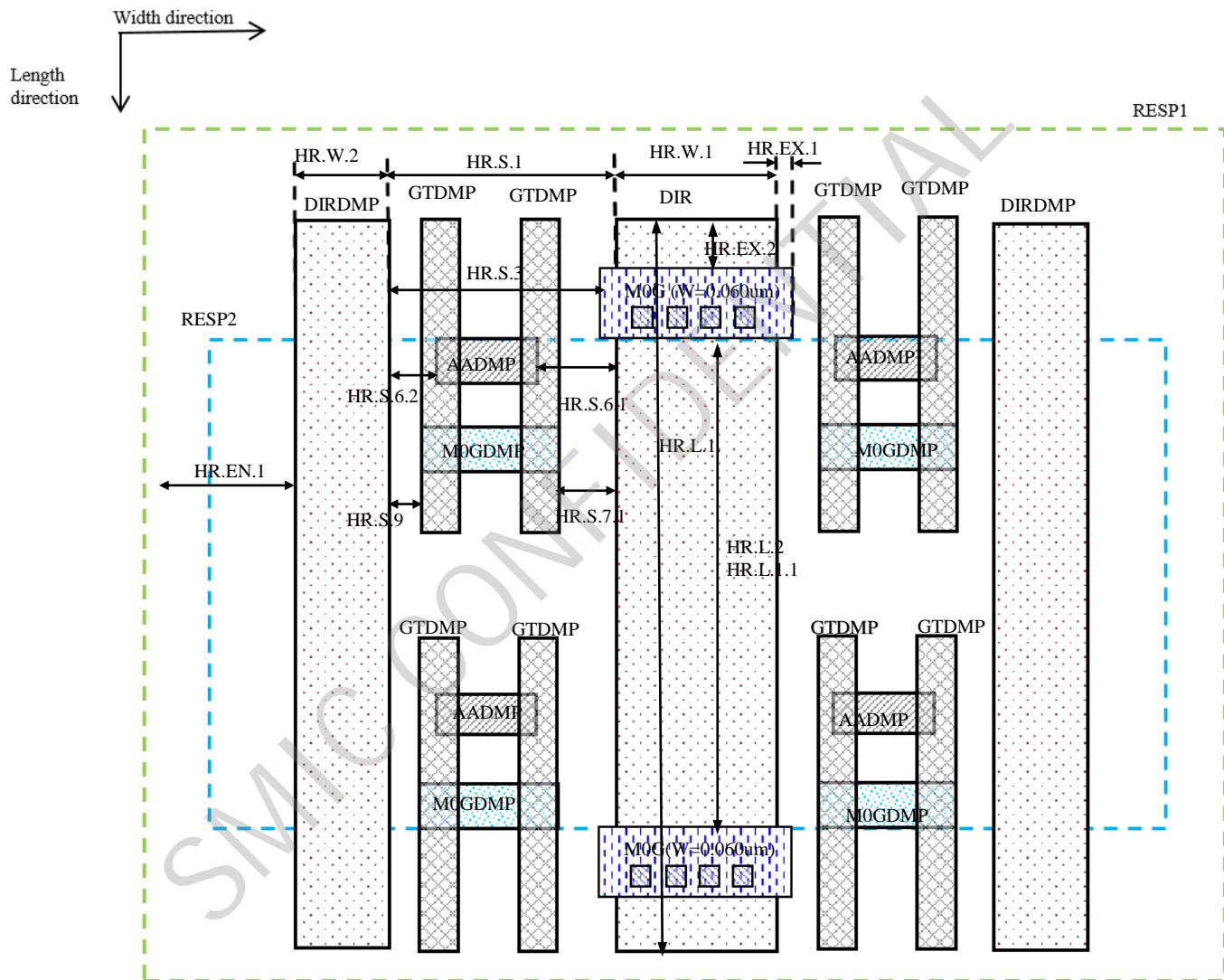
Rule number	Description	Opt.	Design Value	Unit
HR.R.15	(RESP2 AND DIR) overlap M0G is not allowed.			
HR.R.16	DIRDMP length must be same with DIR in DIR length direction.			
HR.R.17	AADMP/GTDMMP/M0GDMP must to be drawn in RESP2 region.			
HR.R.18	M0DMP interact with RESP1 is not allowed.			
HR.DN.1	(DIR OR DIRDMP) density in window 20umx20um,stepping 10um	≤	50%	
HR.DN.2	(DIR OR DIRDMP) full chip density	≤	30%	

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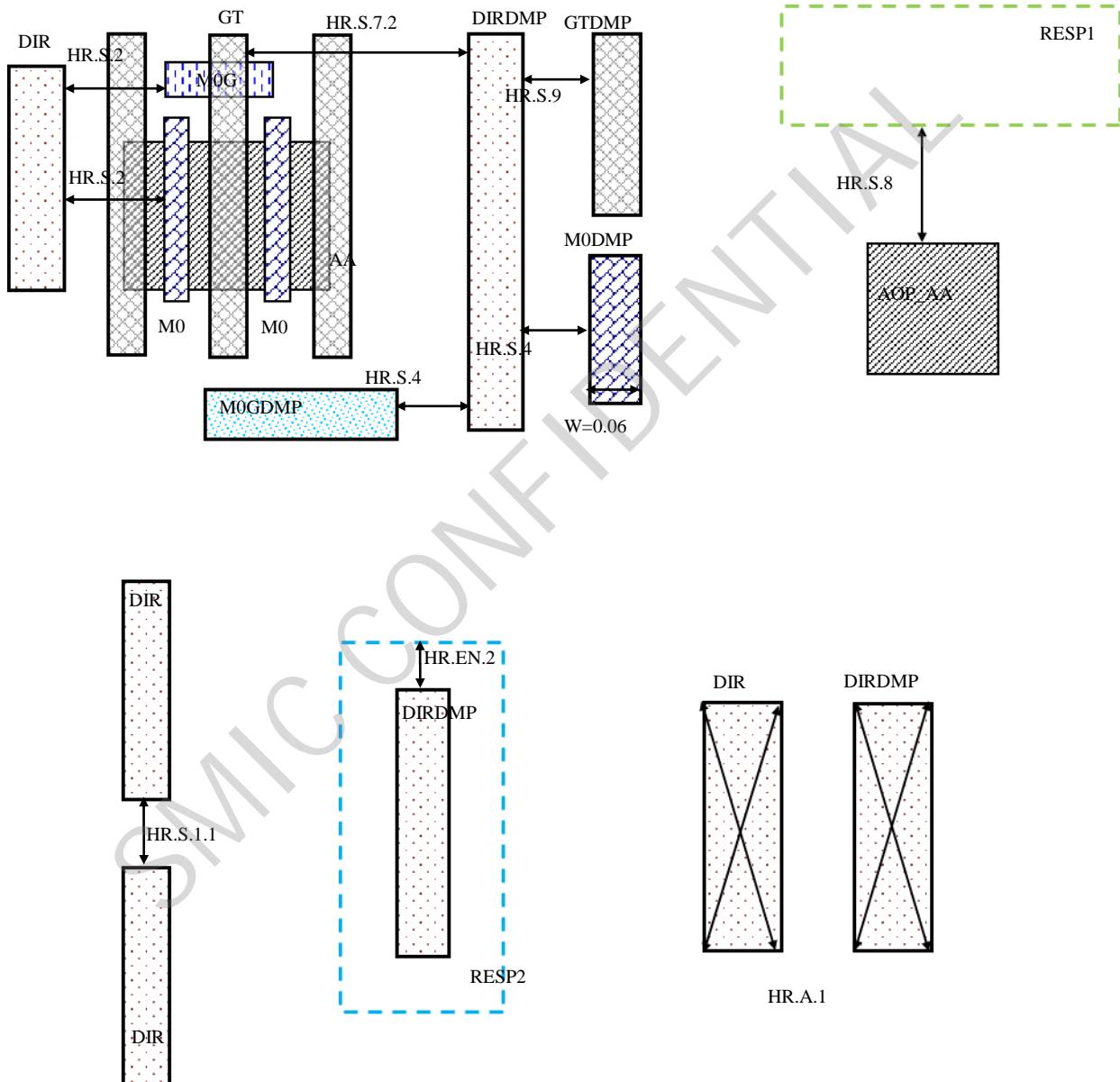


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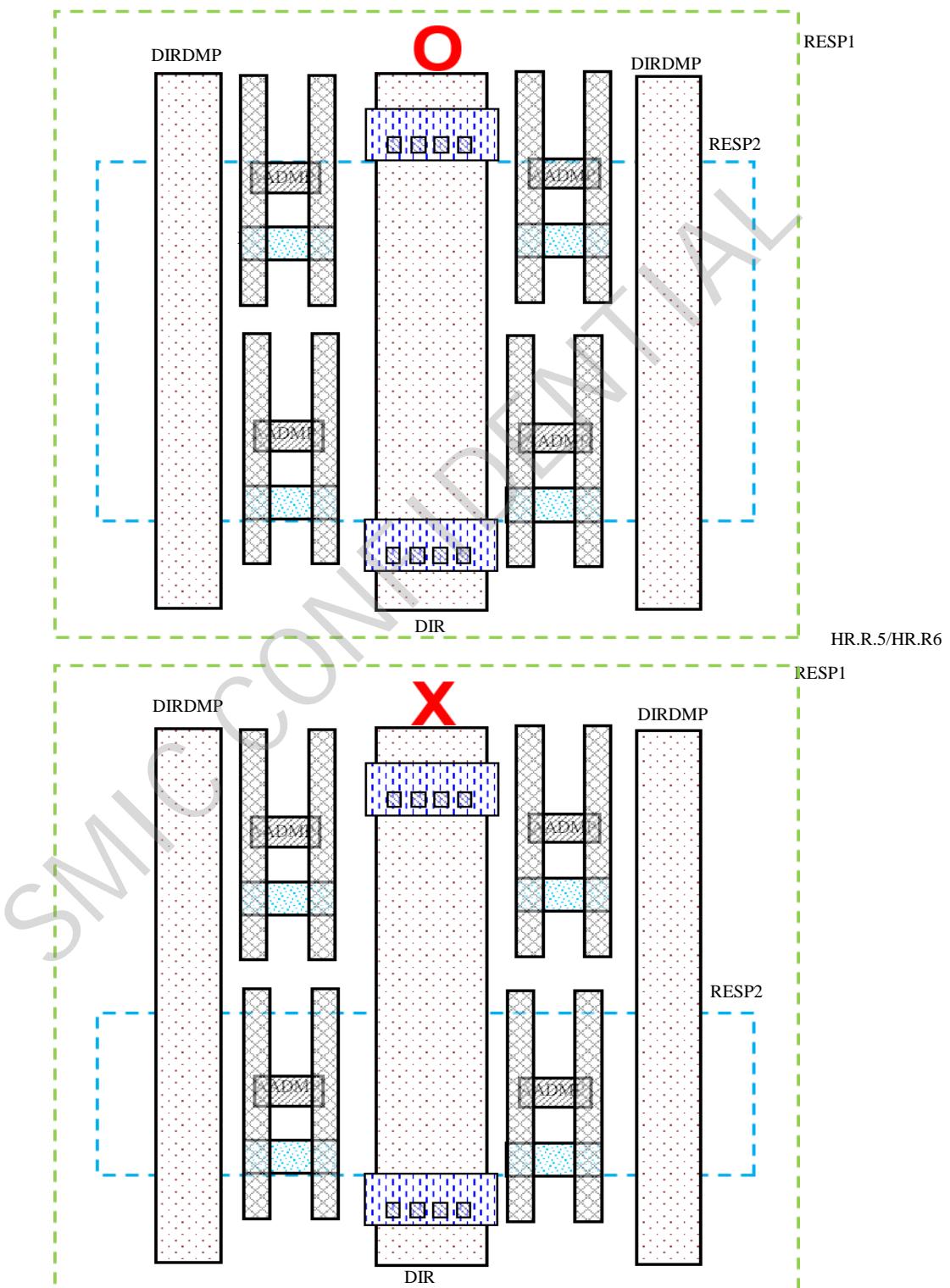


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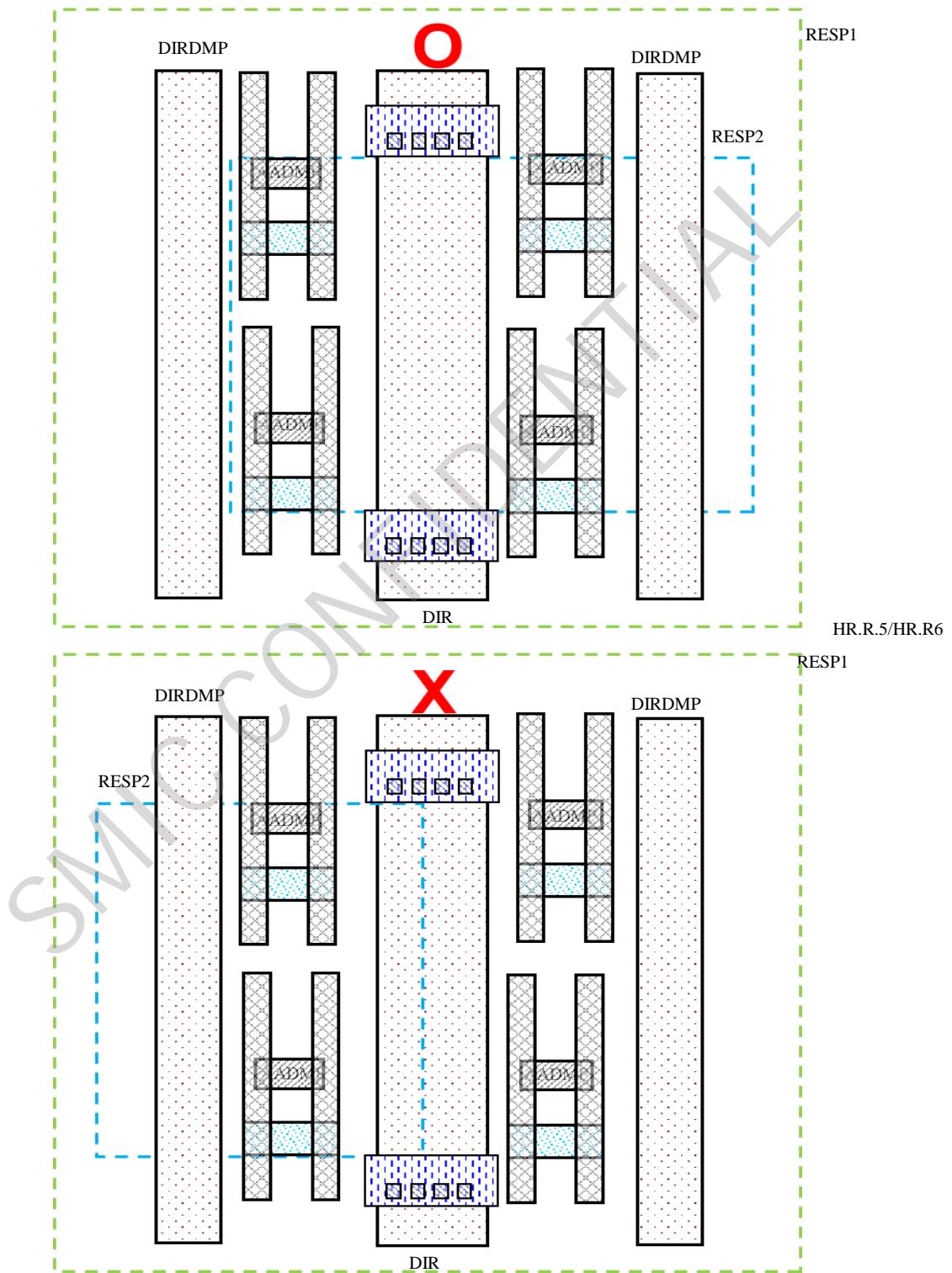


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7.8.2 NW under STI resistor rules

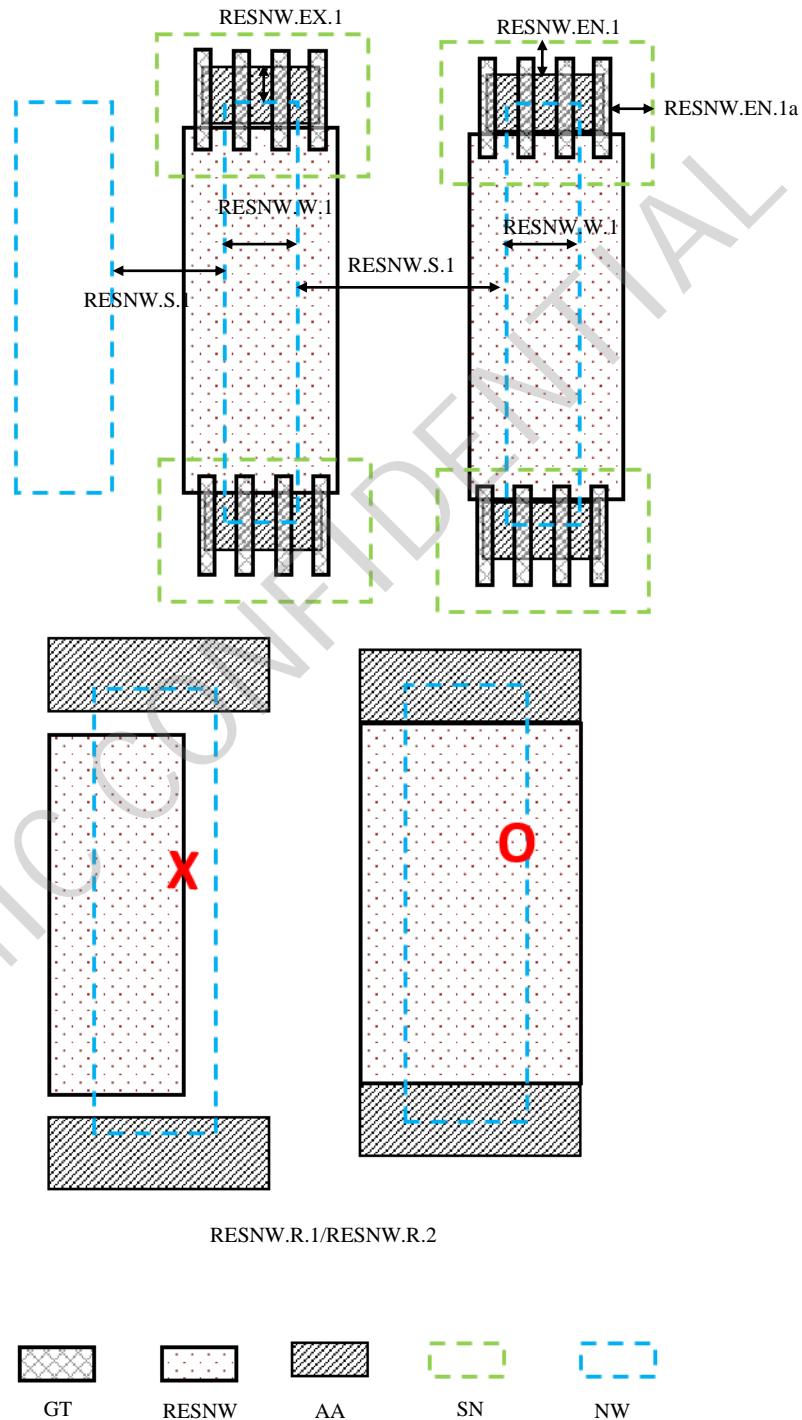
RESNW layer is to define the NW resistor area where no other implantation layer except NW. NW resistor design must be covered with RESNW layer.

NW resistor under STI: (RESNW AND NW) NOT AA.

Resistor NW: NW INTERACT RESNW

Rule number	Description	Opt.	Design Value	Unit
RESNW.W.1	Resistor NW width	\geq	1.584	um
RESNW.W.1a	Suggest Nsq of resistor (length/width ratio) ≥ 1 for stable resistance.			
RESNW.S.1	Space between Resistor NW and Resistor NW or NW	\geq	0.90	um
RESNW.S.2	Space between RESNW and ALL_AA (Overlap is not allowed)	\geq	0.432	um
RESNW.EN.1	SN enclosure of (AA INTERACT Resistor NW)	\geq	0.341	um
RESNW.EN.1a	SN enclosure of (AA INTERACT Resistor NW) (AA vertical edge extend 1/2 GT width) in S/D direction	\geq	0.36	um
RESNW.EX.1	AA extension outside of Resistor NW in GATE poly direction	\geq	0.289	um
RESNW.EX.1a	AA (vertical edge extend 1/2 GT width) extension outside of Resistor NW in S/D direction	\geq	0.27	um
RESNW.EX.2	RESNW extension outside of NW resistor along resistor width direction	\leq	0.4	um
RESNW.R.1	RESNW horizontal edge must align with AA horizontal edge.			
RESNW.R.2	RESNW must separate Resistor NW into two or more NWs			
RESNW.R.3	NW resistor must be rectangle.			
RESNW.R.4	DNW, SP, SVT_P, LVT_P, HVT_P, ULVT_P, LFN_P implant layers are not allowed in NW resistor area.			
RESNW.R.5	NW resistor length direction must be GATE poly direction.			

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7.8.3 Diode design rules

DSTR layer is the DRC marker layer for diode design, designer must draw DSTR layer to cover the diode design for DRC checking.

Rule number	Description	Opt.	Design Value	Unit
DSTR.W.1	DSTR width	\geq	0.192	um
DSTR.W.2	(GT AND GTMK1) width of core region in S/D direction except pickup area.	=	0.02	um
DSTR.W.3	(GT AND GTMK1) width of I/O region and pickup of core region in S/D direction	=	0.086	um
DSTR.S.1	DSTR space	\geq	0.192	um
DSTR.S.2	Space between DSTR (INTERACT ACTIVE) and ACTIVE (ACTIVE CUT DSTR is not allowed)	\geq	0.048	um
DSTR.S.2a	Space between DSTR (INTERACT ACTIVE) and ACTIVE (ACTIVE vertical edge expanding 1/2 GT width) in S/D direction, (ACTIVE CUT DSTR is not allowed)	\geq	0.065	um
DSTR.S.3	Space between DSTR and ALL_GT	\geq	0.035	um
DSTR.EN.1	DSTR enclosure of ACTIVE (INTERACT M0)	\geq	0.048	um
DSTR.EN.1a	DSTR enclosure of ACTIVE (INTERACT M0, ACTIVE vertical edge expanding 1/2 GT width) in S/D direction	\geq	0.065	um
DSTR.EN.2	DSTR enclosure of ALL_GT (Except GT jog width \leq 0.004um)	\geq	0.035	um
DSTR.A.1	Area of DSTR (INTERACT ACTIVE)	\geq	0.092	um
DSTR.A.2	Enclosed area of DSTR (INTERACT ACTIVE)	\geq	0.092	um
DSTR.R.1	DSTR overlap SVT_N, SVT_P, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P is not allowed.			
DSTR.R.2	((GT NOT P2) INTERACT ACTIVE) must connect to S/D ACTIVE in DSTR region.			
DSTR.R.3	Delta V > 3V between core diode GATE and core diode bulk is not allowed.			



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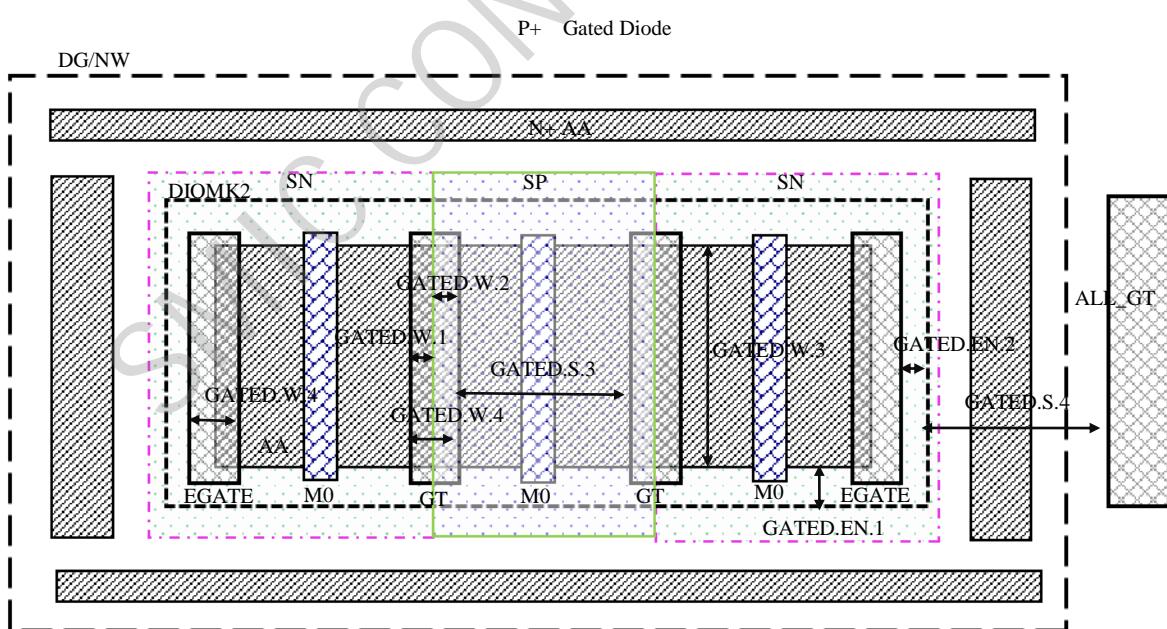
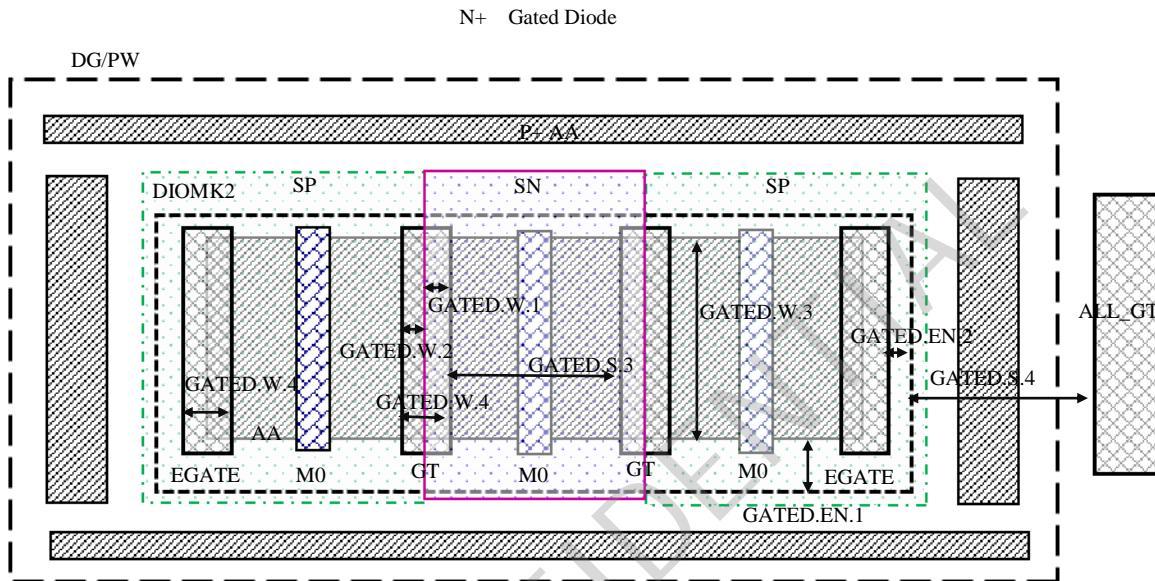
7.8.4 Gated Diode design rules

DIOMK2 is must layer for GATED Diode, designer must draw this marker layer to cover the GATED diode design for DRC checking.

Rule number	Description	Opt.	Design Value	Unit
GATED.W.1	Width of ((SN AND GATE) AND DIOMK2) (Except GATE abut AA vertical edge)	=	0.076	um
GATED.W.2	Width of ((SP AND GATE) AND DIOMK2) (Except GATE abut AA vertical edge)	=	0.076	um
GATED.W.3	Channele width INSIDE DIOMK2 region	=	0.384~0 .96	um
GATED.W.4	Width of (GATE AND DIOMK2)	=	0.152	um
GATED.S.1	Space between DIOMK2 and AA	≥	0.048	um
GATED.S.2	Space between DIOMK2 and AA (AA vertical edge expanding 1/2 GT width) in S/D direction	≥	0.065	um
GATED.S.3	GATE space on the same AA INSIDE DIOMK2 region	=	0.118	um
GATED.S.4	Space between DIOMK2 and (ALL_GT NOT P2)	≥	0.059	um
GATED.EN.1	DIOMK2 enclosure of AA	≥	0.048	um
GATED.EN.1a	DIOMK2 enclosure of AA (AA vertical edge extend 1/2 GT width) in S/D direction	≥	0.065	um
GATED.EN.2	DIOMK2 enclosure of (ALL_GT NOT P2) (Cut is not allowed)	≥	0.059	um
GATED.R.1	AA CUT DIOMK2 is not allowed.			
GATED.R.2	(DIOMK2 AND AA) must be fully covered by DG.			
GATED.R.3	DIOMK2 overlap DUM_GT is not allowed.			
GATED.R.4	(AA NOT GT) INSIDE DIOMK2 must interact M0.			

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7.8.5 BJT design rules

Rule number	Description	Opt.	Design Value	Unit
BJT.W.1a	Base AA width in ENDCAP direction for (DMPNP NOT DG)	\geq	0.144	um
BJT.W.1b	Base AA width in ENDCAP direction for (DMPNP INSIDE DG)	$=$	0.144	um
BJT.W.2a	Collector AA width in ENDCAP direction for (DMPNP NOT DG)	\geq	0.288	um
BJT.W.2b	Collector AA width in ENDCAP direction for (DMPNP INSIDE DG)	$=$	0.144	um
BJT.W.3	Base AA and Collector AA width in S/D direction	\geq	0.204	um
BJT.W.4	AOP_GT width in DMPNP region	$=$	0.086	um
BJT.S.1	Space between Collector AA and Base AA in ENDCAP direction	$=$	0.24	um
BJT.S.2a	Space between Emitter AA and Base AA in ENDCAP direction for (DMPNP NOT DG)	$=$	0.48	um
BJT.S.2b	Space between Emitter AA and Base AA in ENDCAP direction for (DMPNP INSIDE DG)	$=$	0.192	um
BJT.S.3	Space between Collector AA and Base AA in S/D direction	$=$	0.408	um
BJT.S.4	Space between Emitter AA and Base AA in S/D direction	$=$	0.612	um
BJT.S.5	Space between two Collector AA (PRL > 0um) between different units in same DMPNP (different units can not share same Collector AA)	$=$	0.768~0.96	um
BJT.S.6	Space between DMPNP and ALL_GT	\geq	0.035	um
BJT.EN.1	DMPNP enclosure of Collector AA	$=$	0.768~1.008	um
BJT.EN.2	DMPNP enclosure of ALL_GT	\geq	0.035	um
BJT.R.1	((Emitter AA SIZING 0.048um) SIZING -0.048um) must be one 1.632*1.728 um or 2.04um*2.352um rectangle outside DG			
BJT.R.2	Overlap SVT_N, SVT_P, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, VARMOS, or INST is not allowed.			
BJT.R.3	BIPOLA must be inside DMPNP.			

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Rule number	Description	Opt.	Design Value	Unit
BJT.R.4	GT on Emitter AA must connect to Base AA.			

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7.8.6 Varactor design rules

Rule number	Description	Opt.	Design Value	Unit
VAR.W.1	Channel length of (GATE AND VARMOS)	=	0.18~0.242	um
VAR.W.2	Channel width of (GATE AND VARMOS)	\geq	0.384	um
VAR.S.1	Space between VARMOS and ACTIVE	\geq	0.125	um
VAR.S.1a	Space between VARMOS and ACTIVE (ACTIVE vertical edge extend 1/2 GT width) in S/D direction	\geq	0.144	um
VAR.EN.1	VARMOS enclosure of AA	\geq	0.125	um
VAR.EN.1a	VARMOS enclosure of AA (AA vertical edge extend 1/2 GT width) in S/D direction	\geq	0.144	um
VAR.EN.2	VARMOS enclosure of ALL_GT	\geq	0.035	um
VAR.EN.3a	SN fully enclosure (GATE AND VARMOS) AND NW) along the S/D direction	\geq	0.32	um
VAR.EN.3b	SN fully enclosure (GATE AND VARMOS) AND NW) along GATE poly direction.	\geq	0.125	um
VAR.R.1^[NC]	VARMOS layer must be drawn to fully cover the varactor devices			
VAR.R.2	VARMOS overlap (GATE AND SP), SVT_N, SVT_P, LVT_N, LVT_P, HVT_N, HVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, or PSUB is not allowed.			
VAR.R.3	SP overlap ((GATE AND NW) AND VARMOS) is not allowed.			

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7.8.7 MOM design rules

MOM (metal oxide metal) capacitor is based on the capacitance between parallel same layer metal lines and different layer metal lines

SMIC only provided M1/Mxy/1.25xMy/1.25xMn (M1~M7) MOM spice model and PDK. It is strongly recommended designers to use the MOM provided by SMIC PDK to have better characterization prediction and LVS check.

The CAD layers are used for MOM designs:

- a. MOMDMY (211;1) is DRC/LVS mark layer for MOM device.
- b. MOMTEM (211;2) LVS marking layer for MOM region
- c. MOMP1 (211;3) is LVS marking layer for MOM capacitor mesh terminal one
- d. MOMP2 (211;4) is LVS marking layer for MOM capacitor mesh terminal two
- e. MOMMES (211;5) is LVS marking layer for MOM mesh capacitor
- f. RFMOM (211;6) is LVS marking layer for RF MOM capacitor
- g. RF3T (183;2) is DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM
- h. MOMMKn (211;11~211;17, n=1~7) is DRC mark layer for individual MOM metal layer

Dummy block layer MnDUB (n=1~7) are applied in SMIC inductor designs with pre-inserted dummy. So SMIC dummy script will block out MOM region for auto dummy insertion

Rule number	Description	Opt.	Design Value	Unit
MOM.S.1	Space between (Mn AND MOMMKn AND MOMDMY) and Vn /Vn-1 (n = 1~6) outside of MOMDMY. Vn-1 is the via underneath 1xMn, and Vn is the via above 1xMn. Vn can be inter-via or top via (TV1 or TV2).	\geq	0.08	um
MOM.S.2	Space between metal (M1/Mxy) and line-end in MOMMKn	\geq	0.09	um
MOM.L.1	PRL of MOM fingers when M1/Mxy metal finger space < 0.035um	\leq	35	um
MOM.A.1	Maximum sidewall area of total M1/Mxy metals in MOM without Via ($0V \leq \Delta V_{max} \leq 1.155V$)	\leq	7.2E+06	um ²
MOM.A.2	Maximum sidewall area of total M1/Mxy metals in MOM without Via ($\Delta V_{max} > 1.155V$)	\leq	1.2E+07	um ²
MOM.R.1	It is not allowed: 1) V1 in MOMMK1 2) Vn/Vn-1 in MOMMKn (n=2~7), Vn-1 is the via underneath 1xMn, and Vn is the via above 1xMn. Vn can be inter-via or top via (TV1 or TV2 or UTV).			

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Rule number	Description	Opt.	Design Value	Unit
MOM.R.2	MOMDMY and MOMMKn (n=1~7) layers are must for MOM device. DRC checking is based on the label text by MOMDMY layer. Possible label texts and related MOMMKn follow the Table-1.			
MOM.R.3^[NC]	Use symmetrical dummy metal around the matched pairs of MOM cells instead of auto inserted dummy.			
MOM.R.4^[NC]	Active device underneath or above MOM cell should be put into couple capacitance consideration in design.			

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7.8.8 MIM capacitor rules

7.8.8.1 MIMDMY design guidelines

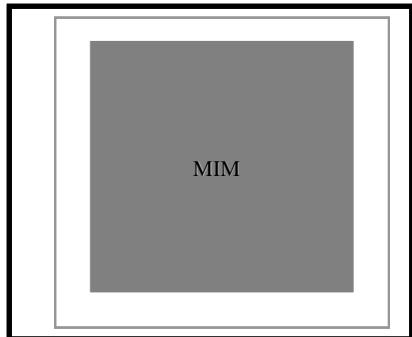
MIMDMY is the DRC marking layer for active MIM, which must not include dummy MIM. Active MIM can not do DRC checking if customers don't draw MIMDMY layer.

MIMDMY design is layout guideline which requires performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow layout guidelines which purpose is to ensure better performance for process and device. Customers can waive violations based on their own judgment, and please consult with process integration engineers if customers feel the need.

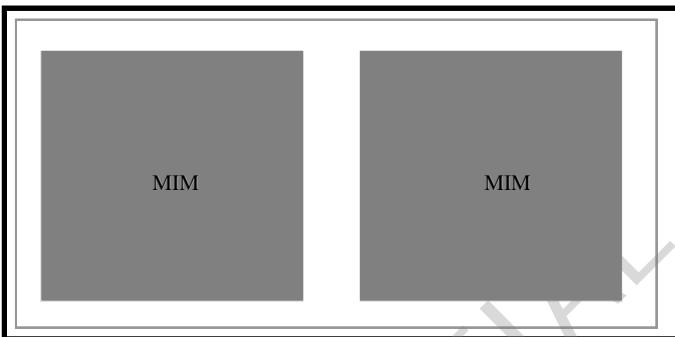
SMIC spice model and PDK is based on SMIC layout guidelines. And SMIC don't provide spice model and PDK if customers don't follow the layout guidelines.

Rule number	Description	Opt.	Design Value	Unit
MIMDMY.1^[G] [NC]	MIMDMY is the DRC marking layer for active MIM, which must not include dummy MIM. Active MIM can not do DRC checking if customers don't draw MIMDMY layer.			
MIMDMY.2^[G]	MIMDMY must fully cover active MIM region. Active MIM is enclosed by MIMDMY	=	0.2	um

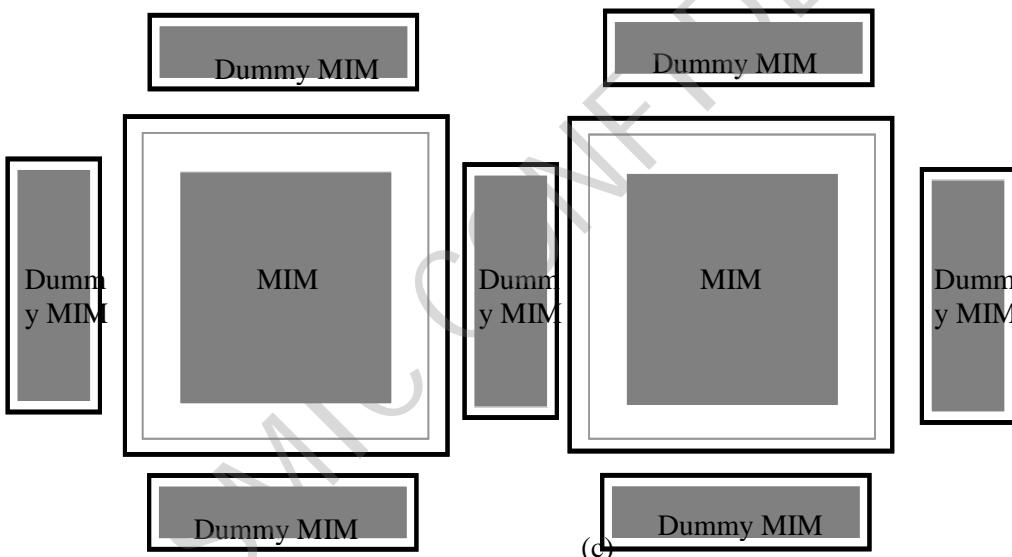
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(a)



(b)



(c)



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7.8.8.2 Two masks MIM (Using two plates form Metal-Insulator-Metal) design rules

7.8.8.2.1 MIM (Top plate of two masks MIM) design rules

Active MIM: MIM blocked by MIMDMY or MIM interact with top via.

MIM: Top plate

CTOP: Bottom electrode or Bottom plate NOT < 2.8um

Rule number	Description	Opt.	Design Value	Unit
MIM.W.1	MIM width and length as capacitor top plate	\geq	2	um
		\leq	50	um
MIM.S.2	Space between two MIMs as top plate	\geq	1.2	um
MIM.EN.3	MIM enclosure of Via which connect to this MIM	\geq	0.24	um
MIM.S.4	Space between Via which connect with bottom plate (plate-2) and MIM region	\geq	0.4	um
MIM.S.5	Space between two Vias on MIM	\geq	0.484	um
MIM.S.6^[R]	To avoid strong coupling, M_n is not recommended to put beneath MIM, minimum space for M_n to MIM.	\geq	1	um
MIM.D.7^[R]	MIM density, except LOGO region Dummy MIM pattern is required if MIM density is less than 3%. Note that if dummy MIM is added, dummy CTOP need be added correspondingly.	\geq	3%	
MIM.W.8	Dummy MIM width	\geq	0.78	um
MIM.S.9	Space between dummy MIM and MIM region	\geq	0.8	um
MIM.S.10	Space between dummy MIM and Plate-2	\geq	0.8	um
MIM.R.11	MIM must be inside CTOP.			
MIM.12^[R]	It's not recommended to put sensitivity devices under MIM. The sensitivity devices include RF, Analog, etc.			
MIM.13	For two top metal process, two-mask MIM structure is required to be placed between TM1 (first top metal) and TM2 (second top metal).			

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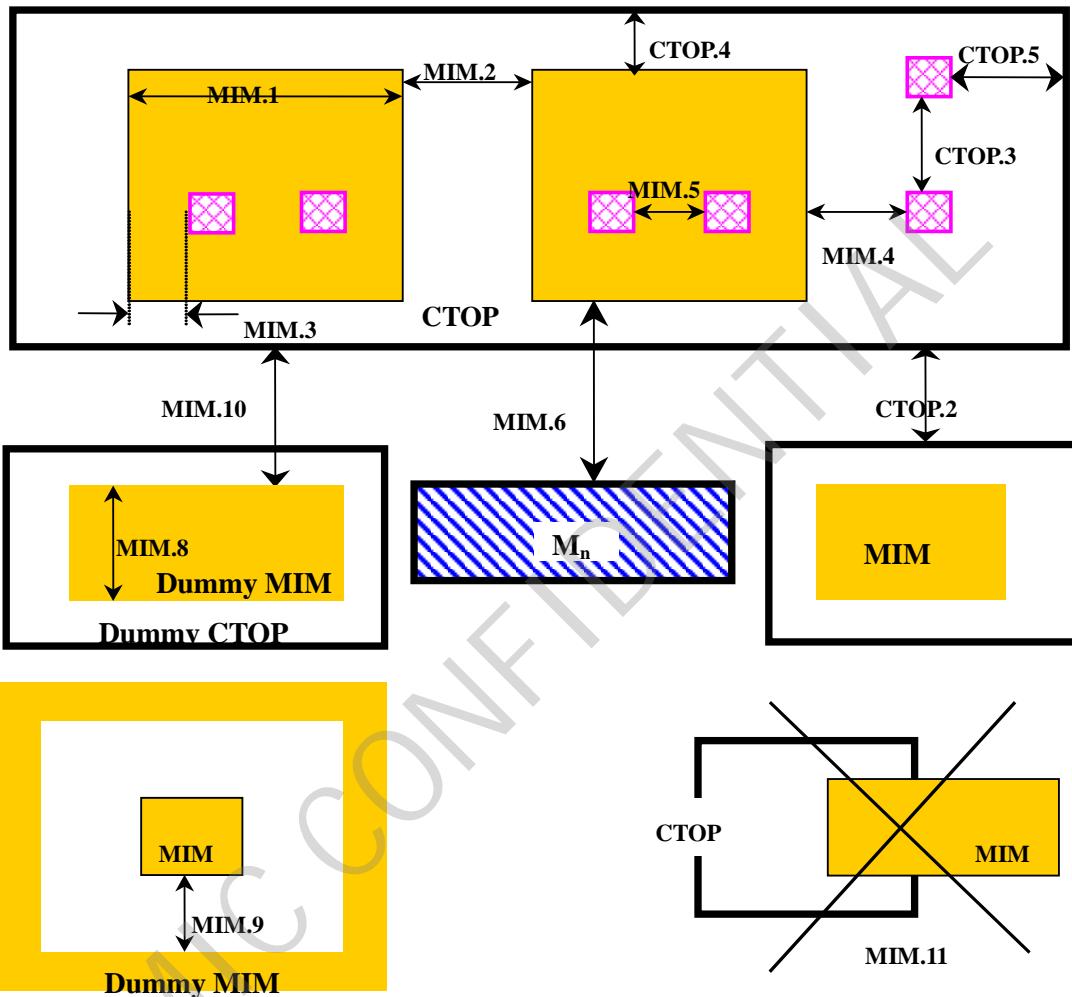
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7.8.8.2.2 CTOP (Bottom plate of two masks MIM) design rules

CTOP: Bottom electrode or Bottom plate

Rule number	Description	Opt.	Design Value	Unit
CTOP.W.1	CTOP width and length	\geq	2.8	um
		\leq	55	um
CTOP.S.2	Space between CTOP	\geq	1.2	um
CTOP.S.3	Space between two Vias on CTOP	\geq	0.484	um
CTOP.EN.4	CTOP enclosure of MIM	\geq	0.4	um
CTOP.EN.5	CTOP enclosure of Vias which connect to this CTOP	\geq	0.2	um
CTOP.S.6^[R]	Space between TM1 and CTOP. TM1 metal line is not recommended to put beneath CTOP	\geq	0.5	um

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CTOP: Capacitor bottom plate or dummy



MIM: Capacitor top plate or dummy MIM pattern



M₁~M_n: Normal metal layer



Via connected to MIM or CTOP

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7.8.9 Metal E-Fuse/OTP layout guidelines

For the fuse component, it must be drawn EFUSE (81;2), MTFUSE (81;3), FUSEAD(81;4); FUSEMK1 (81;152) marker layer.

E-fuse element is covered by EFUSE (81;2).

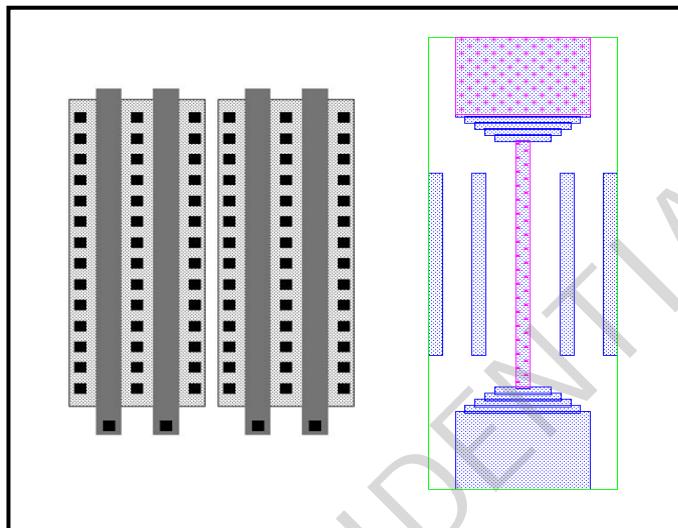
E-fuse fuse link (function area) is marked with MTFUSE (81;3).

E-fuse anode is marked with FUSEAD (81;4).

All fuse component must be fully covered by FUSEMK1 (81;152).

Rule number	Description	Opt.	Design Value	Unit
EFU.1a^{[G][NC]}	FUSEMK1(81;152) must fully cover all fuse component, including EFUSE (81;2) region, program transistor, etc.			
EFU.1b^[G]	FUSEMK1 (81;152) must interact with EFUSE (81;2) region.			
EFU.1c^[G]	EFUSE (81;2) region must be fully covered by FUSEMK1 (81;152).			
EFU.2a^{[G][NC]}	EFUSE (81;2) must fully cover the whole fuse element and related dummy region.			
EFU.2b^[G]	EFUSE (81;2) must interact with MTFUSE(81;3) and FUSEAD(81;4).			
EFU.2c^[G]	MTFUSE(81;3) and FUSEAD(81;4) must be fully covered by EFUSE (81;2).			
EFU.3^{[G][NC]}	(MTFUSE AND M1) is just the EFUSE function area.			
EFU.4^[G]	MTFUSE (81;3) region must exclude M1~M3 dummy patterns.			
EFU.5^{[G][NC]}	It is strongly recommended to adopt SMIC standard efuse element, including program transistor.			
EFU.6^{[G][NC]}	If designers plan to adopt customer own design, designers must provide efuse layout to SMIC for risk assessment before design start.			

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M1



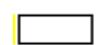
MTFUSE



FUSEAD



EFUSE



FUSEMK1

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7.9 Seal-ring design layout guidelines

A. Use of the scribe lane seal ring to protect test chip is recommended

A continuous scribe lane and seal ring is required on all sides of a chip that is intended for dicing and packaging. The seal ring provides both a low resistance path to ground for surge currents and a metal seal against ionic contaminations. 45 degree bent is expected around every die corner. Multiple stacked via/Metal trench are considered to suppress crack risk during dicing saw operation in assembly.

B. Typical structure of scribe lane seal ring

For products less than 11 metal layers, please skip the metal and via layers that are not used in the product.

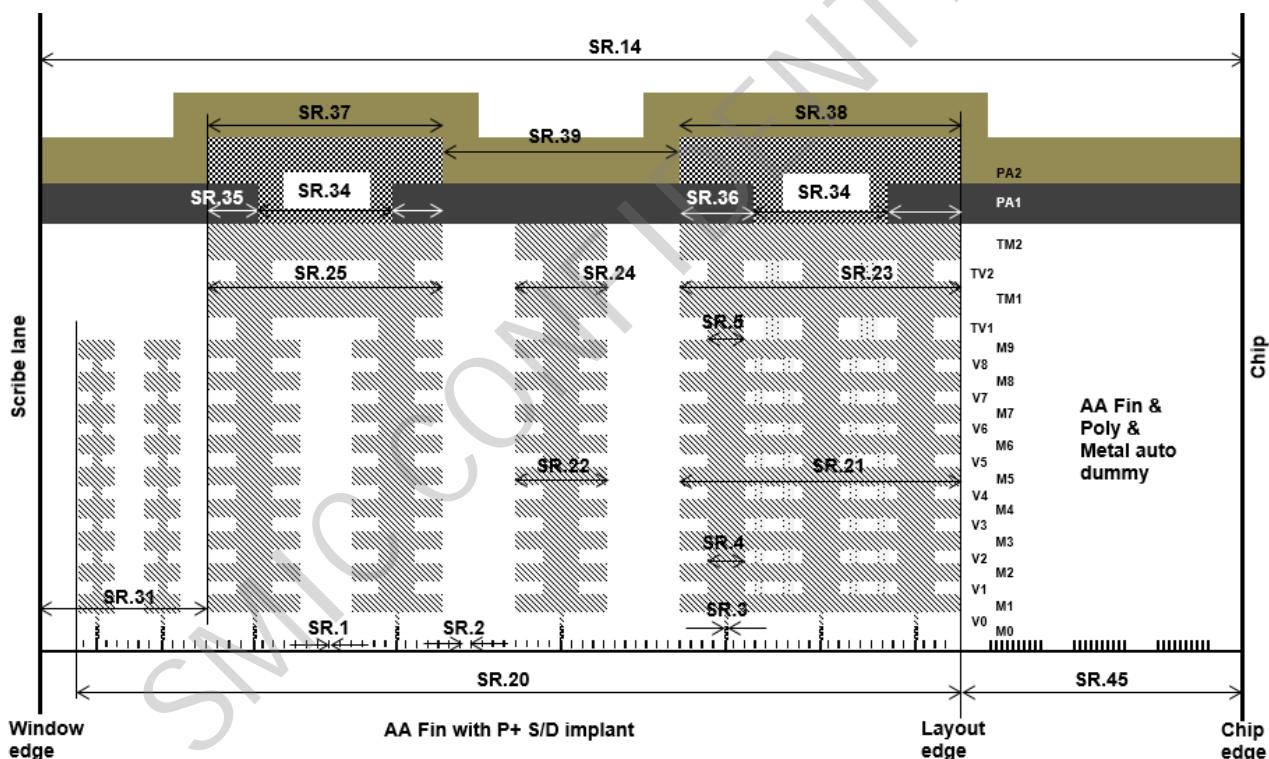


Fig.1 Cross sectional schematic of 11 metal layers seal ring structure

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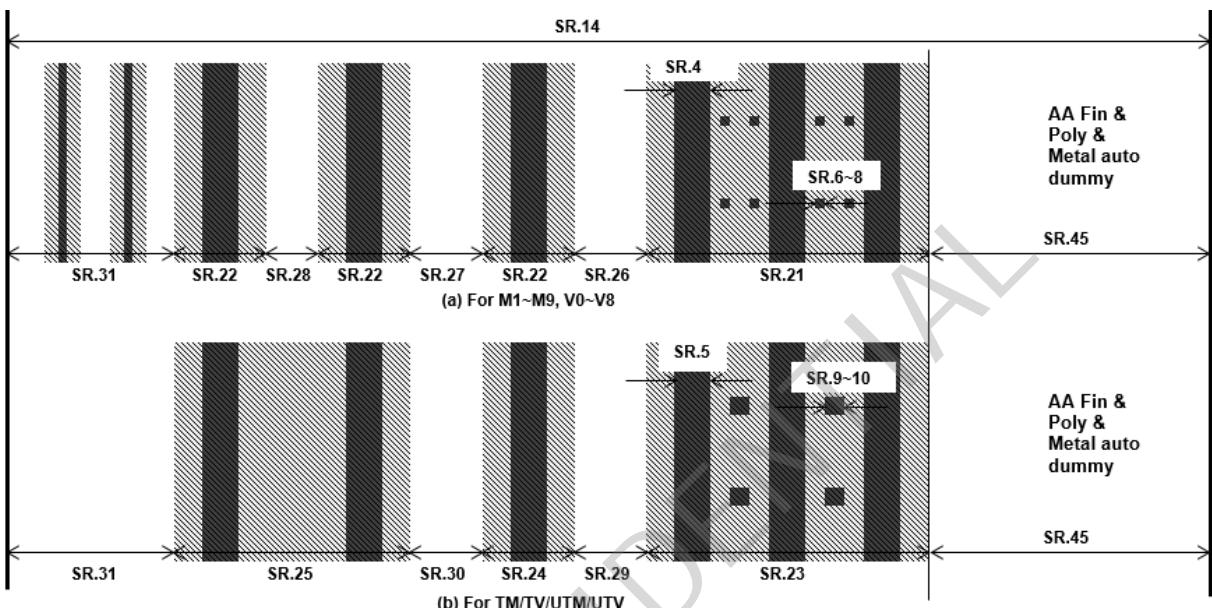


Fig.2 Schematic top view of the seal ring structure

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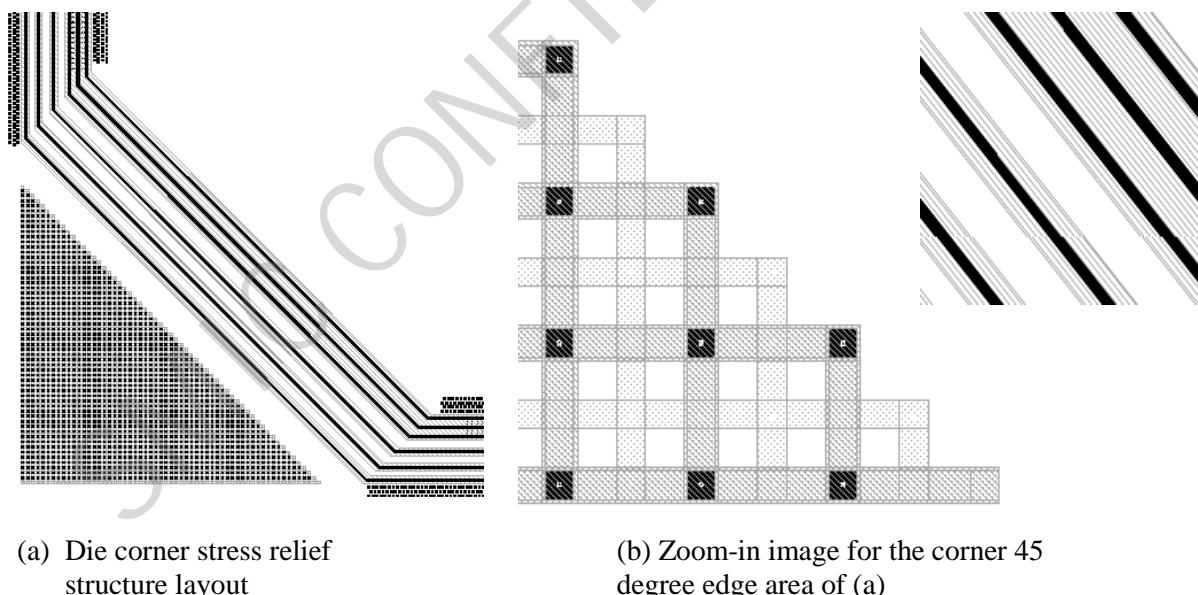
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C. Die Corner Layout

The chamfer region is required for all chips for process robustness. A chamfer or corner bevel of more than 66.6um is required to be cut from each corner of the chip. The chamfer area is triangular and has an area of more than half of 66.6um*66.6um square.

The seal ring corner layout in Figure.3~Figure.5 is recommended to SMIC's customers to manage local stress at each die corner. Metal & via dummy pattern is recommended at each corner of seal ring. The dimension of each segment in the corner layout is given in Figure.3~4.

Please customer follows SMIC standard of seal ring corner rule (figure.4, figure.5) both for the situations that seal ring design and layout implemented in SMIC and customer sides.



(a) Die corner stress relief structure layout

(b) Zoom-in image for the corner 45 degree edge area of (a)

Fig.3 Die corner stress relief structure layout

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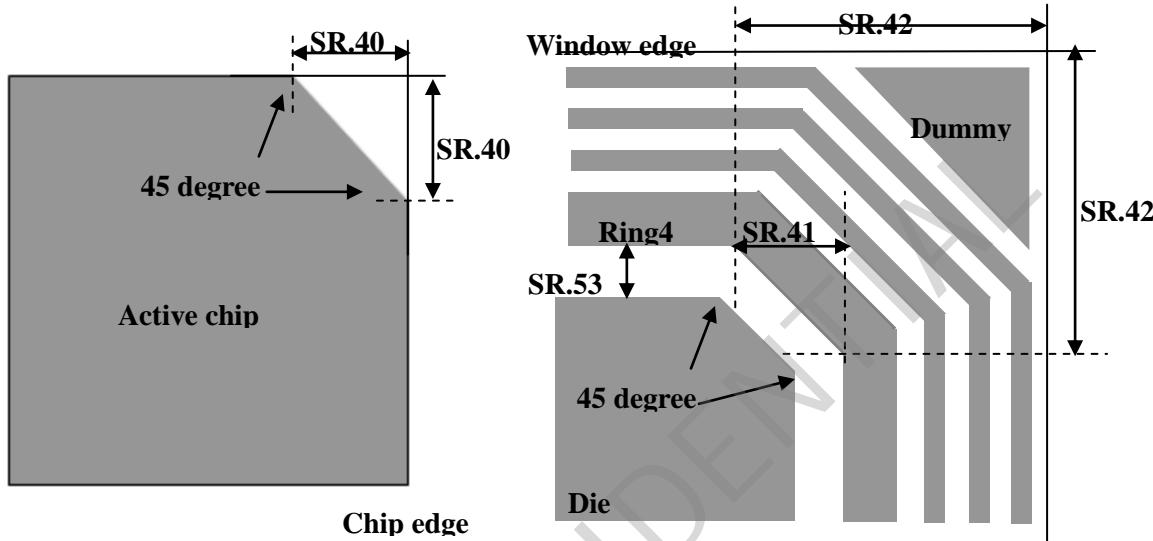


Figure4 Chamfer area at
chip corner

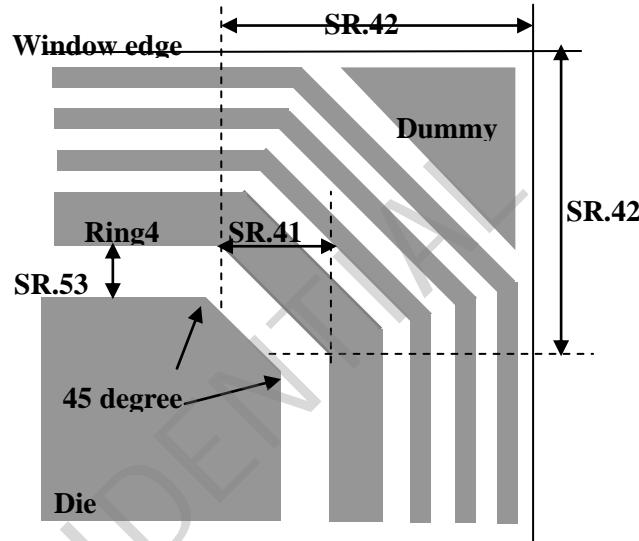


Figure5 Seal ring corner if
applied by SMIC

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7.9.1 Seal-ring design layout guidelines

This section is for Dimension of Seal ring structure, not for DRC check.

Rule number	Description	Opt.	Design Value	Unit
SR.1a^[G]	Fixed width of orthogonal PPAA	=	0.134	um
SR.1b^[G]	Fixed width of PPAA at 45 degree angle area	=	0.132~0.136	um
SR.2a^[G]	Space between orthogonal PPAA	=	0.154	um
SR.2b^[G]	Space between PPAA at 45 degree angle area	=	0.214~0.274	um
SR.3a^[G]	Fixed width of M0/V0 slot at orthogonal direction	=	0.1	um
SR.3b^[G]	Fixed width of M0/V0 slot at 45 degree angle area	=	0.098~0.102	um
SR.4a^[G]	Fixed width of Vy/1.25xVn/2xVn slot at orthogonal direction	=	0.45 or 0.1	um
SR.4b^[G]	Fixed width of Vy/1.25xVn/2xVn slot at 45 degree angle area	=	0.500~0.504 or 0.12~0.16	um
SR.5a^[G]	Fixed width of 10xTVn/14xTVn/UTV slot at orthogonal direction	=	0.414	um
SR.5b^[G]	Fixed width of 10xTVn/14xTVn/UTV slot at 45 degree angle area	=	0.460~0.470	um
SR.6^[G]	Fixed width of square V0/Vy size	=	0.032	um
SR.7^[G]	Fixed width of square 1.25xVn size	=	0.040	um
SR.8^[G]	Fixed width of square 2xVn size	=	0.062	um
SR.9^[G]	Fixed width of square 10xTVn/UTV size	=	0.324	um
SR.10^[G]	Fixed width of square 14xTVn size	=	0.414	um
SR.11^[G]	M0 slot, V0 slot, Vy slot, 1.25xVn slot, 2xVn slot and 10xTVn/14xTVn/UTV/PA slot and PPAA/M1/Mxy/1.25xMy/1.25xMn/2xMn/10xTMn (or 14xTMn) /UTM/ALPA slot must be drawn in sealring region (slot pattern is NOT square pattern).			
SR.12^[G]	Via slot enclosure by metal, except UTV slot	≥	0.15	um
SR.12b^[G]	UTV slot enclosure by UTM	≥	0.45	um
SR.12c^[G]	V0 slot must be coincidence with M0 slot			

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Rule number	Description	Opt.	Design Value	Unit
G]				
SR.13^[G]	Seal ring must be a close ring excluding RF device (RFDEV region).			
SR.14^[G]	Total seal ring MARKS width	=	21.6	um
SR.15^[G]	Space between two square Vys/1.25xVns/2xVns	≥	0.09	um
SR.16^[G]	Space between two square 10xTVns/14xTVns/UTVs	≥	0.5	um
SR.17a^[G]	Width of M1/Mxy/1.25xMy/1.25xMn/2xMn/10xTMn/14xTMn/UTM/ALP A	≥	0.5	um
		≤	5	um
SR.17b^[G]	Width of M1/Mxy/1.25xMy/1.25xMn/2xMn/10xTMn/14xTMn/UTM/ALP A at 45 degree angle area	≥	0.5	um
		≤	7.08	um
SR.18^[G]	Space between two M0s or two M1/Mxy or two 1.25xMy /1.25xMns or two 2xMns or two 10xTMns or two 14xTMns or two UMs	≥	0.5	um
SR.19^[G]	It is not allowed PPAA/GT/M0/M1/Mxy/1.25xMy /1.25xMn/2xMn/10xTMn/14xTMn/UTM/V0/1xVn/1.25xVn/2xVn/10xTVn/14xTVn/UTV/PA CUT MARKS. This rule also checks PPAA, AA, GT, metal, via dummy pattern (data type 1,7,8). V0/1xVn/1.25xVn/2xVn/10xTVn/14xTVn/UTV definition is following main rule.			
SR.20^[G]	Width of ((PPAA su 0.077) sd 0.077) in seal ring	=	15.11	um
SR.21^[G]	M1/Mxy/1.25xMy/1.25xMn/2xMn width of ring4	=	5	um
SR.22^[G]	M1/Mxy/1.25xMy/1.25xMn/2xMn width of ring1,ring2, ring3	=	1.5	um
SR.23^[G]	10xTMn/14xTMn/UTM width of ring3	=	5	um
SR.24^[G]	10xTMn/14xTMn width of ring2	=	1.5	um
SR.24b^[G]	UTM width of ring2	=	1.8	um
SR.25^[G]	10xTMn/14xTMn/UTM width of ring1	=	4	um
SR.26^[G]	Space between M1/Mxy/1.25xMy/1.25xMn/2xMn ring4 and	=	1.5	um

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Rule number	Description	Opt.	Design Value	Unit
	ring3			
SR.27 ^[G]	Space between M1/Mxy/1.25xMy/1.25xMn/2xMn ring3 and ring2	=	1.5	um
SR.28 ^[G]	Space between M1/Mxy/1.25xMy /1.25xMn/2xMn ring2 and ring1	=	1	um
SR.29 ^[G]	Space between 10xTMn/14xTMn ring3 and ring2	=	1.5	um
SR.29b ^[G]	Space between UTM ring3 and ring2	=	1.35	um
SR.30 ^[G]	Space between 10xTMn/14xTMn ring2 and ring1	=	1.5	um
SR.30b ^[G]	Space between UTM ring2 and ring1	=	1.35	um
SR.31 ^[G]	Space between metal ring1 and window edge	=	2.7	um
SR.32 ^[G]	Space between 1xMn/1.25xMn/2xMn ring4 and layout edge	=	5.4	um
SR.33 ^[G]	Space between 10xTMn/14xTMn/UTM ring3 and layout edge	=	5.4	um
SR.34 ^[G]	PA slot width	=	1.966	um
SR.35 ^[G]	PA slot enclosure by Al ring1	≥	0.9	um
SR.36 ^[G]	PA slot enclosure by Al ring2	≥	1.4	um
SR.37 ^[G]	Al ring1 width	=	4	um
SR.38 ^[G]	Al ring2 width	=	5	um
SR.39 ^[G]	Space between Al ring1 and Al ring2	=	4.5	um
SR.40 ^[G]	Chamfer area size at the chip corner	≥	66.6	um
SR.41 ^[G]	Chamfer length of ring4 of seal ring in the bevel corner. This rule is for customer layout and chip design. This rule is for SMIC to apply seal rings for customer.	≥	66.6	um
SR.42 ^[G]	Distance from window edges to the point that ring4 start to bend 45 degree at seal ring corner. This rule is for SMIC to apply seal rings for customer.	=	82.807	um
SR.43 ^[G]	1xMn/1.25xMn/2xMn/10xTMn/14xTMn width in the dummy	=	0.5	um

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Rule number	Description	Opt.	Design Value	Unit
	relief area			
SR.44^[G]	UTM width in the dummy relief area	=	1.88	um
SR.45^[G]	Space between seal ring inner metal ring and real chip edge	≥	5.4	um

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7.9.2 Seal ring check rules

This section rule is for DRC check in MARKS region.

Rule number	Description	Opt.	Design Value	Unit
SRC.1a	Fixed width of orthogonal PPAA	=	0.134	um
SRC.1b	Fixed width of PPAA at 45 degree angle area	=	0.132~0.136	um
SRC.2a	Space between orthogonal PPAA	=	0.154	um
SRC.2b	Space between PPAA at 45 degree angle area	=	0.214~0.274	um
SRC.3a	Fixed width of M0/V0 slot at orthogonal direction	=	0.1	um
SRC.3b	Fixed width of M0/V0 slot at 45 degree angle area	=	0.098~0.102	um
SRC.4a	Fixed width of Vy/1.25xVn/2xVn slot at orthogonal direction, except the edge length < 0.05um between 270-225 corners	=	0.45 or 0.1	um
SRC.4b	Fixed width of Vy/1.25xVn/2xVn slot at 45 degree angle area	=	0.5~0.504 or 0.12~0.16	um
SRC.5a	Fixed width of 10xTVn/14xTVn/UTV slot at orthogonal direction	=	0.414	um
SRC.5b	Fixed width of 10xTVn/14xTVn/UTV slot at 45 degree angle area	=	0.460~0.470	um
SRC.6	Square V0 and Vy size, rectangular V0 or Vy is not allowed	=	0.032	um
SRC.7	Square 1.25xVn size, rectangular 1.25xVn is not allowed	=	0.04	um
SRC.8	Square 2xVn size	=	0.062	um
SRC.9	Square 10xTVn/UTV size	=	0.324	um
SRC.10	Square 14xTVn size	=	0.414	um
SRC.11	M0 slot, V0 slot, Vy slot, 1.25xVn slot, 2xVn slot and 10xTVn/14xTVn/UTV/PA slot and PPAA/M1/Mxy/1.25xMy/1.25xMn/2xMn/10xTMn (or 14xTMn) /UTM/ALPA slot must be drawn in seal ring region.			
SRC.12	Via slot enclosure by metal, except UTV	≥	0.11	um
SRC.12b	UTV slot enclosure by UTM	≥	0.45	um
SRC.12c	PA slot enclosure by ALPA	≥	0.9	um

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Rule number	Description	Opt.	Design Value	Unit
SRC.12d	V0 slot must be coincidence with M0 slot			
SRC.13	Seal ring must be a close ring excluding RF device (RFDEV region).			
SRC.14	Total seal ring MARKS width in orthogonal direction	=	21.6	um
SRC.15	Space between two square V0/Vy/1.25xVns/2xVns	≥	0.438	um
SRC.16	Space between two square 10xTVns/14xTVns/UTV	≥	0.5	um
SRC.17a	Width of M1/Mxy/1.25xMy/1.25xMn/2xMn/10xTMn/14xTMn/UTM/ALPA in orthogonal direction	≥	0.5	um
		≤	5	um
SRC.17b	Width of M1/Mxy/1.25xMy/1.25xMn/2xMn/10xTMn/14xTMn/UTM/ALPA at 45 degree angle area, DRC check parallel edge for ALPA	≥	0.5	um
		≤	7.08	um
SRC.18	Space between two M1/Mxys or two 1.25xMys/1.25xMns or two 2xMns	≥	0.45	um
SRC.18b	Space between two M0s	≥	0.9	um
SRC.18c	Space between two 10xTMns or two 14xTMns	≥	1.5	um
SRC.18d	Space between two UTM	≥	1.35	um
SRC.19	It is not allowed PPAA/GT/M0/M1/Mxy/1.25xMy/1.25xMn/2xMn/10xTMn/14xTMn/UTM/ALPA/V0/Vy/1.25xVn/2xVn/10xTVn/14xTVn/UTV/PA CUT MARKS. This rule also checks PPAA, GT, M0, metal, via dummy pattern (data type 1,7,8). V0/Vy/1.25xVn/2xVn/10xTVn/14xTVn/UTV definition is following main rule.			
SRC.20	Width of ((PPAA su 0.077) sd 0.077) in seal ring in orthogonal direction	=	15.11	um
SRC.21	Metal solid ring (all metal overlap region) enclosure by MARKS (DRC only check orthogonan direction)	=	2.7	um
SRC.22	MARKS inner edge enclosure of seal ring inner metal ring in orthogonal direction	≥	5.4	um
SRC.23	PA slot width in orthogonal direction	=	1.966	um

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Rule number	Description	Opt.	Design Value	Unit
SRC.24	ALPA ring width in orthogonal direction	=	4.0/5.0	um
SRC.25	Space between ALPA ring1 and ALPA ring2 in orthogonal direction	=	4.5	um
SRC.26	Maximum one MARKS is allowed in one chip			
SRC.27	MARKS outside edge must be coincidence with CHIPB			
SRC.28	M0 must overlap ((PPAA su 0.01um) NOT PPAA)			
SRC.29	ALL_GT density in MARKS region	≥	18%	

Note:

DRC need check AR_H layer ((18;0) OR 131;30)) and AR_V layer ((22;0) OR 131;31)).



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7.10 Analog layout guidelines

ACMK1(89;166) is the marker layer of analog design. For the analog design, recommend to follow below guidelines to achieve better analog device performance and matching. In analog circuit, good matching provides good performance margin and production yield.

7.10.1 Analog design layout guidelines

7.10.1.1 General Layout guidelines

Rule number	Description	Opt.	Design Value	Unit
AN.G.1 ^[NC]	Please don't use minimum widths and lengths in the high matching design.			
AN.G.2 ^[NC]	Recommended not to use a very long channel device the high speed design.			
AN.G.3 ^[NC]	Recommended to use simple shapes (rectangles) of AA and poly.			
AN.G.4 ^[NC]	Recommended to perform M1/ Mxy pre-coloring in the AC matching design.			
AN.G.5 ^[NC]	Recommended not to use maximum latch-up rule near narrow well space region.			
AN.G.6 ^[NC]	Recommended to avoid unbalanced DC bias stress during burn-in period for the sensitive circuit.			
AN.G.7 ^[NC]	Please make sure that the analog circuit operates at normal operational condition during burn-in.			
AN.G.8 ^[NC]	Recommended to use the protection diode connection in the sensitive circuit to reduce plasma induced damage.			



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7.10.1.2 MOS Layout guidelines

Rule number	Description	Ope	Design Value	Unit
AN.MOS.1 ^[NC]	For current mirror devices using common AA: 1. Keep the same SA/SB 2. Enlarge extension to put dummy gate at both S/D sides with the same channel width,length,pitch and count, as possible.			
AN.MOS.2 ^[NC]	Recommended not to use a large device by long poly, recommend metal routing rather than poly routing.			
AN.MOS.3 ^[NC]	Recommended GT width is equal to the MOS channel length., when use GT or dummy GT on STI to meet the spacing rule of neighboring to LAST GATE on the matching pair,			
AN.MOS.4 ^[NC]	Recommended to keep MOS total GTAE leakage as lower as possible in current mirror design.			
AN.MOS.5 ^[NC]	Recommended to put V0 overspread S/D, and stack V1 on top of V0 for high speed and high current device.			
AN.MOS.6 ^[NC]	Recommended to use stack gate to achieve low gds of longer channel.			
AN.MOS.7 ^[NC]	Recommened to use stack Gate with shorter channel lengh to get better or competitive performance in Id vartation and low gds.			
AN.MOS.8 ^[NC]	Recommended to use the optimized V0 number and the same M0-to-GATE and V0-to-GATE space at both S/D sides for critical devices.			
AN.MOS.9 ^[NC]	Recommended to use merged-AA than separated-AA or use symmetrical layout to reduce core device offset and Id variation.			

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7.10.1.3 Capacitor Layout guidelines

Rule number	Description	Opt.	Design Value	Unit
AN.CAP.1 ^[NC]	Recommended not to use long channel device in high speed design.			
AN.CAP.2 ^[NC]	Please use Varactor (NMOS capacitor in NW) as MOS capacitor. And the NW must have a P-type guard ring tied to ground.			
AN.CAP.3 ^[NC]	Recommended to use two varactors in parallel for adjusting C-V curve of MOS varactor in VCO differential structure.			
AN.CAP.4	Please use thick oxide (DG) MOS varactor and capacitor to reduce gate oxide leakage. DRC cannot check capacitor.			

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7.10.1.4 BJT Layout guidelines

Rule number	Description	Opt.	Design Value	Unit
AN.BJT.1^[NC]	Two kinds vertical bipolar are provided: PNP bipolar(P+/NW/PSUB) and NPN bipolar (N+/PW/DNW) respectively for core and IO bipola device.			
AN.BJT.2^[NC]	Recommended to use common central layout for BJT diodes and surrounding dummy pattern by SMIC utility			
AN.BJT.3^[NC]	Recommended current density range of BJT from 10nA/um ² to 10uA/um ² for better correlation between silicon and spice model.			

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7.10.1.5 Metal routing Layout guidelines

Rule number	Description	Opt.	Design Value	Unit
AN.MR.1^[NC]	Recommended to use rectangular or redundant vias for high current or resistance sensitive wire.			
AN.MR.2^[NC]	Recommended to use similar metal density for critical metal routing.			
AN.MR.3^[NC]	Recommended to use symmetrical routing for device matching.			
AN.MR.4^[NC]	Recommended to use shielded structure for high speed signal transmission to prevent crosstalk.			

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7.10.2 Device Placement and Matching guidelines

7.10.2.1 General guidelines

Rule number	Description	Opt.	Design Value	Unit
AN.GM.1^[NC]	Use simple rectangle AA for the matching pair.			
AN.GM.2^[NC]	Make sure the matching pairs shapes and areas are identical.			
AN.GM.3^[NC]	Place the matching pair close together and use "inter-digitated" or symmetric placement with symmetric surrounding.			
AN.GM.4^[NC]	Don't put the matching pairs at the corner or edge of the whole chip.			
AN.GM.5^[NC]	Recommended not to put PA over matching pairs.			
AN.GM.6^[NC]	Recommended to use PW strap to separate NWs at differenct net, it's better to use surrounding PW guard-ring.			
AN.GM.7^[NC]	Make sure local pattern density and surrounding of the matching pair should be identical.			
AN.GM.8^[NC]	Use enough dummy cells surrounding the matching pair.			
AN.GM.9^[NC]	Manually draw uniform dummy patterns surrounding the matching pair. The dummy patterns should be identical in the shape, the dimension, the space to the main circuit.			

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7.10.2.2 MOS Matching

Rule number	Description	Opt.	Design Value	Unit
AN.MOS.M.1 ^[NC]	ANMK0(GDS No:131;230): Marking layer for analog normal level matching device. ANMK1(GDS No:131;172): Marking layer for analog medium level matching device. ANMK2(GDS No:131;173): Marking layer for analog high level matching device.			
AN.MOS.M.2 ^[NC]	Recommended to use ANMK0, ANMK1, ANMK2 to mark the matching MOS array.			
AN.MOS.M.3	ANMK0, ANMK1, ANMK2 cannot overlap each other			
AN.MOS.M.4 ^[NC]	Recommended to use more identical dummy patterns surrounding higher level matching device.			
AN.MOS.M.5	Recommended pickup width.	≤	0.96	um
AN.MOS.M.6	Recommended spce between ANMK0/ ANMK1/ ANMK2 region and ALPA (CUT is not allowed).	≥	3	um
AN.MOS.M.7	Recommended ANMK0/ ANMK1/ ANMK2 enclosure ALPA.	≥	3	um
AN.MOS.M.8 ^[NC]	Recommended to put matching devices in the same AA, and fingers are uniform.			
AN.MOS.M.9 ^[NC]	Recommended to put at least two dummy polys with the same channel length in the same AA.			
AN.MOS.M.10 ^[NC]	Recommended to use the symmetrical V0 on M0, same M0 overlapping on AA, and the same M0 shape, sameV0 to GATE space for matching pairs.			
AN.MOS.M.11 ^[NC]	Interconnection routing design should be symmetrical.			
AN.MOS.M.12 ^[NC]	Poly GATE must connect to a protection diode by M1 to minimize the antenna effects in matching pairs.			
AN.MOS.M.13 ^[NC]	Recommended to use identical antenna diode and their metal routing.			
AN.MOS.M.14 ^[NC]	Recommended to use the same ENDCAP size for analog matching pair, including the dummy poly.			

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Rule number	Description	Opt.	Design Value	Unit
AN.MOS.M.15^[NC]	Recommend not to use a very long channel device to ensure the channel relaxation time of the MOS device is enough to build up charge to the steady state.			
AN.MOS.M.16^[NC]	Recommend to same drain and source orientation, and match the total number of D/S and S/D orientations.			
AN.MOS.M.17^[NC]	Recommend to equalize interconnect and GATE loading for matched transistors and tap the GATE connection from GATE both ends.			

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7.10.2.3 Resistor Matching

Rule number	Description	Opt.	Design Value	Unit
AN.RS.M.1 ^[NC]	Recommended to use interdigitated structure, dummy patterns, more V0, far away from power source for resistor matching.			
AN.RS.M.2 ^[NC]	Recommend to place DIRDMP with identical width surroundding high R resistor array in length direction, for high-matching resistor array applications.			
AN.RS.M.3 ^[NC]	Recommendedto use bigger resistor width for high-speed circuit, which can benifit better EM capability and smaller parasitic capacitance.			

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7.10.2.4 Capacitor Matching

Rule number	Description	Opt.	Design Value	Unit
AN.CAP.M.1^[INC]	Recommended MOS capacitor matching structure is identical with dummy patterns, without top metal routing, and far away from power source.			
AN.CAP.M.2^[INC]	Recommended varactor matching structure is interdigitated with dummy varactor cells, also far away from power source.			

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7.10.2.5 MOM Matching

Rule number	Description	Opt.	Design Value	Unit
AN.MOM.M.1^[NC]	Recommendation for MOM matching: -Inter-digitated structure -Uniform metal density -Dummy MOM unit surrounding MOM array -Away from different power region -Use MOM mismatch pair as close as possible.			
AN.MOM.M.2	MOM finger space. This rule is for performing same coloring to get better matching performance.	≥	0.063	um

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7.10.2.6 Metal routing

Rule number	Description	Opt.	Design Value	Unit
AN.MR.M.1^[NC]	Recommended not use routing metal over a matching pair, especially M1. If can't avoid, recommend to use identical routing metal with the same potential.			
AN.MR.M.2^[NC]	Recommended symmetrical metal routing layout and pattern density for the matching pair to reduce the Rs difference and avoid mismatch.			

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7.10.3 Noise

7.10.3.1 Power and Ground

Rule number	Description	Opt.	Design Value	Unit
AN.PG.N.1 ^[NC]	For the low noise circuit, recommended to use a PW ring connected to VSS to surround all PMOS devices in each analog circuit block.			
AN.PG.N.2 ^[NC]	For the low noise circuit, recommended to use a NW ring connected to VDD to surround all NMOS devices in each analog circuit block.			
AN.PG.N.3 ^[NC]	Recommneded to put NMOS in (NW hole in DNW) to benefit isolating critical circuit from substrate noise. Make sure every NW connected to DNW at same net			
AN.PG.N.4 ^[NC]	Recommneded to put PSUB (width \geq 1.5um) as a high resistance region to isolate two high frequency circuit, to reduce the noise or signal coupling from substrate. Minimize the signal lines crossing the high resistance PSUB region, and try to use upper level metal above PSUB.			
AN.PG.N.5 ^[NC]	Use separate power supplies and ground buses for the noisy and sensitive circuit and also for the analog and digital circuits.			
AN.PG.N.6 ^[NC]	Keep enough spacing between the noisy and sensitive area.			
AN.PG.N.7 ^[NC]	Use ground ring to stabilize substrate and well potential.			
AN.PG.N.8 ^[NC]	If transistor within sensitive circuit must be tied source with body together, must use longer metal line to connect them.			
AN.PG.N.9	Place high R resistor on a NW for better noise immunity.			

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7.10.3.2 Signal

Rule number	Description	Opt.	Design Value	Unit
AN.SIG.N.1 ^[NC]	Keep high frequency signal in high level metal layer.			
AN.SIG.N.2 ^[NC]	Use metal shield for victim line which is noise sensitive.			
AN.SIG.N.3 ^[NC]	Use metal shield for attacker line which travels through long distance.			
AN.SIG.N.4 ^[NC]	Use additional guard ring between seal-ring and I/O pads to isolate the coupling caused by the feedback path through chip seal-ring.			

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7.11 Reliability related guidelines

7.11.1 Current Density guidelines ^[NC]

7.11.1.1 Metal line/Via Current Density Rules

Metal Current Density Rules						
Rule number	Description			Operation	Current Density	Unit
	Layer	L(um)	W(um)			
CDR.1	M1	L≤5	Any width	≤	3x0.95xW	mA
CDR.2		L>5	W≥0.08	≤	2x0.95xW	mA
CDR.3			W<0.08	≤	1x0.95xW	mA
CDR.4	Mxy(1x)	L≤5	Any width	≤	3x0.95xW	mA
CDR.5		L>5	W≥0.08	≤	2x0.95xW	mA
CDR.6			W<0.08	≤	1x0.95xW	mA
CDR.7	1.25xMy	L≤5	Any width	≤	3x0.96xW	mA
CDR.8		L>5	W≥0.1	≤	2x0.96xW	mA
CDR.9			W<0.1	≤	1x0.96xW	mA
CDR.10	1.25xMn	L≤5	Any width	≤	3x1.10xW	mA
CDR.11		L>5	W≥0.1	≤	2x1.10xW	mA
CDR.12			W<0.1	≤	1x1.10xW	mA
CDR.16	2xMn	L≤4	Any width	≤	4x1.26xW	mA
CDR.17		L>4	W≥0.4	≤	2x1.26xW	mA
CDR.18		8≥L>4	W<0.4	≤	1.4x1.26xW	mA
CDR.19		L>8	W<0.4	≤	1x1.26xW	mA
CDR.28	10xTMn	L≤4	Any width	≤	4x9.30xW	mA
CDR.29		8≥L>4	Any width	≤	1.4x9.30xW	mA

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Metal Current Density Rules						
Metal current density is tested at 110°C						
Rule number	Description			Operation	Current Density	Unit
	Layer	L(um)	W(um)			
CDR.30		L>8	Any width	≤	1x9.30xW	mA
CDR.31	14xTMn	L≤4	Any width	≤	4x12.00xW	mA
CDR.32		8≥L>4	Any width	≤	1.4x12.00xW	mA
CDR.33		L>8	Any width	≤	1x12.00xW	mA
CDR.34	UTM	Any length	Any width	≤	38.00xW	mA
CDR.35	ALPA(14.5K)	Any length	Any width	≤	2.8xW	mA
CDR.36	ALPA(28K)	Any length	Any width	≤	5.08xW	mA
CDR.37a	M0	Any length	Any width	≤	12.08xW	mA
CDR.37b	M0G	Any length	Any width	≤	7.71xW	mA
CDR.37c	HiR	Any length	Any width	≤	0.390xW	mA

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Via Current Density Rules

Via current density is tested at 110°C

Rule number	Layer	Bottom Metal Via Landed on	Description				Operation	Current Density	Unit
			Bottom Metal Layer		Upper Metal Layer				
			L(um)	W(um)	L(um)	W(um)			
CDR.38a	V0 (0.032x0.032)	Landing on M0/M0G	Any length	Any width	L≤5	W<0.08	≤	3x0.0304	mA/via
CDR.38b			Any length	Any width	L≤5	W≥0.08	≤	3x0.0304	mA/via
CDR.38c			Any length	Any width	L>5	W≥0.08	≤	2x0.0304	mA/via (array)
CDR.38d			Any length	Any width	L>5	W≥0.08	≤	3x0.0304	mA/via (single via)
CDR.38e			Others		Others		≤	1x0.0304	mA/via
CDR.38f	RV0 (0.032x0.08)	Landing on M0/M0G	Any length	Any width	L≤5	Any width	≤	3 x0.0608	mA/via
CDR.38g			Any length	Any width	L>5	W≥0.08	≤	2 x0.0608	mA/via
CDR.38h			Others		Others		≤	1 x0.0608	mA/via
CDR.39	Vy (0.032x0.032)	landing on M1, Mxy (1x)	L≤5	Any width	L≤5	Any width	≤	3x0.0304	mA/via
CDR.40			L>5	W≥0.08	L≤5	Any width	≤	2x0.0304	mA/via
CDR.41			L≤5	Any width	L>5	W≥0.08	≤	2x0.0304	mA/via
CDR.42			Others		Others		≤	1x0.0304	mA/via
CDR.42a	RVy (0.032x0.08)	landing on M1, Mxy (1x)	L≤5	Any width	L≤5	Any width	≤	3 x0.0608	mA/via
CDR. 42b			L>5	W≥0.08	L≤5	Any width	≤	2 x0.0608	mA/via
CDR. 42c			L≤5	Any width	L>5	W≥0.08	≤	2x0.0608	mA/via
CDR. 42d			Others		Others		≤	1x0.0608	mA/via
CDR.43	1.25xVn (0.04x0.04)	landing on 1.25xM _y , 1.25xM _n	L≤4	Any width	L≤4	Any width	≤	3x0.0440	mA/via
CDR.44			L>4	W≥0.1	L≤4	Any width	≤	2x0.0440	mA/via

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Via Current Density Rules									
Rule number	Layer	Bottom Metal Via Landed on	Description				Operation	Current Density	Unit
			Bottom Metal Layer		Upper Metal Layer				
			L(um)	W(um)	L(um)	W(um)			
CDR.45			L≤4	Any width	L>4	W≥0.1	≤	2x0.0440	mA/via
CDR.46			Others		Others		≤	1x0.0440	mA/via
CDR.46a		1.25xRVn (0.04x0.1)	L≤4	Any width	L≤4	Any width	≤	3x0.0880	mA/via
CDR.46b			L>4	W≥0.1	L≤4	Any width	≤	2x0.0880	mA/via
CDR.46c			L≤4	Any width	L>4	W≥0.1	≤	2x0.0880	mA/via
CDR.46d			Others		Others		≤	1x0.0880	mA/via
CDR.65		2xVn (0.062x0.062)	L≤4	Any width	L≤4	Any width	≤	4x0.0781	mA/via
CDR.66			L>4	W≥0.1	L≤4	Any width	≤	2x0.0781	mA/via(array)
CDR.67			L≤4	Any width	L>4	W≥0.4	≤	2x0.0781	mA/via(array)
CDR.68			L≤4	Any width	8≥L>4	W≥0.4	≤	1.5x0.078 1	mA/via(single via)
CDR.69			L>4	W≥0.1	L>4	W≥0.4	≤	2x0.0781	mA/via(array)
CDR.70			L≤4	Any width	8≥L>4	W<0.4	≤	1.5x0.078 1	mA/via
CDR.71			L>4	W≥0.1	8≥L>4	W<0.4	≤	1.5x0.078 1	mA/via
CDR.72			Others		Others		≤	1x0.0781	mA/via
CDR.73		landing on 2xMn	L≤4	Any width	L≤4	Any width	≤	4x0.0781	mA/via
CDR.74			L>4	W≥0.5	L≤4	Any width	≤	2x0.0781	mA/via(array)
CDR.75			8≥L>4	W≥0.5	L≤4	Any width	≤	1.5x0.078 1	mA/via (single via)

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Via Current Density Rules

Via current density is tested at 110°C

Rule number	Layer	Bottom Metal Via Landed on	Description				Operation	Current Density	Unit
			Bottom Metal Layer	Upper Metal Layer	L(um)	W(um)			
CDR.76			L≤4	Any width	L>4	W≥0.5	≤	2x0.0781	mA/via(array)
CDR.77			L≤4	Any width	8≥L>4	W≥0.5	≤	1.5x0.0781	mA/via
CDR.78			L>4	W≥0.5	L>4	W≥0.5	≤	2x0.0781	mA/via(array)
CDR.79			8≥L>4	W≥0.5	8≥L>4	W≥0.5	≤	1.5x0.0781	mA/via
CDR.80			L≤4	Any width	8≥L>4	W<0.5	≤	1.5x0.0781	mA/via
CDR.81			L>4	W≥0.5	8≥L>4	W<0.5	≤	1.5x0.0781	mA/via
CDR.82			8≥L>4	W<0.5	8≥L>4	W<0.5	≤	1.5x0.0781	mA/via
CDR.83			8≥L>4	W<0.5	L≤4	Any width	≤	1.5x0.0781	mA/via
CDR.84			8≥L>4	W<0.5	L>4	W≥0.5	≤	1.5x0.0781	mA/via
CDR.85			Others		Others		≤	1x0.0781	mA/via
CDR.122	10xTVn (0.324x0.324)	landing on 1.25xMn	L≤4	Any width	L≤4	Any width	≤	3x1.1910	mA/via
CDR.123			L>4	W≥0.1	L≤4	Any width	≤	2x1.1910	mA/via(array)
CDR.124			L>4	W≥0.1	8≥L>4	Any width	≤	1.5x1.1910	mA/via
CDR.125			L≤4	Any width	8≥L>4	Any width	≤	1.5x1.1910	mA/via
CDR.126			Others		Others	Others		≤	1x1.1910

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Via Current Density Rules

Via current density is tested at 110°C

Rule number	Layer	Description				Operation	Current Density	Unit
		Bottom Metal Via Landed on	Bottom Metal Layer	Upper Metal Layer	W(um)			
CDR.132	landing on 2xMn	L≤4	Any width	L≤4	Any width	≤	4x1.4150	mA/via
CDR.133		L>4	W≥0.1	L≤4	Any width	≤	2x1.4150	mA/via(array)
CDR.134		8≥L>4	W≥0.1	L≤4	Any width	≤	1.5x1.4150	mA/via(single via)
CDR.135		L>4	W≥0.1	8≥L>4	Any width	≤	1.5x1.4150	mA/via
CDR.136		L≤4	Any width	8≥L>4	Any width	≤	1.5x1.4150	mA/via
CDR.137		8≥L>4	W<0.1	8≥L>4	Any width	≤	1.5x1.4150	mA/via
CDR.138		8≥L>4	W<0.1	L≤4	Any width	≤	1.5x1.4150	mA/via
CDR.139		Others		Others		≤	1x1.4150	mA/via
CDR.156	Landing on 10xMn	L≤4	Any width	L≤4	Any width	≤	4x3.3480	mA/via
CDR.157		L≤4	Any width	8≥L>4	Any width	≤	1.5x3.3480	mA/via
CDR.158		8≥L>4	Any width	8≥L>4	Any width	≤	1.5x3.3480	mA/via
CDR.159		8≥L>4	Any width	L≤4	Any width	≤	1.5x3.3480	mA/via
CDR.160		Others		Others		≤	1x3.3480	mA/via
CDR.166	14xTVn(0.414 x0.414)	L≤4	Any width	L≤4	Any width	≤	4x1.8000	mA/via
CDR.167		L>4	W≥0.1	L≤4	Any width	≤	2x1.8000	mA/via(array)
CDR.168		8≥L>4	W≥0.1	L≤4	Any width	≤	1.5x1.800	mA/via

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Via Current Density Rules

Via current density is tested at 110°C

Rule number	Layer	Bottom Metal Via Landed on	Description				Operation	Current Density	Unit
			L(um)	W(um)	L(um)	W(um)			
								0	(single via)
CDR.169			L>4	W≥0.1	8≥L>4	Any width	≤	1.5x1.8000	mA/via
CDR.170			L≤4	Any width	8≥L>4	Any width	≤	1.5x1.8000	mA/via
CDR.171			8≥L>4	W<0.1	8≥L>4	Any width	≤	1.5x1.8000	mA/via
CDR.172			8≥L>4	W<0.1	L≤4	Any width	≤	1.5x1.8000	mA/via
CDR.173		Landing on 10xMn, 14xMn	Others		Others		≤	1x1.8000	mA/via
CDR.182			L≤4	Any width	L≤4	Any width	≤	4x5.4000	mA/via
CDR.183			L≤4	Any width	8≥L>4	Any width	≤	1.5x5.4000	mA/via
CDR.184			8≥L>4	Any width	8≥L>4	Any width	≤	1.5x5.4000	mA/via
CDR.185			8≥L>4	Any width	L≤4	Any width	≤	1.5x5.4000	mA/via
CDR.186		UTV (0.324x0.324)	Others		Others		≤	1x5.4000	mA/via
CDR.187			L≤4	Any width	L≤4	Any width	≤	4x3.3480	mA/via
CDR.188			L≤4	Any width	8≥L>4	Any width	≤	1.5x3.3480	mA/via
CDR.189			8≥L>4	Any width	8≥L>4	Any width	≤	1.5x3.3480	mA/via
CDR.190			8≥L>4	Any width	L≤4	Any width	≤	1.5x3.3480	mA/via

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Via Current Density Rules

Via current density is tested at 110°C

Rule number	Description						Operati on	Current Density	Unit
	Layer	Bottom Metal Via Landed on	Botto m Metal Layer		Upper Metal Layer				
			L(um)	W(um)	L(um)	W(um)			
CDR.191			Others	Others			≤	1x3.3480	mA/via
CDR.192	(1.8x1.8)PA	Landing on 10xTMn,14xTMn,U TM	Any length	Any width	Any length	Any width	≤	5.0400	mA/via
CDR.193	(2.7x2.7)PA	Landing on 10xTMn,14xTMn,U TM	Any length	Any width	Any length	Any width	≤	13.7160	mA/via

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7.11.1.2 Metal line Irms definition and current density (AC)

$$I_{rms} = \sqrt{\frac{1}{t_w} \int_0^{t_w} i^2(t) dt}$$

Tw=Irms check period. Typically, current period.

i(t)= current

W(in um): the width of the metal line

ΔT (°C): the temperature rise due to Joule heating

Irms rule list below (width in um)

Layer	Operation	Irms(mA)	unit
M1	≤	SQRT(ΔT*(6.794*W^2+0.001*W))	mA
M2	≤	SQRT(ΔT*(4.929*W^2+0.001*W))	mA
M3	≤	SQRT(ΔT*(3.360*W^2+0.001*W))	mA
M4	≤	SQRT(ΔT*(2.895*W^2+0.001*W))	mA
M5	≤	SQRT(ΔT*(2.705*W^2+0.001*W))	mA
M6	≤	SQRT(ΔT*(2.572*W^2+0.001*W))	mA
M7	≤	SQRT(ΔT*(2.531*W^2+0.001*W))	mA
TM1	≤	SQRT(ΔT*(17.189*W^2+7.121*W))	mA
TM2	≤	SQRT(ΔT*(12.960*W^2+5.990*W))	mA
ALPA(14k)	≤	SQRT(ΔT*(10.42*W^2+38.73*W))	mA
ALPA(28k)	≤	SQRT(ΔT*(19.56*W^2+104.74*W))	mA
M0	≤	SQRT(ΔT*(2.433*W^2+0.676*W))	mA
M0G	≤	SQRT(ΔT*(1.244*W^2+0.575*W))	mA
HiR	≤	SQRT(ΔT*(0.00903*W^2+0.00294*W))	mA

It is recommended $\Delta T \leq 5C$, so the rule is below:

Layer	Operation	Irms(mA)	unit
M1	≤	SQRT(5*(6.794*W^2+0.001*W))	mA
M2	≤	SQRT(5*(4.929*W^2+0.001*W))	mA
M3	≤	SQRT(5*(3.360*W^2+0.001*W))	mA
M4	≤	SQRT(5*(2.895*W^2+0.001*W))	mA
M5	≤	SQRT(5*(2.705*W^2+0.001*W))	mA
M6	≤	SQRT(5*(2.572*W^2+0.001*W))	mA
M7	≤	SQRT(5*(2.531*W^2+0.001*W))	mA
TM1	≤	SQRT(5*(17.189*W^2+7.121*W))	mA
TM2	≤	SQRT(5*(12.960*W^2+5.990*W))	mA

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ALPA(14k)	\leq	SQRT($\Delta T * (10.42 * W^2 + 38.73 * W)$)	mA
ALPA(28k)	\leq	SQRT($\Delta T * (19.56 * W^2 + 104.74 * W)$)	mA
M0	\leq	SQRT($5 * (2.433 * W^2 + 0.676 * W)$)	mA
M0G	\leq	SQRT($5 * (1.244 * W^2 + 0.575 * W)$)	mA
HiR	\leq	SQRT($5 * (0.00903 * W^2 + 0.00294 * W)$)	mA

For AC current signal, should follow DC EM rules by using effective current I_{eff} .

I_{eff} rules are same to I_{max} rules, as well as the de-rating factors.

I_{eff} definition:

$$I_{eff} = \left[\left(\int_0^\tau I(t) dt \right) / \tau \right]$$

τ : the period of AC pulse

$I(t)$ = AC current signal

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7.11.1.3 Ipeak rules for metal or resistors

$I_{peak} = \max(|I(t)|)$, is the current at which a metal line or resistor begin to melt due to excessive Joule heating. This current should be used infrequently.

The limit for I_{peak} can be obtained below for frequency larger than 1 MHz and r larger than 0.05. If r smaller than 0.05, let r=0.05. r is duty ratio, t_d duration time, τ is period.

$$I_{peak} = \frac{I_{peak_DC}}{\sqrt{r}}, \quad r = \frac{t_d}{T},$$

If $t_d \geq 0.5 \mu s$, let: $I_{peak} = I_{peak_DC}$

The table below provides the I_{peak} rule at different pulse duration, duty ratio and metal width(W) in μm :

Metal Layer	Pulse duration (t_d)	Duty ratio (r)	I_{peak} (mA)	
			$W \geq 0.096 \mu m$	$W < 0.096 \mu m$
M0	$t_d \geq 0.5 \mu s$	any	NA	$54.62 * W$
	$1 ns \leq t_d < 0.5 \mu s$	$r \geq 0.05$	NA	$54.62 * W / (r)^{0.5}$
	$1 ns \leq t_d < 0.5 \mu s$	$r < 0.05$	NA	$54.62 * W / (0.05)^{0.5}$
	$100 ps \leq t_d < 1 ns$	$r \geq 0.05$	NA	$81.42 * W / (r)^{0.5}$
	$100 ps \leq t_d < 1 ns$	$r < 0.05$	NA	$81.42 * W / (0.05)^{0.5}$
	$t_d < 100 ps$	$r \geq 0.05$	NA	$102.99 * W / (r)^{0.5}$
	$t_d < 100 ps$	$r < 0.05$	NA	$102.99 * W / (0.05)^{0.5}$
MOG	$t_d \geq 0.5 \mu s$	any	NA	$34.57 * W$
	$1 ns \leq t_d < 0.5 \mu s$	$r \geq 0.05$	NA	$34.57 * W / (r)^{0.5}$
	$1 ns \leq t_d < 0.5 \mu s$	$r < 0.05$	NA	$34.57 * W / (0.05)^{0.5}$
	$100 ps \leq t_d < 1 ns$	$r \geq 0.05$	NA	$55.34 * W / (r)^{0.5}$
	$100 ps \leq t_d < 1 ns$	$r < 0.05$	NA	$55.34 * W / (0.05)^{0.5}$
	$t_d < 100 ps$	$r \geq 0.05$	NA	$70.91 * W / (r)^{0.5}$
	$t_d < 100 ps$	$r < 0.05$	NA	$70.91 * W / (0.05)^{0.5}$
M1,Mxy(1x)	$t_d \geq 0.5 \mu s$	any	$10.44 * W$	$18.03 * W$
	$1 ns \leq t_d < 0.5 \mu s$	$r \geq 0.05$	$10.44 * W / (r)^{0.5}$	$18.03 * W / (r)^{0.5}$
	$1 ns \leq t_d < 0.5 \mu s$	$r < 0.05$	$10.44 * W / (0.05)^{0.5}$	$18.03 * W / (0.05)^{0.5}$
	$100 ps \leq t_d < 1 ns$	$r \geq 0.05$	$14.01 * W / (r)^{0.5}$	$26.38 * W / (r)^{0.5}$
	$100 ps \leq t_d < 1 ns$	$r < 0.05$	$14.01 * W / (0.05)^{0.5}$	$26.38 * W / (0.05)^{0.5}$
	$t_d < 100 ps$	$r \geq 0.05$	$20.67 * W / (r)^{0.5}$	$35.92 * W / (r)^{0.5}$
	$t_d < 100 ps$	$r < 0.05$	$20.67 * W / (0.05)^{0.5}$	$35.92 * W / (0.05)^{0.5}$
My(1.25x)	$t_d \geq 0.5 \mu s$	any	$10.37 * W$	$21.38 * W$

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Metal Layer	Pulse duration (t_d)	Duty ratio (r)	I_{peak} (mA)	
			$W \geq 0.096 \mu m$	$W < 0.096 \mu m$
Metal Layer	1 ns $\leq t_d < 0.5 \mu s$	$r \geq 0.05$	$10.37 * W / (r)^{0.5}$	$21.38 * W / (r)^{0.5}$
	1 ns $\leq t_d < 0.5 \mu s$	$r < 0.05$	$10.37 * W / (0.05)^{0.5}$	$21.38 * W / (0.05)^{0.5}$
	100 ps $\leq t_d < 1 \text{ ns}$	$r \geq 0.05$	$13.91 * W / (r)^{0.5}$	$27.91 * W / (r)^{0.5}$
	100 ps $\leq t_d < 1 \text{ ns}$	$r < 0.05$	$13.91 * W / (0.05)^{0.5}$	$27.91 * W / (0.05)^{0.5}$
	$t_d < 100 \text{ ps}$	$r \geq 0.05$	$20.53 * W / (r)^{0.5}$	$40.12 * W / (r)^{0.5}$
	$t_d < 100 \text{ ps}$	$r < 0.05$	$20.53 * W / (0.05)^{0.5}$	$40.12 * W / (0.05)^{0.5}$
	$t_d \geq 0.5 \mu s$	any	$12.16 * W$	$23.47 * W$
Mn(1.25x)	1 ns $\leq t_d < 0.5 \mu s$	$r \geq 0.05$	$12.16 * W / (r)^{0.5}$	$23.47 * W / (r)^{0.5}$
	1 ns $\leq t_d < 0.5 \mu s$	$r < 0.05$	$12.16 * W / (0.05)^{0.5}$	$23.47 * W / (0.05)^{0.5}$
	100 ps $\leq t_d < 1 \text{ ns}$	$r \geq 0.05$	$16.31 * W / (r)^{0.5}$	$33.07 * W / (r)^{0.5}$
	100 ps $\leq t_d < 1 \text{ ns}$	$r < 0.05$	$16.31 * W / (0.05)^{0.5}$	$33.07 * W / (0.05)^{0.5}$
	$t_d < 100 \text{ ps}$	$r \geq 0.05$	$24.07 * W / (r)^{0.5}$	$46.72 * W / (r)^{0.5}$
	$t_d < 100 \text{ ps}$	$r < 0.05$	$24.07 * W / (0.05)^{0.5}$	$46.72 * W / (0.05)^{0.5}$
	$t_d \geq 0.5 \mu s$	any	$63.05 * W$	NA
TM(10x)	1 ns $\leq t_d < 0.5 \mu s$	$r \geq 0.05$	$63.05 * W / (r)^{0.5}$	NA
	1 ns $\leq t_d < 0.5 \mu s$	$r < 0.05$	$63.05 * W / (0.05)^{0.5}$	NA
	100 ps $\leq t_d < 1 \text{ ns}$	$r \geq 0.05$	$93.99 * W / (r)^{0.5}$	NA
	100 ps $\leq t_d < 1 \text{ ns}$	$r < 0.05$	$93.99 * W / (0.05)^{0.5}$	NA
	$t_d < 100 \text{ ps}$	$r \geq 0.05$	$118.89 * W / (r)^{0.5}$	NA
	$t_d < 100 \text{ ps}$	$r < 0.05$	$118.89 * W / (0.05)^{0.5}$	NA
	$t_d \geq 0.5 \mu s$	any	$58.5 * W$	NA
ALPA(14k)	$t_d < 0.5 \mu s$	$r \geq 0.05$	$58.5 * W / (r)^{0.5}$	NA
	$t_d < 0.5 \mu s$	$r < 0.05$	$58.5 * W / (0.05)^{0.5}$	NA
	$t_d \geq 0.5 \mu s$	any	$117.9 * W$	NA
ALPA(28k)	$t_d < 0.5 \mu s$	$r \geq 0.05$	$117.9 * W / (r)^{0.5}$	NA
	$t_d < 0.5 \mu s$	$r < 0.05$	$117.9 * W / (0.05)^{0.5}$	NA
	$t_d \geq 0.5 \mu s$	any	$2 * W$	NA
HiR	$t_d < 0.5 \mu s$	$r \geq 0.05$	$2 * W / (r)^{0.5}$	NA
	$t_d < 0.5 \mu s$	$r < 0.05$	$2 * W / (0.05)^{0.5}$	NA

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7.11.1.4 Temperature coefficient

Cu Temperature coefficient

Temperature C	100	105	110	115	120	125
Factor	2.149	1.459	1	0.692	0.484	0.341

For the other temperature, factor can be used the value of the higher temperature. For example, for temperature between 100~105, the value 1.459 can be used.

M0/M0G temperature coefficient

Temperature C	100	105	110	115	120	125
Factor	2.149	1.459	1	0.692	0.484	0.341

Aluminum(ALPA) temperature coefficient

Temperature C	70	85	100	110	125
Factor	3.443	2.097	1.329	1	0.6707

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7.11.2 Antenna design rules

The "Antenna Ratio Effect" is a common name for the effects of charge accumulation in isolated nodes of an integrated circuit during its processing. This effect is also sometimes called "Plasma Induced Damage"(PID) or "charging effect". In those cases that the discharging of the isolated nodes is done through the thin gate oxide of the transistor, it might cause damage to the transistors and degrade their performance.

Antenna Ratio effect generic prevention rules are intended to reduce gate oxide damage, which was caused when exposed Gate and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler-Nordheim tunneling current to flow through the oxide during high density plasma processing in chip fabrication. Given the known process charge fluency, a figure of exposed conductor area to transistor gate area ratio is determined which guarantees Gate Oxide Integrity (GOI) reliability requirements. Failure to consider antenna rules in a design may lead to either reduced performance in transistors exposed to process induced damage, or may lead to total failure if the antenna rules are seriously violated.

If gate oxide AA is pick up type and the GT is shorting to same pick up AA, then do not perform antenna rule check on this gate oxide.

Rule number	Description	Opt.	Design Value	Unit
ANT.GT1	Drawn ratio of Gate (GT NOT P2) perimeter area to the active IO gate area connected directly to it	≤	130	
ANT.GT2	Drawn ratio of Gate (GT NOT P2) top area to the active gate area (Core, IO) connected directly to it	≤	55	
ANT.GT3	Drawn ratio of M0/M0G area to the active gate area (Core, IO) connected directly to it	≤	110	
ANT.GT4a	When a protection diode is not used, the ratio of cumulative metal area to the core active gate area from M1 to TM (if double TM used, TM layer defined as TM2 layer)	≤	5000	
ANT.GT4b	When a protection diode is not used, the ratio of cumulative metal area to the IO active gate area from M1 to TM (if double TM used, TM layer defined as TM2 layer)	≤	1000	
ANT.GT5a	When a protection diode is used, the ratio of cumulative M1 to Mn (Mn is inter metal layer directly underneath TM) area to the active gate area connected directly to it	≤	diode area *450 +40000	
ANT.GT5b	When a protection diode is used, the ratio of single TM _n (n=1,2) area to the active GATE area connected directly to it	≤	diode area*7500 +45000	
ANT.GT6a	When the protection diode is not used, the drawn ratio of single layer Via area to the active GATE area connected directly to it	≤	20	

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Rule number	Description	Opt.	Design Value	Unit
ANT.GT6b	When the protection diode is not used, the drawn ratio of cumulative Via area to the IO active GATE area connected directly to it	\leq	50	
ANT.GT7	When the protection diode is used, the drawn ratio of cumulative Via area to the active GATE area connected directly to it.	\leq	diode area * 180 + 800	
ANT.GT8a	When the protection diode is not used, the drawn ratio of PA area to the IO active GATE area connected directly to it	\leq	20	
ANT.GT8b	When the protection diode is not used, the drawn ratio of PA area to the core active GATE area connected directly to it	\leq	200	
ANT.GT9a	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the IO active GATE area connected directly to it	\leq	1000	
ANT.GT9b	When the protection diode is not used, the drawn ratio of ALPA side-wall area to the core active GATE area connected directly to it	\leq	2000	
ANT.GT10	When the protection diode is used, the drawn ratio of PA area to the active GATE area connected directly to it	\leq	diode area * 90 + 400	
ANT.GT11	When the protection diode is used, the drawn ratio of ALPA side-wall area to the active GATE area connected directly to it.	\leq	diode area * 8500 + 30000	

A. The definition of GATE Perimeter area

GATE Perimeter Area = Lx t

L: GATE perimeter length connected to GATE

t : GATE thickness (1350A)

B. The definition of ALPA Perimeter area

ALPA Perimeter Area = Lx t

L: ALPA perimeter length connected to GATE

t: ALPA thickness (Two Options: 14.5KA and 28KA)

C. The definition of GATE Area

GATE Area = 0.05um*Channel length for 1fin device

GATE Area = 0.09um*Channel length for 2fin device

GATE Area = 0.16um*Channel length for 3fin device

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GATE Area = 0.23um*Channel length for 4fin device

GATE Area = 1.5*Channel width* Channel length for > 4fin device

Note: AA vertical edge need to extend 1/2 GT width for edge GATE Area definition

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7.11.3 ESD design rules and guidelines

The ESD guidelines are targeted to meet HBM-2KV(Human Body Mode) and MM-100V (Machine mode) spec according to EIA/JEDEC standard and EIA/JESD22 test standard, SMIC does not guarantee the final ESD device performance. If designers do not follow SMIC ESD guideline, chip level ESD test should be done for ESD verification.

7.11.3.1 DRC marker layer for ESD component

ESDIO2 (GDS No: 133;3) is DRC marking layer for ESD protection device including ESD STI diode, gated diode, drain ballasted MOS and big MOS used in power clamp. This layer should cover ESD protection device and its N and P guard rings, but non-ESD device inside the same guard ring should be excluded. Otherwise, all the devices and circuits inside ESDIO2 will be regarded as ESD transistors and may induce false DRC alarms. ESDIO2 should be drawn at each individual ESD protection device. Please refer to the examples in Fig.1

ESDCLP (GDS: 41;2) is a DRC marking layer for ESD RC-triggered power clamp structures connected to power supply pads. Please refer to the example in Fig.2

ESD5V (GDS: 133;1) is a DRC marking layer for HV tolerant ESD protection devices using cascaded N/PMOS. Please refer to the example in Fig.3.

DIOMK1 (GDS: 131;161) is a DRC marking layer for STI bounded ESD diode.

DIOMK2 (GDS: 131;162) is a DRC marking layer for ESD Gated diode.

DBESD2 (GDS: 133;11) is a DRC marking layer to recognize drain side of drain ballasted NMOS and cascaded NMOS.

DBESD (GDS: 133;10) is a DRC marking layer to recognize drain ballasted NMOS and cascaded NMOS.

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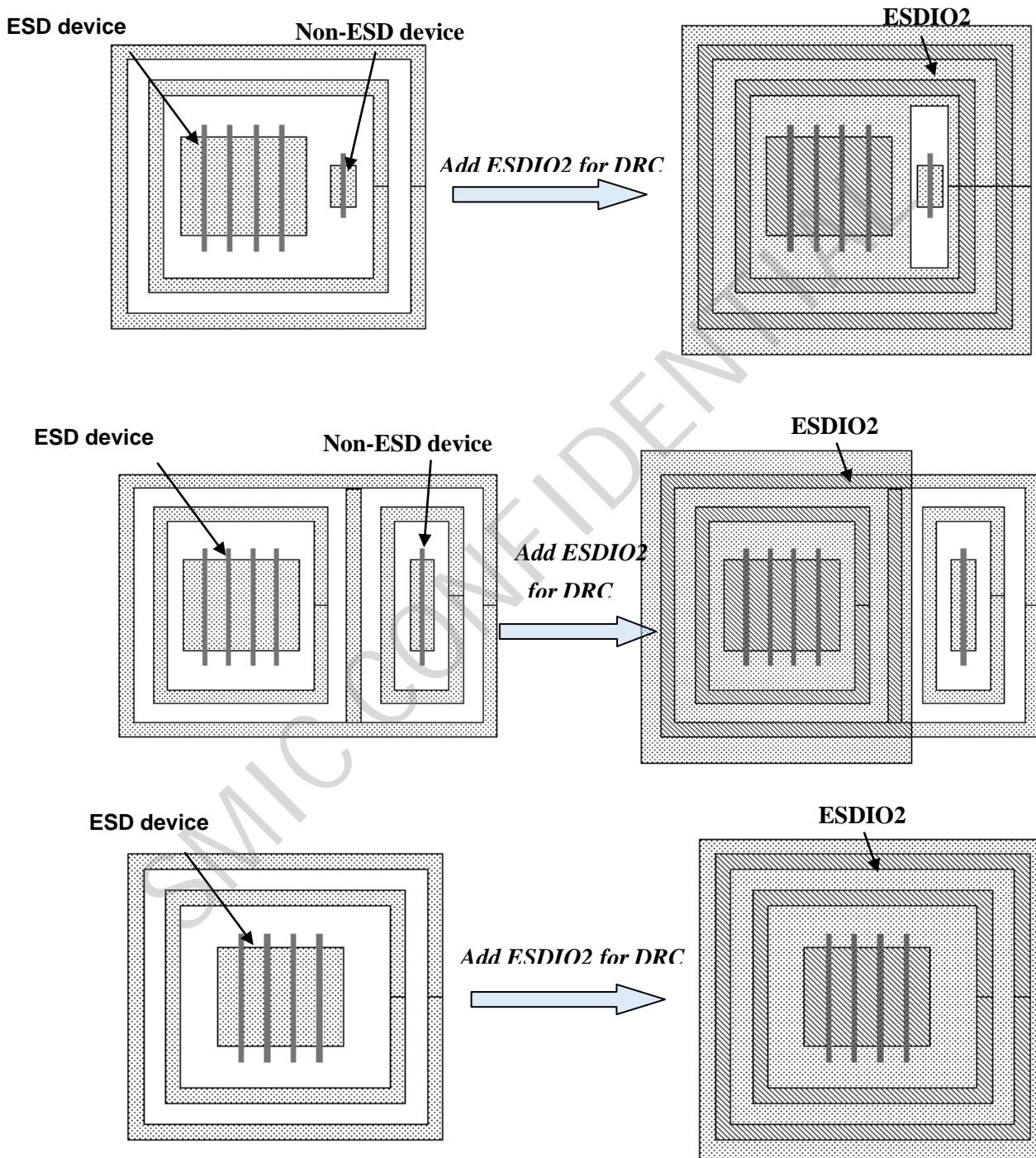


Fig.1 Examples of ESDIO2 for ESD DRC

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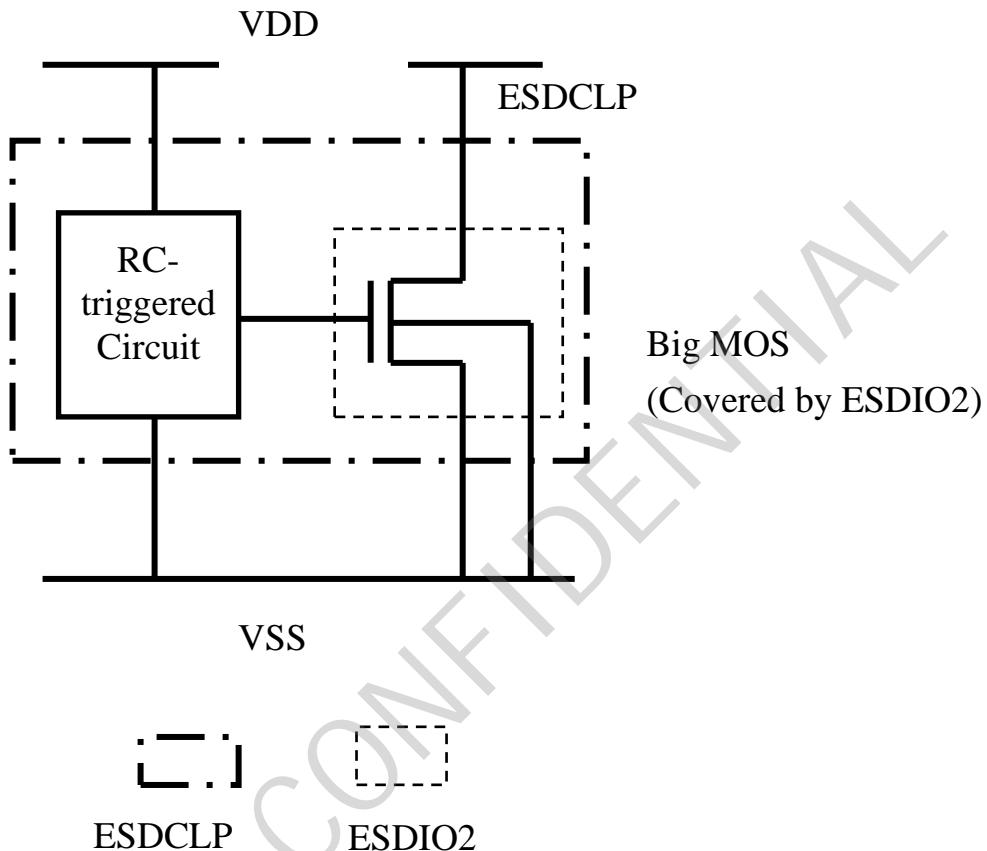


Fig.2 Power Clamp schematic

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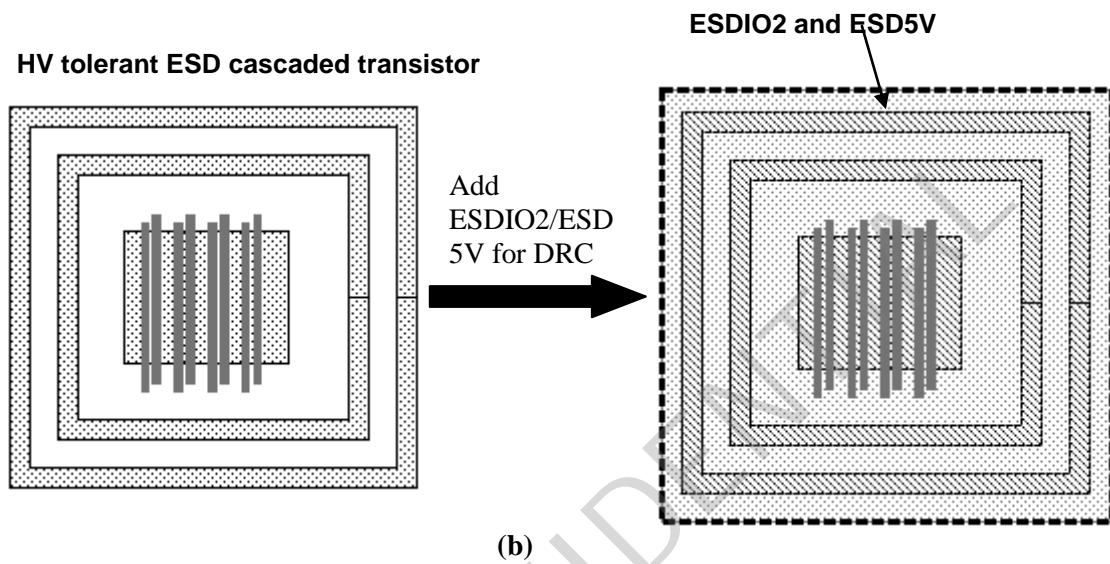


Fig.3 Examples of ESD5V for ESD DRC

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ESD Device Marker Layer Table:

Device	Marker Layer						
	ESDIO2 (133;3)	ESDCLP (41;2)	DBESD2 (133;11)	ESD5V (133;1)	DIOMK1 (131;161)	DIOMK2 (131;162)	DBESD (133;10)
DBNMOS	○	X	○	X	X	X	○
Cascaded NMOS	○	X	○	○	X	X	○
Cascaded PMOS	○	X	X	○	X	X	X
Power Clamp MOS	○	○	X	X	X	X	X
STI Diode	○	X	X	X	○	X	X
Gated Diode	○	X	X	X	X	○	X

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7.11.3.2 General ESD guidelines

Rule number	Description	Opt.	Design Value	Unit
ESD.1^[NC]	For I/O ESD protection, the primary ESD protection devices are required and can be designed as one of the following: 1) Drain Ballasted NMOS (DBNMOS) 2) STI diode 3) Gated diode 4) SCR ⁽¹⁾			
ESD.1a	ESD device must draw ESDIO2 (133;3) marker layer. Any one layer of ESDCLP (41;2), or DBESD2 (133;11), or ESD5V (133;1), or DIOMK1 (131;161), or DIOMK2 (131;162), or DBESD (133;10) must exist together with ESDIO2 (133;3).			
ESD.2^[NC]	Back to back diode is required to be placed to connect different VSS net.			
ESD.3^[NC]	For input pad ESD protection or high ESD risk of circuit, the secondary ESD protection is required to be added after a resistor R.			
ESD.4^[NC]	Apply the same kind of transistor for ESD protection, that is, use 0.8V transistor to design 0.8V power clamp and 0.8V primary ESD protection; use 1.8V transistor to design 1.8V power clamp and 1.8V primary ESD protection			
ESD.5^[NC]	Use 0.8V transistor to design 0.8V secondary ESD protection; use 1.8V transistor to design 1.8V secondary ESD protection			
ESD.6^[NC]	The secondary ESD protection can be designed as MOS based or diode (suggested: Gated diode or STI diode) based. If NMOS based, it needs to have GATE couple design. GGNMOS is not allowed.			
ESD.7^[NC]	Value of input resistor R between the Gated oxide of internal circuit and I/O pad. (Fig. 3)	\geq	200	Ω
ESD.8^[NC]	Channel length of 0.8V NMOS for secondary protection device	\geq	0.032	um
ESD.9^[NC]	Channel width of 0.8V NMOS for secondary protection device	\geq	7.968	um
ESD.10^[NC]	Channel length of 1.8V NMOS for secondary protection device	\geq	0.134	um
ESD.11^[NC]	Channel width of 1.8V NMOS for secondary protection device	\geq	3.984	um

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Rule number	Description	Opt.	Design Value	Unit
ESD.12^[NC]	Total perimeter of diode of diode based secondary ESD protection	\geq	7.998	um
ESD.13^[NC]	If Metal resistance from IO pad to 1 st ESD device is smaller than IO pad to internal device, Resistance of the power/ground bus metal line from the primary ESD device to the closest power clamp (R2+R3 and R4+R5)	\leq	1	Ω
ESD.14^[NC]	If Metal resistance from IO pad to primary ESD device is larger than IO pad to internal device, Resistance of the power/ground bus metal line from the IO pad to the closest power clamp (R1+R2+R3 and R1+R4+R5)	\leq	1	Ω
ESD.15^[NC]	Resistance of the bus metal line from the power pad to the closest GND pad(R6+R3+R5+R7). If R6+R3+R5+R7 is smaller than the resistance of power and ground pad to internal device, this rule can be waived.	\leq	1	Ω
ESD.16^[NC]	Resistance between different power clamp cell.	\leq	2	Ω
ESD.17^[NC]	Resistance for global bus metal between any Vdd/Vss net.	\leq	1	Ω
ESD.18^[NC]	It is not recommended to use core DBNMOS for primary ESD protection. Diode based primary ESD design is recommended.			

(1) If SCR based ESD protection design is used, please contact SMIC for more information.

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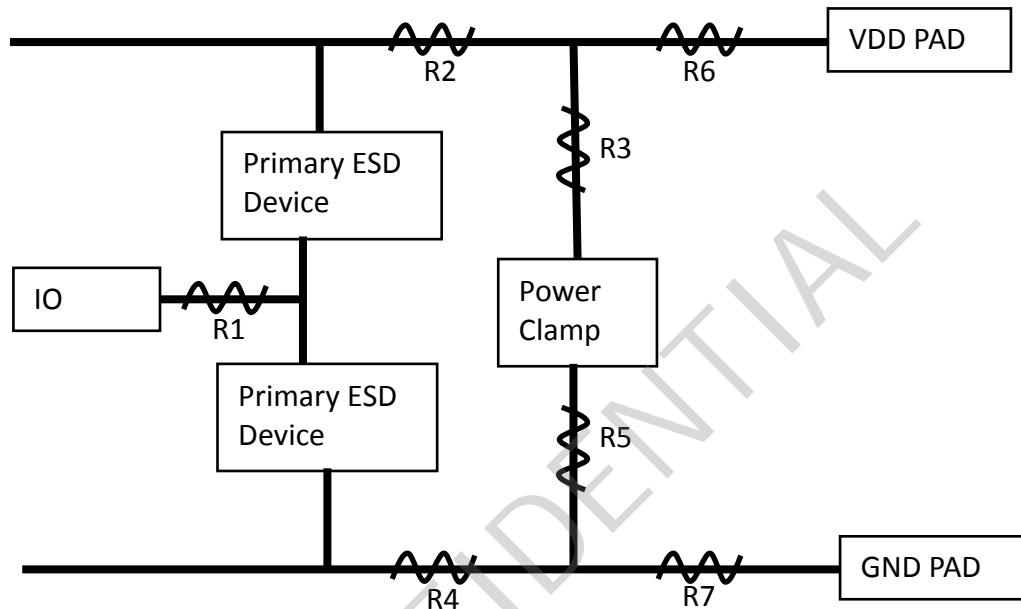


Fig.4 Bus Metal line design for ESD.13, ESD.14, ESD.15

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7.11.3.3 Guidelines for 1.8V Drain-Ballasted ESD NMOS

- The DBESD layer (GDS: 133;10) is used only for 1.8V drain ballasted NMOS and 1.8V cascaded NMOS. With this layer covered, some AA/GT/M0 rules can be waived. (GTDMP.R.2; GT.S.15g; GT.S.17f; GT.S.6)
- The DBESD2 layer (GDS:133;11) is used for recognizing drain side of 1.8V drain ballasted NMOS and cascaded NMOS.

Rule number	Description	Opt.	Design Value	Unit
ESD.19	DBESD width	\geq	0.2	um
ESD.20	DBESD space	\geq	0.2	um
ESD.21	DBESD extension outside of AA	\geq	0.046	um
ESD.21a	DBESD extension on (GT AND GTMK1) in S/D direction	\geq	0.064	um
ESD.22	Space between GTDMP and GT inside DBESD in S/D direction when GTDMP is inserted in drain	=	0.246~0.248	um
ESD.23	Maximum AA length in DBESD region	\leq	61	um
ESD.24	Channel width (W) of NMOS for ESD protection device (Channel width = Finger width*Finger No.)	\geq	548	um
ESD.25	Channel length of 1.8V NMOS for protection device	\geq	0.134	um
ESD.26	Space between M0 and GT at drain side of NMOS	=	0.16~0.162	um
ESD.27	Overlap of DBESD2 to GT at drain side	=	0.05,0.06	um
ESD.28	Space between GT at source side in DBESD	=	0.118, 0.119, 0.246~0.248	um

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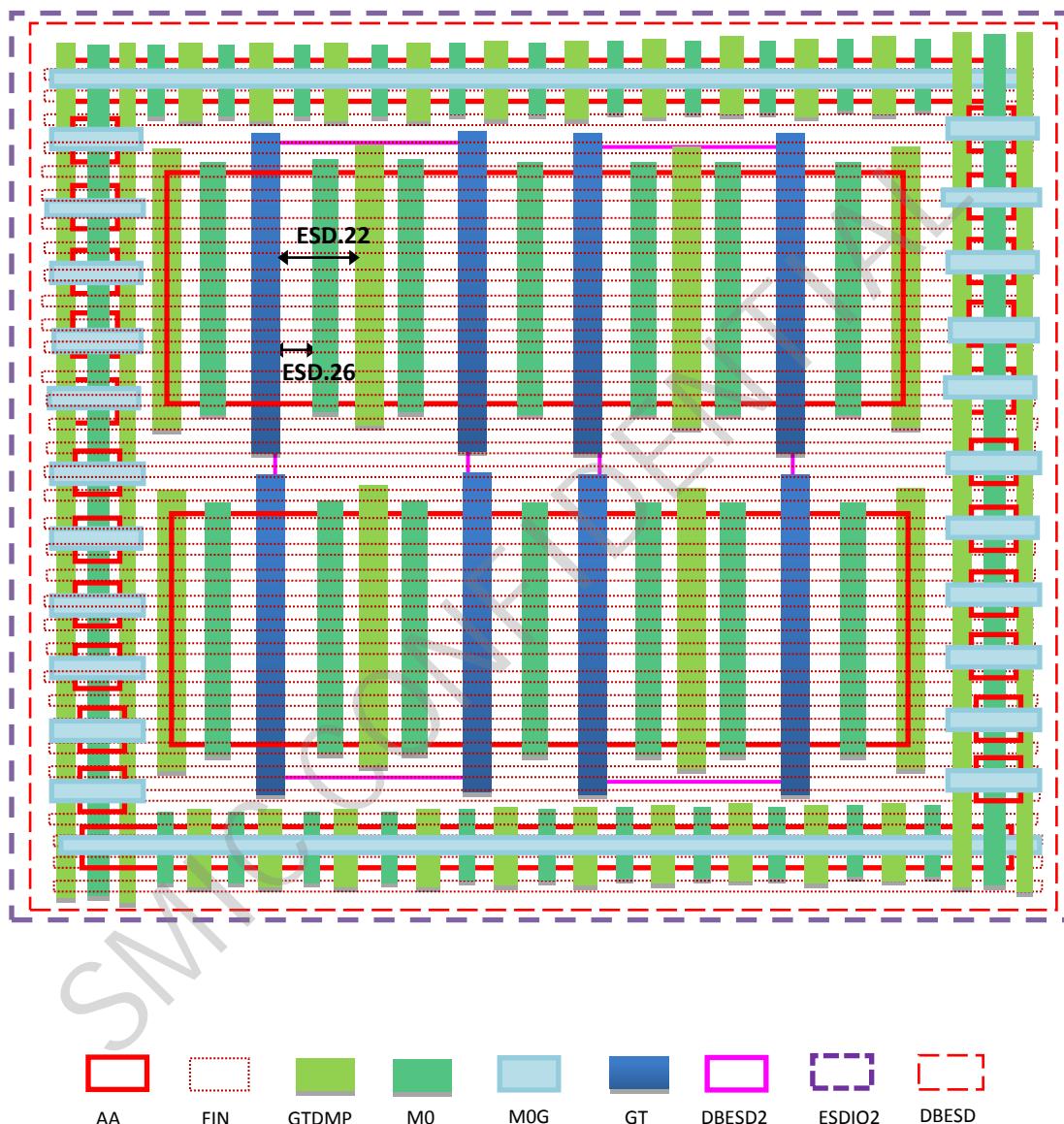


Fig.5 DBNMOS for I/O ESD protection

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7.11.3.4 Guidelines for Cascaded N/PMOS

- ESD5V (133; 1) is the marking layer to recognize cascaded N/PMOS

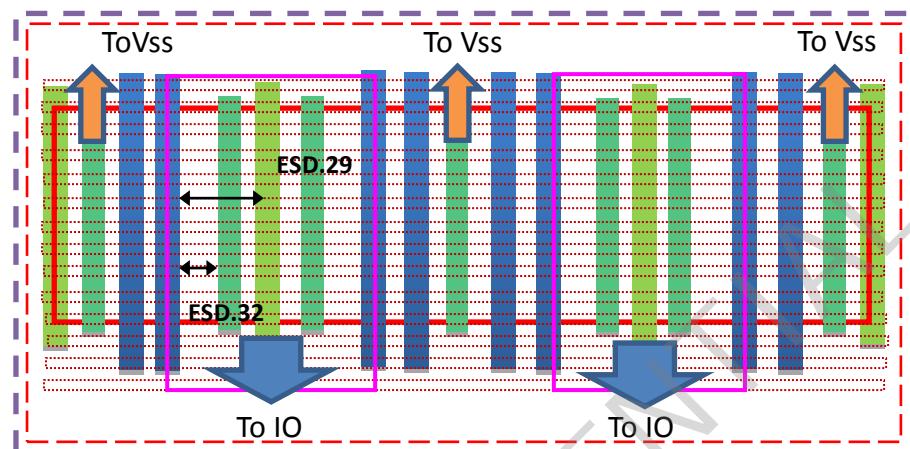
Rule number	Description	Opt.	Design Value	Unit
ESD.29	Space between GTDMP and GT inside DBESD in S/D direction when GTDMP is inserted in drain	=	0.246~0.248	um
ESD.30	Channel width (W) of NMOS for ESD protection device (Channel width = Finger width*Finger No.)	≥	548	um
ESD.31	Channel length of cascaded NMOS for protection device	≥	0.134	um
ESD.32	Spacing between M0 and GT at drain side of cascaded NMOS	=	0.16~0.162	um
ESD.33	When PMOS connected to IO pad, it must be cascaded PMOS to increase trigger voltage and avoid ESD current going through. This rule can be waived when dual diode based ESD protection is designed. (DRC will not check DIOMK1, DIOMK2, and PMOS after resistor)			

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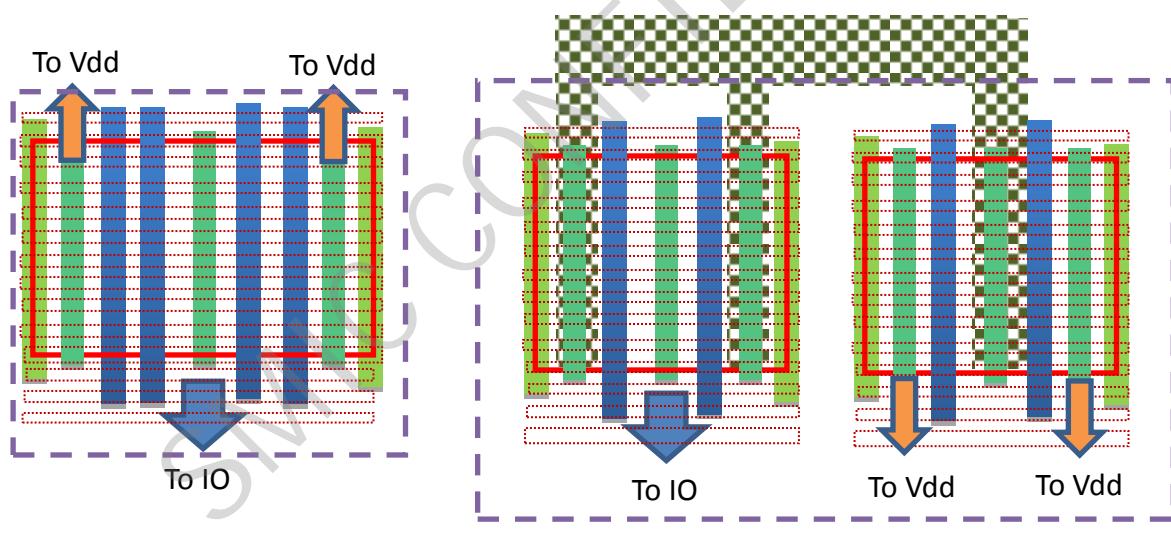
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Cascaded NMOS



AA	FIN	GTDOP	M0	MOG	GT	DBESD2	ESDIO2	DBESD

Two types of Cascaded PMOS

Fig.6 Layout of Cascaded MOS

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7.11.3.5 Power Clamp guidelines

- ESDCLP (41; 2) is the marking layer for ESD RC-triggered power clamp structures connected to a power supply pad.
- Power clamp includes one RC trigger circuit and one big MOS. The trigger circuit will turn on the big MOS during ESD even and keep the big MOS off at normal operation.
- DRC uses ((N+ AA and ESDCLP and ESDIO2) NOT INTERACT DBESD2) to recognize NMOS power clamp NMOS and ((P+ AA and ESDCLP and ESDIO2) NOT INTERACT DBESD2) to recognize PMOS power clamp PMOS.

Rule number	Description	Opt.	Design Value	Unit
ESD.34	ESD.34a ^(G) , ESD.34b ^(G) are defined for total channel width of Power Clamp N/PMOS. The total channel width is calculated by the ESD MOS in the same Source or Drain connection. With either one of calculated total channel width with the same source or drain connection larger than the defined value, DRC does not flag the violation. The connectivity can be formed by all metal, via, ALPA, PA but not broken by resistors.			
ESD.34a	Channel width (W) of 0.8V power clamp N/PMOS (Channel width = Finger width*Finger No.)	\geq	2798	um
ESD.34b	Channel width (W) of 1.8V power clamp N/PMOS (Channel width = Finger width*Finger No.)	\geq	2498	um
ESD.35a	Channel length (L) of 0.8V power clamp N/PMOS	$=$	0.07~0.13	um
ESD.35b	Channel length (L) of 1.8V power clamp N/PMOS	$=$	0.134~0.242	um

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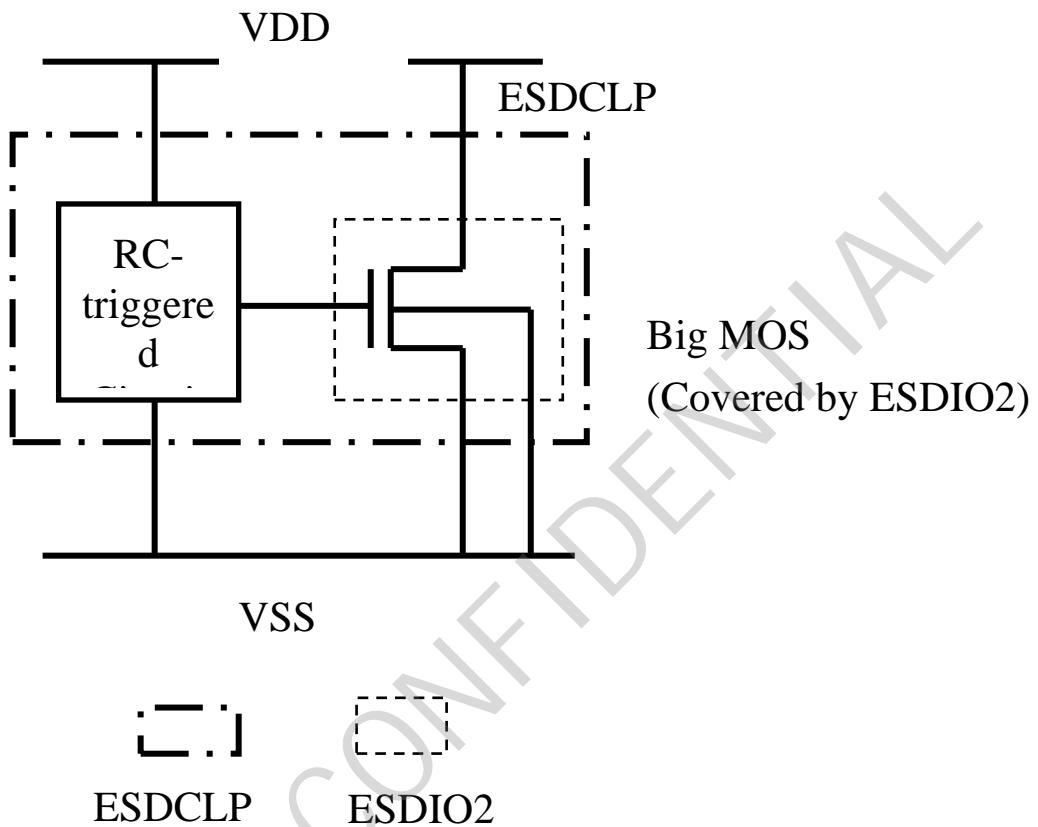


Fig.7 Power Clamp schematic

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7.11.3.6 ESD STI Diode guidelines

- DIOMK1 (131;161) is the marking layer for STI bounded diode. DRC uses (DIOMK1 AND ESDIO2) to recognize STI bounded diode for ESD protection.

Rule number	Description	Opt.	Design Value	Unit
ESD.36	N+AA or P+AA width inside ESD diode (W).	\geq	0.336	um
		\leq	0.576	
ESD.37	N+AA or P+AA length inside ESD diode (L).	\leq	42	um
ESD.38	Total perimeter of STI ESD diode $((L+W)*2)*N$ in the same connection to I/O Pad	\geq	298	um
ESD.39	Spacing between N+AA to P+ pickup AA in N+/PW diode or P+ AA to N+ pickup AA in P+/NW diode (S)	\leq	0.81	um
ESD.40	AOP_GT is must for ESD STI diode design, and AOP_GT width should be	$=$	0.086	um
ESD.41	Space between two AOP_GTs	$=$	0.118,0.119	um
ESD.42	All GT>DM need to be connected to their associated AA by M0G.			
ESD.43	STI diode for ESD protection should be covered by DG			

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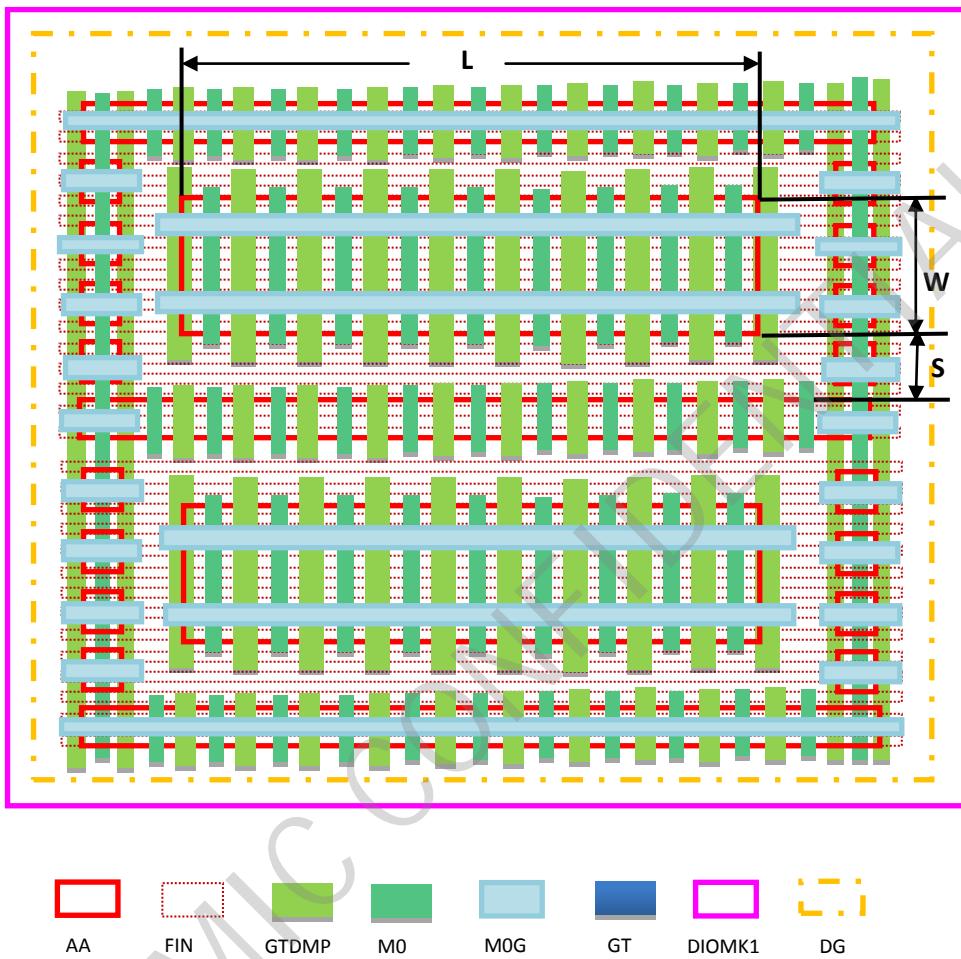


Fig. 8 ESD STI Diode

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7.11.3.7 ESD Gated Diode guidelines

- DIOMK2 (131;162) is the marking layer for poly bounded (Gated) diode. Please refer to 7.2.70 for Gated diode design. DRC uses (DIOMK2 AND ESDIO2) to recognize poly bounded diode for ESD protection.

Rule number	Description	Opt.	Design Value	Unit
ESD.44	Total perimeter of ESD Gated diode in the same connection to I/O pad (H*2*N).	\geq	248	um
ESD.45	Gated diode cannot be used for >1.98V (1.8V+10%) application.			
ESD.46	GT of Gated diode should be floating.			
ESD.47	The number of GTs in one AA inside DIOMK2	\leq	130	

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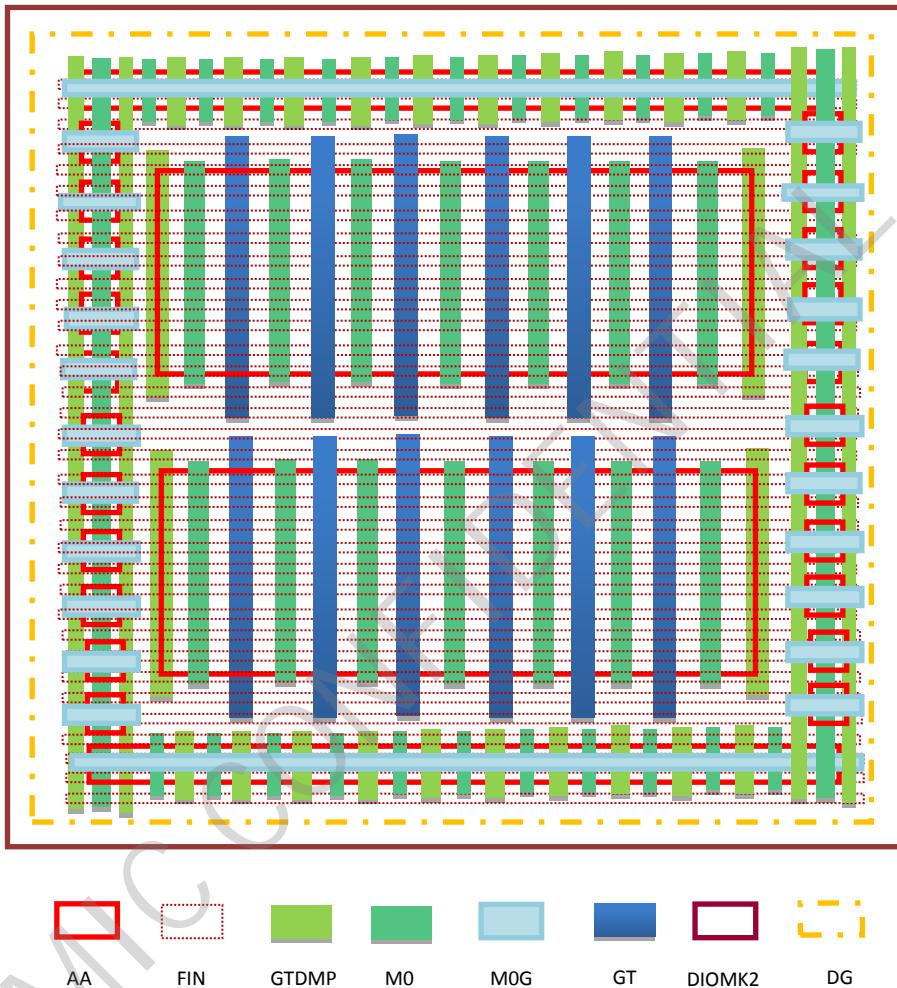


Fig. 9 ESD Gated Diode

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7.11.3.8 CDM protection for interface cross different Vdd/Vss net

To prevent CDM damage at the interface cross different Vdd/Vss net, the layout guideline for interface CDM protection design needs to be followed.

Rule number	Description	Opt.	Design Value	Unit
ESD.48^[NC]	For different Vdd/Vss net with separated grounds, either MOS based or diode based secondary ESD protection with interface resistor is required at interface. Please refer to Fig.10. The interface protection is not required for below two cases: <ol style="list-style-type: none">1. If different net is using common ground.2. If the receiver net is IO device.			
ESD.49^[NC]	Total Width of secondary MOS device.	\geq	7.968	um
ESD.50^[NC]	Channel length of secondary MOS device	\leq	0.032	um
ESD.51^[NC]	Total perimeter of secondary diode device	\geq	7.998	um
ESD.52^[NC]	The secondary NMOS device needs to have gate couple design. GGNMOS is not allowed.			
ESD.53^[NC]	Recommend interface resistor resistance	\geq	200	Ω

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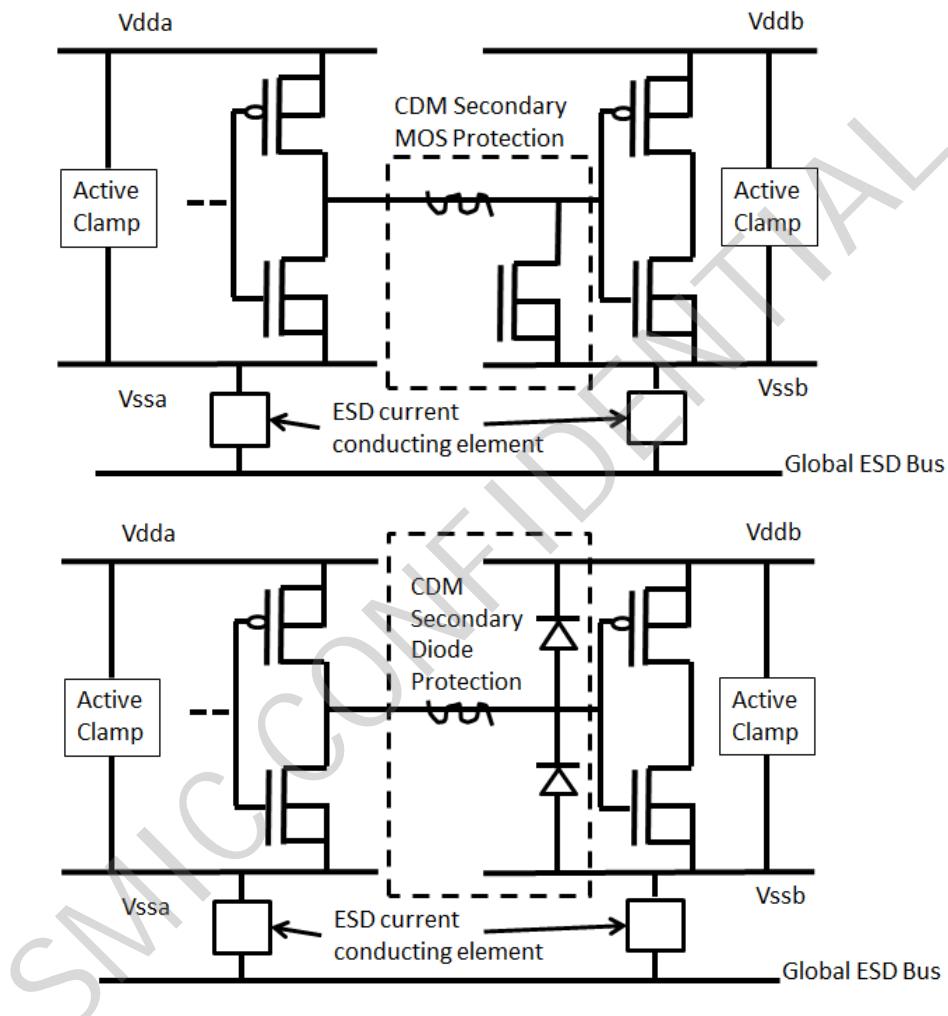


Fig.10 MOS based and Diode based interface CDM protection cross different Vdd/Vss net

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7.11.3.9 ESD Back-End Reliability guidelines

This section provides maximum current density of M0, via, metal line and resistor under ESD stress condition. Maximum current density is extracted from TLP (Transmission Line Pulse) test results.

Minimum Current for ESD Device:

Rule number	Description	Opt.	Design Value	Unit
ESD.54^[NC]	Minimum ESD current for the primary ESD protection	≥	1.33	A
ESD.55^[NC]	Minimum ESD current for the secondary ESD protection	≥	0.012	A

Maximum Current Density for BEOL :

BEOL Layer	Maximum Current density	Unit
High R Resistor	2.5	mA/um
M0	500	mA/um ²
1x Metal	60	mA/um
1.25x Metal	75	mA/um
2x Metal	110	mA/um
10x Metal	450	mA/um
14x Metal	600	mA/um
UTM Metal	1700	mA/um
ALPA	750	mA/um
V0	18	mA/via
1x Via	18	mA/via
1.25x Via	20	mA/via
2x Via	20	mA/via
10x Via	180	mA/via
14x Via	280	mA/via

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BEOL Layer	Maximum Current density	Unit
UTV	120	mA/via
PA	1.8	A/via

Below table shows the 1x to 1.25x Metal length/width effect. For smaller metal width and length, the ESD current density rule can be relaxed. We can use higher current density by multiplying the ratio value and maximum current density value from above table. Metal length refers to the direction parallel to current direction; Metal width refers to the direction perpendicular to current direction.

BEOL Layer	Metal Length L (um)	Unit Metal Width W (um)	Ratio
1x/1.25x Metal Layer	L < 0.5	W < 0.18	2.2
		0.18 ≤ W ≤ 0.55	1.8
		W > 0.55	1.4
	0.5 ≤ L ≤ 1	W < 0.18	2
		0.18 ≤ W ≤ 0.55	1.6
		W > 0.55	1.2
	L > 1	W < 0.18	1.5
		0.18 ≤ W ≤ 0.55	1.25
		W > 0.55	1

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7.11.4 Latch-Up(85°C) prevention layout guidelines

7.11.4.1 Definition of nomenclature in latch up(85°C) guidelines

Name	Definitions
I/O pads	Pads except Vdd pad, Vss pad.
Power Pads	Vdd pad, Vss pad
Internal Circuit	All devices do not connect to IO pad.
Guard-ring	Complete un-broken ring-type AA and M1 with M0 and V0 as many as possible, connected to Vdd or Vss
P+ guard-ring	Complete un-broken ring-type ((SP AND AA) NOT NW) and M1 with M0 and V0 as many as possible, connected to Vss.
N+ guard-ring	Complete un-broken ring-type ((SN AND AA) AND NW) and M1 with M0 and V0 as many as possible, connected to Vdd.
AA injector	Any AA directly connected to I/O pad, ex. MOS, diode, AA resistor, and well resistor directly connected to I/O pad.
IO Anode	((SP AND AA) AND NW) NOT GT directly connected to I/O pad
IO Cathode	((SN AND AA) NOT NW)NOT GT directly connected to I/O pad
Power Anode	((SP AND AA) AND NW) NOT GT directly connected to Vdd/Vss pad
Power Cathode	((SN AND AA) NOT NW)NOT GT directly connected to Vdd/Vss pad
PW Anode	PW in DNW directly connected to Vdd/Vss pad
NW Cathode	NW directly connected to Vdd/Vss pad

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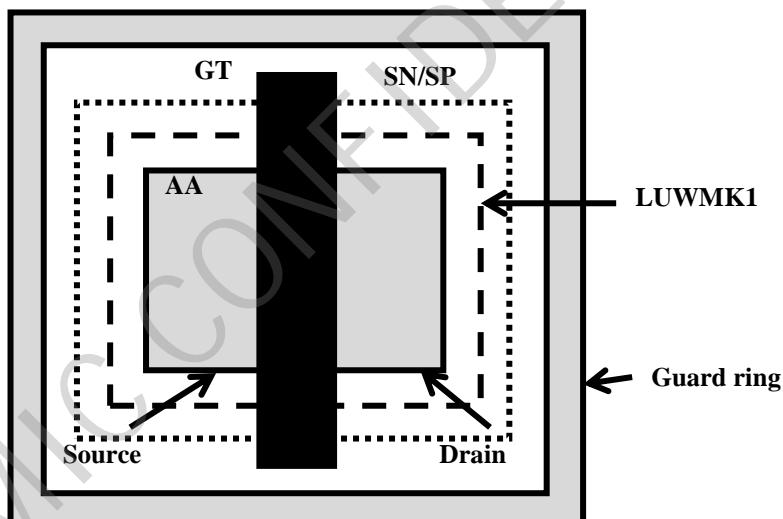
7.11.4.2 Definition of Latch up Dummy Layer

LUWMK1 (131;177) is a dummy layer for designer to waive latch up rules (LU.1~LU.3)

Note:

- 1) DRC will not check the area which is blocked by LUWMK1.
- 2) It will have risk if designer draw this layer to exempt latch up rule check without silicon proven of package level latch up test.
- 3) This layer is for DRC use, not a tape out required CAD layer.
- 4) Designer need to follow the following guidelines to draw LUWMK1.

Draw LUWMK1 to fully cover AA injector, including the source, gate, drain, diode and resistor, but not necessarily to cover well pickup and guard-ring.



LUAREA1 (131;161) is a dummy layer for designer to trigger area I/O latch up rule check. LUAREA1 need to fully cover AA injector, but not necessarily to cover well pickup and guard-ring.

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7.11.4.3 Connectivity Check

RES2H (131;178) is a DRC marking layer to identify resistor with resistance larger than 200ohm. If the resistance of used resistors between PAD and AA injector is larger than 200ohm, the marking layer RES2H (131;178) should be cover on the resistor. Latch up rule check connection will be broken by resistors with RES2H layer.

RESH(131;179) is a DRC marking layer to identify resistor with resistance below 200ohm, but customer consider it is safe to break connectivity for latch up check.

DRC use the following features to check the connectivity:

- 1) The connectivity is formed by metal, via, ALPA, PA.
- 2) If resistors with RES2H (131;178) and RESH(131;179) including AA resistor, Hi-R resistor, well resistor are between PAD and AA injector, the connection is broken.
- 3) The DRC switch of #CONNECT_ALL_RESISTOR (to connect AA resistor, Hi-R resistor, well resistor between PAD and AA injector) can control the connectivity of resistor. If #CONNECT_ALL_RESISTOR is on, the RES2H and RESH layer will not break the connection. This switch is off by default.
- 4) DRC runset provides the following options for designer's control.

Option	Turn on CONNECT_ALL_RESISTOR
A	No (default)
B	Yes

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7.11.4.4 DRC use the following features to identify the Power PAD and I/O PAD.

- 1) DRC will recognize the PAD by MD layer with Metal, via, PA, ALPA layers connectivity
- 2) DRC will recognize Power PAD and IO PAD according to the below methodology definition under #DEFINE_LU_BY_TEXT switch control.

Power net and IO net are taken as Power PAD and IO PAD respectively. In this case, even if a net is not connected to a real PAD(MD), the Power net will be taken as a Power PAD and IO net as IO PAD equivalently.
- 3) Latch up check when #DEFINE_LU_BY_TEXT switch turn off
 - a. Priority: IOMK1 > VDDMK1/VSSMK1 > N+ pickup/P+ pickup
pickup includes normal pickup, strap and guard ring type
 - b. DRC will recognize the IO PAD/net by M1 layer which overlap with IOMK1.
 - c. DRC will recognize the Power PAD which overlap with VDDMK1/VSSMK1
 - d. DRC will recognize the Power PAD which connected to Pick-up. In this case, Power PAD connect to N+ Pick-up AA will be taken as VDD PAD and Power PAD connect to P+ Pick-up AA as VSS PAD
 - e. If a PAD is not check out as case b/c/d, will be taken as IO PAD
- 4) Latch up check when #DEFINE_LU_BY_TEXT switch turn on(Default option)
 - a. Priority: Power text > IO text > IOMK1 > VDDMK1/VSSMK1 > N+ pickup/P+ pickup
pickup includes normal pickup, strap and guard ring type
 - b. DRC will recognize the Power net with label of top level Power text of all metal and metal text layers. These label text should overlap with its own metal layer, for example, M1TXT on M1 pattern, M2TXT on M2 pattern...
 - c. DRC will recognize the IO net with label of top level IO text of all metal and metal text layers. These label text should overlap with its own metal layer, for example, M1TXT on M1 pattern, M2TXT on M1 pattern...
 - d. DRC will recognize the IO PAD/net by M1 layer which overlap with IOMK1.
 - e. DRC will recognize the Power PAD which overlap with VDDMK1/VSSMK1
 - f. DRC will recognize the Power PAD which connected to Pick-up. In this case, Power PAD connect to N+ Pick-up AA will be taken as VDD PAD and Power PAD connect to P+ Pick-up AA as VSS PAD. If Power PAD connect to both N+ Pickup AA and P+ Pick-up AA, it will be considered as VSS PAD.
 - g. If a PAD is not check out as case b/c/d/e/f, will be taken as IO PAD
 - h. Default Power text name are "?VDD?", "?VCC?", "?VSS?", "?GND?", but no default IO text. User can define both Power text and IO text in DRC utility.

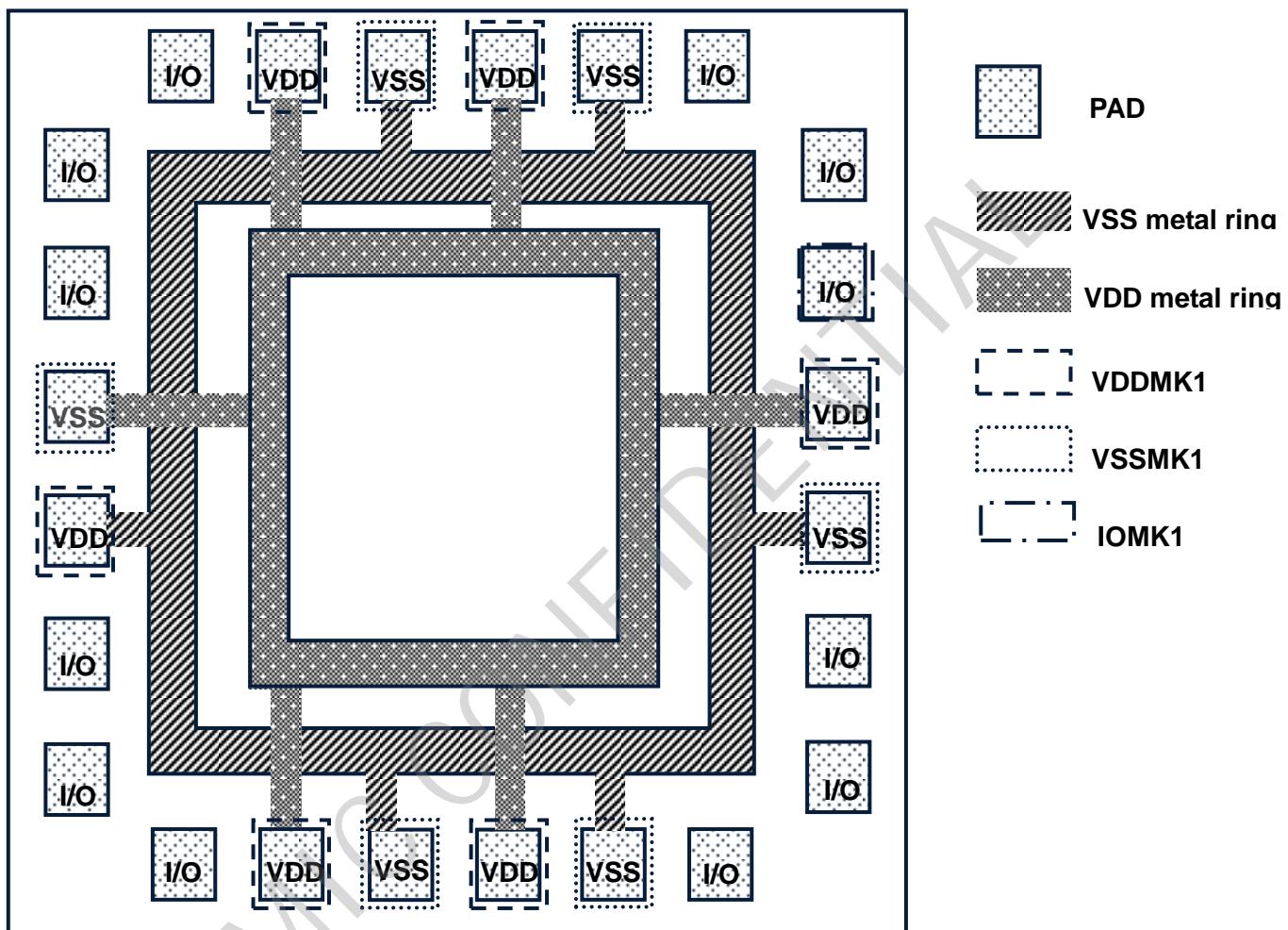
Priority:

Switch setting	Check Priority
(DEFINE_LU_BY_TEXT ON)	Power text > IO text > IOMK1 > VDDMK1/VSSMK1 > N+ Pickup/P+ Pickup
(DEFINE_LU_BY_TEXT OFF)	IOMK1 > VDDMK1/VSSMK1 > P+ Pickup > N+ Pickup

Except for the recognized Power PAD, all the other pads are defined as I/O PAD.

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7.11.4.5 DRC Methodology for Delta Voltage

DRC uses below options for voltage recognition:

- 1) Use Metal voltage top text layer (Mx_V_Hi/Lo_TOP), detailed GDS number please refer to SMIC CAD layer mapping table.
- 2) Use Metal voltage marking layer (Mx_V_Hi/Lo), detailed GDS number please refer to SMIC CAD layer mapping table.
- 3) Use detail Metal voltage marking layer (examples: M1_V18, M2_0d8V, etc), detailed GDS number please refer to SMIC CAD layer mapping table.

Latch up DRC checking flow:

- 1) Voltage rating for all devices connected to IO and power pad need to be identified.
- 2) Identify IO Anode/Cathode, Power Anode/Cathode, PW Anode, NW Cathode.
- 3) If anode voltage > cathode voltage, perform latch up check, otherwise do not perform checking.
- 4) If anode interacts with Mx_V_Hi_TOP or Mx_V_Hi and cathode interacts with Mx_V_Lo_TOP or Mx_V_Lo, perform latch up checking, otherwise do not perform checking.
- 5) Voltage drop between anode and cathode will decide the spacing rule of LU.4.x.

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7.11.4.6 General Latch Up(85°C) Rule

Rule number	Description	Opt.	Design Value	Unit
LU.1	<p>Guard ring should be used to surround AA injector or a group of AA injectors which are connected to an I/O pad, except OCCDFH region.</p> <p>N+ AA injector must be surrounded by a P+ guard-ring.</p> <p>P+ AA injector must be surrounded by a N+ guard-ring.</p> <p>NW/PW pickups rings can be used as guard rings.</p>			
LU.1.1 ^[NC]	<p>One additional PW strap and one additional NW strap are required to be inserted between the guard-rings of LU.1.1, PW strap is in between N+ guard-ring and NW strap, PW strap is in between P+ guard-ring and PW strap.</p>			
LU.1.2	<p>If Delta V ≥ 2.5V, one additional P+ guard-ring and one additional N+ guard-ring are required to be inserted between the guard-ring of LU.1.1.</p>			
LU.2	<p>Within 14.976um from AA injector, a NMOS group must be surrounded by a P+ guard-ring; a PMOS group must be surrounded by a N+ guard-ring.</p> <p>The following cases are excluded:</p> <ol style="list-style-type: none"> 1. The MOS AA is covered by LUWMK1. 2. The MOS AA is floating. (DRC recognize MOS AA without V0 connection as floating MOS AA) 3. The NMOS is inside DNW, and this DNW does not physically interact with PMOS NW. At the same time, voltage of the DNW ≥ voltage of PMOS NW. 4. OCCDFH region 			
LU.3	<p>Within 14.976um from AA injector, if two NW are with different potential, a PW strap must be inserted between these NWs, (DRC only check NWs space ≤ 29.952um), except OCCDFH region</p>			
LU.4.1	<p>Space between IO Anode and IO Cathode, needs to follow latch up space rule table</p>	≥	Latch Up Space Rule Table	um
LU.4.2	<p>Space between IO Anode and Power Cathode, needs to follow latch up space rule table.</p>	≥	Latch Up Space Rule	um

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	The following case can be excluded: NMOS is inside DNW, and this DNW does not physically interact with PMOS NW. At the same time, voltage of the DNW \geq voltage of PMOS NW		Table	
LU.4.3	Space between IO Anode and IO NW Cathode, IO (PW in DNW) Anode and IO Cathode, need to follow latch up space rule table.	\geq	Latch Up Space Rule Table	um
LU.4.4	Within 14.976um from AA injector, space between Power Anode and IO NW Cathode and space between IO (PW in DNW) cathode and Power cathode need to follow latch up space rule table.	\geq	Latch Up Space Rule Table	um
LU.5	Space (S2) from any point within the S/D region to the nearest pickup AA region inside the same well for I/O and internal circuits. (Fig.2). Except OCCDFH region	\leq	50	um
LU.6 ^[NC]	All the guard rings and pickups should be connected to VDD/VSS with low series resistance. Contacts and Vias should be used as many as possible.			
LU.6.1	Guard-ring width of LU.1,	\geq	0.192	um
LU.6.2 ^[NC]	Additional NW and PW strap width of LU.1.1	\geq	0.096	um
LU.6.3	Guard-ring width of LU.2	\geq	0.096	um
LU.6.4 ^[NC]	PW strap width of LU.3	\geq	0.096	um
LU.6.5	DRC will recognize a complete guard-ring when AA space \leq 0.576um and parallel run length \geq 0.192um.			

Latch Up Space Rule Table for LU.4.x

Voltage Drop	Space between Anode and Cathode (um)
$0V < \Delta V \leq 1V$	0.96
$1V < \Delta V \leq 1.32V$	1.824
$1.32V < \Delta V \leq 1.65V$	2.112
$1.65V < \Delta V \leq 1.98V$	4.512
$1.98V < \Delta V \leq 2.75V$	7.968
$2.75V < \Delta V \leq 3.63V$	16.032

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3.63V < ΔV ≤ 5.5V

35.952

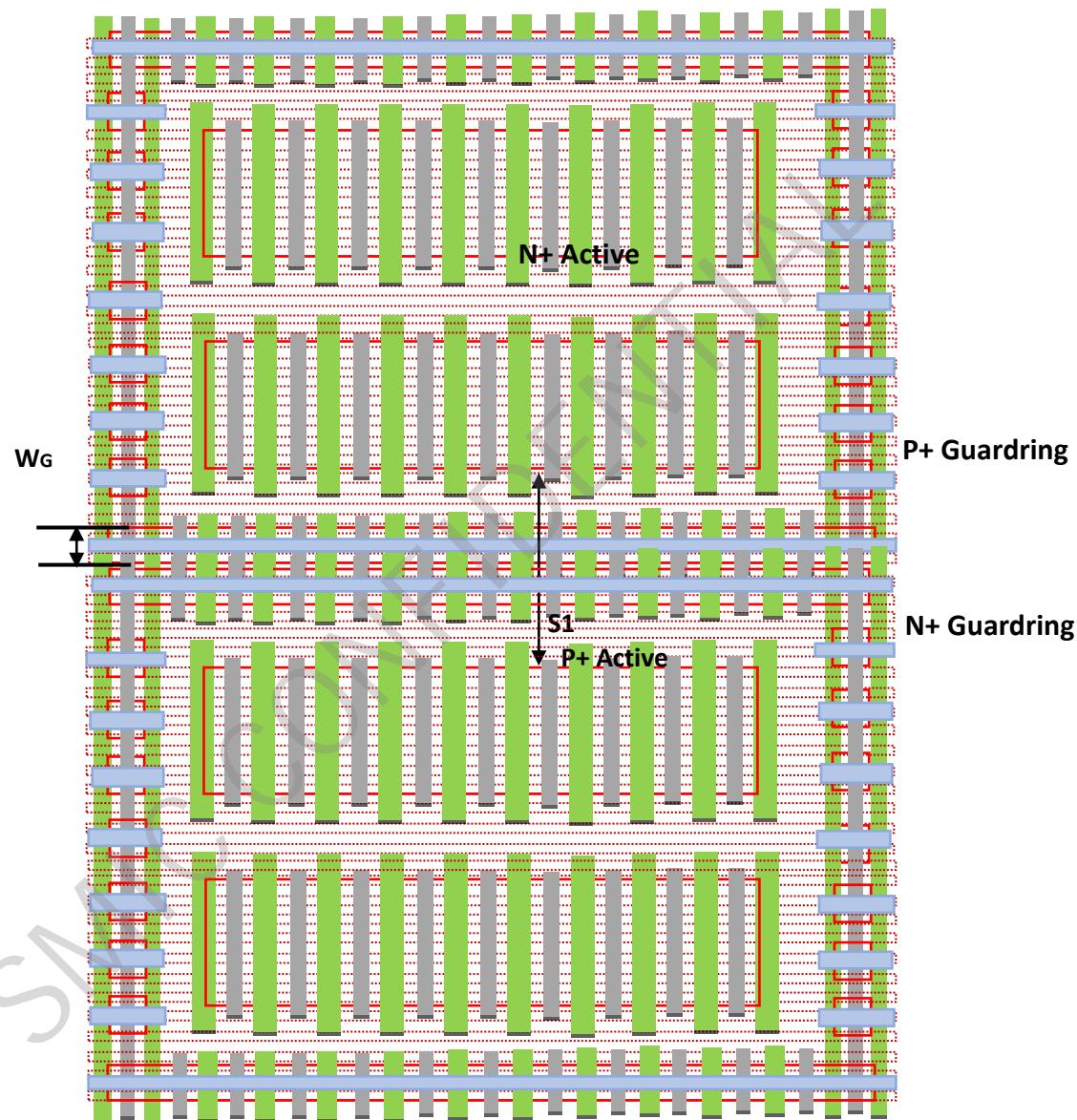
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7.12.4.6 Fig.1 space (S1) between NMOS and PMOS connected to I/O pad

	AA		FIN		GTDUM		M0		M0G		GT
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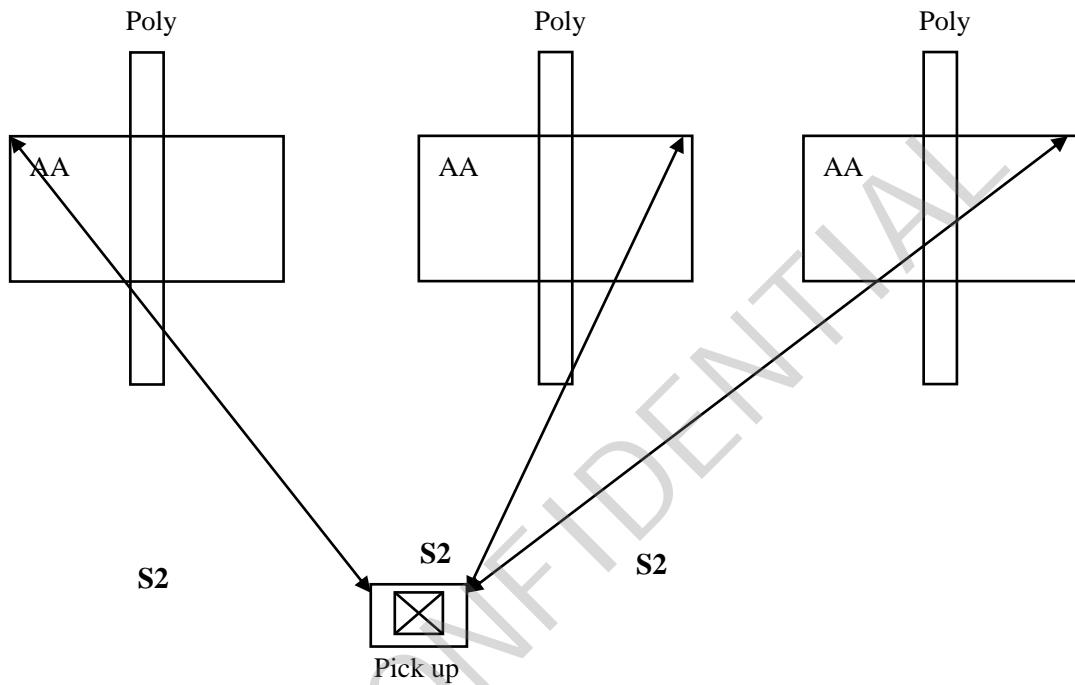


Fig. 2 illustration of the spacing S_2

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7.11.4.7 Latch Up(85°C) guidelines for Area I/O

For advanced VLSI technology, Area I/O design is implemented for new package process such as flip chip. Area I/O is surrounded by internal CMOS circuits and it is different from the peripheral type I/O. Latch up event is easier to happen around Area I/O and it requests more stringent latch up rule. Fig.3 shows the Area I/O and Peripheral I/O schematic diagram.

To enable Area I/O latch up rule check, two options are provided.

- 1) Turn on “Area_IO” switch. If this switch is ON, Area I/O latch up rule will apply for the whole chip. “Area_IO” switch is default OFF.
- 2) Use marker layer LUAREA1(131;163). The design inside LUAREA1 needs to follow Area I/O latch up rule.

Rule number	Description	Operation	Design Value	Unit
LU.7	For Area I/O, within 58um of AA injector, LU.8 to LU.11 should be followed except below conditions: 1) AA injector area < 5 um ² 2) For core circuits, space between N+ AA and P+ AA ≥ 2.976um.			
LU.8	For Area I/O, AA injector must be surrounded by two guard rings with width ≥ 0.192um That is: N+ AA injector is surrounded by a P+ guard-ring, and this P+ guard-ring is surrounded by a N+ guard-ring. P+ AA injector is surrounded by a N+ guard-ring, and this N+ guard-ring is surrounded by a P+ guard-ring	≥	0.192	um
LU.9	For Core devices: Any point inside NMOS S/D space to the nearest PW strap in the same PW. Any point inside PMOS S/D space to the nearest NW strap in the same NW.	≤	24.96	um
LU.10	For Core devices with PMOS S/D voltage > 1.05V: Any point inside NMOS S/D space to the nearest PW strap in the same PW. Any point inside PMOS S/D space to the nearest NW strap in the same NW.	≤	4.992	um
LU.11	For I/O devices:	≤	4.992	um

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	Any point inside NMOS S/D space to the nearest PW strap in the same PW. Any point inside PMOS S/D space to the nearest NW strap in the same NW.		
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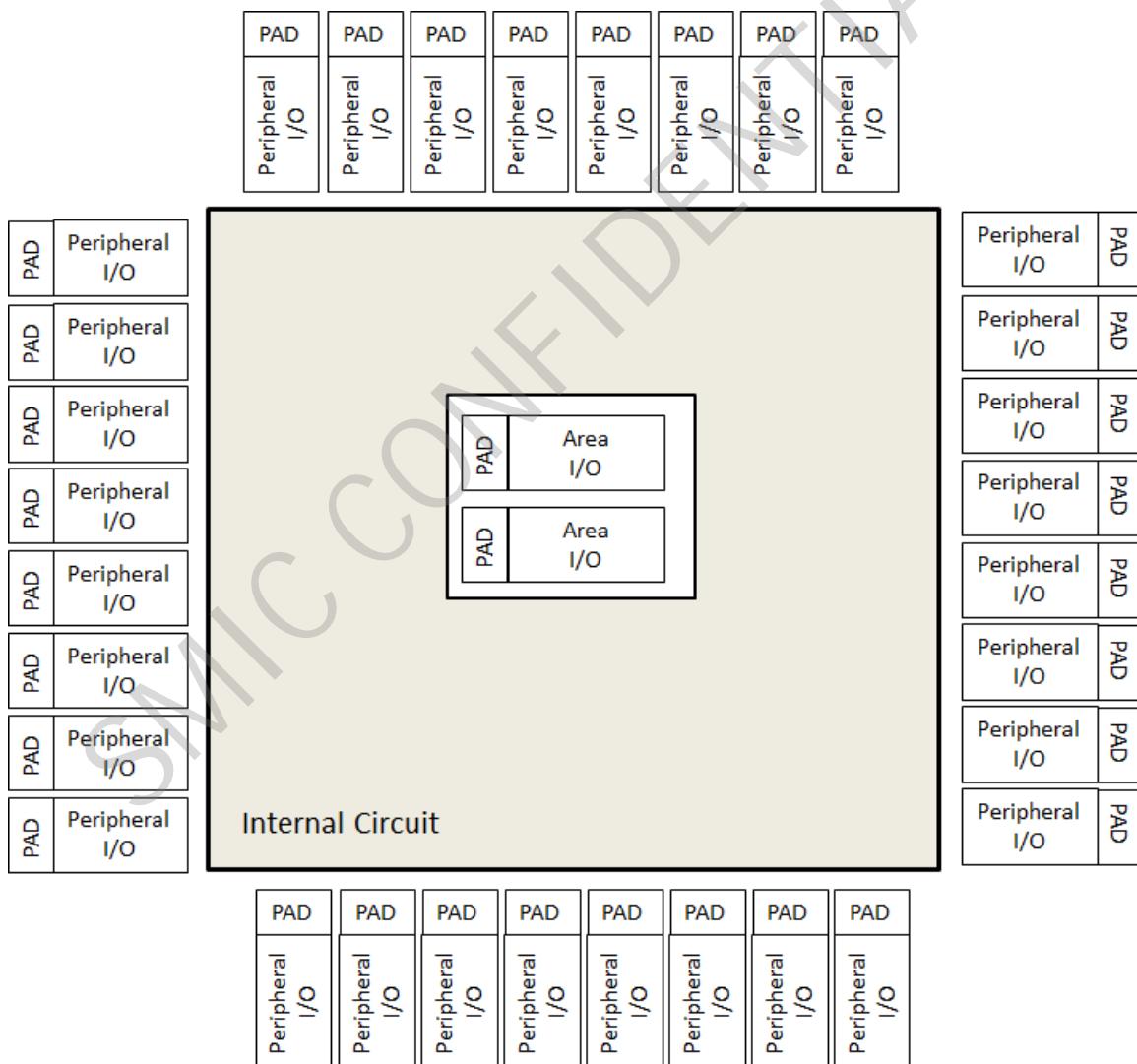


Fig.3 Area I/O and Peripheral I/O Schematic Diagram

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7.11.5 Latch-Up(85~125°C) prevention layout guidelines

7.11.5.1 Definition of nomenclature in latch up(85~125°C) guidelines

Name	Definitions
I/O pads	Pads except Vdd pad, Vss pad.
Power Pads	Vdd pad, Vss pad
Internal Circuit	All devices do not connect to IO pad.
Guard-ring	Complete un-broken ring-type AA and M1 with M0 and V0 as many as possible, connected to Vdd or Vss
P+ guard-ring	Complete un-broken ring-type ((SP AND AA) NOT NW) and M1 with M0 and V0 as many as possible, connected to Vss.
N+ guard-ring	Complete un-broken ring-type ((SN AND AA) AND NW) and M1 with M0 and V0 as many as possible, connected to Vdd.
AA injector	Any AA directly connected to I/O pad, ex. MOS, diode, AA resistor, and well resistor directly connected to I/O pad.
IO Anode	((SP AND AA) NOT GT) directly connected to I/O pad
IO Cathode	((SN AND AA) NOT GT) directly connected to I/O pad
Power Anode	((SP AND AA) NOT GT) directly connected to Vdd/Vss pad
Power Cathode	((SN AND AA) NOT GT) directly connected to Vdd/Vss pad
PW Anode	PW in DNW directly connected to Vdd/Vss pad
NW Cathode	NW directly connected to Vdd/Vss pad

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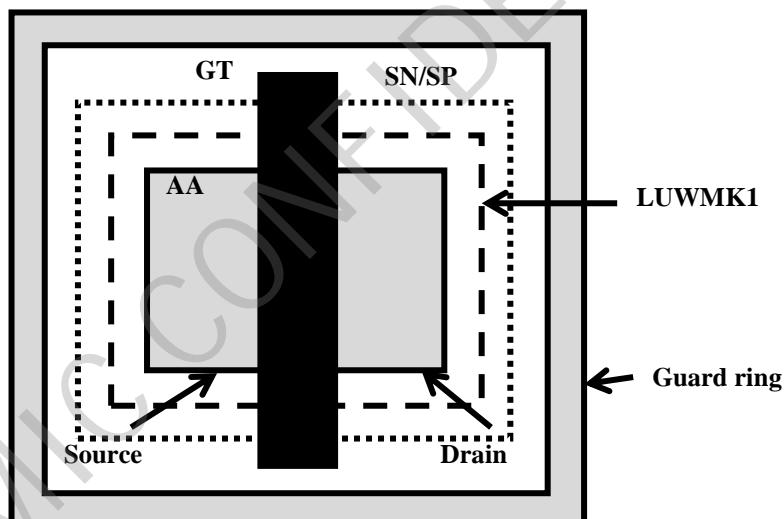
7.11.5.2 Definition of Latch up Dummy Layer

LUWMK1 (131;177) is a dummy layer for designer to waive latch up rules (LU.1~LU.3)

Note:

- 5) DRC will not check the area which is blocked by LUWMK1.
- 6) It will have risk if designer draw this layer to exempt latch up rule check without silicon proven of package level latch up test.
- 7) This layer is for DRC use, not a tape out required CAD layer.
- 8) Designer need to follow the following guidelines to draw LUWMK1.

Draw LUWMK1 to fully cover AA injector, including the source, gate, drain, diode and resistor, but not necessarily to cover well pickup and guard-ring.



LUAREA1 (131;161) is a dummy layer for designer to trigger area I/O latch up rule check. LUAREA1 need to fully cover AA injector, but not necessarily to cover well pickup and guard-ring.



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7.11.5.3 Connectivity Check

RES2H (131;178) is a DRC marking layer to identify resistor with resistance larger than 200ohm. If the resistance of used resistors between PAD and AA injector is larger than 200ohm, the marking layer RES2H (131;178) should be cover on the resistor. Latch up rule check connection will be broken by resistors with RES2H layer.

RESH(131;179) is a DRC marking layer to identify resistor with resistance below 200ohm, but customer consider it is safe to break connectivity for latch up check.

DRC use the following features to check the connectivity:

- 5) The connectivity is formed by metal, via, ALPA, PA.
- 6) If resistors with RES2H (131;178) and RESH(131;179) including AA resistor, Hi-R resistor, well resistor are between PAD and AA injector, the connection is broken.
- 7) The DRC switch of #CONNECT_ALL_RESISTOR (to connect AA resistor, Hi-R resistor, well resistor between PAD and AA injector) can control the connectivity of resistor. If #CONNECT_ALL_RESISTOR is on, the RES2H and RESH layer will not break the connection. This switch is off by default.
- 8) DRC runset provides the following options for designer's control.

Option	Turn on CONNECT_ALL_RESISTOR
A	No (default)
B	Yes

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7.11.5.4 DRC use the following features to identify the Power PAD and I/O PAD.

- 5) DRC will recognize the PAD by MD layer with Metal, via, PA, ALPA layers connectivity
- 6) DRC will recognize Power PAD and IO PAD according to the below methodology definition under #DEFINE_LU_BY_TEXT switch control.

Power net and IO net are taken as Power PAD and IO PAD respectively. In this case, even if a net is not connected to a real PAD(MD), the Power net will be taken as a Power PAD and IO net as IO PAD equivalently.

- 7) Latch up check when #DEFINE_LU_BY_TEXT switch turn off
 - a. Priority: IOMK1 > VDDMK1/VSSMK1 > N+ pickup/P+ pickup
pickup includes normal pickup, strap and guard ring type
 - b. DRC will recognize the IO PAD/net by M1 layer which overlap with IOMK1.
 - c. DRC will recognize the Power PAD which overlap with VDDMK1/VSSMK1
 - d. DRC will recognize the Power PAD which connected to Pick-up. In this case, Power PAD connect to N+ Pick-up AA will be taken as VDD PAD and Power PAD connect to P+ Pick-up AA as VSS PAD
 - e. If a PAD is not check out as case b/c/d, will be taken as IO PAD
- 8) Latch up check when #DEFINE_LU_BY_TEXT switch turn on(Default option)
 - a. Priority: Power text > IO text > IOMK1 > VDDMK1/VSSMK1 > N+ pickup/P+ pickup
pickup includes normal pickup, strap and guard ring type
 - b. DRC will recognize the Power net with label of top level Power text of all metal and metal text layers. These label text should overlap with its own metal layer, for example, M1TXT on M1 pattern, M2TXT on M2 pattern...
 - c. DRC will recognize the IO net with label of top level IO text of all metal and metal text layers. These label text should overlap with its own metal layer, for example, M1TXT on M1 pattern, M2TXT on M1 pattern...
 - d. DRC will recognize the IO PAD/net by M1 layer which overlap with IOMK1.
 - e. DRC will recognize the Power PAD which overlap with VDDMK1/VSSMK1
 - f. DRC will recognize the Power PAD which connected to Pick-up. In this case, Power PAD connect to N+ Pick-up AA will be taken as VDD PAD and Power PAD connect to P+ Pick-up AA as VSS PAD. **If Power PAD connect to both N+ Pickup AA and P+ Pick-up AA, it will be considered as VSS PAD.**
 - g. If a PAD is not check out as case b/c/d/e/f, will be taken as IO PAD
 - h. Default Power text name are "?VDD?", "?VCC?", "?VSS?", "?GND?", but no default IO text. User can define both Power text and IO text in DRC utility.

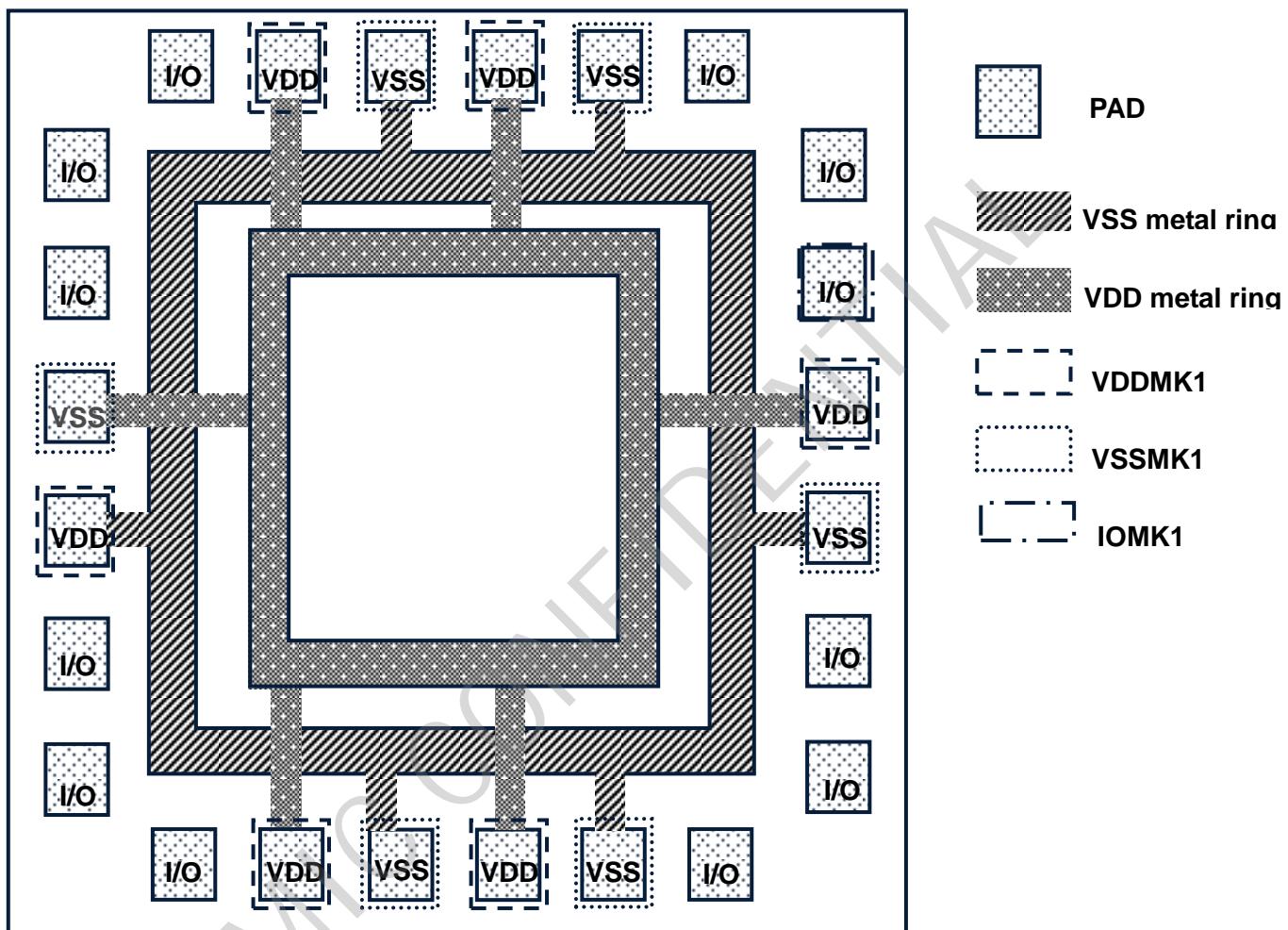
Priority:

Switch setting	Check Priority
(DEFINE_LU_BY_TEXT ON)	Power text > IO text > IOMK1 > VDDMK1/VSSMK1 > N+ Pickup/P+ Pickup
(DEFINE_LU_BY_TEXT OFF)	IOMK1 > VDDMK1/VSSMK1 > P+ Pickup > N+ Pickup

Except for the recognized Power PAD, all the other pads are defined as I/O PAD.

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7.11.5.5 DRC Methodology for Delta Voltage

DRC uses below options for voltage recognition:

- 4) Use Metal voltage top text layer (Mx_V_Hi/Lo_TOP), detailed GDS number please refer to SMIC CAD layer mapping table.
- 5) Use Metal voltage marking layer (Mx_V_Hi/Lo), detailed GDS number please refer to SMIC CAD layer mapping table.
- 6) Use detail Metal voltage marking layer (examples: M1_V18, M2_0d8V, etc), detailed GDS number please refer to SMIC CAD layer mapping table.

Latch up DRC checking flow:

- 6) Voltage rating for all devices connected to IO and power pad need to be identified.
- 7) Identify IO Anode/Cathode, Power Anode/Cathode, PW Anode, NW Cathode.
- 8) If anode voltage > cathode voltage, perform latch up check, otherwise do not perform checking.
- 9) If anode interacts with Mx_V_Hi_TOP or Mx_V_Hi and cathode interacts with Mx_V_Lo_TOP or Mx_V_Lo, perform latch up checking, otherwise do not perform checking.
- 10) Voltage drop between anode and cathode will decide the spacing rule of LU.4.x.

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7.11.5.6 General Latch Up(85~125°C) Rule

Rule number	Description	Opt.	Design Value	Unit
LU.1	<p>Every AA injector must be surrounded by two guard-dings. That is: N+ AA injector is surrounded by a P+ guard-ring, and this P+ guard-ring is surrounded by a N+ guard-ring. P+ AA injector is surrounded by a N+ guard-ring, and this N+ guard-ring is surrounded by a P+ guard-ring NW/PW pickups rings can be used as guard rings. DRC doesn't check OCCDFH region.</p>			
LU.1.1 ^[NC]	One additional PW strap and one additional NW strap are required to be inserted between the guard-rings of LU.1, PW strap is in between N+ guard-ring and NW strap, PW strap is in between P+ guard-ring and PW strap.			
LU.1.2	If Delta V $\geq 2.5V$, one additional P+ strap and one additional N+ strap are required to be inserted between the straps of LU.1.1.			
LU.1.3	DNW interact with IO Anode must be surrounded by P+ guard-ring. Internal Circuit placed between DNW and this guard-ring is not allowed.			
LU.2	<p>Within 30um from AA injector, a NMOS group must be surrounded by a P+ guard-ring; a PMOS group must be surrounded by a N+ guard-ring. The following cases are excluded:</p> <ul style="list-style-type: none"> 5. The MOS AA is covered by LUWMK1. 6. The MOS AA is floating. (DRC recognize MOS AA without V0 connection as floating MOS AA) 7. The NMOS is inside DNW, and this DNW does not physically interact with PMOS NW. At the same time, voltage of the DNW \geq voltage of PMOS NW. 8. OCCDFH region 			
LU.3	Within 14.976um from AA injector, if two NW are with different potential, a PW strap must be inserted between these NWs, (DRC only check NWs space $\leq 29.952\mu m$), except OCCDFH region			
LU.4.1	Space between IO Anode and IO Cathode, needs to follow latch	\geq	Latch Up	um

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	up space rule table		Space Rule Table	
LU.4.2	Space between IO Anode and Power Cathode, or between Power Anode and IO Cathode, needs to follow latch up space rule table. The following case can be excluded: NMOS is inside DNW, and this DNW does not physically interact with PMOS NW. At the same time, voltage of the DNW \geq voltage of PMOS NW	\geq	Latch Up Space Rule Table	um
LU.4.3	Space between IO Anode and NW Cathode, or between PW Anode and IO Cathode, need to follow latch up space rule table.	\geq	Latch Up Space Rule Table	um
LU.4.4	Within 14.976um from AA injector, space between Power Anode and NW Cathode, between PW Anode and Power cathode, and between PW Anode and NW Cathode need to follow latch up space rule table.	\geq	Latch Up Space Rule Table	um
LU.5	Space (S2) from any point within the S/D region to the nearest pickup AA region inside the same well for I/O and internal circuits. (Fig.2). Except OCCDFH region	\leq	25	um
LU.6 ^[NC]	All the guard rings and pickups should be connected to VDD/VSS with low series resistance. Contacts and Vias should be used as many as possible.			
LU.6.1	Guard-ring width of LU.1, LU.1.2 and LU.1.3	>	0.192	um
LU.6.2 ^[NC]	Additional NW and PW strap width of LU.1.1	>	0.096	um
LU.6.3	Guard-ring width of LU.2	>	0.096	um
LU.6.4 ^[NC]	PW strap width of LU.3	>	0.096	um
LU.6.5	DRC will recognize a complete guard-ring when AA space \leq 0.576um and parallel run length \geq 0.192um.			

Latch Up Space Rule Table for LU.4.x

Voltage Drop	Space between Anode and Cathode for LU4.1/4.2 (um)	Space between Anode and Cathode for LU4.3/4.4 (um)
0V < $\Delta V \leq 1V$	0.96	0.96
1V < $\Delta V \leq 1.32V$	1.824	1.824
1.32V < $\Delta V \leq 1.65V$	2.112	2.12

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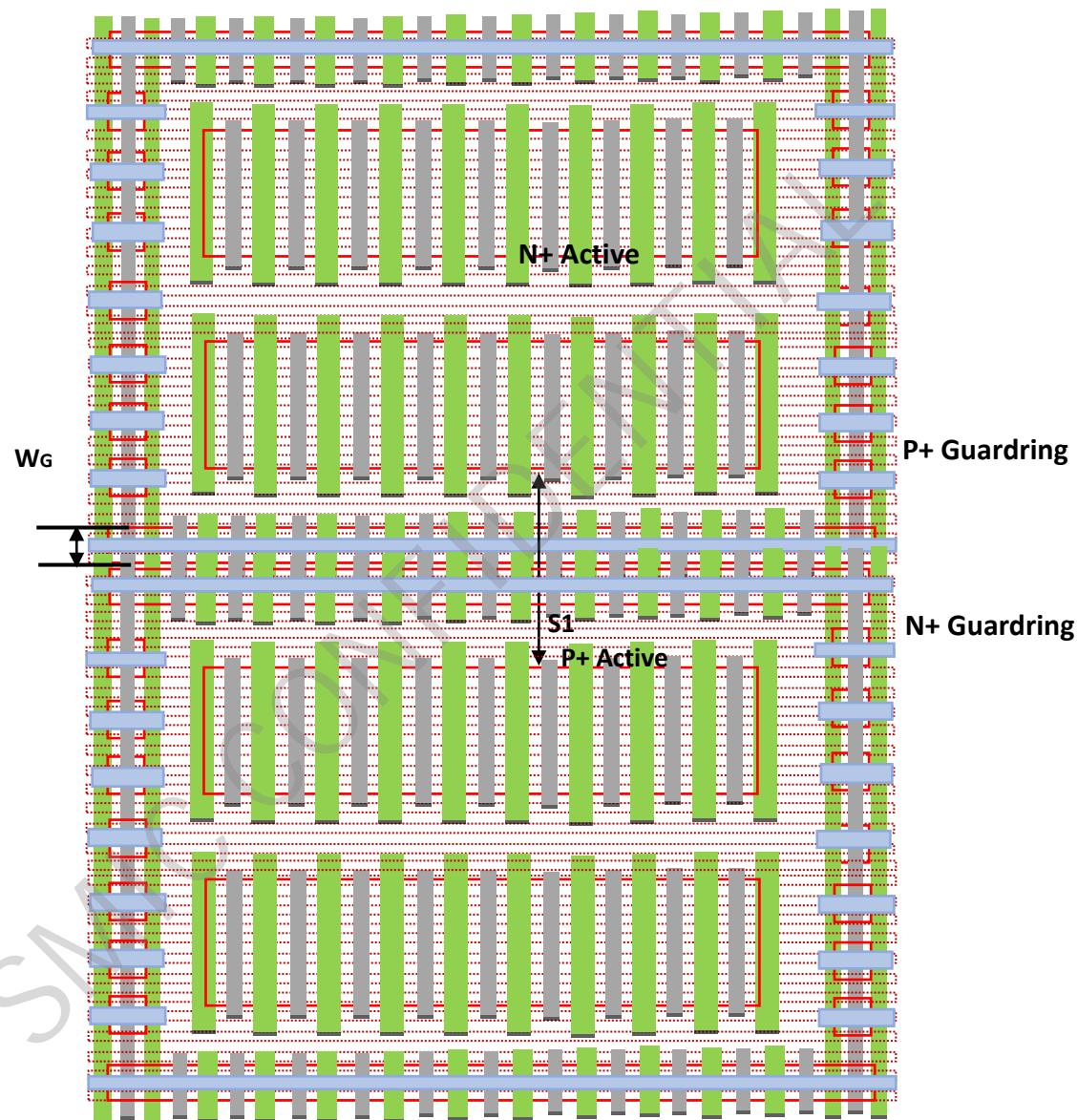
1.65V < $\Delta V \leq 1.98V$	3	4.464
1.98V < $\Delta V \leq 2.75V$	5	7.968
2.75V < $\Delta V \leq 3.63V$	15	16.032
3.63V < $\Delta V \leq 5.5V$	35	36

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7.12.4.6 Fig.1 space (S1) between NMOS and PMOS connected to I/O pad

	AA		FIN		GTDUM		M0		M0G		GT
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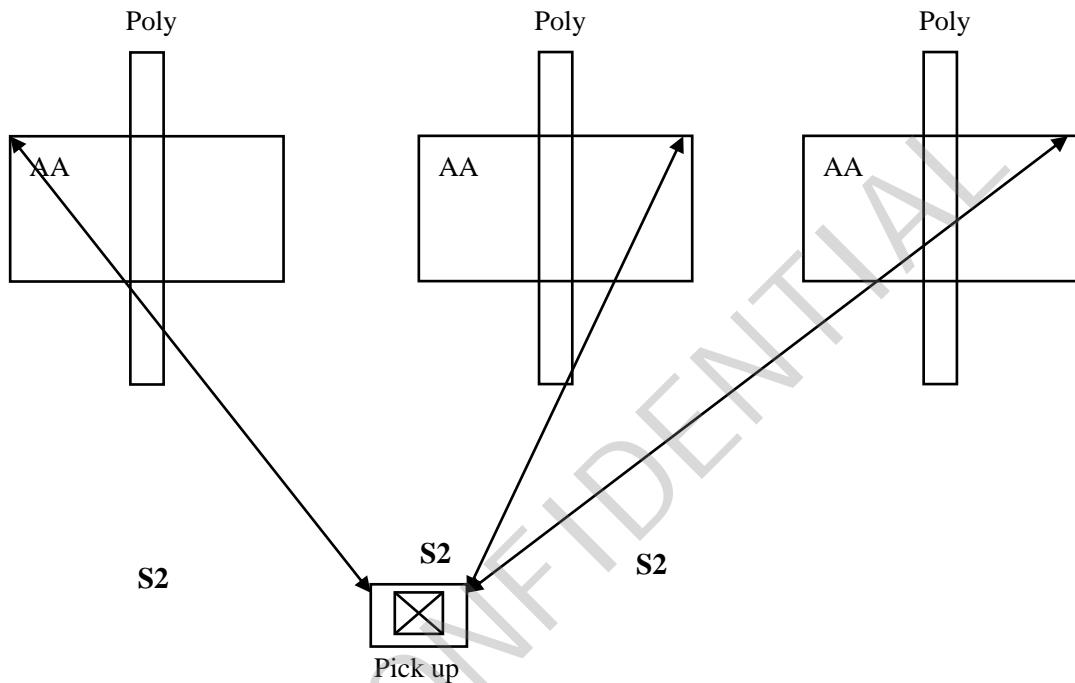


Fig. 2 illustration of the spacing S_2

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7.11.5.7 Latch Up(85~125°C) guidelines for Area I/O

For advanced VLSI technology, Area I/O design is implemented for new package process such as flip chip. Area I/O is surrounded by internal CMOS circuits and it is different from the peripheral type I/O. Latch up event is easier to happen around Area I/O and it requests more stringent latch up rule. Fig.3 shows the Area I/O and Peripheral I/O schematic diagram.

To enable Area I/O latch up rule check, two options are provided.

- 3) Turn on “Area_IO” switch. If this switch is ON, Area I/O latch up rule will apply for the whole chip. “Area_IO” switch is default OFF.
- 4) Use marker layer LUAREA1(131;163). The design inside LUAREA1 needs to follow Area I/O latch up rule.

Rule number	Description	Operation	Design Value	Unit
LU.7	For Area I/O, within 58um of AA injector, LU.8 to LU.11 should be followed except below conditions: 3) AA injector area < 5 um ² 4) For core circuits, space between N+ AA and P+ AA ≥ 2.976um.			
LU.8	For Area I/O, AA injector must be surrounded by two guard rings with width > 0.192um That is: N+ AA injector is surrounded by a P+ guard-ring, and this P+ guard-ring is surrounded by a N+ guard-ring. P+ AA injector is surrounded by a N+ guard-ring, and this N+ guard-ring is surrounded by a P+ guard-ring	>	0.192	um
LU.9	For Core devices: Any point inside NMOS S/D space to the nearest PW strap in the same PW. Any point inside PMOS S/D space to the nearest NW strap in the same NW.	≤	4.992	um
LU.10	For Core devices with PMOS S/D voltage > 1.05V: Any point inside NMOS S/D space to the nearest PW strap in the same PW. Any point inside PMOS S/D space to the nearest NW strap in the same NW.	≤	4.992	um
LU.11	For I/O devices:	≤	4.992	um

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	Any point inside NMOS S/D space to the nearest PW strap in the same PW. Any point inside PMOS S/D space to the nearest NW strap in the same NW.		
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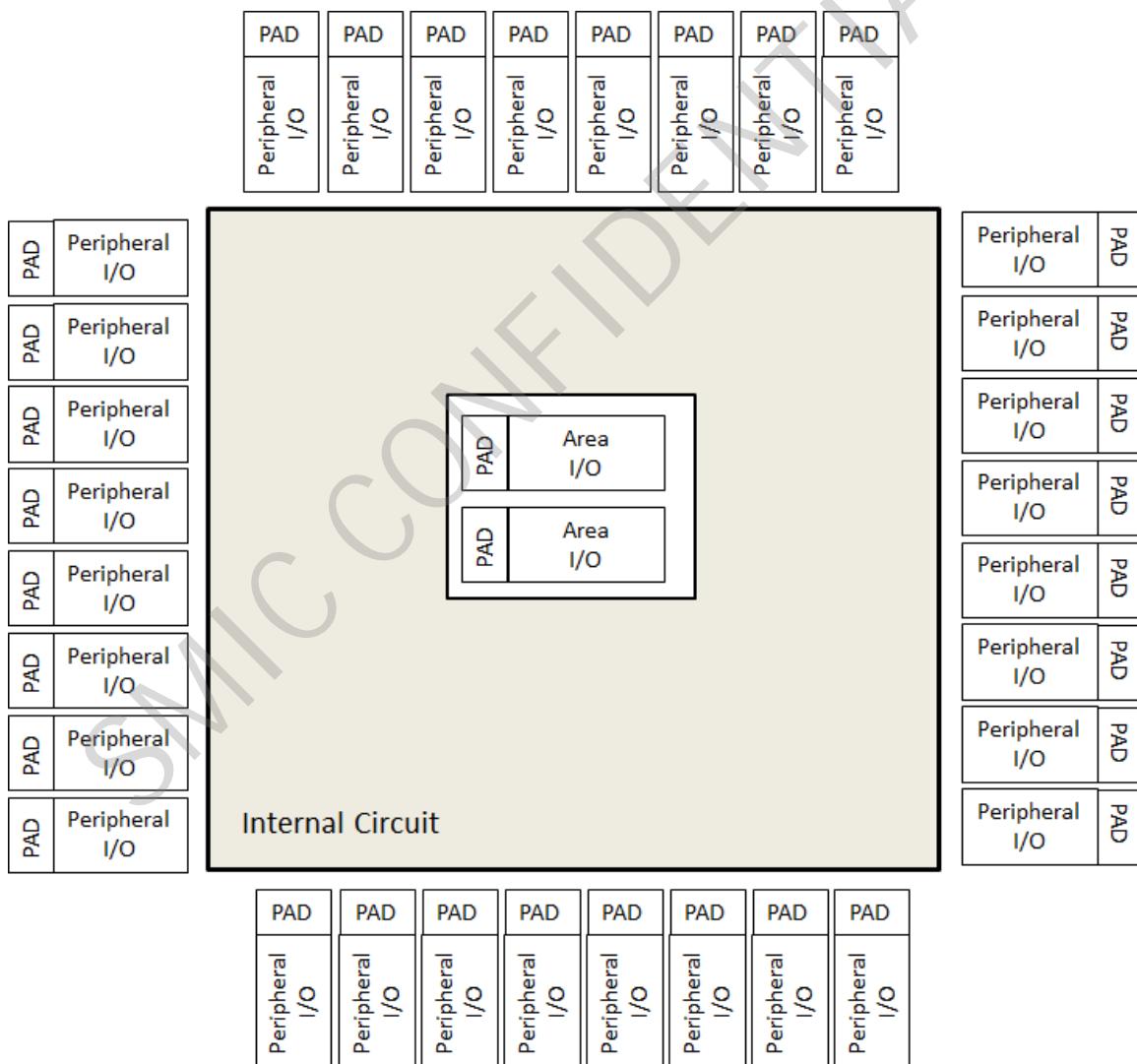


Fig.3 Area I/O and Peripheral I/O Schematic Diagram

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7.12 OCCD and OCOVL design guidelines

SMIC provide on-chip OCCD and OCOVL monitor methodology. Designer can use SMIC script or base GDS samples to insert OCCD and OCOVL in design phase, or request SMIC to add OCCD during dummy filling phase. It is a must that the DRC result is clean before OCCD and OCOVL insertion, except min-density related rules.

7.12.1 OCCD design guidelines

SMIC provide one integrated FEOL OCCD and one integrated BEOL OCCD samples respectively. For BEOL OCCD samples SMIC also provide M1~M8 OCCD sample by layer respectively, for designer convenient usage.

Rule number	Description	Opt.	Design Value	Unit
OCCD.W.1	OCCDFH is for FEOL OCCD marker recognition, width and length of OCCDFH	=	4.128	um
OCCD.W.2	OCCDM1 is for M1 OCCD marker recognition, width and length of OCCDM1	=	4.5	um
OCCD.W.3	OCCDMn(n=2~8) is for Mn OCCD marker recognition, width and length of OCCDMn	=	4.5	um
OCCD.W.4	OCCDBn(n=1~2) is for Bn OCCD marker recognition, width and length of OCCDBn	=	4.5	um
OCCD.S.1	Space between OCCDFH	≥	4.5	um
OCCD.S.2	Space between OCCDM1	≥	4.5	um
OCCD.S.3	Space between OCCDFH and OCCDM1	≥	4.5	um
OCCD.S.4	Space between OCCDMn (n=2~8, respectively)	≥	4.5	um
OCCD.S.5	Space between OCCDBn (n=1~2, respectively)	≥	4.5	um
OCCD.S.6 ^[R]	Recommended space between OCCDFH	≥	140	um
OCCD.S.7 ^[R]	Recommended space between OCCDM1	≥	140	um
OCCD.S.8 ^[R]	Recommended space between OCCDMn (n=2~8, respectively)	≥	140	um
OCCD.S.9 ^[R]	Recommended space between OCCDBn (n=1~2, respectively)	≥	140	um
OCCD.S.10	Space between OCCDFH and DNW, NW, PSUB, AA, AR, GT, GT_P96, P2, SN, SP, DG, M0, M0G, M0C, V0, M1, LOGO, INST, MARKS, MARKG, NODMF, OCOVL, DUMBA, DUMBp, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, V0DUB, M1DUB, EFUSE, RESNW, RESP1, RESP2, ESDIO2, DSTR, DIOMK2, DMPNP, VARMOS, LDBK,	≥	1.8	um

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Rule number	Description	Opt.	Design Value	Unit
	INDMY, FUSEMK1, NPAA, PPAA, AR_H, AR_V, DIOMK1, ESDIO1, SVT_N edge, SVT_P edge, HVT_N edge, HVT_P edge, LVT_N edge, LVT_P edge, ULVT_N edge, ULVT_P edge, LFN_N edge, LFN_P edge, MTFUSE, CTOP			
OCCD.S.11	Space between OCCDFH and DUM_AA, DUM_AR, DUM_GT, DUM_P2, DUM_M0, DUM_M0C, DUM_M0G, DUM_V0, DUM_M1, SNDUM, SPDUM, AR_HDOP, AR_VDOP	≥	0.2	um
OCCD.S.12	Space between OCCDM1 and M1, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCOVL, M1DUB, MTFUSE, MOMDMY, FUSEMK1, CTOP	≥	1.8	um
OCCD.S.13	Space between OCCDM1 and DUM_M1	≥	0.2	um
OCCD.S.14	Space between OCCDMn (n=2~8, respectively) and Mn, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCOVL, MnDUB, MTFUSE, MOMDMY, FUSEMK1, CTOP	≥	1.8	um
OCCD.S.15	Space between OCCDMn (n=2~8, respectively) and DUM_Mn	≥	0.2	um
OCCD.S.16	Space between OCCDBn (n=1~2, respectively) and Bn, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCOVL, BnDUB, MTFUSE, MOMDMY, FUSEMK1, CTOP	≥	1.8	um
OCCD.S.17	Space between OCCDBn (n=1~2, respectively) and DUM_Bn	≥	0.2	um
OCCD.EN.1	OCCD enclosure by CHIPB	≥	1.8	um
OCCD.R.1	OCCDB is for all BEOL OCCD marker recognition, OCCDB must be drawn the same as ((OCCDM1 OR OCCDMn) OR OCCDBn)			
OCCD.R.2	OCCD is for all OCCD markers recognition, OCCD must be drawn the same as (OCCDFH OR OCCDB)			
OCCD.R.3	OCCDFH overlap with PSUB, DG, LOGO, INST, MARKS, MARKG, NODMF, OCOVL, DUMBA, DUMBp, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, V0DUB, M1DUB, EFUSE, RESNW, RESP1, RESP2, ESDIO2, DSTR, DIOMK2, DMPNP, VARMOS, LDBK, INDMY, FUSEMK1, DUM_AA, DUM_AR, DUM_GT, DUM_P2, DUM_M0, DUM_M0C, DUM_M0G, DUM_V0, DUM_M1, SNDUM, SPDUM, NPAA, PPAA, AR_H, AR_V, DIOMK1, ESDIO1, SVT_N edge, SVT_P edge, HVT_N edge, HVT_P edge, LVT_N edge,			

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Rule number	Description	Opt.	Design Value	Unit
	LVT_P edge, ULVT_N edge, ULVT_P edge, LFN_N edge, LFN_P edge, MTFUSE, CTOP, AR_HDOP, AR_VDOP, OCCDM1 is not allowed.			
OCCD.R.4	OCCDM1 overlap with INST, LOGO, MARKS, MARKG, NODMF, OCOVL, M1DUB, MTFUSE, MOMDMY, INDMY, FUSEMK1, DUM_M1, CTOP is not allowed			
OCCD.R.5	OCCDMn(n=2~8, respectively) overlap with INST, LOGO, MARKS, MARKG, NODMF, OCOVL, MnDUB, MTFUSE, MOMDMY, INDMY, FUSEMK1, DUM_Mn, CTOP is not allowed			
OCCD.R.6	OCCDBn(n=1~2, respectively) overlap with INST, LOGO, MARKS, MARKG, NODMF, OCOVL, BnDUB, MOMDMY, INDMY, FUSEMK1, DUM_Bn, CTOP is not allowed			
OCCD.R.7^[R]	Recommended at least one OCCDFH in each 2000umx2000um window of chip.			
OCCD.R.8^[R]	Recommended at least one OCCDM1 in each 2000umx2000um window of chip.			
OCCD.R.9^[R]	Recommended at least one OCCDMn(n=2~8, respectively) in each 2000umx2000um window of chip.			
OCCD.R.10^[R]	Recommended at least one OCCDBn(n=1~2, respectively) in each 2000umx2000um window of chip.			

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7.12.2 OCOVL design guidelines

SMIC provide totally 11 types of FEOL OCOVL markers, and 5 types of BEOL OCOVL markers. Designer need base GDS samples to insert OCOVL in design phase.

1) OCOVL_FEOL = (OR OCOVLRAR OCOVLRARH OCOVLRARV OCOVLGT1 OCOVLGT2 OCOVLP2A OCOVLP2B OCOVLM0C OCOVLM0 OCOVLM0G1 OCOVLM0G2)

2) OCOVL_BEOL = (OR OCOVLM1CA OCOVLM1CB OCOVLM2CA OCOVLM4 OCOVLM0)

OCOVL insertion guideline:

- 1) At least insert 6 OCOVL markers (each type respectively) for 1*1 chip
- 2) At least insert 3 OCOVL markers (each type respectively) for 1*2 and 2*1 chip
- 3) At least insert 2 OCOVL markers (each type respectively) for 2*2 chip
- 4) At least insert 2 OCOVL markers (each type respectively) for 1*3 and 3*1 chip
- 5) At least insert 1 OCOVL markers (each type respectively) for 3*3 chip

Rule number	Description	Opt.	Design Value	Unit
OCOVL.W.1	OCOVL width and length	=	20	um
OCOVL.S.1	Space between OCOVL	≥	100	um
OCOVL.S.2	OCOVL_FEOL space to DNW, NW, PSUB, AA, AR, GT, GT_P96, P2, SN, SP, DG, M0, M0G, M0C, V0, LOGO, INST, MARKS, MARKG, NODMF, OCCD, DUMBA, DUMB, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, V0DUB, EFUSE, RESNW, RESP1, RESP2, ESDIO2, DSTR, DIOMK2, DMPNP, VARMOS, LDBK, INDMY, FUSEMK1, NPAA, PPAA, AR_H, AR_V, CELLB edge, DIOMK1, ESDIO1, SVT_N edge, SVT_P edge, HVT_N edge, HVT_P edge, LVT_N edge, LVT_P edge, ULVT_N edge, ULVT_P edge, LFN_N edge, LFN_P edge, MTFUSE, CTOP	≥	1.8	um
OCOVL.S.3	OCOVL_FEOL space to DUM_AA, DUM_AR, DUM_GT, DUM_P2, DUM_M0, DUM_M0C, DUM_M0G, DUM_V0, SNDUM, SPDUM, AR_HDOP, AR_VDOP	≥	0.4	um
OCOVL.S.4	OCOVLM1CA space to AA, M1, M0, GT, M0C, M0G, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, DUMBA, M1DUB, M0DUB, DUMB, M0CDUB, M0GDUB, CTOP	≥	1.8	um
OCOVL.S.5	OCOVLM1CA space to DUM_AA, DUM_M1, DUM_M0, DUM_GT, DUM_M0C, DUM_M0G	≥	0.4	um
OCOVL.S.6	OCOVLM1CA space to M1, M0, M0C, M0G, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE,	≥	1.8	um

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Rule number	Description	Opt.	Design Value	Unit
	MOMDMY, FUSEMK1, M1DUB, M0DUB, M0CDUB, M0GDUB, CTOP			
OCOVL.S.7	OCOVL.M1CB space to DUM_M1, DUM_M0, DUM_M0C, DUM_M0G	≥	0.4	um
OCOVL.S.8	OCOVL.M2CA space to M1, M2, M0G, M0C, M0, V0, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, M1DUB, M2DUB, M0GDUB, M0CDUB, M0DUB, V0DUB, CTOP	≥	1.8	um
OCOVL.S.9	OCOVL.M2CA space to DUM_M1, DUM_M2, DUM_M0G, DUM_M0C, DUM_M0, DUM_V0	≥	0.4	um
OCOVL.S.10	OCOVL.M4 space to M1, M2, M3, M4, V0, V1, V2, V3, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, M1DUB, M2DUB, M3DUB, M4DUB, CTOP	≥	1.8	um
OCOVL.S.11	OCOVL.M4 space to DUM_M1, DUM_M2, DUM_M3, DUM_M4, DUM_V0, DUM_V1, DUM_V2, DUM_V3	≥	0.4	um
OCOVL.S.12	OCOVL.V0 space to V0, M1, M0G, M0C, M0, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, V0DUB, M1DUB, M0GDUB, M0CDUB, M0DUB, CTOP	≥	1.8	um
OCOVL.S.13	OCOVL.V0 space to DUM_V0, DUM_M1, DUM_M0G, DUM_M0C, DUM_M0	≥	0.4	um
OCOVL.EN.1	OCOVL enclosure by CHIPB	≥	1.8	um
OCOVL.R.1	OCOVL should be drawn the same as (OCOVL_FEOL OR OCOVL_BEOL)			
OCOVL.R.2	16 OCOVL marks (OCOVLAR, OCOVLARH, OCOVLARV, OCOVLGT1, OCOVLGT2, OCOVLP2A, OCOVLP2B, OCOVLM0C, OCOVLM0, OCOVLM0G1, OCOVLM0G2, OCOVLM1CA, OCOVLM1CB, OCOVLM2CA, OCOVLM4, OCOVLV0) interact each other is not allowed.			
OCOVL.R.3	OCOVL_FEOL overlap DNW, NW, PSUB, AA, GT_P96, SN, SP, DG, V0, LOGO, INST, MARKS, MARKG, NODMF, OCCD, DUMBA, DUMB, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, V0DUB, EFUSE, RESNW, RESP1, RESP2, ESDIO2, DSTR, DIOMK2, DMPNP, VARMOS,			

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Rule number	Description	Opt.	Design Value	Unit
	LDBK, INDMY, FUSEMK1, DUM_AA, DUM_AR, DUM_GT, DUM_P2, DUM_M0, DUM_M0C, DUM_M0G, DUM_V0, SNDUM, SPDUM, NPAA, CELLB edge, DIOMK1, ESDIO1, SVT_N edge, SVT_P edge, HVT_N edge, HVT_P edge, LVT_N edge, LVT_P edge, ULVT_N edge, ULVT_P edge, LFN_N edge, LFN_P edge, MTFUSE, CTOP, AR_HDOP, AR_VDOP is not allowed.			
OCOVL.R.4	OCOVL.M1CA overlap AA, M1CB, GT, M0C, M0G, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, DUMBA, M1DUB, M0DUB, DUMBP, M0CDUB, M0GDUB, DUM_AA, DUM_M1, DUM_M0, DUM_GT, DUM_M0C, DUM_M0G, CTOP is not allowed			
OCOVL.R.5	OCOVL.M1CB overlap INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, M1DUB, M0DUB, M0CDUB, M0GDUB, DUM_M1, DUM_M0, DUM_M0C, DUM_M0G, CTOP is not allowed			
OCOVL.R.6	OCOVL.M2CA overlap M1CB, M2CB, M0C, M0, V0, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, M1DUB, M2DUB, M0GDUB, M0CDUB, M0DUB, V0DUB, DUM_M1, DUM_M2, DUM_M0G, DUM_M0C, DUM_M0, DUM_V0, CTOP is not allowed			
OCOVL.R.7	OCOVL.M4 overlap M1CB, M2CB, M3CB, V0, V1, V2, V3, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, M3DUB, M4DUB, DUM_M1, DUM_M2, DUM_M3, DUM_M4, DUM_V0, DUM_V1, DUM_V2, DUM_V3, CTOP is not allowed			
OCOVL.R.8	OCOVL.V0 overlap V0CB, M1CB, INDMY, INST, LOGO, MARKS, MARKG, NODMF, OCCD, MTFUSE, MOMDMY, FUSEMK1, V0DUB, M1DUB, M0GDUB, M0CDUB, M0DUB, DUM_V0, DUM_M1, DUM_M0G, DUM_M0C, DUM_M0, CTOP is not allowed			
OCOVL.R.9	V0, M1, M2, M3 inside OCOVL must be pre-colored			

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7.13 Dummy Check Rules

7.13.1 Dummy insertion method selection guideline

- a. SMIC auto dummy fills insertion utility now supports both FEOL and BEOL insertion design manual.
- b. It's strongly recommended designers to use SMIC model based dummy insertion utility to do dummy insertion which has better performance to comply with density rules. Application notice please refer dummy insertion utility; designers can download these utilities from SMIC NOW. In order to get layout uniform and friendly globally for process control, you must to use SMIC's auto dummy insertion utility (document: TD-LO14-DT-2002).
- c. If designers still found DRC violations after use SMIC-provided dummy insertion utilities, SMIC will review the results and take proactive steps to close the DRC violation issues. If you use non-SMIC-provided dummy fill scripts, you must ensure DRC clean, and consult with SMIC.
- d. Please designers ensure timing closure post dummy insertion. It is strongly recommended design to check timing with dummy fillings.
- e. It is recommended to fill on the whole chip again; even dummy fill is done in blocks or chip. It is high risky to use dummy utility only on the instance blocks.
- f. For RF device or the other concerning circuits with dummy auto insertion, you can draw dummy block layers to prevent dummy auto fill. It is suggest to manually drawing dummy using manual draw dummy rules (.8 data type) but you should make sure this areas are meet DRC density requirement.
- g. Special note for some dummy forbidden device area:
 - a) For AA/AR_H/AR_V/P2/SN/SP/M0/M0C/M0G layers: dummy will skip area covered by mark layer of LDBK/INST/RESP2/DSTR/DMPNP/VARMOS/EFUSE/INDMY/MARKS/MARKG/DIOMK1/DIOMK2. Designer should ensure these area density/DFM rule DRC clean.
 - b) For GT layer: dummy will skip area covered by mark layer of LDBK/INST/RESP2/DSTR/DMPNP/VARMOS/EFUSE/INDMY/MARKS/MARKG/DIOMK1/DIOMK2. Designer should ensure these area density/DFM rule DRC clean.
 - c) For inter metal/via layer: dummy will skip area covered by mark layer of INST/EFUSE/INDMY/MARKG/MARKS (INST just work for M1~M3 and V1~V3). Designer should ensure these area density/DFM rule DRC clean.
 - d) For top metal layer: dummy will skip area covered by mark layer of INDGY/MARKG/MARKS. Designer should ensure these area density/DFM rule DRC clean.
 - e) For ALPA layer: dummy will skip area covered by mark layer of MARKG/MARKS/INDGY. Designer should ensure these area density/DFM rule DRC clean.

7.13.2 Device table for dummy pattern insertion

Designers can refer to below device table for dummy pattern insertion and need add dummy block layers if you do not want to fill dummy at this area.



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Dummy patterns device category	Marker Layer	GDS No.	AA Dummy	AR_H/AR_V/AR Dummy	Poly Dummy	P2 Dummy	M0 Dummy	M0C Dummy	M0G Dummy	M1/Mxy/1.25xMMy/1.25xMn/2xMn Dummy	Vy//1.25xVn/2xVn/10xTVn/14xTMn/UTM TV Dummy	10xTMn/14xTMn/UTM Dummy	ALPA Dummy	Remark
LDMOS	LDBK	216; 150	N	N	N	N	N	N	N	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement.
SRAM	INST	60; 0	N	N	N	N	N	N	N	Y	Y	Y	Y	
NW Resistor	RESNW	95; 0	N	N	N	N	N	N	N	Y	Y	Y	Y	
TiN Resistor	RESP2	96; 2	N	N	N	N	N	N	N	Y	Y	Y	Y	
Diode	DSTR	138; 0	N	N	N	N	N	N	N	Y	Y	Y	Y	
BJT	DMPNP	134;0	N	N	N	N	N	N	N	Y	Y	Y	Y	
MOS Varactor	VARMOS	93; 0	N	N	N	N	N	N	N	Y	Y	Y	Y	
MOM	MOMDMY	211;1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	
E-fuse	EFUSE	81;2	N	N	N	N	N	N	N	N	Y	Y	Y	
Inductor	INDMY	212; 0	N	N	N	N	N	N	N	N	N	N	Y	
Seal Ring	MARKS	189;151	N	N	N	N	N	N	N	N	N	N	N	
Guard Ring	MARKG	189; 0	N	N	N	N	N	N	N	N	N	N	N	

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Note:

For the above device table:

1. Y means this marker layer is allowed to fill dummy in the device region by script automatically. Designers can draw dummy block layer based on their requirement
2. N means this marker layer has been regarded as dummy block layer in dummy utility. Designers can manually draw dummy pattern based on their requirement.
3. In SRAM region,it is not permitted to auto-fill M1and M2 dummy of all BEOL dummy types.



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7.13.3 FEOL Dummy Pattern Check Rules for SMIC dummy

Nomenclatures and Abbreviations

M0DOP_M0	M0 OR (M0DOP NOT INSIDE DMCMK1)
M0DOP_M0_40	(M0 OR (M0DOP NOT INSIDE DMCMK1)) with width = 0.04/0.042
NPAA_EXT	EXTENTS NPAA
OCOVL_NOT_OCOVLM4	OCOVL NOT OCOVLM4

Rule number	Description	Opt.	Design Value	Unit
DUMC.1	Inside edge of CHIPB space to DMC1. Outside and cut is not allowed.	≥	3	um
DUMC.2	DMC1 space to DUMBA,DUMBP, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, NPAA_EXT, AA, AADMP, PPAA, GT, GTDMP, P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), M0, M0DMP, M0C, M0CDMP, M0G, M0GDMP, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	3	um
DUMC.3	DMC1 space to (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), (M0DOP NOT INSIDE DMCMK1), (M0GDUM NOT INSIDE DMCMK1), (M0GDOP NOT INSIDE DMCMK1), DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.27	um
DUMC.4	DMC1 space to AR_H, AR_V, (AR_HDOP NOT INSIDE DMCMK1), (AR_VDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.5	DMC1 space to AR, Overlap is not allowed.	≥	0.16	um
DUMC.6	DMC1 space to (ARDUM NOT INSIDE DMCMK1), (ARDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.182	um
DUMC.7	DMC1 space to (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.274	um
DUMC.8	DMC1 space to GT_P96 edge, Cut is not allowed.	≥	0.006	um
DUMC.9	DMC1 space to (M0CDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.346	um
DUMC.10	DMC1 space to (M0CDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.75	um
DUMC.11	DMC1 space to INST, Overlap is not allowed.	≥	0.21	um
DUMC.12	DMC1 space to PSUB NW, DNW edge. Cut is not allowed.	≥	0.001	um
DUMC.13	DMC1 space to RESNW, Overlap is not allowed.	≥	0.384	um
DUMC.14	DMC1 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS,	≥	0	um

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Rule number	Description	Opt.	Design Value	Unit
	EFUSE, V0, Overlap is not allowed.			
DUMC.15	DMC1 space to IND MY, Overlap is not allowed.	≥	0.2	um
DUMC.16	DMC1 space to OCCDFH, OCOVL_NOT_OCOVLM4, Overlap is not allowed.	≥	3	um
blank				
DUMC.18	DMC1 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.025	um
DUMC.19	DMC1 space to MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.20	DMC1 space to edge of HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.026	um
DUMC.21	DMC1 space to edge of DG, DGUD, DGV, Cut is not allowed.	≥	3	um
DUMC.22	Inside edge of CHIPB space to DMC2, Outside and cut is not allowed.	≥	0.45	um
DUMC.23	DMC2 space to DUMBA, DUMBP, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, AR_H, AR_V, (AR_HDOP NOT INSIDE DMCMK1), (AR_VDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.24	DMC2 space to NPAA_EXT, RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.25	DMC2 space to AA, AADMP, PPAA, M0, M0DMP, (M0DOP NOT INSIDE DMCMK1), M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), IND MY, DG, DGUD, DGV, Overlap is not allowed.	≥	0.2	um
DUMC.26	DMC2 space to (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), M0C, M0CDMP, (M0GDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.27	um
DUMC.27	DMC2 space to AR, Overlap is not allowed.	≥	0.16	um
DUMC.28	DMC2 space to (ARDUM NOT INSIDE DMCMK1), (ARDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.182	um
DUMC.29	DMC2 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.274	um
DUMC.30	DMC2 space to edge of GT_P96, PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.001	um
DUMC.31	DMC2 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.32	DMC2 horizontal space to M0DOP_M0, Overlap is not allowed.	≥	0.215	um
DUMC.33	DMC2 space to (M0CDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.3	um
DUMC.34	DMC2 space to (M0CDOP NOT INSIDE DMCMK1), Overlap is not	≥	0.75	um

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Rule number	Description	Opt.	Design Value	Unit
	allowed.			
DUMC.35	DMC2 space to INST, Overlap is not allowed.	≥	0.21	um
DUMC.36	DMC2 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.35	um
DUMC.37	DMC2 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, Overlap is not allowed.	≥	0	um
DUMC.38	DMC2 space to RSPMK1, Overlap is not allowed.	≥	0.001	um
DUMC.39	DMC2 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.41	DMC2 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.025	um
DUMC.42	DMC2 space to V0, Overlap is not allowed.	≥	0.04	um
DUMC.43	DMC2 space to DMC1, Overlap is not allowed.	≥	0.285	um
DUMC.44	Inside edge of CHIPB space to DMC3, Outside and cut is not allowed.	≥	0.45	um
DUMC.45	DMC3 space to DUMBA, DUMBP, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, AR_H, AR_V, (AR_HDOP NOT INSIDE DMCMK1), (AR_VDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.46	DMC3 space to NPAA_EXT, RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.47	DMC3 space to AA, AADMP, PPAA, M0, M0DMP, (M0DOP NOT INSIDE DMCMK1), M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), INDMY, Overlap is not allowed.	≥	0.2	um
DUMC.48	DMC3 space to (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), M0C, M0CDMP, (M0GDUM NOT INSIDE DMCMK1), DMC1, Overlap is not allowed.	≥	0.27	um
DUMC.49	DMC3 space to AR, Overlap is not allowed.	≥	0.16	um
DUMC.50	DMC3 space to (ARDUM NOT INSIDE DMCMK1), (ARDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.182	um
DUMC.51	DMC3 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.274	um
DUMC.52	DMC3 space to edge of GT_P96, PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), Cut is not allowed.	≥	0.001	um
DUMC.53	DMC3 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.54	DMC3 horizontal space to M0DOP_M0_40, Overlap is not allowed.	≥	0.23	um
DUMC.55	DMC3 space to (M0CDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.3	um
DUMC.56	DMC3 space to (M0CDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.75	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.57	DMC3 space to INST, Overlap is not allowed.	≥	0.21	um
DUMC.58	DMC3 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.35	um
DUMC.59	DMC3 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, Overlap is not allowed.	≥	0	um
DUMC.60	DMC3 space to RSPMK1, Overlap is not allowed.	≥	0.001	um
DUMC.61	DMC3 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.63	DMC3 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.025	um
DUMC.64	DMC3 space to V0, Overlap is not allowed.	≥	0.04	um
DUMC.65	DMC3 space to edge of HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.007	um
DUMC.66	Inside edge of DG space to DMC3, Outside and cut is not allowed.	≥	0.002	um
DUMC.67	DMC3 space to edge of DGUD, DGV, Cut is not allowed.	≥	0.002	um
DUMC.68	DMC3 space to DMC2, Overlap is not allowed.	≥	0.192	um
DUMC.69	DMC3 horizontal space to DMC2, Overlap is not allowed.	≥	0.215	um
DUMC.70	Inside edge of CHIPB space to DMC4, Outside and cut is not allowed.	≥	0.45	um
DUMC.71	DMC4 space to DUMBA, DUMBP, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, AR_H, AR_V, (AR_HDOP NOT INSIDE DMCMK1), (AR_VDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.72	DMC4 space to NPAA_EXT, RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.73	DMC4 space to AA, AADMP, PPAA, M0, M0DMP, (M0DOP NOT INSIDE DMCMK1), M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), INDMY, DG, DGUD, DGV, Overlap is not allowed.	≥	0.2	um
DUMC.74	DMC4 space to (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), M0C, M0CDMP, (M0GDUM NOT INSIDE DMCMK1), DMC1, Overlap is not allowed.	≥	0.27	um
DUMC.75	DMC4 space to AR, Overlap is not allowed.	≥	0.16	um
DUMC.76	DMC4 space to (ARDUM NOT INSIDE DMCMK1), (ARDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.182	um
DUMC.77	DMC4 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.274	um
DUMC.78	DMC4 space to edge of GT_P96, PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.001	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.79	DMC4 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.80	DMC4 space to (M0CDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.3	um
DUMC.81	DMC4 space to (M0CDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.75	um
DUMC.82	DMC4 space to INST, Overlap is not allowed.	≥	0.21	um
DUMC.83	DMC4 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.35	um
DUMC.84	DMC4 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, Overlap is not allowed.	≥	0	um
DUMC.85	DMC4 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.87	DMC4 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.025	um
DUMC.88	DMC4 space to V0, Overlap is not allowed.	≥	0.04	um
DUMC.89	DMC4 space to DMC2, Overlap is not allowed.	≥	0.142	um
DUMC.90	DMC4 vertical space to DMC2, Overlap is not allowed.	≥	0.192	um
DUMC.91	DMC4 space to DMC3, Overlap is not allowed.	≥	0.192	um
DUMC.92	DMC4 horizontal space to DMC3, Overlap is not allowed.	≥	0.2	um
DUMC.93	Inside edge of CHIPB space to DMC5, Outside and cut is not allowed.	≥	0.45	um
DUMC.94	DMC5 space to DUMBA, DUMBP, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, AR_H, AR_V, (AR_HDOP NOT INSIDE DMCMK1), (AR_VDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.95	DMC5 space to NPAA_EXT, RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.96	DMC5 space to AA, AADMP, PPAA, M0, M0DMP, (M0DOP NOT INSIDE DMCMK1), M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), INDMY, Overlap is not allowed.	≥	0.2	um
DUMC.97	DMC5 space to (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), M0C, M0CDMP, (M0GDUM NOT INSIDE DMCMK1), DMC1, Overlap is not allowed.	≥	0.27	um
DUMC.98	DMC5 space to AR, Overlap is not allowed.	≥	0.16	um
DUMC.99	DMC5 space to (ARDUM NOT INSIDE DMCMK1), (ARDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.182	um
DUMC.100	DMC5 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.274	um
DUMC.101	DMC5 space to edge of GT_P96, PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), Cut is not allowed.	≥	0.001	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.102	DMC5 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.103	DMC5 space to (M0CDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.3	um
DUMC.104	DMC5 space to (M0CDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.75	um
DUMC.105	DMC5 space to INST, Overlap is not allowed.	≥	0.21	um
DUMC.106	DMC5 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.35	um
DUMC.107	DMC5 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, Overlap is not allowed.	≥	0	um
DUMC.108	DMC5 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.110	DMC5 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.025	um
DUMC.111	DMC5 space to V0, Overlap is not allowed.	≥	0.04	um
DUMC.112	DMC5 space to edge of HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.007	um
DUMC.113	Inside edge of DG space to DMC5, Outside and cut is not allowed.	≥	0.002	um
DUMC.114	DMC5 space to edge of DGUD, DGV, Cut is not allowed.	≥	0.002	um
DUMC.115	DMC5 space to DMC2, DMC3, DMC4, Overlap is not allowed.	≥	0.192	um
DUMC.116	DMC5 horizontal space to DMC2, DMC3, DMC4, Overlap is not allowed.	≥	0.2	um
DUMC.117	Inside edge of CHIPB space to DMC6, Outside and cut is not allowed.	≥	0.45	um
DUMC.118	DMC6 space to DUMBA, DUMBP, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, AR_H, AR_V, (AR_HDOP NOT INSIDE DMCMK1), (AR_VDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.119	DMC6 space to NPAA_EXT, RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.120	DMC6 space to AA, AADMP, PPAA, M0, M0DMP, (M0DOP NOT INSIDE DMCMK1), M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), INDMY, DG, DGUD, DGV, Overlap is not allowed.	≥	0.2	um
DUMC.121	DMC6 space to (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), M0C, M0CDMP, (M0GDUM NOT INSIDE DMCMK1), DMC1, Overlap is not allowed.	≥	0.27	um
DUMC.122	DMC6 space to AR, Overlap is not allowed.	≥	0.16	um
DUMC.123	DMC6 space to (ARDUM NOT INSIDE DMCMK1), (ARDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.182	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.124	DMC6 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.274	um
DUMC.125	DMC6 space to edge of GT_P96, PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.001	um
DUMC.126	DMC6 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.127	DMC6 space to (M0CDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.3	um
DUMC.128	DMC6 space to (M0CDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.75	um
DUMC.129	DMC6 space to INST, Overlap is not allowed.	≥	0.21	um
DUMC.130	DMC6 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.35	um
DUMC.131	DMC6 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, Overlap is not allowed.	≥	0	um
DUMC.132	DMC6 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.134	DMC6 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.025	um
DUMC.135	DMC6 space to V0, Overlap is not allowed.	≥	0.04	um
DUMC.136	DMC6 space to DMC2, DMC4, Overlap is not allowed.	≥	0.142	um
DUMC.137	DMC6 vertical space to DMC2, DMC4, Overlap is not allowed.	≥	0.192	um
DUMC.138	DMC6 space to DMC3, DMC5, Overlap is not allowed.	≥	0.192	um
DUMC.139	DMC6 horizontal space to DMC3, DMC5, Overlap is not allowed.	≥	0.2	um
DUMC.140	Inside edge of CHIPB space to DMC7, Outside and cut is not allowed.	≥	0.45	um
DUMC.141	DMC7 space to DUMBA, DUMBp, ARDUB, P2DUB, M0DUB, M0CDUB, M0GDUB, AR_H, AR_V, (AR_HDOP NOT INSIDE DMCMK1), (AR_VDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.142	DMC7 space to NPAA_EXT, RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.143	DMC7 space to AA, AADMP, PPAA, M0, M0DMP, (M0DOP NOT INSIDE DMCMK1), M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), INDMY, Overlap is not allowed.	≥	0.2	um
DUMC.144	DMC7 space to (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), M0C, M0CDMP, (M0GDUM NOT INSIDE DMCMK1), DMC1, Overlap is not allowed.	≥	0.27	um
DUMC.145	DMC7 space to AR, Overlap is not allowed.	≥	0.16	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.146	DMC7 space to (ARDUM NOT INSIDE DMCMK1), (ARDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.182	um
DUMC.147	DMC7 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.274	um
DUMC.148	DMC7 space to edge of GT_P96, PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), Cut is not allowed.	≥	0.001	um
DUMC.149	DMC7 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.150	DMC7 space to (M0CDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.3	um
DUMC.151	DMC7 space to (M0CDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.75	um
DUMC.152	DMC7 space to INST, Overlap is not allowed.	≥	0.21	um
DUMC.153	DMC7 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.35	um
DUMC.154	DMC7 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, Overlap is not allowed.	≥	0	um
DUMC.155	DMC7 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.157	DMC7 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.025	um
DUMC.158	DMC7 space to V0, Overlap is not allowed.	≥	0.04	um
DUMC.159	DMC7 space to edge of HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.007	um
DUMC.160	Inside edge of DG space to DMC7, Outside and cut is not allowed.	≥	0.002	um
DUMC.161	DMC7 space to edge of DGUD, DGV, Cut is not allowed.	≥	0.002	um
DUMC.162	DMC7 space to DMC2, DMC3, DMC4, DMC5, DMC6, Overlap is not allowed.	≥	0.192	um
DUMC.163	DMC7 horizontal space to DMC2, DMC3, DMC4, DMC5, DMC6, Overlap is not allowed.	≥	0.2	um
DUMC.164	Inside edge of CHIPB space to DMC8, Outside and cut is not allowed.	≥	0.45	um
DUMC.165	DMC8 space to DUMBA, AA, AADMP, (AADOP NOT INSIDE DMCMK1), PPAA, Overlap is not allowed.	≥	0.067	um
DUMC.166	DMC8 space to DUMBP, Overlap is not allowed.	≥	0.144	um
DUMC.167	DMC8 space to NPAA_EXT, Overlap is not allowed.	≥	0.267	um
DUMC.168	DMC8 space to (AADUM NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), (M0GDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.27	um
DUMC.169	DMC8 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.344	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.170	DMC8 space to edge of GT_P96, Cut is not allowed.	≥	0.04	um
DUMC.171	DMC8 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.172	DMC8 space to M0, M0DMP, (M0DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.047	um
DUMC.173	DMC8 space to M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.05	um
DUMC.174	DMC8 space to INST, Overlap is not allowed.	≥	0.118	um
DUMC.175	DMC8 space to edge of RESNW, DG, DGUD, DGV, Cut is not allowed.	≥	0.001	um
DUMC.176	DMC8 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.07	um
DUMC.177	DMC8 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, V0, Overlap is not allowed.	≥	0	um
DUMC.178	DMC8 space to INDMY, Overlap is not allowed.	≥	0.2	um
DUMC.179	DMC8 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.181	DMC8 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.059	um
DUMC.182	DMC8 space to DMC1, DMC2, DMC3, DMC4, DMC5, DMC6, DMC7, Overlap is not allowed.	≥	0.274	um
DUMC.183	DMC8 space to edge of PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), Cut is not allowed.	≥	0.048	um
DUMC.184	DMC8 space to edge of HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.059	um
DUMC.185	DMC8 space to MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.186	Inside edge of CHIPB space to DMC9, Outside and cut is not allowed.	≥	0.45	um
DUMC.187	DMC9 space to DUMBA, AA, AADMP, (AADOP NOT INSIDE DMCMK1), PPAA, Overlap is not allowed.	≥	0.067	um
DUMC.188	DMC9 space to DUMB_P, Overlap is not allowed.	≥	0.144	um
DUMC.189	DMC9 space to NPAA_EXT, Overlap is not allowed.	≥	0.267	um
DUMC.190	DMC9 space to (AADUM NOT INSIDE DMCMK1), (P2DUM NOT INSIDE DMCMK1), (M0DUM NOT INSIDE DMCMK1), (M0GDUM NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.27	um
DUMC.191	DMC9 space to GT, GTDMP, (GTDUM NOT INSIDE DMCMK1), (GTDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.344	um
DUMC.192	DMC9 space to edge of GT_P96, Cut is not allowed.	≥	0.04	um
DUMC.193	DMC9 space to P2, P2DMP, (P2DOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.18	um
DUMC.194	DMC9 space to M0, M0DMP, (M0DOP NOT INSIDE DMCMK1),	≥	0.047	um

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Rule number	Description	Opt.	Design Value	Unit
	Overlap is not allowed.			
DUMC.195	DMC9 space to M0G, M0GDMP, (M0GDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.05	um
DUMC.196	DMC9 space to INST, Overlap is not allowed.	≥	0.118	um
DUMC.197	DMC9 space to edge of RESNW, DG, DGUD, DGV, Cut is not allowed.	≥	0.001	um
DUMC.198	DMC9 space to DIR, DIRDMP, RESP1, Overlap is not allowed.	≥	0.07	um
DUMC.199	DMC9 space to PLRES, RESP2, LDBK, DMPNP, DSTR, VARMOS, EFUSE, V0, Overlap is not allowed.	≥	0	um
DUMC.200	DMC9 space to INDMY, Overlap is not allowed.	≥	0.2	um
DUMC.201	DMC9 space to OCCDFH, Overlap is not allowed.	≥	0.32	um
blank				
DUMC.203	DMC9 space to DIOMK1, DIOMK2, Overlap is not allowed.	≥	0.059	um
DUMC.204	DMC9 space to DMC1, DMC2, DMC3, DMC4, DMC5, DMC6, DMC7, Overlap is not allowed.	≥	0.274	um
DUMC.205	DMC9 space to edge of PSUB, NW, DNW, SN, SP, (SNDUM NOT INSIDE DMCMK1), (SPDUM NOT INSIDE DMCMK1), Cut is not allowed.	≥	0.048	um
DUMC.206	DMC9 space to edge of HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.059	um
DUMC.207	DMC9 space to MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.208	DMC9 space to DMC8, Overlap is not allowed.	≥	0.35	um
DUMC.209	Inside edge of CHIPB space to DMC10, Outside and cut is not allowed.	≥	0.75	um
DUMC.210	DMC10 space to M0CDUB, Overlap is not allowed.	≥	0.067	um
DUMC.211	DMC10 space to edge of GT_P96, HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.001	um
DUMC.212	DMC10 space to M0, M0DMP, (M0DUM NOT INSIDE DMCMK1), (M0DOP NOT INSIDE DMCMK1), M0G, M0GDMP, (M0GDUM NOT INSIDE DMCMK1), (M0GDOP NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.15	um
DUMC.213	DMC10 space to M0C, M0CDMP, Overlap is not allowed.	≥	1	um
DUMC.214	DMC10 space to (M0CDUM NOT INSIDE DMCMK1), (M0CDOP NOT INSIDE DMCMK1), DMC1, DMC2, DMC3, DMC4, DMC5, DMC6, DMC7, Overlap is not allowed.	≥	0.75	um
DUMC.215	DMC10 space to INST, Overlap is not allowed.	≥	0.18	um
DUMC.216	DMC10 space to MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.217	DMC10 space to OCOVL_NOT_OCOVLM4, Overlap is not allowed.	≥	0.4	um
DUMC.218	Inside edge of CHIPB space to DMC11, Outside and cut is not allowed.	≥	0.75	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.219	DMC11 space to NPAA_EXT, Overlap is not allowed.	≥	0.44	um
DUMC.220	DMC11 space to AA, AADMP, (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), PPAA, Overlap is not allowed.	≥	0.24	um
DUMC.221	DMC11 space to AR_H, (AR_HDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), Overlap is not allowed.	≥	0.144	um
DUMC.222	DMC11 space to edge of GT_P96, HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.001	um
DUMC.223	DMC11 space to DMC1, DMC2, DMC3, DMC4, DMC5, DMC6, DMC7, Overlap is not allowed.	≥	0.75	um
DUMC.224	DMC11 space to INST, Overlap is not allowed.	≥	0	um
DUMC.225	DMC11 space to RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.226	DMC11 space to OCOVL_NOT_OCOVLM4, Overlap is not allowed.	≥	0.4	um
DUMC.227	Inside edge of CHIPB space to DMC12, Outside and cut is not allowed.	≥	0.75	um
DUMC.228	DMC12 space to NPAA_EXT, Overlap is not allowed.	≥	0.44	um
DUMC.229	DMC12 space to AA, AADMP, (AADUM NOT INSIDE DMCMK1), (AADOP NOT INSIDE DMCMK1), PPAA, Overlap is not allowed.	≥	0.24	um
DUMC.230	DMC12 space to AR_H, (AR_HDOP NOT INSIDE DMCMK1), (ARBL NOT INSIDE DMCMK1), DMC11, Overlap is not allowed.	≥	0.144	um
DUMC.231	DMC12 space to edge of GT_P96, HVT_N, HVT_P, SVT_N, SVT_P, LVT_N, LVT_P, ULVT_N, ULVT_P, LFN_N, LFN_P, Cut is not allowed.	≥	0.001	um
DUMC.232	DMC12 space to DMC1, DMC2, DMC3, DMC4, DMC5, DMC6, DMC7, Overlap is not allowed.	≥	0.75	um
DUMC.233	DMC12 space to INST, Overlap is not allowed.	≥	0	um
DUMC.234	DMC12 space to RESNW, MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.4	um
DUMC.235	DMC12 space to OCOVL_NOT_OCOVLM4, Overlap is not allowed.	≥	0.4	um
DUMC.236	DMC11 space to AR, GT, GTDMP, Overlap is not allowed.	≥	0.048	um
DUMC.237	DMC12 space to AR, GT, GTDMP, Overlap is not allowed.	≥	0.048	um
DUMC.238	AADOP/AADUM/ARDOP/ARDUM/AR_HDOP/AR_VDOP/GTDOP/GTDUM/P2DOP/P2DUM/SNDUM/SPDUM/M0DOP/M0DUM/M0CDOP/M0CDUM/M0GDOP/M0GDUM/V0DUM/V0DPDUM must be fully covered by DMCMK1.outside and cut is not allowed. These layer are dedicated for SMIC FEOL and MEOL dummy auto-insertion utility usage, can't be used for manually drawn purpose; Drawn dummy layer please use main layer.			

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Rule number	Description	Opt.	Design Value	Unit
DUMC.239	AADOP/AADUM/ARDOP/ARDUM/AR_HDOP/AR_VDOP/GTDOP/GTDUM/P2DOP/P2DUM/SNDUM/SPDUM/M0DOP/M0DUM/M0CDOP/M0CDUM/M0GDOP/M0GDUM/V0DUM/V0DPDUM must be fully covered by {{{{{{{{DMC1 or DMC2} or DMC3} or DMC4} or DMC5} or DMC6} or DMC7} or DMC8} or DMC9} or DMC10} or DMC11} or DMC12}.outside and cut is not allowed. These layer are dedicated for SMIC FEOL and MEOL dummy auto-insertion utility usage, can't be used for manually drawn purpose; Drawn dummy layer please use main layer.			
DUMC.240	AADUM fixed width	=	0.384	um
DUMC.241	AADUM fixed length	=	1.8	um
DUMC.242	GTDUM fixed width	=	0.22	um
DUMC.243	GTDUM fixed length	=	1.18	um
DUMC.244	ARDUM fixed width	=	0.1	um
DUMC.245	ARDUM fixed length	=	1.236	um
DUMC.246	P2DUM fixed width	=	0.13	um
DUMC.247	P2DUM fixed length	=	1.36	um
DUMC.248	M0DUM fixed width	=	0.1	um
DUMC.249	M0DUM fixed length	=	1.18	um
DUMC.250	M0GDUM fixed width	=	0.125	um
DUMC.251	M0GDUM fixed length	=	2.02	um
DUMC.252	M0CDUM fixed width	=	0.19	um
DUMC.253	M0CDUM fixed length	=	2.16	um
DUMC.254	SNDUM fixed length.	=	2.16	um
DUMC.255	SNDUM fixed width.	=	0.624	um
DUMC.256	SPDUM fixed length.	=	2.16	um
DUMC.257	SPDUM fixed width.	=	0.624	um
DUMC.258	AR_HDOP minimum width.	\geq	0.096	um
DUMC.259	AR_HDOP minimum length.	\geq	0.21	um
DUMC.260	AR_VDOP minimum width	\geq	0.048	um
DUMC.261	AADOP minimum width	\geq	0.096	um
DUMC.262	AADOP minimum length	\geq	0.212	um
DUMC.263	GTDOP minimum width	\geq	0.032	um
DUMC.264	GTDOP minimum length	\geq	0.208	um
DUMC.265	ARDOP fixed width.	=	0.02	um
DUMC.266	ARDOP minimum length	\geq	0.248	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.267	P2DOP minimum width	≥	0.068	um
DUMC.268	P2DOP minimum length	≥	0.87	um
DUMC.269	M0DOP minimum width	≥	0.04	um
DUMC.270	M0DOP minimum length	≥	0.208	um
DUMC.271	M0GDOP minimum width	≥	0.04	um
DUMC.272	M0GDOP minimum length	≥	0.118	um
DUMC.273	M0CDOP minimum width	≥	0.052	um
DUMC.274	M0CDOP minimum length	≥	0.36	um
DUMC.275	Minimum space between AADUM in vertical direction, overlap is not allowed.	≥	0.288	um
DUMC.276	Minimum space between AADUM in horizontal direction, overlap is not allowed.	≥	0.288	um
DUMC.277	Minimum space between GTDUM in vertical direction, overlap is not allowed.	≥	0.164	um
DUMC.278	Minimum space between GTDUM in horizontal direction, overlap is not allowed.	≥	0.164	um
DUMC.279	Minimum space between ARDUM in vertical direction, overlap is not allowed.	≥	0.108	um
DUMC.280	Minimum space between ARDUM in horizontal direction, overlap is not allowed.	≥	0.108	um
DUMC.281	Minimum space between P2DUM in vertical direction, overlap is not allowed.	≥	0.27	um
DUMC.282	Minimum space between P2DUM in horizontal direction, overlap is not allowed.	≥	0.27	um
DUMC.283	Minimum space between M0DUM in vertical direction, overlap is not allowed.	≥	0.164	um
DUMC.284	Minimum space between M0DUM in horizontal direction, overlap is not allowed.	≥	0.164	um
DUMC.285	Minimum space between M0GDUM in vertical direction, overlap is not allowed.	≥	0.27	um
DUMC.286	Minimum space between M0GDUM in horizontal direction, overlap is not allowed.	≥	0.27	um
DUMC.287	Minimum space between M0CDUM in vertical direction, overlap is not allowed.	≥	0.3	um
DUMC.288	Minimum space between M0CDUM in horizontal direction, overlap is not allowed.	≥	0.3	um
DUMC.289	Minimum space between SNDUM in vertical direction, overlap is not allowed.	≥	0.3	um
DUMC.290	Minimum space between SNDUM in horizontal direction, overlap is not allowed.	≥	0.3	um
DUMC.291	Minimum space between SPDUM in vertical direction, overlap is not allowed.	≥	0.3	um

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Rule number	Description	Opt.	Design Value	Unit
	allowed.			
DUMC.292	Minimum space between SPDUM in horizontal direction, overlap is not allowed.	≥	0.3	um
DUMC.293	Minimum space between AR_HDOP in vertical direction, overlap is not allowed.	≥	0.096	um
DUMC.294	Minimum space between AR_HDOP in horizontal direction, overlap is not allowed.	≥	0.096	um
DUMC.295	Minimum space between AR_VDOP in vertical direction, overlap is not allowed.	≥	0.096	um
DUMC.296	Minimum space between AR_VDOP in horizontal direction, overlap is not allowed.	≥	0.142	um
DUMC.297	Minimum space between AADOP in vertical direction, overlap is not allowed.	≥	0.318	um
DUMC.298	Minimum space between AADOP in horizontal direction, overlap is not allowed.	≥	0.318	um
DUMC.299	Minimum space between GTDOP in vertical direction, overlap is not allowed.	≥	0.118	um
DUMC.300	Minimum space between GTDOP in horizontal direction, overlap is not allowed.	≥	0.072	um
DUMC.301	Minimum space between ARDOP in vertical direction, overlap is not allowed.	≥	0.228	um
DUMC.302	Minimum space between ARDOP in horizontal direction, overlap is not allowed.	≥	0.192	um
DUMC.303	Minimum space between P2DOP in vertical direction, overlap is not allowed.	≥	0.19	um
DUMC.304	Minimum space between P2DOP in horizontal direction, overlap is not allowed.	≥	0.19	um
DUMC.305	Minimum space between M0DOP in vertical direction, overlap is not allowed.	≥	0.2	um
DUMC.306	Minimum space between M0DOP in horizontal direction, overlap is not allowed.	≥	0.066	um
DUMC.307	Minimum space between M0GDOP in vertical direction, overlap is not allowed.	≥	0.182	um
DUMC.308	Minimum space between M0GDOP in horizontal direction, overlap is not allowed.	≥	0.094	um
DUMC.309	Minimum space between M0CDOP in vertical direction, overlap is not allowed.	≥	0.18	um
DUMC.310	Minimum space between M0CDOP in horizontal direction, overlap is not allowed.	≥	0.18	um
DUMC.311	Minimum space between AADUM and AADOP, overlap is not allowed.	≥	0.27	um
DUMC.312	Minimum space between GTDUM and GTDOP, overlap is not allowed.	≥	0.27	um
DUMC.313	Minimum space between ARDUM and ARDOP, overlap is not allowed.	≥	0.182	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.314	Minimum space between P2DUM and P2DOP, overlap is not allowed.	\geq	0.27	um
DUMC.315	Minimum space between M0DUM and M0DOP, overlap is not allowed.	\geq	0.27	um
DUMC.316	Minimum space between M0GDUM and M0GDOP, overlap is not allowed.	\geq	0.27	um
DUMC.317	Minimum space between M0CDUM and M0CDOP, overlap is not allowed.	\geq	0.27	um
DUMC.318	DMC10 space to OCCDFH, Overlap is not allowed.	\geq	0.8	um
DUMC.319	DMC11, DMC12 space to OCCDFH, Overlap is not allowed.	\geq	0.32	um
DUMC.320	DMC2, DMC3, DMC4, DMC5, DMC6, DMC7, DMC8, DMC9 space to OCOVL_NOT_OCOVLM4, Overlap is not allowed.	\geq	0.4	um
DUMC.321	DMC1, DMC8, DMC9 space to (V0DUM NOT INSIDE DMCMK1) or (V0DPDUM NOT INSIDE DMCMK1), Overlap is not allowed.	\geq	0	um
DUMC.322	DMC2, DMC3, DMC4, DMC5, DMC6, DMC7 space to (V0DUM NOT INSIDE DMCMK1) or (V0DPDUM NOT INSIDE DMCMK1), Overlap is not allowed.	\geq	0.04	um
DUMC.323	AR_HDOP or AR_VDOP must be fully covered by ARBL.			

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7.13.4 BEOL Dummy Pattern Check Rules for SMIC dummy

Rule number	Description	Opt.	Design Value	Unit
DUMC.401	Space between MnDUM or MnDPDUM and Mn or MnDP (n = 1~3), Overlap is not allowed, except MARKS region.	≥	0.75	um
DUMC.402	Space between MnDUM or MnDPDUM and Mn or MnDP [width≥2um] (n = 1~3), Overlap is not allowed, except MARKS region.	≥	0.898	um
DUMC.403	Space between MnDUM or MnDPDUM and NODMF, MARKG, MARKS. (n = 1~3), Overlap is not allowed.	≥	0.6	um
DUMC.404	Space between MnDUM or MnDPDUM and MnDUB. (n = 1~3), Overlap is not allowed.	≥	0.6	um
DUMC.405	Space between MnDUM or MnDPDUM and INST (for INST only n=1~2), Overlap is not allowed.	≥	0.6	um
DUMC.406	Inside edge of CHIPB space to MnDUM or MnDPDUM (n = 1~3). Outside and cut is not allowed.	≥	2	um
DUMC.407	Space between MnDUM or MnDPDUM and MTFUSE (n = 1~3), Overlap is not allowed.	≥	1	um
DUMC.408	Space between MnDUM or MnDPDUM and 45-degree Mn (n = 1~3), Overlap is not allowed.	≥	0.75	um
DUMC.409	Space between MnDUM and Mn (n≥4), Overlap is not allowed, except MARKS region.	≥	0.75	um
DUMC.410	Space between MnDUM and Mn [width≥2um] (n≥4), Overlap is not allowed, except MARKS region.	≥	0.898	um
DUMC.411	Space between MnDUM and NODMF, MARKG, MARKS (n≥4), Overlap is not allowed.	≥	0.6	um
DUMC.412	Space between MnDUM and MnDUB. (n≥4), Overlap is not allowed.	≥	0.6	um
DUMC.413	Inside edge of CHIPB space to MnDUM (n≥4), Outside and cut is not allowed.	≥	2	um
DUMC.414	Space between MnDUM and 45-degree Mn (n≥4), Overlap is not allowed.	≥	0.75	um
DUMC.415	Space between BnDUM and Bn. Overlap is not allowed, except MARKS region.	≥	1	um
DUMC.416	Space between BnDUM and Bn [width≥2um]. Overlap is not allowed, except MARKS region.	≥	1.5	um
DUMC.417	Space between BnDUM and Bn [width≥4um]. Overlap is not allowed, except MARKS region.	≥	1.898	um
DUMC.418	Space between BnDUM and BnDUB, NODMF, Overlap is not allowed.	≥	0.5	um
DUMC.419	Space between BnDUM and MARKG. Overlap is not allowed.	≥	1	um
DUMC.420	Space between BnDUM and MARKS. Overlap is not allowed.	≥	1	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.421	Inside edge of CHIPB space to BnDUM. Outside and cut is not allowed.	≥	2	um
DUMC.422	Space between BnDUM and 45-degree Bn. Overlap is not allowed.	≥	1	um
DUMC.423	Space between TMnDUM and TMn or TMn_40, Overlap is not allowed, except MARKS region.	≥	0.75	um
DUMC.424	Space between TMnDUM and TMn or TMn_40 [width≥4um], Overlap is not allowed, except MARKS region.	≥	1.898	um
DUMC.425	Space between TMnDUM and TMn or TMn_40 [width≥7.0um], Overlap is not allowed, except MARKS region.	≥	3	um
DUMC.426	Space between TMnDUM and TMn or TMn_40 [width≥10um], Overlap is not allowed, except MARKS region.	≥	4.5	um
DUMC.427	Space between TMnDUM and TMnDUB, NODMF, MARKG, MARKS, Overlap is not allowed.	≥	0.7	um
DUMC.428	Inside edge of CHIPB space to TMnDUM, Outside and cut is not allowed.	≥	2	um
DUMC.429	Space between TMnDUM and 45-degree TMn or TMn_40, Overlap is not allowed, except MARKS region.	≥	0.75	um
DUMC.430	Space between UTMDUM and UTM, Overlap is not allowed, except MARKS region.	≥	2	um
DUMC.431	Space between UTMDUM and UTMDUB, NODMF, MARKG, MARKS, Overlap is not allowed.	≥	2	um
DUMC.432	Inside edge of CHIPB space to UTMDUM, Outside and cut is not allowed.	≥	2	um
DUMC.433	Space between UTMDUM and 45-degree UTM, Overlap is not allowed.	≥	2	um
DUMC.434	Space between ALDUM and ALPA, Overlap is not allowed.	≥	2.85	um
DUMC.435	Space between ALDUM and ALDUB, NODMF, MARKG, MARKS, Overlap is not allowed.	≥	2.85	um
DUMC.436	Inside edge of CHIPB space to ALDUM, Outside and cut is not allowed.	≥	2	um
DUMC.437	Space between ALDUM and 45-degree ALPA, Overlap is not allowed.	≥	2.85	um
DUMC.438	Space between VnDUM (n=1~7) and Vn, Overlap is not allowed, except MARKS region.	≥	0.75	um
DUMC.439	Space between VnDUM (n=1~7) and VnDUB, Overlap is not allowed.	≥	0.6	um
DUMC.440	Space between VnDUM (n=1~7) and MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.6	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.441	Space between VnDUM (n=1~7) and INDMY, Overlap is not allowed.	≥	0.6	um
DUMC.442	Space between VnDUM and MTFUSE (only n=1-3), Overlap is not allowed.	≥	1	um
DUMC.443	Space between BVnDUM and BVn, Overlap is not allowed, except MARKS region.	≥	5	um
DUMC.444	Space between BVnDUM and BVnDUB, Overlap is not allowed.	≥	0.6	um
DUMC.445	Space between BVnDUM and MARKG, MARKS, NODMF, Overlap is not allowed.	≥	0.6	um
DUMC.446	Space between BVnDUM and INDMY, Overlap is not allowed.	≥	0.6	um
DUMC.447	Space between MnDOP or MnDPDOP and Mn (n = 1~3), Overlap is not allowed.	≥	0.12	um
Blank				
Blank				
Blank				
DUMC.451	Space between MnDOP or MnDPDOP to Mn [width≥0.18 um] (n = 1~3), Overlap is not allowed.	≥	0.15	um
DUMC.452	Space between MnDOP or MnDPDOP to Mn [width≥0.50 um] (n = 1~3), Overlap is not allowed.	≥	0.22	um
DUMC.453	Space between MnDOP or MnDPDOP to Mn [width≥1um] (n = 1~3), Overlap is not allowed.	≥	0.45	um
DUMC.454	Space between MnDOP or MnDPDOP to Mn [width≥2um] (n = 1~3), Overlap is not allowed.	≥	0.898	um
DUMC.455	Space between MnDOP or MnDPDOP and MnDUB, NODMF, MARKG, MARKS, LOGO, INST (for INST only n=1~2) (n = 1~3), Overlap is not allowed.	≥	0.6	um
DUMC.456	Inside edge of CHIPB space to MnDOP or MnDPDOP (n = 1~3), Outside and cut is not allowed.	≥	2	um
DUMC.457	Space between MnDOP or MnDPDOP and MTFUSE (only n=1-3), Overlap is not allowed.	≥	1	um
DUMC.458	Space between MnDOP or MnDPDOP to 45-degree Mn (n = 1~3), Overlap is not allowed.	≥	0.175	um
DUMC.459	Space between MnDOP to Mn (n≥4), Overlap is not allowed.	≥	0.12	um
DUMC.460	Space between MnDOP to Mn [width≥0.23um] (n≥4), Overlap is not allowed.	≥	0.24	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.461	Space between MnDOP to Mn [width \geq 1um] ($n \geq 4$), Overlap is not allowed.	\geq	0.45	um
DUMC.462	Space between MnDOP to Mn [width \geq 2um] ($n \geq 4$), Overlap is not allowed.	\geq	0.898	um
DUMC.463	Space between MnDOP and MnDUB, NODMF, MARKG, MARKS, LOGO ($n \geq 4$), Overlap is not allowed.	\geq	0.6	um
DUMC.464	Inside edge of CHIPB space to MnDOP ($n \geq 4$), Outside and cut is not allowed.	\geq	2	um
DUMC.465	Space between MnDOP to 45-degree Mn ($n \geq 4$), Overlap is not allowed.	\geq	0.4	um
DUMC.466	When MnDOP width <0.09um, the short side edge must perpendicular to Mn($n \geq 4$)			
DUMC.467	Space between BnDOP and Bn, Overlap is not allowed.	\geq	0.54	um
DUMC.468	Space between BnDOP and Bn [width \geq 2um], Overlap is not allowed.	\geq	0.898	um
DUMC.469	Space between BnDOP and Bn [width \geq 4um], Overlap is not allowed.	\geq	1.898	um
DUMC.470	Space between BnDOP and BnDUB, NODMF, Overlap is not allowed.	\geq	0.5	um
DUMC.471	Space between BnDOP and MARKG, MARKS. Overlap is not allowed.	\geq	1	um
DUMC.472	Inside edge of CHIPB space to BnDOP, Outside and cut is not allowed.	\geq	2	um
DUMC.473	Space between BnDOP and 45-degree Bn, Overlap is not allowed.	\geq	0.54	um
DUMC.474	Space between TM1DUM and MIM, CTOP, Overlap is not allowed.	\geq	2	um
Blank				
DUMC.476	Space between (((M1DUM OR M1DPDUM) OR M1DOP) OR M1DPDOP) and OCOVLM1CA, OCOVLM1CB, OCOVLM2CA, OCOVLM4, OCOVLV0, Overlap is not allowed.	\geq	0.6	um
DUMC.477	Space between (((M2DUM OR M2DPDUM) OR M2DOP) OR M2DPDOP) and OCOVLM2CA, OCOVLM4, Overlap is not allowed.	\geq	0.6	um
DUMC.478	Space between (((M3DUM OR M3DPDUM) OR M3DOP) OR M3DPDOP) and OCOVLM4, Overlap is not allowed.	\geq	0.6	um
DUMC.479	Space between (M4DUM OR M4DOP) and OCOVLM4, Overlap is not allowed.	\geq	0.6	um
DUMC.480	M1DOP/M1DUM/M1DPDOP/M1DPDUM/M2DUM/M2DOP/M2DP DUM/M2DPDOP/M3DUM/M3DOP/M3DPDUM/M3DPDOP/M4DU M/M4DOP/M5DUM/M5DOP/M6DUM/M6DOP/M7DUM/M7DOP/V 1DUM/V2DUM/V3DUM/V4DUM/V5DUM/V6DUM/BV1DUM/BV 2DUM/B1DUM/B1DOP/B2DUM/B2DOP/UTMDUM/TM1DUM/TM 2DUM/ALDUM/MIMDUM/CTOPDUM/V0DUM/V0DPDUM must be covered by DMCMK2. Outside and cut is not allowed.			

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Rule number	Description	Opt.	Design Value	Unit
	These layers are dedicated for SMIC BEOL dummy auto-insertion utility usage, can't be used for manually drawn purpose. Drawn dummy layer please use main layer.			
DUMC.481	MnDUM or MnDPDUM (n=1~3) minimum width.	\geq	0.118	um
DUMC.482	MnDUM (n \geq 4) minimum width.	\geq	0.11	um
DUMC.483	MnDOP or MnDPDOP (n=1~3) minimum width.	\geq	0.06	um
DUMC.484	MnDOP (n \geq 4) minimum width.	\geq	0.06	um
DUMC.485	BnDUM (n=1~2) fixed width.	=	0.6, 0.4	um
DUMC.486	BnDOP (n=1~2) fixed width.	=	0.2	um
DUMC.487	BVnDUM (n=1~2) fixed width.	=	0.09	um
DUMC.488	TMnDUM (n=1~2) minimum width.	\geq	1.0	um
DUMC.489	UTMDUM fixed width.	=	3.5	um
DUMC.490	ALDUM fixed width.	=	7.0	um
DUMC.491	MIMDUM fixed width.	=	0.78	um
DUMC.492	CTOPDUM fixed width.	=	1.58	um
DUMC.493	Space between (MnDUM or MnDPDUM) and MnDUM, MnDPDUM (n=1~3), Overlap is not allowed.	\geq	0.094	um
DUMC.494	Space between MnDUM and MnDUM (n \geq 4), Overlap is not allowed.	\geq	0.102	um
DUMC.495	Space between (MnDOP or MnDPDOP) and MnDOP, MnDPDOP (n=1~3), Overlap is not allowed.	\geq	0.08	um
DUMC.496	Space between MnDOP and MnDOP (n \geq 4), Overlap is not allowed.	\geq	0.06	um
DUMC.497	Space between (MnDUM or MnDPDUM) and MnDOP, MnDPDOP (n=1~3), Overlap is not allowed.	\geq	0.2	um
DUMC.498	Space between MnDUM and MnDOP (n \geq 4), Overlap is not allowed.	\geq	0.2	um
DUMC.499	Space between BnDUM to BnDUM (n=1~2).	\geq	0.2	um
DUMC.500	Space between BnDOP to BnDOP (n=1~2).	\geq	0.14	um
DUMC.501	Space between BnDUM to BnDOP (n=1~2).	\geq	0.14	um
DUMC.502	Space between BVnDUM to BVnDUM (n=1~2).	\geq	0.122	um
DUMC.503	Space between TMnDUM to TMnDUM (n=1~2).	\geq	0.75	um
DUMC.504	Space between UTMDUM to UTMDUM.	\geq	3	um
DUMC.505	VnDUM width.(n \geq 1)	=	0.096	um
DUMC.506	Space between VnDUM and VnDUM (n \geq 1), Overlap is not allowed.	\geq	0.242	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.507	VnDUM enclosure by bottom metal dummy (MnDUM or MnDPDUM) (n=1~3) (all sides), Outside is not allowed. VnDUM enclosure by bottom metal dummy MnDUM (n≥4) (all sides), Outside is not allowed. Base on metal option to select bottom metal dummy.	≥	0.007	um
DUMC.508	VnDUM(n=1~2) enclosure by upper metal dummy (MnDUM or MnDPDUM) (n=2~3) (all sides), Outside is not allowed. VnDUM (n≥3) enclosure by upper metal dummy MnDUM (n≥4) (all sides), Outside is not allowed. Base on metal option to select upper metal dummy.	≥	0.007	um
DUMC.509	Space between {M1DUM or M1DPDUM} and OCCDFH, OCCDM1, Overlap is not allowed.	≥	0.75	um
DUMC.510	Space between (MnDUM or MnDPDUM) and OCCDMn (n=2~3), Overlap is not allowed.	≥	0.75	um
DUMC.511	Space between MnDUM and OCCDMn (n≥4), Overlap is not allowed.	≥	0.75	um
DUMC.512	Space between BnDUM and OCCDBn (n=1~2), Overlap is not allowed.	≥	1	um
DUMC.513	Space between (M1DOP or M1DPDOP) and OCCDFH, OCCDM1, Overlap is not allowed.	≥	0.335	um
DUMC.514	Space between (MnDOP or MnDPDOP) and OCCDMn (n=2~3), Overlap is not allowed.	≥	0.335	um
DUMC.515	Space between MnDOP and OCCDMn (n≥4), Overlap is not allowed.	≥	0.335	um
DUMC.516	Space between BnDOP and OCCDBn (n=1~2), Overlap is not allowed.	≥	0.54	um
DUMC.517	Space between MIMDUM or CTOPDUM and MIM, CTOP, Overlap is not allowed.	≥	2.000	um
DUMC.518	Space between MIMDUM or CTOPDUM and MIMDUB, CTOPDUB, NODMF, MARKG, MARKS, TM1, Overlap is not allowed.	≥	2.000	um
DUMC.519	Inside edge of CHIPB space to MIMDUM, CTOPDUM, Outside is not allowed.	≥	2.000	um
DUMC.520	Space between MIMDUM and 45-degree MIM, Overlap is not allowed.	≥	2.000	um
DUMC.521	Space between CTOPDUM and 45-degree CTOP, Overlap is not allowed.	≥	2.000	um
DUMC.522	MIMDUM must be enclosed by CTOPDUM, outside and cut is not allowed.	=	0.400	um
DUMC.523	V0DUM width.	=	0.096	um
DUMC.524	Space between (V0DUM or V0DPDUM) and V0DUM, V0DPDUM, Overlap is not allowed.	≥	0.106	um
DUMC.525	Space between (V0DUM or V0DPDUM) and V0, Overlap is not allowed.	≥	0.75	um
DUMC.526	(V0DUM or V0DPDUM) enclosure by M0GDUM, outside is not allowed.	≥	0	um

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Rule number	Description	Opt.	Design Value	Unit
DUMC.527	(V0DUM or V0DPDUM) enclosure by (M1DUM or M1DPDUM), outside is not allowed.	≥	0	um
DUMC.528	BVnDUM(n=1~2) enclosure by bottom metal dummy (all sides), outside is not allowed. (base on metal option to select bottom metal)	≥	0.01	um
DUMC.529	BVnDUM enclosure by upper metal dummy (n=1~2) (all sides), outside is not allowed.(base on metal option to select upper metal)	≥	0.149	um

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7.13.5 Redundant Via Insertion Guidelines

For better yield and reliability, it is strongly recommended to utilize SMIC offered qualified redundant via auto insertion utilities to do redundant via insertion which will replace the single square vias with the rectangular vias in 1x Vn(n=1-7) layers wherever the layout and design rules permit. Application notice please refer to redundant via utilities; designers can contact SMIC CE to get the utilities.

Features of this utility:

1. The utility strictly follows design rules for these layers Mn(n=1-8), Vn(n=1-7).
2. The new generated redundant vias will be marked by VnRM (n=1-7).
3. For putting redundant vias to replace the single square vias with the rectangular vias in 1x Vn layers as required by design rules, metal lines can be extended. Therefore, designers should ensure LVS,DRC&timing result pass after using redundant via utilities. Designers can also refer to design reference flow offered by SMIC for LVS check and timing analysis.

The following layers will prevent the utility from inserting redundant via:

1. VnRB (n=1-7) are the block layers for redundant via auto insertion. User can draw these layers where the DFM Via layout enhancement is not desired, especially for timing or resistance sensitive circuit area.
2. INDMY(212;0), LOGO(26;0), MARKG(189;0), MARKS(189;151), MnDUB (n=1-8), VnDUB(n=1-7), INST are also redundant via block layers



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7.14 DFM (Design for Manufacturing) rules

7.14.1 Manufacturability Enhancement Rules

7.14.1.1 P2 ME rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
P2.S.1a.ME	Space between two P2s, except poly center-to-center space = 0.09um design, except INST region	≥	0.096	device	off	1
P2.S.4b.ME	Space between P2 and AOP_AA in P2 width direction (overlap is not allowed), except P2 to pick-up space = 0.014um and INST region	≥	0.02	device	off	1
P2.EX.1a.ME	P2 extension outside of AOP_GT (width = 0.016um) in P2 length direction in GT_P96 region, except INST region	≥	0.04	Other process	off	1
P2.EX.1b.ME	P2 extension outside of AOP_GT (width = 0.018um) in P2 length direction in GT_P96 region, except INST region	≥	0.039	Other process	off	1
P2.EX.1c.ME	P2 extension outside of AOP_GT (width = 0.02um) in P2 length direction in GT_P96 region, except INST region	≥	0.038	Other process	off	1
P2.EX.1c1.ME	P2 extension outside of AOP_GT (width = 0.022um) in P2 length direction in GT_P96 region, except INST region	≥	0.037	Other process	off	1
P2.EX.1d.ME	P2 extension outside of AOP_GT (width = 0.024um) in P2 length direction in GT_P96 region, except INST region	≥	0.036	Other process	off	1

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7.14.1.2 M0 ME rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
M0.S.4. ME	Short side space between AOP_M0 (width = 0.04/0.042um, PRL > -0.05um) except the following conditions and INST region: Short side space \geq 0.086 um (length \geq 0.23 um, either one short side INTERACT M0C (width = 0.054um), short side (NOT INTERACT M0C) space to M0G \geq 0.04 um).	\geq	0.1	Other process	off	1

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7.14.1.3 M0G ME rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
M0G.S.1c. ME	Space between the short side of AOP_M0G (width = 0.04um) when PRL > -0.02um (DOP_M0G overlap with M0G is not allowed), except INST region	≥	0.078	Other process	off	1
M0G.S.3a. ME	Center-to-center space between M0G (width = 0.05um), except INST region. DRC only flag opposite space.	≥	0.102	Other process	off	1
M0G.S.3b. ME	Center-to-center space between M0G (width = 0.05um) when PRL < 0.05um, except INST region	≥	0.106	Other process	off	1
M0G.S.7a. ME	Space between M0G and AOP_AA (Overlap is not allowed, except OCCD or ((M0G AND AOP_AA) INTERACT M0)) (Except ME.M0G.S.7b, INST region).	≥	0.039	Other process	off	1
M0G.S.7b. ME	Space between M0G and AOP_AA in GATE poly direction. (Overlap is not allowed) Except OCCD, INST, or M0G and AA interact same (M0 NOT M0C).	≥	0.019	Other process	off	1
M0G.S.10a. ME	Space between M0G (width = 0.04/0.06um, not interact AA) to AOP_GT in GT_P96 region, except INST region	≥	0.031	Other process	off	1
M0G.S.21a. ME	Space between long side of M0G (width = 0.04/0.06/0.09um) and short side of M0 (short side NOT INTERACT M0C) when PRL ≥ -0.018um. Which rule is not applied for INST region and 7.5T standard cell design.	≥	0.035	Other process	off	1
M0G.S.21a1.	Space between long side of M0G	≥	0.032	Other	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
ME	(width = 0.04/0.06/0.09um) and short side of M0 (short side NOT INTERACT M0C) when PRL \geq -0.018um, for 7.5T standard cell design. Which rule is not applied for INST region			process		
M0G.S.25a. ME	Space between M0G (width = 0.05um) and the short side of M0 (short side NOT INTERACT M0C) when PRL \geq -0.018 um. Which rule is not applied for INST region	\geq	0.03	Other process	off	1

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7.14.1.4 V0 ME rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
V0.S.10. ME	Projection space between square V0 and the M1 concave corner (square V0 enclosure of M1 edge $< 0.003\mu m$ at opposite side of M1 concave corner; the concave corner with M1 width $\leq 0.034\mu m$ and jog height $\geq 0.004\mu m$), except INST region	\geq	0.012	Other process	off	1
V0.EN.1 7a. ME	V0 enclosure by M1 (short side of M1 width $> 0.046\mu m$ and $\leq 0.056\mu m$) for two opposite sides with the other two sides $\geq 0.009\mu m$ when V0 interact with M0G (width = $0.05\mu m$), for 9T standard cell design, except INST region	\geq	0.025	Other process	off	1
V0.EN.1 7a1. ME	V0 enclosure by M1 (short side of M1 width $> 0.046\mu m$ and $\leq 0.056\mu m$) for two opposite sides with the other two sides $\geq 0.006\mu m$ when V0 interact with M0G (width = $0.05\mu m$), for 7.5T standard cell design, except INST region	\geq	0.025	Other process	off	1
V0.EN.2 7. ME	V0 enclosure by M1 edge at opposite side of M1 inner vertex (projection space between V0 and the M1 inner vertex = $0 \sim 0.012\mu m$; the inner vertex with width = $0.035 \sim 0.046\mu m$ and jog height $\geq 0.004\mu m$), except INST region	\geq	0.003	Other process	off	1

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7.14.1.5 M1 ME rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
M1.S.13. ME	Space between M1 and line-end (width $< 0.046\mu m$) when PRL $> -0.016\mu m$, except INST region.	\geq	0.07	Other process	off	1
M1.S.13a. ME	Space between M1 and line-end ($0.046\mu m \leq M1 \text{ width} \leq 0.049\mu m$), when PRL $> -0.016\mu m$, except INST region.	\geq	0.036	Other process	off	1
M1.S.14.ME	Space between M1 line-end and line-end (width $< 0.046\mu m$) when PRL $> -0.016\mu m$, except INST region.	\geq	0.081	Other process	off	1
M1.S.50. ME	Space between M1 outside vertex (M1 line-end outer vertex or L-shape outer vertex) and nearby L-shape inner vertex. DRC flag if both projection space $< 0.036\mu m$, except INST region	\geq	0.047	Other process	off	1
M1.R.6.ME	It's not allowed to use U-shape M1, except INST region. DRC check condition: 1. with at least one RV0 or RV1; 2. M1 width $W \leq 0.038\mu m$; 3. $S \leq 0.12\mu m$			Other process	off	1
M1.R.7.ME	It's not allowed to use Hook-shape M1, except INST region. Hook-shape M1 definition: (1) Hook-end line width ($W_1 \leq 0.05\mu m$), length($L_1 \leq 0.15\mu m$), $\Delta L > 0.1\mu m$ and Hook-end interact one via (2) $W_2/W_3 \text{ width} \leq 0.072\mu m$. (3) Space between two M1 arms($S_1 \leq 0.1\mu m$). (4) Space between via and another M1 $S_2 \leq 0.038\mu m$ when PRL $> -0.015\mu m$ DRC waive if hook-end enclosure			Other process	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Prior ity
	V0/V1 \geq 0.05um					
M1.ORCS.2. ME	Continuous three or more same color M1 spacing $<$ 0.063um is not allowed, except INST region. DRC flag if all these M1 space $<$ 0.063um.			Other process	off	1

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7.14.1.6 Vy ME rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
Vy.EN.2a. ME	Vy enclosure by M1 or Mxy (width < 0.05um) for two opposite sides with the other two side ≥ 0um. (M1/Mxy is the metal underneath Vy), except INST region	≥	0.032	Other process	off	1
Vy.EN.2c. ME	Vy enclosure by M1 or Mxy (width ≥ 0.05um) for two opposite sides with the other two side ≥ 0.009um. (M1/Mxy is the metal underneath Vy), except INST region	≥	0.025	Other process	off	1
Vy.EN.16a. ME	Vy enclosure by Mxy+1 (width = 0.032um) for two opposite sides with the other two sides ≥ 0um, except INST region	≥	0.039	Other process	off	1

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7.14.1.7 Mxy ME rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
Mxy.S.9.M E	Space between Mxy line and line-end ($W < 0.046\mu m$) when $PRL > -0.022\mu m$, except INST region	\geq	0.07	Other process	off	1
Mxy.A.1.M E	M2 Area, except INST region	\geq	0.0066	Other process	off	1
Mxy.R.6.M E	U-shape Mxy is not allowed, except INST region. DRC check condition: 1. With at least one RVy or RVy-1 2. Mxy width $W \leq 0.038\mu m$ 3. $S \leq 0.12\mu m$			Other process	off	1
Mxy.R.7.M E	It's not allowed to use Hook-shape Mxy, except INST region. Hook-shape Mxy definition: (1) Hook-end line width($W1 \leq 0.05\mu m$, length ($L1 \leq 0.15\mu m$, $\Delta L > 0.1\mu m$ and Hook-end interact one via, (2) $W2/W3 \leq 0.072\mu m$. (3) Space between two Mxy arms($S1 \leq 0.1\mu m$). (4) Space between via and another Mxy $S2 \leq 0.038\mu m$ when $PRL > -0.015\mu m$ DRC waive if hook-end enclosure via $\geq 0.05\mu m$			Other process	off	1

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7.14.2 DFM rules

All the recommendations are listed in the following DFM rule section, it is recommended to follow them as much as possible, which can achieve larger process window, better device and reliability performance, and higher yield, but they are not the gating items for tape-out.

DFM rules are grouped with different priority levels, and higher priority indicates higher risk of manufacturability and yield loss when the rule is not obeyed. It's strongly recommended for designers to follow priority-1 DFM rules.

SMIC PDK provide minima design rule based Pcell by default, also provide DFM rule based Pcell by option. Designers can base on self-requirement to use them by choice. SMIC DFM based Pcell has followed priority-1 DFM rules but not followed priority-2 DFM rules.

DRC check methodology: there are two switches setting for DFM priority-1 and priority-2 rules respectively, and DRC switch defalut turn off. Designers can turn on the DRC switch to check DFM rules if feel needs.

7.14.2.1 GT DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
GT.S.20a.DFM	Empty space between (ALL_GT NOT P2), except DIR, RESNW, OCCD, OCOVL, LOGO, and ((Chip corner stress relief and MARKS) su 0.45um) regions. DRC flags (((chip NOT (ALL_GT NOT P2)) sd 0.45um) su 0.45um)	≤	0.9	CMP	off	1
GT.R.4.DFM	Recommend width of AOP_GT (width \leq 0.024um INTERACT the same AA) must be the same, except INST region. DRC flag AOP_GT width not equal on same AA when there has at least one AOP_GT width \leq 0.024um			Device	off	1
GT.R.20.DFM	GT abut with EMPTY_GT region in S/D direction is not allowed when meet either one of below condition. EMPTY_GT region definition: ((chip NOT ALL_GT) sd 0.125um) su 0.125um) with one horizontal edge length > 0.35um and vertical edge length \geq 0.25um.			Litho	off	2

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
	1) (ALL_GT NOT P2) width \leq 0.2um and area \leq 0.0055um ² 2) (ALL_GT NOT P2) abut EMPTY_GT length in GATE poly direction \geq 0.25um.					
GT.R.21.DFM	It's not allowed to use GT on AA edge for routing. DRC flag (Edge GT not P2) electrically connect both P+AA and N+AA.			Device	off	2
GT.R.23.DFM	It is not recommended to use GATE at L-shape AA corner.			Device	off	1
GT.R.24.DFM	It is not recommended to use NMOS with both SA and SB > 15CPP (Critical poly pitch), except ESD device.			Device	off	2

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7.14.2.2 P2 DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
P2.S.7.DFM	Recommended P2 space to GATE in GATE poly direction when AA width \leq 0.576um, poly \leq 0.02um, PRL > -0.215um	\geq	0.12	Device	off	1
P2.S.8.DFM	Recommended P2 space to GATE in GATE poly direction when AA width \leq 0.576um, poly \leq 0.024um, PRL > -0.23um inside GT_P96 region	\geq	0.12	Device	off	1
P2.S.9.DFM	For NMOS, Channel length \leq 24nm, SA/SB=(192nm-GT/2) or (180-GT/2): If both left and right first adjacent GT is cut, Fin number=2, suggest P2 to AA space \geq 40nm, Fin number =3&4, suggest P2 to AA space \geq 25nm			Device	off	1
P2.S.10.DFM	For PMOS, Channel length \leq 24nm: If both left and right first adjacent GT is cut, Fin number =2, suggest P2 to AA space \geq 68nm, Fin number = 3&4, suggest P2 to AA space \geq 50nm if only one side adjacent GT is cut, suggest P2 to AA space \geq 25nm			Device	off	1

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7.14.2.3 SP DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
S.P.S.10.DFM	For PMOS, Channel length \leq 24nm: Fin number \leq 4, (SA=SB) \leq 0.096um, suggest N/P boundary space to AA space \geq 80nm			Device	off	1

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7.14.2.4 M0 DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
M0.R.10.DFM	It's not recommended to use M0 P-to-N routing with M0G on adjacent GT, except INST. DRC flag condition: (M0 not M0C) electrically connect both P+AA and N+AA and with M0G on adjacent GT DRC waive if M0G and M0 PRL< 0um in GATE poly direction.			Device	off	1
M0.R.11.DFM	It is not allowed M0 (M0 width = 0.04/0.042um) $\Delta L > 0.1\text{um}$, except single M0 pickup case. DRC highlight M0 segment (length > 0.1um) without an adjacent M0.			Device	off	1
M0.R.12.DFM	It is not allowed the outmost (M0 on AA) (M0 width = 0.04/0.042um) without an adjacent (M0 on STI), except pick-up and DSTR region. DRC searching region: 0~0.12um from AA in S/D direction.			Device	off	1

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7.14.2.5 V0 DFM rules

7.14.2.5.1 Square V0 DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
V0.EN.1.DFM	<p>Recommended square V0 enclosure of M0 (width = 0.04/0.042/0.054um) is defined by V0.EN.2.DFM/V0.EN.3.DFM respectively.</p> <p>Recommended square V0 enclosure of M0G (width = 0.04/0.05um) is defined by V0.EN.4.DFM/V0.EN.5.DFM respectively.</p> <p>DRC waive the violation either V0/M0 or V0/M0G pass the enclosure rules when V0 INTERACT (M0 AND M0G).</p>			Other process	off	1
V0.EN.2.DFM	Recommended square V0 enclosure by (M0 NOT M0C) which M0 width = 0.04/0.042um for two opposite sides with the other two sides \geq 0.004um	\geq	0.020	Other process	off	1
V0.EN.3.DFM	Recommended square V0 enclosure by (M0 NOT M0C) which M0 width = 0.054um for two opposite sides with the other two sides \geq 0.011um	\geq	0.025	Other process	off	1
V0.EN.4.DFM	Recommended square V0 enclosure by MOG with width = 0.04um for two opposite sides with the other two sides \geq 0.004um	\geq	0.018	Other process	off	1
V0.EN.5.DFM	Recommended square V0 enclosure by MOG with width = 0.05um for two opposite sides with the other two sides \geq 0.009um	\geq	0.005	Other process	off	1
V0.EN.9.DFM	Recommended square V0 enclosure by M1 is defined by either V0.EN.10.DFM or V0.EN.13.DFM or			Other process	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Prior ity
	V0.EN.13a.DFM					
V0.EN.10.DFM	Recommended square V0 enclosure by M1 for all sides to avoid high Rc.	\geq	0.02	Other process	off	1
V0.EN.13.DFM	Recommended square V0 enclosure by M1(width < 0.05um) for two opposite sides with the other two sides $\geq 0.007\text{um}$	\geq	0.05	Other process	off	1
V0.EN.13a.DFM	Recommended square V0 enclosure by M1(width $\geq 0.05\text{um}$) for two opposite sides with the other two sides $\geq 0.009\text{um}$	\geq	0.05	Other process	off	1
V0.EN.27.DFM	Enclosure by M1 edge at opposite side of M1 inner vertex (projection space between V0 and the M1 inner vertex $< 0.012\text{um}$; the inner vertex with width = 0.035~0.046um and jog height $\geq 0.004\text{um}$)	\geq	0.003	Other process	off	1
V0.S.5.DFM	Space between V0 and M0G at different net when PRL $> -0.012\text{um}$	\geq	0.04	Litho	off	1
V0.S.23.DFM	Recommended protection space between square V0 and the M1 concave corner (square V0 enclosure by M1 edge $< 0.003\text{um}$ at opposite side of M1 concave corner; the concave corner with M1 width $\leq 0.034\text{um}$ and jog length $\geq 0.004\text{um}$)	\geq	0.03	Litho	off	1
V0.R.1.DFM	Only one same color square V0 in 0.5*0.5um area is not allowed. DRC waive if ≥ 5 V0 exist in the 0.5*0.5um area.			Litho	off	2

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7.14.2.5.2 Rectangular V0 DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Prior ity
RV0.EN.1.DFM	<p>Recommended rectangular V0 enclosure of M0 (width = 0.04/0.042/0.054um) is defined by RV0.EN.2.DFM/RV0.EN.3.DFM respectively.</p> <p>Recommended rectangular V0 enclosure of M0G (width = 0.04um/0.06um) is defined by RV0.EN.4.DFM/ RV0.EN.6.DFM respectively.</p> <p>DRC waive the violation either V0/M0 or V0/M0G pass the enclosure rules when V0 INTERACT (M0 AND M0G).</p>			Other process	off	1
RV0.EN.2.DFM	Recommended rectangular V0 long side enclosure by (M0 NOT MOC) which M0 width = 0.04/0.042um for two opposite sides with the other two sides = 0.004um	≥	0.022	Other process	off	1
RV0.EN.3.DFM	Recommended rectangular V0 long side enclosure by (M0 NOT MOC) which M0 width = 0.054um for two opposite sides with the other two sides = 0.011um	≥	0.022	Other process	off	1
RV0.EN.4.DFM	Recommended rectangular V0 enclosure by M0G with width = 0.04um for two opposite sides with the other two sides = 0.004um	≥	0.022	Other process	off	1
RV0.EN.5.DFM	Recommended V0 enclosure by M0G with width = 0.06um for two opposite sides with the other two sides = 0.014um	≥	0.033	Other process	off	1
RV0.EN.7.DFM	Recommended RV0 enclosure by M1 is defined by either V0.EN.8.DFM or V0.EN.9.DFM.			Other process	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Prior ity
RV0.EN.8.DFM	Recommended RV0 enclosure by M1 for all sides to avoid high Rc.	\geq	0.02	Other process	off	1
RV0.EN.9.DFM	Recommended RV0 enclosure by M1 for two opposite sides with the other two sides $\geq 0.007\mu m$	\geq	0.025	Other process	off	1

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7.14.2.6 M1 DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
M1.W.1. DFM	Recommended M1 width to reduce the line open possibility, except MOMDMY and FUSEMK1 regions	\geq	0.046	Defect	off	1
M1.S.1.D FM	Recommended M1 space to reduce the short possibility, except MOMDMY region	\geq	0.044	Litho	off	1
M1.S.7.D FM	Recommended M1 space when either one M1 width $> 0.09\mu m$	\geq	0.072	Litho	off	1
M1.S.8.D FM	Recommended M1 space when either one M1 width $> 0.12\mu m$	\geq	0.106	Litho	off	1
M1.S.9.D FM	Recommended M1 space when either one M1 width $> 0.18\mu m$	\geq	0.126	Litho	off	1
M1.S.10. DFM	Recommended M1 space when either one M1 width $> 0.27\mu m$	\geq	0.144	Litho	off	1
M1.S.13a .DFM	Space between M1 and line-end ($W < 0.046\mu m$, $PRL > -0.022\mu m$)	\geq	0.07	Litho	off	1
M1S.13b. DFM	Space between M1 and line-end ($0.046 < W \leq 0.051\mu m$, $PRL > -0.022\mu m$)	\geq	0.063	Litho	off	1
M1S.13c. DFM	Space between M1 line-end ($W \leq 0.051\mu m$) and line-end ($W < 0.048\mu m$, $PRL > -0.022\mu m$)	\geq	0.081	Litho	off	1
M1.S.17. DFM	Space between M1 line and (V0 or V1) enclosed by dense M1 line-end (when $PRL (L1) > -0.025\mu m$; $E \leq 0.045\mu m$) Dense M1 line end definition: ($W+S < 0.11\mu m$, the $PRL (L2)$ of (V0 or V1) and neighboring M1 line $> 0\mu m$) This rule isn't applicable for SRAM region.	\geq	0.117	Litho	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
M1.S.19. DFM	Recommended M1 forbidden zone of ((W1+S1+W2+S2) or (S1+W2+S2+W3)) when M1 width is < 0.037um. DRC flags edge of forbidden zone, and waive the violation in same polygon.	=	0.14~0. 159	Litho	off	1
M1.S.35. DFM	Space between M1 outside vertex (M1 line-end outer vertex or L-shape outer vertex) and nearby L-shape inner vertex. DRC flag if both projection space < 0.036um.	≥	0.047	Litho	off	1
M1.A.1.D FM	M1 area, except INST region	≥	0.01	Litho	off	1
M1.OR.1 5.DFM	Continuous 3 or more M1 with spacing < 0.063um is not allowed. DRC flag if all these M1 space < 0.063um.			Litho	off	2
M1.R.6.D FM	It's not recommended to use U-shape M1. DRC check condition: 1. With at least one RV0 or RV1; 2. M1 width $W \leq 0.038\text{um}$; 3. $S \leq 0.12\text{um}$; This rule is not applied for INST region .			Litho	off	1
M1.R.7.D FM	It's not recommended to use Hook-shape M1. Hook-shape M1 definition: (1) Hook-end line width (W_1) is $\leq 0.05\text{um}$, length (L_1) $\leq 0.15\text{um}$, $\Delta L > 0.1\text{um}$ and Hook-end interact one via/rectangle via, (2) W_2/W_3 width $\leq 0.072\text{um}$. (3) Space between two M1 arms (S_1) $\leq 0.1\text{um}$. (4) Space between via and another M1 $S_2 \leq 0.038\text{um}$ when $PRL > -0.015\text{um}$ DRC waive if hook-end enclosure $V_0/V_1 \geq 0.05\text{um}$ This rule is not applied for INST region			Litho	off	1
M1.R.8.D FM	It's not recommended to use dense M1 line end pattern. DRC flag conditions:			Litho	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
	(1) Middle line width(W_1) $\leq 0.038\mu m$, both two neighbour M1 lines width $\leq 0.064\mu m$; (2) Both the V0 dense region (dense region definition: region formed by V0 horizontal edge extension $0.038\mu m$, vertical edge extension $0.05\mu m$) horizontal edges interact neighbour M1 line-end. DRC waive if M1 enclosure $V_0 > 0.05\mu m$. This rule is not applied for INST region					
M1.R.9.D FM	It's not recommended to use dense M1 3-bar pattern. DRC flag conditions: (1) Middle M1 line width (W_1) is $\leq 0.048\mu m$, both two neighbour M1 line width $\leq 0.064\mu m$ and interact square or rectangle V0 or V1. (2) M1 Space to both via (S_1/S_2) = $0.058\sim 0.063\mu m$. (3) The via PRL: $-0.1 < PRL < 0.1\mu m$. (4) Both neighbour M1 enclosure V_0 or $V_1 < 0.05\mu m$ This rule is not applied for INST region			Litho	off	1

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7.14.2.7 Vy DFM rules

7.14.2.7.1 Square Vy DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
Vy.EN.1.DFM	Recommended square Vy enclosure by M1/Mxy is defined by either Vy.EN.2.DFM or Vy.EN.3.DFM			Other process	off	1
Vy.EN.2.DFM	Recommended square Vy enclosure by M1/Mxy for two opposite sides with the other two sides $\geq 0.007\mu m$, except FUSEMK1 region	\geq	0.05	Other process	off	1
Vy.EN.2b.DFM	Recommended enclosure by M1 or Mxy (width $< 0.05\mu m$) along width direction must be equal or 1nm difference (M1/Mxy is the metal underneath Vy.)			Other process	off	1
Vy.EN.3.DFM	Recommended square Vy enclosure by M1, Mxy for all sides to avoid high Rc, except FUSEMK1 region	\geq	0.02	Other process	off	1
Vy.EN.14.DFM	Recommended square Vy fully enclosure by Mxy+1/1.25xMy is defined by either Vy.EN.16.DFM, Vy.EN.16a.DFM or Vy.EN.16b.DFM, which Mxy+1/1.25xMy is the metal layer directly above Vy.			Other process	off	1
Vy.EN.16.DFM	Recommended square Vy enclosure by Mxy+1/1.25xMy for all sides	\geq	0.02	Other process	off	1
Vy.EN.16a.DFM	Recommended square Vy enclosure by Mxy+1/1.25xMy (width $< 0.05\mu m$) for two opposite sides with the other two sides $\geq 0.007\mu m$	\geq	0.05	Other process	off	1
Vy.EN.16b.DFM	Recommended square Vy enclosure by Mxy+1/1.25xMy (width $\geq 0.05\mu m$) for two opposite sides with the other two sides $\geq 0.009\mu m$	\geq	0.05	Other process	off	1

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7.14.2.7.2 Rectangular Vy DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Pri priorit y
RVy.EN.1.DFM	Recommended RVy enclosure by M1/Mxy is defined by either RVy.EN.2.DFM or RVy.EN.2a.DFM.			Other process	off	1
RVy.EN.2.DFM	Recommended RVy enclosure by M1/Mxy for two opposite sides with the other twosides $\geq 0.007\text{um}$	\geq	0.025	Other process	off	1
RVy.EN.2a.DFM	Recommended RVy enclosure by M1,Mxy for all sides	\geq	0.02	Other process	off	1
RVy.EN.9.DFM	Recommended RVy fully enclosure by $M_{xy} + 1/1.25 \times M_{xy}$ is defined by either RVy.EN.9a.DFM or Vy.EN.9b.DFM, which $M_{xy} + 1/1.25 \times M_{xy}$ is the metal layer directly above rectangular RVy.			Other process	off	1
RVy.EN.9a.DFM	Recommended RVy enclosure by $M_{xy} + 1/1.25 \times M_{xy}$ for all sides	\geq	0.02	Other process	off	1
RVy.EN.9b.DFM	Recommended RVy enclosure by $M_{xy} + 1/1.25 \times M_{xy}$ for two opposite sides with the other twosides $\geq 0.007\text{um}$	\geq	0.025	Other process	off	1

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7.14.2.8 Mxy DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
Mxy.W.1.DFM	Recommended Mxy width to reduce the line open possibility, except MOMDMY and EFUSE regions	\geq	0.046	Litho	off	1
Mxy.S.1.DFM	Recommend Mxy space to reduce the short possibility, except MOMDMY region	\geq	0.044	Litho	off	1
Mxy.S.2.DFM	Recommended Mxy space when either one Mxy width $> 0.07\mu m$	\geq	0.072	Litho	off	1
Mxy.S.3.DFM	Recommended Mxy space when either one Mxy width $> 0.088\mu m$	\geq	0.081	Litho	off	1
Mxy.S.4.DFM	Recommended Mxy space when either one Mxy width $> 0.112\mu m$, except EFUSE region	\geq	0.106	Litho	off	1
Mxy.S.5.DFM	Recommended Mxy space when either one Mxy width $> 0.18\mu m$, except EFUSE region	\geq	0.126	Litho	off	1
Mxy.S.6.DFM	Recommended Mxy space when either one Mxy width $> 0.27\mu m$	\geq	0.144	Litho	off	1
Mxy.S.9a.DFM	Space between Mxy line and line-end ($W < 0.046\mu m$, $PRL > -0.022\mu m$)	\geq	0.070	Litho	off	1
Mxy.S.9b.DFM	Space between Mxy line and line-end ($0.046 < W \leq 0.051\mu m$, $PRL > -0.022\mu m$)	\geq	0.063	Litho	off	1
Mxy.S.10.DFM	Space between Mxy line-end ($W \leq 0.051\mu m$) and line-end ($W < 0.048\mu m$, $PRL > -0.022\mu m$)	\geq	0.081	Litho	off	1
Mxy.A.1.DFM	Recommended Mxy area	\geq	0.01	Litho	off	1
Mxy.R.2.DFM	Recommended M2 forbidden zone of (($W_1+S_1+W_2+S_2$) or ($S_1+W_2+S_2+W_3$)) when Mxy width $< 0.037\mu m$. DRC flags the edge of forbidden zone and	\geq	0.14~0.175	Litho	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Pri priority
	waive the violation in same polygon.					
Mxy.R.6.DFM	<p>It's not recommended to use U-shape Mxy. DRC check condition:</p> <ol style="list-style-type: none">1. With at least one RVy or RVy-1;2. Mxy width $W \leq 0.038\text{um}$;3. $S \leq 0.12\text{um}$; <p>Which rule is not applied for INST region .</p>			Other area	off	1
Mxy.R.7.DFM	<p>It's not recommended to use Hook-shape Mxy. Hook-shape Mxy definition:</p> <ol style="list-style-type: none">(1) Hook-end line width(W_1) is $\leq 0.05\text{um}$, length(L_1) $\leq 0.15\text{um}$, $\Delta L > 0.1\text{um}$ and Hook-end interact one via,(2) W_2/W_3 width $\leq 0.072\text{um}$.(3) Space between two Mxy arms(S_1) $\leq 0.1\text{um}$.(4) Space between via and another Mxy $S_2 \leq 0.038\text{um}$ when $PRL > -0.015\text{um}$ DRC waive if hook-end enclosure via $\geq 0.05\text{um}$ <p>This rule is not applied for INST region</p>			Other area	off	1
Mxy.R.8.DFM	<p>It's not recommended to use dense Mxy line end pattern. DRC flag conditions:</p> <ol style="list-style-type: none">(1) Middle Mxy line width(W_1) $\leq 0.038\text{um}$, both two neighbour Mxy lines width $\leq 0.064\text{um}$;(2) Both the Vy-1 dense region (dense region definition: region formed by Vy-1 horizontal edge extension 0.038um, vertical edge extension 0.05um) horizontal edges neighbour Mxy line-end. <p>DRC waive if Mxy enclosure Vy-1 $> 0.05\text{um}$. (Vy-1 is the via underneath Mxy)</p> <p>This rule is not applied for INST region</p>			Other area	off	1

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Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Prip ority
Mxy.R.9.DFM	<p>It's not recommended to use dense Mxy 3-bar pattern. DRC flag conditions:</p> <p>(1) Middle Mxy line width(W1) is \leq 0.048um, both two neighbour Mxy line width \leq 0.064um and interact square or rectangle Vy or Vy-1.</p> <p>(2) Mxy Space to both via (S1/S2) = 0.058~0.063um.</p> <p>(3) The via PRL: -0.1 < PRL < 0.1um.</p> <p>(4) Both neighbour Mxy enclosure Vy or Vy-1 < 0.05um</p> <p>This rule is not applied for INST region</p>			Other area	off	1

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7.14.2.9 1.25xMy DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Pripority
1.25xMy.S.3.DFM	Recommended 1.25xMy space when either one 1.25xMy width > 1.35um	≥	0.45	Litho	off	1
1.25xMy.A.1.DFM	Recommended 1.25xMy area	≥	0.02	Litho	off	1
1.25xMy.R.1.DFM	Maximum number of stacked metal layers (including M1) of high density area (density > 70% in window size 800um*800um, stepping size 100um)	≤	4	CMP	off	1
1.25xMy.R.12.DFM	<p>It's not recommended to use dense 1.25xMy 3-bar pattern. DRC flag conditions:</p> <ul style="list-style-type: none">(1) Middle 1.25xMy line width (W1) is ≤ 0.044um, both two neighbour 1.25xMy line width ≤ 0.06um and interact square or rectangle Vy-1 or Vy.(2) 1.25xMxy Space to both via (S1/S2) < 0.048um.(3) The via PRL: -0.1 < PRL < 0.1um.(4) Both neighbour 1.25xMxy enclosure Vy < 0.05um, or Both neighbour 1.25xMxy enclosure 1.25xVn < 0.065um <p>This rule is not applied for INST region.</p>			Litho	off	1

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7.14.2.10 1.25xMn DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Pripority
1.25xMn.S.3.DFM	Recommended 1.25xMn space when either one 1.25xMn width > 1.35um	≥	0.45	Litho	off	1
1.25xMn.A.1.DFM	Recommended 1.25xMn area	≥	0.02	Litho	off	1
1.25xMn.R.1.DFM	Maximum number of stacked metal layers (including M1) of high density area (density > 70% in window size 800um*800um, stepping size 100um)	≤	4	CMP	off	1
1.25xMn.R.9.DFM	<p>It's not recommended to use dense 1.25xMn 3-bar pattern. DRC flag conditions:</p> <ul style="list-style-type: none"> (1) Middle line width(W1) is ≤ 0.044um, both two neighbour 1.25xMn line width ≤ 0.06um and interact square or rectangle Vy or 1.25xVn. (2) 1.25xMn Space to both via (S1/S2) < 0.048um. (3) The via PRL: -0.1 < PRL < 0.1um. (4) Both neighbor 1.25xMn enclosure 1.25xVn or 1.25xVn-1 < 0.065um <p>This rule is not applied for INST region.</p>			Litho	off	1

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7.14.2.11 2xVn (BV1/BV2) DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Pripority
2xVn.EN.1. DFM	Recommended 2xVn fully enclosure by 1.25xMy/1.25xMn/2xMn is defined by either VIAy.EN.2.DFM, which 1.25xMy/1.25xMn/2xMn the metal layer directly underneath 2xVn.			Other process	off	1
2xVn.EN.2. DFM	Recommended 2xVn enclosure by 1.25xMn/2xMn for two opposite sides with the other two sides \geq 0.027um	\geq	0.045	Other process	off	1
2xVn.EN.7. DFM	Recommended 2xVn fully enclosure by 2xMn+1 is defined by 2xVn.EN.8.DFM, which 2xMn+1 is the metal layer directly above 2xVn.			Other process	off	1
2xVn.EN.8. DFM	Recommended 2xVn enclosure by 2xMn+1 for two opposite sides with the other two sides \geq 0.027um	\geq	0.035	Other process	off	1

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7.14.2.12 2xMn (B1/B2) DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
2xMn.S.1. DFM	Recommended 2xMn space to reduce the short possibility	\geq	0.08	Defect	off	1
2xMn.A.1. DFM	Recommended 2xMn area	\geq	0.26	Litho	off	1

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7.14.2.13 10xTV DFM rule

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
10xTV.R.10. DFM	Recommended maximum continuous stacked VIA layers (including V0), which has only one square via for each via layer to avoid high Rc.	\leq	4	Other process	off	1

7.14.2.14 14xTV DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
14xTV.R.10. DFM	Recommended maximum continuous stacked VIA layers (including V0), which has only one square via for each via layer to avoid high Rc.	\leq	4	Other process	off	1

7.14.2.15 UTV DFM rules

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Priority
UTV.R.10.D FM	Recommended maximum continuous stacked VIA layers (including V0), which has only one square via for each via layer to avoid high Rc.	\leq	4	Other process	off	1

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7.14.2.16 ALRDL DFM rules

SMIC can support two options for RDL layer, one is standard 14.5K RDL thickness and the other is for 28K RDL thickness. Both options could share the same design rules.

RDL layer can be used to draw AL inter-connect lines, Al fuse metal line, AL bumping pads and re-distribution AL pads.

Rule number	Description	Opt.	Design Value	Concerned Area	DRC switch default	Pripority
ALPA.W.2. DFM	Recommended ALRDL width connected with AL bump pad	\geq	18	Other process	off	1

Notes:

1. If RDL is used for AL bumping or re-distributed AL pads, suggest consulting with package vendors for the dimension.



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7.14.3 Unique Pattern Design Rules for Logic Standard cells

1. Logic Standard cells PowerRail Definition:

- 1) M1 width = 0.09um in GATE poly direction.
- 2) M1 (width=0.09um) centerline space = 0.576um for 9T design/0.48um for 7.5T design.
- 3) M1 interact with RSPMK1.

2. DDB design Definition:

[The region between two (Logic Standard cells PowerRail)] NOT INTERCACT AR.

3. SDB design Definition:

[The region between two (Logic Standard cells PowerRail)] INTERCACT AR.

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7.14.3.1 AA Unique Pattern Design Rules

Rule number	Description	Opt.	Design Value	Unit
AA.W.1.9TBS	AA width in GATE poly direction in 9T DDB/SDB design.	=	0.096/0.14 4/ 0.192	um
AA.W.1.7TBS	AA width in GATE poly direction in 7.5T DDB/SDB design.	=	0.096/0.14 4	um
AA.S.1a.TBS	Space between ALL_AA and PowerRail centerline. Excluding pick-up AA ,or AA not interact (V0, M0G, M1).	=	0.048	um
AA.S.1b.9TBS	Space between pick-up AA and PowerRail centerline in 9T DDB design.	=	0.24/0.144	um
AA.S.1b.7TBS	Space between pick-up AA and PowerRail centerline in 7.5T DDB design.	=	0.192	um
AA.S.1b.ARTBS	Space between pick-up AA and PowerRail centerline in SDB design.	=	0.144/0.19 2	um
AA.S.2.TBS	Space between ALL_AA in S/D direction in GT_P96	≥	0.096	um
AA.R.1.TBS	AA must be a rectangle orthogonal to grid or single L-, U-, or combined L/U- shape.			

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7.14.3.2 M0 Unique Pattern Design Rules

Rule number	Description	Opt.	Design Value	Unit
M0.S.2a.TBS	Space between the long side of M0 and GT (width = 0.017/0.016/0.015um), except GT_P96 region.	=	0.017/0.016/0.015	um
M0.S.2b.TBS	Space between the long side of M0 and GT (width = 0.017/0.018/0.02/0.024um), inside GT_P96 region.	=	0.02/0.019/0.018/0.016	um
M0.EX.2.9TBS	M0 line-end (line-end not interact PowerRail) extension outside of PowerRail centerline in 9T DDB design	=	0.137/0.161/0.165/0.185/0.233	um
M0.EX.2.7TBS	M0 line-end (line-end not interact PowerRail) extension outside of PowerRail centerline in 7.5T DDB design	=	0.137/0.161/0.167/0.185/0.188/0.191	um
M0.EX.2.ARTBS	M0 line-end (line-end not interact PowerRail) extension outside of PowerRail centerline in SDB design	=	0.137/0.161/0.169/0.185/0.188/0.201/0.233	um
M0.EX.2a.TBS	Extension of M0 short side (short side not interact M0C) outside of AA (horizontal edge extend -0.019um) in GATE poly direction.	≥	0.012	um
M0.EX.2b.TBS	M0 short side (short side interact M0C) extension outside of AA (horizontal edge extend -0.019um) in GATE poly direction.	≥	0.009	um

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7.14.3.3 M0C Unique Pattern Design Rules

Rule number	Description	Opt.	Design Value	Unit
M0C.W.1.TBS	M0C width in GATE poly direction	=	0.051	um
M0C.S.1.TBS	Space between M0C and PowerRail centerline	=	0.007	um
M0C.EX.1a.TBS	M0C extension outside of AOP_M0 in S/D direction, except GT_P96 region	=	0.025	um
M0C.EX.1b.TBS	M0C extension outside of AOP_M0 in S/D direction in GT_P96 region.	=	0.028	um
M0C.O.1.TBS	M0C overlap M0 in poly direction.	=	0.026/0.051	um
M0C.R.1.TBS	M0C must interact with RSPMK1.			
M0C.R.2.TBS	M0C must be a rectangle, other shapes like L, T, U-shape are not allowed.			

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7.14.3.4 M0G Unique Pattern Design Rules

Rule number	Description	Opt.	Design Value	Unit
M0G.S.1.9TBS	Space between M0G (width = 0.04um) line and PowerRail centerline in 9T DDB design	=	0.066/0.076/ 0.172/0.220/ 0.268	um
M0G.S.1.7TBS	Space between M0G (width = 0.04um) line and PowerRail centerline in 7.5T DDB design	=	0.066/0.172/ 0.196/0.204/ 0.218/0.22	um
M0G.S.1.ARTBS	Space between M0G (width = 0.04um) line and PowerRail centerline in SDB design.	=	0.066/0.068/ 0.076/0.172/ 0.206/0.22/0. 268	um
M0G.S.2.9TBS	Space between M0G (width = 0.04um) line-end and GT centerline in 9T DDB design	=	0.042	um
M0G.S.2.7TBS	Space between M0G (width = 0.04um) line-end and GT centerline in 7.5T DDB design	=	0.042/0.045	um
M0G.S.2.ARTBS	Space between M0G (width = 0.04um) line-end and GT centerline in SDB design.	=	0.039/0.042	um
M0G.S.3.9TBS	Space between M0G (width = 0.05um) and PowerRail centerline in 9T DDB design	=	0.167/0.176/ 0.183/0.195/ 0.215/0.231/ 0.263	um
M0G.S.3.7TBS	Space between M0G (width = 0.05um) and PowerRail centerline in 7.5T DDB design	=	0.170/0.191/ 0.199/0.215	um
M0G.S.3.ARTBS	Space between M0G (width = 0.05um) and PowerRail centerline in SDB design.	=	0.167/0.17/0. 183/0.191/0. 199/0.215/0. 231/0.239/0. 247/0.263	um
M0G.S.4.TBS	Space between M0G (width = 0.05um) centerline and GT centerline	=	0/0.009/0.01 9	um
M0G.S.4.ARTBS	Space between M0G (width = 0.05um) centerline and GT centerline in SDB design.	=	0/0.009/0.01/ 0.013/0.016/ 0.019	um

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Rule number	Description	Opt.	Design Value	Unit
M0G.S.5.9TBS	Space between M0G (width = 0.054/0.09um) and PowerRail centerline in 9T DDB design	=	0.051	um
M0G.S.5.7TBS	Space between M0G (width = 0.054/0.09um) and PowerRail centerline in 7.5T DDB design	=	0.042	um
M0G.S.5.ARTBS	Space between M0G (width = 0.051/0.054/0.088um) and PowerRail centerline in SDB design.	=	0.042/0.053	um
M0G.EX.1.9TBS	M0G (width = 0.04um) line-end extension GT centerline in 9T DDB design	=	0.008	um
M0G.EX.1.7TBS	M0G (width = 0.04um) line-end extension GT centerline in 7.5T DDB design	=	0.006/0.032	um
M0G.EX.1.ARTBS	M0G (width = 0.04um) line-end extension GT centerline in SDB design.	=	0.006/0.032/ 0.034	um
M0G.O.1.TBS	M0G (width = 0.088um) and (GT (width = 0.016/0.018/0.02/0.024um) NOT P2) overlap in S/D direction	=	0.008/0.009/ 0.010/0.012	um
M0G.S.7.TBS	Space between the short side of AOP_M0G (width = 0.04um) when PRL > -0.02um	≥	0.078	um
M0G.S.9a.TBS	Space between the center of M0G (width = 0.05um) when PRL = 0.05um inside DDB standard-cell	≥	0.105	um
M0G.S.9b.TBS	Space between the center of M0G (width = 0.05um) when PRL=0.05um inside SDB standard-cell	≥	0.099	um
M0G.S.10.TBS	Space between the center of M0G (width = 0.05um) when PRL< 0.05um	≥	0.106	um
M0G.S.11a.TBS	Space between M0G and AOP_AA (Overlap is not allowed, except ((M0G AND AOP_AA) INTERACT M0)) (Except M0G.S.11b.TBS)	≥	0.039	um
M0G.S.11b.TBS	Space between M0G and AOP_AA in GATE poly direction (Overlap is not allowed, except ((M0G AND AOP_AA) INTERACT M0))	≥	0.019	um
M0G.S.12a.TBS	Space between M0G (width = 0.04um, not interact M0) to AOP_GT in GT_P96 region.	≥	0.031	um
M0G.S.13.TBS	Space between M0G (width = 0.04um) and (M0 NOT	≥	0.028	um

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Rule number	Description	Opt.	Design Value	Unit
	M0C) in S/D direction (PRL > -0.016 um)			
M0G.S.14a.TBS	Space between M0G (width = 0.04um) and the short side of M0 (short side NOT INTERACT M0C) when PRL \geq -0.018 um in 7.5T design.	\geq	0.032	um
M0G.S.14b.TBS	Space between M0G (width = 0.04um) and the short side of M0 (short side NOT INTERACT M0C) when PRL \geq -0.018 um in 9T design.	\geq	0.035	um
M0G.S.15.TBS	Space between M0G (width = 0.05um) and the short side of M0 (short side NOT INTERACT M0C) when PRL \geq -0.018 um.	\geq	0.03	um

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According to: SMIC Document Control Procedure; Attachment No.: QR-QUSM-02-2001-023; Rev.:2

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7.14.3.5 V0 Unique Pattern Design Rules

Rule number	Description	Opt.	Design Value	Unit
V0.S.1.9TBS	Space between V0 (interact with M0) center-line and PowerRail center-line in 9T DDB design.	=	0.024/0.095 /0.127/0.13 3/0.149/0.1 60/0.169/0. 176/0.199/0 .201	um
V0.S.1.7TBS	Space between V0 (interact with M0) center-line and PowerRail center-line in 7.5T DDB design.	=	0.024/0.093 /0.095/0.11 1/0.127/0.1 30/0.135/0. 143/0.157/0 .160	um
V0.S.1.ARTBS	Space between V0 (interact with M0) center-line and PowerRail center-line in SDB design.	=	0.024/0.093 /0.095/0.09 6/0.102/0.1 09/0.111/0. 125/0.127/0 .128/0.133/ 0.137/0.143 /0.15/0.151 /0.157/0.16 0/0.162/0.1 66/0.169/0. 176/0.182/0 .185/0.197/ 0.199/0.201	um
V0.S.2.9TBS	Space between V0 (interact with M0G) center-line and PowerRail center-line in 9T DDB design.	=	0.192/0.201 /0.208/0.22 0/0.240/0.2 56/0.288	um
V0.S.2.7TBS	Space between V0 (interact with M0G) center-line and PowerRail center-line in 7.5T DDB design.	=	0.192/0.195 /0.216/0.22 4/0.238/0.2 40	um
V0.S.2.ARTBS	Space between V0 (interact with M0G) center-line and PowerRail center-line in SDB design.	=	0.192/0.195 /208/0.216/ 0.224/0.226	um

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Rule number	Description	Opt.	Design Value	Unit
			/0.240/256/ 0.264/0.272 /0.288	
V0.EN.1.9TBS	V0 Enclosure by M0G (width = 0.04um) with other two sides \geq 0.004um in 9T DDB design. Exclude V0 totally enclosed by M0. Drc waive if enclosure \geq 0.036um.	=	0.012/0.018 /0.029	um
V0.EN.1.7TBS	V0 Enclosure by M0G (width = 0.04um) with other two sides \geq 0.004um in 7.5T DDB design. Exclude V0 totally enclosed by M0. DRC waive if enclosure \geq 0.036um.	=	0.016	um
V0.EN.1.ARTBS	V0 Enclosure by M0G (width = 0.04um) with other two sides \geq 0.004um in SDB design. Exclude V0 totally enclosed by M0. DRC waive if enclosure \geq 0.036um.	=	0.016/0.035	um
V0.EN.2a.TBS	V0 Enclosure by M0G (width = 0.05um) in Gate poly direction \geq 0.009um with other side \geq 0.002um.	\geq	0.016	um
V0.EN.2b.TBS	V0 Enclosure by M0G (width = 0.05um) in four direction	\geq	0.009	um
V0.EN.2c.ARTBS	V0 Enclosure by M0G (width = 0.05um) in Gate poly direction \geq 0.009um with other side \geq 0um in SDB design.	\geq	0.018	um
V0.EN.3.TBS	V0 Enclosure by M1 (width = 0.032um) line-end with the other two sides \geq 0um in DDB design. DRC waive if enclosure \geq 0.048um.	=	0.038/0.040	um
V0.EN.3.ARTBS	V0 Enclosure by M1 (width = 0.032um) line-end with the other two sides \geq 0um in SDB design. DRC waive if enclosure \geq 0.048um.	=	0.036/0.038 /0.040	um
V0.EN.4.9TBS	V0 Enclosure by M1 (width=0.034um) line-end with the other two sides \geq 0.001um in 9T DDB design. DRC waive if enclosure \geq 0.048um.	=	0.038/0.040 /0.041	um
V0.EN.4.7TBS	V0 Enclosure by M1 (width = 0.034um) line-end with the other two sides \geq 0.001um in 7.5T DDB design. DRC waive if enclosure \geq 0.048um.	=	0.038/0.040	um
V0.EN.4.ARTBS	V0 Enclosure by M1 (width=0.034um) line-end with the other two sides \geq 0.001um in SDB design. DRC waive if enclosure \geq 0.048um.	=	0.038/0.040	um

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Rule number	Description	Opt.	Design Value	Unit
V0.EN.5.7TBS	V0 Enclosure by M1 (width = 0.035um) line-end with the other two sides = 0/0.003um in 7.5T DDB design. DRC waive if enclosure \geq 0.048um.	=	0.038/0.040	um
V0.EN.5.ARTBS	V0 Enclosure by M1 (width = 0.035um) line-end with the other two sides = 0/0.003um in SDB design.. DRC waive if enclosure \geq 0.048um.	=	0.038	um
V0.EN.6.TBS	V0 Enclosure by M1 (width = 0.046um) line-end with the other two sides = 0/0.003/0.007/0.011/0.014um in DDB design. DRC waive if enclosure \geq 0.048um.	=	0.032	um
V0.EN.6.ARTBS	V0 Enclosure by M1 (width = 0.046um) line-end with the other two sides = 0/0.004/0.007/0.01/0.014um in SDB design. DRC waive if enclosure \geq 0.048um.	=	0.032	um
V0.EN.7.9TBS	V0 Enclosure by M1 (width = 0.050um) line-end with the other two sides \geq 0.009um in 9T DDB design. DRC waive if enclosure \geq 0.036um.	=	0.025/0.027 /0.029/0.035	um
V0.EN.7.7TBS	V0 Enclosure by M1 (width = 0.050um) line-end with the other two sides = 0.006/0.009/0.012um in 7.5T DDB design. DRC waive if enclosure \geq 0.036um.	=	0.025/0.028	um
V0.EN.7.ARTBS	V0 Enclosure by M1 (width = 0.050um) line-end with the other two sides \geq 0.006um in SDB design. DRC waive if enclosure \geq 0.036um.	=	0.025/0.028	um
V0.EN.13.ARTBS	Enclosure by M1 [width=0.058um] line-end with the other two sides \geq 0.006um in SDB design. Drc waive if enclosure \geq 0.036um.	=	0.025	um
V0.EN.8.9TBS	V0 Enclosure by M1 (width = 0.064um) in three direction in 9T DDB design	=	0.016	um
V0.EN.8.7TBS	Enclosure by M1 (width = 0.064um) line-end with the other two sides \geq 0.016um in 7.5T DDB design. DRC waive if enclosure \geq 0.036um.	=	0.016/0.017 /0.025	um
V0.EN.8.ARTBS	Enclosure by M1 (width = 0.064um) line-end with the other two sides \geq 0.016um in SDB design. DRC waive if enclosure \geq 0.025um.	=	0.016/0.017	um
V0.EN.9.7TBS	Enclosure by M1 (width = 0.066um) line-end with the other	=	0.016	um

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Rule number	Description	Opt.	Design Value	Unit
	two sides \geq 0.017um in 7.5T DDB design. DRC waive if enclosure \geq 0.036um.			
V0.EN.9.ARTBS	Enclosure by M1 (width = 0.066um) line-end with the other two sides \geq 0.017um in SDB design. DRC waive if enclosure \geq 0.025um.	=	0.016	um
V0.EN.10.7TBS	Enclosure by M1 (width=0.076um) line-end with the other two sides \geq 0.009um in 7.5T DDB design. DRC waive if enclosure \geq 0.036um.	=	0.025	um
V0.EN.10.ARTBS	Enclosure by M1 (width = 0.076um) line-end with the other two sides \geq 0.009um in SDB design. DRC waive if enclosure \geq 0.036um.	=	0.025	um
V0.EN.11.9TBS	Enclosure by M1 (width = 0.082um) line-end with the other two sides = 0.016/0.025/0.034um in 9T DDB design. Enclosure = (0.009,0.016) by two neighbor sides is not allowed DRC waive if enclosure \geq 0.036um.	=	0.009/0.016 /0.025/0.032	um
V0.EN.11.7TBS	Enclosure by M1 (width=0.082um) line-end with the other two sides = 0.016/0.025/0.034um in 7.5T DDB design. DRC waive if enclosure \geq 0.036um.	=	0.016/0.018 /0.024/0.025/0.029/0.032/0.035	um
V0.EN.11.ARTBS	Enclosure by M1 (width = 0.082um) line-end with the other two sides = 0.009/0.016/0.024/0.025 um in SDB design. DRC waive if enclosure \geq 0.036um. Enclosure = (0.009,0.012)/(0.009,0.016)/(0.012,0.016) by two neighbor sides is not allowed	=	0.012/0.016 /0.025	um
V0.S.3.TBS	Space to M0G (different net and PRL > 0). DRC only check space along M1 enclosure V0 >0	\geq	0.04	um
V0.S.4.TBS	Space between V0 and (M0 NOT M0C) (different net) in S/D direction when PRL > 0um DRC only check space along M1 enclosure V0 >0 in S/D direction.	\geq	0.028	um
V0.EN.12.TBS	Enclosure by M1 corner (0.032um \leq M1 width \leq 0.046um) for opposite side (line-end) \geq 0.036um with the other two sides \geq 0um	\geq	0.041	um

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7.14.3.6 M1 Unique Pattern Design Rules

Rule number	Description	Opt.	Design Value	Unit
M1.W.1.9TBS	M1 width in 9T DDB design.	=	0.032/0.034/0. 038/0.046/0.05 /0.064/0.082/0. 09/0.096	um
M1.W.1.7TBS	M1 width in 7.5T DDB design.	=	0.032/0.034/0. 035/0.046/0.05 /0.064/0.066/0. 076/0.082/0.09 /0.096	um
M1.W.1.ARTBS	M1 width in SDB design.	=	0.032/0.034/0. 035/0.038/0.04 6/0.050/0.058/ 0.063/0.064/0. 066/0.076/0.07 7/0.082/0.090	um
M1.S.1a.9TBS	Space between M1 (width = 0.032um) line and PowerRail centerline in 9T DDB design	=	0.144	um
M1.S.1a.7TBS	Space between M1 (width = 0.032um) line and PowerRail centerline in 7.5T DDB design	=	0.077/0.141/0. 144	um
M1.S.1a.ARTBS	Space between M1 (width = 0.032um) line and PowerRail centerline in SDB design.	=	0.077/0.08/0.1 09/0.141/0.144 /0.161/0.173/0. 190	um
M1.S.1b.9TBS	Space between M1 (width = 0.032um) line-end and GT centerline in 9T DDB design	=	0.042	um
M1.S.1b.7TBS	Space between M1 (width = 0.032um) line-end and GT centerline in 7.5T DDB design DRC flag all M1 (width = 0.032um) line-end space to GT centerline.	=	\	um
M1.S.2a.9TBS	Space between M1 (width = 0.034um) line and PowerRail centerline in 9T DDB design	=	0.078/0.11/0.1 75/0.19	um
M1.S.2a.7TBS	Space between M1 (width = 0.034um) line and PowerRail centerline in 7.5T DDB design	=	0.078/0.11	um

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Rule number	Description	Opt.	Design Value	Unit
M1.S.2a.ARTBS	Space between M1 (width = 0.034um) line and PowerRail centerline in SDB design.	=	0.078/0.127	um
M1.S.2b.9TBS	Space between M1 (width = 0.034um) centerline and GT centerline in 9T DDB design.	=	0.008/0.022/0. 026/0.048	um
M1.S.2b.7TBS	Space between M1 (width = 0.034um) centerline and GT centerline in 7.5T DDB design.	=	0.008/0.026/0. 037	um
M1.S.2c.9TBS	Space between M1 (width = 0.034um) line-end and GT centerline in 9T DDB desig.	=	0.04	um
M1.S.2c.7TBS	Space between M1 (width = 0.034um) line-end and GT centerline in 7.5T DDB desig. DRC flag all M1 (width = 0.034um) line-end space to GT centerline.	=	\	um
M1.S.2d.TBS	Space between M1 (width = 0.034um) line-end and PowerRail centerline. DRC flag horizontal M1(width = 0.034um) line-end	=	\	um
M1.S.3a.7TBS	Space between M1 (width = 0.035um) line and PowerRail centerline in 7.5T DDB design	=	0.141	um
M1.S.3a.ARTBS	Space between M1 (width = 0.035um) line and PowerRail centerline in SDB design.	=	0.141	um
M1.S.3b.7TBS	Space between M1 (width = 0.035um) line-end and GT centerline in 7.5T DDB design DRC flag all M1 (width = 0.035um) line-end space to GT centerline.	=	\	um
M1.S.3b.ARTBS	Space between M1 (width = 0.035um) line-end and GT centerline in SDB design.	=	0.046	um
M1.S.4a.9TBS	Space between M1 (width = 0.038um) centerline and GT centerline in 9T DDB design	=	0.026	
M1.S.4a.ARTBS	Space between M1 (width = 0.038um) centerline and GT centerline in SDB design.	=	0.001/0.01/0.0 12/0.02/0.022/ 0.026/0.029/0. 031/0.033/0.03 5/0.042/0.045	
M1.S.4b.9TBS	Space between M1 (width = 0.038um) line-end and	=	\	um

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Rule number	Description	Opt.	Design Value	Unit
	PowerRail centerline in 9T DDB design. DRC flag horizontal M1(width = 0.038um) line-end			
M1.S.4b.ARTBS	Space between M1 (width = 0.038um) line-end and PowerRail centerline in SDB design.	=	0.129/0.236	um
M1.S.4c.ARTBS	Space between M1 (width = 0.038um) line and PowerRail centerline in SDB design.	=	0.173/0.184	um
M1.S.4d.ARTBS	Space between M1 (width = 0.038um) line-end and GT centerline in SDB design.	=	0.012	um
M1.S.5a.9TBS	Space between M1 (width = 0.046um) centerline and GT centerline in 9T DDB design.	=	0.002/0.006/0. 011/0.016/0.03 0/0.048	um
M1.S.5a.7TBS	Space between M1 (width = 0.046um) centerline and GT centerline in 7.5T DDB design.	=	0.002/0.007/0. 011/0.016/0.03 0/0.048	um
M1.S.5a.ARTBS	Space between M1 (width = 0.046um) centerline and GT centerline in SDB design.	=	0.001/0.005/0. 01/0.012/0.017 /0.023/0.026/0. 029/0.033/0.03 5/0.038/0.041/ 0.045	um
M1.S.5b.9TBS	Space between M1 (width = 0.046um) line-end and PowerRail centerline in 9T DDB design.	=	0.087/0.119/0. 151/0.183/0.21 5/0.240/0.279	um
M1.S.5b.7TBS	Space between M1 (width = 0.046um) line-end and PowerRail centerline in 7.5T DDB design.	=	0.082/0.087/0. 109/0.119/0.15 1/0.183/0.215	um
M1.S.5b.ARTBS	Space between M1 (width = 0.046um) line-end and PowerRail centerline in SDB design.	=	0.081/0.085/0. 11/0.119/0.151 /0.183/0.204/0. 215/0.236/0.24 7/0.268	um
M1.S.6a.9TBS	Space between M1 (width = 0.05um) line and PowerRail centerline in 9T DDB design	=	0.078/0.108/0. 144/0.176/0.19 5/0.208/0.240/ 0.263	um

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Rule number	Description	Opt.	Design Value	Unit
M1.S.6a.7TBS	Space between M1 (width = 0.05um) line and PowerRail centerline in 7.5T DDB design	=	0.080/0.108/0. 109/0.144/0.17 3/0.176/0.208/ 0.215	um
M1.S.6a.ARTBS	Space between M1 (width = 0.05um) line and PowerRail centerline in SDB design.	=	0.077/0.108/0. 112/0.126/0.14 1/0.144/0.172/ 0.173/0.176/0. 19/0.208/0.215 /0.263	um
M1.S.6b.TBS	Space between M1 (width = 0.05um) centerline and GT centerline in DDB design.	=	0/0.009/0.019/ 0.026/0.037/0. 048	um
M1.S.6b.ARTBS	Space between M1 (width = 0.05um) centerline and GT centerline in SDB design.	=	0/0.009/0.01/0. 012/0.016/0.01 9/0.026/0.045/ 0.048	um
M1.S.6c.9TBS	Space between M1 (width = 0.05um) line-end and PowerRail centerline in 9T DDB design	=	0.087/0.151/0. 183/0.215/0.24 7/0.279	um
M1.S.6c.7TBS	Space between M1 (width = 0.05um) line-end and PowerRail centerline in 7.5T DDB design	=	0.087/0.119/0. 151/0.175/0.18 3/0.215	um
M1.S.6c.ARTBS	Space between M1 (width = 0.05um) line-end and PowerRail centerline in SDB design.	=	0.087/0.109/0. 119/0.151/0.17 5/0.183/0.199/ 0.215/0.247/0. 279	um
M1.S.6d.9TBS	Space between M1 (width = 0.050um) line-end and GT centerline in 9T DDB design	=	0.007/0.020/0. 029/0.030/0.03 9/0.048	um
M1.S.6d.7TBS	Space between M1 (width = 0.050um) line-end and GT centerline in 7.5T DDB design	=	0.007/0.029/0. 030/0.039/0.04 8	um
M1.S.6d.ARTBS	Space between M1 (width = 0.050um) line-end and GT centerline in SDB design.	=	0.002/0.004/0. 007/0.013/0.01	um

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Rule number	Description	Opt.	Design Value	Unit
			5/0.023/0.029/ 0.033/0.034	
M1.S.15a.ARTB S	Space between M1 (width = 0.058um) line-end and PowerRail centerline in SDB design.	=	0.151/0.183/0. 199	um
M1.S.15b.ARTB S	Space between M1 (width = 0.058um) centerline and GT centerline in SDB design.	=	0.035	um
M1.S.16a.ARTB S	Space between M1 (width = 0.063um) line and PowerRail centerline in SDB design.	=	0.077	um
M1.S.16b.ARTB S	Space between M1 (width = 0.063um) line-end and GT centerline in SDB design.	=	0.004	um
M1.S.7a.9TBS	Space between M1 (width = 0.064um) line and PowerRail centerline in 9T DDB design.	=	0.144/0.256	um
M1.S.7a.7TBS	Space between M1 (width = 0.064um) line and PowerRail centerline in 7.5T DDB design.	=	0.208	um
M1.S.7a.ARTBS	Space between M1 (width = 0.064um) line and PowerRail centerline in SDB design.	=	0.077/0.144/0. 208/0.256	um
M1.S.7b.9TBS	Space between M1 (width = 0.064um) centerline and GT centerline in 9T DDB design	=	0.048	um
M1.S.7b.7TBS	Space between M1 (width = 0.064um) centerline and GT centerline in 7.5T DDB design	=	0.009/0.012/0. 019/0.048	um
M1.S.7b.ARTBS	Space between M1 (width = 0.064um) centerline and GT centerline in SDB design.	=	0.007/0.01/0.0 12/0.019/0.026 /0.045/	um
M1.S.7c.9TBS	Space between M1 (width = 0.064um) line-end and PowerRail centerline in 9T DDB design. DRC flag all M1 (width = 0.064um) line-end space to PowerRail centerline.	=	\	um
M1.S.7c.7TBS	Space between M1 (width = 0.064um) line-end and PowerRail centerline in 7.5T DDB design.	=	0.087/0.175/0. 208	um
M1.S.7c.ARTBS	Space between M1 (width = 0.064um) line-end and PowerRail centerline in SDB design.	=	0.119/0.191/0. 223/0.239/0.25 5	um

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Rule number	Description	Opt.	Design Value	Unit
M1.S.7d.9TBS	Space between M1 (width = 0.064um) line-end and GT centerline in 9T DDB design	=	0.016	um
M1.S.7d.7TBS	Space between M1 (width = 0.064um) line-end and GT centerline in 7.5T DDB design	=	0.009/0.020/0. 023	um
M1.S.7d.ARTBS	Space between M1 (width = 0.064um) line-end and GT centerline in SDB design.	=	0.013/0.022/0. 032	um
M1.S.8a.7TBS	Space between M1 (width = 0.066um) line and PowerRail centerline in 7.5T DDB design	=	0.078/0.110	um
M1.S.8a.ARTBS	Space between M1 (width = 0.066um) line and PowerRail centerline in SDB design.	=	0.078/0.110	um
M1.S.8b.7TBS	Space between M1 (width = 0.066um) line-end and GT centerline in 7.5T DDB design	=	0.016	um
M1.S.8b.ARTBS	Space between M1 (width = 0.066um) line-end and GT centerline in SDB design.	=	0.016	um
M1.S.9a.7TBS	Space between M1 (width = 0.076um) line and PowerRail centerline in 7.5T DDB design	=	0.144	um
M1.S.9a.ARTBS	Space between M1 (width = 0.076um) line and PowerRail centerline in SDB design.	=	0.144	um
M1.S.9b.7TBS	Space between M1 (width = 0.076um) line-end and GT centerline in 7.5T DDB design	=	0.01	um
M1.S.9b.ARTBS	Space between M1 (width = 0.076um) line-end and GT centerline in SDB design.	=	0.01	um
M1.S.17a.ARTB S	Space between M1 (width = 0.077um) centerline and GT centerline in SDB design.	=	0.0315	um
M1.S.10a.9TBS	Space between M1 (width = 0.082um) line and PowerRail centerline in 9T DDB design.	=	0.092/0.108/0. 135/0.247	um
M1.S.10a.7TBS	Space between M1 (width = 0.082um) line and PowerRail centerline in 7.5T DDB design.	=	0.19	um
M1.S.10a.ARTB S	Space between M1 (width = 0.082um) line and PowerRail centerline in SDB design.	=	0.141/0.199	um
M1.S.10b.9TBS	Space between M1 (width = 0.082um) centerline and GT	=	0/0.007/0.009/	um

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Rule number	Description	Opt.	Design Value	Unit
	centerline in 9T DDB design		0.019/0.026/0. 032/0.035/0.04 8	
M1.S.10b.7TBS	Space between M1 (width = 0.082um) centerline and GT centerline in 7.5T DDB design	=	0/0.003/0.007/ 0.009/0.01/0.0 19/0.025/0.026 /0.035/0.048	um
M1.S.10b.ARTBS	Space between M1 (width = 0.082um) centerline and GT centerline in SDB design.	=	0/0.002/0.006/ 0.007/0.009/0. 01/0.019/0.025 /0.026/0.035/0. 037/0.039/0.04 5/0.048	um
M1.S.10c.9TBS	Space between M1 (width = 0.082um) line-end and PowerRail centerline in 9T DDB design.	=	0.108/0.144/0. 171/0.176/0.20 8/0.235/0.240/ 0.256/0.272	um
M1.S.10c.7TBS	Space between M1 (width = 0.082um) line-end and PowerRail centerline in 7.5T DDB design.	=	0.08/0.112/0.1 44/0.176/0.208	um
M1.S.10c.ARTBS	Space between M1 (width = 0.082um) line-end and PowerRail centerline in SDB design.	=	0.08/0.112/0.1 44/0.176/0.208 /0.224/0.24/0.2 56	um
M1.S.10d.9TBS	Space between M1 (width = 0.082um) line-end and GT centerline in 9T DDB design	=	0.007/0.023/0. 045	um
M1.S.10d.7TBS	Space between M1 (width = 0.082um) line-end and GT centerline in 7.5T DDB design	=	0.029	um
M1.S.10d.ARTBS	Space between M1 (width = 0.082um) line-end and GT centerline in SDB design.	=	0.001/0.02	um
M1.S.11a.7TBS	Space between M1 (width = 0.096um) line-end and PowerRail centerline in 7.5T DDB design. DRC flag horizontal M1(width = 0.096um) line-end	=	\	um
M1.S.11b.7TBS	Space between M1 (width = 0.096um) centerline and GT centerline in 7.5T DDB design	=	0.048	um
M1.S.11c.9TBS	Space between M1 (width = 0.096um) centerline and GT	=	0.041	um

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Rule number	Description	Opt.	Design Value	Unit
	centerline in 9T DDB design			
M1.EX.1.9TBS	M1 (width = 0.032um) line-end extension GT centerline in 9T DDB design.	=	0.006/0.008	
M1.EX.1.7TBS	M1 (width = 0.032um) line-end extension GT centerline in 7.5T DDB design.	=	0.006/0.008	
M1.EX.1.ARTBS	M1 (width = 0.032um) line-end extension GT centerline in SDB design.	=	0.006/0.008	
M1.EX.2.9TBS	M1 (width = 0.034um) line-end extension GT centerline in 9T DDB design.	=	0.006/0.008	
M1.EX.2.7TBS	M1 (width = 0.034um) line-end extension GT centerline in 7.5T DDB design.	=	0.006/0.008	
M1.EX.2.ARTBS	M1 (width = 0.034um) line-end extension GT centerline in SDB design.	=	0.006/0.008	
M1.EX.3.7TBS	M1 (width = 0.035um) line-end extension GT centerline in 7.5T DDB design.	=	0.006/0.008	
M1.EX.3.ARTBS	M1 (width = 0.035um) line-end extension GT centerline in SDB design.	=	0.006	
M1.EX.10a.ARTBS	M1 (width = 0.038um) line-end extension PowerRail centerline in SDB design.	=	0.189	um
M1.EX.10b.ARTBS	M1 (width = 0.038um) line-end extension GT centerline in SDB design.	=	0.026	um
M1.EX.4.9TBS	M1 (width = 0.046um) line-end extension PowerRail centerline in 9T DDB design.	=	0.265	
M1.EX.4.ARTBS	M1 (width = 0.046um) line-end extension PowerRail centerline in SDB design.	=	0.135/0.189/0. 221/0.265	
M1.EX.5a.9TBS	M1 (width = 0.050um) line-end extension PowerRail centerline in 9T DDB design.	=	0.265	
M1.EX.5a.7TBS	M1 (width = 0.050um) line-end extension PowerRail centerline in 7.5T DDB design.	=	0.236	um
M1.EX.5a.ARTBS	M1 (width = 0.050um) line-end extension PowerRail centerline in SDB design.	=	0.233/0.236/0. 265	um

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Rule number	Description	Opt.	Design Value	Unit
M1.EX.5b.9TBS	M1 (width = 0.050um) line-end extension GT centerline in 9T DDB design.	=	0.007/0.015	
M1.EX.5b.7TBS	M1 (width = 0.050um) line-end extension GT centerline in 7.5T DDB design.	=	0.015	um
M1.EX.5b.ARTBS	M1 (width = 0.050um) line-end extension GT centerline in SDB design.	=	0.015/0.026/0.033/0.043/0.044	um
M1.EX.11.ARTBS	M1 (width = 0.058um) line-end extension PowerRail centerline in SDB design.	=	0.236	
M1.EX.6a.9TBS	M1 (width = 0.064um) line-end extension PowerRail centerline in 9T DDB design.	=	0.208	
M1.EX.6a.7TBS	M1 (width = 0.064um) line-end extension PowerRail centerline in 7.5T DDB design.	=	0.144/0.176	
M1.EX.6a.ARTBS	M1 (width = 0.064um) line-end extension PowerRail centerline in SDB design.	=	0.141/0.225/0.273	
M1.EX.6b.9TBS	M1 (width = 0.064um) line-end extension GT centerline in 9T DDB design.	=	0.023/0.034	
M1.EX.6b.7TBS	M1 (width = 0.064um) line-end extension GT centerline in 7.5T DDB design.	=	0.006/0.013/0.032/0.034/0.035/0.044	
M1.EX.6b.ARTBS	M1 (width = 0.064um) line-end extension GT centerline in SDB design.	=	0.006/0.025/0.032/0.034/0.044	
M1.EX.7.7TBS	M1 (width = 0.066um) line-end extension GT centerline in 7.5T DDB design. DRC flag all M1 (width = 0.066um) line-end space to GT centerline.	=	\	
M1.EX.7.ARTBS	M1 (width = 0.066um) line-end extension GT centerline in SDB design.	=	0.006/0.018	
M1.EX.8.7TBS	M1 (width = 0.076um) line-end extension GT centerline in 7.5T DDB design.	=	0.022	
M1.EX.8.ARTBS	M1 (width = 0.076um) line-end extension GT centerline	=	0.022	

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Rule number	Description	Opt.	Design Value	Unit
	in SDB design.			
M1.EX.12.ARTBS	M1 (width = 0.077um) line-end extension PowerRail centerline in SDB design.	=	0.204	
M1.EX.9a.9TBS	M1 (width = 0.082um) line-end extension PowerRail centerline in 9T DDB design.	=	0.190/0.272/0.208	um
M1.EX.9a.7TBS	M1 (width = 0.082um) line-end extension PowerRail centerline in 7.5T DDB design.	=	0.240	um
M1.EX.9a.ARTBS	M1 (width = 0.082um) line-end extension PowerRail centerline in SDB design.	=	0.24/0.272	um
M1.EX.9b.9TBS	M1 (width = 0.082um) line-end extension GT centerline in 9T DDB design.	=	0.037	
M1.EX.9b.7TBS	M1 (width = 0.082um) line-end extension GT centerline in 7.5T DDB design.	=	0.013	
M1.R.1a.9TBS	M1 (width = 0.032um) must be horizontal in 9T DDB design.			
M1.R.1a.7TBS	M1 (width = 0.032/0.035/0.066/0.076um) must be horizontal in 7.5T DDB design.			
M1.R.1b.9TBS	M1 (width = 0.038um) must be vertical in 9T DDB design.			
M1.R.1c.TBS	M1 (width = 0.046um) must be vertical.			
M1.R.1d.TBS	M1 (width = 0.09um) must be horizontal.			
M1.R.2.TBS	M1 (width = 0.09um) must interact with RSPMK1.			
M1.R.3.7TBS	M1 (width = 0.096um) must be vertical in 7.5T DDB design.			
M1.R.4.TBS	M1 must be orthogonal to grid.			
M1.S.12.TBS	Space between M1 and line-end (width < 0.046um, and PRL > -0.016um) in 9T DDB design.	≥	0.07	um
M1.S.13.TBS	Space between M1 and line-end (0.046um ≤ M1 width ≤ 0.049um, and PRL > -0.016um).	≥	0.036	um

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Rule number	Description	Opt.	Design Value	Unit
M1.S.14.TBS	Space between M1 line-end and line-end (width< 0.046um, and PRL > -0.016um) in 9T DDB design.	\geq	0.081	um
M1.S.15.TBS	Space between M1 outside vertex (M1 line-end outer vertex or L-shape outer vertex) to nearby L-shape inner vertex. DRC flag if both projection space < 0.036um	\geq	0.047	um

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8. Attachment

[14nm_Sealring_DR_20181120.gds](#)

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