Socle Technology Corporation

MDK-3D
3D Multimedia Development Kit

Hardware User Guide

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Preface

Read This First

About the Document

This user's manual describes how to set up, operate and use L6021 Development Kit (MDK-3D). It has been written for experienced users to getting start in short time.

Documentation Organization

This document contains the following chapters:

Chapter 1 MDK-3D EVB Overview

This chapter contains general overview of MDK-3D EVB, including block diagram, main features

Chapter 2 Setting up MDK-3D

This chapter describes how to start using MDK-3D EVB, including System requirement, how to set up every jumper.

Chapter 3 Hardware Description

This chapter describes the hardware architecture of MDK-3D EVB in more detail, including power, clock, reset, control, peripherals and bus interface.

Appendix A FPGA Pin Assignment

Provide detailed FPGA pin assignment.

Appendix B IO Expansion Board details

Provide mechanical dimension information of IO Expansion Daughter Board

Appendix C AMBA Expansion Board details

Provide mechanical dimension information of AMBA Expansion Daughter Board

Appendix D LCD-008 LCD Board details

Provide 5" TFT LCD board mechanical dimension and hardware information

Recommended information for further reading

The list shown below is the recommended information for user's further understanding to MDK-3D EVB.

- AMBA Specification
- Socle L6021 chip datasheet
- Programmer's guide
- Xilinx Virtex-5 datasheet

Chapter 1

MDK-3D EVB Overview

This chapter gives a brief description of the architecture, features of MDK-3D EVB. It contains the following sections:

- Introduction
- Features
- System Architecture

1.1 Introduction

Socle L6021 Connectivity ASIC includes two major portions -- one is a highly integrated, pre-verified and silicon-proven System-on-Chip (SoC) design platform core, the other is metal programmable logic cells and I/Os. By changing only 4-6 metal layers, fine-grained fabrics implement logic; the metal programmable logic cells allow timing-optimized ASIC-like cell to be built and ensure performance is optimal. The MDK-3D EVB is designed with Socle L6021 Connectivity ASIC and one on-chip FPGA to emulate on-chip metal programmable logic cells for user to develop, verify application and hardware/software easily.
The board also provides clock handling, URAT, MAC, RTC, DDR2 SDRAM, etc…. circuit and integrated software as a reference design.
Fig 1-1 is the overview for MDK-3D EVB. It shows the locations of every component,

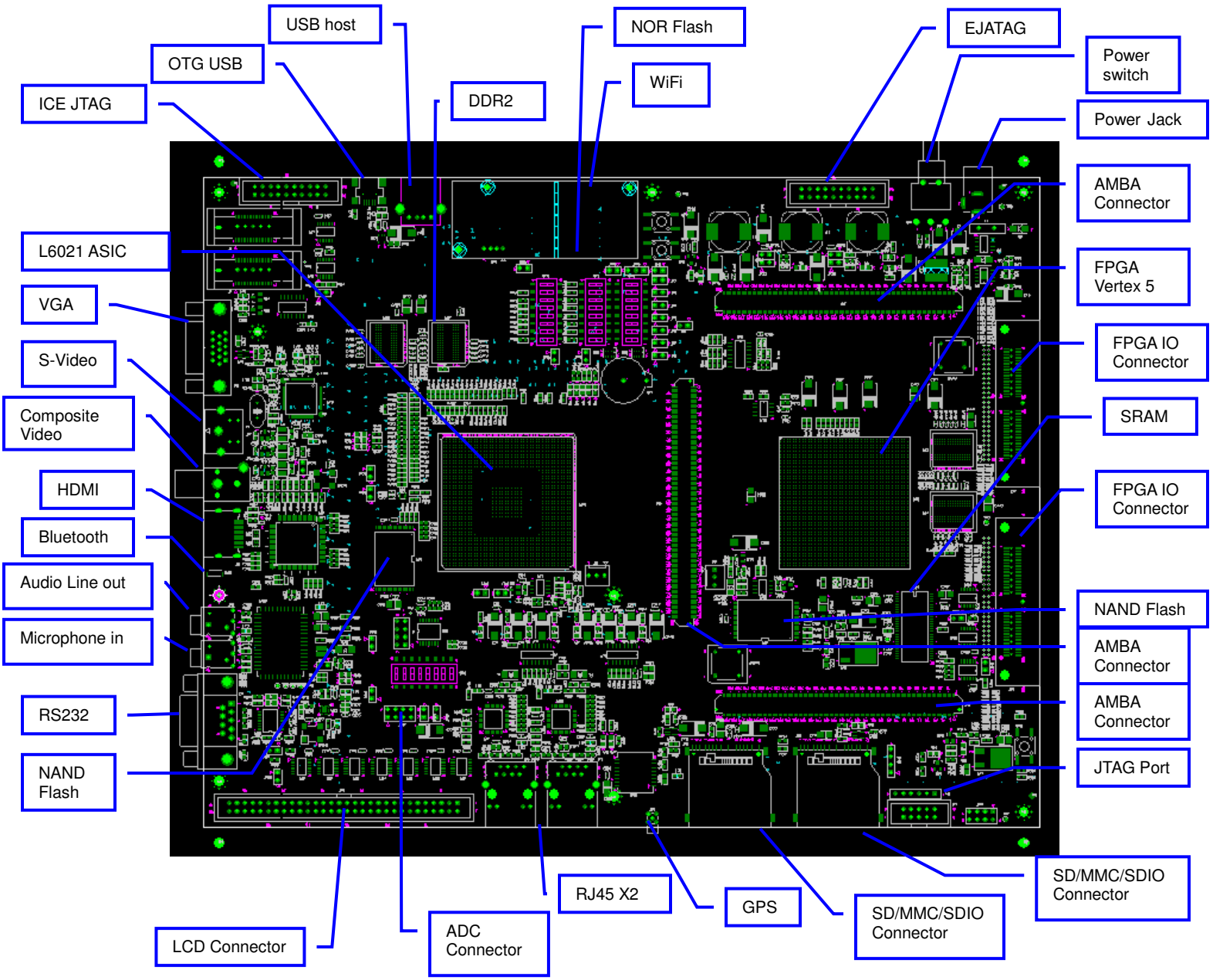


Fig1-1 MDK-3D EVB Overview

1.2 Features

The following is the main features list of MDK-3D EVB:

Main board

- A power switch and a power jack connector for 12V/3.33A AC/DC switching adapter power supply input.
- Socle L6021 Chip with PBGA-1380 (42.5mmX42.5mm) package on board.
- FPGA
  - Support one Xilinx Virtex-5 XC5VLX110FF1760 or XC5VLX220FF1760 or XC5VLX330FF1760 FPGA.
    - MDK-3D-110: support Xilinx Virtex-5 XC5VLX110FF1760
    - MDK-3D-220: support Xilinx Virtex-5 XC5VLX220FF1760
    - MDK-3D-330: support Xilinx Virtex-5 XC5VLX330FF1760
  - Support one 2.54mm 2x5 pins header for FPGA download port.
  - Support one 2.54mm 1x6 pins header for customer JTAG download port.
  - Support one 2.54mm 2x10 pins header for EJTAG port to use ARM image combined with debug port.
  - Support one 2M Bytes Cypress CY7C1061AV33-10ZXC SRAM.
  - Support one 1Gbx8 NAND Flash memory and up to 8G Bytes.
  - Support two 64Mbx16 DDR2-800 SDRAM and up to 512M Bytes total.
  - Support two 100 pins SAMTEC QSS-050-01-L-D-RA-WT-LS1 IO expansion connector and four 2.54mm 2x25 pins header combined with High speed FPGA Download/Debug port.
  - Support a 3V CR-1220 Battery is powered for encryption key.

- Memory
  - Support two 64M Bytes Numonyx JS28F512M29EW for Boot code with a 8 bits/16 bits data width jumper setting
  - Support two 64Mbx16 DDR2-800 SDRAM and up to 512M Bytes total.
  - Support a 1Gbx8 NAND Flash memory and up to 8G Bytes.

- Peripheral
  - Ethernet

    Two RJ-45 port

    Use IC-Plus IP101A PHY with MII interface on board

  - UART

    One UART for RS232 port (DB9 type)

    One UART for GPS module connection or FPGA or AMBA

expansion using
One UART for Bluetooth module connection

- SPI
  One SPI for TFT LCD module
  One SPI for touch screen controller
  One SPI for ADC controller
  One SPI is reserved for FPGA or AMBA expansion using

- SD/MMC/SDIO card interface
  Two SD/MMC/SDIO host socket

- Audio/I^2S
  One microphone connector on board
  One Line out connector on board
  Bluetooth audio support
- I^2C
  I^2C0 for regulator (for L6021), TV encoder, HDMI transmitter, Camera, Fan controller (for L6021), GPIO expander
  I^2C1 for regulator (for FPGA), Audio DAC, FM tuner, Fan controller (for FPGA), 3-axis accelerometer
  I^2C2 is reserved for FPGA or AMBA expansion using

- USB
  USB0 for WiFi module connection
  USB1 for A-type host connector
  USB2 for mini AB-type connector

- LCD controller
  A TV encoder with composite, S-video and VGA D-sub port
  or A 5” 800x480 pixel TFT LCD with touch panel
  or A 7” 800x480 pixel TFT LCD with touch panel
  or A HDMI transmitter with HDMI A-type connector

- VIP
  One VIP for a 0.3M pixels camera

- AHB/AXI
  Three Samtec BTH-150-06-F-D-A 300 pins connectors for AHB/AXI bus expansion

- Other
  - Two standard 2.54mm header with 8 ADC channels
  - One JTAG port which can chain to FPGA with 2x10 pin header for ICE debug
  - Two fan connectors for L6021 and FPGA heat radiation
  - One standard 2.54mm header for LCD daughter board connection

- 12 layers PCB

1.3 System Block Diagram

The Fig1-2 shows the MDK-3D EVB Block Diagram.

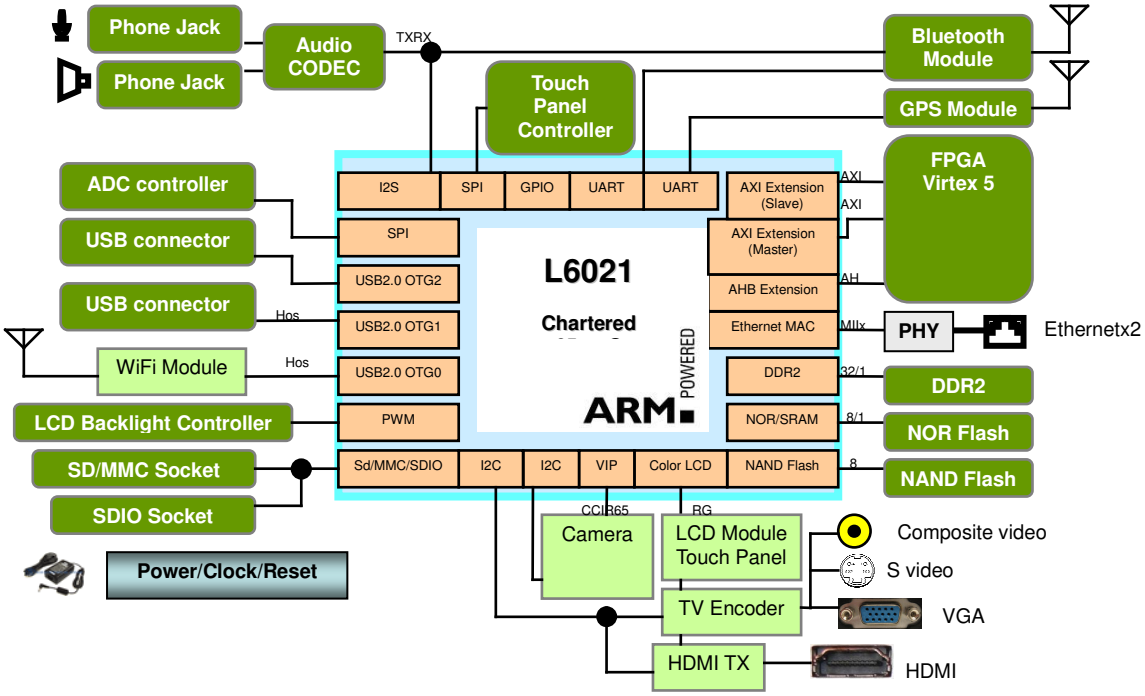


Fig1-2 MDK-3D Block Diagram

Chapter 2
Setting Up and Hardware Reference

This chapter describes how to use the MDK-3D EVB and shows the positions of jumper, headers and connectors. It contains the following sections:

- Install MDK-3D EVB
- Jumper Setting
- Switch Setting
- Connector
- LED Display

2.1 Install MDK-3D EVB

This section describes how to connect hardware components

2.1.1 Requirement

The development system should contain the following items at least:

- MDK-3D EVB
- 12VDC output power adapter
- Multi-ICE or other debug tool
- IBM compatible PC

Install Steps

1. Plug IO board or AMBA expansion board into MDK-3D FPGA Expansion Connector (optional)
2. Switch on power supply
3. Power on ICE

To prevent damaging to all boards, make sure to power down before inserting or removing any device.

2.2 Jumper Setting

In general, jumpers are used to select options for certain features. On MDK-3D EVB, some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (short) or remove it from the jumper pins. Fig 2-1 is the jumper/connector location diagram for MDK-3D EVB. The default settings shipped from Socle company are marked with a ★.

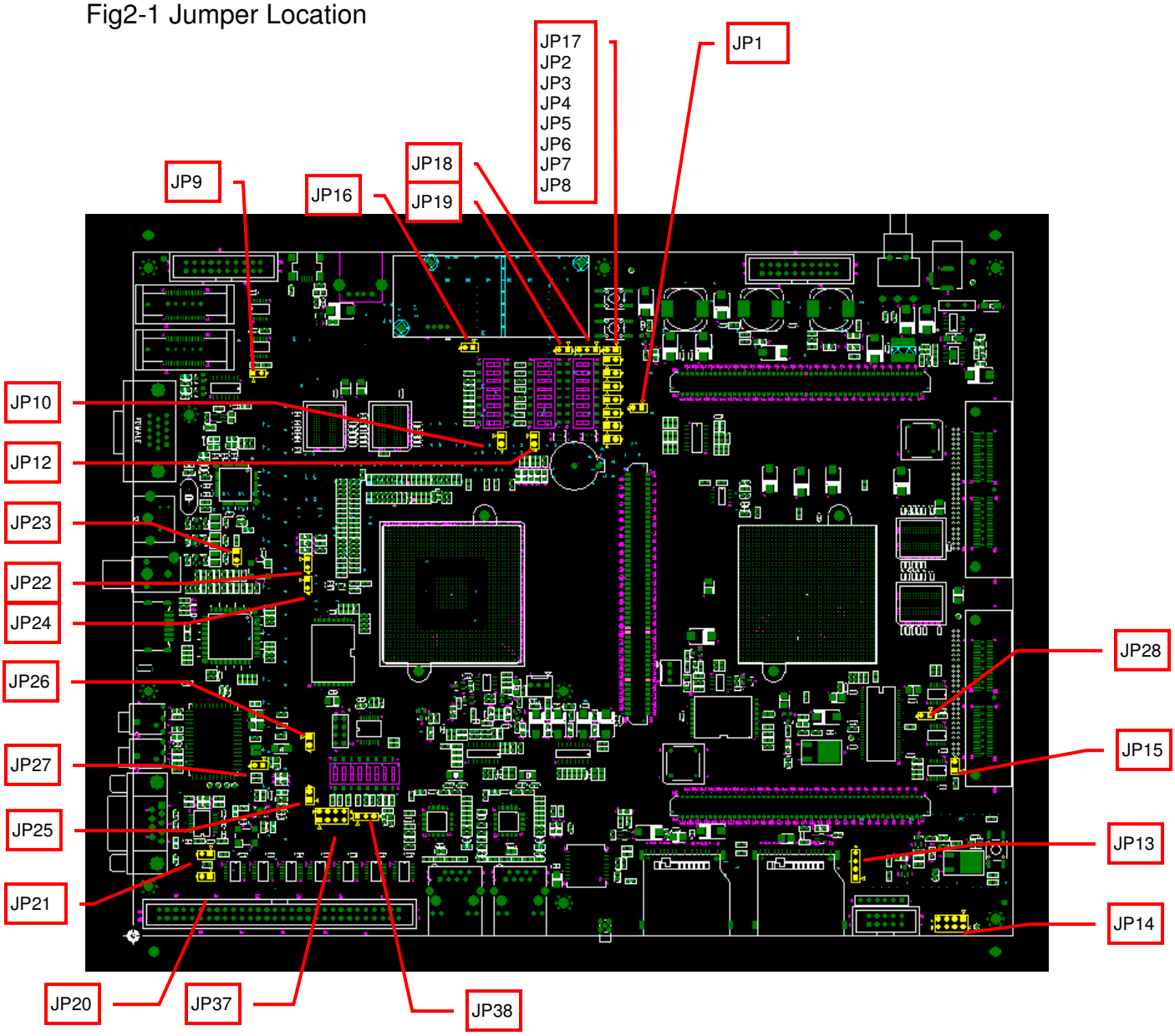
Make sure to have all of configuration jumpers on MDK-3D EVB in the proper location before turning on power

Table 2-1 Jumper List

Location	Function
JP1	FPGA Done reset to L6021
JP2	CPU_SEL0 Selection
JP3	CPU_SEL1 Selection
JP4	AHRESET_SEL Selection
JP5	PLL0BP Selection
JP6	PLL1BP Selection
JP7	PLL2BP Selection
JP8	LCD SEL
JP9	FPGA EJTAG Chain Selection
JP10	GPIO selection 1
JP12	GPIO selection 2
JP13	Xilinx FPGA Image Download Chain Setting
JP14	Xilinx FPGA image download channel selection 1
JP15	Xilinx FPGA image download channel selection 2
JP16	NOR Flash Data Bus Size Selection 1
JP17	NOR Flash Write Protected Setting 1
JP18	NOR Flash R/W Byte Setting
JP19	NOR Flash Write Protected Setting 2
JP20	TV encoder data bus selection
JP21	Video data 24bit/16bit selection
JP22	CVBS/S-video or VGA selection
JP23	HDMI data bus selection
JP24	Reserved
JP25	Audio ADC data bus selection
JP26	I2S Master Selection 1
JP27	I2S Slave Selection 2

JP28	Xilinx FPGA image download channel selection 3
JP37	ADC connector
JP38	ADC voltage reference Selection

Fig2-1 Jumper Location



2.2.1 FPGA Status/ Sleep mode function Selection

Set FPGA status for generating system reset

JP1	Description
ON	FPGA active/No FPGA on board
OFF	FPGA no image/ When Sleep mode active

2.2.2 CPU Selection

Select CPU type and status

JP2	JP3	Description
OFF	OFF	Internal ARM1176JZF active.
OFF	ON	Internal ARM926EJ active.
ON	OFF	Reserved.
ON	ON	All internal CPUs inactive.

2.2.3 AHRESET_SEL Selection

Select AXI and AHB bus reset generation mode

JP4	Description
OFF	Hardware reset, external bus reset is the same as internal bus one
ON	Software reset, for dual-core sequential booting

2.2.4 PLL0BP Selection

Select status of PLL0.

JP5	Description
OFF	PLL0 active
ON	PLL0 bypass mode

2.2.5 PLL1BP Selection

Select status of PLL1.

JP6	Description
OFF	PLL1 active
ON	PLL1 bypass mode

2.2.6 PLL2BP Selection

Select status of PLL2.

JP7	Description
OFF	PLL2 active
ON	PLL2 bypass mode

2.2.7 FPGA EJTAG Chain Selection

Select Independent/chain of EJTAG.

JP9	Description
OFF	EJTAG chain to JP13
ON	Independent EJTAG at J13

2.2.8 GPIO selection 1

Select GPIO or PLL detection.

JP10	Description
OFF	GPIO0~2 are PLL detections
ON	GPIO0~2 are GPIOs

2.2.9 GPIO selection 2

Select GPIO or PLL detection.

JP12	Description
OFF	GPIO3~5, GPIO8~12 are PLL detections
ON	GPIO3~5, GPIO8~12 are GPIOs

2.2.10 Xilinx FPGA Image Download Chain Setting

Set FPGA image download chain. This is a 1X4 pin header.

JP13	Description	Default Setting
1-2, 3-4	Program PROM & FPGA	★
2-3	Program FPGA only	

2.2.11 Xilinx FPGA image download channel selection 1

Set FPGA image download channel. This is a 2X4 pin header.

JP14	Description
1-2, 3-4, 5-6 OFF	High Speed Download
1-2, 3-4, 5-6 ON	Normal Download PROM & FPGA
1-2, 5-6 OFF, 3-4 ON	Normal Download FPGA only
7-8 OFF	Disable IO pin pull-up internal
7-8 ON	Enable IO pin pull-up internal

2.2.12 Xilinx FPGA image download channel selection 2

Set FPGA image download channel.

JP15	Description
OFF	High Speed Download
ON	Normal Download

2.2.13 NOR Flash Data Bus Size Selection 1

Select Boot Flash data bus size

JP16	Description	Default Setting
ON	8 Bit Mode	
OFF	16 Bit Mode	★

2.2.14 NOR Flash Write Protected Setting 1

Select Flash Programming or Write Protected of U51. This is a 1X2 pin header.

JP17	Description	Default Setting
ON	Flash Programming Mode	
OFF	Flash Write Protected Mode	★

2.2.15 NOR Flash R/W Byte Setting

Select Boot Flash data bus size. This is a 1X3 pin header.

JP18	Description	Default Setting
1-2	16 Bit Mode	★
2-3	8 Bit Mode	

2.2.16 NOR Flash Write Protected Setting 2

Select Flash Programming or Write Protected of U54. This is a 1X2 pin header.

JP19	Description	Default Setting
ON	Flash Programming Mode	★
OFF	Flash Write Protected Mode	

2.2.17 TV encoder data bus selection

Enable/Disable data bus of TV encoder.

JP20	Description
OFF	Disable
ON	Enable

2.2.18 Video data 24bit/16bit selection

Select Video data bus 24bit/16bit width.

JP21	Description
OFF	24bit width
ON	16bit width

2.2.19 CVBS/S-video or VGA selection

Select CVBS/S-video or VGA output.

JP22	Description
OFF	CVBS/S-video
ON	VGA

2.2.20 HDMI data bus selection

Enable/Disable data bus of HDMI.

JP23	Description
OFF	Disable
ON	Enable

2.2.21 Audio ADC data bus selection

Enable/Disable data bus of Audio ADC.

JP25	Description
OFF	Disable
ON	Enable

2.2.22 Audio ADC Master/Slave selection

Enable/Disable Master of Audio ADC.

JP26	Description
OFF	Disable
ON	Enable

2.2.23 Audio ADC Master/Slave selection

Enable/Disable Slave of Audio ADC.

JP27	Description
OFF	Disable
ON	Enable

2.2.24 Xilinx FPGA image download channel selection 3

Set FPGA image download channel.

JP28	Description
OFF	High Speed Download
ON	Normal Download

2.2.25 ADC voltage reference Selection

IO of ADC. This is a 2X4 pin header.

JP37	Description
1	ADC_IN0
3	ADC_IN1
5	ADC_IN2
7	ADC_IN3
2	ADC_VREF
4	+3.3V
6	+3.3V
8	GND

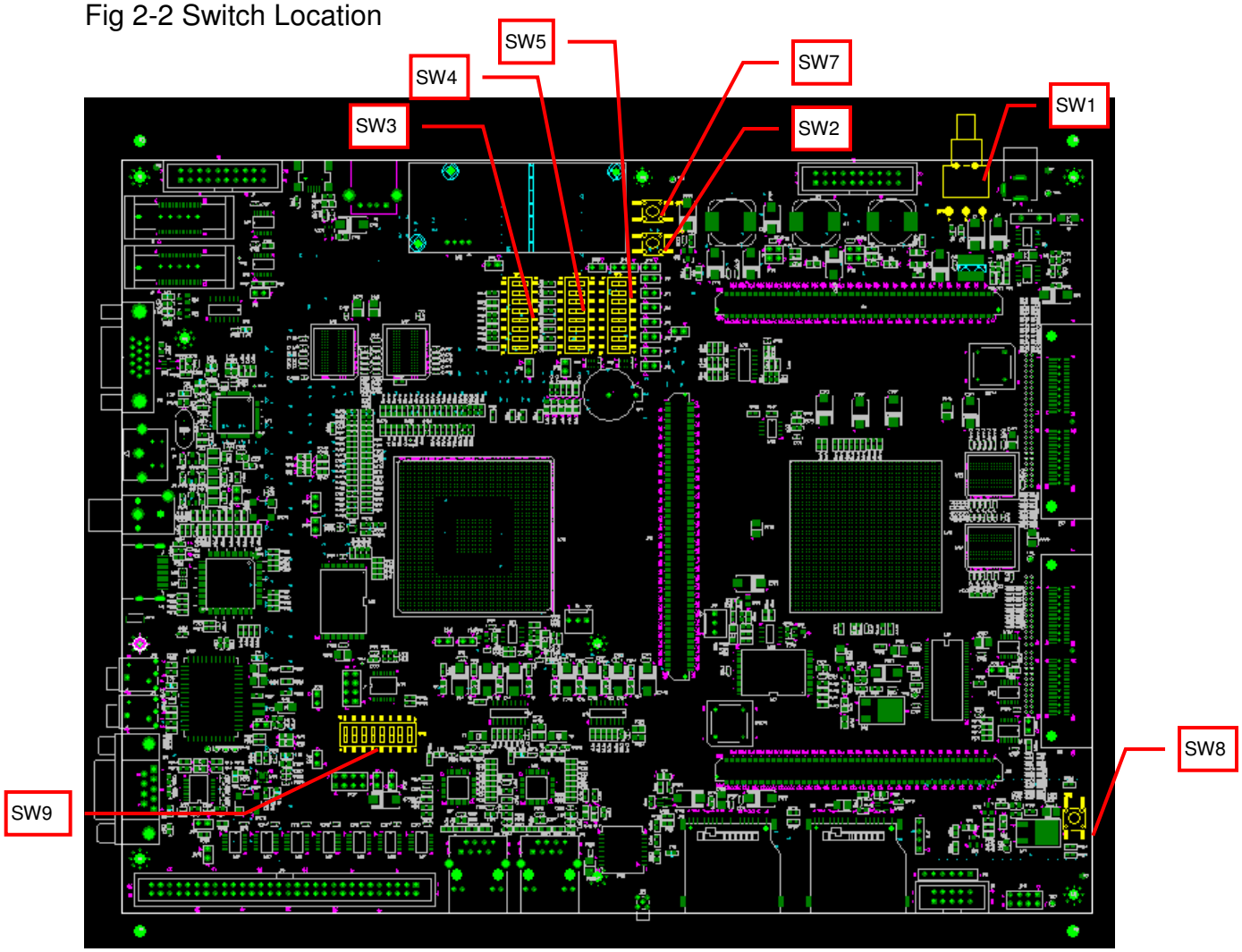
2.3 Switch Setting

The section shows the location of all the switches on the board, and describes the function of each switch.

Table 2-2 Switch List

Location	Function
SW1	System Power Switch
SW2	System Reset Push Button
SW3	L6021 configurations Setting Switch 1
SW4	L6021 configurations Setting Switch 2
SW5	L6021 GPIO Setting Switch
SW7	Design Reset Switch to FPGA
SW8	Xilinx FPGA Re-program Start
SW9	Design of ADC Switch

Fig 2-2 Switch Location



2.3.1 System Power Switch

SW1 switches on/off system power.

2.3.2 System Reset Button

This push button SW2 is provided to reset all system which is low active.

2.3.3 L6021 configurations Setting Switch 1

SW3 provides L6021 configurations settings as follows.

SW3	Action	Description
1	OFF	Set DEBUG_SEL0 to Low, see Note1
	ON	Set DEBUG_SEL0 to High
2	OFF	Set DEBUG_SEL1 to Low
	ON	Set DEBUG_SEL1 to High
3	OFF	Reserved
	ON	Reserved
4	OFF	Reserved
	ON	Reserved
5	OFF	Set PLL0_CONFIG0 to Low, see Note2
	ON	Set PLL0_CONFIG0 to High
6	OFF	Set PLL0_CONFIG1 to Low
	ON	Set PLL0_CONFIG1 to High
7	OFF	Set PLL0_CONFIG2 to Low
	ON	Set PLL0_CONFIG2 to High
8	OFF	Reserved
	ON	Reserved

Note1 : DEBUG_SEL[1:0]: CPU JTEG debug mode section.
00: Debug embedded ARM1176JZF or ARM926EJ core only
01: Reserved.
10: Debug both embedded and external processors.
-> Embedded processor -> External processor.
11: Debug external processor only.

Note2: PLL0 output clock configuration, when CLKPLL0 is 32MHz.
PLL0 is the clock source of AXI/AHB/APB bus clock.
AXI clock = 1/2 PLL0 clock; AHB clock = 1/4 PLL0 clock; APB clock = 1/8 PLL0 clock.
000: 336MHz
001: 400MHz
010: 528MHz
011: 664MHz
100: 800MHz

101: 928MHz
110: 1000MHz
111: 1056MHz

2.3.4 L6021 configurations Setting Switch 2

SW4 provides L6021 configurations settings as follows.

SW4	Action	Description
1	OFF	Set PLL1_CONFIG0 to Low, see Note3
	ON	Set PLL1_CONFIG0 to High
2	OFF	Set PLL1_CONFIG1 to Low
	ON	Set PLL1_CONFIG1 to High
3	OFF	Set PLL1_CONFIG2 to Low
	ON	Set PLL1_CONFIG2 to High
4	OFF	Set PLL2_CONFIG0 to Low, see Note4
	ON	Set PLL2_CONFIG0 to High
5	OFF	Set PLL2_CONFIG1 to Low
	ON	Set PLL2_CONFIG1 to High
6	OFF	Set PLL2_CONFIG2 to Low
	ON	Set PLL2_CONFIG2 to High
7	OFF	Set CLKEXT_CONFIG0 to Low, see Note5
	ON	Set CLKEXT_CONFIG0 to High
8	OFF	Set CLKEXT_CONFIG1 to Low
	ON	Set CLKEXT_CONFIG1 to High

Note3: PLL1 output clock configuration, when CLKPLL1 is 32MHz.
PLL1 is the clock source of ARM1176JZF CPU clock.
000: 336MHz
001: 400MHz
010: 528MHz
011: 664MHz
100: 800MHz
101: 928MHz
110: 1000MHz
111: 1056MHz

Note4: PLL2 output clock configuration, when CLKPLL2 is 32MHz.
PLL2 is the clock source of ARM926EJ CPU clock.
000: 336MHz
001: 400MHz
010: 528MHz
011: 664MHz
100: 800MHz

101: 928MHz
110: 1000MHz
111: 1056MHz

Note5: External ACLK/HCLK bus clock output (CLKEXTOUT) configuration.
00: Divide by 1
01: Divide by 2
10: Divide by 4
11: Divide by 8

2.3.5 L6021 GPIO Setting Switch

SW5 provides High/Low signal to GPIO Port.

SW5	Action	Description
1	OFF	Set GPIO0 to High
	ON	Set GPIO0 to Low
2	OFF	Set GPIO1 to High
	ON	Set GPIO1 to Low
3	OFF	Set GPIO2 to High
	ON	Set GPIO2 to Low
4	OFF	Set GPIO3 to High
	ON	Set GPIO3 to Low
5	OFF	Set GPIO4 to High
	ON	Set GPIO4 to Low
6	OFF	Set GPIO5 to High
	ON	Set GPIO5 to Low
7	OFF	Set GPIO6 to High
	ON	Set GPIO6 to Low
8	OFF	Set GPIO7 to High
	ON	Set GPIO7 to Low

2.3.6 ADC Setting Switch

SW6 provides ADC test on board, see 3.5.15 section.

SW9	Action	Description
1	OFF	Set ADC ch0 connected to connector JP37.1
	ON	Set ADC ch0 test on board
2	OFF	Set ADC ch1 connected to connector JP37.3
	ON	Set ADC ch1 test on board
3	OFF	Set ADC ch2 connected to connector JP37.5
	ON	Set ADC ch2 test on board

4	OFF	Set ADC ch3 connected to connector JP37.7
	ON	Set ADC ch3 test on board
5	OFF	Set ADC ch4 connected to connector J7.1
	ON	Set ADC ch4 test on board
6	OFF	Set ADC ch5 connected to connector J7.3
	ON	Set ADC ch5 test on board
7	OFF	Set ADC ch6 connected to connector J7.5
	ON	Set ADC ch6 test on board
8	OFF	Set ADC ch7 connected to connector J7.7
	ON	Set ADC ch7 test on board

2.3.7 FPGA Reset Button

This push button SW7 is provided to reset FPGA which is low active.

2.3.8 FPGA Re-program Switch

SW8 restarts or resets download image process from EEPROM to Xilinx FPGA

2.2.9 ADC voltage reference Selection

Select voltage reference of ADC. This is a 1X3 pin header.

JP35	Description
1-2	Voltage reference is 3.3V
2-3	Voltage reference is PWM1 charged

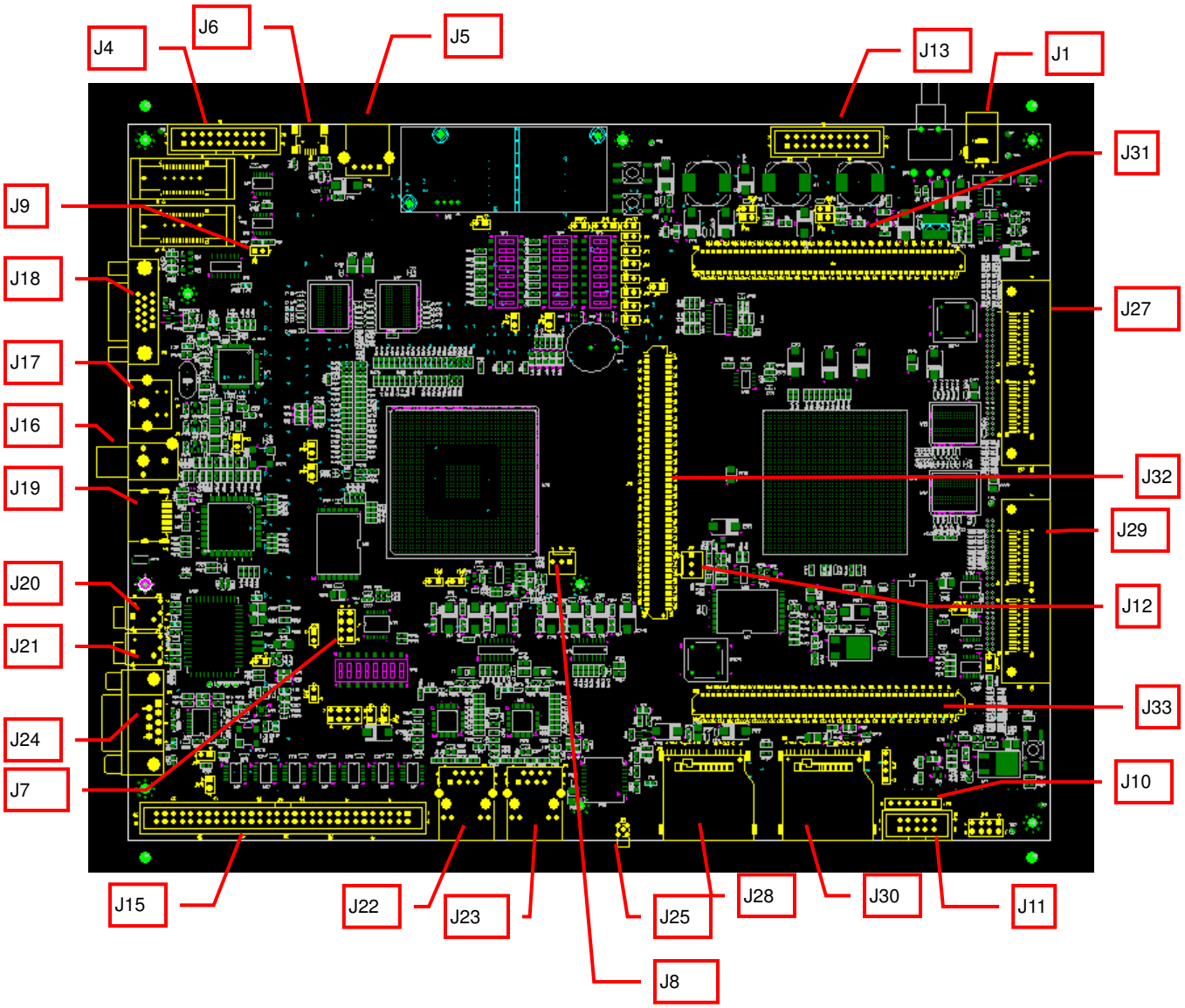
2.4 Connectors

The section shows the location of all the connectors on the board, and describes the function of each connector.

Table 2-3 Connector List

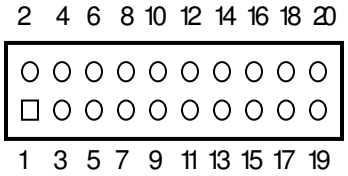
Location	Function
J1	Power Jack
J4	ICE JTAG Port
J5	USB A-type Host Port
J6	Mini USB AB-type OTG Port
J7	ADC/PWM external connector
J8	Fan connector for L6021
J9	ADC external connector
J10	Download JTAG Connector 1 for Xilinx FPGA
J11	Download JTAG Connector 2 for Xilinx FPGA
J12	Fan connector for FPGA
J13	EJTAG Connector for FPGA
J15	External LCD Connector
J16	Video composite Port
J17	S-video Port
J18	VGA Port
J19	HDMI Port
J20	Audio Stereo Line out Port
J21	Audio Stereo Line in Port
J22	RJ45 10/100M Ethernet Port 1
J23	RJ45 10/100M Ethernet Port 2
J24	RS232 Port
J25	GPS antenna connector(MMCX)
J27	FPGA IO Expansion Connector 1
J28	SD/MMC/SDIO socket 1
J29	FPGA IO Expansion Connector 2
J30	SD/MMC/SDIO socket 2
J31	AMBA Expansion Connector A
J32	AMBA Expansion Connector B
J33	AMBA Expansion Connector C

Fig 2-3 Connector Location



2.4.1 ICE JTAG Connector

The connector is used to link with ICE for ARM Processor system program developing.

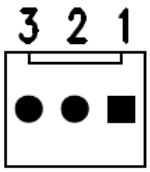


J4

Pin	Name	Pin	Name
1	+3.3V	2	+3.3V
3	ARM_nTRST	4	GND
5	ARM_TDI	6	GND
7	ARM_TMS	8	GND
9	ARM_TCK	10	GND
11	ARM_RTCK	12	GND
13	ARM_TDO	14	GND
15	ARM_nSRST	16	GND
17	ARM_DBGRQ	18	GND
19	ARM_DBGACK	20	GND

2.4.2 Fan connector for L6021

The connector links with fan for L6021 cooling.

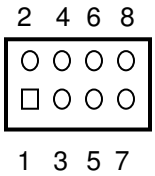


J8

Pin	Name
1	Negative power of fan
2	Positive power of fan
3	Detection

2.4.3 ADC/PWM external connector

The 2x4 pin header is used to link with PWM signals.

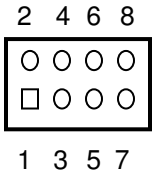


J7

Pin	Name	Pin	Name
1	ADC_IN4	2	PWM0
3	ADC_IN5	4	PWM1
5	ADC_IN6	6	PWM2
7	ADC_IN7	8	PWM3

2.4.4 ADC external connector

The connector contains all ADC signals.



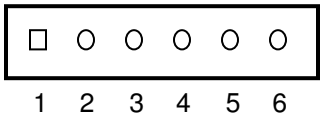
JP37

Pin	Name	Pin	Name
1	ADC_IN0	2	ADC_VREF
3	ADC_IN1	4	3V3P
5	ADC_IN2	6	3V3P
7	ADC_IN3	8	GND

5

2.4.5 Download JTAG Connector 1 for Xilinx FPGA

The connector is used to link with FPGA download cable for FPGA programming.

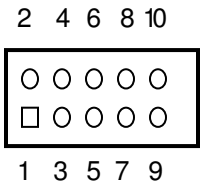


J10

Pin	Name
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	+3.3V

2.4.6 Download JTAG Connector 2 for Xilinx FPGA

The connector is used to link with FPGA download cable for FPGA programming.

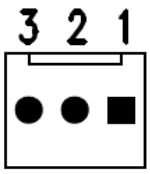


J11

Pin	Name	Pin	Name
1	TCK	2	GND
3	TDO	4	+3.3V
5	TMS	6	+3.3V
7	No Connect	8	No Connect
9	TDI	10	GND

2.4.7 Fan connector for FPGA

The connector links with fan for FPGA cooling.

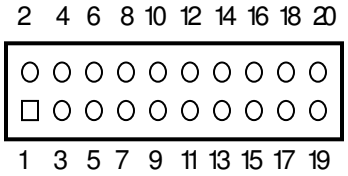


J12

Pin	Name
1	Negative power of fan
2	Positive power of fan
3	Detection

2.4.8 EJTAG Connector for FPGA

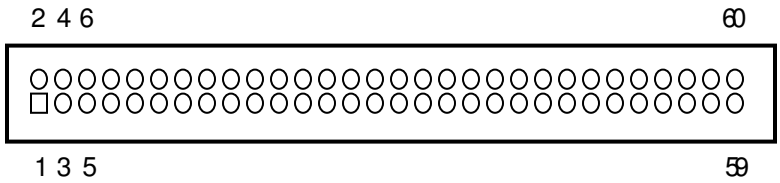
It connects to FPGA for debug. For FPGA pin assignment information, please refer to Appendix A.3.



J13

Pin	Name	Pin	Name
1	+3.3V	2	+3.3V
3	EJTAG_nTRST/FPGA GPIO	4	GND
5	EJTAG _TDI/ FPGA GPIO	6	GND
7	EJTAG _TMS/FPGA GPIO	8	GND
9	EJTAG _TCK/FPGA GPIO	10	GND
11	EJTAG _RTCK/FPGA GPIO	12	GND
13	EJTAG _TDO/FPGA GPIO	14	GND
15	EJTAG _nSRST	16	GND
17	Pull Dwon 4.7K ohms	18	GND
19	Pull Dwon 4.7K ohms	20	GND

2.4.11 External LCD Connector

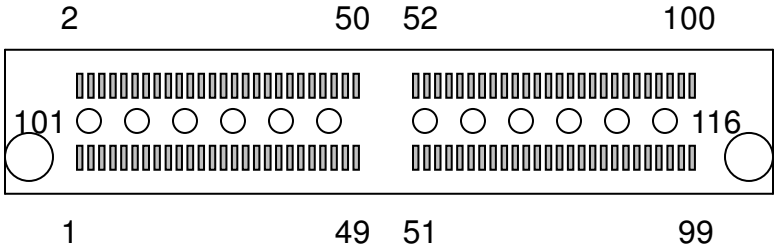


J15

Pin	Name	Pin	Name
1	LCD_CP	2	DB0
3	DB1	4	DB2
5	DB3	6	DB4
7	DB5	8	DB6
9	DB7	10	DG0
11	DG1	12	DG2
13	DG3	14	DG4
15	DG5	16	DG6
17	DG7	18	DR0
19	DR1	20	DR2
21	DR3	22	DR4
23	DR5	24	DR6
25	DR7	26	LCD_LP
27	LCD_FP	28	LCD_AC
29	LCDRSTn	30	LCD_POWER
31	EXT_INT0_PEN	32	PWM0
33	SPI0_SCK	34	SPI0_SCSn1
35	SPI0_MOSI	36	SPI0_SCSn0
37	SPI0_MISO	38	EXT_INT4_TS_BZ
39	I2C0_DATA	40	I2C0_CLK
41	VIP_CLK	42	VIP_D7
43	VIP_D0	44	VIP_D6
45	VIP_D1	46	VIP_D5
47	VIP_D2	48	VIP_D4
49	EXT_INT2_CAM	50	VIP_D3
51	+3.3V	52	GND
53	+3.3V	54	GND
55	+3.3V_Standby	56	GND
57	+5V	58	GND
59	+5V	60	GND

2.4.12 FPGA IO Expansion Connector 1

The Slot is provided to extend design IO functions. For FPGA pin assignment information, please refer to Appendix A.2.



J27

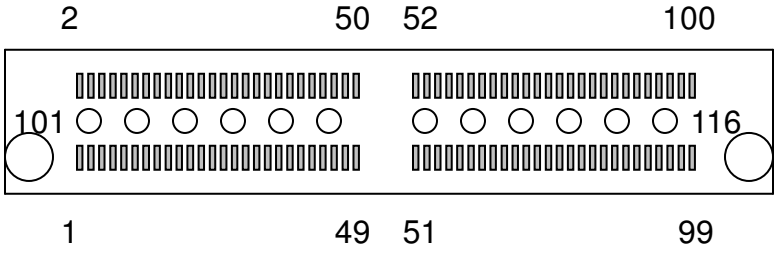
Pin	Name	Pin	Name
1	P1_101	2	P1_151
3	P1_102	4	P1_152
5	P1_103	6	P1_153
7	P1_104	8	P1_154
9	P1_105	10	P1_155
11	P1_106	12	P1_156
13	P1_107	14	P1_157
15	P1_108	16	P1_158
17	P1_109	18	P1_159
19	P1_110	20	P1_160
21	P1_111	22	P1_161
23	P1_112	24	P1_162
25	P1_113	26	P1_163
27	P1_114	28	P1_164
29	P1_115	30	P1_165
31	P1_116	32	P1_166
33	P1_117	34	P1_167
35	P1_118	36	P1_168
37	P1_119	38	P1_169
39	P1_120	40	P1_170
41	P1_121	42	P1_171
43	P1_122	44	P1_172
45	P1_123	46	P1_173
47	P1_124	48	P1_174
49	P1_125	50	P1_175
51	P1_126	52	P1_176
53	P1_127	54	P1_177
55	P1_128	56	P1_178

57	P1_129	58	P1_179
59	P1_130	60	P1_180
61	P1_131	62	P1_181
63	P1_132	64	P1_182
65	P1_133	66	P1_183
67	P1_134	68	P1_184
69	P1_135	70	P1_185
71	P1_136	72	P1_186
73	P1_137	74	P1_187
75	P1_138	76	P1_188
77	P1_139	78	P1_189
79	P1_140	80	P1_190
81	P1_141	82	P1_191
83	P1_142	84	P1_192
85	P1_143	86	P1_193
87	P1_144	88	P1_194
89	P1_145	90	P1_195
91	P1_146	92	P1_196
93	P1_147	94	P1_197
95	P1_148	96	P1_198
97	P1_149	98	P1_199
99	P1_150	100	P1_200

101	+5V
102	+5V
103	+5V
104	+5V
105	+5V
106	+5V
107	+5V
108	+5V
109	GND
110	GND
111	GND
112	GND
113	GND
114	GND
115	GND
116	GND

2.4.13 FPGA IO Expansion Connector 2

The Slot is provided to extend design IO functions. For FPGA pin assignment information, please refer to Appendix A.2.



J29

Pin	Name	Pin	Name
1	P1_1	2	P1_51
3	P1_2	4	P1_52
5	P1_3	6	P1_53
7	P1_4	8	P1_54
9	P1_5	10	P1_55
11	P1_6	12	P1_56
13	P1_7	14	P1_57
15	P1_8	16	P1_58
17	P1_9	18	P1_59
19	P1_10	20	P1_60
21	P1_11	22	P1_61
23	P1_12	24	P1_62
25	P1_13	26	P1_63
27	P1_14	28	P1_64
29	P1_15	30	P1_65
31	P1_16	32	P1_66
33	P1_17	34	P1_67
35	P1_18	36	P1_68
37	P1_19	38	P1_69
39	P1_20	40	P1_70
41	P1_21	42	P1_71
43	P1_22	44	P1_72
45	P1_23	46	P1_73
47	P1_24	48	P1_74
49	P1_25	50	P1_75
51	P1_26	52	P1_76
53	P1_27	54	P1_77
55	P1_28	56	P1_78

57	P1_29	58	P1_79
59	P1_30	60	P1_80
61	P1_31	62	P1_81
63	P1_32	64	P1_82
65	P1_33	66	P1_83
67	P1_34	68	P1_84
69	P1_35	70	P1_85
71	P1_36	72	P1_86
73	P1_37	74	P1_87
75	P1_38	76	P1_88
77	P1_39	78	P1_89
79	P1_40	80	P1_90
81	P1_41	82	P1_91
83	P1_42	84	P1_92
85	P1_43	86	P1_93
87	P1_44	88	P1_94
89	P1_45	90	P1_95
91	P1_46	92	P1_96
93	P1_47	94	P1_97
95	P1_48	96	P1_98
97	P1_49	98	P1_99
99	P1_50	100	P1_100

101	+5V
102	+5V
103	+5V
104	+5V
105	+5V
106	+5V
107	+5V
108	+5V
109	GND
110	GND
111	GND
112	GND
113	GND
114	GND
115	GND
116	GND

2.4.14 AMBA Expansion Connector A

The Slot is provided to extend design IO functions for AMBA expansion. For FPGA pin assignment information, please refer to Appendix A.1 and A.4.

J31

Pin	Name	Pin	Name
1	WDATA_S9	2	WDATA_S8
3	WDATA_S7	4	WDATA_S6
5	WDATA_S5	6	WDATA_S4
7	WDATA_S3	8	WDATA_S2
9	WDATA_S1	10	WDATA_S0
11	WREADY_S	12	WVALID_S
13	WID_S8	14	WID_S7
15	WID_S6	16	WID_S5
17	WID_S4	18	WID_S3
19	WID_S2	20	WID_S1
21	WID_S0	22	WSTRB_S7
23	WSTRB_S6	24	WSTRB_S5
25	WSTRB_S4	26	WSTRB_S3
27	WSTRB_S2	28	WSTRB_S1
29	WSTRB_S0	30	RVALID_S
31	RREADY_S	32	RID_S8
33	RID_S7	34	RID_S6
35	RID_S5	36	RID_S4
37	RID_S3	38	RID_S2
39	RID_S1	40	RID_S0
41	WDATA_S49	42	WDATA_S48
43	WDATA_S47	44	WDATA_S46
45	WDATA_S45	46	WDATA_S44
47	WDATA_S43	48	WDATA_S42
49	WDATA_S41	50	WDATA_S40
51	WDATA_S39	52	WDATA_S38
53	WDATA_S37	54	WDATA_S36
55	WDATA_S35	56	WDATA_S34
57	WDATA_S33	58	WDATA_S32
59	WDATA_S31	60	WDATA_S30

61	WDATA_S29	62	WDATA_S28
63	WDATA_S27	64	WDATA_S26
65	WDATA_S25	66	WDATA_S24
67	WDATA_S23	68	WDATA_S22
69	WDATA_S21	70	WDATA_S20
71	WDATA_S19	72	WDATA_S18
73	WDATA_S17	74	WDATA_S16
75	WDATA_S15	76	WDATA_S14
77	WDATA_S13	78	WDATA_S12
79	WDATA_S11	80	WDATA_S10
81	WDATA_S63	82	WDATA_S62
83	WDATA_S61	84	WDATA_S60
85	WDATA_S59	86	WDATA_S58
87	WDATA_S57	88	WDATA_S56
89	WDATA_S55	90	WDATA_S54
91	WDATA_S53	92	WDATA_S52
93	WDATA_S51	94	WDATA_S50
95	RDATA_S63	96	RDATA_S62
97	RDATA_S61	98	RDATA_S60
99	RDATA_S59	100	RDATA_S58
101	RDATA_S57	102	RDATA_S56
103	RDATA_S55	104	RDATA_S54
105	RDATA_S53	106	RDATA_S52
107	RDATA_S51	108	RDATA_S50
109	RDATA_S49	110	RDATA_S48
111	RDATA_S47	112	RDATA_S46
113	RDATA_S45	114	RDATA_S44
115	RDATA_S43	116	RDATA_S42
117	RDATA_S41	118	RDATA_S40
119	RDATA_S39	120	RDATA_S38
121	BID_S8	122	BID_S7
123	BID_S6	124	BID_S5
125	BID_S4	126	BID_S3
127	BID_S2	128	BID_S1
129	BID_S0	130	BRESP_S1
131	BRESP_S0	132	ARBURST_S1
133	ARBURST_S0	134	ARCACHE_S3
135	ARCACHE_S2	136	ARCACHE_S1
137	ARCACHE_S0	138	ARLOCK_S1
139	ARLOCK_S0	140	ARSIZE_S2
141	ARSIZE_S1	142	ARSIZE_S0
143	ARLEN_S3	144	ARLEN_S2

145	ARLEN_S1	146	ARLEN_S0
147	ARVALID_S	148	ARREADY_S
149	ARPROT_S2	150	ARPROT_S1
151	ARPROT_S0	152	ARADDR_S31
153	ARADDR_S30	154	ARADDR_S29
155	ARADDR_S28	156	ARADDR_S27
157	ARADDR_S26	158	ARADDR_S25
159	ARADDR_S24	160	ARADDR_S23
161	GND	162	GND
163	EXTRESET_N	164	HSEL
165	HGRANT	166	HBURST2
167	HBURST1	168	HBURST0
169	HTRANS1	170	HTRANS0
171	HADDR31	172	HADDR30
173	HADDR29	174	HADDR28
175	HADDR27	176	HADDR26
177	HADDR25	178	HADDR24
179	HADDR23	180	HADDR22
181	HADDR21	182	HADDR20
183	HADDR19	184	HADDR18
185	HADDR17	186	HADDR16
187	HADDR15	188	HADDR14
189	HADDR13	190	HADDR12
191	HADDR11	192	HADDR10
193	HADDR9	194	HADDR8
195	HADDR7	196	HADDR6
197	HADDR5	198	HADDR4
199	HADDR3	200	HADDR2
201	HADDR1	202	HADDR0
203	GND	204	CLKEXTOUT
205	HREADY	206	HWRITE
207	HLOCK	208	HBUSREQ
209	HRESP1	210	HRESP0
211	HSIZE1	212	HSIZE0
213	HDATA31	214	HDATA30
215	HDATA29	216	HDATA28
217	HDATA27	218	HDATA26
219	HDATA25	220	HDATA24
221	HDATA23	222	HDATA22
223	HDATA21	224	HDATA20
225	HDATA19	226	HDATA18
227	HDATA17	228	HDATA16

229	HDATA15	230	HDATA14
231	HDATA13	232	HDATA12
233	HDATA11	234	HDATA10
235	HDATA9	236	HDATA8
237	HDATA7	238	HDATA6
239	HDATA5	240	HDATA4
241	HDATA3	242	HDATA2
243	HDATA1	244	HDATA0
245	GND	246	GND
247	EXT_INT5_FPGA	248	EXT_INT4_FPGA
249	EXT_INT3_FPGA	250	EXT_INT2_FPGA
251	EXT_INT1_FPGA	252	EXT_INT0_FPGA
253	I2C2_DATA	254	I2C2_CLK
255	GND	256	GND
257	CPU1_DBGACK	258	CPU1_DBGREQ
259	CPU1_RTCK	260	CPU1_TDO
261	CPU1_TDI	262	GND
263	AMBA_CON7	264	AMBA_CON6
265	AMBA_CON5	266	AMBA_CON4
267	AMBA_CON3	268	AMBA_CON2
269	AMBA_CON1	270	AMBA_CON0
271	IORSTn	272	nRESET_FPGA
273	NIRQ	274	NFIQ
275	GND	276	+5V
277	GND	278	+5V
279	GND	280	+5V
281	GND	282	+5V
283	GND	284	+5V
285	GND	286	+5V
287	GND	288	No Connect
289	GND	290	+3.3V
291	GND	292	+3.3V
293	GND	294	+3.3V
295	GND	296	+3.3V
297	GND	298	+3.3V
299	GND	300	+3.3V

2.4.15 AMBA Expansion Connector B

The Slot is provided to extend design IO functions for AMBA expansion. For FPGA pin assignment information, please refer to Appendix A.1 and A.4.

J32

Pin	Name	Pin	Name
1	AMBA_CON9	2	AMBA_CON8
3	AMBA_CON11	4	AMBA_CON10
5	AMBA_CON13	6	AMBA_CON12
7	AMBA_CON15	8	AMBA_CON14
9	GND	10	GND
11	RDATA_S37	12	RDATA_S36
13	RDATA_S35	14	RDATA_S34
15	RDATA_S33	16	RDATA_S32
17	RDATA_S31	18	RDATA_S30
19	RDATA_S29	20	RDATA_S28
21	RDATA_S27	22	RDATA_S26
23	RDATA_S25	24	RDATA_S24
25	RDATA_S23	26	RDATA_S22
27	RDATA_S21	28	RDATA_S20
29	RDATA_S19	30	RDATA_S18
31	RDATA_S17	32	RDATA_S16
33	RDATA_S15	34	RDATA_S14
35	RDATA_S13	36	RDATA_S12
37	RDATA_S11	38	RDATA_S10
39	RDATA_S9	40	RDATA_S8
41	RDATA_S7	42	RDATA_S6
43	RDATA_S5	44	RDATA_S4
45	RDATA_S3	46	RDATA_S2
47	RDATA_S1	48	RDATA_S0
49	BVALID_S	50	BREADY_S
51	GND	52	GND
53	ARADDR_S22	54	ARADDR_S21
55	ARADDR_S20	56	ARADDR_S19
57	ARADDR_S18	58	ARADDR_S17
59	ARADDR_S16	60	ARADDR_S15

61	ARADDR_S14	62	ARADDR_S13
63	ARADDR_S12	64	ARADDR_S11
65	ARADDR_S10	66	ARADDR_S9
67	ARADDR_S8	68	ARADDR_S7
69	ARADDR_S6	70	ARADDR_S5
71	ARADDR_S4	72	ARADDR_S3
73	ARADDR_S2	74	ARADDR_S1
75	ARADDR_S0	76	AWID_S8
77	AWID_S7	78	AWID_S6
79	AWID_S5	80	AWID_S4
81	AWID_S3	82	AWID_S2
83	AWID_S1	84	AWID_S0
85	AWPROT_S2	86	AWPROT_S1
87	AWPROT_S0	88	AWLOCK_S1
89	AWLOCK_S0	90	AWSIZE_S2
91	AWSIZE_S1	92	AWSIZE_S0
93	GND	94	GND
95	MMU_INT	96	MPG2_INT
97	M200_INT	98	SD_INT
99	DDR2_INT	100	MBOX1_INT
101	MBOX0_INT	102	CLCD_INT
103	VIP_INT	104	NFC_INT
105	HDMA1_INT	106	HDMA0_INT
107	GPIO_INT	108	OTG2_INT
109	OTG1_INT	110	OTG0_INT
111	I2S_INT	112	I2C2_INT
113	I2C1_INT	114	I2C0_INT
115	SPI1_INT	116	SPI0_INT
117	UART2_INT	118	UART1_INT
119	UART0_INT	120	RTC_INT
121	PWM3_INT	122	PWM2_INT
123	PWM1_INT	124	PWM0_INT
125	TIMER2_INT	126	TIMER1_INT
127	TIMER0_INT	128	MAC1_INT
129	MAC0_INT	130	No Connect
131	No Connect	132	GND
133	GND	134	GND
135	RDATA_M63	136	RDATA_M62
137	RDATA_M61	138	RDATA_M60
139	RDATA_M59	140	RDATA_M58
141	RDATA_M57	142	RDATA_M56
143	RDATA_M55	144	RDATA_M54

145	RDATA_M53	146	RDATA_M52
147	RDATA_M51	148	RDATA_M50
149	RDATA_M49	150	RDATA_M48
151	RDATA_M47	152	RDATA_M46
153	RDATA_M45	154	RDATA_M44
155	RDATA_M43	156	RDATA_M42
157	RDATA_M41	158	RDATA_M40
159	AWADDR_S15	160	AWADDR_S14
161	AWADDR_S13	162	AWADDR_S12
163	AWADDR_S11	164	AWADDR_S10
165	AWADDR_S9	166	AWADDR_S8
167	AWADDR_S7	168	AWADDR_S6
169	AWADDR_S5	170	AWADDR_S4
171	AWADDR_S3	172	AWADDR_S2
173	AWADDR_S1	174	AWADDR_S0
175	GND	176	GND
177	AWCACHE_S3	178	AWCACHE_S2
179	AWCACHE_S1	180	AWCACHE_S0
181	AWBURST_S1	182	AWBURST_S0
183	AWLEN_S3	184	AWLEN_S2
185	AWLEN_S1	186	AWLEN_S0
187	AWREADY_S	188	AWVALID_S
189	RRESP_S1	190	RRESP_S0
191	RLAST_S	192	ARID_S8
193	ARID_S7	194	ARID_S6
195	ARID_S5	196	ARID_S4
197	ARID_S3	198	ARID_S2
199	ARID_S1	200	ARID_S0
201	AWADDR_S31	202	AWADDR_S30
203	AWADDR_S29	204	AWADDR_S28
205	AWADDR_S27	206	AWADDR_S26
207	AWADDR_S25	208	AWADDR_S24
209	AWADDR_S23	210	AWADDR_S22
211	AWADDR_S21	212	AWADDR_S20
213	AWADDR_S19	214	AWADDR_S18
215	AWADDR_S17	216	AWADDR_S16
217	GND	218	GND
219	BREADY_M	220	WREADY_M
221	RVALID_M	222	RID_M4
223	RID_M3	224	RID_M2
225	RID_M1	226	RID_M0
227	WSTRB_M7	228	WSTRB_M6

229	WSTRB_M5	230	WSTRB_M4
231	WSTRB_M3	232	WSTRB_M2
233	WSTRB_M1	234	WSTRB_M0
235	BRESP_M1	236	BRESP_M0
237	BVALID_M	238	RLAST_M
239	BID_M4	240	BID_M3
241	BID_M2	242	BID_M1
243	BID_M0	244	RRESP_M1
245	RRESP_M0	246	WID_M4
247	WID_M3	248	WID_M2
249	WID_M1	250	WID_M0
251	RREADY_M	252	WVALID_M
253	ARVALID_M	254	ARID_M4
255	ARID_M3	256	ARID_M2
257	ARID_M1	258	ARID_M0
259	GND	260	GND
261	RDATA_M39	262	RDATA_M38
263	RDATA_M37	264	RDATA_M36
265	RDATA_M35	266	RDATA_M34
267	RDATA_M33	268	RDATA_M32
269	RDATA_M31	270	RDATA_M30
271	RDATA_M29	272	RDATA_M28
273	RDATA_M27	274	RDATA_M26
275	RDATA_M25	276	RDATA_M24
277	RDATA_M23	278	RDATA_M22
279	RDATA_M21	280	RDATA_M20
281	RDATA_M19	282	RDATA_M18
283	RDATA_M17	284	RDATA_M16
285	RDATA_M15	286	RDATA_M14
287	RDATA_M13	288	RDATA_M12
289	RDATA_M11	290	RDATA_M10
291	RDATA_M9	292	RDATA_M8
293	RDATA_M7	294	RDATA_M6
295	RDATA_M5	296	RDATA_M4
297	RDATA_M3	298	RDATA_M2
299	RDATA_M1	300	RDATA_M0

2.4.16 AMBA Expansion Connector C

The Slot is provided to extend design IO functions for AMBA expansion. For FPGA pin assignment information, please refer to Appendix A.1 and A.4.

J33

Pin	Name	Pin	Name
1	AWADDR_M15	2	AWADDR_M16
3	AWADDR_M17	4	AWADDR_M18
5	AWADDR_M19	6	AWADDR_M20
7	AWADDR_M21	8	AWADDR_M22
9	AWADDR_M23	10	AWADDR_M24
11	AWADDR_M25	12	AWADDR_M26
13	AWADDR_M27	14	AWADDR_M28
15	AWADDR_M29	16	AWADDR_M30
17	AWADDR_M31	18	AWLEN_M1
19	AWLEN_M3	20	AWLEN_M0
21	AWPROT_M1	22	AWLEN_M2
23	AWSIZE_M0	24	AWPROT_M0
25	AWSIZE_M2	26	AWPROT_M2
27	AWREADY_M	28	AWSIZE_M1
29	ARPROT_M0	30	ARREADY_M
31	ARPROT_M2	32	WLAST_M
33	AWLOCK_M1	34	ARPROT_M1
35	AWBURST_M1	36	AWLOCK_M0
37	AWVALID_M	38	AWBURST_M0
39	AWADDR_M5	40	AWADDR_M6
41	AWADDR_M3	42	AWADDR_M4
43	AWADDR_M1	44	AWADDR_M2
45	GND	46	AWADDR_M0
47	No Connect	48	GND
49	No Connect	50	No Connect
51	LVDS2-	52	No Connect
53	LVDS2+	54	No Connect
55	No Connect	56	No Connect
57	LVDS3-	58	No Connect
59	LVDS3+	60	No Connect

61	No Connect	62	No Connect
63	No Connect	64	No Connect
65	AMBA_CON51	66	AMBA_CON50
67	AMBA_CON49	68	AMBA_CON48
69	AMBA_CON47	70	AMBA_CON46
71	AMBA_CON45	72	AMBA_CON44
73	AMBA_CON43	74	AMBA_CON42
75	GND	76	GND
77	No Connect	78	No Connect
79	No Connect	80	No Connect
81	AWID_M0	82	AWID_M1
83	AWID_M2	84	AWID_M3
85	AWID_M4	86	ARBURST_M0
87	ARBURST_M1	88	ARLEN_M0
89	ARLEN_M1	90	ARLEN_M2
91	ARLEN_M3	92	ARSIZE_M0
93	ARSIZE_M1	94	ARSIZE_M2
95	ARLOCK_M0	96	ARLOCK_M1
97	WDATA_M0	98	WDATA_M1
99	WDATA_M2	100	WDATA_M3
101	WDATA_M4	102	WDATA_M5
103	WDATA_M6	104	WDATA_M7
105	WDATA_M8	106	WDATA_M9
107	WDATA_M10	108	WDATA_M11
109	WDATA_M12	110	WDATA_M13
111	WDATA_M14	112	WDATA_M15
113	WDATA_M16	114	WDATA_M17
115	WDATA_M18	116	WDATA_M19
117	WDATA_M20	118	WDATA_M21
119	WDATA_M22	120	WDATA_M23
121	WDATA_M24	122	WDATA_M25
123	WDATA_M26	124	WDATA_M27
125	WDATA_M28	126	WDATA_M29
127	WDATA_M30	128	WDATA_M31
129	WDATA_M32	130	WDATA_M33
131	WDATA_M34	132	WDATA_M35
133	WDATA_M36	134	WDATA_M37
135	WDATA_M38	136	WDATA_M39
137	WDATA_M40	138	WDATA_M41
139	WDATA_M42	140	WDATA_M43
141	WDATA_M44	142	WDATA_M45
143	WDATA_M46	144	WDATA_M47

145	WDATA_M48	146	WDATA_M49
147	WDATA_M50	148	WDATA_M51
149	WDATA_M52	150	WDATA_M53
151	WDATA_M54	152	WDATA_M55
153	WDATA_M56	154	WDATA_M57
155	WDATA_M58	156	WDATA_M59
157	WDATA_M60	158	WDATA_M61
159	WDATA_M62	160	WDATA_M63
161	GND	162	GND
163	AWADDR_M14	164	AWADDR_M13
165	AWADDR_M12	166	AWADDR_M11
167	AWADDR_M10	168	AWADDR_M9
169	AWADDR_M8	170	AWADDR_M7
171	ARADDR_M31	172	ARADDR_M30
173	ARADDR_M29	174	ARADDR_M28
175	ARADDR_M27	176	ARADDR_M26
177	ARADDR_M25	178	ARADDR_M24
179	ARADDR_M23	180	ARADDR_M22
181	ARADDR_M21	182	ARADDR_M20
183	ARADDR_M19	184	ARADDR_M18
185	ARADDR_M17	186	ARADDR_M16
187	ARADDR_M15	188	ARADDR_M14
189	ARADDR_M13	190	ARADDR_M12
191	ARADDR_M11	192	ARADDR_M10
193	ARADDR_M9	194	ARADDR_M8
195	ARADDR_M7	196	ARADDR_M6
197	ARADDR_M5	198	ARADDR_M4
199	ARADDR_M3	200	ARADDR_M2
201	ARADDR_M1	202	ARADDR_M0
203	ARCACHE_M3	204	ARCACHE_M2
205	ARCACHE_M1	206	ARCACHE_M0
207	WLAST_S	208	No Connect
209	AWCACHE_M3	210	AWCACHE_M2
211	AWCACHE_M1	212	AWCACHE_M0
213	GND	214	GND
215	RXD1_FPGA	216	TXD1_FPGA
217	GND	218	GND
219	SPI1_MISO	220	SPI1_MOSI
221	SPI1_SCSn1	222	SPI1_SCK
223	GND	224	GND
225	No Connect	226	No Connect
227	No Connect	228	No Connect

229	No Connect	230	No Connect
231	AMBA_CON41	232	AMBA_CON40
233	AMBA_CON39	234	AMBA_CON38
235	AMBA_CON37	236	AMBA_CON36
237	AMBA_CON35	238	AMBA_CON34
239	AMBA_CON33	240	AMBA_CON32
241	AMBA_CON31	242	AMBA_CON30
243	AMBA_CON29	244	AMBA_CON28
245	AMBA_CON27	246	AMBA_CON26
247	AMBA_CON25	248	AMBA_CON24
249	AMBA_CON23	250	AMBA_CON22
251	AMBA_CON21	252	AMBA_CON20
253	AMBA_CON19	254	AMBA_CON18
255	AMBA_CON17	256	AMBA_CON16
257	GND	258	GND
259	No Connect	260	No Connect
261	No Connect	262	No Connect
263	No Connect	264	No Connect
265	No Connect	266	No Connect
267	No Connect	268	No Connect
269	+5V	270	GND
271	+5V	272	GND
273	+5V	274	GND
275	+5V	276	GND
277	+5V	278	GND
279	No Connect	280	GND
281	+3.3V	282	GND
283	+3.3V	284	GND
285	+3.3V	286	GND
287	+3.3V	288	GND
289	+3.3V	290	GND
291	No Connect	292	GND
293	+12V	294	GND
295	+12V	296	GND
297	+12V	298	GND
299	+12V	300	GND

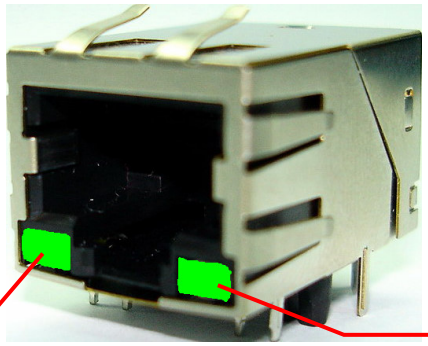
2.5 LED Display

LED displays are to show board's status.

Table 2-4 LED Display List

Location	Description
D1	L6021 3V3P Logic Power OK
D3	L6021 1VP CORE Power OK
D5	5VP Power OK for L6021
D6	1V8P DDR2 IO Power OK for L6021
D7	3V3P AMBA Power OK for L6021
D9	3V3P Standy by Power OK
D11	3V3 Logic Power OK for L6021
D13~D20	GPIO Control LED
D22	FPGA 1VP CORE Power OK
D23	FPGA 3V3P AUX Power OK
D24	FPGA IO Power OK
D25	FPGA AMBA IO Power OK
D26	FPGA 1.8V DDR2 IO Power OK
D27	FPGA Expansion IO Power OK
D28	FPGA PROM 1.8V Power OK
D29	FPGA Image load Done
D44	UART TXD0 Active
D45	UART RXD0 Active
D46	UART TXD1 Active
D47	UART RXD1 Active
D49	Bluetooth LED0
D50	Bluetooth LED1
D51	SD/MMC/SDIO card Power OK at port 0
D52	SD/MMC/SDIO card Power OK at port 1
D53	12VP Power OK

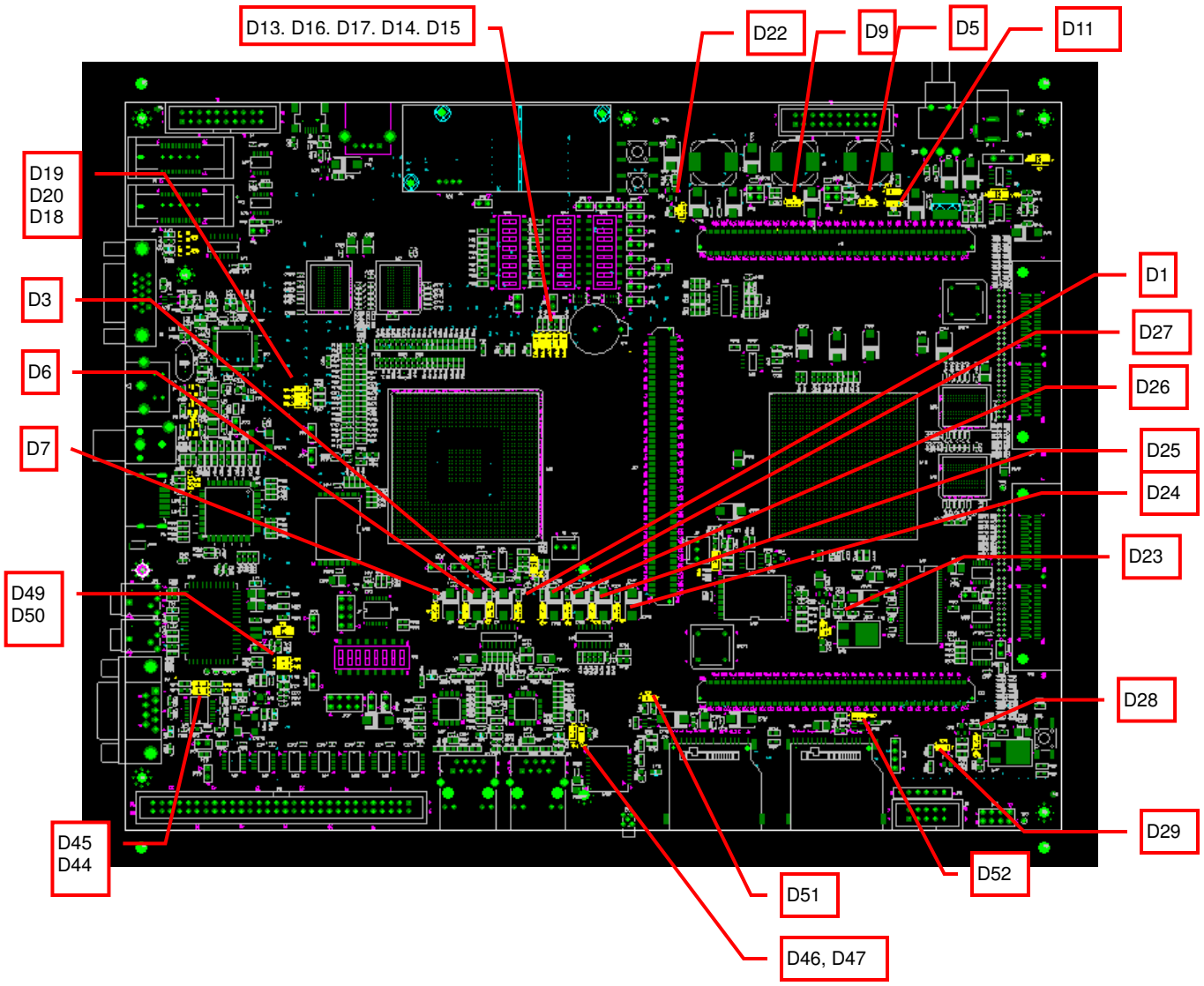
LED on RJ45 (location at J23 and J24)



Light On: MAC LINK
Blinking: Tx/Rx Active

Light On: Full Duplex
Blinking: Half Duplex Collision

Fig 2-4 LED Location



Chapter 3

Hardware Description

This chapter describes hardware of MDK-3D EVB. It contains the following sections:

- Power
- Reset
- Clock
- Memory
- Peripheral
- FPGA

3.1 Power

The power for entire MDK-3D EVB Development Board is provided by an external 12V power adapter. Use different regulators to provide power to different components. Following is the power scheme of MDK-3D EVB.

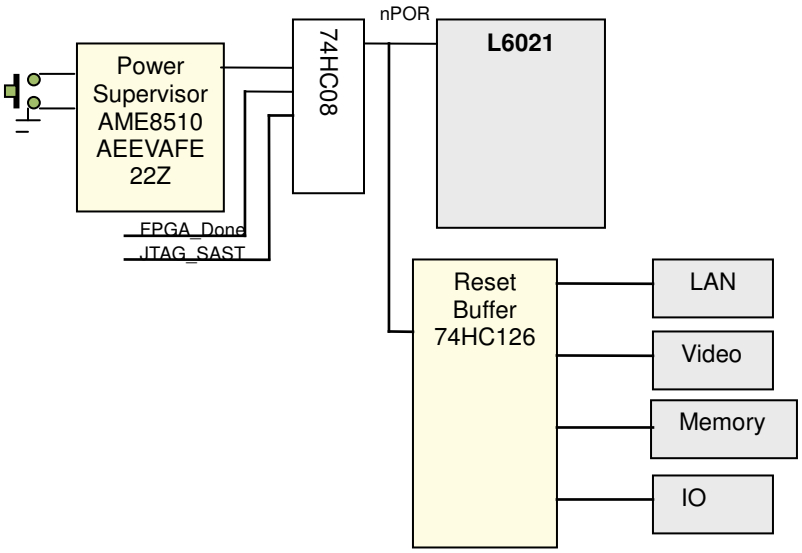
Power		
Device/Connector	**Voltage Requirement**	**Description**
Switching power adapter	Provide 12V	
L6021 Chip	Core/USB/RTC:1.0V IO/USB/RTC: 3.3V DDR2: 1.8V USB: 2.5V DDR2: 0.9V	
DDR2	1.8V/0.9V	
NOR Flash/NAND flash/SRAM	3.3V	
MAC PHY	3.3V	
ADC controller	3.3V	
RS232 Transceiver	3.3V	
FPGA	3.3V/2.5V/1.8V/1.0V/0.9V	
LCD display	5V/3.3V	
Audio/FM tuner	3.3V	
3-axis accelerometer	3.3V	
SD/MMC socket	3.3V	
USB port	5V	
TV encoder/VGA	5V/3.3V/2.5V/1.8V	
TFT LCD	3.3V	
HDMI	5V/3.3V/1.8V	
Camera module	3.3/2.5V/1.8V	
Bluetooth module	5V	
Battery	Provide 3V	

3.2 Reset

There are four sources for reset signal

1. Power on reset to AME8510AEEVAFE22Z and reset output
2. Tact SW to AME8510AEEVAFE22Z and reset output.
3. EJTAG_RSTn from ICE to 74HC08 input.
4. FPGA_Done from FPGA to 74HC08 input.

The reset signal will provide L6021 ASIC reset and different components through 74HC126 buffer.
Press tact SW to generate a manual reset signal to whole system when power is on.
Below is the reset scheme of MDK-3D.



3.3 Clock

All clock sources for devices are listed in the following table.

Clock		
Device	**Clock Speed**	**Description**
L6021	66MHz (OSC)	AMBA
	54MHz (OSC)	LCD controller
	32MHz (OSC)	PLL0~2
	12MHz (OSC)	USB2.0 OTG PHY0~2
	50MHz (OSC)	SD/MMC/SDIO
	32.768KHz (OSC)	RTC like
	88.5MHz (OSC)	UART
	16.9344MHz (OSC)	Audio
LAN PHY	25MHz (Crystal x2)	
FM tuner	32.768KHz (OSC)	
TV encoder	12MHz(Crystal)	
Camera	27MHz (OSC)	VIP
FPGA	OSC can	

3.4 Memory

The MDK-3D EVB supports two 64M bytes Numonyx JS28F512M29EW NOR type boot sector Flash. A jumper can set NOR Flash in 8bit or 16bit mode. Another jumper can set NOR Flash in write protection. NOR flash signals are also connected to a 2.54mm 2x25 pins header for other applications.
The MDK-3D EVB supports two Winbond W971GG6JB-25 64Mbx16 DDR2-800. The DDR2 SDRAM data bus is 32bit wide.
The MDK-3D EVB supports one Samsung K9K8G08U0B-PCB0 1Gx8 bits NAND Flash memory. It can be replaced by any 8bit data bus NAND Flash for different memory size requirements.

3.5 Peripherals

The following are the introduction of various peripherals.

3.5.1 UART

UART0 is connected to channel 1 of ADI ADM3222 RS232 transceiver for DB9 port. Two LEDs show the TX and RX signals status.
UART1 is connected to Vastera FGPMMOSL3 GPS module or FPGA or AMBA expansion.
UART2 is connected to CC&C BM-382-V2 Bluetooth module.

3.5.2 Ethernet

L6021 provides two MII interface to IC+ IP101A Ethernet PHY. Use LanKom LJ-H41S1D-36-F RJ45 module which is integrated with X'FMR, impedance, resistor and high voltage capacitor to save PCB space.

3.5.3 SPI

SPI0(Controller0, CS0) controls Samsung LMS480KC02 4.8” TFT LCD module with touch panel.
SPI1(Controller0, CS1) controls AiT A8946 touch screen controller which supports 4-wire resistance touch panel.
SPI2(Controller1, CS0) controls MAXIM MAX1110CAP ADC controller which supports 8 channels ADC.
SPI3(Controller1, CS1) is connected to FPGA or AMBA expansion.

3.5.4 TV encoder

A Chrontel CH7026 TV encoder supports composite, S-video and VGA output ports.

3.5.5 SD/MMC/SDIO

Two Globemaster 1-081-400288 SD sockets support SD, MMC and SDIO card.

3.5.6 USB 2.0 OTG

The EVB provide one mini USB AB-type and one USB A-type receptacle connectors. Another USB port connect to Modulestek SWUR102G 802.11b/g WiFi module.
USB0 for WiFi module connection
USB1 for A-type host connector
USB2 for mini AB-type connector

3.5.7 HDMI

An ITE CAT6613 HDMI 1.3 transmitter supports one HDMI A-type output port.

3.5.8 Audio

L6021 can control MOSA MS6635 audio DAC via I^2C interface to have sound features in playback mode. MS6635 supports I^2S-bus data format. Sound data can communicate between L6021 and DAC via I^2S bus.
L6021 can receive I^2S-bus data from KHTEK AD1181 audio ADC.
The EVB provide two phone jacks to connect speaker and microphone.
L6021 can transfer I^2S-bus data via Bluetooth.

3.5.9 LCD

The EVB provides one HSD050IDW1-A30-R0 5” TFT LCD module with 800X480 display resolution and touch screen function. A 40-pins FPC connector connects to LCD module. Or, the EVB provides one Microtips MTF-T070ACSLP-LB 7” TFT LCD module with 800X480 display resolution and touch screen function. A 40-pins FPC connector connects to LCD module.

3.5.10 Camera

The EVB provides one Aptina MT9V125IA7XTC CMOS camera with 640X480 pixels resolution. L6021 supports CCIR656 format to camera.

3.5.11 FM radio tuner

L6021 can control a Silicon Labs Si4703 FM radio tuner via I^2C interface. An audio out phone jack is for antenna connection.

3.5.12 GPIO

The MDK-3D EVB provides two GPIO port, GPIO[7:0] and GPIO[15:8].

GPIO [7:0] are connected to LEDs for debug.

GPIO0: DEBUG or share with PLL0_CONFIG0 detection
GPIO1: DEBUG or share with PLL0_CONFIG1 detection
GPIO2: DEBUG or share with PLL0_CONFIG2 detection
GPIO3: DEBUG or share with PLL1_CONFIG0 detection
GPIO4: DEBUG or share with PLL1_CONFIG1 detection
GPIO5: DEBUG or share with PLL1_CONFIG2 detection
GPIO6: DEBUG
GPIO7: DEBUG

GPIO [15:8] are connected to switchs for debug.

GPIO8: DEBUG or share with PLL2_CONFIG0 detection
GPIO9: DEBUG or share with PLL2_CONFIG1 detection
GPIO10: DEBUG or share with PLL2_CONFIG2 detection
GPIO11: DEBUG or share with CLKEXT_CONFIG0 detection
GPIO12: DEBUG or share with CLKEXT_CONFIG1 detection
GPIO13: DEBUG
GPIO14: DEBUG
GPIO15: DEBUG

3.5.13 ADC

The MDK-3D EVB use a MAXIM MAX1110CAP ADC controller to provides eight AD channels which are connected to 2.54mm 2x4 pins header (J7,JP37) for debug.

3.5.14 PWM

PWM0 controls LCD backlight power.
PWM1~3 are connected to 2.54mm 2x4 pins header for debug.

3.5.15 Interrupt

INT0 is from AiT A8946 touch screen controller which detect pen touching.
INT1 is connected to ITE CAT6613 HDMI 1.3 transmitter for cable detection.
INT2 is connected to a FINTEK F75111R GPIO expander which detect push button switch on LCD board.
INT3 is from VTI CMA3000-D01 3-axis accelerometer which detect acceleration.
INT4 is from AiT A8946 touch screen controller which provide busy status
INT0~5 are also connected to FPGA for sharing.

3.5.16 Always power

Always power is powered for RTC like function. A REGPWR_ON signal can turn off VDD1~VDD12, VDD15~VDD19, Vref power of Leopard 6. At REGPWR_ON signal turning off status, only DDR2 devices and touch screen controller are powered on.

3.6 FPGA

The following are the introduction of various FPGA.

3.6.1 Xilink Vertex-5

The MDK-3D EVB provides one Xilinx Virtex-5 XC5VLX110FF1760 or XC5VLX2200FF1760 or XC5VL330FF1760 FPGA to connect to L6021 AMBA for developing IP easily. These AMBA signals also are connected to three expansion slots. XC5VLX110FF1760 or XC5VLX2200FF1760 only supports AHB bus connection. XC5VL330FF1760 supports AXI and AHB connection.

3.6.2 IO port, Download port and EJTAG

The MDK-3D EVB provides two download ports as below.
1. One 2.54mm 2x5 pins header for FPGA download.
2. One 2.54mm 1x6 pins header for customer download port.

For IO expansion, the MDK-3D EVB also provide two 100 pins SAMTEC QSS-050-01-L-D-RA-WT-LS1 IO expansion connector
The MDK-3D EVB also provides one 2.54mm 2x10 pins header for EJTAG ICE debug or IO ports applications.

3.6.3 SRAM

One 1MX16 bits Cypress CY7C1061AV33-10ZXC SRAM on board.

3.6.4 DDR2

Two Winbond W971GG6JB-25 64Mbx16 bits DDR2-800 SDRAM on board and can up to 512M Bytes total.

3.6.5 NAND Flash

One Samsung K9K8G08U0A-PCB0 1Gx8 bits NAND Flash memories on board and can up to 8G Bytes.

3.6.6 Battery

A 3V CR-1220 Battery is powered for encryption key.

Appendix A

FPGA Pin Assignment

This Appendix provides FPGA pin assignment for all devices and connectors.

A.1 AMBA Pin Assignment on FPGA

These signals are connected to J31, J32 and J33, please refer to section 2.4.16, 2.4.17 and 2.4.18.

TableA.1.1 AXI Master

Name	Pin Location on FPGA	Name	Pin Location on FPGA
EXTRESET_N	R15	CLKEXTOUT	M14
AWADDR_M31	AV33	AWADDR_M30	AC35
AWADDR_M29	AV34	AWADDR_M28	AB36
AWADDR_M27	AV31	AWADDR_M26	AC36
AWADDR_M25	AU31	AWADDR_M24	AD35
AWADDR_M23	AT32	AWADDR_M22	AD36
AWADDR_M21	AT31	AWADDR_M20	AD37
AWADDR_M19	AP31	AWADDR_M18	AE37
AWADDR_M17	AN31	AWADDR_M16	AD38
AWADDR_M15	AR32	AWADDR_M14	AP37
AWADDR_M13	AN40	AWADDR_M12	AG36
AWADDR_M11	AF37	AWADDR_M10	AH35
AWADDR_M9	AG37	AWADDR_M8	AG34
AWADDR_M7	AG38	AWADDR_M6	AN33
AWADDR_M5	AJ31	AWADDR_M4	AP33
AWADDR_M3	AH31	AWADDR_M2	AR33
AWADDR_M1	AG32	AWADDR_M0	AP32
AWVALID_M	AV35	AWREADY_M	AT34
AWLEN_M3	AU33	AWLEN_M2	AM31
AWLEN_M1	AC34	AWLEN_M0	AB34
AWSIZE_M2	AR35	AWSIZE_M1	AL32
AWSIZE_M0	AR34	AWBURST_M1	AV36
AWBURST_M0	AM33	AWLOCK_M1	AU36
AWLOCK_M0	AK33	AWCACHE_M3	AB32
AWCACHE_M2	AR40	AWCACHE_M1	AB33
AWCACHE_M0	AP40	AWPROT_M2	AM32
AWPROT_M1	AU32	AWPROT_M0	AL31

AWID_M4	AD11	AWID_M3	AU42
AWID_M2	AC11	AWID_M1	AV41
AWID_M0	AB11	ARADDR_M31	AH34
ARADDR_M30	AF39	ARADDR_M29	AF36
ARADDR_M28	AE38	ARADDR_M27	AF35
ARADDR_M26	AE39	ARADDR_M25	AF34
ARADDR_M24	AK34	ARADDR_M23	AE35
ARADDR_M22	AL34	ARADDR_M21	AT36
ARADDR_M20	AL35	ARADDR_M19	AR37
ARADDR_M18	AL36	ARADDR_M17	AR38
ARADDR_M16	AK35	ARADDR_M15	AT37
ARADDR_M14	AJ35	ARADDR_M13	AU37
ARADDR_M12	AJ36	ARADDR_M11	AU38
ARADDR_M10	AH36	ARADDR_M9	AV38
ARADDR_M8	AM34	ARADDR_M7	AV39
ARADDR_M6	AN34	ARADDR_M5	AE34
ARADDR_M4	AN35	ARADDR_M3	AE33
ARADDR_M2	AM36	ARADDR_M1	AE32
ARADDR_M0	AN36	ARREADY_M	AK32
ARVALID_M	AH9	ARLEN_M3	AC9
ARLEN_M2	AT42	ARLEN_M1	AC10
ARLEN_M0	AT41	ARSIZE_M2	AP41
ARSIZE_M1	AB8	ARSIZE_M0	AR42
ARBURST_M1	AD10	ARBURST_M0	AU41
ARLOCK_M1	AP42	ARLOCK_M0	AB9
ARCACHE_M3	AD33	ARCACHE_M2	AP35
ARCACHE_M1	AD32	ARCACHE_M0	AP36
ARPROT_M2	AT35	ARPROT_M1	AJ33
ARPROT_M0	AU34	ARID_M4	AP26
ARID_M3	AJ8	ARID_M2	AR27
ARID_M1	AH10	ARID_M0	AN19
WLAST_M	AJ32	WDATA_M63	AB41
WDATA_M62	AN5	WDATA_M61	AB42
WDATA_M60	AM6	WDATA_M59	AC41
WDATA_M58	AR4	WDATA_M57	AD42
WDATA_M56	AR3	WDATA_M55	AE42
WDATA_M54	AM4	WDATA_M53	AD41
WDATA_M52	AN4	WDATA_M51	AF41
WDATA_M50	AN3	WDATA_M49	AF42
WDATA_M48	AP3	WDATA_M47	AF40
WDATA_M46	AL4	WDATA_M45	AG41
WDATA_M44	AK5	WDATA_M43	AG42

WDATA_M42	AL5	WDATA_M41	AH41
WDATA_M40	AL6	WDATA_M39	AJ42
WDATA_M38	AH5	WDATA_M37	AJ41
WDATA_M36	AJ6	WDATA_M35	AH40
WDATA_M34	AK4	WDATA_M33	AJ40
WDATA_M32	AJ5	WDATA_M31	AB37
WDATA_M30	AG4	WDATA_M29	AB38
WDATA_M28	AH4	WDATA_M27	AB39
WDATA_M26	AH6	WDATA_M25	AC38
WDATA_M24	AG6	WDATA_M23	AE40
WDATA_M22	AF5	WDATA_M21	AD40
WDATA_M20	AF6	WDATA_M19	AC40
WDATA_M18	AF4	WDATA_M17	AC39
WDATA_M16	AE4	WDATA_M15	AK40
WDATA_M14	AD8	WDATA_M13	AL40
WDATA_M12	AD7	WDATA_M11	AL41
WDATA_M10	AE7	WDATA_M9	AK42
WDATA_M8	AD6	WDATA_M7	AL42
WDATA_M6	AE5	WDATA_M5	AM42
WDATA_M4	AD5	WDATA_M3	AM41
WDATA_M2	AB7	WDATA_M1	AN41
WDATA_M0	AC8	WVALID_M	AP17
WREADY_M	F5	WSTRB_M7	AK12
WSTRB_M6	J5	WSTRB_M5	AF11
WSTRB_M4	AL26	WSTRB_M3	AE10
WSTRB_M2	AM26	WSTRB_M1	AE9
WSTRB_M0	AK18	WID_M4	AN26
WID_M3	AG8	WID_M2	AN25
WID_M1	AJ7	WID_M0	AN18
RDATA_M63	AT4	RDATA_M62	AJ16
RDATA_M61	AT5	RDATA_M60	AH29
RDATA_M59	AT6	RDATA_M58	AH30
RDATA_M57	AV3	RDATA_M56	AJ15
RDATA_M55	AU3	RDATA_M54	AH16
RDATA_M53	AB6	RDATA_M52	AV6
RDATA_M51	AC6	RDATA_M50	AU7
RDATA_M49	AC4	RDATA_M48	AU8
RDATA_M47	AC5	RDATA_M46	AV8
RDATA_M45	AC3	RDATA_M44	AT7
RDATA_M43	AD3	RDATA_M42	AU6
RDATA_M41	AB3	RDATA_M40	AR7
RDATA_M39	AU11	RDATA_M38	AP18

RDATA_M37	AT10	RDATA_M36	AR28
RDATA_M35	AT11	RDATA_M34	AR29
RDATA_M33	AR9	RDATA_M32	AR15
RDATA_M31	AR10	RDATA_M30	AP15
RDATA_M29	AR12	RDATA_M28	AR13
RDATA_M27	AT12	RDATA_M26	AR14
RDATA_M25	AP11	RDATA_M24	AT30
RDATA_M23	AP12	RDATA_M22	AR30
RDATA_M21	AN9	RDATA_M20	AP16
RDATA_M19	AP8	RDATA_M18	AR17
RDATA_M17	AM9	RDATA_M16	AU29
RDATA_M15	AN10	RDATA_M14	AT29
RDATA_M13	AN11	RDATA_M12	AT14
RDATA_M11	AP10	RDATA_M10	AT15
RDATA_M9	AM12	RDATA_M8	AL25
RDATA_M7	AM11	RDATA_M6	AM24
RDATA_M5	AL11	RDATA_M4	AK19
RDATA_M3	AL12	RDATA_M2	AJ18
RDATA_M1	AK10	RDATA_M0	AJ25
RVALID_M	AJ10	RREADY_M	AK7
RID_M4	E5	RID_M3	AJ11
RID_M2	G7	RID_M1	AJ12
RID_M0	H6	RRESP_M1	AM17
RRESP_M0	AH8	RLAST_M	AP28
BREADY_M	AL10	BVALID_M	AF10
BRESP_M1	AE8	BRESP_M0	AL17
BID_M4	AF9	BID_M3	AP27
BID_M2	AG7	BID_M1	AM18
BID_M0	AF7		

TableA.1.2 AXI Slave

Name	Pin Location on FPGA	Name	Pin Location on FPGA
AWADDR_S31	AM8	AWADDR_S30	V10
AWADDR_S29	AR5	AWADDR_S28	AL30
AWADDR_S27	AP5	AWADDR_S26	AL29
AWADDR_S25	AP7	AWADDR_S24	AK15
AWADDR_S23	AP6	AWADDR_S22	AK14
AWADDR_S21	AV5	AWADDR_S20	AJ30
AWADDR_S19	AV4	AWADDR_S18	AK30
AWADDR_S17	AU4	AWADDR_S16	AJ17
AWADDR_S15	AB4	AWADDR_S14	AR8
AWADDR_S13	AD2	AWADDR_S12	AU9
AWADDR_S11	AE3	AWADDR_S10	AT9
AWADDR_S9	AB2	AWADDR_S8	AV10
AWADDR_S7	AB1	AWADDR_S6	AV9
AWADDR_S5	AC1	AWADDR_S4	AU13
AWADDR_S3	AD1	AWADDR_S2	AU12
AWADDR_S1	AE2	AWADDR_S0	AV11
AWVALID_S	V8	AWREADY_S	AK8
AWLEN_S3	AH11	AWLEN_S2	AL24
AWLEN_S1	AG11	AWLEN_S0	AK25
AWSIZE_S2	AU2	AWSIZE_S1	L7
AWSIZE_S0	AU1	AWBURST_S1	AF12
AWBURST_S0	AM19	AWLOCK_S1	AT2
AWLOCK_S0	M6	AWCACHE_S3	AG9
AWCACHE_S2	AK24	AWCACHE_S1	AG12
AWCACHE_S0	AL19		
AWPROT_S2	J6	AWPROT_S1	AT1
AWPROT_S0	M7	AWID_S8	AA5
AWID_S7	H5	AWID_S6	AR2
AWID_S5	J7	AWID_S4	AP2
AWID_S3	K7	AWID_S2	AP1
AWID_S1	K5	AWID_S0	AN1
ARADDR_S31	M32	ARADDR_S30	M36
ARADDR_S29	M33	ARADDR_S28	N35
ARADDR_S27	M34	ARADDR_S26	P35
ARADDR_S25	N34	ARADDR_S24	R34
ARADDR_S23	N33	ARADDR_S22	H4
ARADDR_S21	U3	ARADDR_S20	J3
ARADDR_S19	U2	ARADDR_S18	H3
ARADDR_S17	V3	ARADDR_S16	G3

ARADDR_S15	V4	ARADDR_S14	L5
ARADDR_S13	W2	ARADDR_S12	L4
ARADDR_S11	W3	ARADDR_S10	K3
ARADDR_S9	W1	ARADDR_S8	K4
ARADDR_S7	V1	ARADDR_S6	N5
ARADDR_S5	AA4	ARADDR_S4	P5
ARADDR_S3	Y4	ARADDR_S2	N4
ARADDR_S1	Y5	ARADDR_S0	M4
ARREADY_S	N31	ARVALID_S	N36
ARLEN_S3	L36	ARLEN_S2	H34
ARLEN_S1	P36	ARLEN_S0	P31
ARSIZE_S2	G33	ARSIZE_S1	L35
ARSIZE_S0	G34	ARBURST_S1	H31
ARBURST_S0	J36	ARLOCK_S1	H33
ARLOCK_S0	K35	ARCACHE_S3	G31
ARCACHE_S2	H35	ARCACHE_S1	G32
ARCACHE_S0	J35	ARPROT_S2	M37
ARPROT_S1	M31	ARPROT_S0	L37
ARID_S8	AH33	ARID_S7	AK9
ARID_S6	AG33	ARID_S5	AM7
ARID_S4	AF32	ARID_S3	AN6
ARID_S2	AF31	ARID_S1	AN8
ARID_S0	AG31	WLAST_S	AC33
WDATA_S63	H13	WDATA_S62	T31
WDATA_S61	G13	WDATA_S60	U31
WDATA_S59	H11	WDATA_S58	U32
WDATA_S57	W11	WDATA_S56	T32
WDATA_S55	W10	WDATA_S54	R32
WDATA_S53	AA11	WDATA_S52	R33
WDATA_S51	AA10	WDATA_S50	P32
WDATA_S49	AA40	WDATA_S48	J38
WDATA_S47	Y40	WDATA_S46	K38
WDATA_S45	W40	WDATA_S44	L39
WDATA_S43	P40	WDATA_S42	M38
WDATA_S41	N40	WDATA_S40	M39
WDATA_S39	N41	WDATA_S38	N39
WDATA_S37	M42	WDATA_S36	N38
WDATA_S35	M41	WDATA_S34	P38
WDATA_S33	L42	WDATA_S32	P37
WDATA_S31	L41	WDATA_S30	R37
WDATA_S29	L40	WDATA_S28	R38
WDATA_S27	K42	WDATA_S26	R39

WDATA_S25	J42	WDATA_S24	E40
WDATA_S23	J41	WDATA_S22	E39
WDATA_S21	H41	WDATA_S20	F40
WDATA_S19	G41	WDATA_S18	F39
WDATA_S17	F41	WDATA_S16	G39
WDATA_S15	G42	WDATA_S14	G38
WDATA_S13	F42	WDATA_S12	H39
WDATA_S11	AA41	WDATA_S10	H38
WDATA_S9	AA42	WDATA_S8	W37
WDATA_S7	Y42	WDATA_S6	W36
WDATA_S5	W42	WDATA_S4	W35
WDATA_S3	W41	WDATA_S2	Y35
WDATA_S1	V40	WDATA_S0	Y34
WVALID_S	AA34	WREADY_S	V41
WSTRB_S7	J27	WSTRB_S6	R40
WSTRB_S5	J26	WSTRB_S4	P41
WSTRB_S3	M19	WSTRB_S2	P42
WSTRB_S1	U38	WSTRB_S0	R42
WID_S8	U42	WID_S7	AA36
WID_S6	U41	WID_S5	AA35
WID_S4	T42	WID_S3	W38
WID_S2	T41	WID_S1	V39
WID_S0	T40	RDATA_S63	L12
RDATA_S62	P33	RDATA_S61	N11
RDATA_S60	L31	RDATA_S59	M11
RDATA_S58	L32	RDATA_S57	L9
RDATA_S56	J32	RDATA_S55	K10
RDATA_S54	K32	RDATA_S53	G36
RDATA_S52	J33	RDATA_S51	F36
RDATA_S50	K33	RDATA_S49	G37
RDATA_S48	K34	RDATA_S47	H36
RDATA_S46	L34	RDATA_S45	V36
RDATA_S44	E33	RDATA_S43	U36
RDATA_S42	E32	RDATA_S41	T36
RDATA_S40	F32	RDATA_S39	R35
RDATA_S38	F31	RDATA_S37	T6
RDATA_S36	J2	RDATA_S35	T5
RDATA_S34	J1	RDATA_S33	R5
RDATA_S32	G1	RDATA_S31	R4
RDATA_S30	H1	RDATA_S29	U4
RDATA_S28	L2	RDATA_S27	T4
RDATA_S26	M2	RDATA_S25	U6

RDATA_S24	K2	RDATA_S23	V5
RDATA_S22	L1	RDATA_S21	W7
RDATA_S20	M1	RDATA_S19	W8
RDATA_S18	N1	RDATA_S17	W5
RDATA_S16	M3	RDATA_S15	V6
RDATA_S14	N3	RDATA_S13	Y7
RDATA_S12	P3	RDATA_S11	W6
RDATA_S10	R3	RDATA_S9	AA7
RDATA_S8	P2	RDATA_S7	AA6
RDATA_S6	P1	RDATA_S5	Y8
RDATA_S4	R2	RDATA_S3	AA9
RDATA_S2	T2	RDATA_S1	Y10
RDATA_S0	U1	RVALID_S	U37
RREADY_S	AA37	RID_S8	V38
RID_S7	Y37	RID_S6	K39
RID_S5	Y38	RID_S4	K40
RID_S3	Y39	RID_S2	J40
RID_S1	AA39	RID_S0	H40
RRESP_S1	AL7	RRESP_S0	V11
RLAST_S	AL9	BREADY_S	T1
BVALID_S	Y9	BRESP_S1	J31
BRESP_S0	K37	BID_S8	U33
BID_S7	F34	BID_S6	T34
BID_S5	E34	BID_S4	T35
BID_S3	E35	BID_S2	U34
BID_S1	F35	BID_S0	J37

TableA.1.3 AHB

Name	Pin Location on FPGA	Name	Pin Location on FPGA
HADDR31	P13	HDATA31	J15
HADDR30	K13	HDATA30	G11
HADDR29	N14	HDATA29	H15
HADDR28	J13	HDATA28	F10
HADDR27	M29	HDATA27	L26
HADDR26	AU39	HDATA26	F11
HADDR25	N29	HDATA25	M26
HADDR24	P10	HDATA24	H9
HADDR23	P15	HDATA23	J16
HADDR22	L15	HDATA22	H10
HADDR21	N15	HDATA21	J17
HADDR20	L16	HDATA20	E10
HADDR19	P28	HDATA19	K24
HADDR18	N8	HDATA18	E9
HADDR17	N28	HDATA17	K25
HADDR16	V33	HDATA16	F9
HADDR15	R17	HDATA15	G16
HADDR14	H28	HDATA14	G9
HADDR13	P17	HDATA13	H16
HADDR12	L14	HDATA12	H8
HADDR11	P26	HDATA11	L24
HADDR10	G27	HDATA10	J8
HADDR9	P27	HDATA9	L25
HADDR8	L17	HDATA8	K8
HADDR7	N13	HDATA7	H14
HADDR6	N16	HDATA6	K9
HADDR5	M13	HDATA5	G14
HADDR4	M16	HDATA4	E7
HADDR3	R27	HDATA3	N24
HADDR2	M17	HDATA2	E8
HADDR1	R28	HDATA1	M24
HADDR0	L30	HDATA0	F7
HTRANS1	P30	HTRANS0	M18
HWRITE	G12	HREADY	L19
HSIZE1	P25	HSIZE0	F12
HRESP1	N25	HRESP0	E13
HLOCK	K19	HGRANT	P16
HSEL	K15	HBUSREQ	E12
HBURST2	K14	HBURST1	N30

HBURST0	T39		

A.2 FPGA IO Expansion Pin assignment

These signals are connected to J14, J27 and J29, please refer to section 2.4.11, 2.4.14, 2.4.15.

TableA.2.1

Name	Pin Location on FPGA	Name	Pin Location on FPGA
P1_1	AL27	P1_51	AW17
P1_2	AW23	P1_52	AV18
P1_3	AW22	P1_53	AV13
P1_4	AW27	P1_54	AW13
P1_5	AV28	P1_55	AW16
P1_6	AV24	P1_56	AV16
P1_7	AV23	P1_57	AU14
P1_8	AW26	P1_58	AV14
P1_9	AW25	P1_59	AW15
P1_10	AU23	P1_60	AV15
P1_11	AU22	P1_61	AY15
P1_12	AV21	P1_62	AY14
P1_13	AV20	P1_63	BA14
P1_14	AW21	P1_64	BB13
P1_15	AW20	P1_65	AY42
P1_16	AW18	P1_66	AW42
P1_17	AV19	P1_67	AW41
P1_18	AU17	P1_68	AW40
P1_19	AY40	P1_69	AW35
P1_20	BA41	P1_70	BB33
P1_21	BA42	P1_71	BA34
P1_22	BB41	P1_72	AY33
P1_23	BA40	P1_73	AW33
P1_24	BB38	P1_74	AW32
P1_25	BA39	P1_75	AY32
P1_26	AY38	P1_76	BA32
P1_27	AW37	P1_77	BB32
P1_28	AW38	P1_78	BB31
P1_29	AY39	P1_79	BA30
P1_30	BB37	P1_80	BA31

P1_31	BA37	P1_81	AY30
P1_32	AY37	P1_82	AW31
P1_33	AW36	P1_83	AW7
P1_34	BB36	P1_84	BA7
P1_35	BA36	P1_85	BB7
P1_36	AY35	P1_86	BB4
P1_37	BA5	P1_87	AP22
P1_38	BA4	P1_88	AR22
P1_39	AY4	P1_89	AT22
P1_40	AW5	P1_90	AU21
P1_41	AY5	P1_91	AM22
P1_42	BB3	P1_92	AL22
P1_43	BB2	P1_93	AT21
P1_44	AW3	P1_94	AT20
P1_45	AY3	P1_95	AN23
P1_46	BA2	P1_96	AM23
P1_47	BA1	P1_97	AN24
P1_48	AY2	P1_98	AP23
P1_49	AW2	P1_99	AM28
P1_50	AW1	P1_100	AR23

TableA.2.2

Name	**Pin Location on FPGA**	**Name**	**Pin Location on FPGA**
P1_101	L29	P1_151	C9
P1_102	AT39	P1_152	D12
P1_103	AR39	P1_153	D11
P1_104	F15	P1_154	A12
P1_105	N18	P1_155	B12
P1_106	N19	P1_156	C11
P1_107	G28	P1_157	B11
P1_108	G29	P1_158	D13
P1_109	R18	P1_159	C13
P1_110	P18	P1_160	F16
P1_111	K30	P1_161	D22
P1_112	J30	P1_162	D23
P1_113	K29	P1_163	D21
P1_114	K28	P1_164	D20
P1_115	M28	P1_165	F21
P1_116	L27	P1_166	E22

P1_117	H29	P1_167	E23
P1_118	H30	P1_168	F24
P1_119	F17	P1_169	E24
P1_120	E20	P1_170	E25
P1_121	F20	P1_171	F27
P1_122	D18	P1_172	F26
P1_123	E18	P1_173	F25
P1_124	E19	P1_174	E29
P1_125	F19	P1_175	E28
P1_126	D27	P1_176	F29
P1_127	D28	P1_177	D30
P1_128	F30	P1_178	E30
P1_129	M23	P1_179	F22
P1_130	N23	P1_180	H23
P1_131	P20	P1_181	G23
P1_132	N20	P1_182	J18
P1_133	P23	P1_183	H24
P1_134	P22	P1_184	G24
P1_135	P21	P1_185	K20
P1_136	N21	P1_186	J20
P1_137	L22	P1_187	H25
P1_138	N22	P1_188	J25
P1_139	M21	P1_189	L20
P1_140	K22	P1_190	L21
P1_141	K23	P1_191	G26
P1_142	J21	P1_192	H26
P1_143	H21	P1_193	AV29
P1_144	J22	P1_194	AW28
P1_145	J23	P1_195	AV26
P1_146	G21	P1_196	AU26
P1_147	H20	P1_197	AV30
P1_148	H19	P1_198	AW30
P1_149	G19	P1_199	N26
P1_150	G22	P1_200	AU24

Name	**Pin Location on FPGA**	**Name**	**Pin Location on FPGA**
LVDS2+	AT25	LVDS3+	AR18
LVDS2-	AT24	LVDS3-	AR19

A.3 FPGA Debug Port Pin assignment

These signals are connected to J13 if JP9 is ON, please refer to section 2.4.10.

TableA.3

Name	Pin Location on FPGA	Name	Pin Location on FPGA
FPGA_TRSTn/FPGA GPIO	V35	FPGA _TCK/FPGA GPIO	E38
FPGA _TDI/FPGA GPIO	F37	FPGA _RTCK/FPGA GPIO	E37
FPGA _TMS/FPGA GPIO	D37	FPGA _TDO/FPGA GPIO	V34

A.4 FPGA GPIO Pin assignment for AMBA Expansion connectors

These signals are connected to J31, J32 and J33, please refer to section 2.4.16, 2.4.17 and 2.4.18.

TableA.4

Name	Pin Location on FPGA	Name	Pin Location on FPGA
AMBA_CON0	D2	AMBA_CON1	B1
AMBA_CON2	D1	AMBA_CON3	C1
AMBA_CON4	B2	AMBA_CON5	C3
AMBA_CON6	A2	AMBA_CON7	B3
AMBA_CON8	Y3	AMBA_CON9	Y2
AMBA_CON10	AA2	AMBA_CON11	AA1
AMBA_CON12	E4	AMBA_CON13	E3
AMBA_CON14	F4	AMBA_CON15	G4
AMBA_CON16	BA26	AMBA_CON17	BA21
AMBA_CON18	BB26	AMBA_CON19	AY18
AMBA_CON20	BA24	AMBA_CON21	AY17
AMBA_CON22	BB23	AMBA_CON23	BA19
AMBA_CON24	AY24	AMBA_CON25	AY19
AMBA_CON26	AY25	AMBA_CON27	BA17
AMBA_CON28	AY23	AMBA_CON29	BB17
AMBA_CON30	AY22	AMBA_CON31	BB19
AMBA_CON32	AY20	AMBA_CON33	BB18
AMBA_CON34	BA20	AMBA_CON35	BB14
AMBA_CON36	BB22	AMBA_CON37	BA15
AMBA_CON38	BB21	AMBA_CON39	BA16

AMBA_CON40	BA22	AMBA_CON41	BB16
AMBA_CON42	AY29	AMBA_CON43	AY27
AMBA_CON44	BA29	AMBA_CON45	BB27
AMBA_CON46	BB28	AMBA_CON47	BA27
AMBA_CON48	BB29	AMBA_CON49	BA25
AMBA_CON50	AY28	AMBA_CON51	BB24

A.5 FPGA Control SRAM Pin assignment

TableA.5

Name	Pin Location on FPGA	Name	Pin Location on FPGA
SRAM_D0	AG39	SRAM_D1	AH39
SRAM_D2	AJ38	SRAM_D3	AK39
SRAM_D4	AK38	SRAM_D5	AK37
SRAM_D6	AJ37	SRAM_D7	AH38
SRAM_D8	AL39	SRAM_D9	AM39
SRAM_D10	AN39	SRAM_D11	AP38
SRAM_D12	AN38	SRAM_D13	AM38
SRAM_D14	AM37	SRAM_D15	AL37
SRAM_A0	AN13	SRAM_A1	AP13
SRAM_A2	AM27	SRAM_A3	K17
SRAM_A4	AN14	SRAM_A5	AN15
SRAM_A6	AN28	SRAM_A7	K18
SRAM_A8	AM14	SRAM_A9	AM13
SRAM_A10	AN29	SRAM_A11	AP30
SRAM_A12	AM16	SRAM_A13	AN16
SRAM_A14	J28	SRAM_A15	AM29
SRAM_A16	AK17	SRAM_A17	AL16
SRAM_A18	AK27	SRAM_A19	K27
SRAM_OEn	M12	SRAM_WEn	N10
SRAM_CEn	AN30	SRAM_LBn	P11
SRAM_UBn	P12		

A.6 FPGA Control NAND Flash Pin assignment

TableA.6

Name	Pin Location on FPGA	Name	Pin Location on FPGA
FN_FD0	AY12	FN_FD1	AY13
FN_FD2	BA11	FN_FD3	BB11
FN_FD4	BB12	FN_FD5	BA12
FN_FD6	AW12	FN_FD7	AW11
FN_FRDYn1	AY9	FN_FRDYn2	AY8
FN_FRDYn3	BA10	FN_FRDYn4	BB9
FN_FCEn1	AW10	FN_FCEn2	AY10
FN_FCEn3	BA9	FN_FCEn4	BB8
FN_FREn	AW8	FN_FCLE	AY7
FN_FALE	BA6	FN_FWEn	BB6
FN_FWP	AW6		

A.7 FPGA Control DDR2 SDRAM Pin assignment

TableA.7

Name	Pin Location on FPGA	Name	Pin Location on FPGA
DDR_DATA0	B14	DDR_DATA1	B13
DDR_DATA2	C15	DDR_DATA3	C14
DDR_DATA4	B16	DDR_DATA5	A15
DDR_DATA6	A14	DDR_DATA7	B18
DDR_DATA8	B17	DDR_DATA9	A16
DDR_DATA10	C19	DDR_DATA11	C18
DDR_DATA12	C26	DDR_DATA13	A24
DDR_DATA14	B23	DDR_DATA15	C25
DDR_DATA16	C24	DDR_DATA17	B24
DDR_DATA18	A27	DDR_DATA19	B28
DDR_DATA20	C29	DDR_DATA21	A26
DDR_DATA22	B27	DDR_DATA23	B29
DDR_DATA24	D31	DDR_DATA25	C31
DDR_DATA26	B31	DDR_DATA27	C30
DDR_DATA28	A31	DDR_DATA29	A32
DDR_DATA30	B32	DDR_DATA31	B33
DDR_ADDR0	C40	DDR_ADDR1	C39
DDR_ADDR2	B36	DDR_ADDR3	B37

DDR_ADDR4	A36	DDR_ADDR5	A37
DDR_ADDR6	C35	DDR_ADDR7	C36
DDR_ADDR8	A35	DDR_ADDR9	A34
DDR_ADDR10	B34	DDR_ADDR11	C34
DDR_ADDR12	A29	DDR_ADDR13	D33
DDR_ADDR14	D32	DDR_ADDR15	E42
DDR_DQS0	A20	DDR_DQS1	C21
DDR_DQS2	C23	DDR_DQS3	D35
DDR_DQSn0	B21	DDR_DQSn1	C20
DDR_DQSn2	B22	DDR_DQSn3	D36
DDR_CK	A21	DDR_CKn	A22
DDR_CSn	C41	DDR_CASn	B41
DDR_RASn	A41	DDR_WEn	B42
DDR_ODT	D41	DDR_CKE	D42
DDR_BA0	A40	DDR_BA1	A39
DDR_BA2	B39	DDR_DM0	C16
DDR_DM1	B26	DDR_DM2	C28
DDR_DM3	A30		

A.8 FPGA miscellaneous Pin assignment

TableA.8

Name	Pin Location on FPGA	Name	Pin Location on FPGA
NIRQ	F6	NFIQ	L10
MAC0_INT	U8	MAC1_INT	AL1
TIMER0_INT	T7	TIMER1_INT	AM1
TIMER2_INT	U7	PWM0_INT	AM2
PWM1_INT	R8	PWM2_INT	AM3
PWM3_INT	R7	RTC_INT	AJ1
UART0_INT	T9	UART1_INT	AK2
UART2_INT	R9	SPI0_INT	AK3
SPI1_INT	R10	I2C0_INT	AL2
I2C1_INT	T10	I2C2_INT	AG1
I2S_INT	P6	OTG0_INT	AH1
OTG1_INT	N6	OTG2_INT	AJ3
GPIO_INT	T37	HDMA0_INT	AJ2
HDMA1_INT	P7	NFC_INT	AH3
VIP_INT	M9	CLCD_INT	AG3
MBOX0_INT	M8	MBOX1_INT	AG2
DDR2_INT	N9	SD_INT	AF2
M200_INT	P8	MPG2_INT	AF1
MMU_INT	L6	nRESET_FPGA	L11
IORSTn	G6	EXT_INT0_FPGA	T11
EXT_INT1_FPGA	J10	EXT_INT2_FPGA	U11
EXT_INT3_FPGA	J12	EXT_INT4_FPGA	U9
EXT_INT5_FPGA	K12	I2C2_CLK	V9
I2C2_DATA	J11	SPI1_SCK	F1
SPI1_SCSn1	F2	SPI1_MOSI	G2
SPI1_MISO	E2	TXD1_FPGA	AV40
RXD1_FPGA	AT40	CLK0_FPGA	AK28
CLK1_FPGA	M27	CPU1_TDI	Y32
CPU1_TDO	AA32	CPU1_RTCK	W32
CPU1_DBGREQ	Y33	CPU1_DBGACK	W33

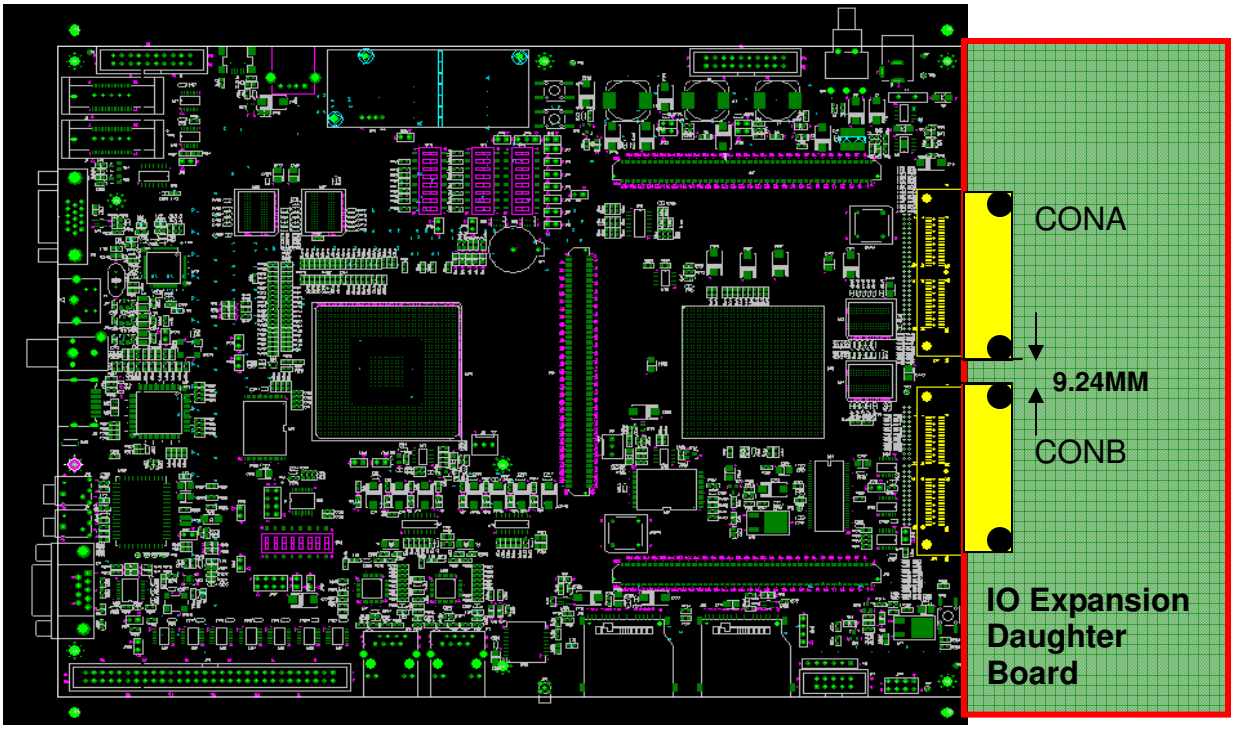
Appendix B
IO Expansion Board Details

This Appendix gives the mechanical dimension for IO Expansion Slot for user to develop application board.

B.1 Layout Dimension

The mechanical dimension of the expansion slots of the board is shown below. It contains the recommended dimension for making daughter board. CONA is matched with J27 of MDK-3D EVB and CONB is matched with J29 of MDK-3D EVB. Please refer to section 2.4.14 and 2.4.15 for the detail pin definition.

Recommend IO Expansion Daughter Board Layout Dimension :



Connector Information

Connector Vendor	Part Number	Connector Form factor
SAMTEC	QTS-050-01-L-D-RA-WT-LS1	Socket

SAMTEC , Inc., http://www.samtec.com/

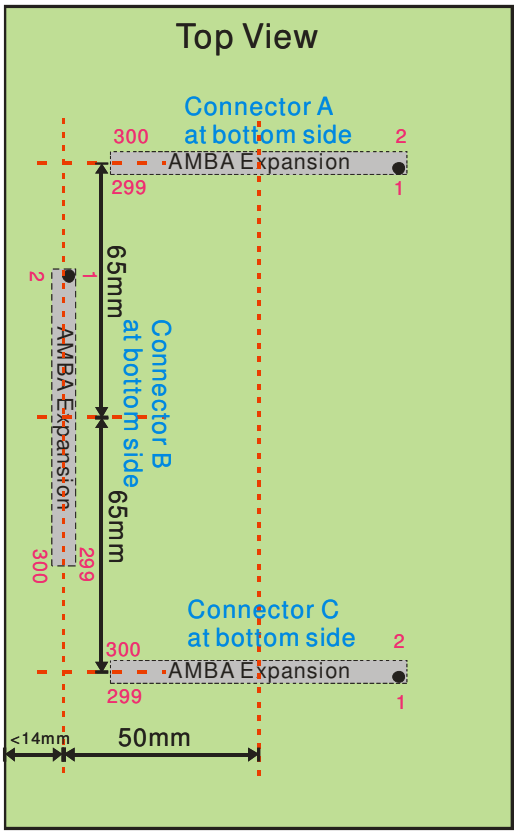
Appendix C

AMBA Expansion Board Details

This Appendix gives the mechanical dimension for AMBA Expansion Slot for user to develop application board.

C.1 Recommended Board Layout Dimensions

The mechanical dimension of the expansion slots of the board is shown below. It contains the recommended dimension for making daughter board. Connector A is matched with J31 of MDK-3D EVB, Connector B is matched with J32 of MDK-3D EVB and Connector C is matched with J33 of MDK-3D EVB. Please refer to section 2.4.16 , 2.4.17 and 2.4.18 for the detail pin definition. The following is the detail dimensions of board layout:



Connector Vendor	Part Number	Connector Form factor
SAMTEC	BSH-150-01-F-D-A	Socket

SAMTEC , Inc., http://www.samtec.com/

Appendix D

LCD-008 LCD board

This Appendix provides LCD-008 board features, Keypad, pin assignment for all devices and connectors.

E.1 Features

The following is the main features list of LCD-008 EVB

- One HANNSTAR HSD050IDW1-A30-R0 5" TFT LCD module with 800X480 display resolution and touch screen function
- One Aptina MT9V125IA7XTC CMOS camera with 640X480 pixels resolution
- One photo capture button for camera
- Ten functional buttons
- One FINTEK F75111R GPIO expander which detect push button switch
- One 2x30 header connector for main board connection
- 4 layers PCB
- PCB size: 83.5(W)X137.5(L)MM

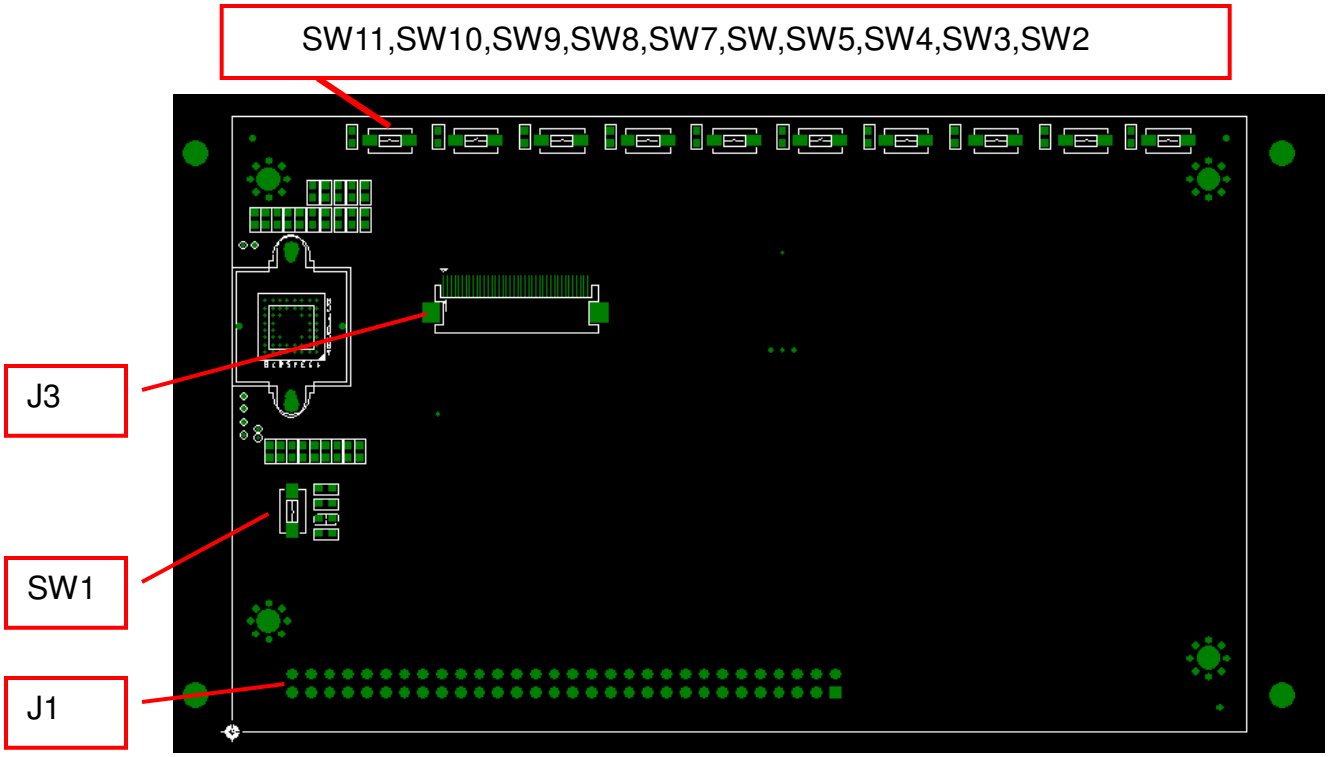
E.2 Keypad Definition

This section shows the location of all the keypads on the board, and describes the function of each keypad.

TableE.2.1 Keypad List

Location	Function
SW1	Low activity to GPIO11 of F75111R during Button Pushed (Camera)
SW2	Low activity to GPIO30 of F75111R during Button Pushed (Function)
SW3	Low activity to GPIO31 of F75111R during Button Pushed (Function)
SW4	Low activity to GPIO32 of F75111R during Button Pushed (Function)
SW5	Low activity to GPIO33 of F75111R during Button Pushed (Function)
SW6	Low activity to GPIO23 of F75111R during Button Pushed (Function)
SW7	Low activity to GPIO24 of F75111R during Button Pushed (Function)
SW8	Low activity to GPIO25 of F75111R during Button Pushed (Function)
SW9	Low activity to GPIO26 of F75111R during Button Pushed (Function)
SW10	Low activity to GPIO27 of F75111R during Button Pushed (Function)
SW11	Low activity to GPIO15 of F75111R during Button Pushed (Function)

Fig E-1 Keypad Location
Top side



E.3 Connectors

This section shows the location of all the connectors on the board, and describes the function of each connector.

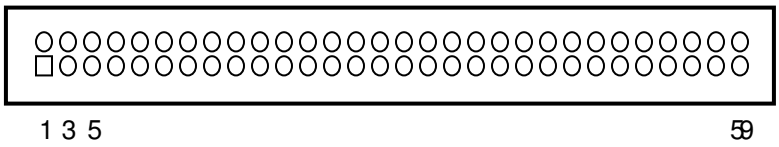
Table E.3.1 Connector List

Location	Function
J1	I/O Connector to MDK-3D
J3	LCD module connector

Fig E-2 Connectors Location
Bottom side

E.3.1 I/O Connector to MDK-3D

This connector is matched with J16 of MDK-3D EVB.



J1

Pin	Name	Pin	Name
1	DB0	2	LCD_CP
3	DB2	4	DB1
5	DB4	6	DB3
7	DB6	8	DB5
9	DG0	10	DB7
11	DG2	12	DG1
13	DG4	14	DG3
15	DG6	16	DG5
17	DR0	18	DG7
19	DR2	20	DR1
21	DR4	22	DR3
23	DR6	24	DR5
25	LCD_LP	26	DR7
27	LCD_AC	28	LCD_FP
29	LCD_POWER	30	LCDRSTn
31	PWM0	32	EXT_INT0_PEN
33	SPI0_SCSn1	34	SPI0_SCK
35	SPI0_SCSn0	36	SPI0_MOSI
37	EXT_INT4_TS_BZ	38	SPI0_MISO
39	I2C0_CLK	40	I2C0_DATA
41	VIP_D7	42	VIP_CLK
43	VIP_D6	44	VIP_D0
45	VIP_D5	46	VIP_D1
47	VIP_D4	48	VIP_D2
49	VIP_D3	50	EXT_INT2_CAM
51	GND	52	+3.3V
53	GND	54	+3.3V
55	GND	56	+3.3V_Standby
57	GND	58	+5V
59	GND	60	+5V

E.3.2 LCD Module Connector

Pin	Name
1	VLED-
2	VLED+
3	GND
4	+3.3V
5	R0
6	R1
7	R2
8	R3
9	R4
10	R5
11	R6
12	R7
13	G0
14	G1
15	G2
16	G3
17	G4
18	G5
19	G6
20	G7
21	B0
22	B1
23	B2
24	B3
25	B4
26	B5
27	B6
28	B7
29	DGND
30	DCLK
31	DISP
32	HSYNC
33	VSYNC
34	DE
35	NC
36	GND
37	X1
38	Y1
39	X2
40	Y2