

MX25U51245G

**1.8V, 512M-BIT [x 1/x 2/x 4]
CMOS MXSMIO[®] (SERIAL MULTI I/O)
FLASH MEMORY**

Key Features

- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
 - *Support DTR (Double Transfer Rate) Mode*
 - *8/16/32/64 byte Wrap-Around Read Mode*
-

Contents

1. FEATURES	5
2. GENERAL DESCRIPTION	7
Table 1. Read performance Comparison	7
3. PIN CONFIGURATIONS	8
Table 2. PIN DESCRIPTION	8
4. BLOCK DIAGRAM.....	9
5. MEMORY ORGANIZATION	10
6. DATA PROTECTION.....	11
6-1. Block lock protection	12
Table 3. Protected Area Sizes	12
6-2. Additional 8K-bit secured OTP	13
Table 4. 8K-bit Secured OTP Definition	13
7. DEVICE OPERATION	14
7-1. 256Mb Address Protocol.....	16
7-2. Quad Peripheral Interface (QPI) Read Mode	19
8. COMMAND SET	20
Table 5. Read/Write Array Commands.....	20
Table 6. Read/Write Array Commands (4 Byte Address Command Set)	21
Table 7. Register/Setting Commands.....	22
Table 8. ID/Security Commands.....	23
Table 9. Reset Commands	24
9. REGISTER DESCRIPTION.....	25
9-1. Status Register	25
9-2. Configuration Register	26
9-3. Security Register	28
Table 10. Security Register Definition	28
10. COMMAND DESCRIPTION	29
10-1. Write Enable (WREN).....	29
10-2. Write Disable (WRDI).....	30
10-3. Read Identification (RDID).....	31
10-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)	32
10-5. Read Electronic Manufacturer ID & Device ID (REMS).....	34
10-6. QPI ID Read (QPIID)	35
Table 11. ID Definitions	35
10-7. Read Status Register (RDSR)	36
10-8. Read Configuration Register (RDCR).....	37
10-9. Write Status Register (WRSR).....	40
Table 12. Protection Modes.....	41
10-10. Enter 4-byte mode (EN4B)	44
10-11. Exit 4-byte mode (EX4B)	44
10-12. Read Data Bytes (READ)	45
10-13. Read Data Bytes at Higher Speed (FAST_READ)	46

10-14. Dual Output Read Mode (DREAD)	47
10-15. 2 x I/O Read Mode (2READ)	48
10-16. Quad Read Mode (QREAD)	49
10-17. 4 x I/O Read Mode (4READ)	50
10-18. 4 x I/O Double Transfer Rate Read Mode (4DTRD)	52
10-19. Preamble Bit	54
10-20. 4 Byte Address Command Set	58
10-21. Performance Enhance Mode	63
10-22. Performance Enhance Mode Reset	68
10-23. Burst Read	70
10-24. Fast Boot	71
10-25. Sector Erase (SE)	74
10-26. Block Erase (BE32K)	75
10-27. Block Erase (BE)	76
10-28. Chip Erase (CE)	77
10-29. Page Program (PP)	78
10-30. 4 x I/O Page Program (4PP)	80
10-31. Deep Power-down (DP)	81
10-32. Enter Secured OTP (ENSO)	82
10-33. Exit Secured OTP (EXSO)	82
10-34. Read Security Register (RDSCUR)	82
10-35. Write Security Register (WRSCUR)	82
10-36. Write Protection Selection (WPSEL)	83
10-37. Advanced Sector Protection	85
10-38. Program/Erase Suspend/Resume	91
10-39. Erase Suspend	91
10-40. Program Suspend	91
10-41. Write-Resume	93
10-42. No Operation (NOP)	93
10-43. Software Reset (Reset-Enable (RSTEN) and Reset (RST))	93
11. Serial Flash Discoverable Parameter (SFDP)	95
11-1. Read SFDP Mode (RDSFDP)	95
Table 13. Signature and Parameter Identification Data Values	96
Table 14. Parameter Table (0): JEDEC Flash Parameter Tables	98
Table 15. Parameter Table (1): 4-Byte Instruction Tables	105
Table 16. Parameter Table (2): Macronix Flash Parameter Tables	107
12. RESET	109
Table 17. Reset Timing-(Power On)	109
Table 18. Reset Timing-(Other Operation)	109
13. POWER-ON STATE	110
14. ELECTRICAL SPECIFICATIONS	111
Table 19. ABSOLUTE MAXIMUM RATINGS	111
Table 20. CAPACITANCE TA = 25°C, f = 1.0 MHz	111
Table 21. DC CHARACTERISTICS	113



Table 22. AC CHARACTERISTICS	114
15. OPERATING CONDITIONS	116
Table 23. Power-Up/Down Voltage and Timing	118
15-1. INITIAL DELIVERY STATE	118
16. ERASE AND PROGRAMMING PERFORMANCE	119
17. DATA RETENTION	119
18. LATCH-UP CHARACTERISTICS	119
19. ORDERING INFORMATION	120
20. PART NAME DESCRIPTION	121
21. PACKAGE INFORMATION.....	122
22. REVISION HISTORY	124

**1.8V 512M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY****1. FEATURES****GENERAL**

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
 - 1.7 to 2.0 volt for read, erase, and program operations
- 512Mb: 536,870,912 x 1 bit structure or 268,435,456 x 2 bits (two I/O mode) structure or 134,217,728 x 4 bits (four I/O mode) structure
- Protocol Support
 - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Fast read for SPI mode
 - Support fast clock frequency up to 166MHz
 - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions
 - Support DTR (Double Transfer Rate) Mode
 - Configurable dummy cycle number for fast read operation
- Quad Peripheral Interface (QPI) available
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
 - Any Block can be erased individually
- Programming :
 - 256byte page buffer
 - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
 - The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
 - Advanced sector protection function
- Additional 8K bit security OTP
 - Features unique identifier
 - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte device ID
 - RES command for 1-byte Device ID
 - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI/SIO0
 - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
 - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
 - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- RESET#/SIO3
 - Hardware Reset pin or Serial input & Output for 4 x I/O read mode
- PACKAGE
 - 16-pin SOP (300mil)
 - 24-Ball BGA (5x5 ball array)
 - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25U51245G is 512Mb bits serial Flash memory, which is configured as 67,108,864 x 8 internally. When it is in two or four I/O mode, the structure becomes 268,435,456 bits x 2 or 134,217,728 bits x 4. MX25U51245G feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# and RESET# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U51245G MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25U51245G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

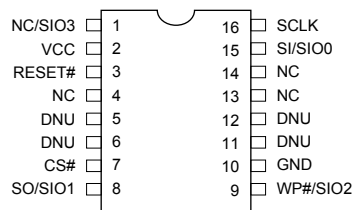
Table 1. Read performance Comparison

Numbers of Dummy Cycles	Fast Read (MHz)	Dual Output Fast Read (MHz)	Quad Output Fast Read (MHz)	Dual IO Fast Read (MHz)	Quad IO Fast Read (MHz)	Quad I/O DT Read (MHz)
4	-	-	-	84*	70	42
6	133	133	104	104	84*	52*
8	133*	133*	133*	133	104	66
10	166	166	166	166	133	100

Note: * mean default status

3. PIN CONFIGURATIONS

16-PIN SOP (300mil)



24-Ball BGA (5x5 ball array)

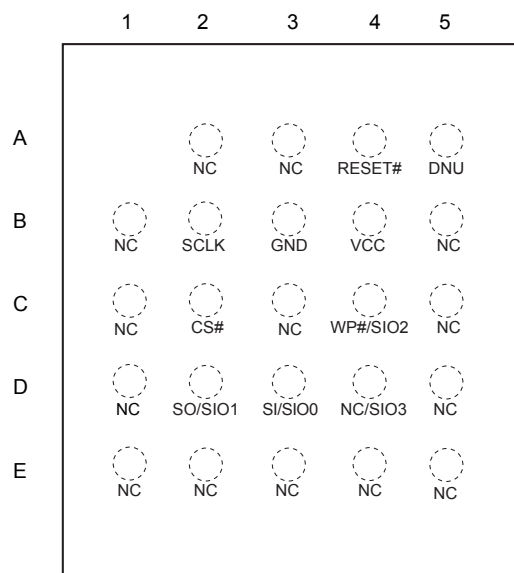
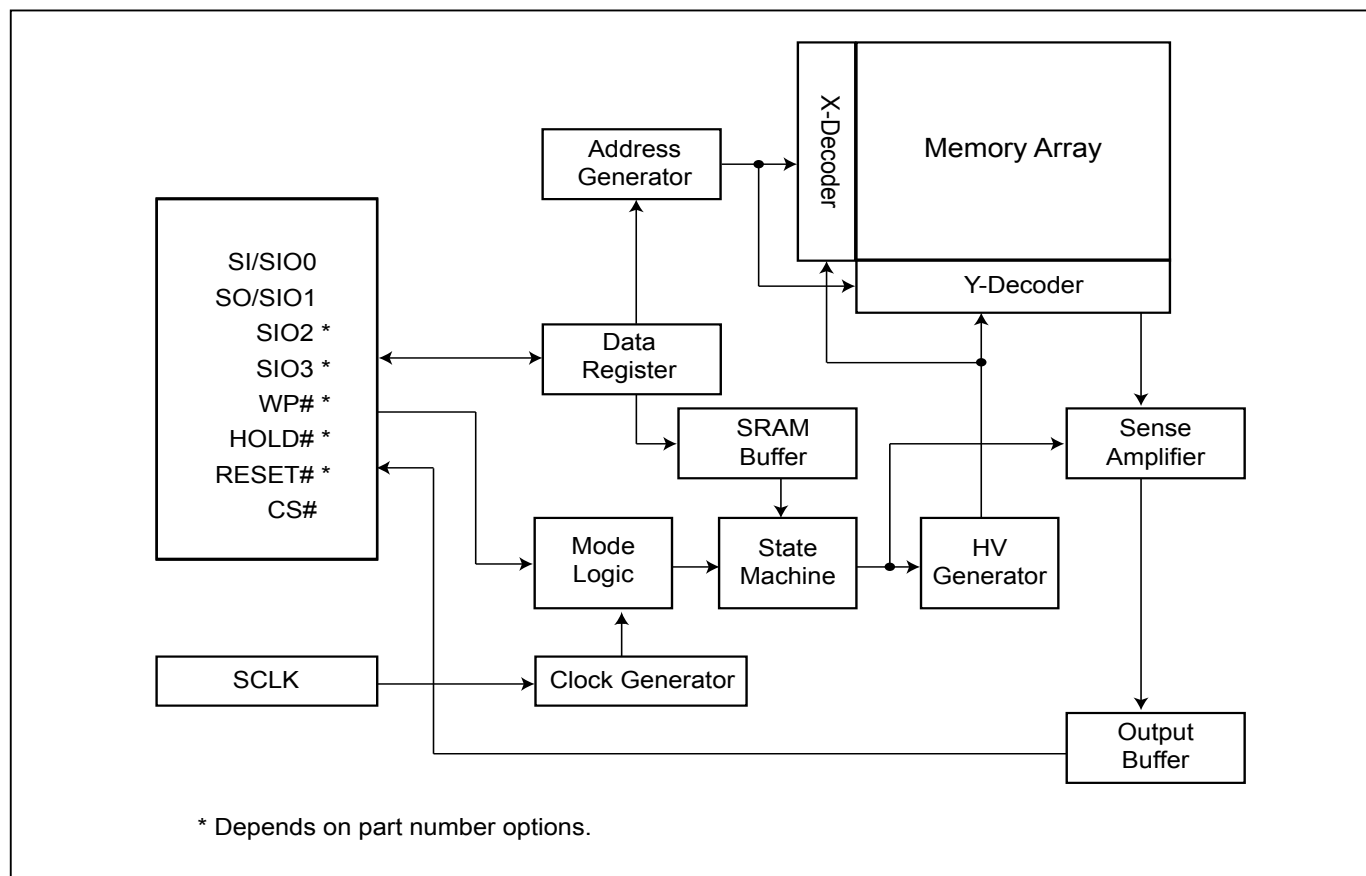


Table 2. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SCLK	Clock Input
RESET#	Hardware Reset Pin Active low ^(Note1)
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	No Connection or Serial Data Input & Output (for 4xI/O read mode)
VCC	Power Supply
GND	Ground
NC	No Connection
DNU	Do Not Use (It may connect to internal signal inside)

Note:

1. RESET# and WP# with internal pull high circuit.

4. BLOCK DIAGRAM

5. MEMORY ORGANIZATION

Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
1023	2047	16383	3FFF000h	3FFFFFFh
		⋮	⋮	⋮
	2046	16376	3FF8000h	3FF8FFFh
		16375	3FF7000h	3FF7FFFh
		⋮	⋮	⋮
1022	2045	16368	3FF0000h	3FF0FFFh
		16367	3FEF000h	3FEFFFFh
	2044	⋮	⋮	⋮
		16360	3FE8000h	3FE8FFFh
		16359	3FE7000h	3FE7FFFh
1021	2043	⋮	⋮	⋮
		16352	3FE0000h	3FE0FFFh
	2042	16351	3FDF000h	3FDFFFFh
		⋮	⋮	⋮
		16344	3FD8000h	3FD8FFFh

individual block
lock/unlock unit:64K-byte

individual 16 sectors
lock/unlock unit:4K-byte

individual block
lock/unlock unit:64K-byte

2	5	47	002F000h	002FFFFh
		⋮	⋮	⋮
	4	40	0028000h	0028FFFh
		39	027000h	0027FFFh
		⋮	⋮	⋮
1	3	32	0020000h	0020FFFh
		31	001F000h	001FFFFh
	2	⋮	⋮	⋮
		24	0018000h	0018FFFh
		23	0017000h	0017FFFh
0	1	⋮	⋮	⋮
		16	0010000h	0010FFFh
	0	15	000F000h	000FFFFh
		⋮	⋮	⋮
		8	0008000h	0008FFFh

individual block
lock/unlock unit:64K-byte

individual 16 sectors
lock/unlock unit:4K-byte

6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), Erase/Program suspend command, Erase/Program resume command and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

6-1. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as "Table 3. Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 3. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	512Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 1023rd)
0	0	1	0	2 (2 blocks, protected block 1022nd~1023rd)
0	0	1	1	3 (4 blocks, protected block 1020th~1023rd)
0	1	0	0	4 (8 blocks, protected block 1016th~1023rd)
0	1	0	1	5 (16 blocks, protected block 1008th~1023rd)
0	1	1	0	6 (32 blocks, protected block 992nd~1023rd)
0	1	1	1	7 (64 blocks, protected block 960th~1023rd)
1	0	0	0	8 (128 blocks, protected block 896th~1023rd)
1	0	0	1	9 (256 blocks, protected block 768th~1023rd)
1	0	1	0	10 (512 blocks, protected block 512nd~1023rd)
1	0	1	1	11 (1024 blocks, protected all)
1	1	0	0	12 (1024 blocks, protected all)
1	1	0	1	13 (1024 blocks, protected all)
1	1	1	0	14 (1024 blocks, protected all)
1	1	1	1	15 (1024 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	512Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th~1th)
0	0	1	1	3 (4 blocks, protected block 0th~3rd)
0	1	0	0	4 (8 blocks, protected block 0th~7th)
0	1	0	1	5 (16 blocks, protected block 0th~15th)
0	1	1	0	6 (32 blocks, protected block 0th~31st)
0	1	1	1	7 (64 blocks, protected block 0th~63rd)
1	0	0	0	8 (128 blocks, protected block 0th~127th)
1	0	0	1	9 (256 blocks, protected block 0th~255th)
1	0	1	0	10 (512 blocks, protected block 0th~511st)
1	0	1	1	11 (1024 blocks, protected all)
1	1	0	0	12 (1024 blocks, protected all)
1	1	0	1	13 (1024 blocks, protected all)
1	1	1	0	14 (1024 blocks, protected all)
1	1	1	1	15 (1024 blocks, protected all)

6-2. Additional 8K-bit secured OTP

The secured OTP for unique identifier: to provide 8K-bit one-time program area for setting device unique serial number. Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 8K-bit secured OTP by entering secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting secured OTP mode by writing Exit Security OTP command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to ["Table 10. Security Register Definition"](#) for security register bit definition and ["Table 4. 8K-bit Secured OTP Definition"](#) for address range definition.
- Note: Once lock-down by factory or customer, the corresponding range cannot be changed any more. While in secured OTP mode, array access is not allowed.

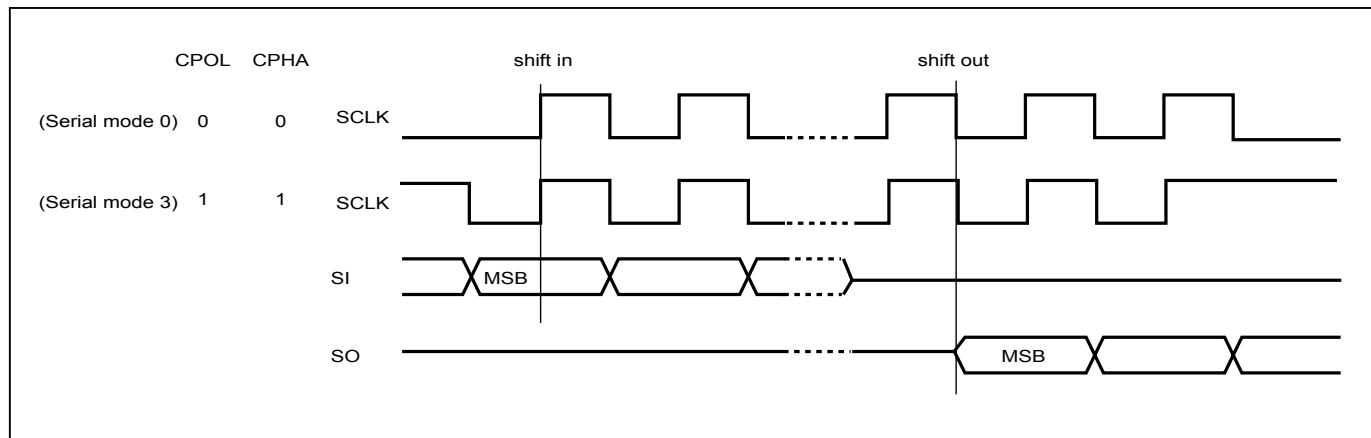
Table 4. 8K-bit Secured OTP Definition

Address range	Size	Lock-down
xxx000~xxx1FF	4096-bit	Determined by Factory
xxx200~xxx3FF	4096-bit	Determined by Customer

7. DEVICE OPERATION

- Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
- When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.
- When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.
- Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Serial Modes Supported".
- For the following instructions: RDID, RDSR, RDSCUR, READ/READ4B, FAST_READ/FAST_READ4B, 2READ/2READ4B, DREAD/DREAD4B, 4READ/4READ4B, QREAD/QREAD4B, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDLR, RDEAR, RDFBR, RDCR, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, PP/PP4B, 4PP/4PP4B, DP, ENSO, EXSO, WRSCUR, EN4B, EX4B, WPSEL, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
- During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

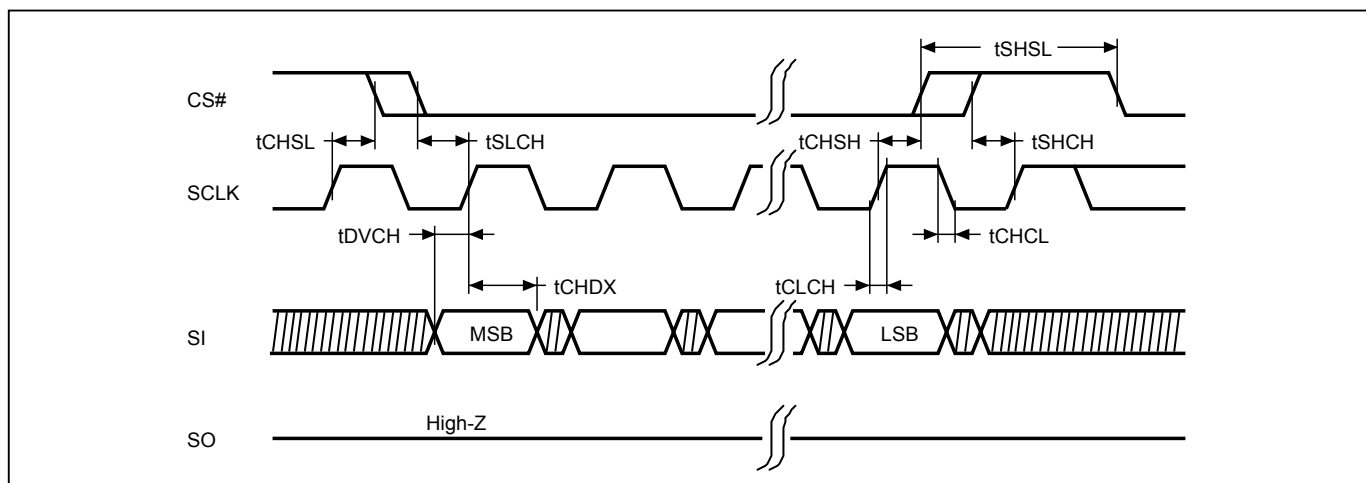


Figure 3. Output Timing (STR mode)

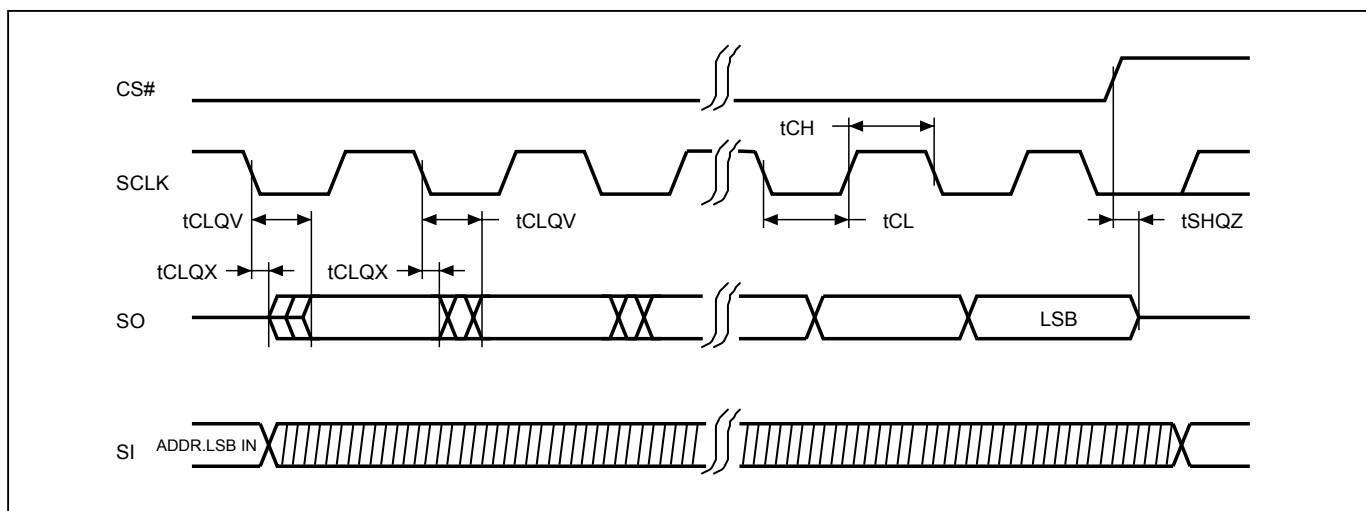
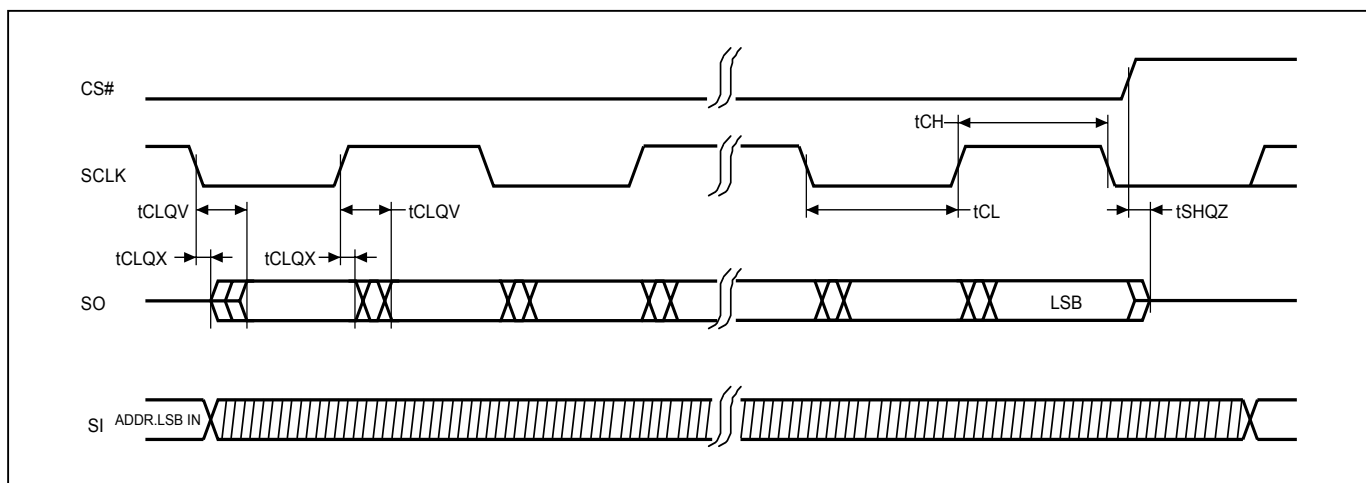


Figure 4. Output Timing (DTR mode)



7-1. 256Mb Address Protocol

The original 24 bit address protocol of serial Flash can only access density size below 128Mb. For the memory device of 256Mb and above, the 32bit address is requested for access higher memory size. The MX25U51245G provides three different methods to access the whole density:

(1) Command entry 4-byte address mode:

Issue Enter 4-Byte mode command to set up the 4BYTE bit in Configuration Register bit. After 4BYTE bit has been set, the number of address cycle become 32-bit.

(2) Extended Address Register (EAR):

configure the memory device into four 128Mb segments to select which one is active through the EAR<0-1>.

(3) 4-byte Address Command Set:

When issuing 4-byte address command set, 4-byte address (A31-A0) is requested after the instruction code. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Enter 4-Byte Address Mode

In 4-byte Address mode, all instructions are 32-bits address clock cycles. By using EN4B and EX4B to enable and disable the 4-byte address mode.

When 4-byte address mode is enabled, the EAR<0-1> becomes "don't care" for all instructions requiring 4-byte address. The EAR function will be disabled when 4-byte mode is enabled.

Extended Address Register

The device provides an 8-bit volatile register for extended Address Register: it identifies the extended address (A31~A24) above 128Mb density by using original 3-byte address.

Extended Address Register (EAR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A31	A30	A29	A28	A27	A26	A25	A24

For the MX25U51245G the A31 to A26 are Don't Care. During EAR, reading these bits will read as 0. The bit 0 is default as "0".

Figure 7. EAR Operation Segments

03FFFFFFh	EAR<1-0>= 11
03000000h	
02FFFFFFh	EAR<1-0>= 10
02000000h	
01FFFFFFh	EAR<1-0>= 01
01000000h	
00FFFFFFh	EAR<1-0>= 00
00000000h	

When under EAR mode, Read, Program, Erase operates in the selected segment by using 3-byte address mode.

For the read operation, the whole array data can be continually read out with one command. Data output starts from the selected top or bottom 128Mb, but it can cross the boundary. When the last byte of the segment is reached, the next byte (in a continuous reading) is the first byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.

The Chip erase command will erase the whole chip and is not limited by EAR selected segment. However, the sector erase ,block erase , program operation are limited in selected segment and will not cross the boundary.

Figure 5. Write EAR Register (WREAR) Sequence (SPI Mode)

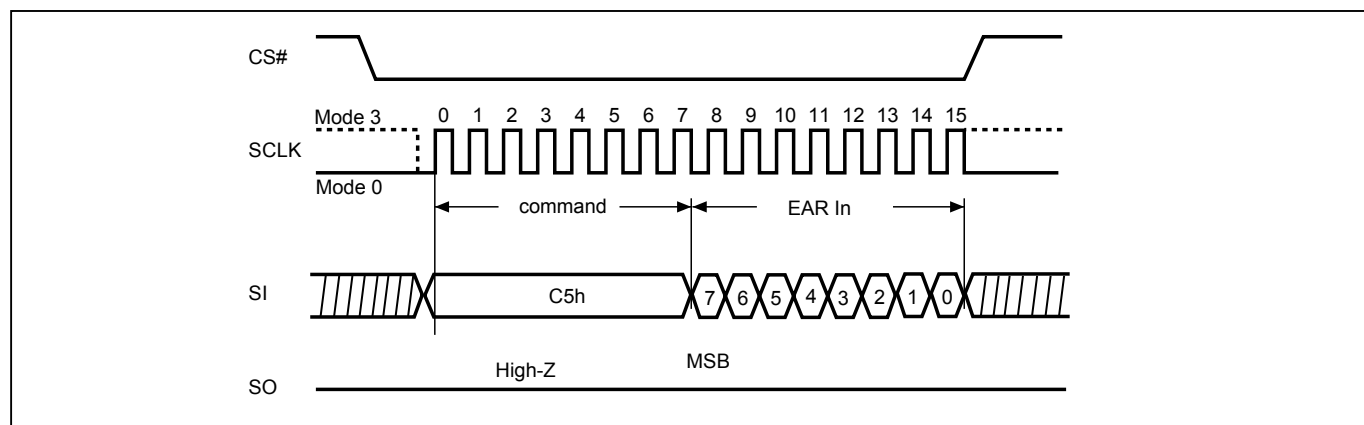


Figure 6. Write EAR Register (WREAR) Sequence (QPI Mode)

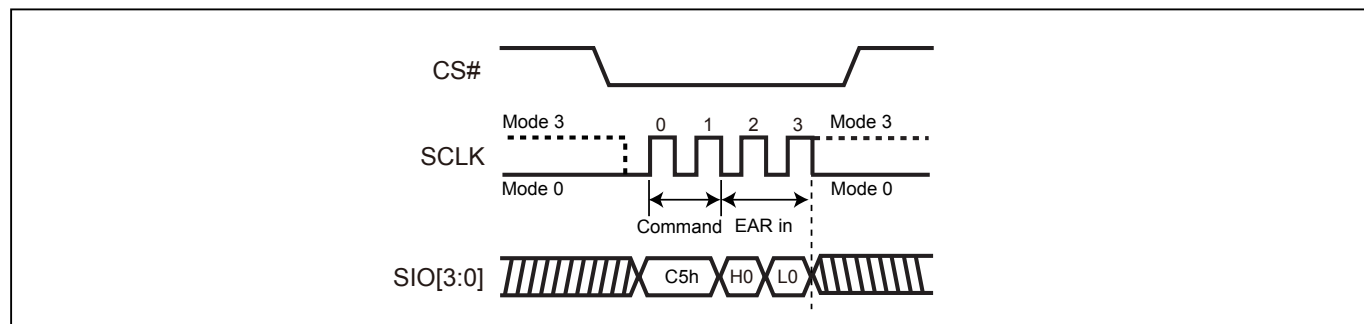


Figure 8. Read EAR (RDEAR) Sequence (SPI Mode)

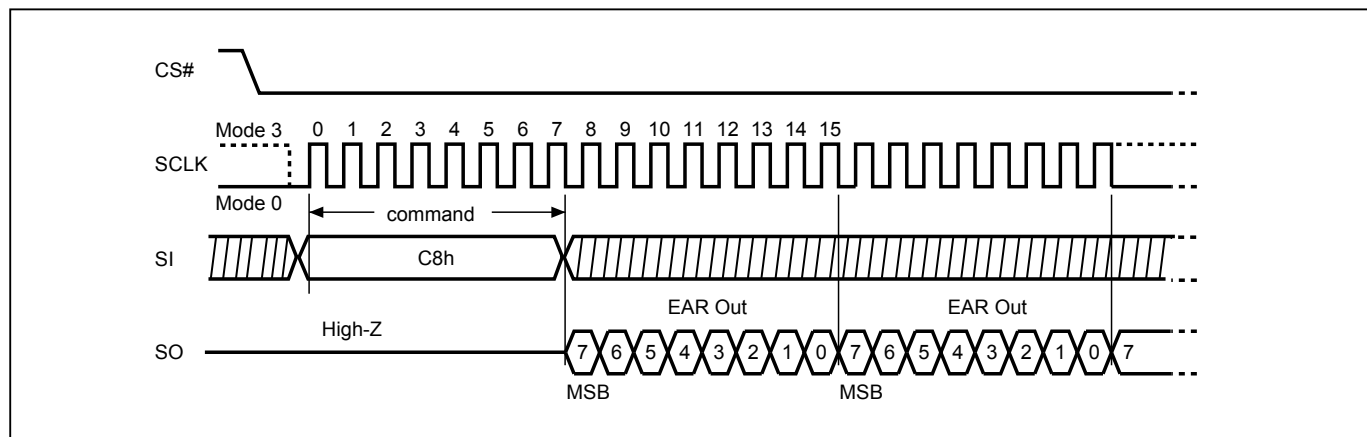
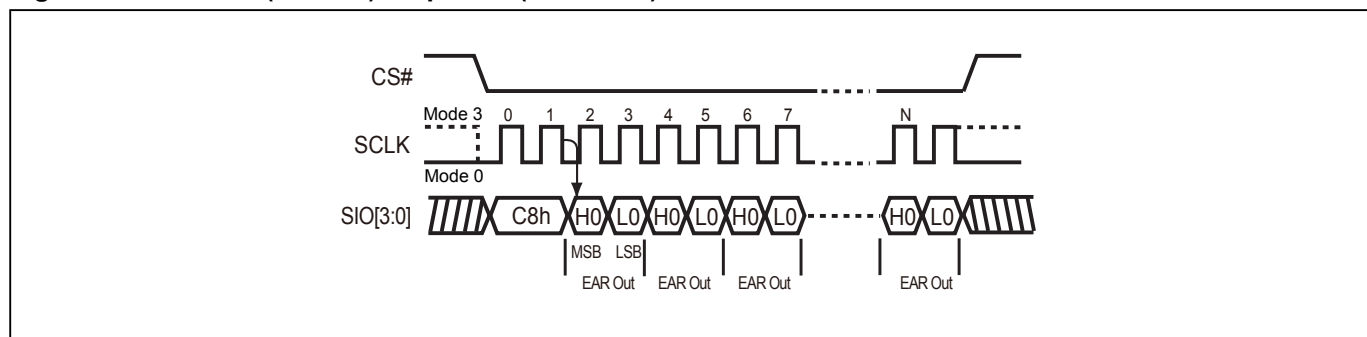


Figure 9. Read EAR (RDEAR) Sequence (QPI Mode)



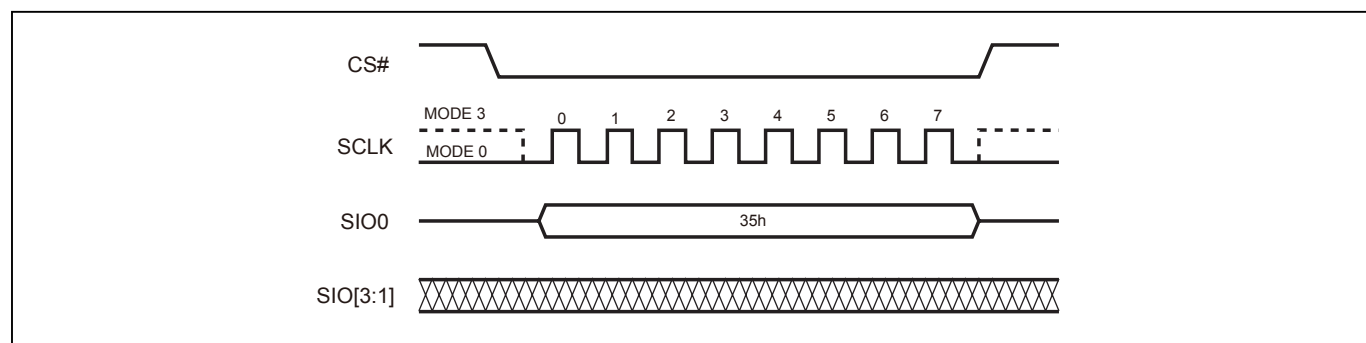
7-2. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing 35H command, the QPI mode is enable.

Figure 10. Enable QPI Sequence



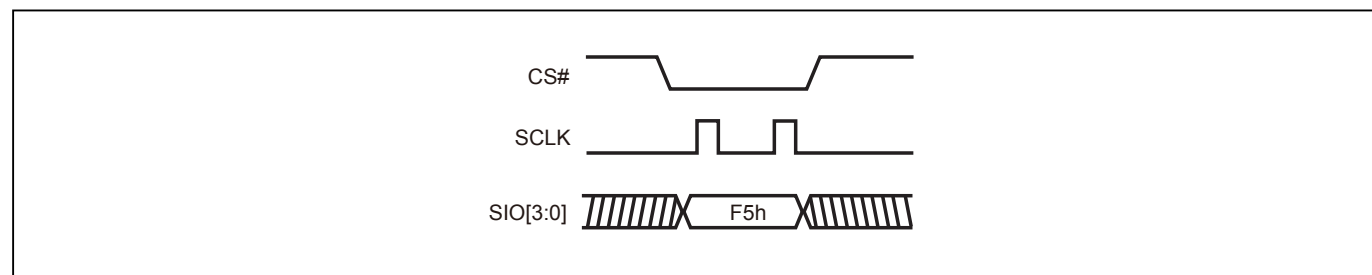
Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5H) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:

For EQIO and RSTQIO commands, CS# high width has to follow "write spec" tSHSL for next instruction.

Figure 11. Reset QPI Mode



8. COMMAND SET

Table 5. Read/Write Array Commands

Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I 2O read)	4READ (4 I/O read start from bottom 128Mb)	QREAD (1I 4O read)	4DTRD (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	3/4	3/4
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)	ED (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	Quad I/O read for bottom 128Mb with 6 dummy cycles	n bytes read out by Quad output until CS# goes high	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	0
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte		ADD1	ADD1	ADD1	ADD1	
3rd byte		ADD2	ADD2	ADD2	ADD2	
4th byte		ADD3	ADD3	ADD3	ADD3	
5th byte						
Data Cycles	1-256	1-256				
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Notes 2: Please note the address cycles above are based on 3-byte address mode. After enter 4-byte address mode by EN4B command, the address cycles will be increased to 4byte.

Table 6. Read/Write Array Commands (4 Byte Address Command Set)

Command (byte)	READ4B	FAST READ4B	2READ4B	DREAD4B	4READ4B	QREAD4B	4DTRD4B (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	4	4	4	4	4	4	4
1st byte	13 (hex)	0C (hex)	BC (hex)	3C (hex)	EC (hex)	6C (hex)	EE (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	read data byte by 4 byte address	read data byte by 4 byte address	read data byte by 2 x I/O with 4 byte address	Read data byte by Dual Output with 4 byte address	read data byte by 4 x I/O with 4 byte address	Read data byte by Quad Output with 4 byte address	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP4B	4PP4B	BE4B (block erase 64KB)	BE32K4B (block erase 32KB)	SE4B (Sector erase 4KB)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	4	4	4	4	4
1st byte	12 (hex)	3E (hex)	DC (hex)	5C (hex)	21 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte					
Data Cycles	1-256	1-256			
Action	to program the selected page with 4byte address	Quad input to program the selected page with 4byte address	to erase the selected (64KB) block with 4byte address	to erase the selected (32KB) block with 4byte address	to erase the selected (4KB) sector with 4byte address

Table 7. Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	RDEAR (read extended address register)	WREAR (write extended address register)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	C8 (hex)	C5 (hex)
2nd byte					Values		
3rd byte					Values		
4th byte							
5th byte							
Data Cycles					1-2		1
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/ configuration register	read extended address register	write extended address register

Command (byte)	WPSEL (Write Protect Selection)	EQIO (Enable QPI)	RSTQIO (Reset QPI)	EN4B (enter 4-byte mode)	EX4B (exit 4-byte mode)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)
Mode	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	68 (hex)	35 (hex)	F5 (hex)	B7 (hex)	E9 (hex)	B0 (hex)	30 (hex)
2nd byte							
3rd byte							
4th byte							
5th byte							
Data Cycles							
Action	to enter and enable individual block protect mode	Entering the QPI mode	Exiting the QPI mode	to enter 4-byte mode and set 4BYTE bit as "1"	to exit 4-byte mode and clear 4BYTE bit to be "0"		

Command (byte)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)	RDFBR (read fast boot register)	WRFBR (write fast boot register)	ESFBR (erase fast boot register)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI	SPI	SPI
1st byte	B9 (hex)	AB (hex)	C0 (hex)	16(hex)	17(hex)	18(hex)
2nd byte						
3rd byte						
4th byte						
5th byte						
Data Cycles				1-4	4	
Action	enters deep power down mode	release from deep power down mode	to set Burst length			

Table 8. ID/Security Commands

Command (byte)	RDID (read identification)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	0	0	0	0	3	0	0
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1		
3rd byte		x	x		ADD2		
4th byte			ADD1		ADD3		
5th byte					Dummy (8)		
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	ID in QPI interface	Read SFDP mode	to enter the secured OTP mode	to exit the secured OTP mode

Command (byte)	RDSCUR (read security register)	WRSCUR (write security register)	GBLK (gang block lock)	GBULK (gang block unlock)	WRLR (write Lock register)	RDLR (read Lock register)	WRSPB (SPB bit program)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI	SPI	SPI
Address Bytes	0	0	0	0	0	0	4
1st byte	2B (hex)	2F (hex)	7E (hex)	98 (hex)	2C (hex)	2D (hex)	E3 (hex)
2nd byte							ADD1
3rd byte							ADD2
4th byte							ADD3
5th byte							ADD4
Data Cycles					2	2	
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	whole chip write protect	whole chip unprotect			

Command (byte)	ESSPB (all SPB bit erase)	RDSPB (read SPB status)	WRDPB (write DPB register)	RDDPB (read DPB register)
Mode	SPI	SPI	SPI	SPI
Address Bytes	0	4	4	4
1st byte	E4 (hex)	E2 (hex)	E1 (hex)	E0 (hex)
2nd byte		ADD1	ADD1	ADD1
3rd byte		ADD2	ADD2	ADD2
4th byte		ADD3	ADD3	ADD3
5th byte		ADD4	ADD4	ADD4
Data Cycles		1	1	1
Action				

Table 9. Reset Commands

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
Mode	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 3: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

Note 4: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in. Please note the number after "ADD" are based on 3-byte address mode, for 4-byte address mode, which will be increased.

9. REGISTER DESCRIPTION

9-1. Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in [Table 3](#)) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, RESET# are enable. While QE is "1", it performs Quad I/O mode and WP#, RESET# are disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM and RESET will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the ["Table 3. Protected Area Sizes"](#).

9-2. Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit

The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *Output Driver Strength Table*) of the device. The Output Driver Strength is defaulted as 30 Ohms when delivered from factory. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

TB bit

The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as "0", which means Top area protect. When it is set as "1", the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

PBE bit

The Preamble Bit Enable (PBE) bit is a volatile bit. It is used to enable or disable the preamble bit data pattern output on dummy cycles. The PBE bit is defaulted as "0", which means preamble bit is disabled. When it is set as "1", the preamble bit will be enabled, and inputted into dummy cycles. To write the PBE bits requires the Write Status Register (WRSR) instruction to be executed.

4BYTE Indicator bit

By writing EN4B instruction, the 4BYTE bit may be set as "1" to access the address length of 32-bit for memory area of higher density (large than 128Mb). The default state is "0" as the 24-bit address mode. The 4BYTE bit may be cleared by power-off or writing EX4B instruction to reset the state to be "0".

Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DC1 (Dummy cycle 1)	DC0 (Dummy cycle 0)	4 BYTE	PBE (Preamble bit Enable)	TB (top/bottom selected)	ODS 2 (output driver strength)	ODS 1 (output driver strength)	ODS 0 (output driver strength)
(note 2)	(note 2)	0=3-byte address mode 1=4-byte address mode (Default=0)	0=Disable 1=Enable	0=Top area protect 1=Bottom area protect (Default=0)	(note 1)	(note 1)	(note 1)
volatile bit	volatile bit	volatile bit	volatile bit	OTP	volatile bit	volatile bit	volatile bit

Note 1: see *"Output Driver Strength Table"*

Note 2: see *"Dummy Cycle and Frequency Table (MHz)"*

Output Driver Strength Table

ODS2	ODS1	ODS0	Description	Note
0	0	0	150 Ohms	Impedance at VCC/2 (Typical)
0	0	1	75 Ohms	
0	1	0	50 Ohms	
0	1	1	38 Ohms	
1	0	0	30 Ohms	
1	0	1	25 Ohms	
1	1	0	22 Ohms	
1	1	1	20 Ohms (Default)	

Dummy Cycle and Frequency Table (MHz)

DC[1:0]	Numbers of Dummy clock cycles	Fast Read	Dual Output Fast Read	Quad Output Fast Read
00 (default)	8	133	133	133
01	6	133	133	104
10	8	133	133	133
11	10	166	166	166

DC[1:0]	Numbers of Dummy clock cycles	Dual IO Fast Read
00 (default)	4	84
01	6	104
10	8	133
11	10	166

DC[1:0]	Numbers of Dummy clock cycles	Quad IO Fast Read	Quad I/O DTR Read
00 (default)	6	84	52
01	4	70	42
10	8	104	66
11	10	133	100

9-3. Security Register

The definition of the Security Register bits is as below:

Write Protection Selection bit. Please reference to "[Write Protection Selection bit](#)"

Erase Fail bit. The Erase Fail bit is a status flag, which shows the status of last Erase operation. It will be set to "1", if the erase operation fails or the erase region is protected. It will be set to "0", if the last operation is success. Please note that it will not interrupt or stop any operation in the flash memory.

Program Fail bit. The Program Fail bit is a status flag, which shows the status of last Program operation. It will be set to "1", if the program operation fails or the program region is protected. It will be set to "0", if the last operation is success. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the Secured OTP area cannot be updated any more. While it is in secured OTP mode, main array access is not allowed.

Table 10. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (indicate if lock-down)	Secured OTP indicator bit
0=normal WP mode 1=individual mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock- down 1 = lock-down (cannot program/ erase OTP)	0 = non- factory lock 1 = factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (OTP)

10. COMMAND DESCRIPTION

10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP/PP4B, 4PP/4PP4B, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 12. Write Enable (WREN) Sequence (SPI Mode)

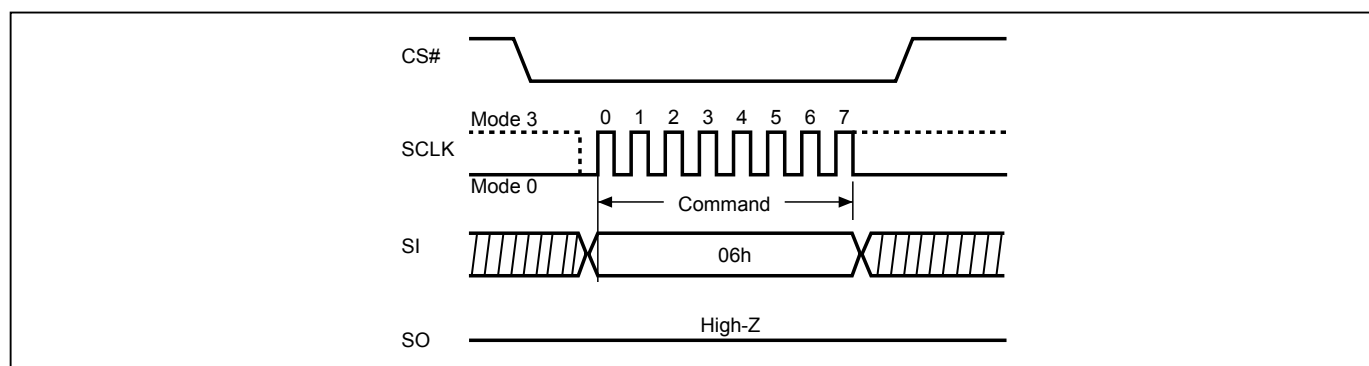
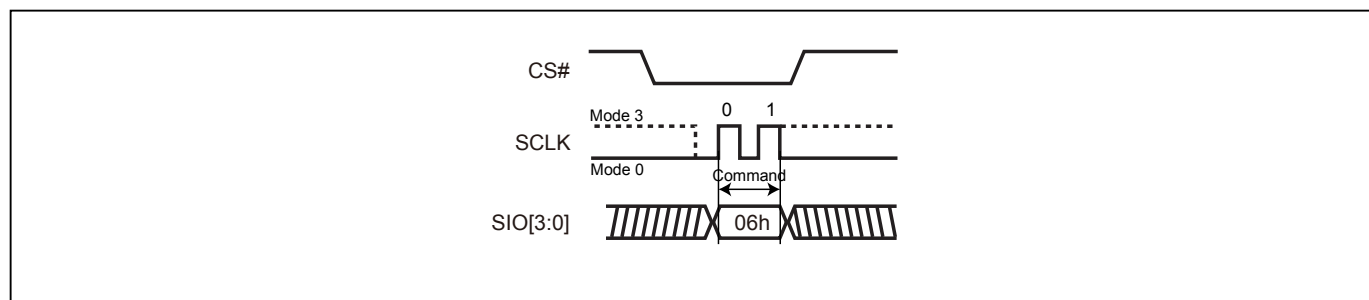


Figure 13. Write Enable (WREN) Sequence (QPI Mode)



10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSRcommand completion
- PP/PP4B command completion
- 4PP/4PP4B command completion
- SE/SE4B command completion
- BE32K/BE32K4B command completion
- BE/BE4B command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion
- WREAR command completion
- WRLR command completion
- WRSPB command completion
- WRUSPB command completion
- ESSPB command completion
- WRDPB command completion
- WRFBR command completion
- ESFBR command completion

Figure 14. Write Disable (WRDI) Sequence (SPI Mode)

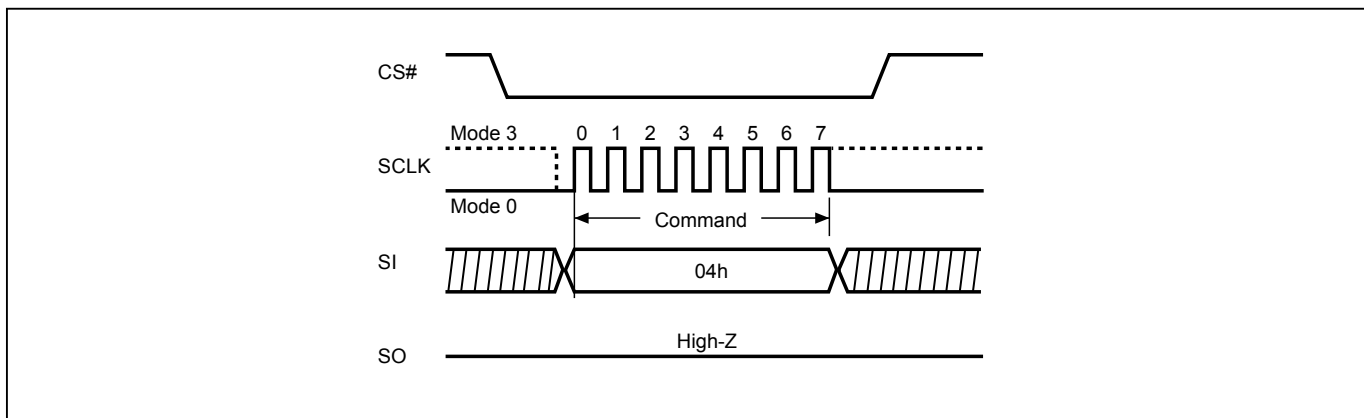
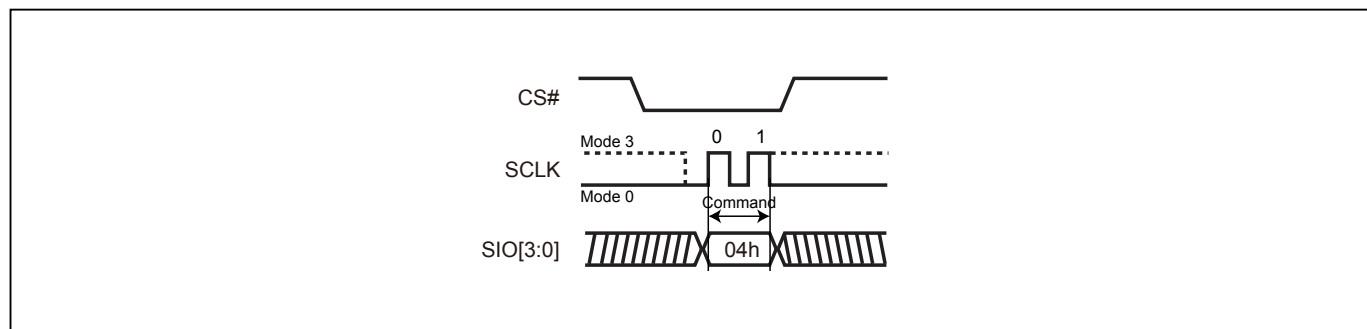


Figure 15. Write Disable (WRDI) Sequence (QPI Mode)



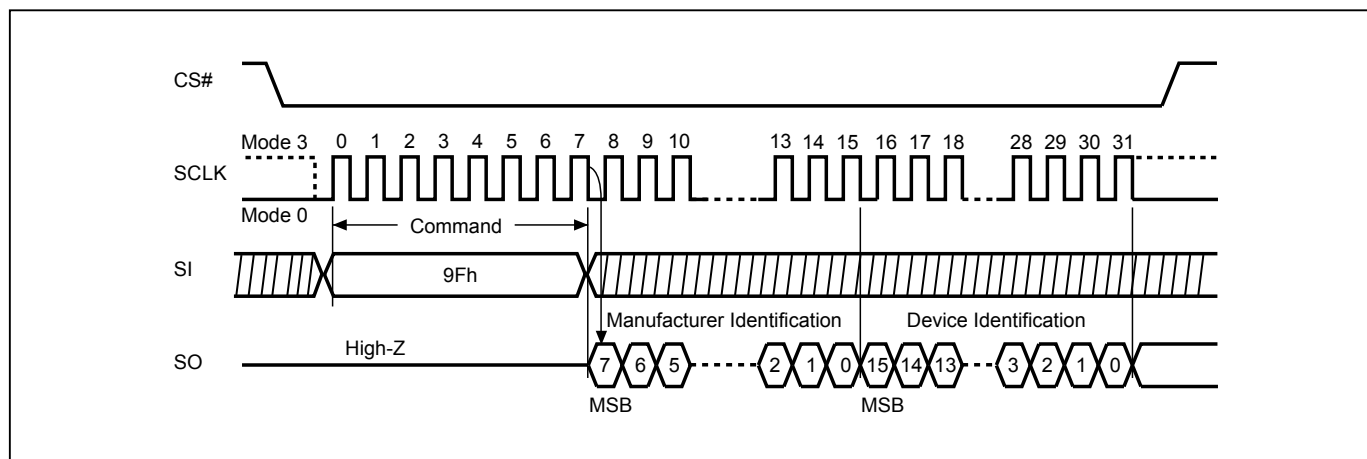
10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as ["Table 11. ID Definitions"](#).

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 16. Read Identification (RDID) Sequence (SPI mode only)



10-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES2} , and Chip Select (CS#) must remain High for at least $t_{RES2}(\max)$, as specified in "Table 22. AC CHARACTERISTICS". Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as Table 11 ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of t_{RES2} to transit to standby mode, and CS# must remain to high at least $t_{RES2}(\max)$. Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 17. Read Electronic Signature (RES) Sequence (SPI Mode)

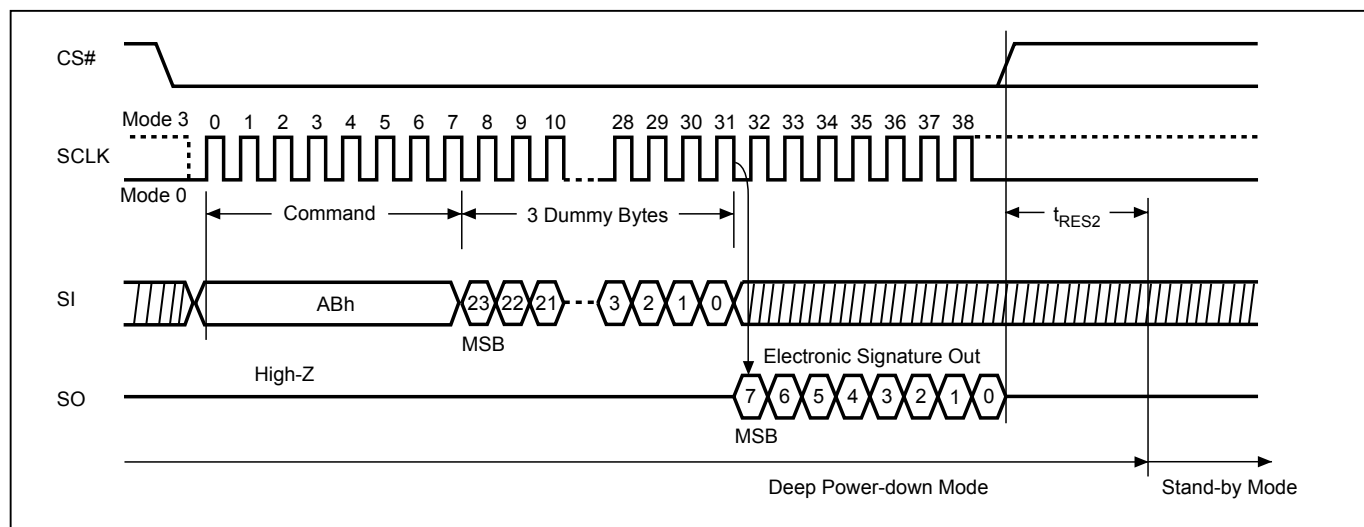


Figure 18. Read Electronic Signature (RES) Sequence (QPI Mode)

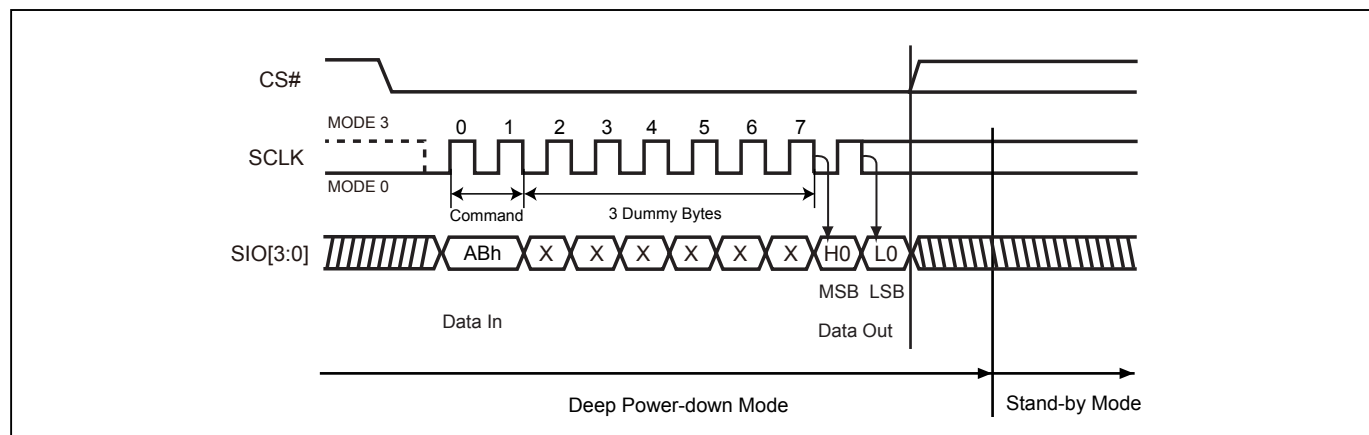


Figure 19. Release from Deep Power-down (RDP) Sequence (SPI Mode)

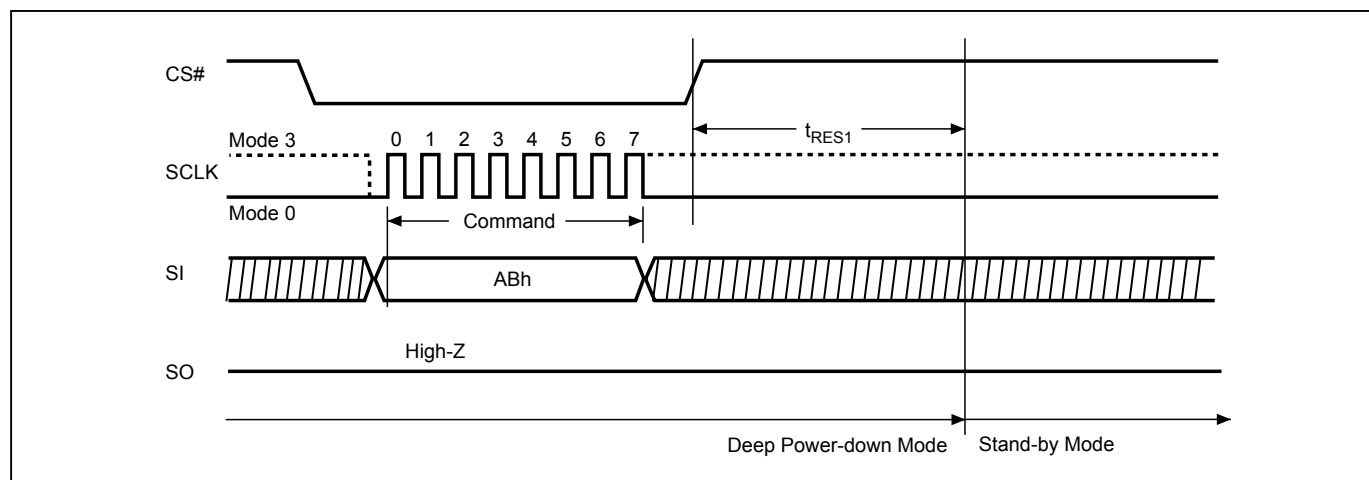
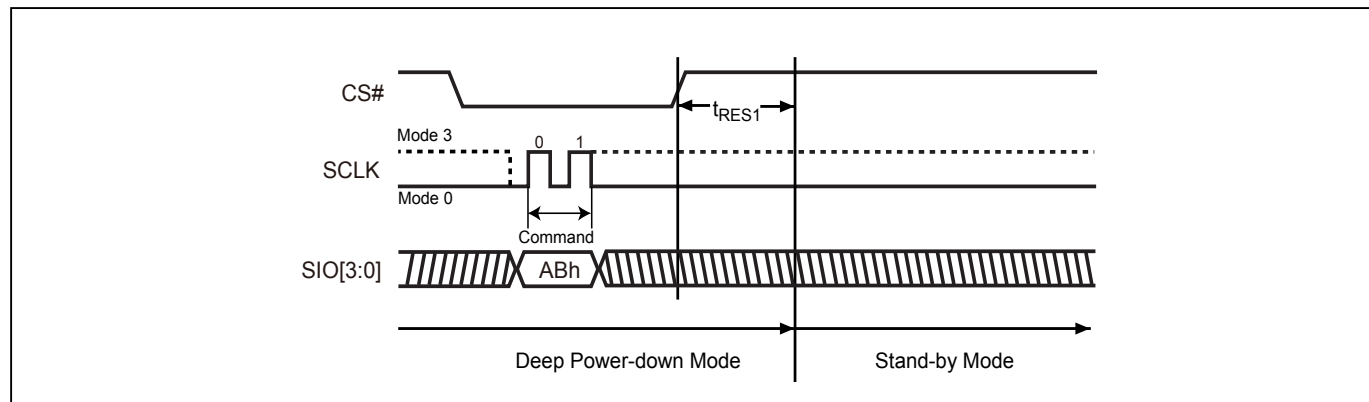


Figure 20. Release from Deep Power-down (RDP) Sequence (QPI Mode)

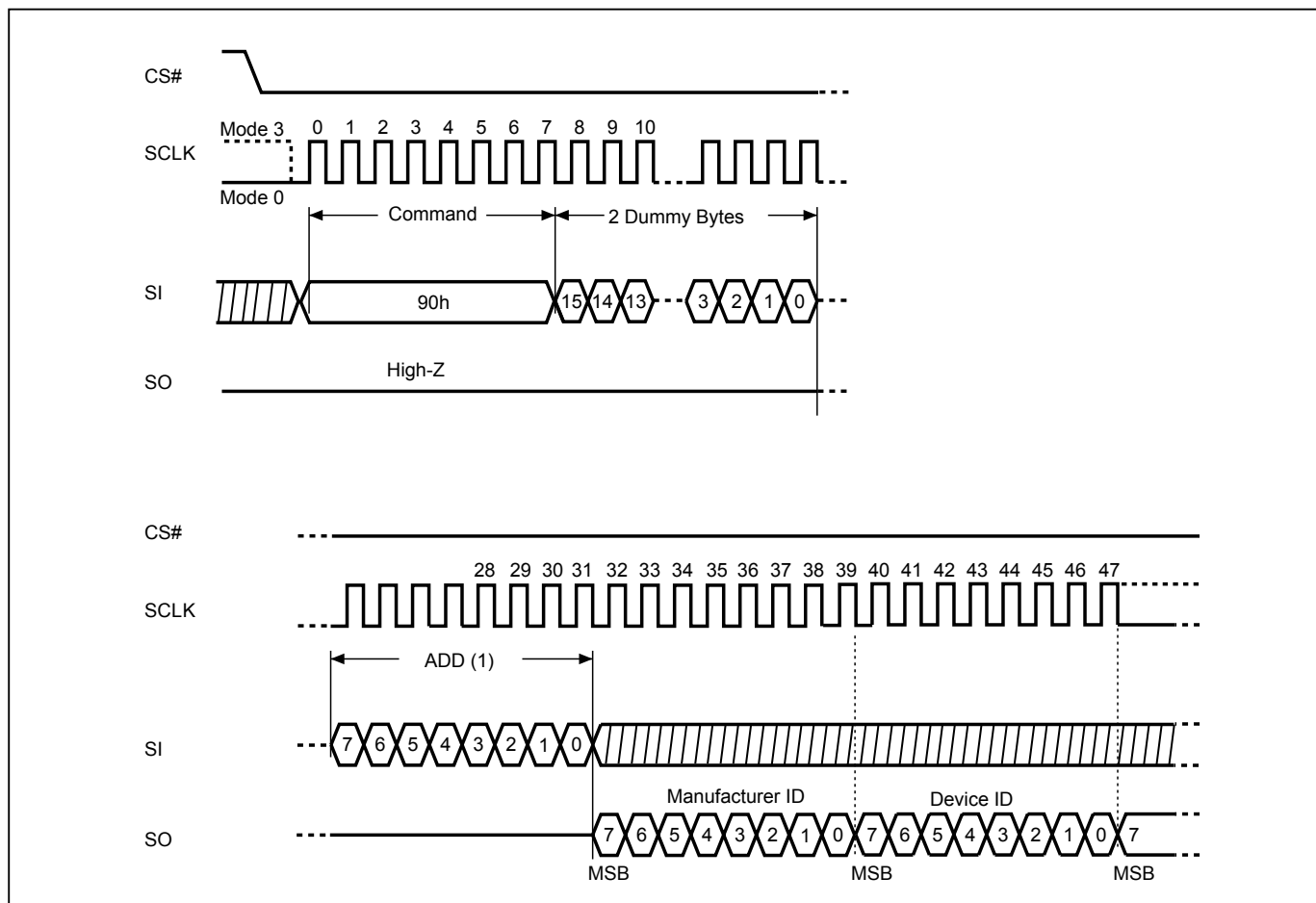


10-5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID values are listed in [Table 11](#) of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 21. Read Electronic Manufacturer & Device ID (REMS) Sequence (SPI Mode only)



Notes:

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

10-6. QPI ID Read (QPIID)

User can execute this QPIID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issue QPIID instruction is CS# goes low→sending QPI ID instruction→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

Table 11. ID Definitions

Command Type		MX25U51245G		
RDID	9Fh	Manufactory ID	Memory type	Memory density
		C2	25	3A
RES	ABh	Electronic ID		
		3A		
REMS	90h	Manufactory ID	Device ID	
		C2	3A	
QPIID	AFh	Manufactory ID	Memory type	Memory density
		C2	25	3A

10-7. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 22. Read Status Register (RDSR) Sequence (SPI Mode)

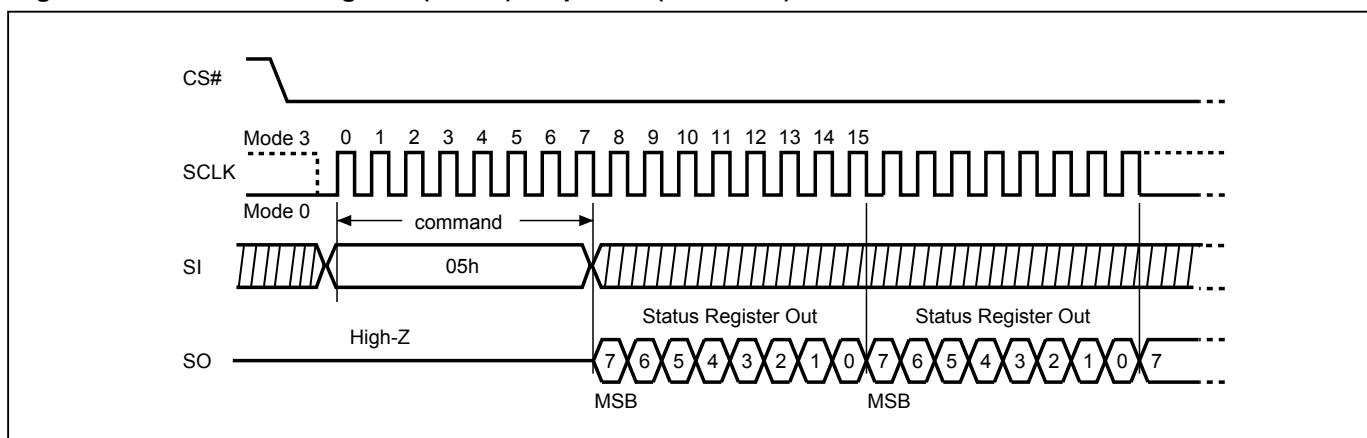
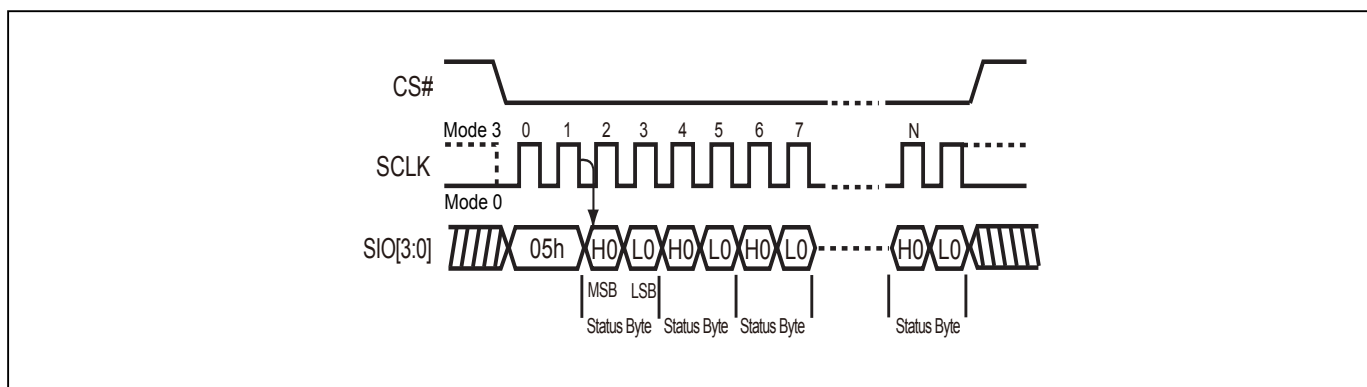


Figure 23. Read Status Register (RDSR) Sequence (QPI Mode)



10-8. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 24. Read Configuration Register (RDCR) Sequence (SPI Mode)

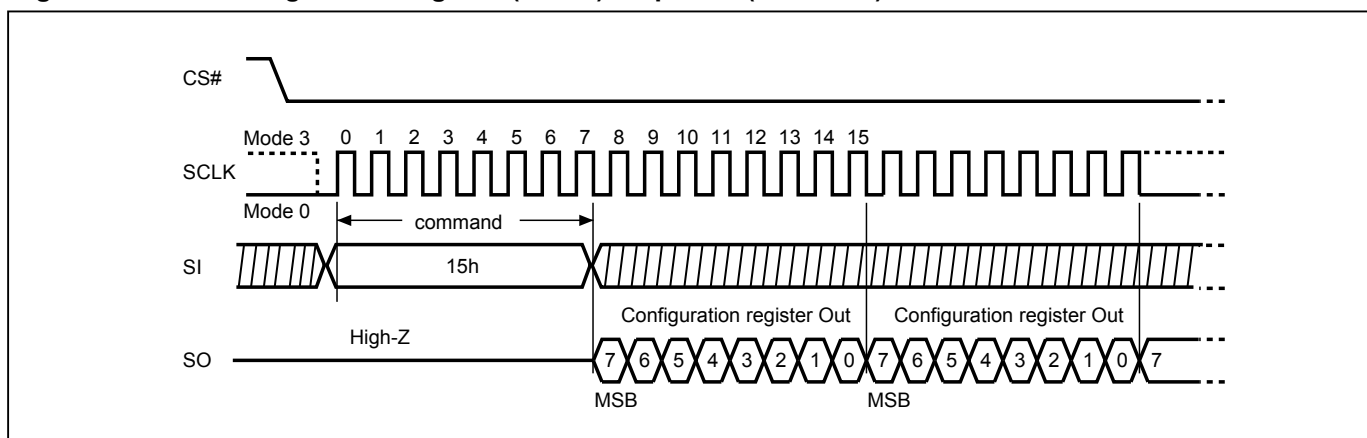
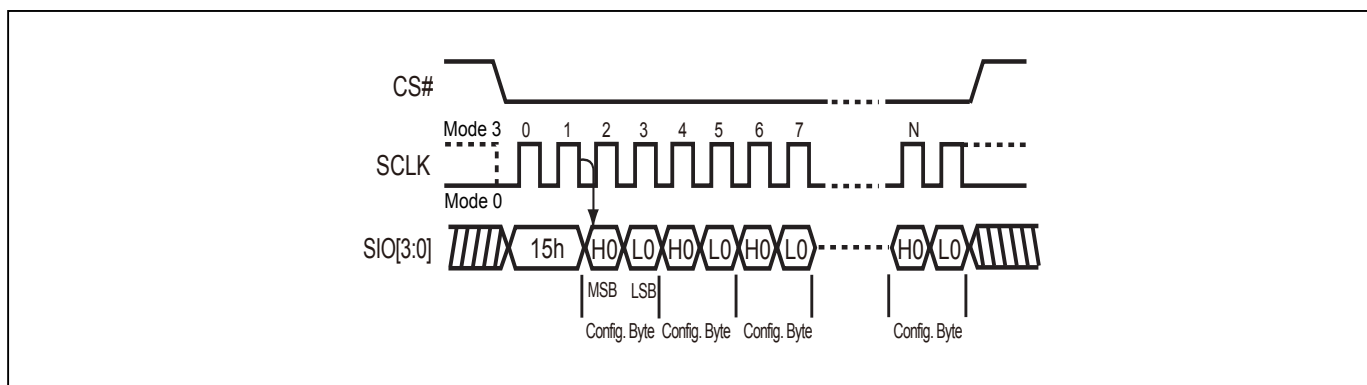


Figure 25. Read Configuration Register (RDCR) Sequence (QPI Mode)



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 26. Program/Erase flow with read array data

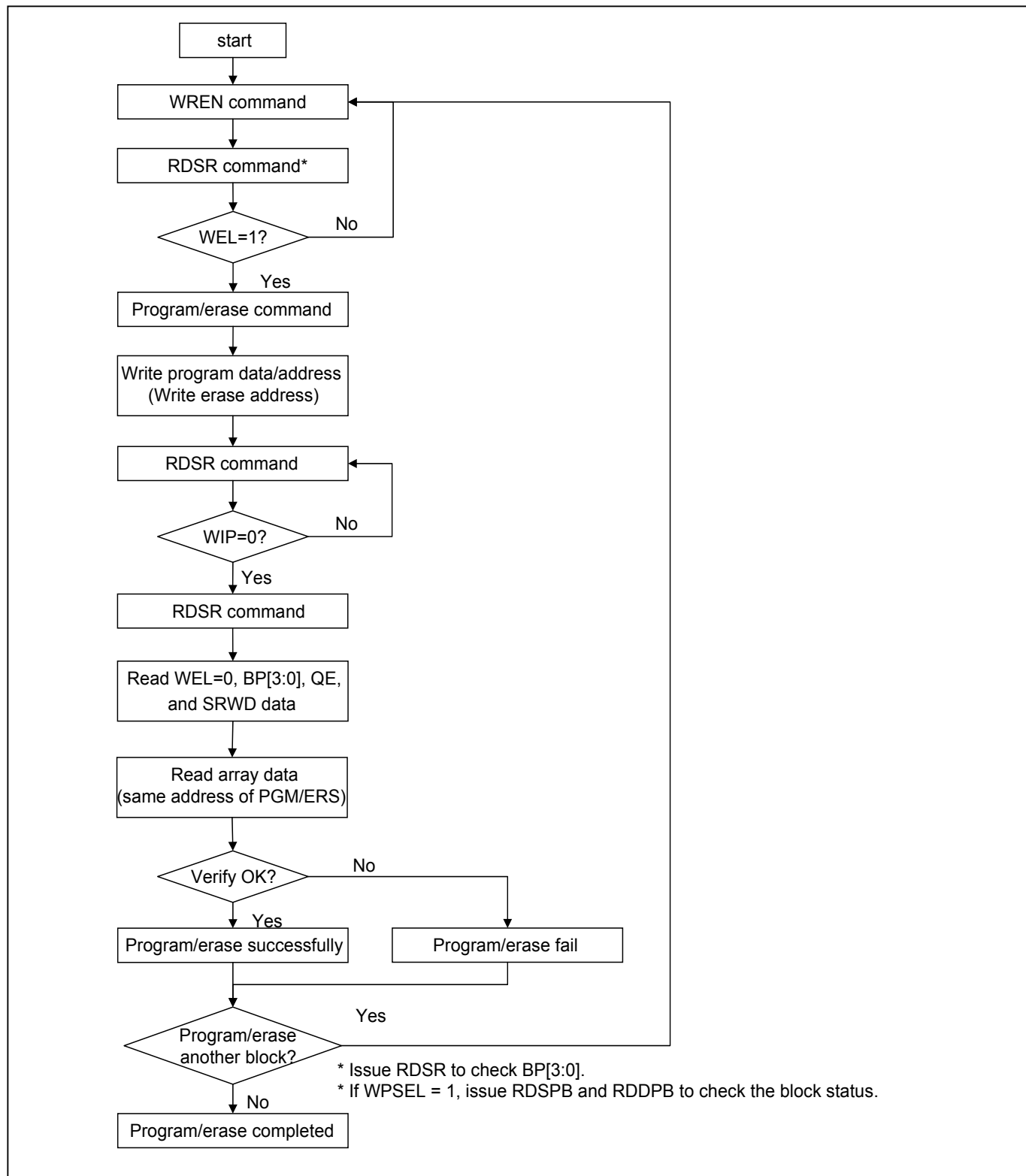
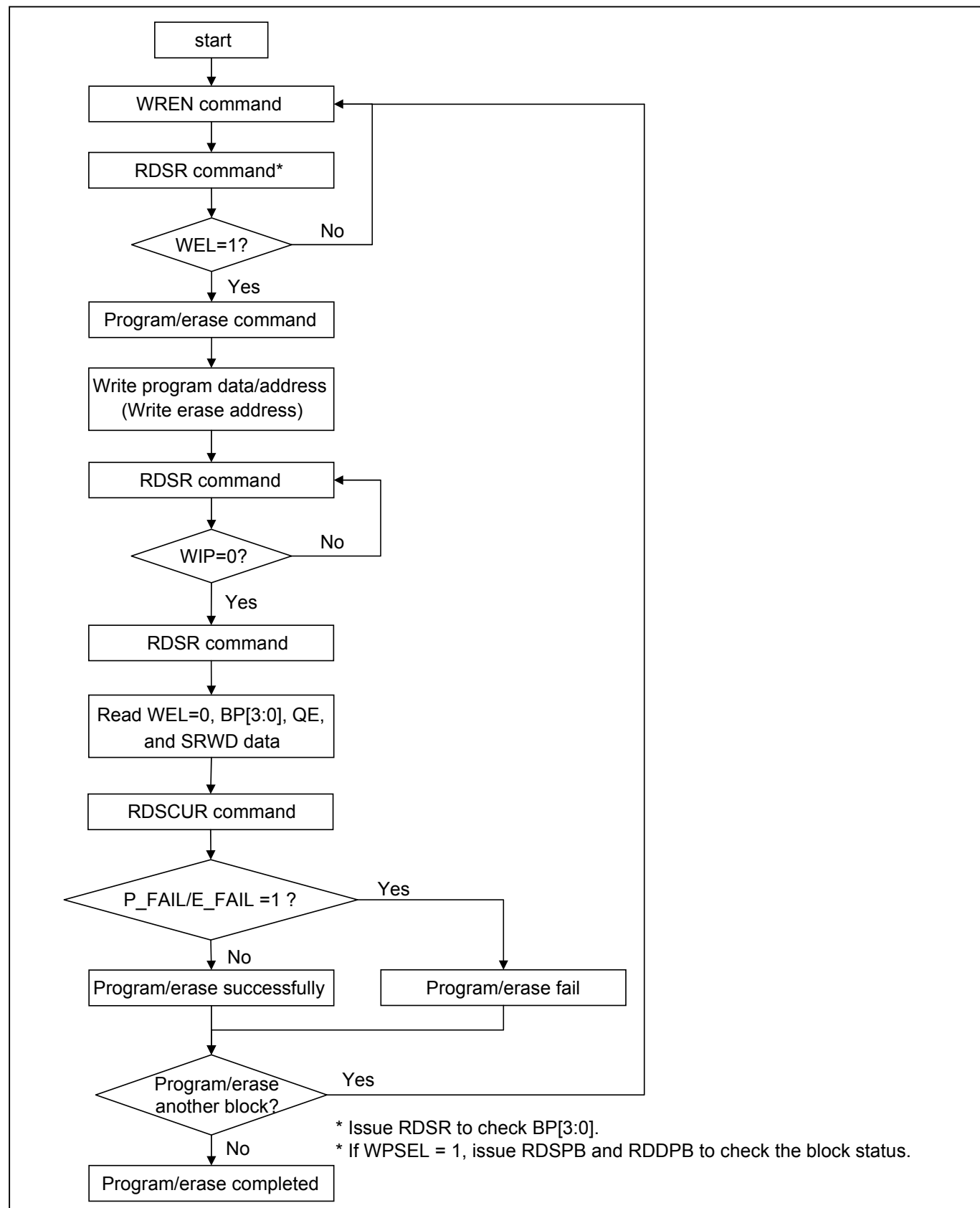


Figure 27. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



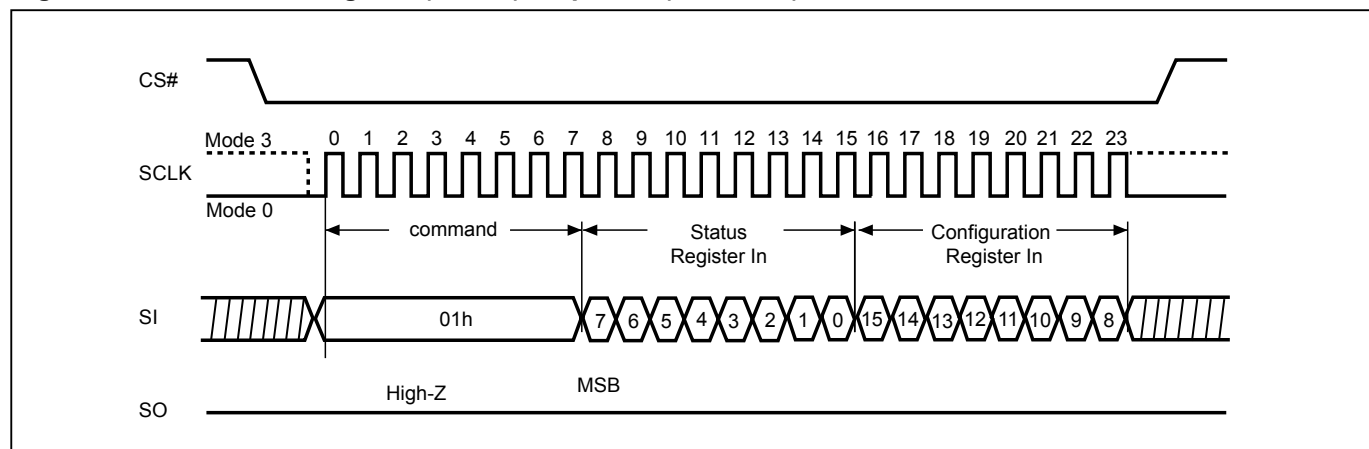
10-9. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in [Table 3](#)). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

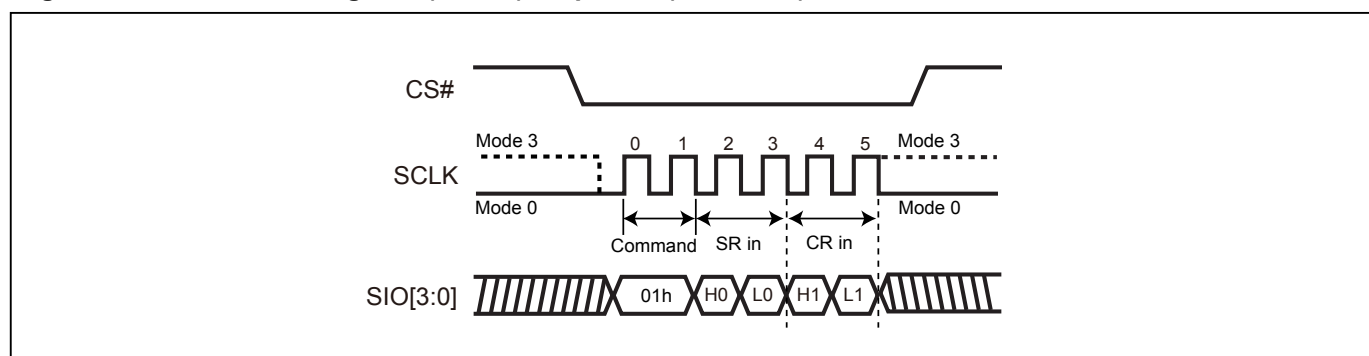
The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 28. Write Status Register (WRSR) Sequence (SPI Mode)



Note : The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

Figure 29. Write Status Register (WRSR) Sequence (QPI Mode)



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM)

Note:

If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and T/B bit and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0 and T/B bit.

If the system enter QPI or set QE=1, the feature of HPM will be disabled.

Table 12. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in [Table 3](#).

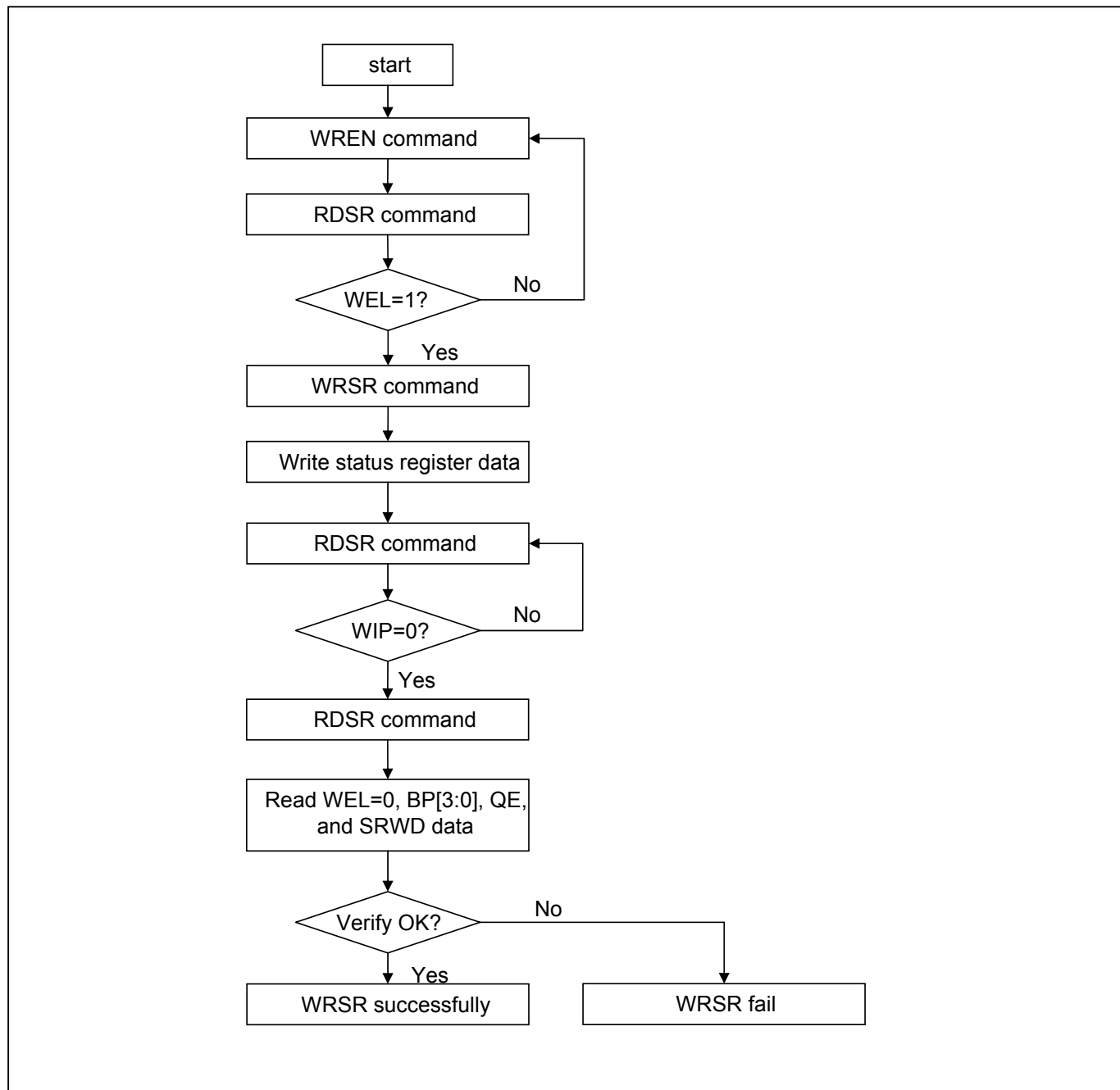
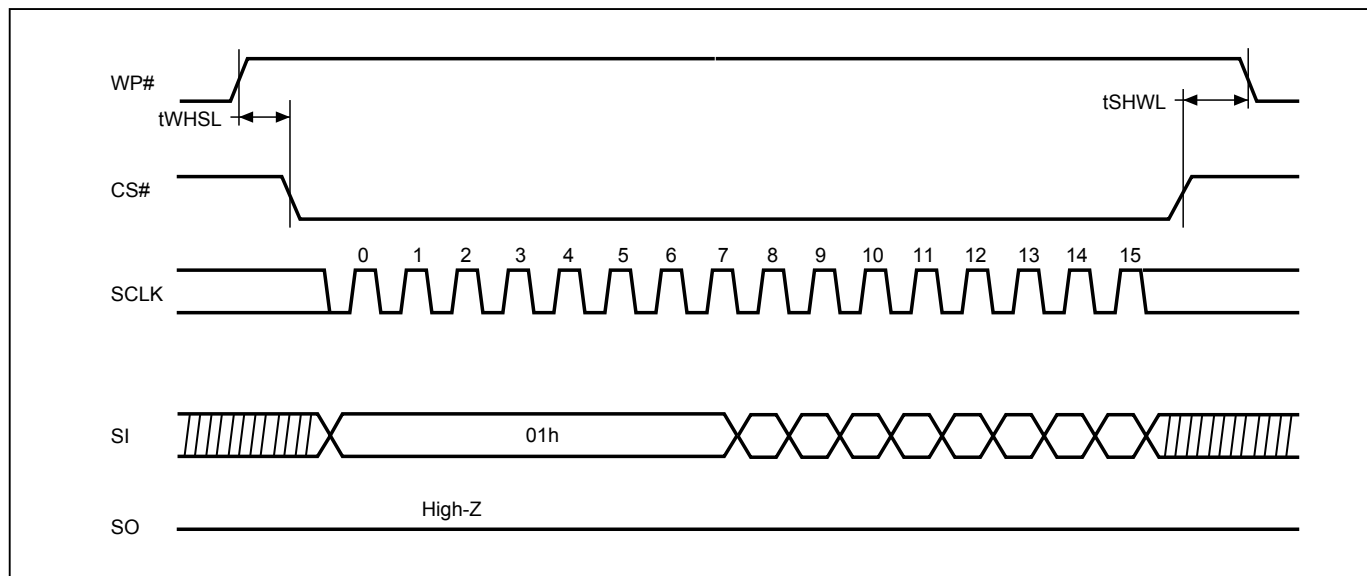
Figure 30. WRSR flow

Figure 31. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



Note: WP# must be kept high until the embedded operation finish.

10-10. Enter 4-byte mode (EN4B)

The EN4B instruction enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit5 (4BYTE bit) of security register will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit. There are three methods to exit the 4-byte mode: writing exit 4-byte mode (EX4B) instruction, Reset or power-off.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The following command don't support 4byte address: RDSFDP, RES and REMS.

The sequence of issuing EN4B instruction is: CS# goes low → sending EN4B instruction to enter 4-byte mode(automatically set 4BYTE bit as "1") → CS# goes high.

10-11.Exit 4-byte mode (EX4B)

The EX4B instruction is executed to exit the 4-byte address mode and return to the default 3-bytes address mode. After sending out the EX4B instruction, the bit5 (4BYTE bit) of Configuration register will be cleared to be "0" to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.

The sequence of issuing EX4B instruction is: CS# goes low → sending EX4B instruction to exit 4-byte mode (automatically clear the 4BYTE bit to be "0") → CS# goes high.

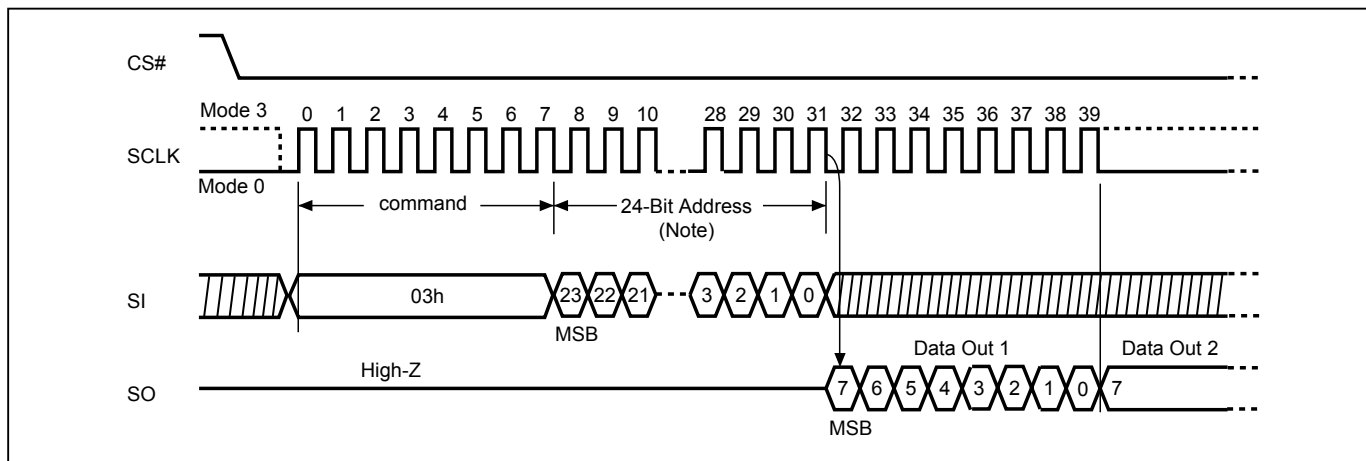
10-12. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency f_R . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte or 4-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 32. Read Data Bytes (READ) Sequence (SPI Mode only)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-13. Read Data Bytes at Higher Speed (FAST_READ)

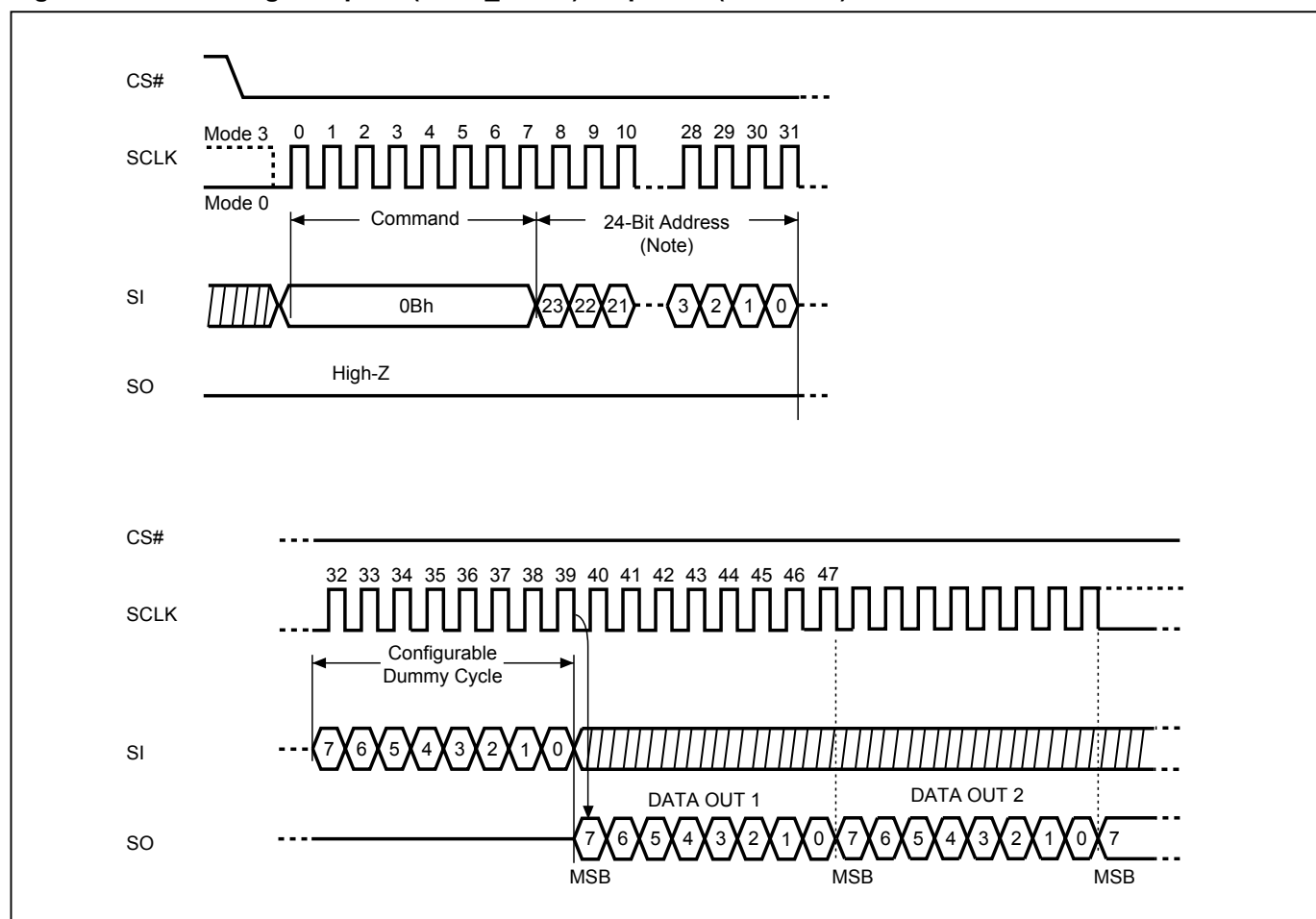
The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency f_C . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

Read on SPI Mode The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte or 4-byte address on SI→ 8 dummy cycles (default)→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 33. Read at Higher Speed (FAST_READ) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-14. Dual Output Read Mode (DREAD)

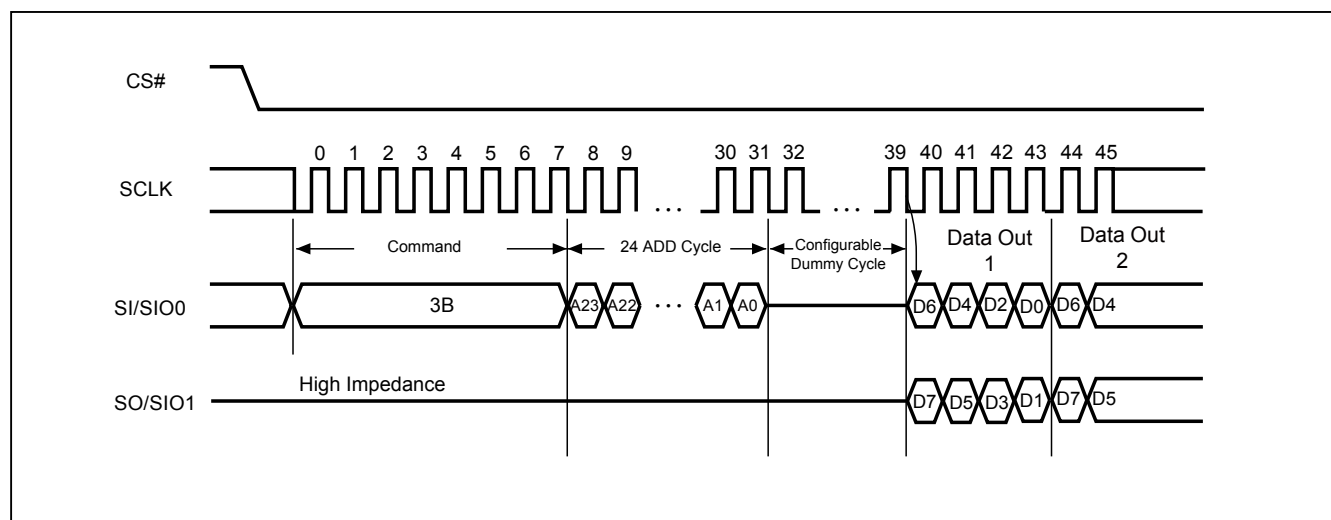
The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing DREAD instruction is: CS# goes low→ sending DREAD instruction→3-byte or 4-byte address on SIO0→ 8 dummy cycles (default) on SIO0→ data out interleave on SIO1 & SIO0→ to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 34. Dual Read Mode Sequence



Notes:

1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

10-15. 2 x I/O Read Mode (2READ)

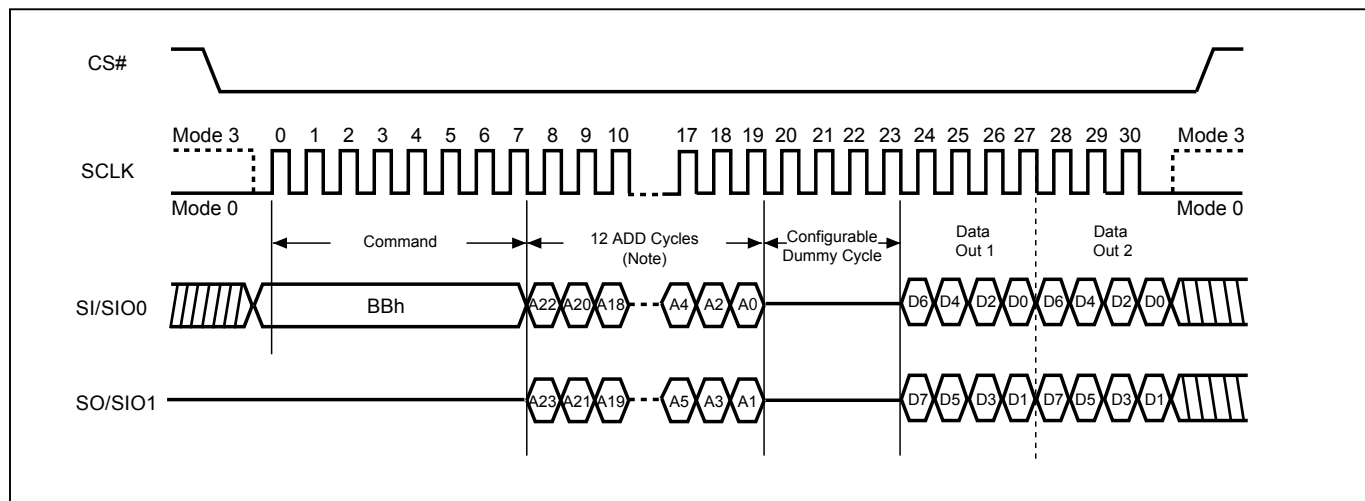
The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency f_T . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing 2READ instruction is: CS# goes low → sending 2READ instruction → 3-byte or 4-byte address interleave on SIO1 & SIO0 → 4 dummy cycles (default) on SIO1 & SIO0 → data out interleave on SIO1 & SIO0 → to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 35. 2 x I/O Read Mode Sequence (SPI Mode only)



Notes:

1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

10-16. Quad Read Mode (QREAD)

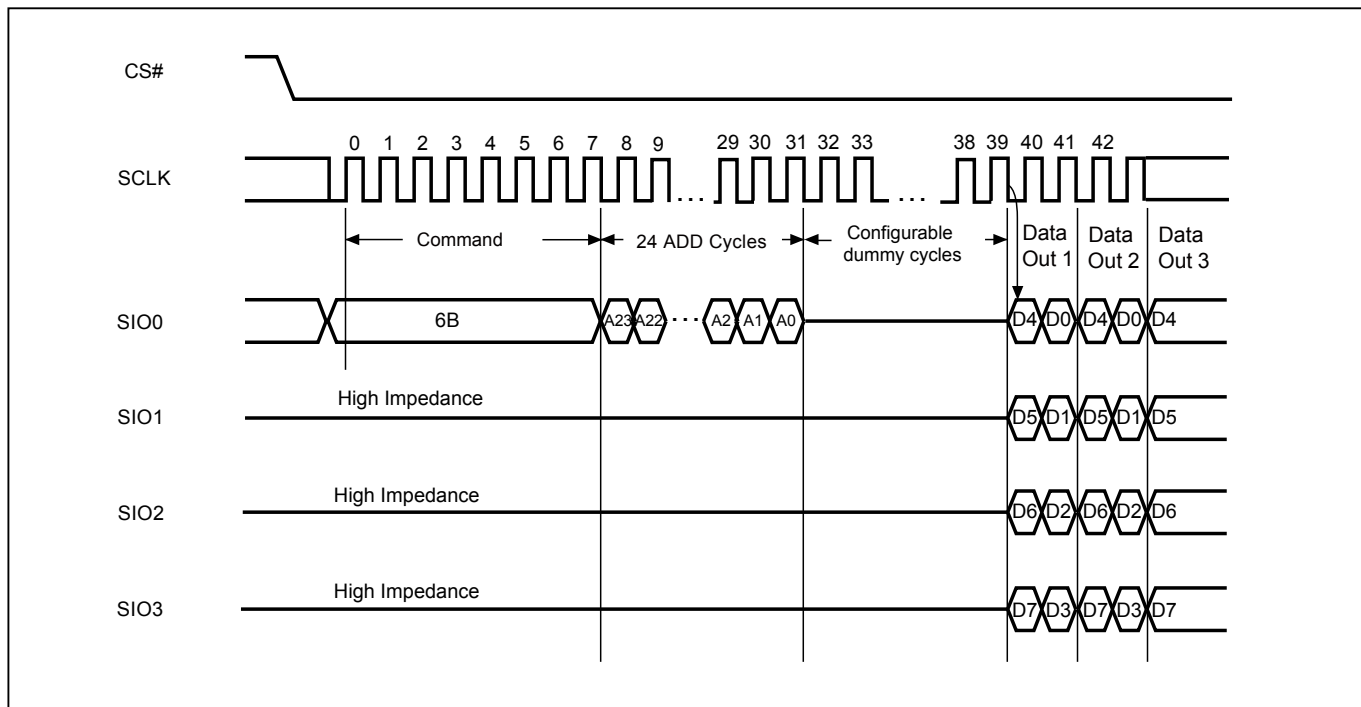
The QREAD instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency f_Q . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing QREAD instruction is: CS# goes low → sending QREAD instruction → 3-byte or 4-byte address on SI → 8 dummy cycle (Default) → data out interleave on SIO3, SIO2, SIO1 & SIO0 → to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 36. Quad Read Mode Sequence



Notes:

1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

10-17. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

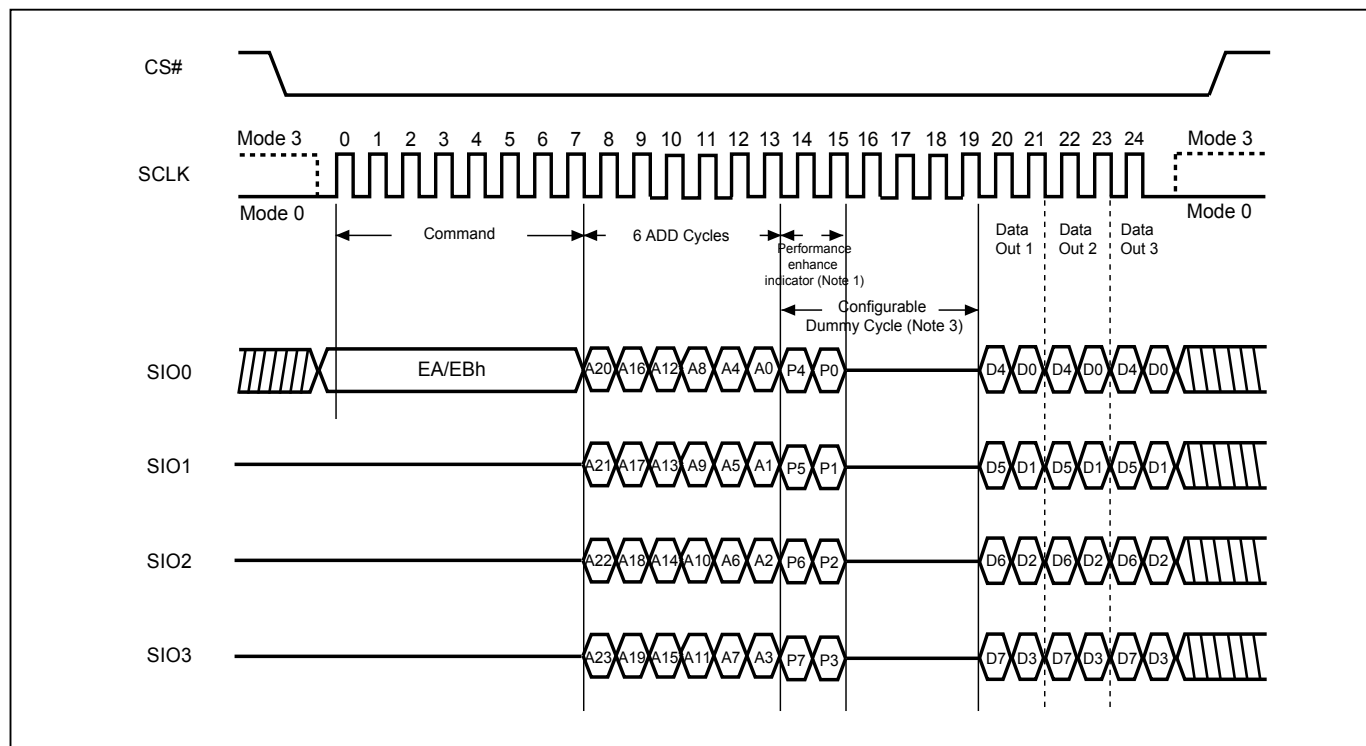
The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 3-byte or 4-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ sending 4READ instruction→ 3-byte or 4-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

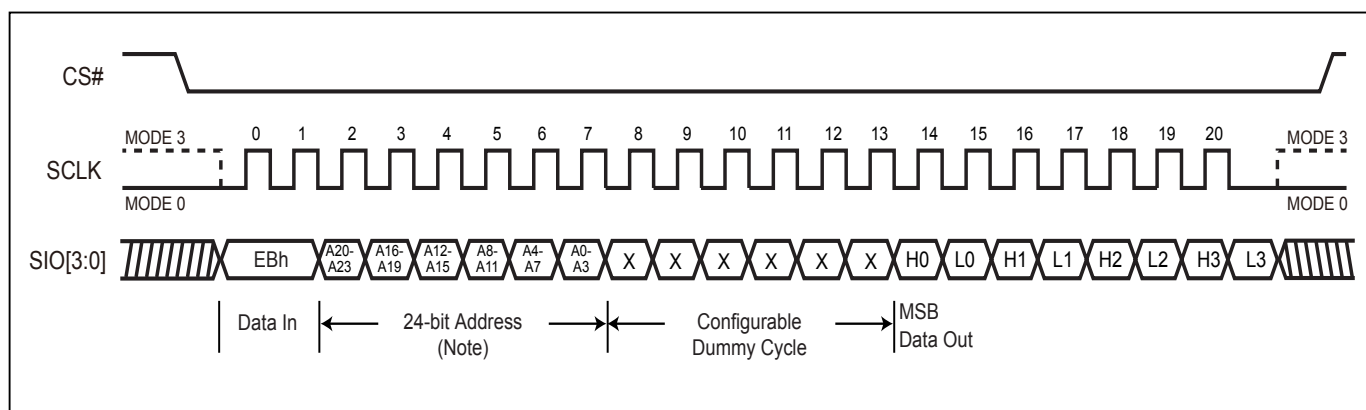
Figure 37. 4 x I/O Read Mode Sequence (SPI Mode)



Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 38. 4 x I/O Read Mode Sequence (QPI Mode)



Notes:

1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

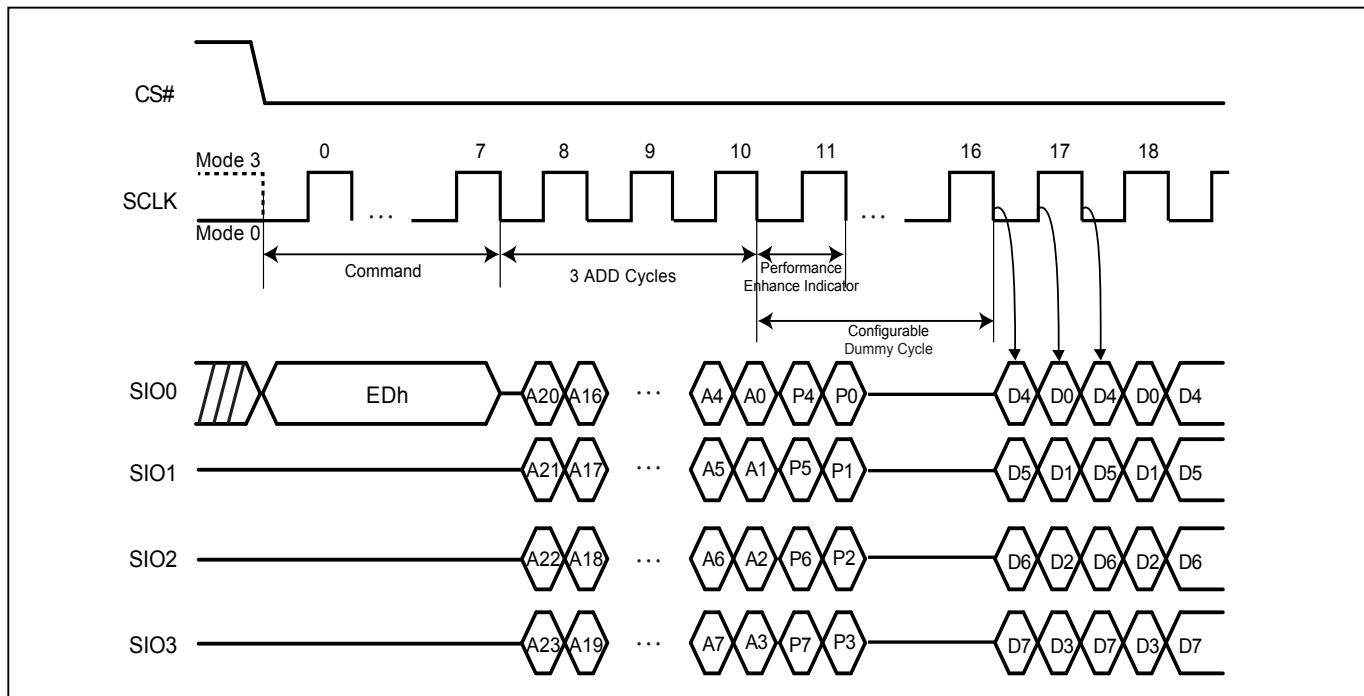
10-18. 4 x I/O Double Transfer Rate Read Mode (4DTRD)

The 4DTRD instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4DTRD instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4DTRD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4DTRD instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

While Program/Erase/Write Status Register cycle is in progress, 4DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

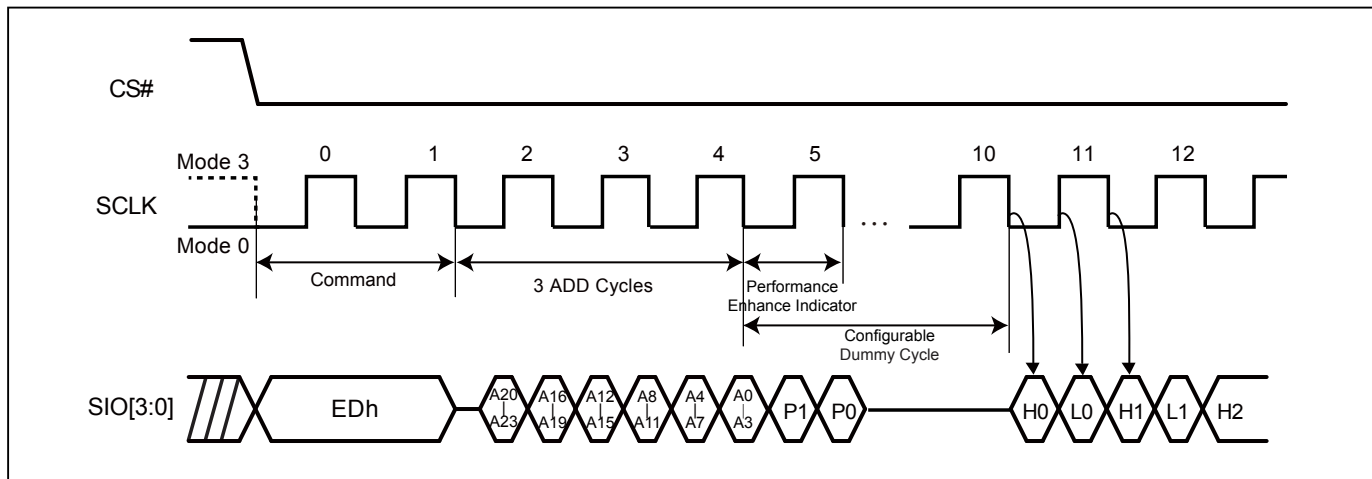
Figure 39. Fast Quad I/O DT Read (4DTRD) Sequence (SPI Mode)



Notes:

1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 40. Fast Quad I/O DT Read (4DTRD) Sequence (QPI Mode)



Notes:

1. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

10-19. Preamble Bit

The Preamble Bit data pattern supports system/memory controller to determine valid window of data output more easily and improve data capture reliability while the flash memory is running in high frequency.

Preamble Bit data pattern can be enabled or disabled by setting the bit4 of Configuration register (Preamble bit Enable bit). Once the CR<4> is set, the preamble bit is inputted into dummy cycles.

Enabling preamble bit will not affect the function of enhance mode bit. In Dummy cycles, performance enhance mode bit still operates with the same function. Preamble bit will output after performance enhance mode bit.

The preamble bit is a fixed 8-bit data pattern (00110100). While dummy cycle number reaches 10, the complete 8 bits will start to output right after the performance enhance mode bit. While dummy cycle is not sufficient of 10 cycles, the rest of the preamble bits will be cut. For example, 8 dummy cycles will cause 6 preamble bits to output, and 6 dummy cycles will cause 4 preamble bits to output.

Figure 41. SDR 1I/O (10DC)

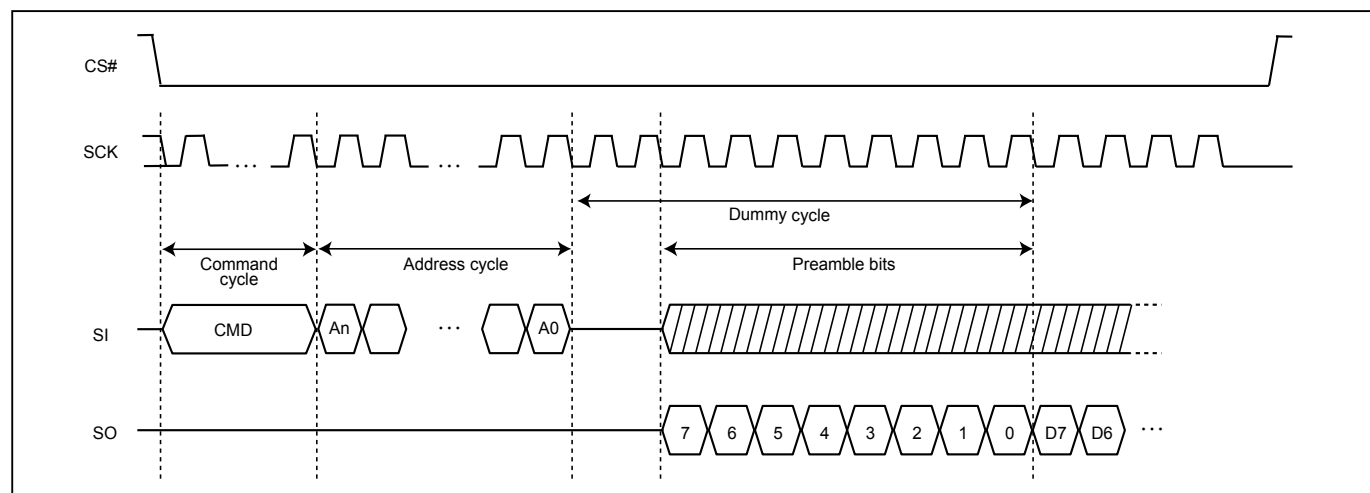


Figure 42. SDR 1I/O (8DC)

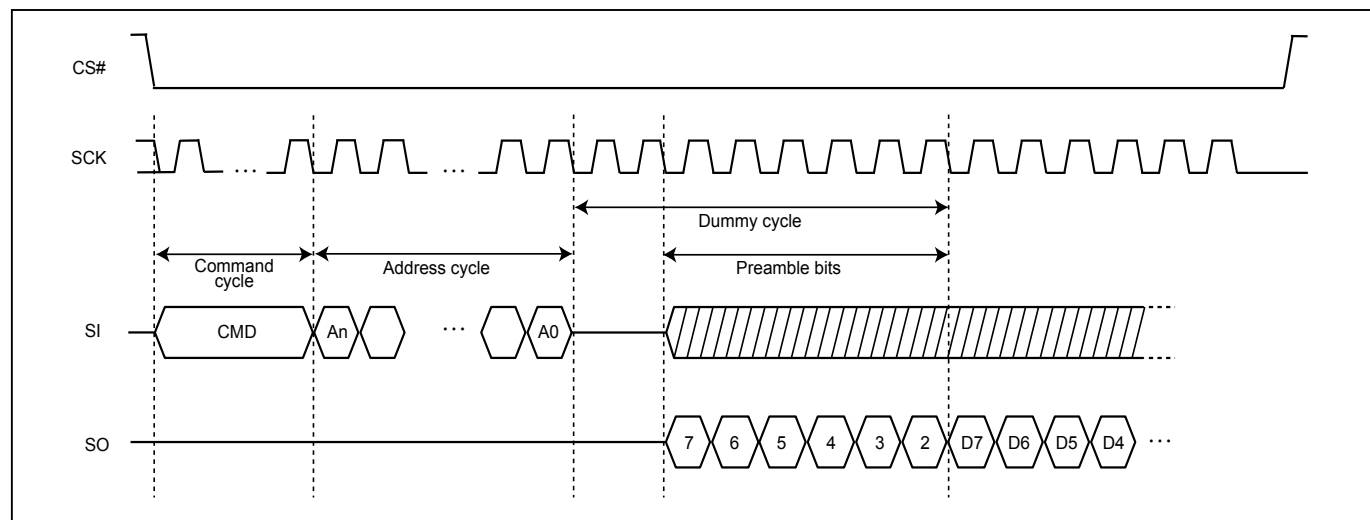


Figure 43. SDR 2I/O (10DC)

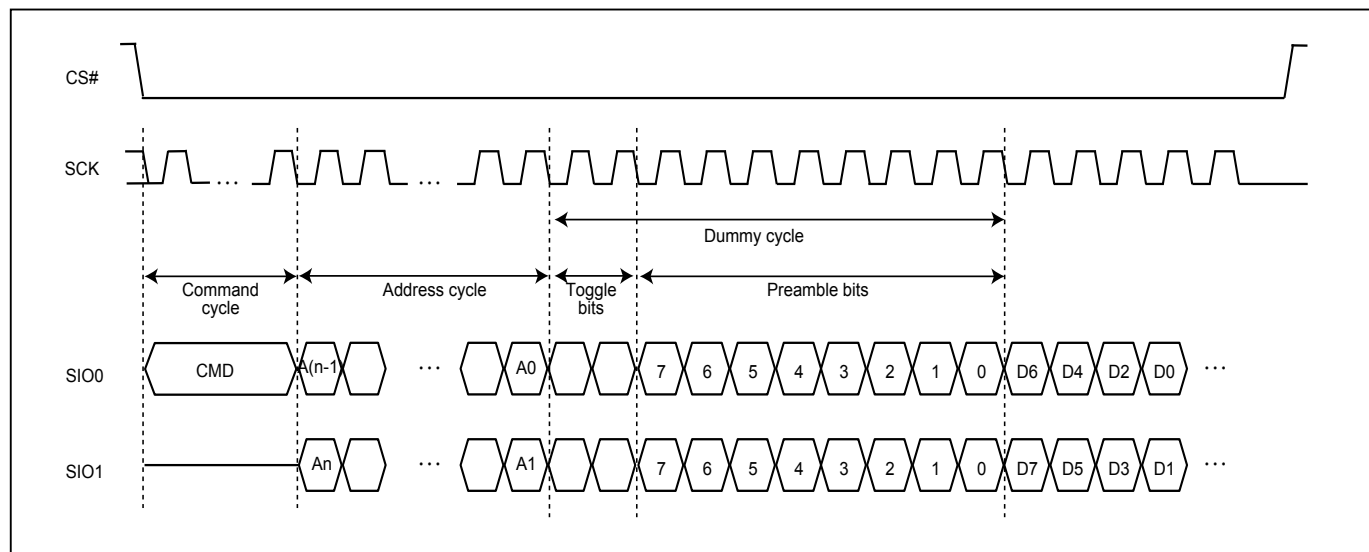


Figure 44. SDR 2I/O (8DC)

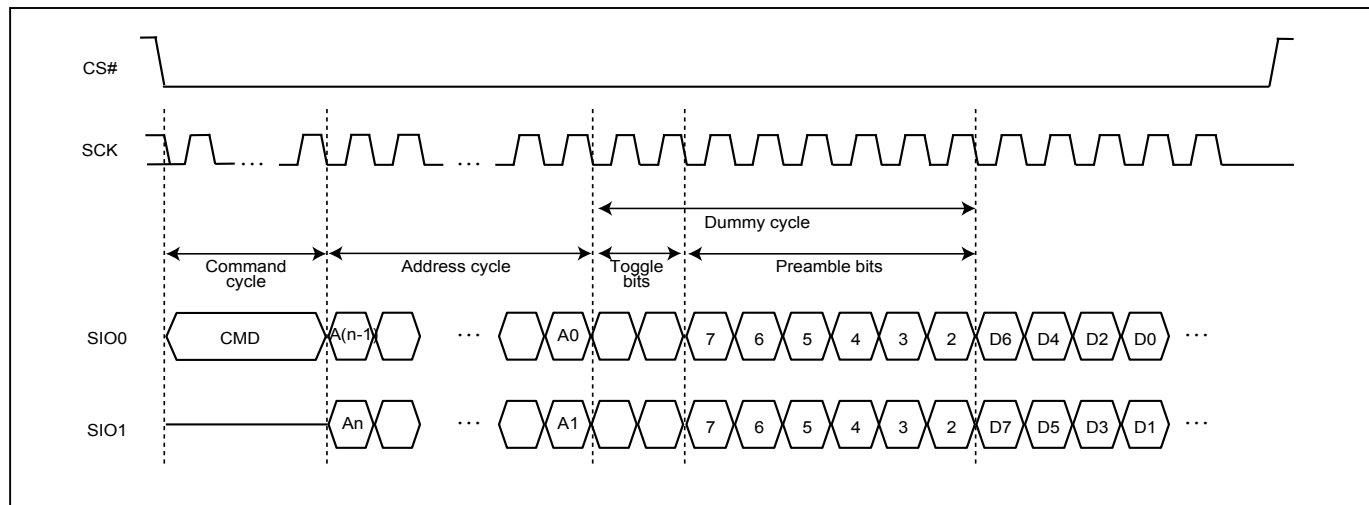


Figure 45. SDR 4I/O (10DC)

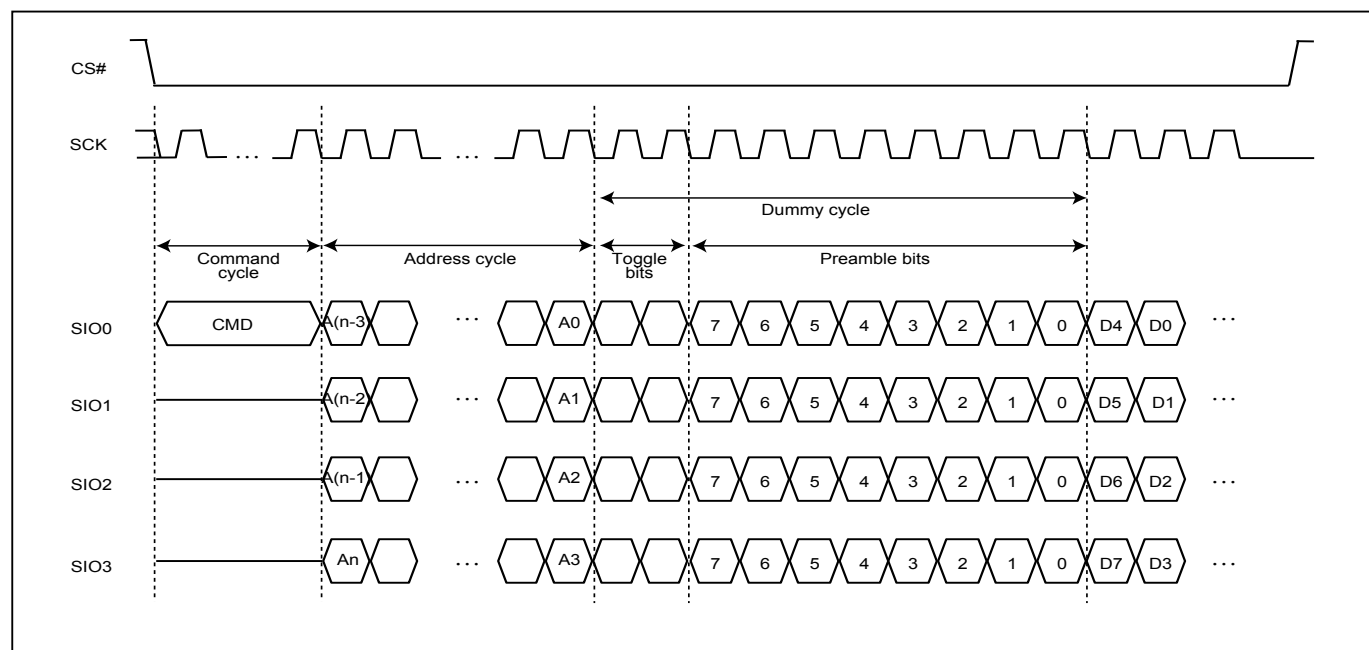


Figure 46. SDR 4I/O (8DC)

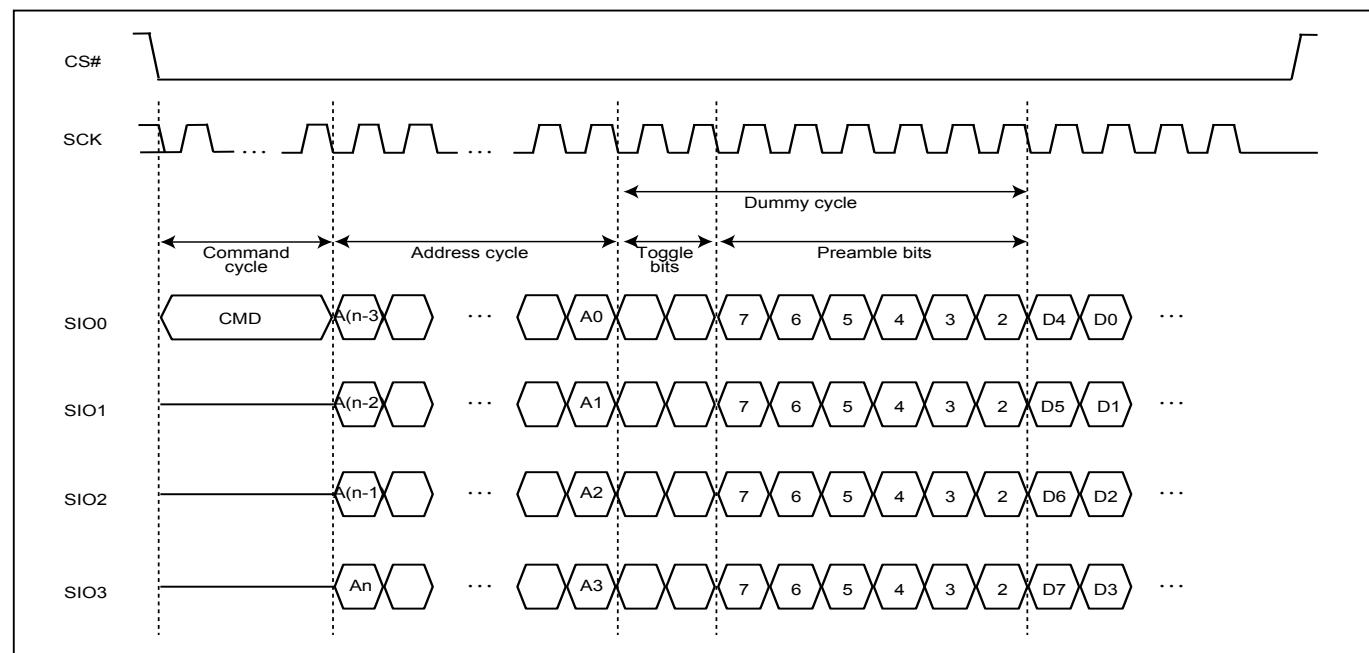
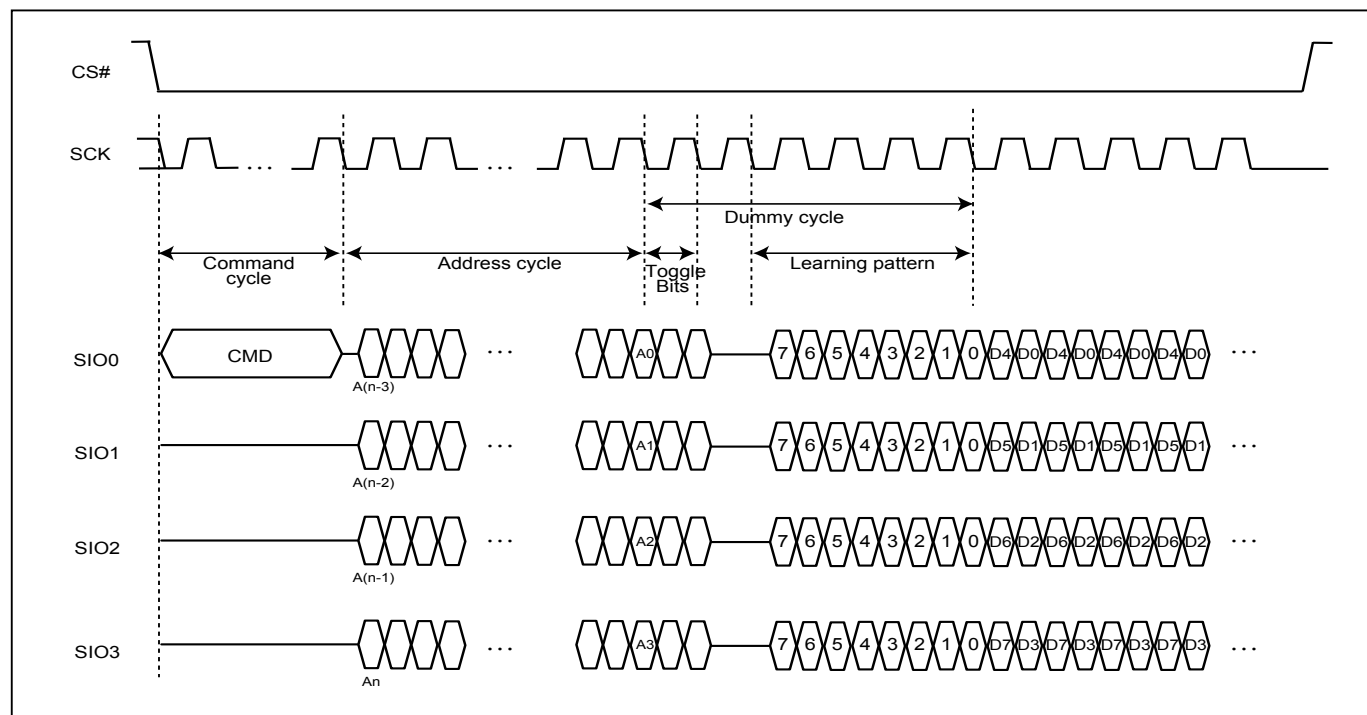


Figure 47. DTR4IO (DC=6)



10-20. 4 Byte Address Command Set

The operation of 4-byte address command set was very similar to original 3-byte address command set. The only different is all the 4-byte command set request 4-byte address (A31-A0) followed by instruction code. The command set support 4-byte address including: READ4B, Fast_Read4B, DREAD4B, 2READ4B, QREAD4B, 4READ4B, 4DTRD4B, PP4B, 4PP4B, SE4B, BE32K4B, BE4B. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Figure 48. Read Data Bytes using 4 Byte Address Sequence (READ4B)

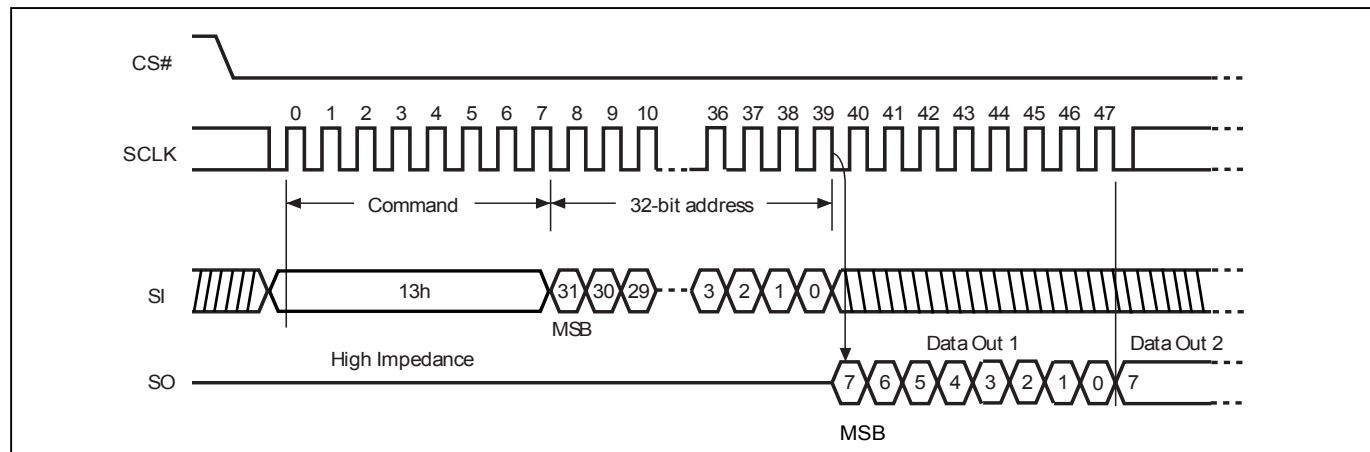
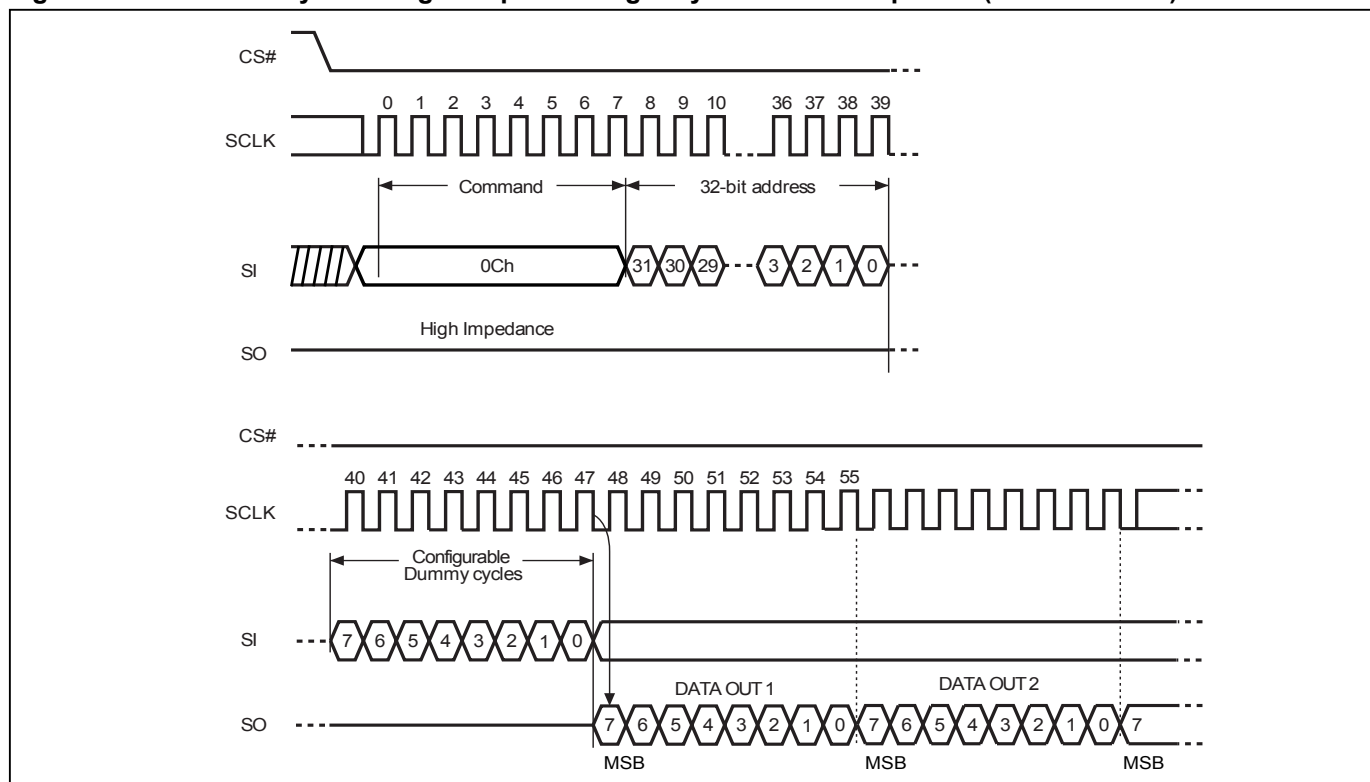


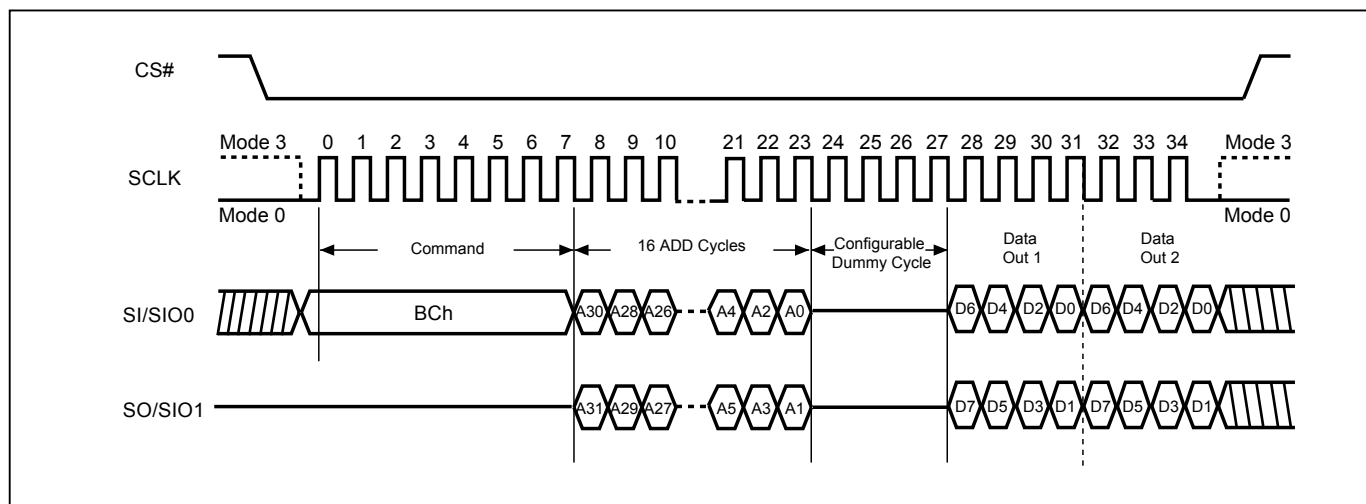
Figure 49. Read Data Bytes at Higher Speed using 4 Byte Address Sequence (FASTREAD4B)



Note:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

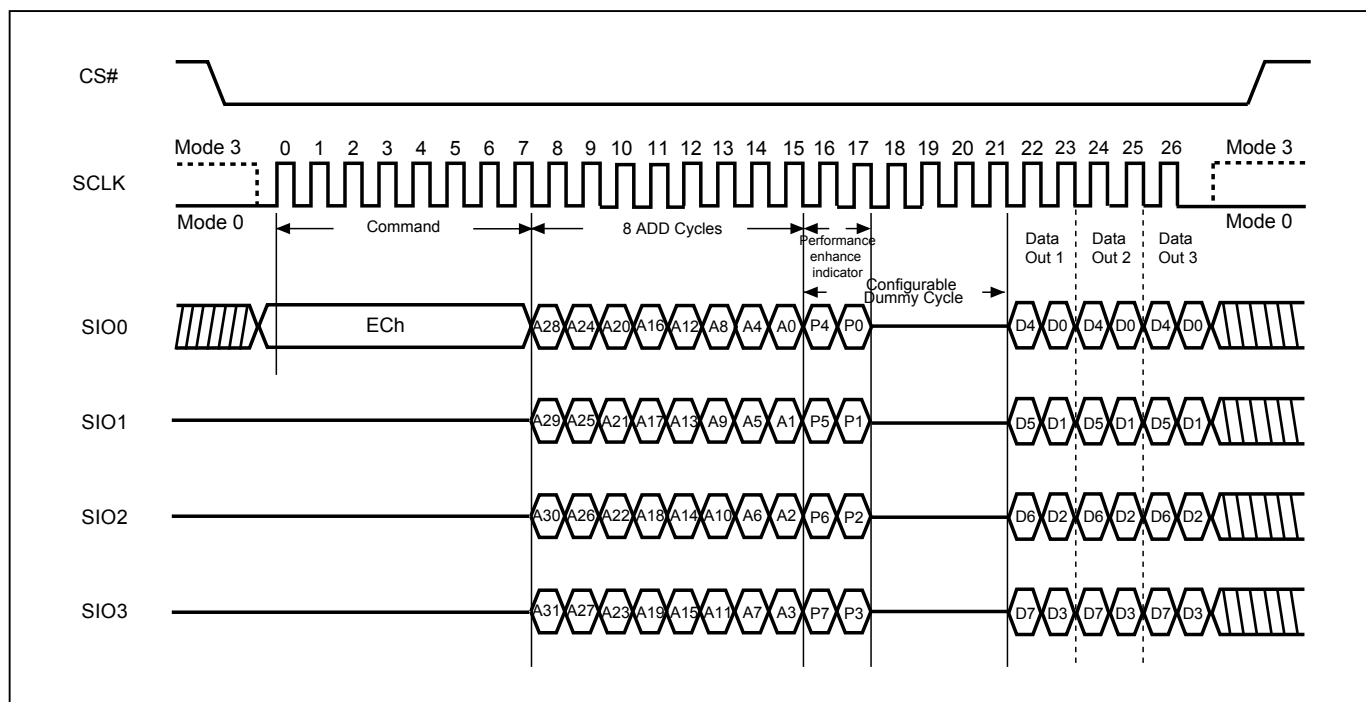
Figure 50. 2 x I/O Fast Read using 4 Byte Address Sequence (2READ4B)



Note:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

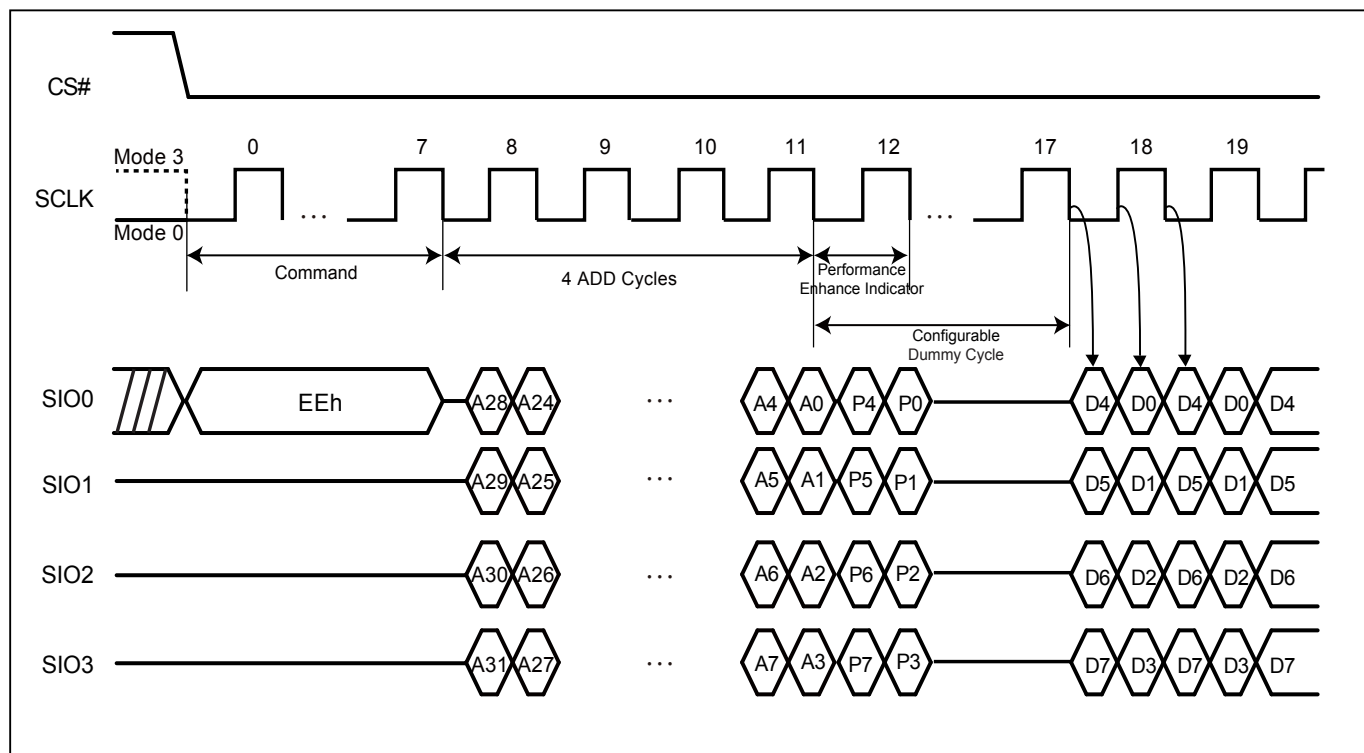
Figure 51. 4 I/O Fast Read using 4 Byte Address sequence (4READ4B)



Note:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

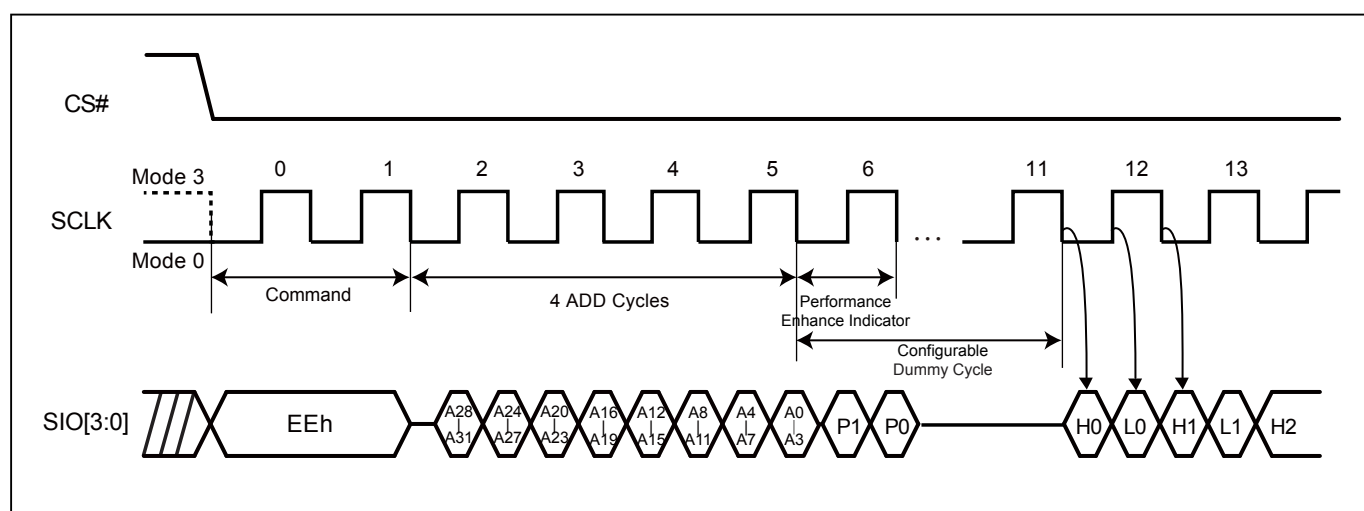
Figure 52. Fast Quad I/O DT Read (4DTRD4B) Sequence (SPI Mode)



Note:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

Figure 53. Fast Quad I/O DT Read (4DTRD4B) Sequence (QPI Mode)



Note:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

Figure 54. Sector Erase (SE4B) Sequence (SPI Mode)

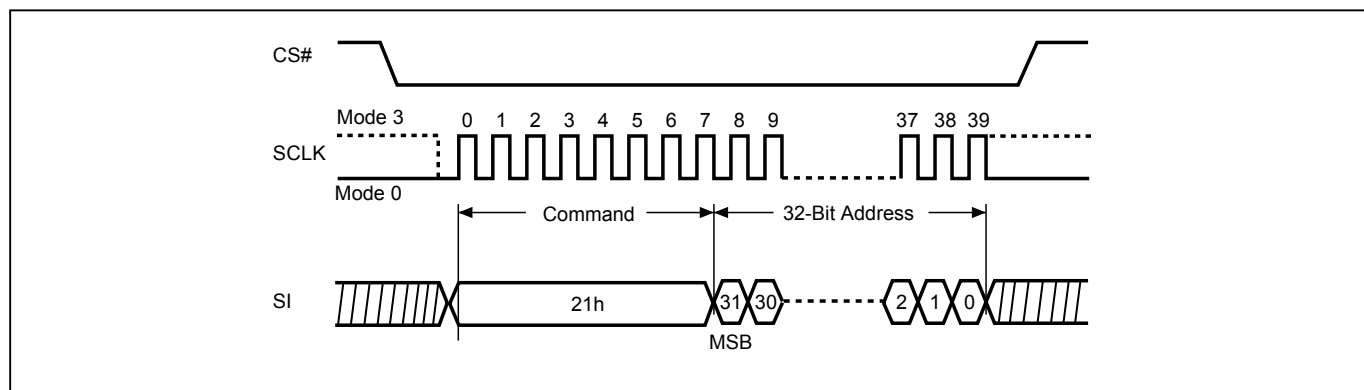


Figure 55. Block Erase 32KB (BE32K4B) Sequence (SPI Mode)

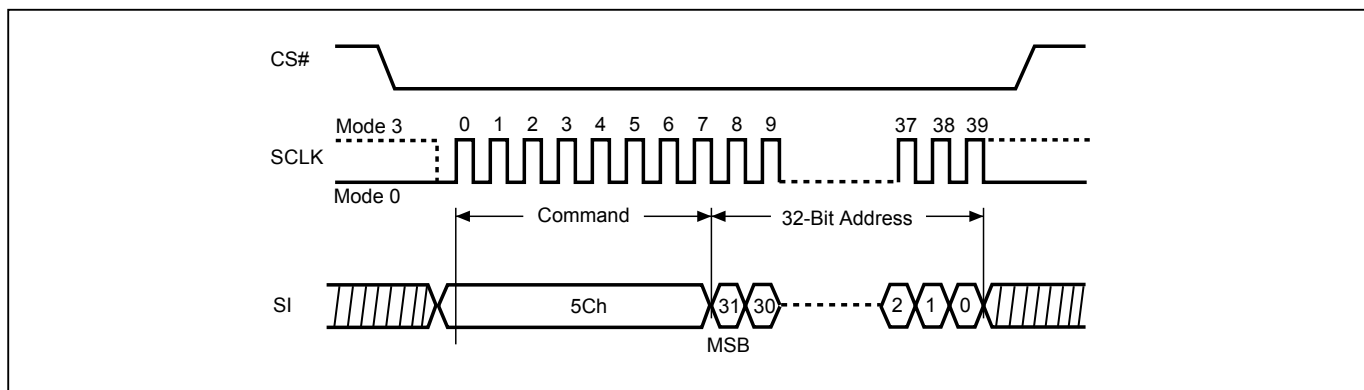


Figure 56. Block Erase (BE4B) Sequence (SPI Mode)

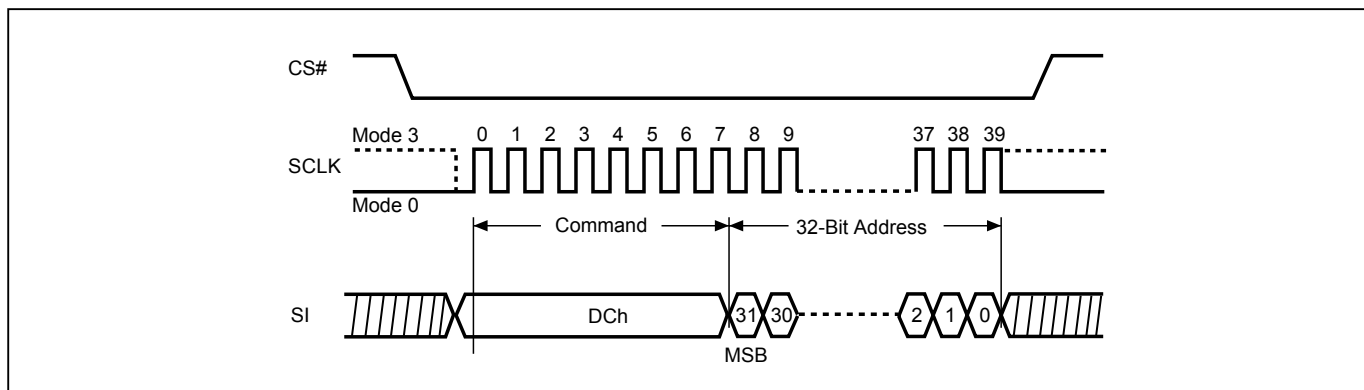


Figure 57. Page Program (PP4B) Sequence (SPI Mode)

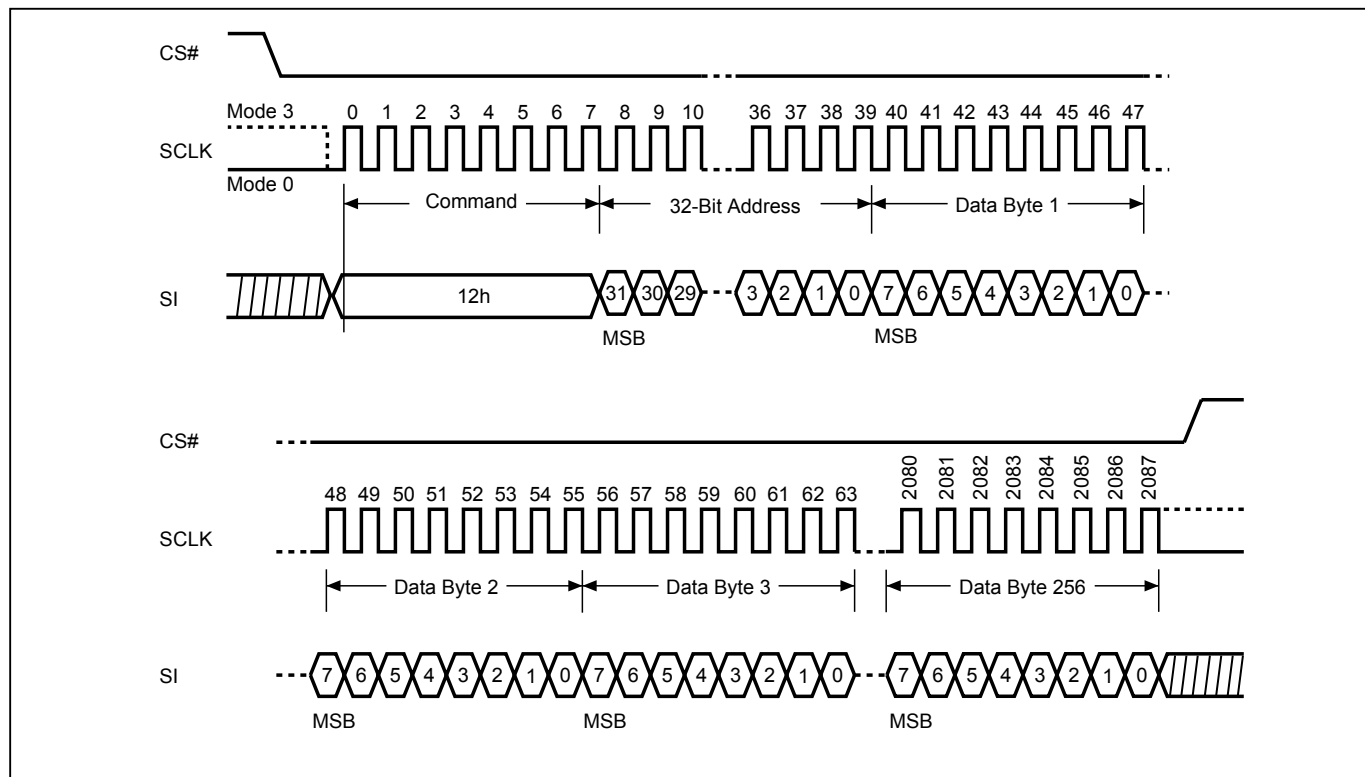
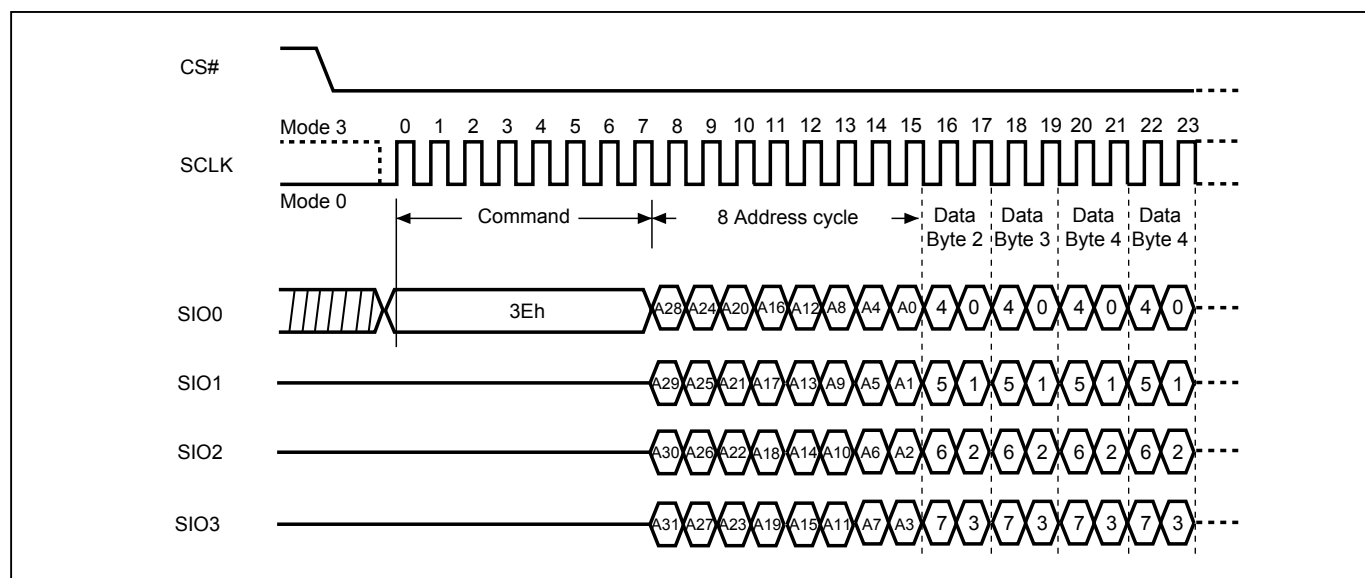


Figure 58. 4 x I/O Page Program (4PP4B) Sequence (SPI Mode only)



10-21. Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

Performance enhance mode is supported in both SPI and QPI mode.

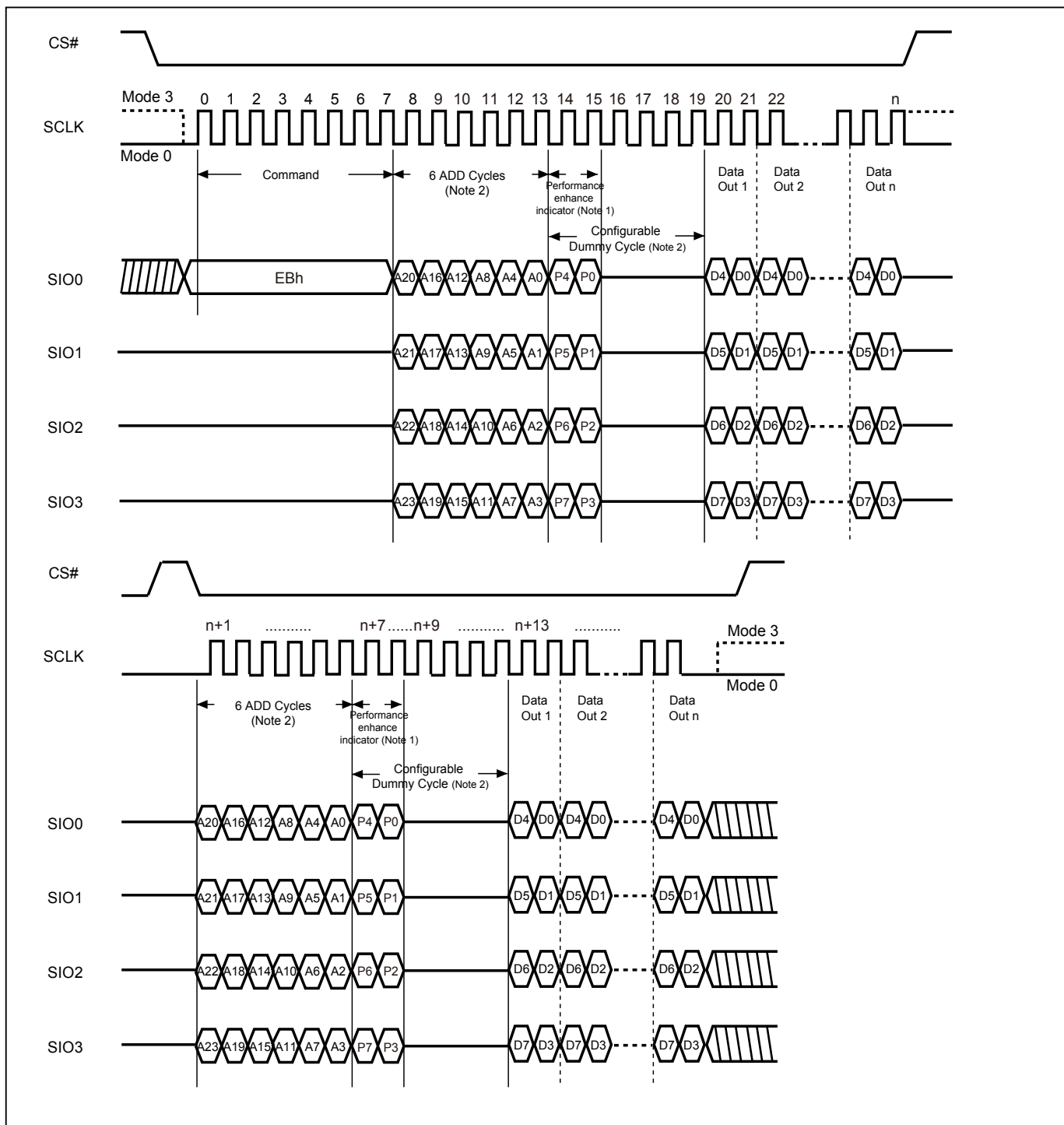
In QPI mode, "EBh" "ECh" "EDh" "EEh" and SPI "EBh" "ECh" "EDh" "EEh" commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

To enter performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and skip the next 4READ instruction. To leave enhance mode, P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h along with CS# is afterwards raised and then lowered. Issuing "FFh" data cycle can also exit enhance mode. The system then will leave performance enhance mode and return to normal operation.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→3-bytes or 4-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles (Default) →data out still CS# goes high → CS# goes low (reduce 4 Read instruction) → 3-bytes or 4-bytes random access address.

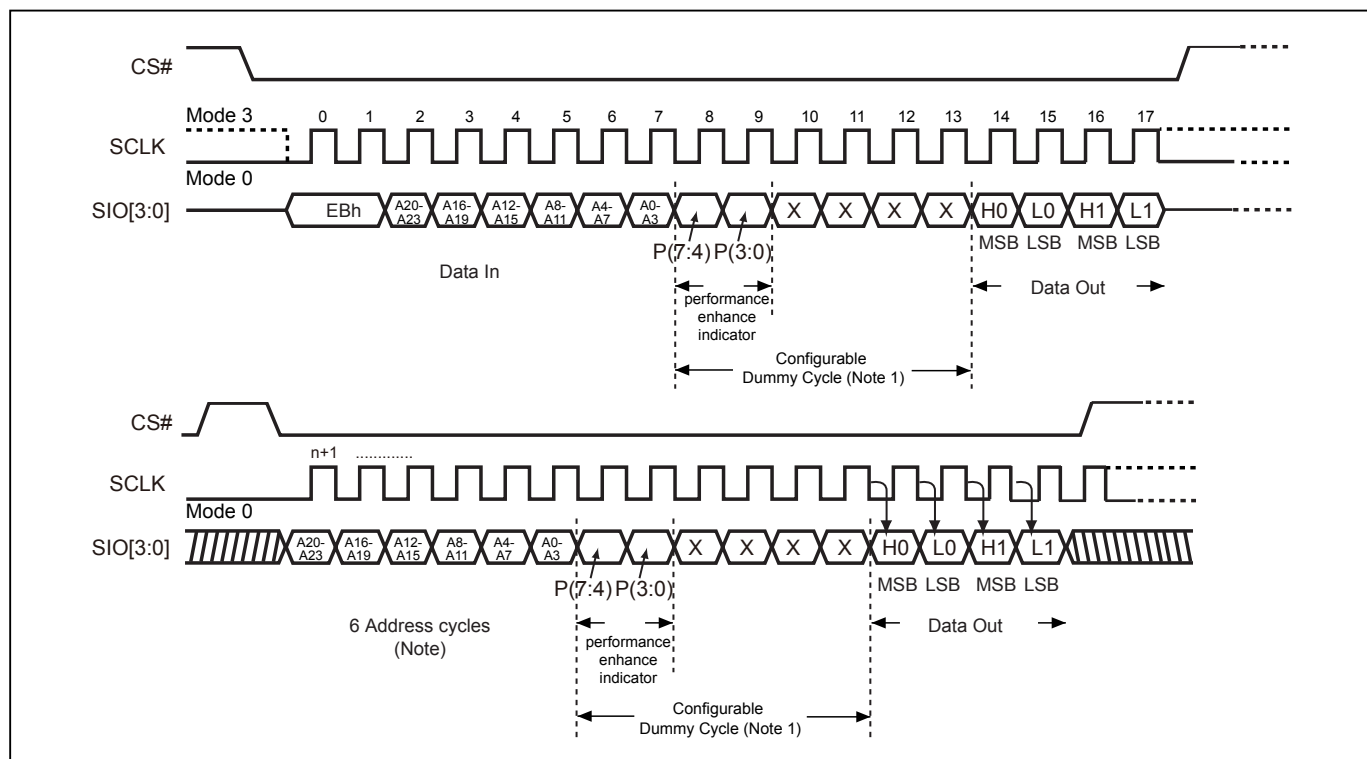
Figure 59. 4 x I/O Read enhance performance Mode Sequence (SPI Mode)



Notes:

1. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
3. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

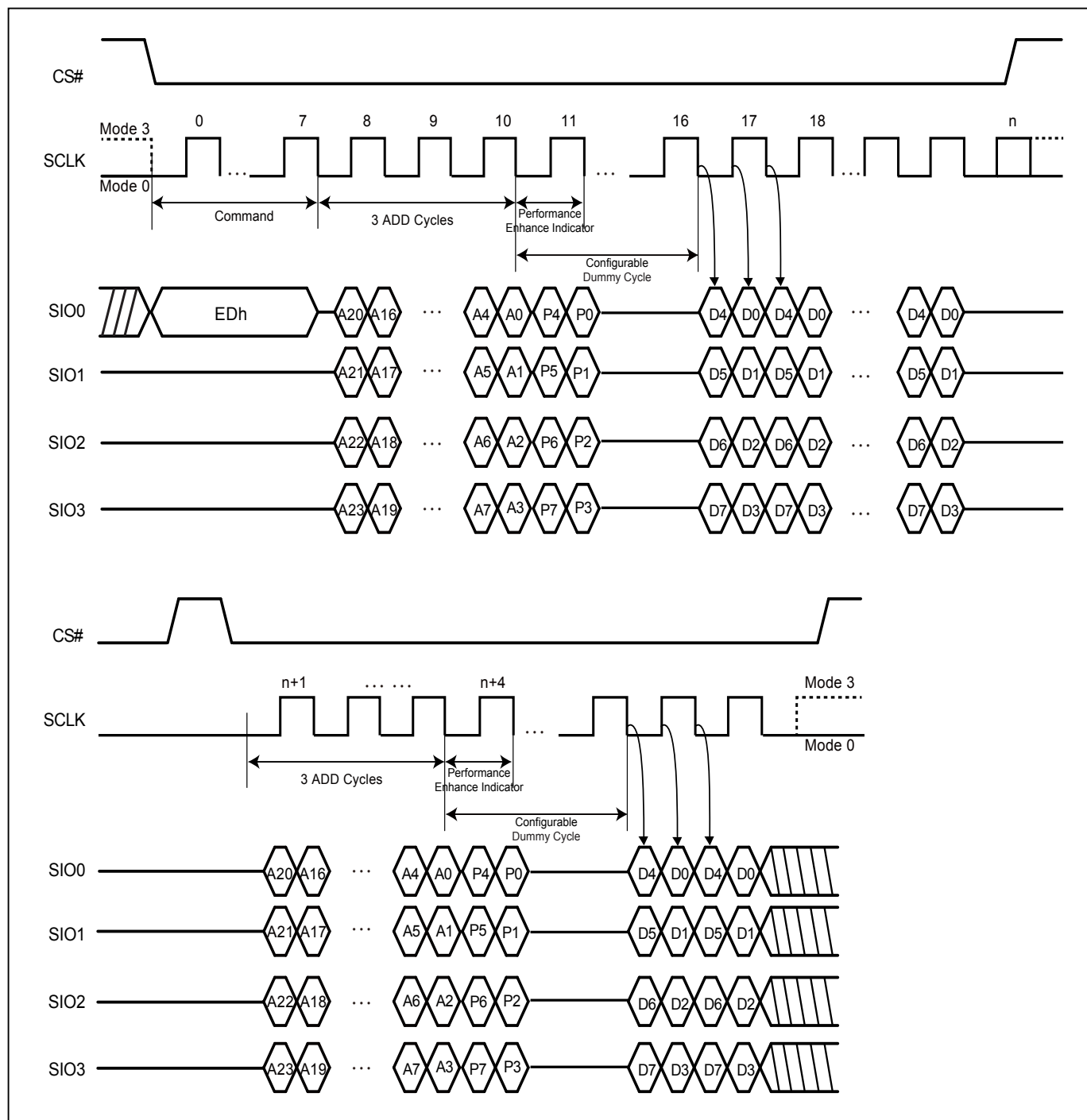
Figure 60. 4 x I/O Read enhance performance Mode Sequence (QPI Mode)



Notes:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
2. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

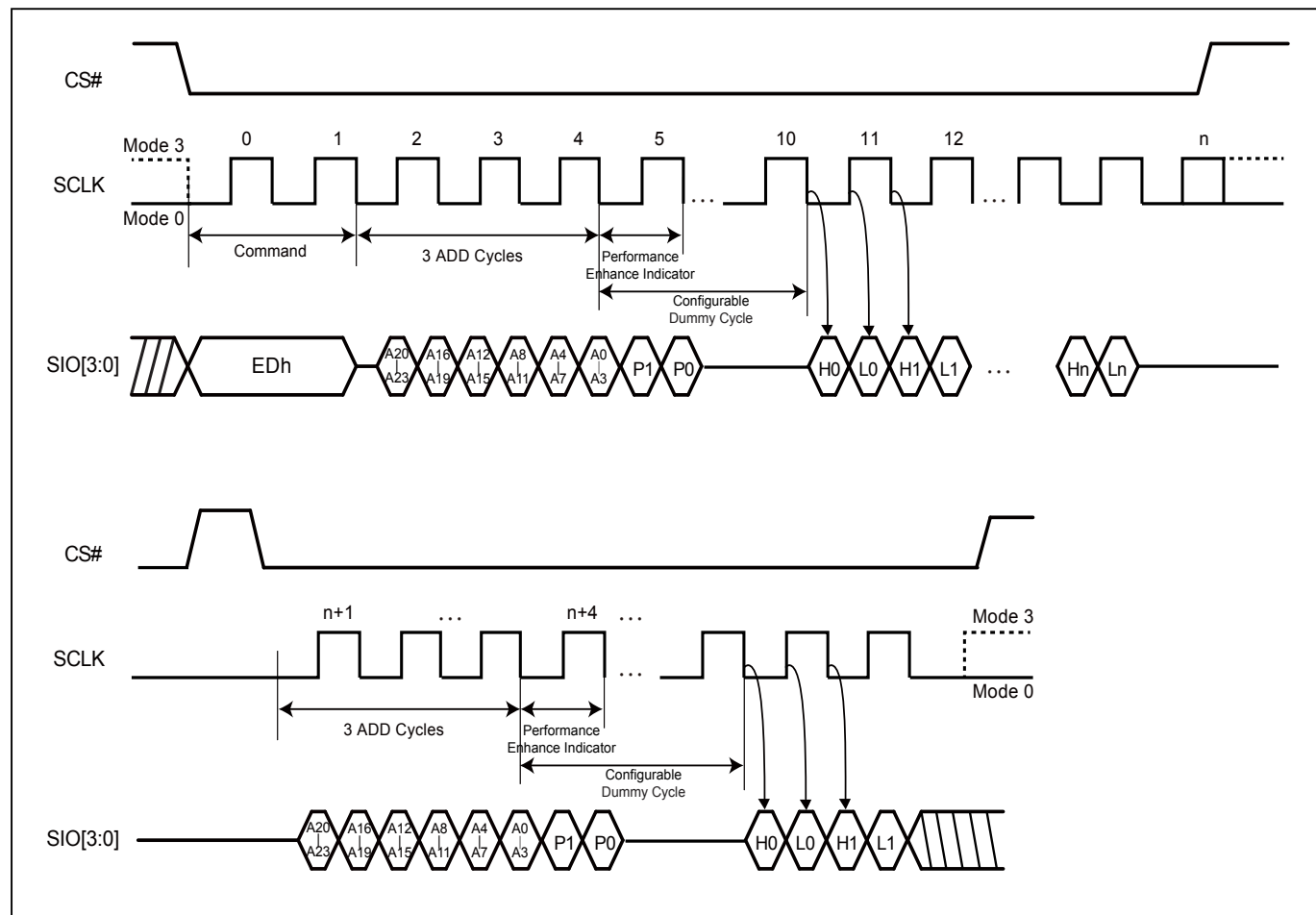
Figure 61. 4 x I/O DT Read enhance performance Mode Sequence (SPI Mode)



Notes:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
2. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 62. 4 x I/O DT Read enhance performance Mode Sequence (QPI Mode)



Notes:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
2. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-22. Performance Enhance Mode Reset

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh data cycle(8 clocks in 3-byte address mode)/3FFh data cycle(10 clocks in 4-byte address mode), should be issued in 1I/O sequence. In QPI Mode, FFFFFFFFh data cycle(8 clocks in 3-byte address mode)/FFFFFFFFh data cycle (10 clocks in 4-byte address mode), in 4I/O should be issued.

If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 63. Performance Enhance Mode Reset for Fast Read Quad I/O (SPI Mode)

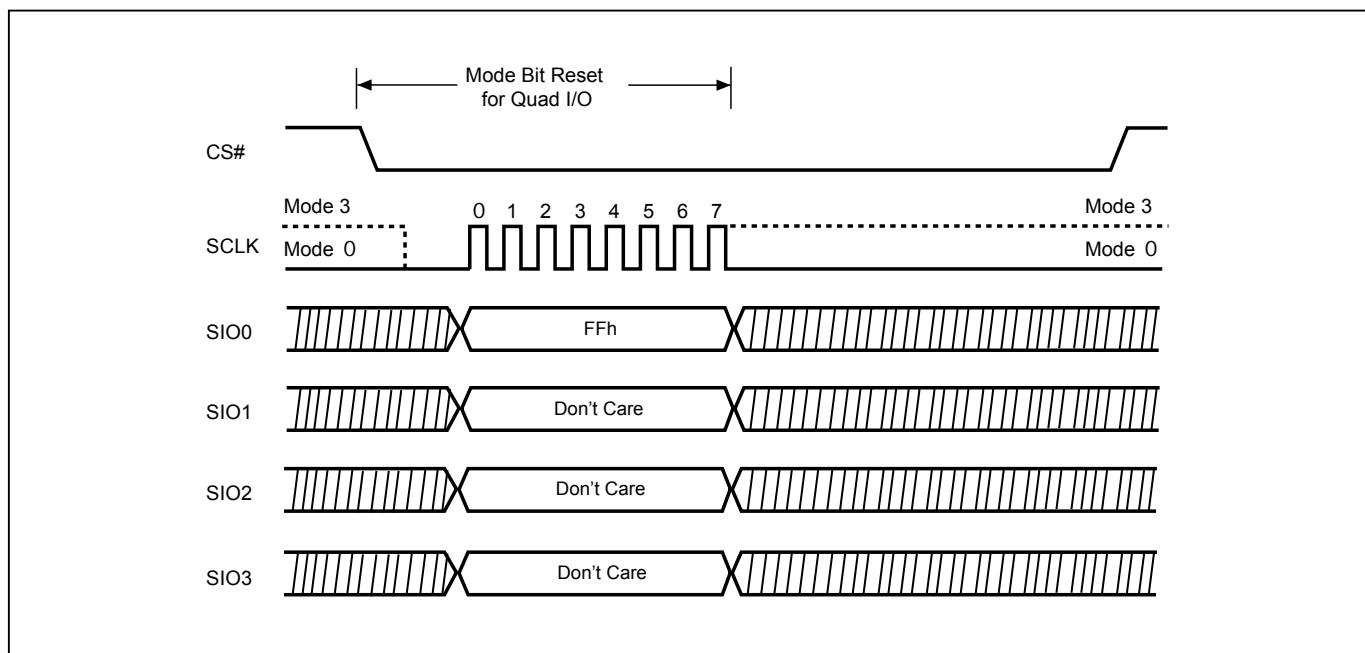


Figure 64. Performance Enhance Mode Reset for Fast Read Quad I/O (QPI Mode)

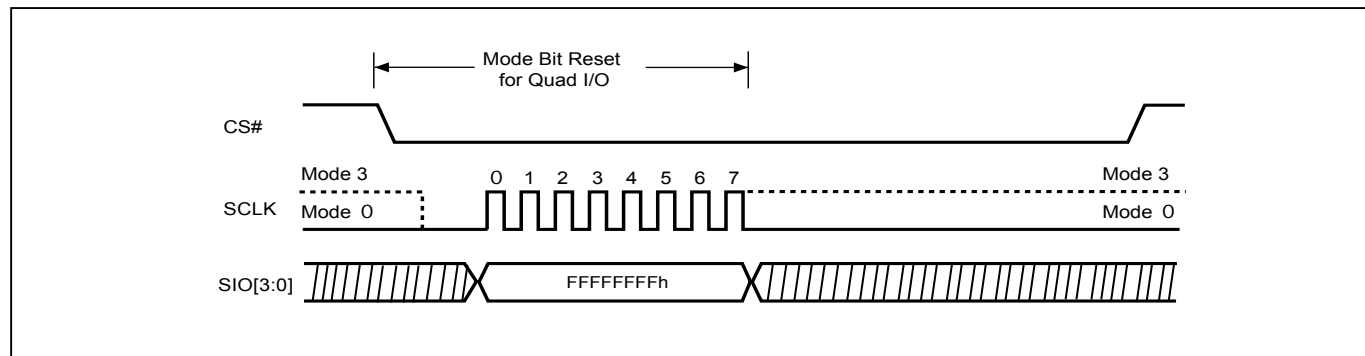


Figure 65. Performance Enhance Mode Reset for Fast Read Quad I/O using 4Byte Address Sequence (SPI Mode)

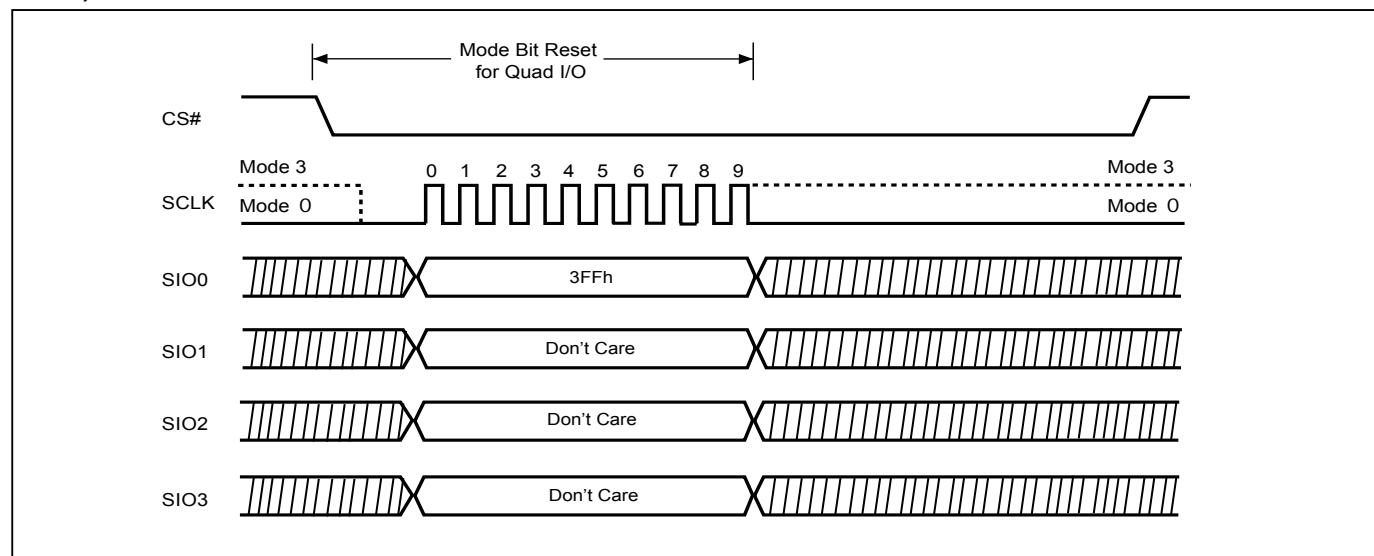
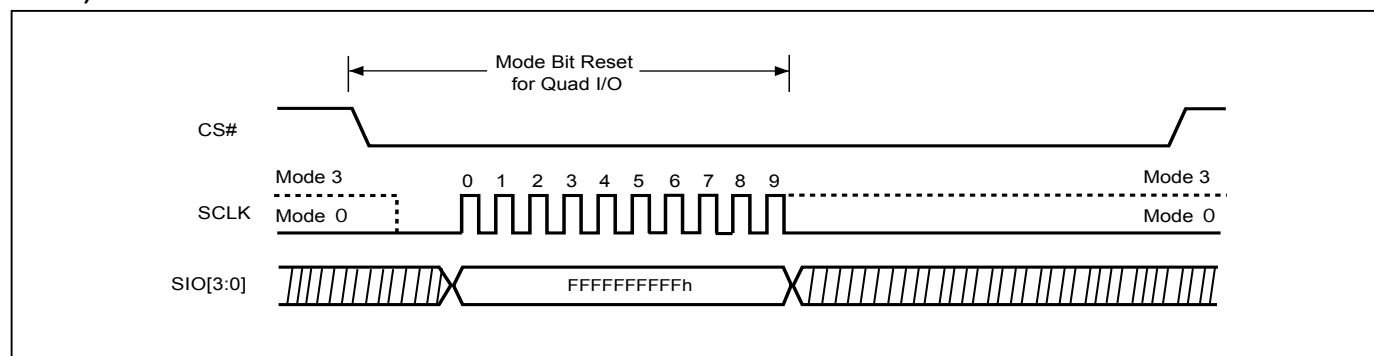


Figure 66. Performance Enhance Mode Reset for Fast Read Quad I/O using 4Byte Address Sequence (QPI Mode)



10-23. Burst Read

To set the Burst length, following command operation is required to issue command: “C0h” in the first Byte (8-clocks), following 4 clocks defining wrap around enable with “0h” and disable with “1h”.

The next 4 clocks are to define wrap around depth. Their definitions are as the following table:

Data	Wrap Around	Wrap Depth
00h	Yes	8-byte
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

The wrap around unit is defined within the 256Byte page, with random initial address. It is defined as “wrap-around mode disable” for the default state of the device. To exit wrap around, it is required to issue another “C0” command in which data=‘1xh’. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is required to issue another “C0” command in which data=“0xh”. QPI “EBh” “ECh” and SPI “EBh” “ECh” support wrap around feature after wrap around is enabled. Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 67. SPI Mode

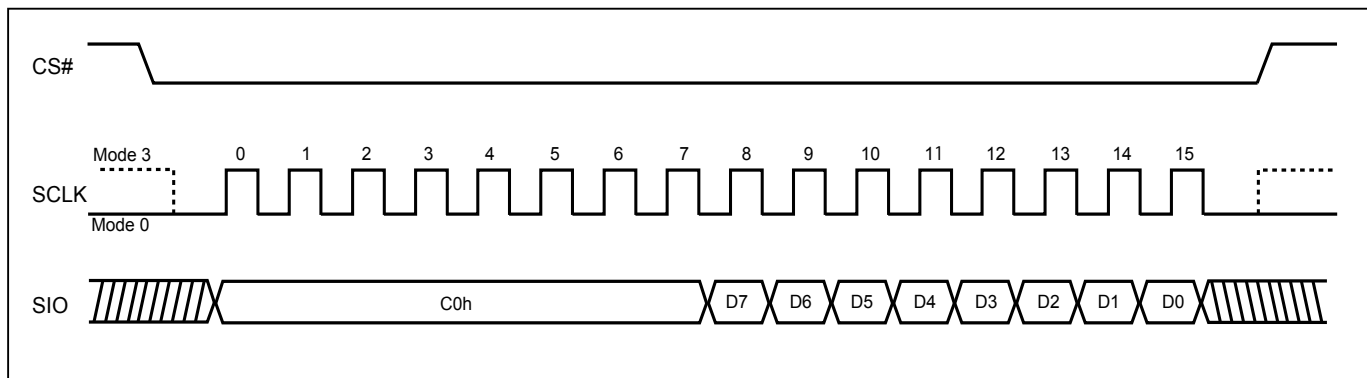
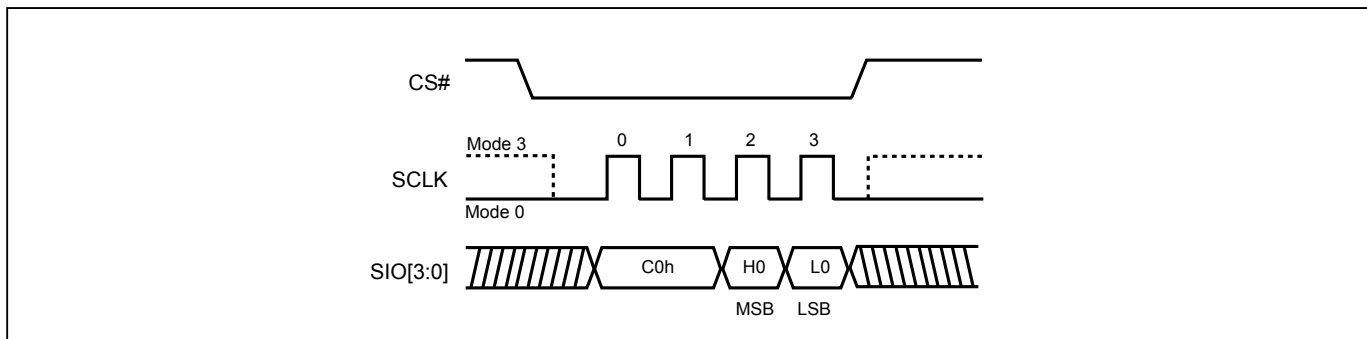


Figure 68. QPI Mode



Note: MSB=Most Significant Bit
LSB=Least Significant Bit

10-24. Fast Boot

The Fast Boot Feature provides the ability to automatically execute read operation after power on cycle or reset without any read instruction.

A Fast Boot Register is provided on this device. It can enable the Fast Boot function and also define the number of delay cycles and start address (where boot code being transferred). Instruction WRFBR (write fast boot register) and ESFBR (erase fast boot register) can be used for the status configuration or alternation of the Fast Boot Register bit. RDFBR (read fast boot register) can be used to verify the program state of the Fast Boot Register. The default number of delay cycles is 13 cycles, and there is a 16bytes boundary address for the start of boot code access.

When CS# starts to go low, data begins to output from default address after the delay cycles (default as 13 cycles). After CS# returns to go high, the device will go back to standard SPI mode and user can start to input command. In the fast boot data out process from CS# goes low to CS# goes high, a minimum of one byte must be output.

Once Fast Boot feature has been enabled, the device will automatically start a read operation after power on cycle, reset command, or hardware reset operation.

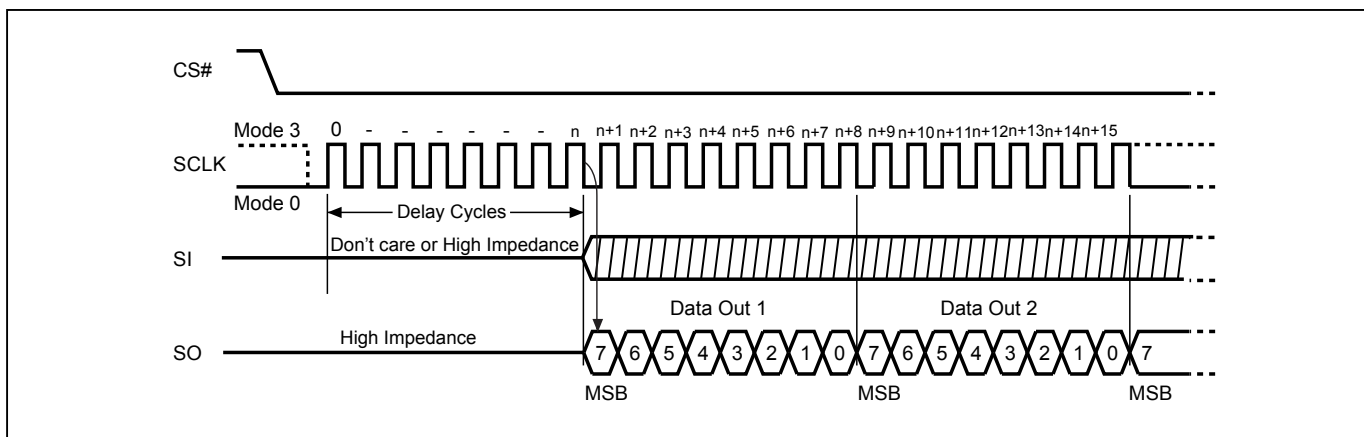
The fast Boot feature can support Single I/O and Quad I/O interface. If the QE bit of Status Register is "0", the data is output by Single I/O interface. If the QE bit of Status Register is set to "1", the data is output by Quad I/O interface.

Fast Boot Register (FBR)

Bits	Description	Bit Status	Default State	Type
31 to 4	FBSA (FastBoot Start Address)	16 bytes boundary address for the start of boot code access.	FFFFFFF	Non-Volatile
3	x		1	Non-Volatile
2 to 1	FBSD (FastBoot Start Delay Cycle)	00: 7 delay cycles 01: 9 delay cycles 10: 11 delay cycles 11: 13 delay cycles	11	Non-Volatile
0	FBE (FastBoot Enable)	0=FastBoot is enabled. 1=FastBoot is not enabled.	1	Non-Volatile

Note: If FBSD = 11, the maximum clock frequency is 133 MHz
If FBSD = 10, the maximum clock frequency is 104 MHz
If FBSD = 01, the maximum clock frequency is 84 MHz
If FBSD = 00, the maximum clock frequency is 70 MHz

Figure 69. Fast Boot Sequence (QE=0)



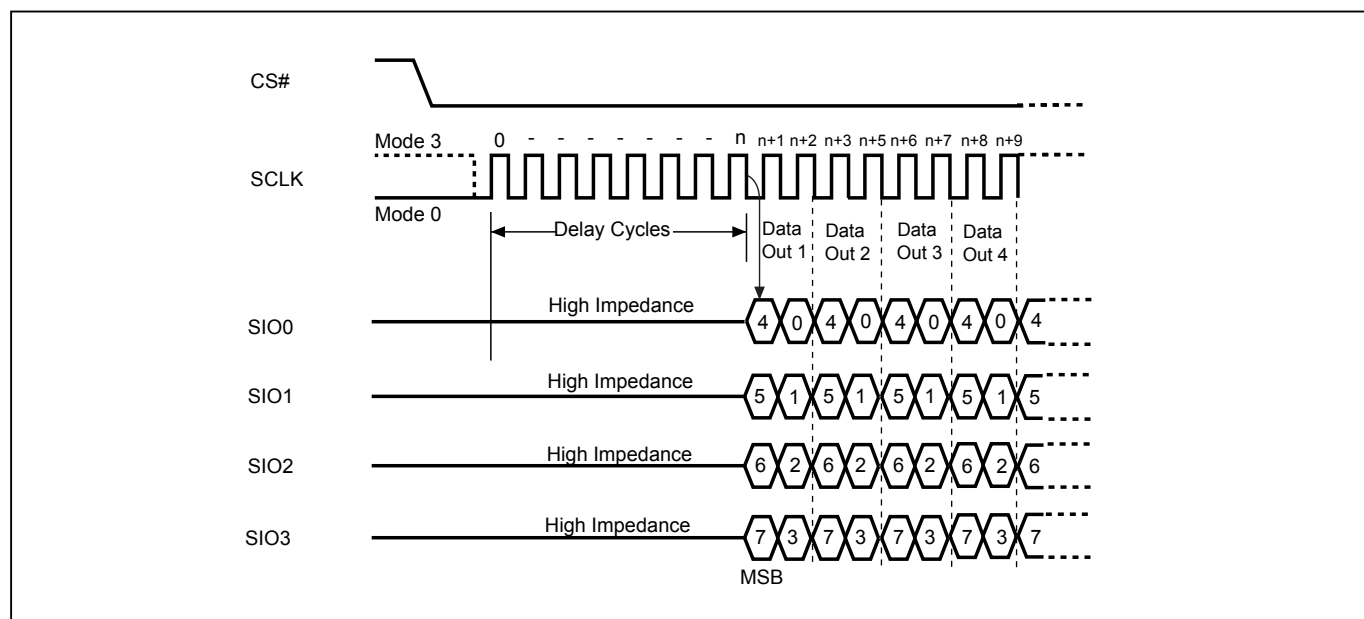
Note: If FBSD = 11, delay cycles is 13 and n is 12.

If FBSD = 10, delay cycles is 11 and n is 10.

If FBSD = 01, delay cycles is 9 and n is 8.

If FBSD = 00, delay cycles is 7 and n is 6.

Figure 70. Fast Boot Sequence (QE=1)



Note: If FBSD = 11, delay cycles is 13 and n is 12.

If FBSD = 10, delay cycles is 11 and n is 10.

If FBSD = 01, delay cycles is 9 and n is 8.

If FBSD = 00, delay cycles is 7 and n is 6.

Figure 71. Read Fast Boot Register (RDFBR) Sequence

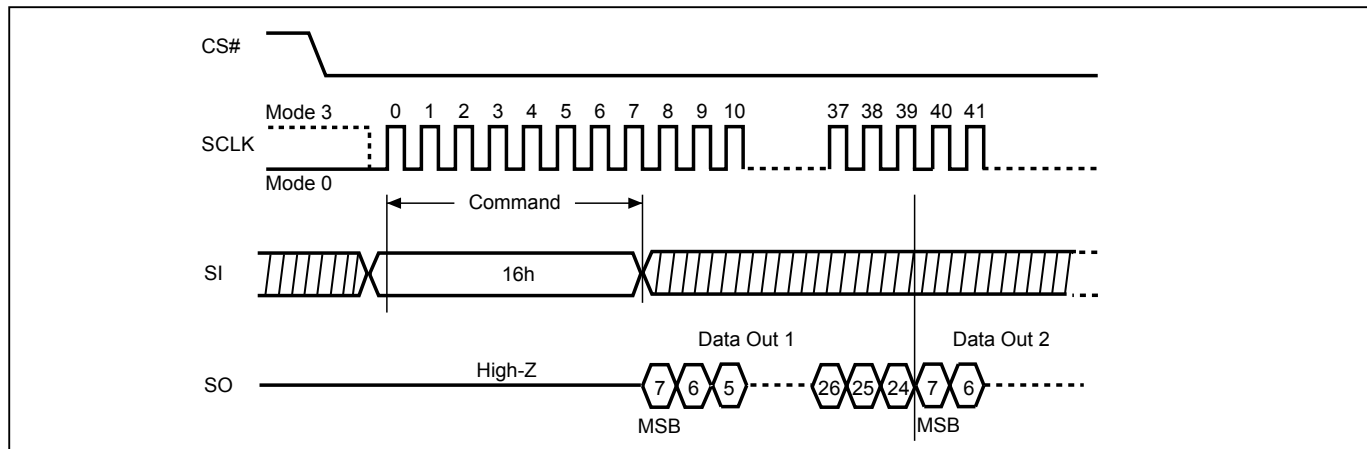


Figure 72. Write Fast Boot Register (WRFBR) Sequence

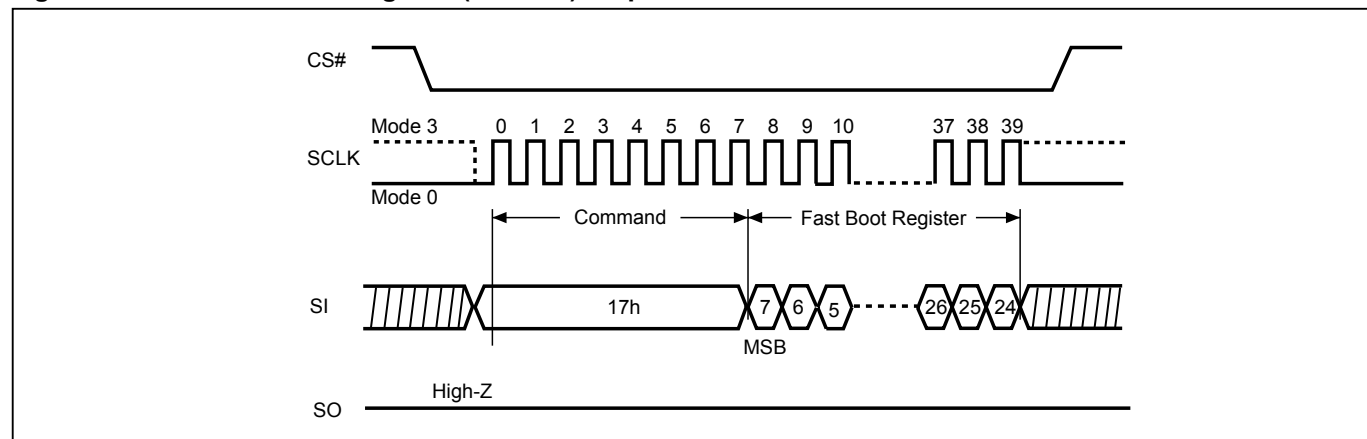
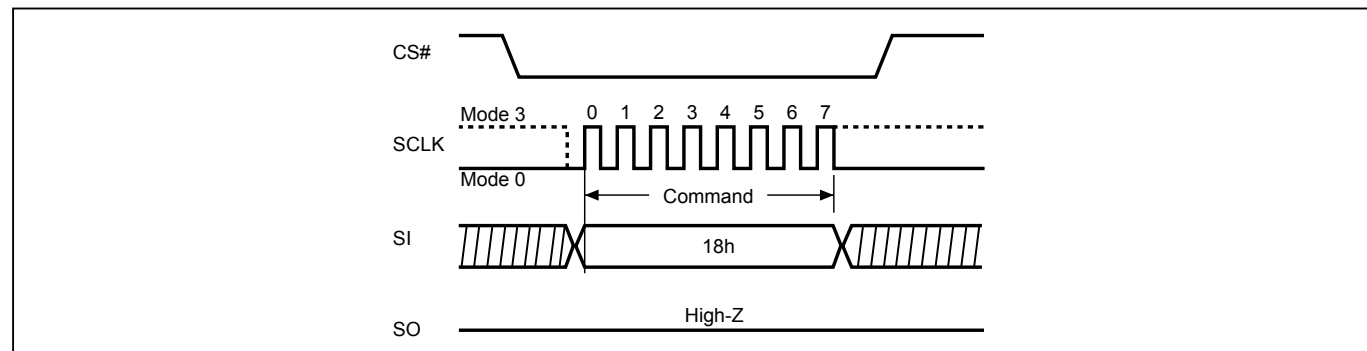


Figure 73. Erase Fast Boot Register (ESFBR) Sequence



10-25. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to "5. MEMORY ORGANIZATION") is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. Address bits [Am-A12] (Am is the most significant address) select the sector address.

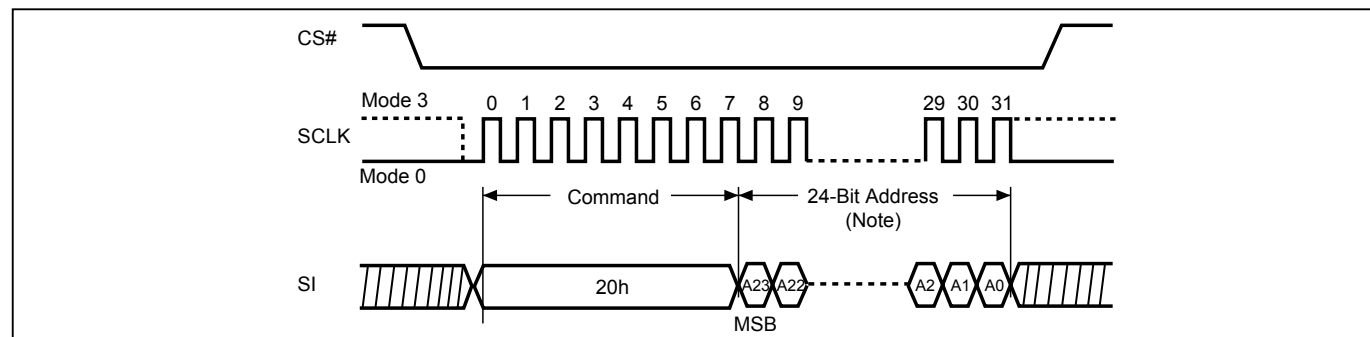
To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte or 4-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

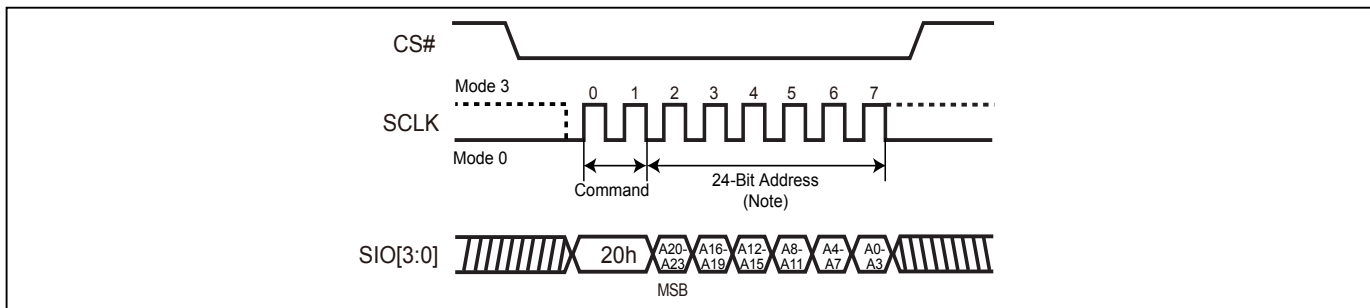
The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Sector Erase (SE) instruction will not be executed on the block.

Figure 74. Sector Erase (SE) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 75. Sector Erase (SE) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-26. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (Please refer to "5. MEMORY ORGANIZATION") is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

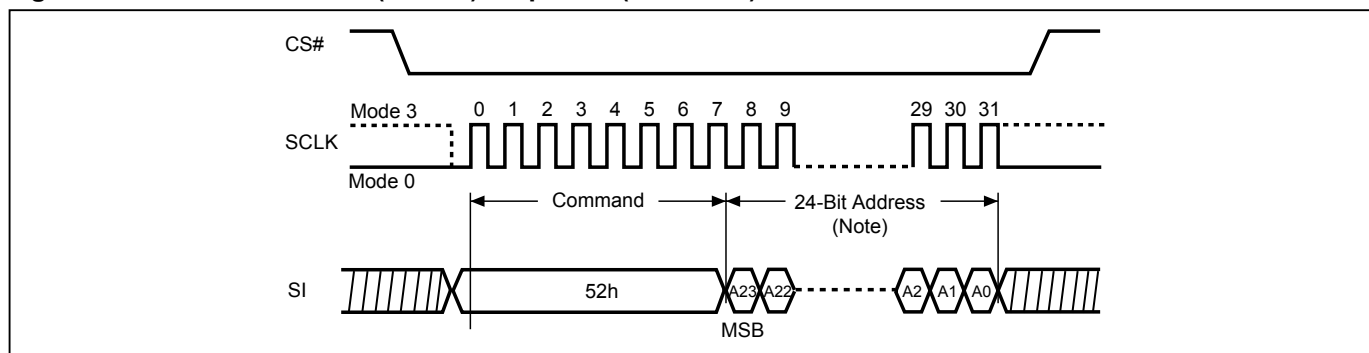
Address bits [Am-A15] (Am is the most significant address) select the 32KB block address. The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing BE32K instruction is: CS# goes low→ sending BE32K instruction code→ 3-byte or 4-byte address on SI→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

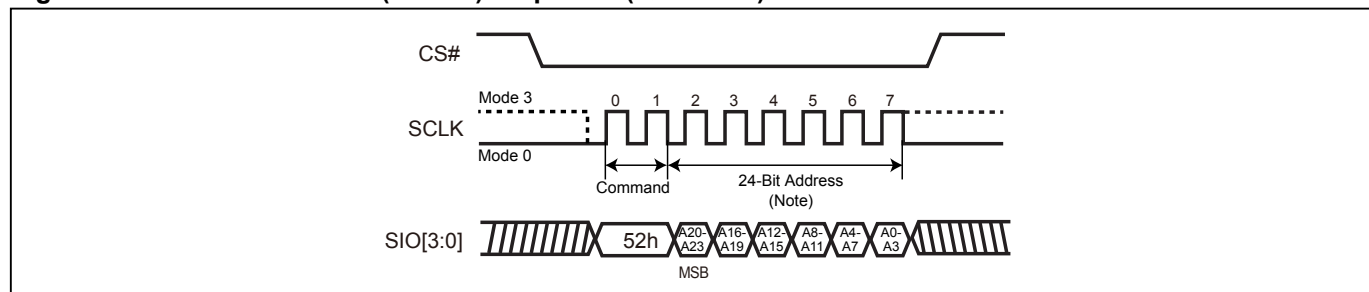
The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while during the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Block Erase (BE32K) instruction will not be executed on the block.

Figure 76. Block Erase 32KB (BE32K) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 77. Block Erase 32KB (BE32K) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-27. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to "5. MEMORY ORGANIZATION") is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

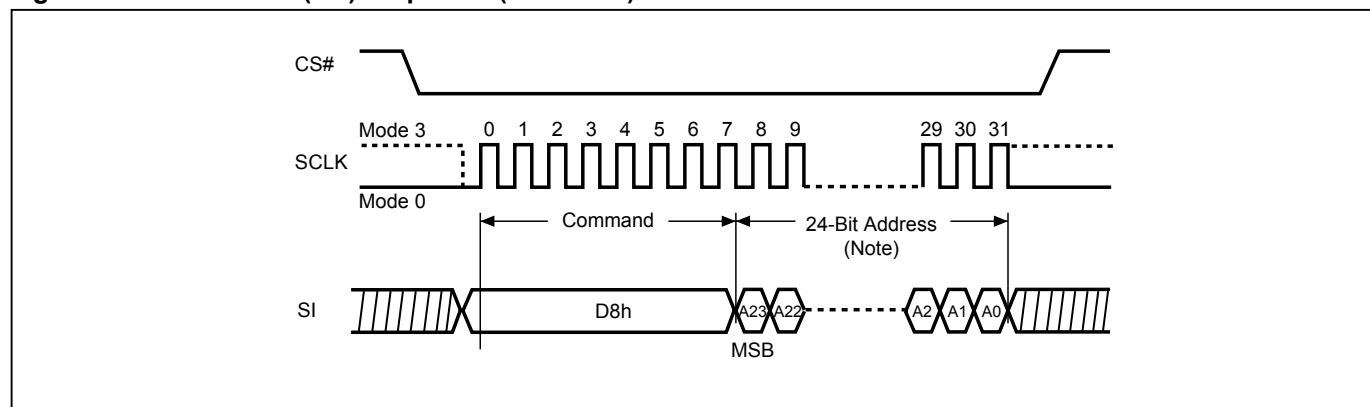
The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte or 4-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

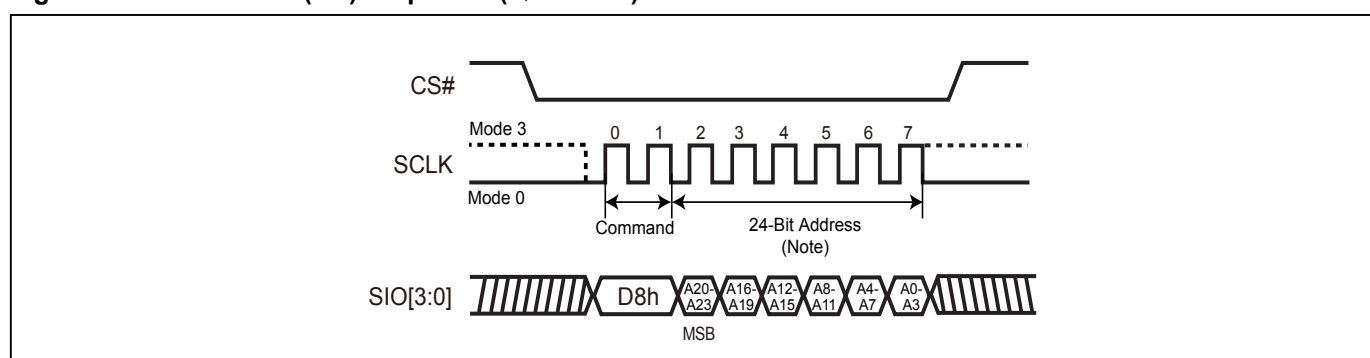
The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Block Erase (BE) instruction will not be executed on the block.

Figure 78. Block Erase (BE) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 79. Block Erase (BE) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-28. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The self-timed Chip Erase Cycle time (t_{CE}) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the t_{CE} timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block protect (BP) Mode" (WPSEL=0). The Chip Erase (CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

When the chip is under "Advances Sector Protect Mode" (WPSEL=1). The Chip Erase (CE) instruction will be executed on unprotected block. The protected Block will be skipped. If one (or more) 4K byte sector was protected in top or bottom 64K byte block, the protected block will also skip the chip erase command.

Figure 80. Chip Erase (CE) Sequence (SPI Mode)

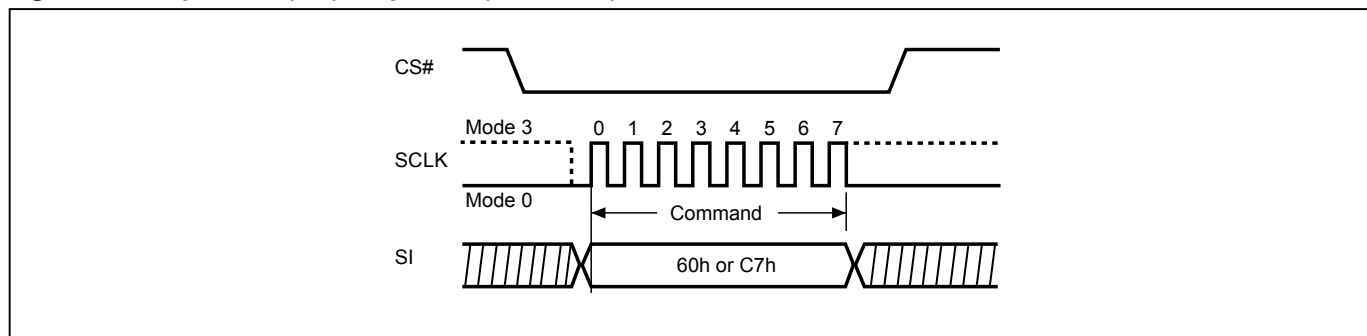
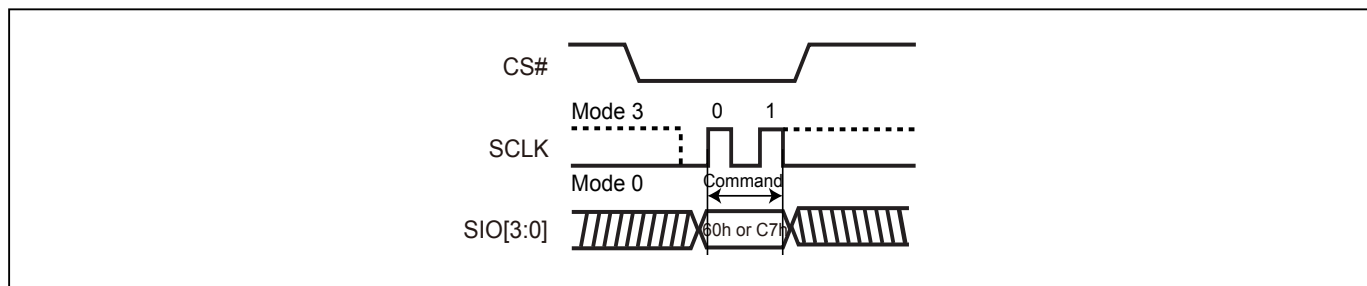


Figure 81. Chip Erase (CE) Sequence (QPI Mode)



10-29. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

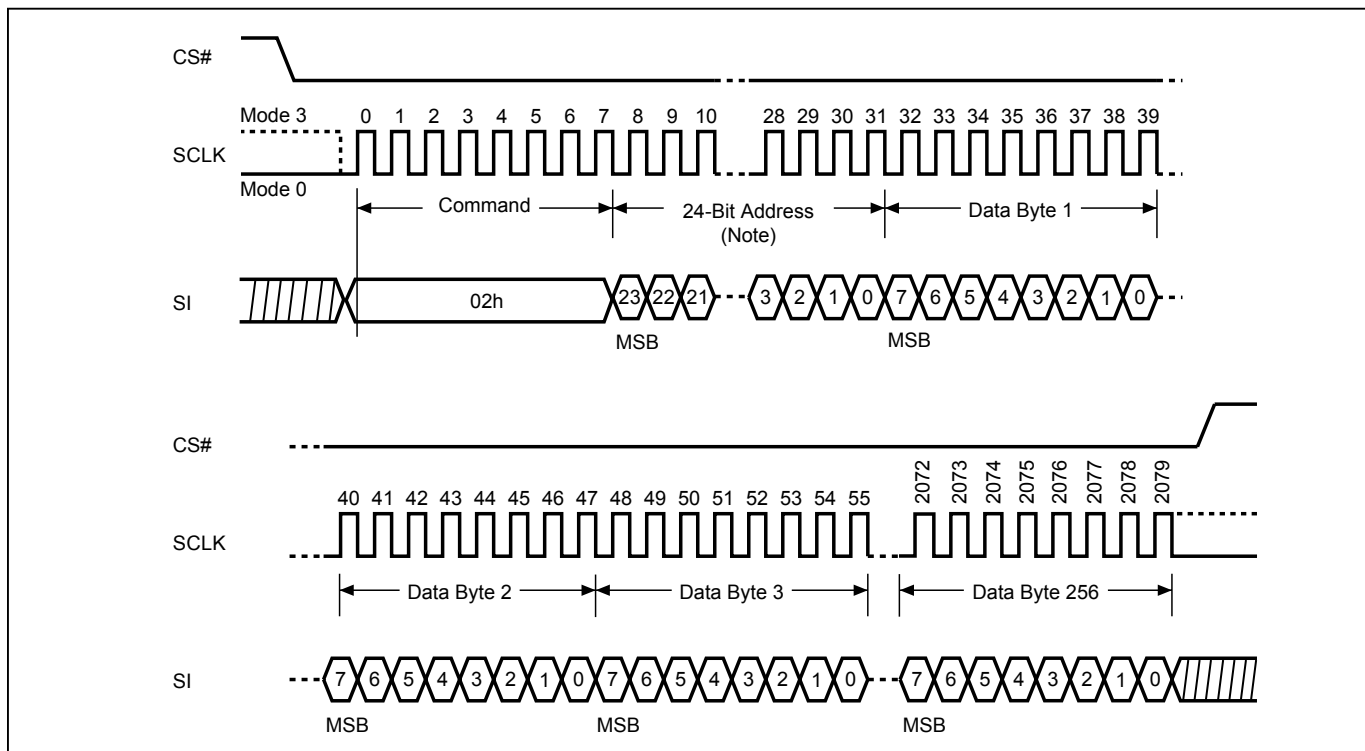
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte or 4-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Page Program (PP) instruction will not be executed.

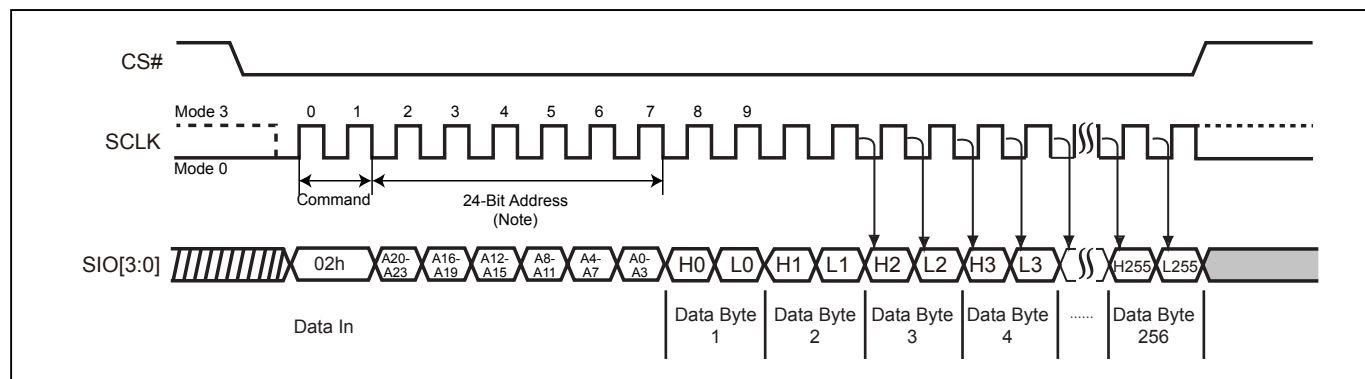
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 82. Page Program (PP) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 83. Page Program (PP) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-30. 4 x I/O Page Program (4PP)

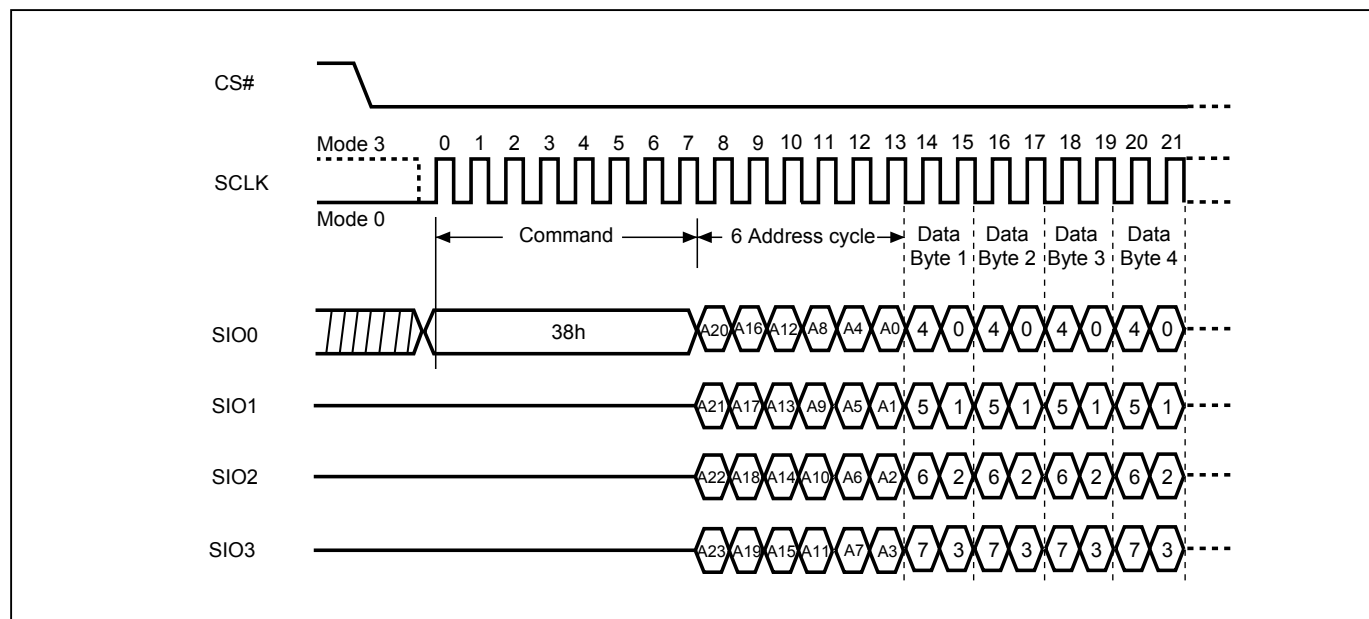
The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The other function descriptions are as same as standard page program.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte or 4-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Quad Page Program (4PP) instruction will not be executed.

Figure 84. 4 x I/O Page Program (4PP) Sequence (SPI Mode only)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-31. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of t_{DP} is required before entering the Deep Power-down mode.

Figure 85. Deep Power-down (DP) Sequence (SPI Mode)

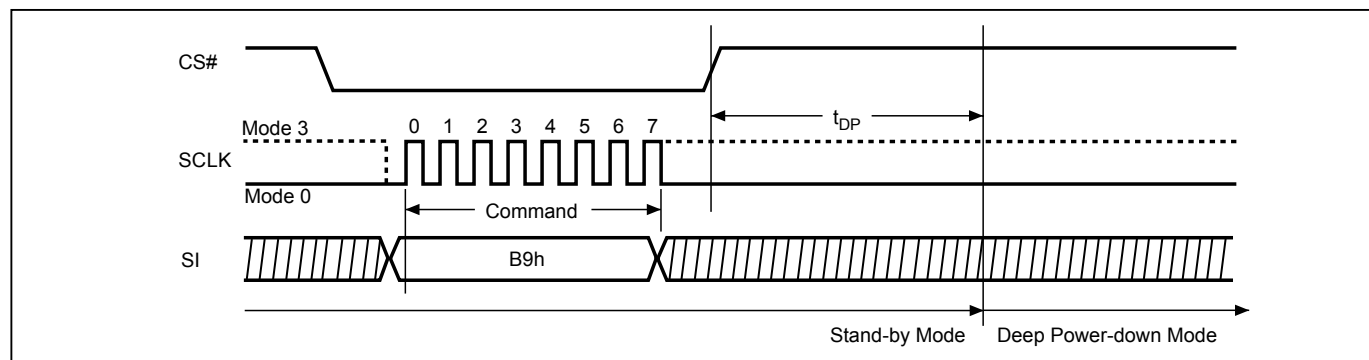
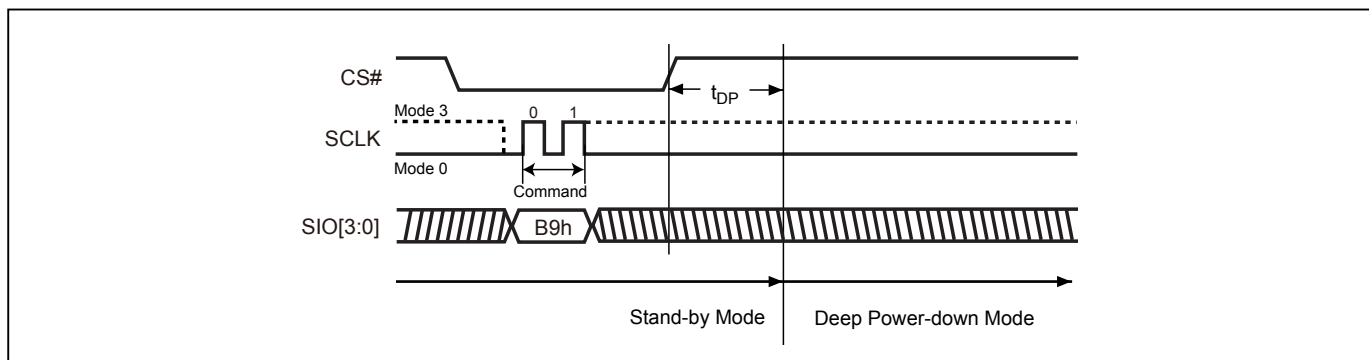


Figure 86. Deep Power-down (DP) Sequence (QPI Mode)



10-32. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 8K-bit secured OTP mode. While device is in secured OTP mode, main array access is not available. The additional 8K-bit secured OTP is independent from main array and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

10-33. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

10-34. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

10-35. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

10-36. Write Protection Selection (WPSEL)

There are two write protection methods provided on this device, (1) Block Lock (BP) protection mode (2) Advanced Sector protection mode. If WPSEL=0, flash is under BP protection mode. If WPSEL=1, flash is under Advanced Sector protection mode. The default value of WPSEL is "0". WPSEL command can be used to set WPSEL=1. **Please note that WPSEL is an OTP bit. Once WPSEL is set to 1, there is no chance to recovery WPSEL back to "0".** If the flash is put on BP mode, the Advanced Sector protection mode is disabled. Contrarily, if flash is on the Advanced Sector protection mode, the BP mode is disabled.

Every time after the system is powered-on, and the Security Register bit 7 is checked to be WPSEL=1, all the blocks or sectors will be write protected by Dynamic Protected Bit (DPB) in default. User may only unlock the blocks or sectors via GBULK instruction. Program or erase functions can only be operated after the Unlock instruction is conducted.

When WPSEL = 0: Block Lock (BP) protection mode.

Array is protected by BP3~BP0 and BP bits are protected by "SRWD=1 and WP#=0", where SRWD is bit 7 of status register that can be set by WRSR command.

When WPSEL =1: Advanced Sector protection mode.

Blocks are individually protected by their own SPB or DPB lock bits which are set to "1" after power up. When the system accepts and executes WPSEL instruction, the bit 7 in security register will be set. It will activate WRLR, RDLR, WRSPB, ESSPB, WRDPB, RDDPB, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3~BP0) indicated block methods. Under the Advanced Sector protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SPB or DPB lock bits.

The sequence of issuing WPSEL instruction is: CS# goes low → sending WPSEL instruction to enter the individual block protect mode → CS# goes high.

Write Protection Selection

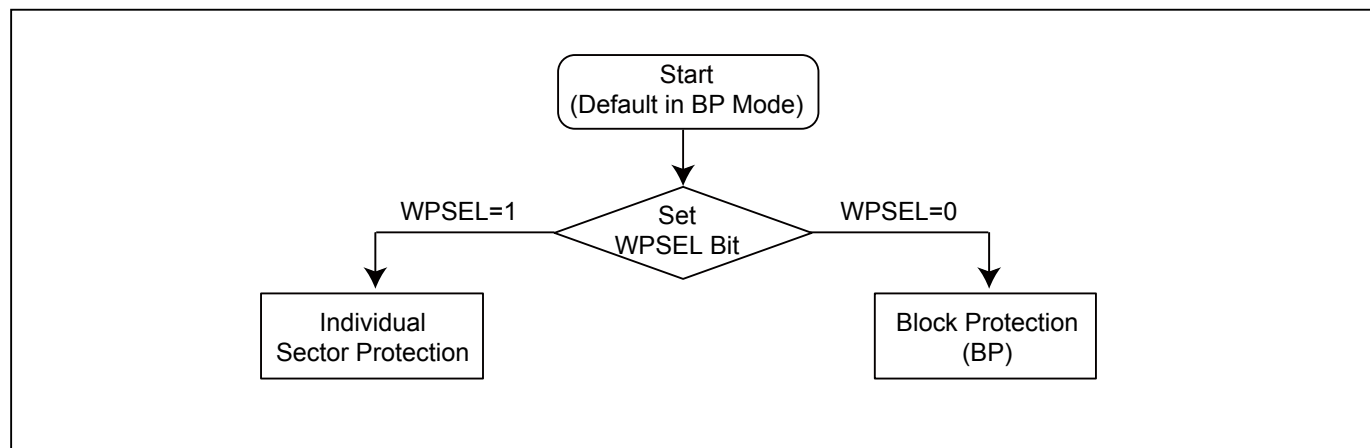
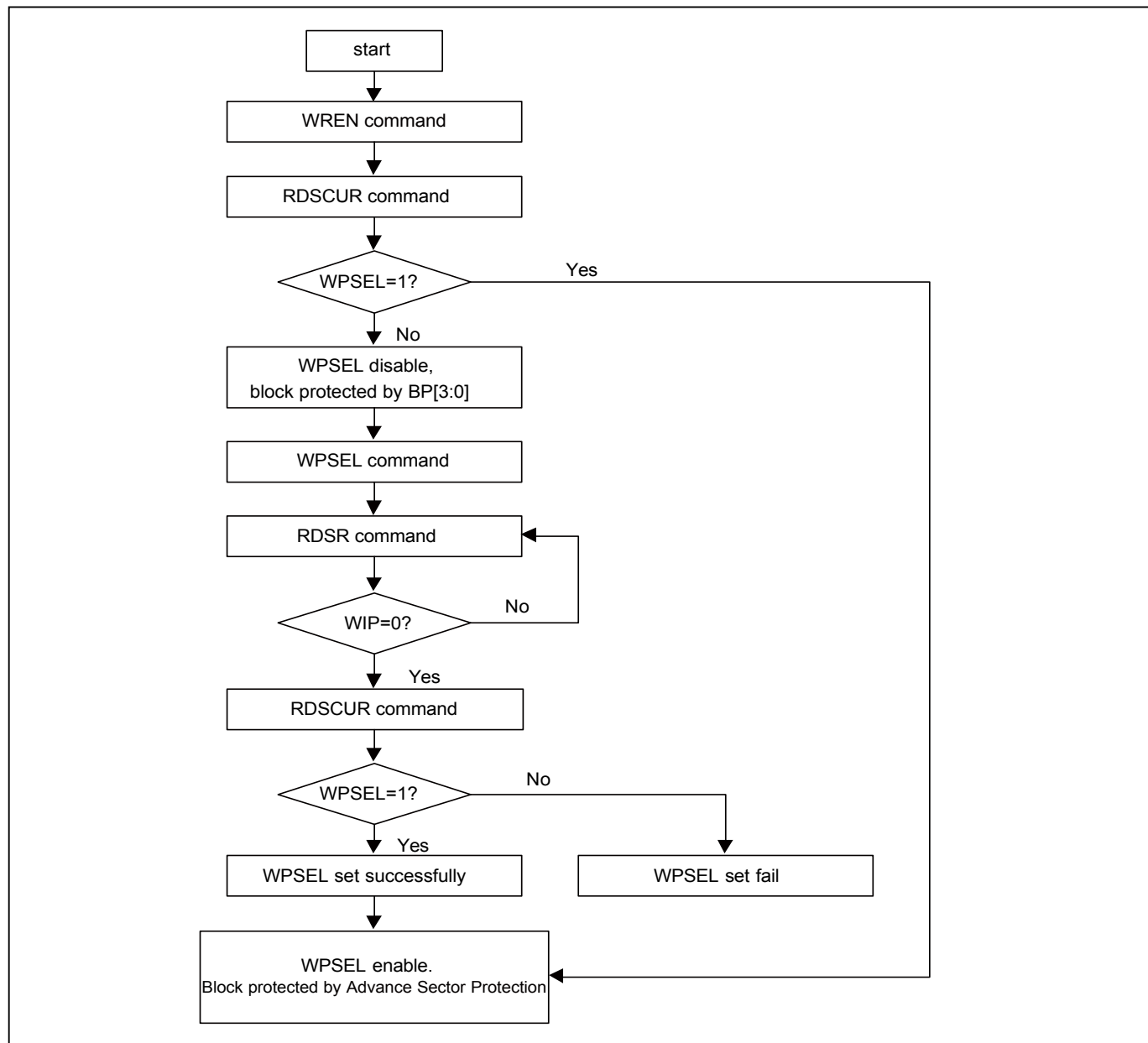


Figure 87. WPSEL Flow

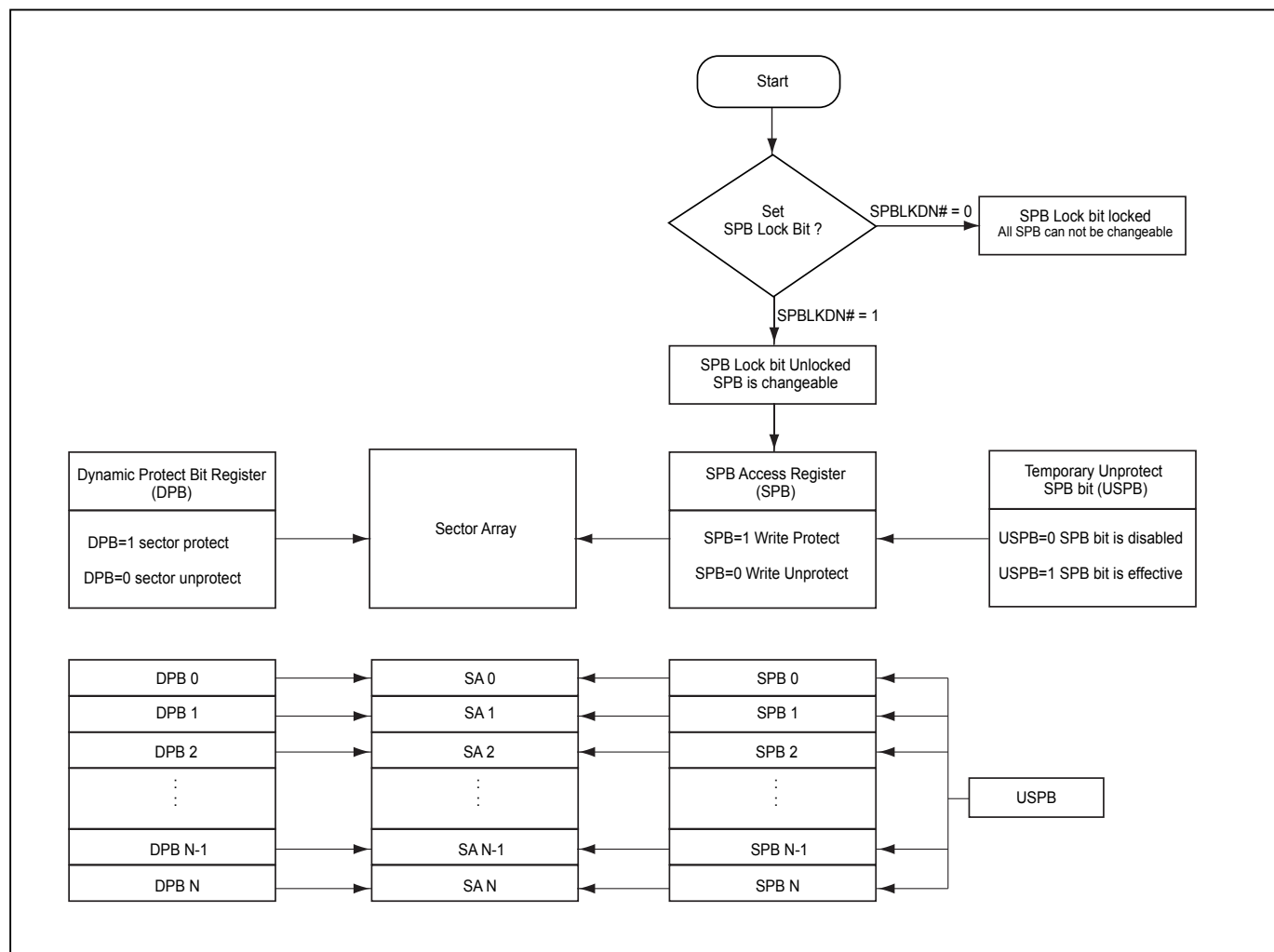
10-37. Advanced Sector Protection

There are two ways to implement software Advanced Sector Protection on this device. Through these two protection methods, user can disable or enable the programming or erasing operation to any individual sector or all sectors.

There is a non-volatile (SPB) and volatile (DPB) protection bit related to the single sector in main flash array. Each of the sectors is protected from programming or erasing operation when the bit is set. The temporary unprotect solid write protect bit (USPB) can temporarily unprotect the sectors protected by SPB.

The figure below helps describing an overview of these methods. The device is default to the Solid mode when shipped from factory. The detail algorithm of advanced sector protection is shown as follows:

Figure 88. Advanced Sector Protection Overview



10-37-1. Lock Register

The Lock Register is a 16-bit one-time programmable register. Lock Register bit [6] is SPB Lock Down Bit (SPBLKDN#) which is an unique bit assigned to control all SPB bit status.

When SPBLKDN is 1, SPB can be changed. When it is locked as 0, all SPB can not be changed anymore, and SPBLKDN bit itself can not be altered anymore, either.

The Lock Register is programmed using the WRLR (Write Lock Register) command. A WREN command must be executed to set the WEL bit before sending the WRLR command.

Lock Register

Bits	Field Name	Function	Type	Default State	Description
15 to 7	RFU	Reserved	OTP	1	Reserved for Future Use
6	SPBLKDN#	SPB Lock Down	OTP	1	1 = SPB changeable 0 = freeze SPB
5 to 0	RFU	Reserved	OTP	1	Reserved for Future Use

Figure 89. Read Lock Register (RDLR) Sequence

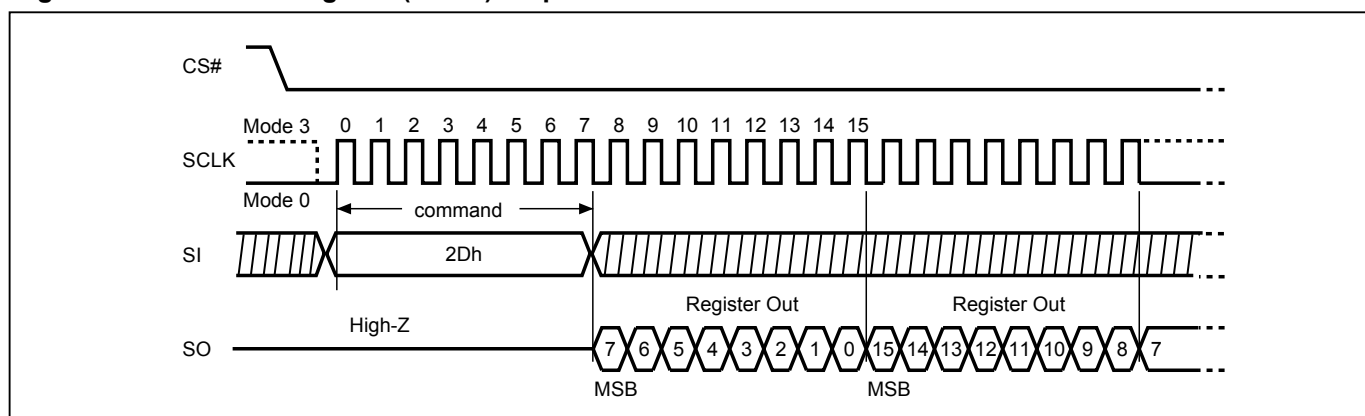
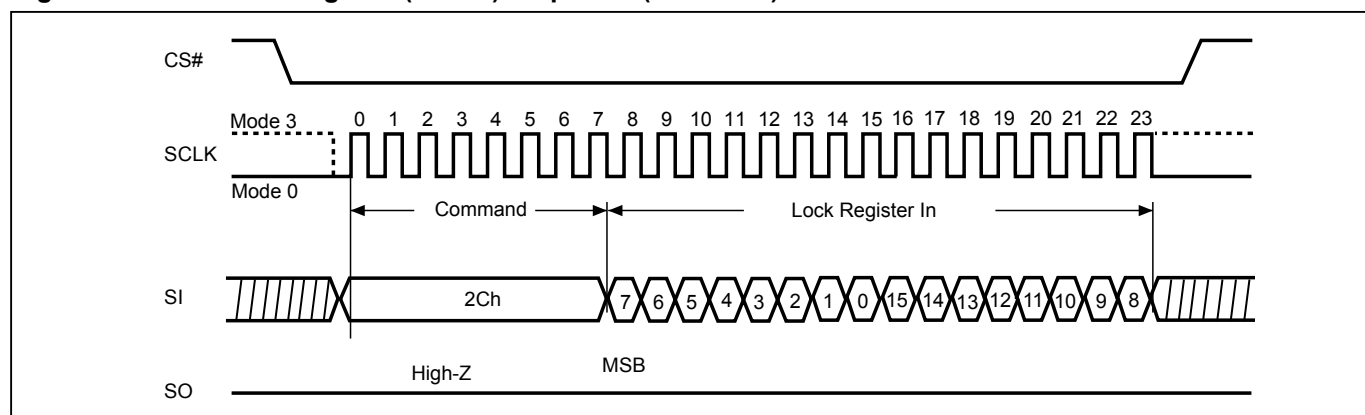


Figure 90. Write Lock Register (WRLR) Sequence (SPI Mode)



10-37-2. Solid Protection Bits

The Solid write Protection bit (SPB) is a nonvolatile bit with the same endurance as the Flash memory. It is assigned to each sector individually.

When a SPB is set to “1”, the associated sector may be protected, preventing any program or erase operation on this sector. The SPB bits are set individually by WRSPB command. However, it cannot be cleared individually. Issuing the ESSPB command will erase all SPB in the same time.

To unprotect a protected sector (corresponding SPB cleared to “0”), the SPB lock bit must be unlocked first. A reset or a power-up cycle can unlock the SPB lock bit.

After the SPB lock bit is unlocked, the SPB status can be changed for desired settings. To lock the Solid Protection Bits after the modification has finished, the SPB Lock Bit must be set once again.

To verify the programming state of the SPB for a given sector, issuing a RDSPB Command to the device is required.

Note:

1. Once SPB Lock Bit is set, its program or erase command will not be executed and time-out without programming or erasing the SPB.

SPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	SPB (Solid protected Bit)	00h= SPB for the sector address unprotected FFh= SPB for the sector address protected	00h	Non-volatile

Figure 91. Read SPB Status (RDSPB) Sequence

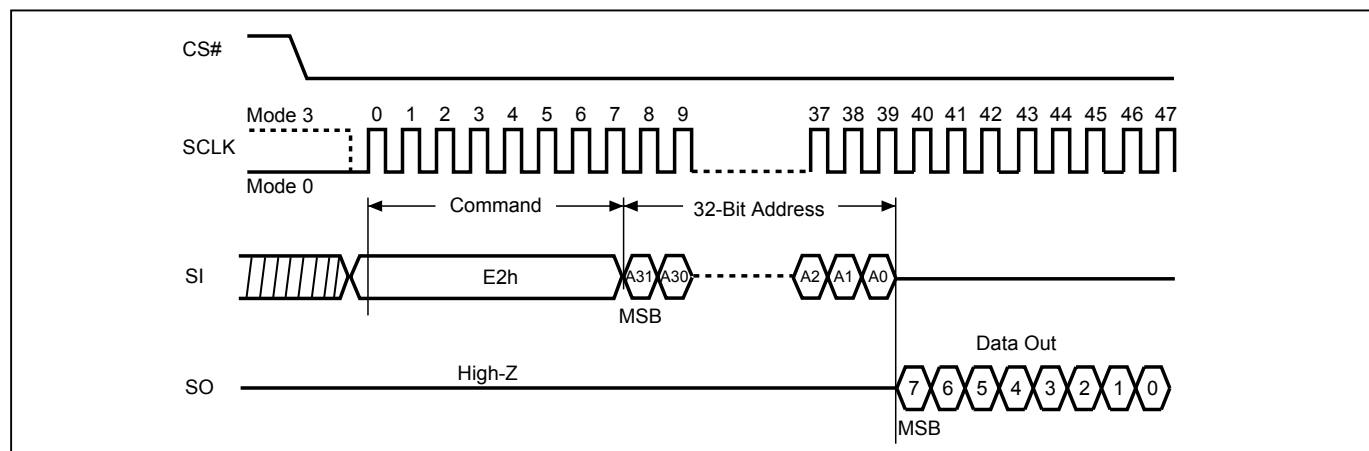


Figure 92. SPB Erase (ESSPB) Sequence

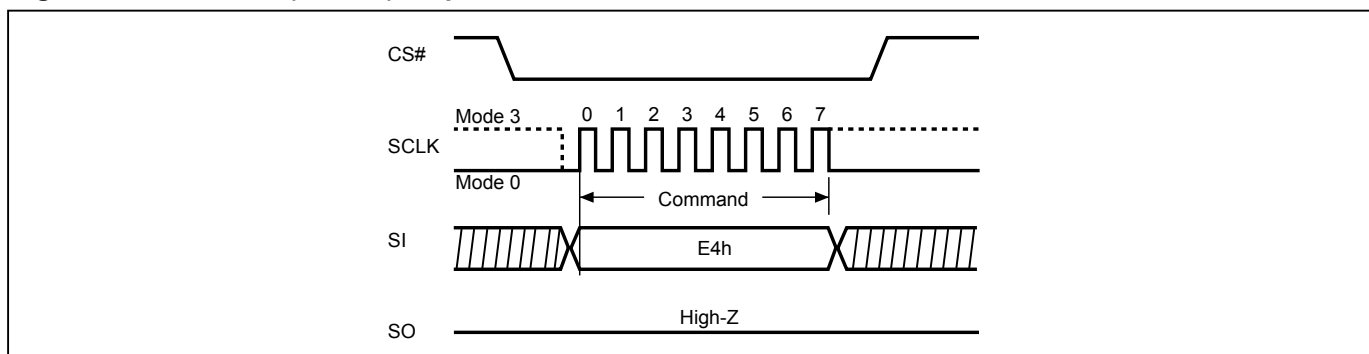
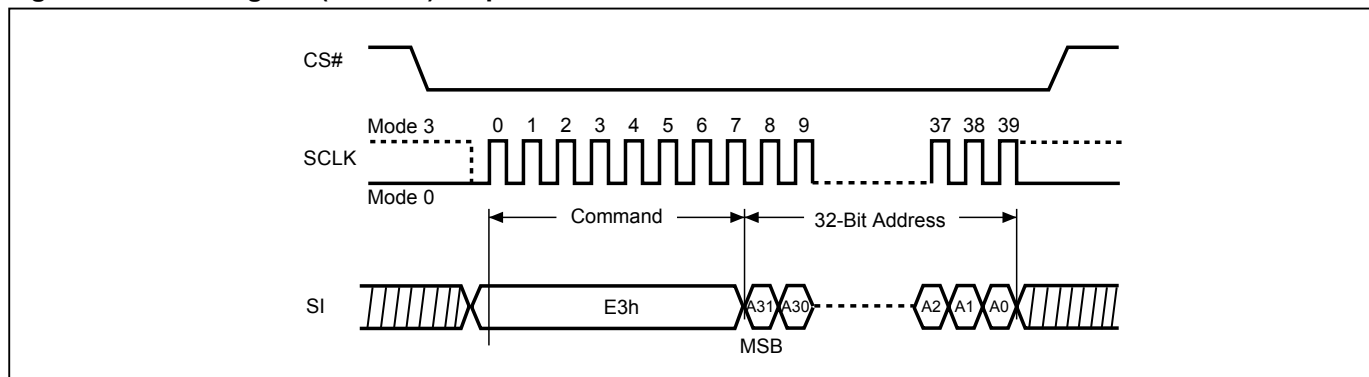


Figure 93. SPB Program (WRSPB) Sequence



10-37-3. Dynamic Write Protection Bits

The Dynamic Protection features a volatile type protection to each individual sector. It can protect sectors from unintentional change, and is easy to disable when there are necessary changes.

All DPBs are default as protected (FFh) after reset or upon power up cycle. Via setting up Dynamic Protection bit (DPB) by write DPB command (WRDPB), user can cancel the Dynamic Protection of associated sector.

The Dynamic Protection only works on those unprotected sectors whose SPBs are cleared. After the DPB state is cleared to "0", the sector can be modified if the SPB state is unprotected state.

DPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic protected Bit)	00h= DPB for the sector address unprotected FFh= DPB for the sector address protected	FFh	Volatile

Figure 94. Read DPB Register (RDDPB) Sequence

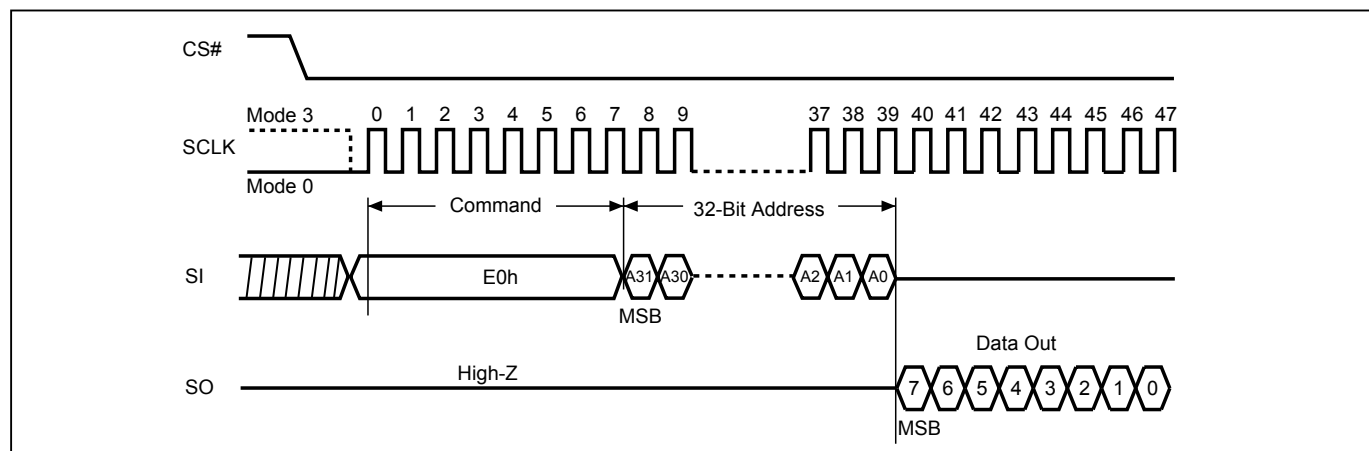
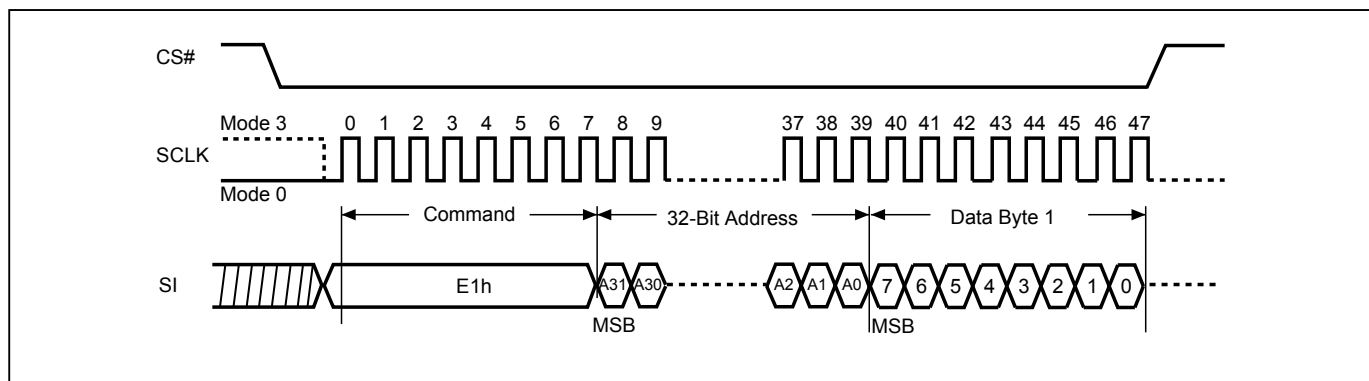


Figure 95. Write DPB Register (WRDPB) Sequence



10-37-4. Temporary Un-protect Solid write protect bit (USPB)

Temporary Un-protect Solid write Protect Bit is volatile bit. Software can temporarily unprotect write protect sectors despite of SPBs' property when DPBs are cleared. While the USPB=0, all the SPBs' property is masked.

Notes:

1. Upon power up, the USPB status is default protected. The USPB can be unprotected (to "0") or protected (to "1") as often as needed. The hardware reset will reset USPB/DPB to their default values.
2. Please refer to ["10-37-6. Sector Protection States Summary Table"](#) for the sector state with the protection status of DPB/SPB/USPB bits.

10-37-5. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is a chip-based protected or unprotected operation. It can enable or disable all DPB.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.

The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

10-37-6. Sector Protection States Summary Table

Protection Status			Sector State
DPB bit	SPB bit	USPB bit	
0	0	0	Unprotect
0	0	1	Unprotect
0	1	0	Unprotect
0	1	1	Protect
1	0	0	Protect
1	0	1	Protect
1	1	0	Protect
1	1	1	Protect

10-38. Program/Erase Suspend/Resume

The device allow the interruption of Sector-Erase, Block-Erase or Page-Program operations and conduct other operations.

After issue suspend command, the system can determine if the device has entered the Erase-Suspended mode through Bit2 (PSB) and Bit3 (ESB) of security register. (please refer to "[Table 10. Security Register Definition](#)")

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

10-39. Erase Suspend

Erase suspend allow the interruption of all erase operations. After the device has entered Erase-Suspended mode, the system can read any sector(s) or Block(s) except those being erased by the suspended erase operation. Reading the sector or Block being erase suspended is invalid.

After erase suspend, WEL bit will be clear, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, 3Bh, 6Bh, BBh, EBh, ECh, EDh, EEh, 0Ch, BCh, 3Ch, 5Ah, C0h, 06h, 04h, 2Bh, 9Fh, AFh, 05h, ABh, 90h, B1h, C1h, B0h, 30h, 66h, 99h, 00h, 35h, F5h, 15h, 2Dh, 27h, A7h, E2h, E0h, 16h, 71h, 72h)

If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended mode until 20us time has elapsed.

Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

10-40. Program Suspend

Program suspend allows the interruption of all program operations. After the device has entered Program-Suspended mode, the system can read any sector(s) or Block(s) except those being programmed by the suspended program operation. Reading the sector or Block being program suspended is invalid.

After program suspend, WEL bit will be cleared, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, 3Bh, 6Bh, BBh, EBh, ECh, EDh, EEh, 0Ch, BCh, 3Ch, 5Ah, C0h, 06h, 04h, 2Bh, 9Fh, AFh, 05h, ABh, 90h, B1h, C1h, B0h, 30h, 66h, 99h, 00h, 35h, F5h, 15h, 2Dh, 27h, A7h, E2h, E0h, 16h, 71h, 72h)

Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Figure 96. Suspend to Read Latency

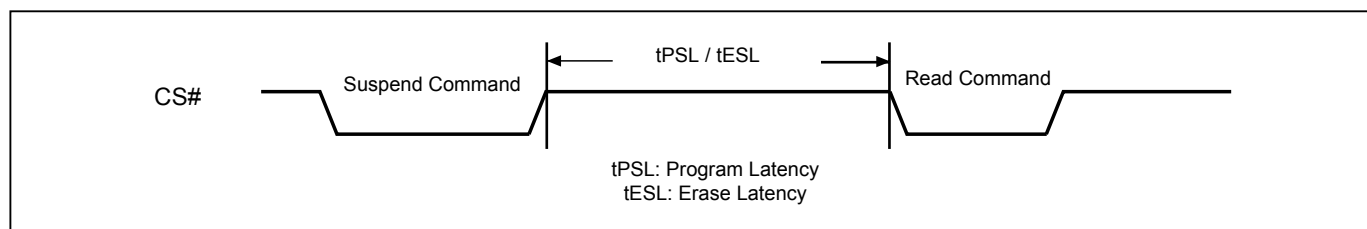


Figure 97. Resume to Read Latency

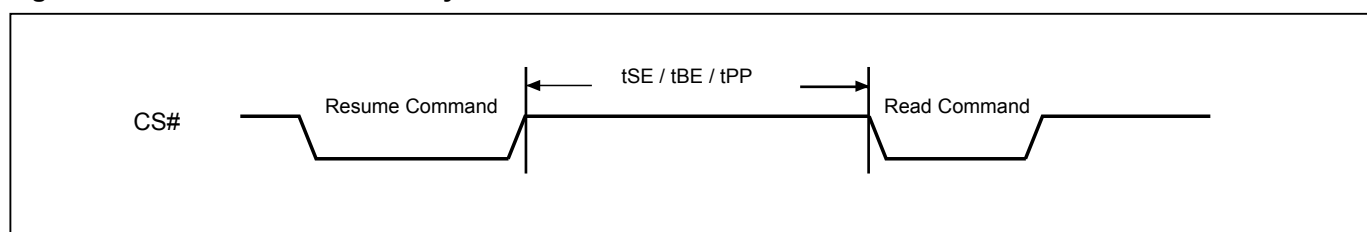
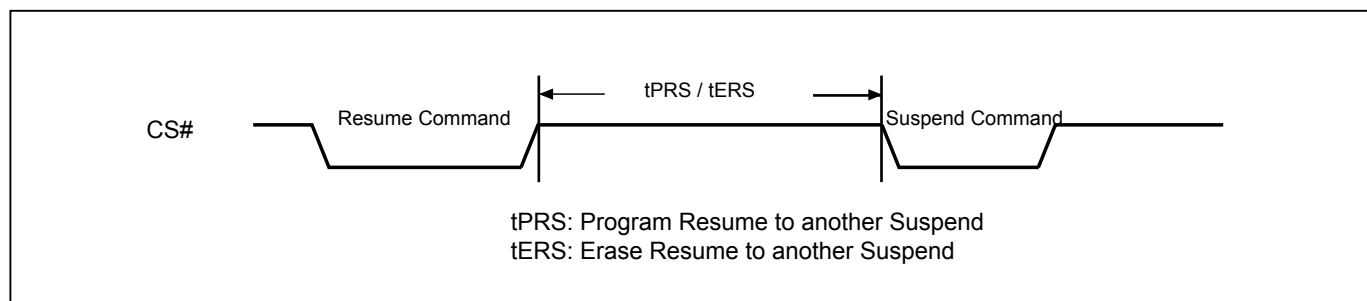


Figure 98. Resume to Suspend Latency



10-41. Write-Resume

The Write operation is being resumed when Write-Resume instruction issued. ESB or PSB (suspend status bit) in Status register will be changed back to "0".

The operation of Write-Resume is as follows: CS# drives low → send write resume command cycle (30H) → drive CS# high. By polling Busy Bit in status register, the internal write operation status could be checked to be completed or not. The user may also wait the time lag of tSE, tBE, tPP for Sector-erase, Block-erase or Page-programming. WREN (command "06") is not required to issue before resume. Resume to another suspend operation requires latency time of 1ms.

Please note that, if "performance enhance mode" is executed during suspend operation, the device can not be resumed. To restart the write command, disable the "performance enhance mode" is required. After the "performance enhance mode" is disabled, the write-resume command is effective.

10-42. No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care during SPI mode.

10-43. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

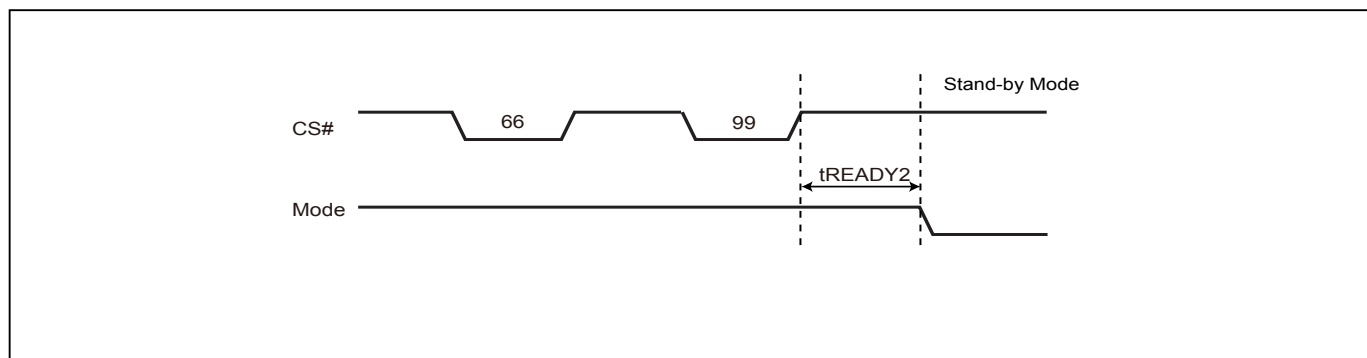
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to ["Table 18. Reset Timing- \(Other Operation\)"](#) for tREADY2.

Figure 99. Software Reset Recovery



Note: Refer to "[Table 18. Reset Timing-\(Other Operation\)](#)" for tREADY2.

Figure 100. Reset Sequence (SPI mode)

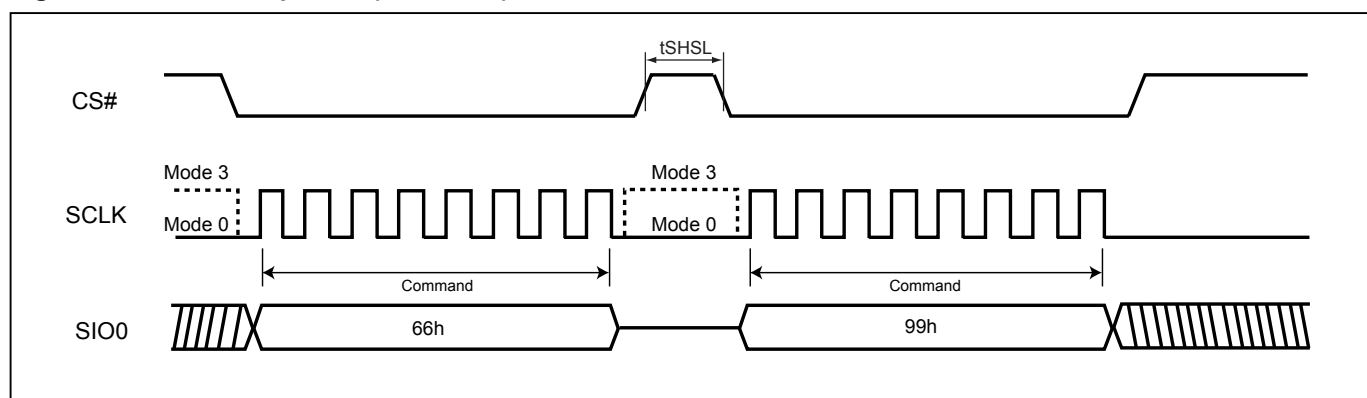
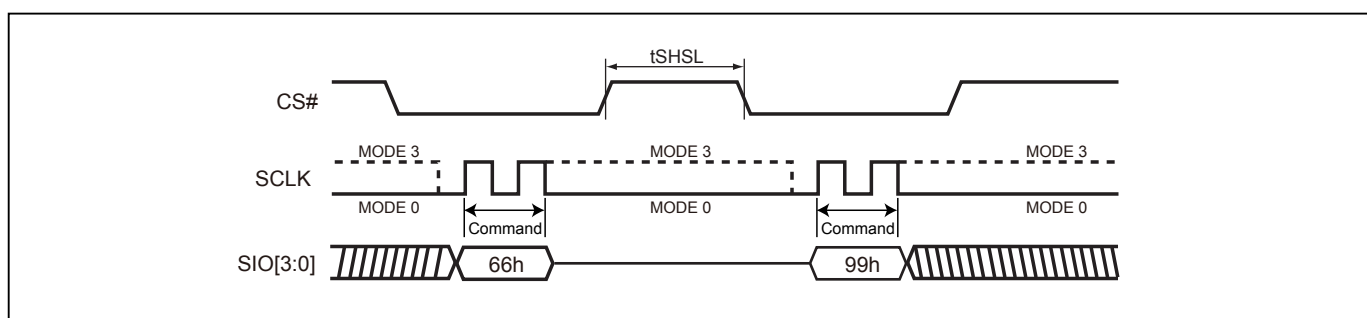


Figure 101. Reset Sequence (QPI mode)



11. Serial Flash Discoverable Parameter (SFDP)

11-1. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC standard, JESD216B.

Figure 102. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

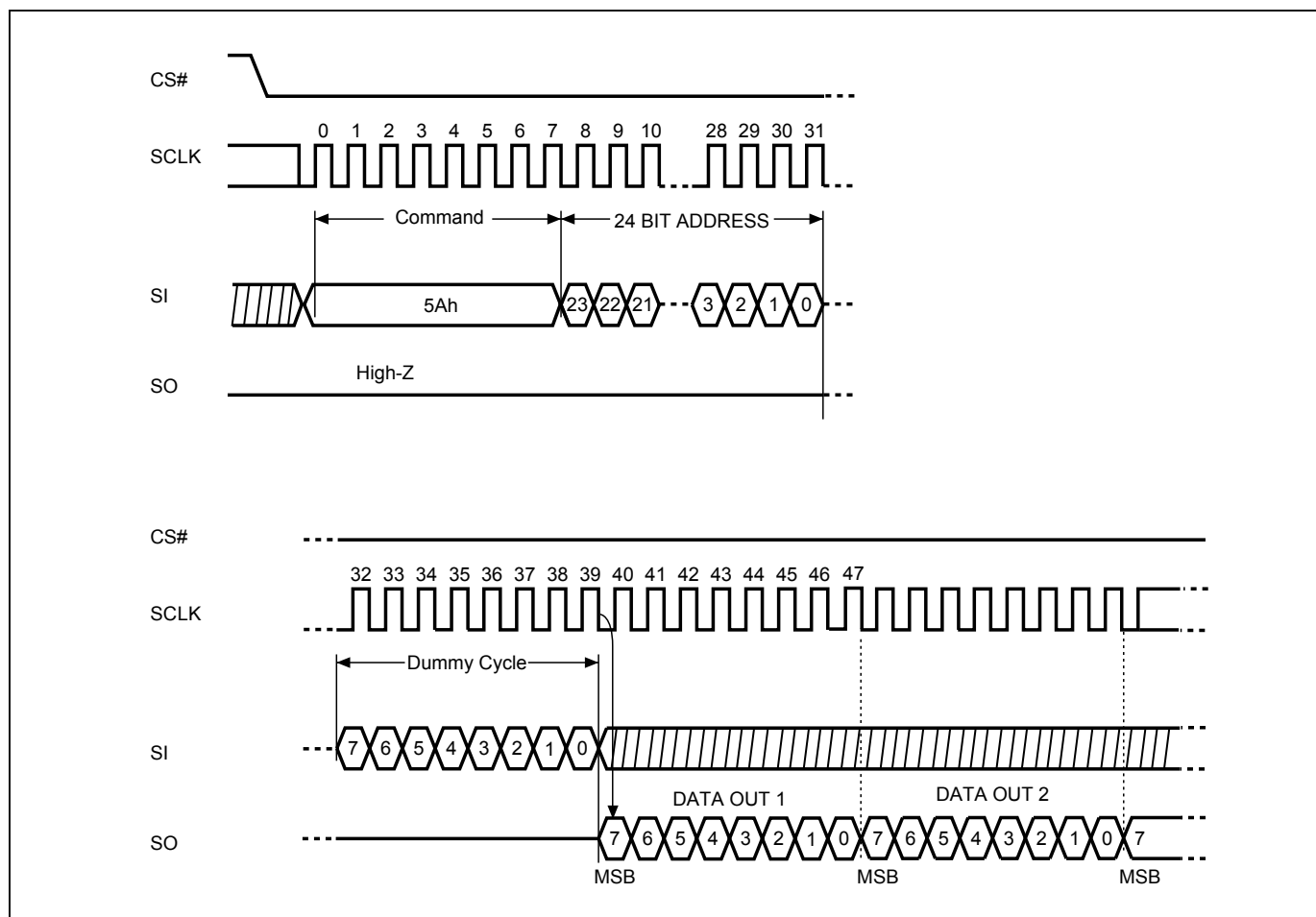


Table 13. Signature and Parameter Identification Data Values

SFDP Table (JESD216B) below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
SFDP Signature	Fixed: 50444653h	00h	07:00	53h	53h
		01h	15:08	46h	46h
		02h	23:16	44h	44h
		03h	31:24	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	07:00	06h	06h
SFDP Major Revision Number	Start from 01h	05h	15:08	01h	01h
Number of Parameter Headers	This number is 0-based. Therefore, 0 indicates 1 parameter header.	06h	23:16	02h	02h
Unused		07h	31:24	FFh	FFh
ID number (JEDEC)	00h: it indicates a JEDEC specified header.	08h	07:00	00h	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:08	06h	06h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0Bh	31:24	10h	10h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	07:00	30h	30h
		0Dh	15:08	00h	00h
		0Eh	23:16	00h	00h
Unused		0Fh	31:24	FFh	FFh

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
ID number (Macronix manufacturer ID)	it indicates Macronix manufacturer ID	10h	07:00	C2h	C2h
Parameter Table Minor Revision Number	Start from 00h	11h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13h	31:24	04h	04h
Parameter Table Pointer (PTP)	First address of Macronix Flash Parameter table	14h	07:00	10h	10h
		15h	15:08	01h	01h
		16h	23:16	00h	00h
Unused		17h	31:24	FFh	FFh
ID number (4-byte Address Instruction)	4-byte Address Instruction parameter ID	18h	07:00	84h	84h
Parameter Table Minor Revision Number	Start from 00h	19h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	1Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	1Bh	31:24	02h	02h
Parameter Table Pointer (PTP)	First address of 4-byte Address Instruction table	1Ch	07:00	C0h	C0h
		1Dh	15:08	00h	00h
		1Eh	23:16	00h	00h
Unused		1Fh	31:24	FFh	FFh

Table 14. Parameter Table (0): JEDEC Flash Parameter Tables

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Block/Sector Erase sizes	00: Reserved, 01: 4KB erase, 10: Reserved, 11: not supported 4KB erase	30h	01:00	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Required for Writing to Volatile Status Registers	0: not required 1: required 00h to be written to the status register		03	0b	
Write Enable Instruction Select for Writing to Volatile Status Registers	0: use 50h instruction 1: use 06h instruction Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Instruction		31h	15:08	20h	20h
(1-1-2) Fast Read (Note2)	0=not supported 1=supported	32h	16	1b	FBh
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	01b	
Double Transfer Rate (DTR) Clocking	0=not supported 1=supported		19	1b	
(1-2-2) Fast Read	0=not supported 1=supported		20	1b	
(1-4-4) Fast Read	0=not supported 1=supported		21	1b	
(1-1-4) Fast Read	0=not supported 1=supported		22	1b	
Unused			23	1b	
Unused		33h	31:24	FFh	FFh
Flash Memory Density		37h:34h	31:00	1FFF FFFFh	
(1-4-4) Fast Read Number of Wait states (Note3)	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	38h	04:00	0 0100b	44h
(1-4-4) Fast Read Number of Mode Bits (Note4)	Mode Bits: 000b: Not supported; 010b: 2 bits		07:05	010b	
(1-4-4) Fast Read Instruction		39h	15:08	EBh	EBh
(1-1-4) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	3Ah	20:16	0 1000b	08h
(1-1-4) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	000b	
(1-1-4) Fast Read Instruction		3Bh	31:24	6Bh	6Bh

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
(1-1-2) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	3Ch	04:00	0 1000b	08h
(1-1-2) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		07:05	000b	
(1-1-2) Fast Read Instruction		3Dh	15:08	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	3Eh	20:16	0 0100b	04h
(1-2-2) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	000b	
(1-2-2) Fast Read Instruction		3Fh	31:24	BBh	BBh
(2-2-2) Fast Read	0=not supported 1=supported	40h	00	0b	FEh
Unused			03:01	111b	
(4-4-4) Fast Read	0=not supported 1=supported		04	1b	
Unused			07:05	111b	
Unused		43h:41h	31:08	FFh	FFh
Unused		45h:44h	15:00	FFh	FFh
(2-2-2) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	46h	20:16	0 0000b	00h
(2-2-2) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	000b	
(2-2-2) Fast Read Instruction		47h	31:24	FFh	FFh
Unused		49h:48h	15:00	FFh	FFh
(4-4-4) Fast Read Number of Wait states	0 0000b: Not supported; 0 0100b: 4 0 0110b: 6; 0 1000b: 8	4Ah	20:16	0 0100b	44h
(4-4-4) Fast Read Number of Mode Bits	Mode Bits: 000b: Not supported; 010b: 2 bits		23:21	010b	
(4-4-4) Fast Read Instruction		4Bh	31:24	EBh	EBh
Erase Type 1 Size	Sector/block size = 2 ^N bytes (Note5) 0Ch: 4KB; 0Fh: 32KB; 10h: 64KB	4Ch	07:00	0Ch	0Ch
Erase Type 1 Erase Instruction		4Dh	15:08	20h	20h
Erase Type 2 Size	Sector/block size = 2 ^N bytes 00h: N/A; 0Fh: 32KB; 10h: 64KB	4Eh	23:16	0Fh	0Fh
Erase Type 2 Erase Instruction		4Fh	31:24	52h	52h
Erase Type 3 Size	Sector/block size = 2 ^N bytes 00h: N/A; 0Fh: 32KB; 10h: 64KB	50h	07:00	10h	10h
Erase Type 3 Erase Instruction		51h	15:08	D8h	D8h
Erase Type 4 Size	00h: N/A, This sector type doesn't exist	52h	23:16	00h	00h
Erase Type 4 Erase Instruction		53h	31:24	FFh	FFh

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Multiplier from typical erase time to maximum erase time	Multiplier value: 0h~Fh (0~15) Max. time = 2 * (Multiplier + 1) * Typical Time	54h	03:00	0011b	D3h
Erase Type 1 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	55h	07:04 08	1 1101b	49h
	Units 00: 1ms, 01: 16ms 10b: 128ms, 11b: 1s		10:09	00b	
EraseType 2 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	56h	15:11	0 1001b	C5h
	Units 00: 1ms, 01: 16ms 10b: 128ms, 11b: 1s		17:16	01b	
Erase Type 3 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	57h	22:18	1 0001b	00h
	Units 00: 1 ms, 01: 16 ms 10b: 128ms, 11b: 1s		24:23	01b	
Erase Type 4 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	58h	29:25	0 0000b	81h
	Units 00: 1ms, 01: 16ms 10b: 128 ms, 11b: 1 s		31:30	00b	
Multiplier from typical time to max time for Page or byte program	Multiplier value: 0h~Fh (0~15) Max. time = 2 * (Multiplier + 1) * Typical Time	58h	03:00	0001b	81h
Page Program Size	Page size = 2^N bytes 2^8 = 256 bytes, 8h = 1000b		07:04	1000h	
Page Program Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	59h	12:08	1 1111b	DFh
	Units 0: 8us, 1: 64us		13	0b	
Byte Program Time, First Byte (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units	5Ah	15:14 17:16	0011b	04h
	Units 0: 1us, 1: 8us		18	1b	
Byte Program Time, Additional Byte (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units	5Ah	22:19	0000b	04h
	Units 0: 1us, 1: 8us		23	0b	

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Chip Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	5Bh	27:24	0 0011b	E3h
	Units		28		
	00: 16ms, 01: 256ms 10: 4s, 11: 64s		30:29	11b	
Reserved	Reserved: 1b		31	1b	
Prohibited Operations During Program Suspend	<ul style="list-style-type: none"> • xxx0b: May not initiate a new erase anywhere • xx0xb: May not initiate a new page program anywhere • x1xxb: May not initiate a read in the program suspended page size • 1xxxb: The erase and program restrictions in bits 1:0 are sufficient 	5Ch	03:00	0100b	44h
Prohibited Operations During Erase Suspend	<ul style="list-style-type: none"> • xxx0b: May not initiate a new erase anywhere • xx1xb: May not initiate a page program in the erase suspended sector size • xx0xb: May not initiate a page program anywhere • x1xxb: May not initiate a read in the erase suspended sector size • 1xxxb: The erase and program restrictions in bits 5:4 are sufficient 		07:04	0100b	
Reserved	Reserved: 1b	5Dh	08	1b	01h
Program Resume to Suspend Interval (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us		12:09	0000b	
Program Suspend Latency (Max.)	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units	5Eh	15:13	1 1000b	07h
	Units		17:16		
	00: 128ns, 01: 1us 10: 8us, 11: 64us		19:18	01b	
Erase Resume to Suspend Interval (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us		23:20	0000b	
Erase Suspend Latency (Max.)	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units	5Fh	28:24	1 1000b	38h
	Units		30:29	01b	
	00: 128ns, 01: 1us 10: 8us, 11: 64us				
Suspend / Resume supported	0= Support 1= Not supported		31	0b	
Program Resume Instruction	Instruction to Resume a Program	60h	07:00	30h	30h
Program Suspend Instruction	Instruction to Suspend a Program	61h	15:08	B0h	B0h
Erase Resume Instruction	Instruction to Resume Write/Erase	62h	23:16	30h	30h
Erase Suspend Instruction	Instruction to Suspend Write/Erase	63h	31:24	B0h	B0h

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Reserved	Reserved: 11b		01:00	11b	
Status Register Polling Device Busy	<ul style="list-style-type: none"> Bit 2: Read WIP bit [0] by 05h Read instruction Bit 3: Read bit 7 of Status Register by 70h Read instruction (0=not supported 1=support) Bit 07:04, Reserved: 1111b 	64h	07:02	11 1101b	F7h
Release from Deep Power-down (RDP) Delay (Max.)	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units Units 00: 128ns, 01: 1us 10: 8us, 11: 64us	65h	12:08	1 1101b	BDh
Release from Deep Power-down (RDP) Instruction	Instruction to Exit Deep Power Down	66h	15 22:16	1010 1011b (ABh)	D5h
Enter Deep Power Down Instruction	Instruction to Enter Deep Power Down	67h	23 30:24	1011 1001b (B9h)	5Ch
Deep Power Down Supported	0: Supported 1: Not supported	67h	31	0b	
4-4-4 Mode Disable Sequences	Methods to exit 4-4-4 mode ♦ xx1xb: issue F5h instruction	68h	03:00	1010b	4Ah
4-4-4 Mode Enable Sequences	Methods to enter 4-4-4 mode ♦ x x1xxb: issue instruction 35h		07:04 08	0 0100b	
0-4-4 Mode Supported	Performance Enhance Mode, Continuous Read, Execute in Place 0: Not supported 1: Supported		09	1b	
0-4-4 Mode Exit Method	<ul style="list-style-type: none"> xx_1xb: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation. xx_xx1xb: If 3-Byte address active, input Fh on DQ0-DQ3 for 8 clocks. If 4-Byte address active, input Fh on DQ0-DQ3 for 10 clocks. xx_x1xxb: Reserved xx_1xxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. x1_1xxb: Mode Bit[7:0]≠Axh 1x_1xxb: Reserved 	69h	15:10	10 0111b	9Eh
0-4-4 Mode Entry Method	<ul style="list-style-type: none"> xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode x1xb: Mode Bit[7:0]=Axh 1xxb: Reserved 		19:16	1001h	
Quad Enable (QE) bit Requirements	<ul style="list-style-type: none"> 000b: No QE bit. Detects 1-1-4/1-4-4 reads based on instruction 010b: QE is bit 6 of Status Register, where 1=Quad Enable or 0=not Quad Enable 111b: Not Supported 	6Ah	22:20	010b	29h
HOLD and RESET Disable by bit 4 of Ext. Configuration Register	0: Not supported		23	0b	

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Reserved		6Bh	31:24	FFh	FFh
Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1	♦ xxx_xxx1b: Non-Volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write ♦ x1x_xxxxb: Reserved ♦ 1xx_xxxxb: Reserved	6Ch	06:00	111 0000b	F0h
Reserved			07	1b	
Soft Reset and Rescue Sequence Support	Return the device to its default power-on state ♦ x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h.	6Dh	13:08	01 0000b	50h
Exit 4-Byte Addressing	♦ xx_xxxx_xxx1b: issue instruction E9h to exit 4-Byte address mode (write enable instruction 06h is not required) ♦ xx_xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:A24] bits. Read with instruction C8h. Write instruction is C5h, data length is 1 byte. Return to lowest memory segment by setting A[31:24] to 00h and use 3-Byte addressing. ♦ xx_xx1x_xxxxb: Hardware reset ♦ xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) ♦ xx_1xxx_xxxxb: Power cycle ♦ x1_xxxx_xxxxb: Reserved ♦ 1x_xxxx_xxxxb: Reserved		15:14	01b	
		6Eh	23:16	1111 1001b	F9h

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Enter 4-Byte Addressing	<ul style="list-style-type: none"> ♦ xxxx_xxx1b: issue instruction B7h (preceding write enable not required) ♦ xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:24] bits. Read with instruction C8h. Write instruction is C5h with 1 byte of data. Select the active 128 Mbit memory segment by setting the appropriate A[31:24] bits and use 3-Byte addressing. ♦ xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition. ♦ 1xxx_xxxxb: Reserved 	6Fh	31:24	1000 0101b	85h

Table 15. Parameter Table (1): 4-Byte Instruction Tables

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Support for (1-1-1) READ Command, Instruction=13h	0=not supported 1=supported	C0h	00	1b	7Fh
Support for (1-1-1) FAST_READ Command, Instruction=0Ch	0=not supported 1=supported		01	1b	
Support for (1-1-2) FAST_READ Command, Instruction=3Ch	0=not supported 1=supported		02	1b	
Support for (1-2-2) FAST_READ Command, Instruction=BCh	0=not supported 1=supported		03	1b	
Support for (1-1-4) FAST_READ Command, Instruction=6Ch	0=not supported 1=supported		04	1b	
Support for (1-4-4) FAST_READ Command, Instruction=ECh	0=not supported 1=supported		05	1b	
Support for (1-1-1) Page Program Command, Instruction=12h	0=not supported 1=supported		06	1b	
Support for (1-1-4) Page Program Command, Instruction=34h	0=not supported 1=supported		07	0b	
Support for (1-4-4) Page Program Command, Instruction=3Eh	0=not supported 1=supported	C1h	08	1b	8Fh
Support for Erase Command – Type 1 size, Instruction lookup in next Dword	0=not supported 1=supported		09	1b	
Support for Erase Command – Type 2 size, Instruction lookup in next Dword	0=not supported 1=supported		10	1b	
Support for Erase Command – Type 3 size, Instruction lookup in next Dword	0=not supported 1=supported		11	1b	
Support for Erase Command – Type 4 size, Instruction lookup in next Dword	0=not supported 1=supported		12	0b	
Support for (1-1-1) DTR_Read Command, Instruction=0Eh	0=not supported 1=supported		13	0b	
Support for (1-2-2) DTR_Read Command, Instruction=BEh	0=not supported 1=supported		14	0b	
Support for (1-4-4) DTR_Read Command, Instruction=EEh	0=not supported 1=supported		15	1b	

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Support for volatile individual sector lock Read command, Instruction=E0h	0=not supported 1=supported	C2h	16	1b	FFh
Support for volatile individual sector lock Write command, Instruction=E1h	0=not supported 1=supported		17	1b	
Support for non-volatile individual sector lock read command, Instruction=E2h	0=not supported 1=supported		18	1b	
Support for non-volatile individual sector lock write command, Instruction=E3h	0=not supported 1=supported		19	1b	
Reserved	Reserved		23:20	1111b	
Reserved	Reserved	C3h	31:24	FFh	FFh
Instruction for Erase Type 1	FFh=not supported	C4h	07:00	21h	21h
Instruction for Erase Type 2	FFh=not supported	C5h	15:08	5Ch	5Ch
Instruction for Erase Type 3	FFh=not supported	C6h	23:16	DCh	DCh
Instruction for Erase Type 4	FFh=not supported	C7h	31:24	FFh	FFh

Table 16. Parameter Table (2): Macronix Flash Parameter Tables

SFDP Table below is for MX25U51245GMI and MX25U51245GXDI

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	111h:110h	07:00 15:08	00h 20h	00h 20h
Vcc Supply Minimum Voltage	1650h=1.650V, 1750h=1.750V 2250h=2.250V, 2300h=2.300V 2350h=2.350V, 2650h=2.650V 2700h=2.700V	113h: 112h	23:16 31:24	00h 17h	00h 17h
H/W Reset# pin	0=not supported 1=supported	115h: 114h	00	1b	F99Dh
H/W Hold# pin	0=not supported 1=supported		01	0b	
Deep Power Down Mode	0=not supported 1=supported		02	1b	
S/W Reset	0=not supported 1=supported		03	1b	
S/W Reset Instruction	Reset Enable (66h) should be issued before Reset Instruction		11:04	1001 1001b (99h)	
Program Suspend/Resume	0=not supported 1=supported		12	1b	
Erase Suspend/Resume	0=not supported 1=supported		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not supported 1=supported		15	1b	
Wrap-Around Read mode Instruction		116h	23:16	C0h	C0h
Wrap-Around Read data length	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B	117h	31:24	64h	64h
Individual block lock	0=not supported 1=supported	11Bh: 118h	00	1b	CB85h
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Instruction			09:02	1110 0001b (E1h)	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not supported 1=supported		11	1b	
Read Lock	0=not supported 1=supported		12	0b	
Permanent Lock	0=not supported 1=supported		13	0b	
Unused			15:14	11b	
Unused			31:16	FFh	FFh
Unused		11Fh: 11Ch	31:00	FFh	FFh

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg, read performance enhance toggling bits)

Note 5: 4KB=2⁰Ch, 32KB=2⁰Fh, 64KB=2¹0h

Note 6: All unused and undefined area data is blank FFh for SFDP Tables that are defined in Parameter Identification Header. All other areas beyond defined SFDP Table are reserved by Macronix.

12. RESET

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After reset cycle, the device is at the following states:

- Standby mode
- All the volatile bits such as WEL/WIP/SRAM lock bit will return to the default status as power on.
- 3-byte address mode

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SO data becomes high impedance and the current will be reduced to minimum.

Figure 103. RESET Timing

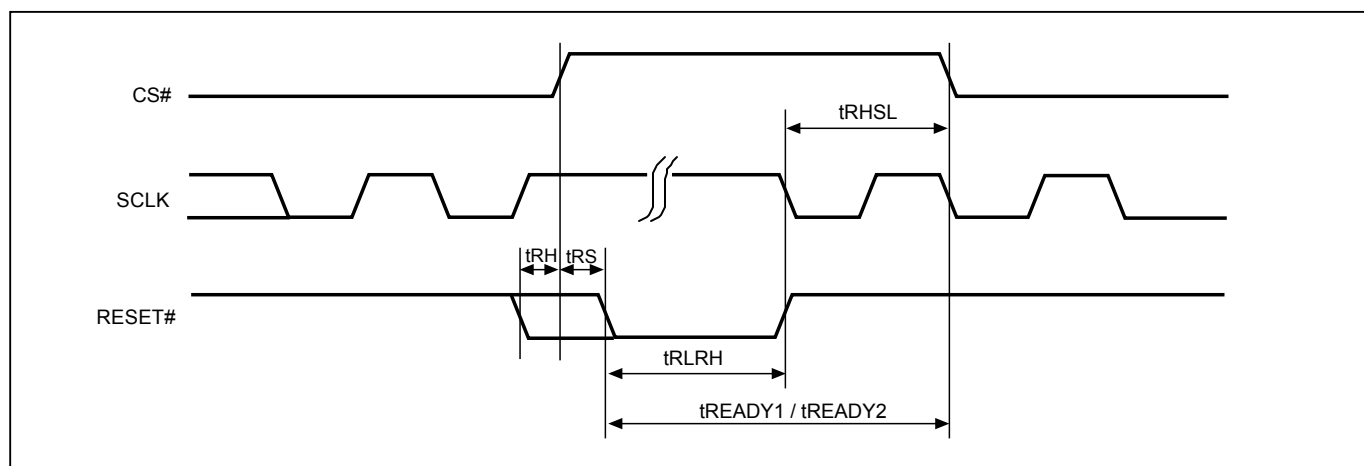


Table 17. Reset Timing-(Power On)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY1	Reset Recovery time	35			us

Table 18. Reset Timing-(Other Operation)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY2	Reset Recovery time (During instruction decoding)	40			us
	Reset Recovery time (for read operation)	40			us
	Reset Recovery time (for program operation)	310			us
	Reset Recovery time(for SE4KB operation)	12			ms
	Reset Recovery time (for BE64K/BE32KB operation)	25			ms
	Reset Recovery time (for Chip Erase operation)	1000			ms
	Reset Recovery time (for WRSR operation)	40			ms

13. POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the "[power-up timing](#)".

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

14. ELECTRICAL SPECIFICATIONS

Table 19. ABSOLUTE MAXIMUM RATINGS

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 2.5V

NOTICE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
- Specifications contained within the following tables are subject to change.
- During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 104. Maximum Negative Overshoot Waveform

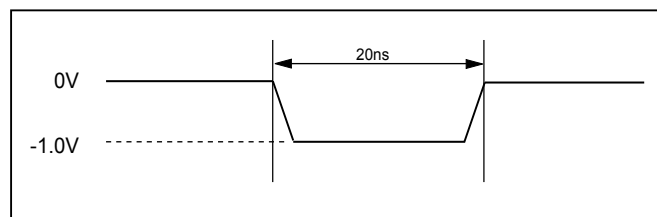


Figure 105. Maximum Positive Overshoot Waveform

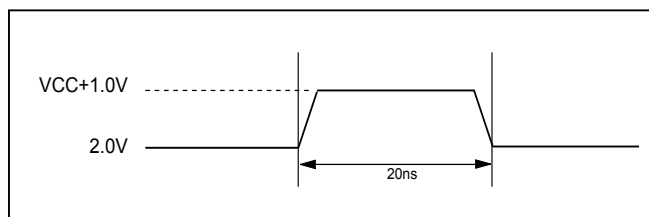


Table 20. CAPACITANCE TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			16	pF	VIN = 0V
COUT	Output Capacitance			16	pF	VOOUT = 0V

Figure 106. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

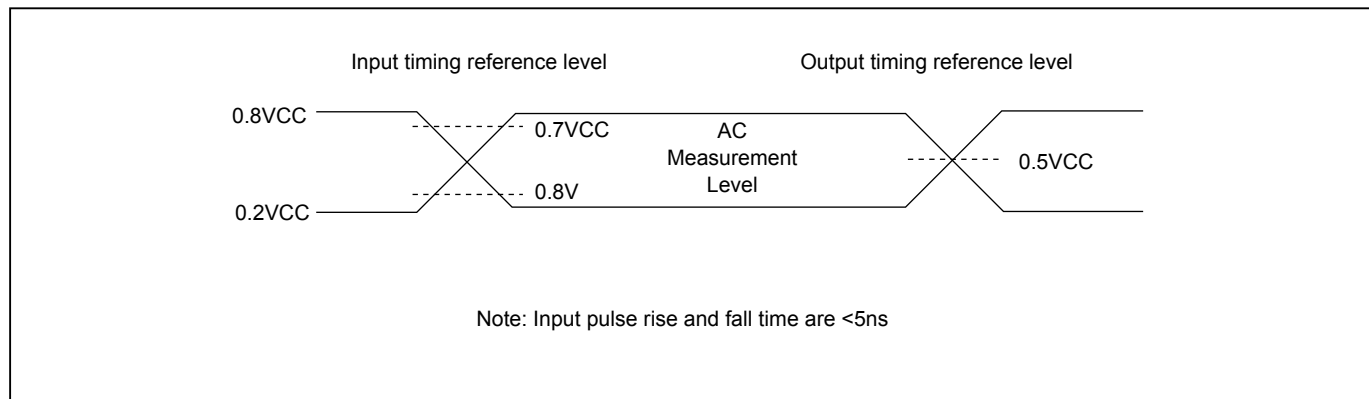


Figure 107. OUTPUT LOADING

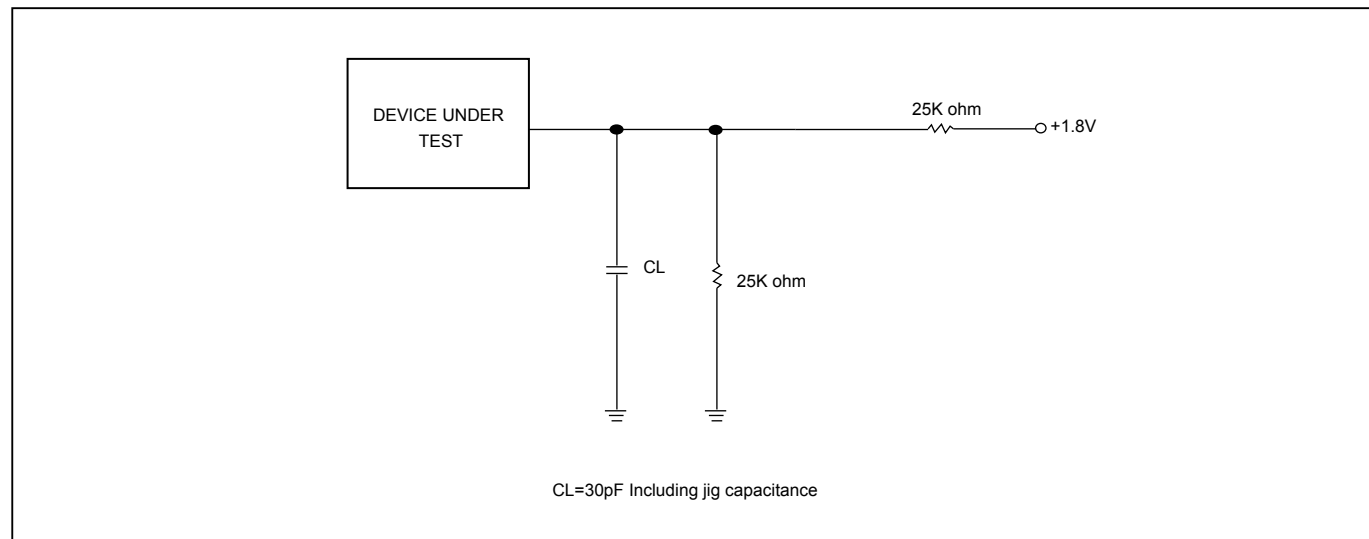


Table 21. DC CHARACTERISTICS

Temperature = -40°C to 85°C, VCC = 1.7V ~ 2.0V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOU = VCC or GND
ISB1	VCC Standby Current	1		20	100	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			5	20	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read (Note 3)	1			30	mA	f=100MHz, (DTR 4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					20	mA	f=104MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					15	mA	f=84MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		40	60	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	40	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K)	1		40	60	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		40	60	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.4		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :

1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. Pattern = Blank

Table 22. AC CHARACTERISTICS

Temperature = -40°C to 85°C, VCC = 1.7V ~ 2.0V

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for all commands(except Read Operation)	D.C.		133	MHz
fRCLK	fR	Clock Frequency for READ instructions			66	MHz
fTCLK		Clock Frequency for FAST READ, DREAD, 2READ, QREAD, 4READ, 4DTRD	see "Dummy Cycle and Frequency Table (MHz)"			MHz
tCH ⁽¹⁾	tCLH	Clock High Time	Others (fSCLK)	45% fTCLK		ns
			Normal Read (fRCLK)	7		ns
tCL ⁽¹⁾	tCLL	Clock Low Time	Others (fSCLK)	45% fTCLK		ns
			Normal Read (fRCLK)	7		ns
tCLCH ⁽²⁾		Clock Rise Time (peak to peak)	0.1			V/ns
tCHCL ⁽²⁾		Clock Fall Time (peak to peak)	0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	3			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	4			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	2			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	3			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	3			ns
tSHSL	tCSH	CS# Deselect Time	Read	7		ns
			Write/Erase/Program	30		ns
tSHQZ ⁽²⁾	tDIS	Output Disable Time			8	ns
tCLQV	tV	Clock Low to Output Valid	Loading: 30pF		8	ns
			Loading: 15pF		6	ns
			Loading: 10pF		5	ns
tCLQX	tHO	Output Hold Time	1			ns
tWHSL ⁽³⁾		Write Protect Setup Time	20			ns
tSHWL ⁽³⁾		Write Protect Hold Time	100			ns
tDP ⁽²⁾		CS# High to Deep Power-down Mode			10	us
tRES1 ⁽²⁾		CS# High to Standby Mode without Electronic Signature Read			30	us
tRES2 ⁽²⁾		CS# High to Standby Mode with Electronic Signature Read			30	us
tW		Write Status/Configuration Register Cycle Time			40	ms
tWREAW		Write Extended Address Register		40		ns
tBP		Byte-Program		25	60	us
tPP		Page Program Cycle Time		0.25	0.75	ms
tPP ⁽⁵⁾		Page Program Cycle Time (n bytes)		0.016 + 0.016* (n/16) ⁽⁶⁾	0.75	ms
tSE		Sector Erase Cycle Time		30	200	ms
tBE32		Block Erase (32KB) Cycle Time		150	1000	ms
tBE		Block Erase (64KB) Cycle Time		280	2000	ms
tCE		Chip Erase Cycle Time		200	600	s
tESL ⁽⁸⁾		Erase Suspend Latency			25	us
tPSL ⁽⁸⁾		Program Suspend Latency			25	us
tPRS ⁽⁹⁾		Latency between Program Resume and next Suspend	0.3	100		us
tERS ⁽¹⁰⁾		Latency between Erase Resume and next Suspend	0.3	400		us

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Test condition is shown as [Figure 106](#) and [Figure 107](#).
5. While programming consecutive bytes, Page Program instruction provides optimized timings by selecting to program the whole 256 bytes or only a few bytes between 1~256 bytes.
6. "n"=how many bytes to program. The number of (n/16) will be round up to next integer. In the formula, while n=1, byte program time=32us. While n=17, byte program time=48us.
7. By default dummy cycle value. Please refer to the ["Table 1. Read performance Comparison"](#).
8. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
9. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
10. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.

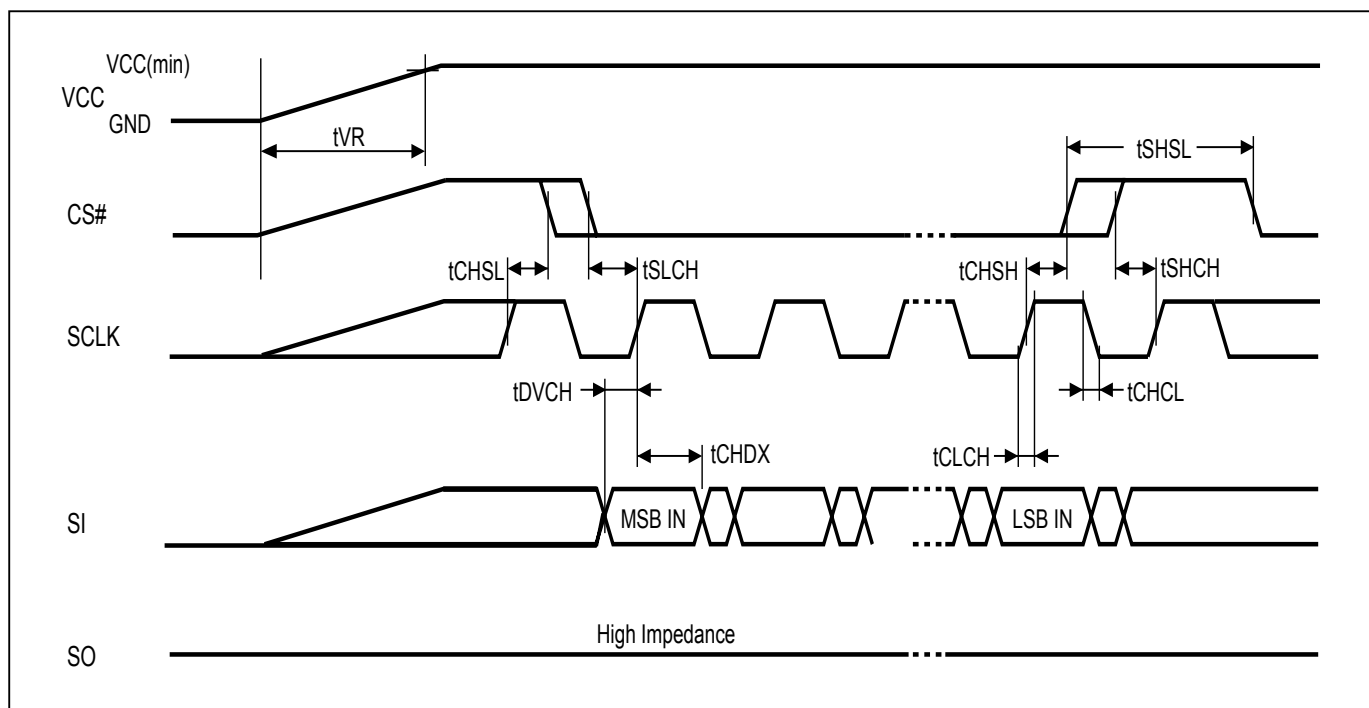
15. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in [Figure 108](#) and [Figure 109](#) are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 108. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to ["Table 22. AC CHARACTERISTICS"](#).

Figure 109. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

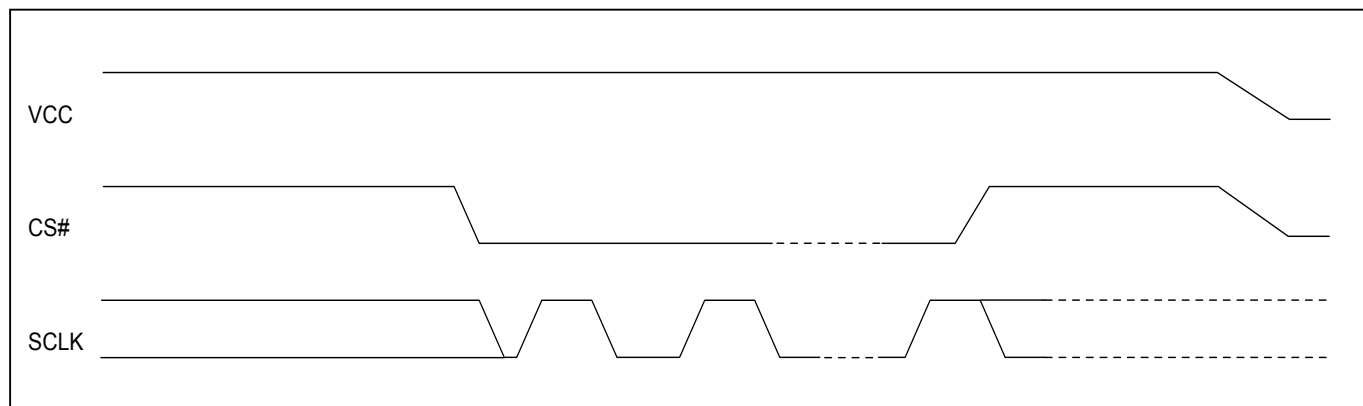
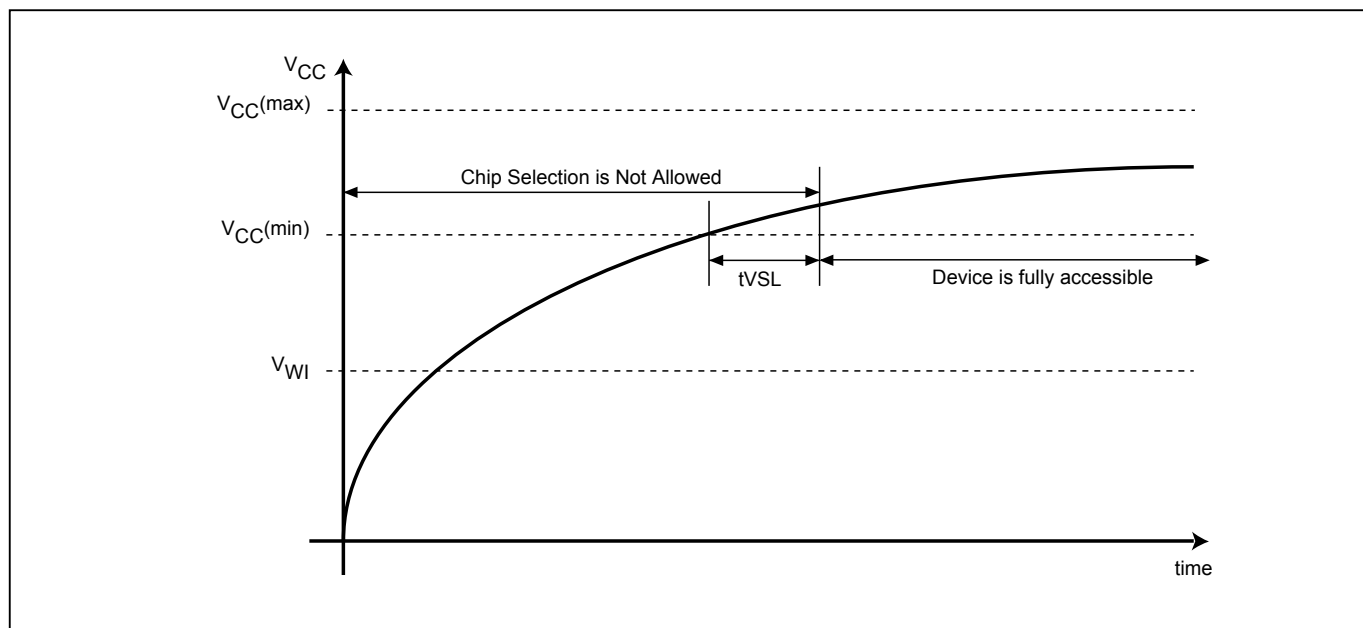
**Figure 110. Power-up Timing**

Figure 111. Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below V_{PVD} for at least t_{PVD} timing. Please check the table below for more detail.

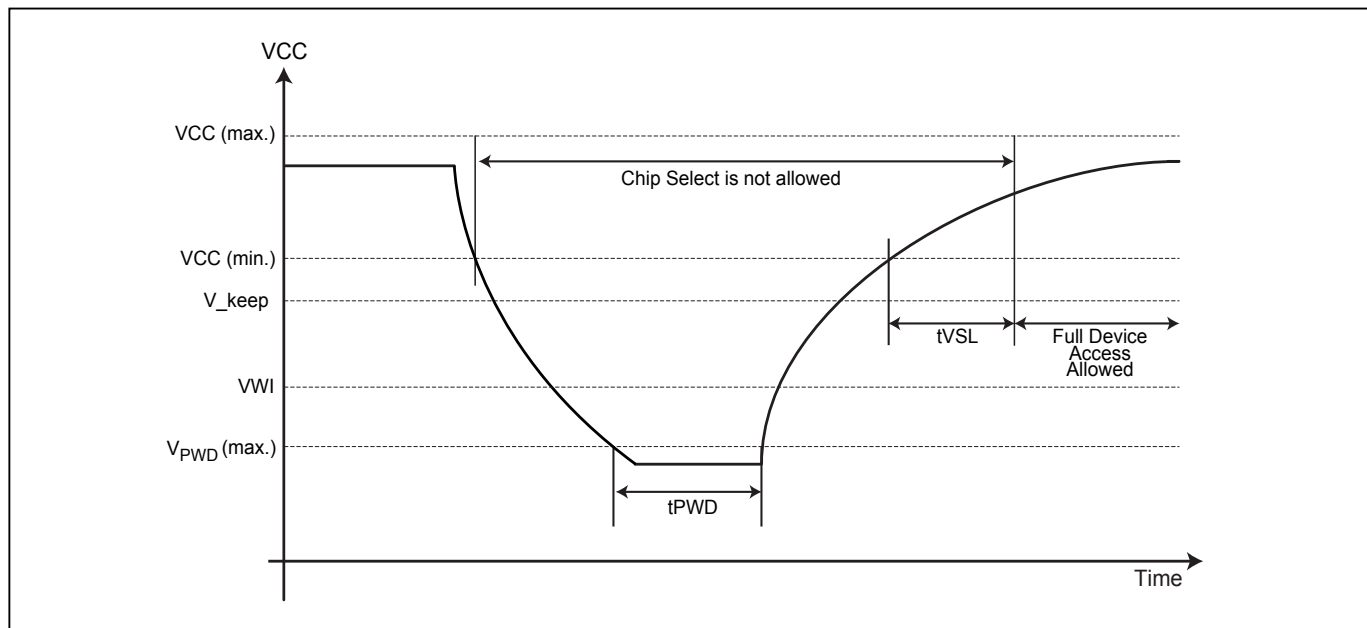


Table 23. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
V_{PVD}	VCC voltage needed to below V_{PVD} for ensuring initialization will occur		0.8	V
V_{keep}	Voltage that a re-initialization is necessary if VDD drop below to V_{KEEP}	1.5		V
t_{PVD}	The minimum duration for ensuring initialization will occur	300		us
t_{VSL}	VCC(min.) to device operation	3		ms
t_{VR}	VCC Rise Time	20	500000	us/V
VCC	VCC Power Supply	1.7	2.0	V
VWI	Write Inhibit Voltage	1.0	1.4	V

15-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

16. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. ⁽¹⁾	Max. ⁽²⁾	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		30	200	ms
Block Erase Cycle Time (32KB)		0.15	1	s
Block Erase Cycle Time (64KB)		0.28	2	s
Chip Erase Cycle Time		200	600	s
Byte Program Time (via page program command)		25	60	us
Page Program Time		0.25	0.75	ms
Erase/Program Cycle		100,000		cycles

Note:

1. Typical program and erase time assumes the following conditions: 25°C, 1.8V, and checkerboard pattern.
2. Under worst conditions of 85°C and 1.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0°C, VCC=1.8V, and 100K cycle with 90% confidence level.

17. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55°C	20		years

18. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 1.8V, one pin at a time.		



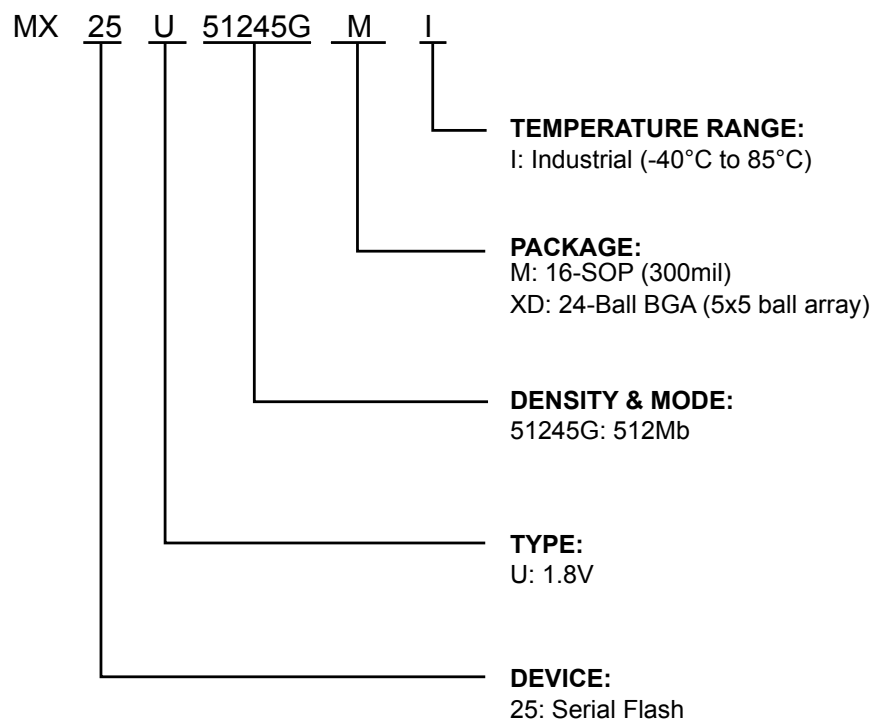
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MX25U51245G

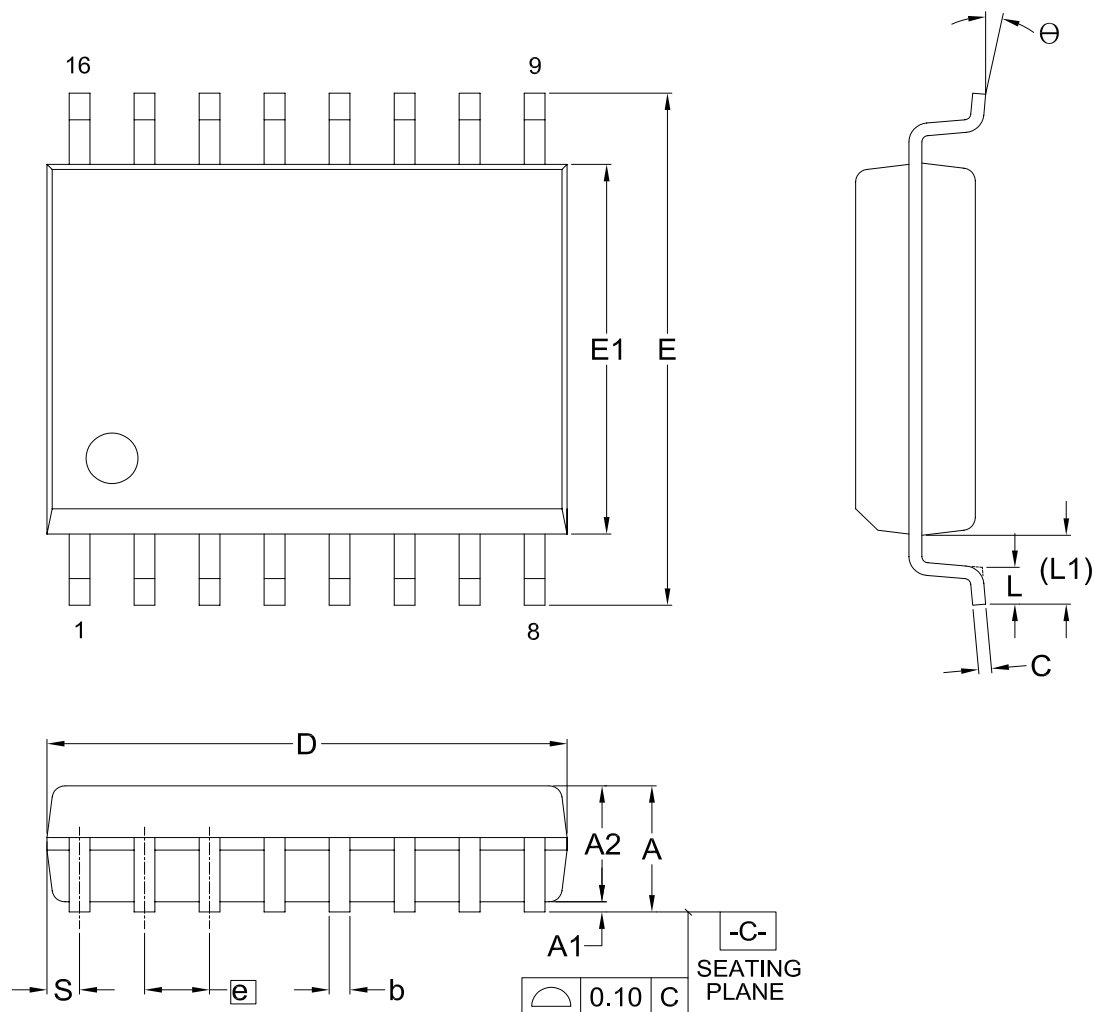
19. ORDERING INFORMATION

PART NO.	TEMPERATURE	PACKAGE	Remark
MX25U51245GMI	-40°C~85°C	16-SOP (300mil)	
MX25U51245GXDI	-40°C~85°C	24-Ball BGA (5x5 ball array)	

20. PART NAME DESCRIPTION

21. PACKAGE INFORMATION

Doc. Title: Package Outline for SOP 16L (300MIL)



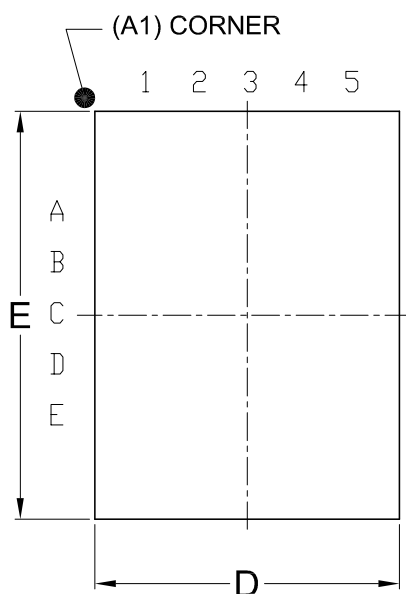
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
UNIT														
mm	Min.	---	0.10	2.25	0.31	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0°
	Nom.	---	0.20	2.35	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5°
	Max.	2.65	0.30	2.45	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8°
Inch	Min.	---	0.004	0.089	0.012	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0°
	Nom.	---	0.008	0.093	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5°
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8°

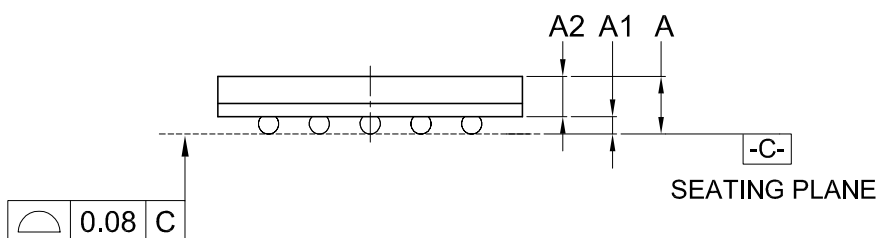
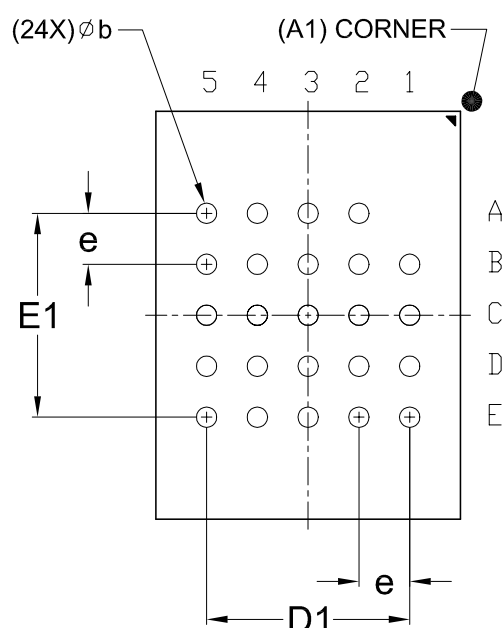
Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1402	13	MS-013			

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)

TOP VIEW



BOTTOM VIEW



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	e
UNIT										
mm	Min.	---	0.25	0.65	0.35	5.90	---	7.90	---	---
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	4.00	1.00
	Max.	1.20	0.35	---	0.45	6.10	---	8.10	---	---
Inch	Min.	---	0.010	0.026	0.014	0.232	---	0.311	---	---
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.157	0.039
	Max.	0.047	0.014	---	0.018	0.240	---	0.319	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4257.1	1				



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MX25U51245G

22. REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Content correction	P13,24,30	MAY/22/2015

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