3.3.1. Instruction summary

Table 3.64 Shows a summary of CP instructions that the processor can use.

Table 3.64. Summary of CP15 instructions

Instruction	Operation	Reference
`MRC p15, 0, <Rd>, c0, c0, 0`	Read ID Code	*c0, Main ID Register*
`MRC p15, 0, <Rd>, c0, c0, 1`	Read Cache Type	*c0, Cache Type Register*
`MRC p15, 0, <Rd>, c0, c0, 2`	Read TCM status	*c0, TCM Status Register*
`MRC p15, 0, <Rd>, c0, c0, 4`	Read MPU	*c0, MPU Type Register*
`MRC p15, 0, <Rd>, c0, c1-c2, {0-7}`	Read Feature Id Registers	*c0, Core feature ID registers*
`MRC p15, 0, <Rd>, c1, c0, 0` `MCR p15, 0, <Rd>, c1, c0, 0`	Read Control Register configuration data Write Control Register configuration data	*c1, Control Register*
`MRC p15, 0, <Rd>, c1, c0, 1` `MCR p15, 0, <Rd>, c1, c0, 1`	Read Auxiliary Control Register configuration data Write Auxiliary Control Register configuration data	*c1, Auxiliary Control Register*
`MRC p15, 0, <Rd>, c1, c0, 2` `MCR p15, 0, <Rd>, c1, c0, 2`	Read Coprocessor Access Control Register configuration data Write Coprocessor Access Control Register configuration data	*c1, Coprocessor Access Control Register*
`MRC p15, 0, <Rd>, c5, c0, 0` `MCR p15, 0, <Rd>, c5, c0, 0`	Read Data Fault Status Register Write Data Fault Status Register	*c5, Data Fault Status Register*
`MRC p15, 0, <Rd>, c5, c0, 1` `MCR p15, 0, <Rd>, c5, c0, 1`	Read Instruction Fault Status Register Write Instruction Fault Status Register	*c5, Instruction Fault Status Register*
`MRC p15, 0, <Rd>, c6, c0, 0` `MCR p15, 0, <Rd>, c6, c0, 0`	Read Fault Address Register Write Fault Address Register	*c6, Fault Address Register*
`MRC p15, 0, <Rd>, c6, c0, 1` `MCR p15, 0, <Rd>, c6, c0, 1`	Read Watchpoint Fault Address Register Write Watchpoint Fault Address Register	*c6, Watchpoint Fault Address Register*

MRC p15, 0, <Rd>, c6, c0, 2 MCR p15, 0, <Rd>, c6, c0, 2	Read Instruction Fault Address Register Write Instruction Fault Address Register	*c6, Instruction Fault Address Register*
MRC p15, 0, <Rd>, c6, c1, 0 MCR p15, 0, <Rd>, c6, c1, 0	Read Data Region Base Address Register Write Data Region Base Address Register	*c6, Region Base Address Register*
MRC p15, 0, <Rd>, c6, c1, 2 MCR p15, 0, <Rd>, c6, c1, 2	Read Region Size and Enable Register Write Region Size and Enable Register	*c6, Region Size and Enable Register*
MRC p15, 0, <Rd>, c6, c1, 4 MCR p15, 0, <Rd>, c6, c1, 4	Read Region Access Control Register Write Region Access Control Register	*c6, Region Access Control Register*
MRC p15, 0, <Rd>, c6, c2, 0 MCR p15, 0, <Rd>, c6, c2, 0	Read Memory Region Number Register Write Memory Region Number Register	*c6, Memory Region Number Register*
MCR p15, 0, <Rd>, c7, c0, 4	Wait For Interrupt	*Wait For Interrupt operation*
MCR p15, 0, <Rd>, c7, c5, 0	Invalidate entire Instruction Cache	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c5, 1	Invalidate Instruction Cache line using address	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c5, 2	Invalidate Instruction Cache line using Set/ Way	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c5, 4	Flush Prefetch Buffer	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c6, 0	Invalidate Entire Data Cache	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c6, 1	Invalidate Data Cache line using address	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c6, 2	Invalidate Data Cache line using Set/ Way	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c7, 0	Invalidate both caches	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c10, 0	Clean Entire Data Cache	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c10, 1	Clean Data Cache Line using address	*Invalidate, Clean, and Prefetch operations*
MCR p15, 0, <Rd>, c7, c10, 2	Clean Data Cache Line using	*Invalidate, Clean, and Prefetch*

	Set/ Way	*operations*
`MCR p15, 0, <Rd>, c7, c10, 4`	Drain Write Buffer	*Invalidate, Clean, and Prefetch operations*
`MCR p15, 0, <Rd>, c7, c10, 5`	Data Memory Barrier	*Invalidate, Clean, and Prefetch operations*
`MRC p15, 0, <Rd>, c7, c10, 6`	Read Cache Dirty Status	*c7, Cache Dirty Status Register*
`MCR p15, 0, <Rd>, c7, c13, 1`	Prefetch Instruction Cache Line	*Flush operations*
`MCR p15, 0, <Rd>, c7, c14, 0`	Write Clean and Invalidate Entire Data Cache	*Invalidate, Clean, and Prefetch operations*
`MCR p15, 0, <Rd>, c7, c14, 1`	Write Clean and Invalidate Data Cache Line using address	*Invalidate, Clean, and Prefetch operations*
`MCR p15, 0, <Rd>, c7, c14, 2`	Write Clean and Invalidate Data Cache Line using Set/ Way	*Invalidate, Clean, and Prefetch operations*
`MRC p15, 0, <Rd>, c9, c0, 0` `MCR p15, 0, <Rd>, c9, c0, 0`	Read Data Cache Lockdown Register Write Data Cache Lockdown Register	*c9, Data and instruction cache lockdown registers*
`MRC p15, 0, <Rn>, c9, c0, 1` `MCR p15, 0, <Rn>, c9, c0, 1`	Read Instruction Cache Lockdown Register Write Instruction Cache Lockdown Register	*c9, Data and instruction cache lockdown registers*
`MRC p15, 0, <Rd>, c9, c1, 0` `MCR p15, 0, <Rd>, c9, c1, 0`	Read Data TCM Region Register Write Data TCM Region Register	*c9, Data TCM Region Register*
`MRC p15, 0, <Rd>, c9, c1, 1` `MCR p15, 0, <Rd>, c9, c1, 1`	Read Instruction TCM Region Register Write Instruction TCM Region Register	*c9, Instruction TCM Region Register*
`MRC p15, 0, <Rd>, c13, c0, 1` `MCR p15, 0, <Rd>, c13, c0, 1`	Read Process ID Write Process ID	*c13, Process ID Register*
`MRC p15, 0, <Rd>, c15, c12, 0` `MCR p15, 0, <Rd>, c15, c12, 0`	Read Performance Monitor Control Register Write Performance Monitor Control Register	*c15, Performance Monitor Control Register*
`MRC p15, 0, <Rd>, c15, c12, 1` `MCR p15, 0, <Rd>, c15, c12, 1`	Read Cycle Counter Register Write Cycle Counter Register	*c15, Cycle Counter Register*
`MRC p15, 0, <Rd>, c15, c12, 2`	Read Count Register 0	*c15, Count Register 0*

`MCR p15, 0, <Rd>, c15, c12, 2`	Write Count Register 0	
`MRC p15, 0, <Rd>, c15, c12, 3`	Read Count Register 1	*c15, Count Register 1*
`MCR p15, 0, <Rd>, c15, c12, 3`	Write Count Register 1	
`MRC p15, 3, <Rd>, c15, c0, 0`	Read Data Cache Debug Register	*c15, Data Cache Debug Register*
`MCR p15, 3, <Rd>, c15, c0, 0`	Write Data Cache Debug Register	
`MRC p15, 3, <Rd>, c15, c0, 1`	Read Instruction Cache Debug Register	*c15, Instruction Cache Debug Register*
`MCR p15, 3, <Rd>, c15, c0, 1`	Write Instruction Cache Debug Register	
`MCR p15, 3, <Rd>, c15, c2, 0`	Data Tag RAM Read Operation	*c15, Data cache Tag RAM operation*
`MCR p15, 3, <Rd>, c15, c2, 1`	Instruction cache Tag RAM Read Operation	*c15, Instruction cache Tag RAM operation*
`MCR p15, 3, <Rd>, c15, c2, 2`	Data Tag RAM Parity Read Operation	*c15, Tag RAM parity read operation*
`MCR p15, 3, <Rd>, c15, c2, 3`	Instruction cache Tag RAM Parity Read Operation	*c15, Tag RAM parity read operation*
`MCR p15, 3, <Rd>, c15, c4, 1`	Instruction Cache Data RAM Read Operation	*c15, Instruction Cache Data RAM operation*
`MCR p15, 3, <Rd>, c15, c4, 2`	Data Cache Data RAM Parity Read Operation	*c15, Cache Data RAM parity read operations*
`MCR p15, 3, <Rd>, c15, c4, 3`	Instruction Cache Data RAM Parity Read Operation	*c15, Cache Data RAM parity read operations*
`MRC p15, 3, <Rd>, c15, c8, <R>`[1]	Read Instruction Cache Master Valid Register	*c15, Instruction Cache Master Valid Register*
`MCR p15, 3, <Rd>, c15, c8, <R>`[a]	Write Instruction Cache Master Valid Register	
`MRC p15, 3, <Rd>, c15, c12, <R>`[a]	Read Data Cache Master Valid Register	*c15, Data Cache Master Valid Register*
`MCR p15, 3, <Rd>, c15, c12, <R>`[a]	Write Data Cache Master Valid Register	
`MRC p15, 7, <Rd>, c15, c0, 0`	Read Cache Debug Control Register	*c15, Cache Debug Control Register*
`MRC p15, 7, <Rd>, c15, c0, 0`	Write Cache Debug Control Register	
`MCR p15, 7, <Rd>, c15, c2, 0`	Write Data Tag RAM operation	*c15, Data cache Tag RAM operation*
`MCR p15, 7, <Rd>, c15, c2, 1`	Write Instruction cache Tag RAM operation	*c15, Instruction cache Tag RAM operation*

`MCR p15, 7, <Rd>, c15, c2, 2`	Write Data Valid RAM and Dirty RAM operation	*c15, Data Cache Valid RAM and Dirty RAM bit write operation*
`MCR p15, 7, <Rd>, c15, c4, 1`	Write Instruction Cache Data RAM	*c15, Instruction Cache Data RAM operation*

[1] Register number