# F75111R/F75111RG/F75111N

## Low Power GPIO Datasheet



**Release Date: July, 2007**
**Revision: V0.27P**

## F75111 Datasheet Revision History

| Version | Date | Page | Revision History |
|---|---|---|---|
| 0.20P | 01/04/2003 | | Internal Use Preliminary Public Version |
| 0.21P | 09/04/2003 | 6~8 | Add F75111N pin configuration and description |
| 0.22P | 02/06/2003 | 7~8<br>38~39 | (1) Revised pin description of LED function<br>(2) Revised electron characteristic(operating temperature)<br>(3) Revised DC spec (Input high/low leakage current) |
| 0.23P | 12/29/2003 | 21,28 | Update register description( Index 0x18, 0x28) |
| 0.24P | 4/26/2004 | 7,8 | Update pin description of GPIO pin |
| 0.25P | 1/12/2005 | 8,9 | Revise SMBus access timing |
| 0.26P | 7/14/2005 | 36,39 | Modify AC Characteristics and delete version ID register |
| 0.27P | 7/5/2007 | - | Add company address |

## *Table of Contents*

# 1. General Description

F75111 is a low power general purpose IO chip providing 20 GPIO. Most GPIO pins can be programmed to be power LED. Level or pulse modes can be programmed by registers. Two power-down modes (manual or Smart) can be selected to save power and control the total consumption under 10uA, so F75111 can fit the requirement of mobile device such as Smart Phone, PDA or cell phone.

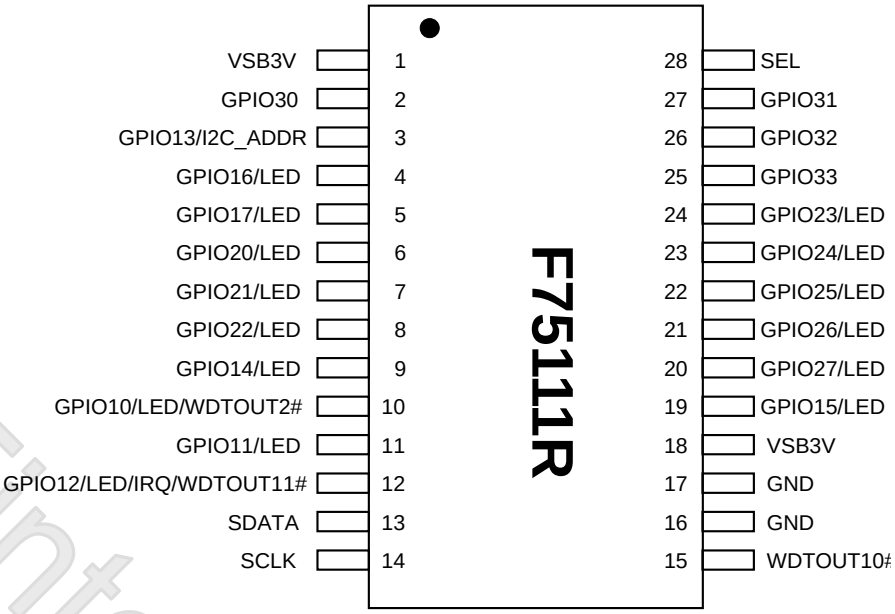
# 2. Features

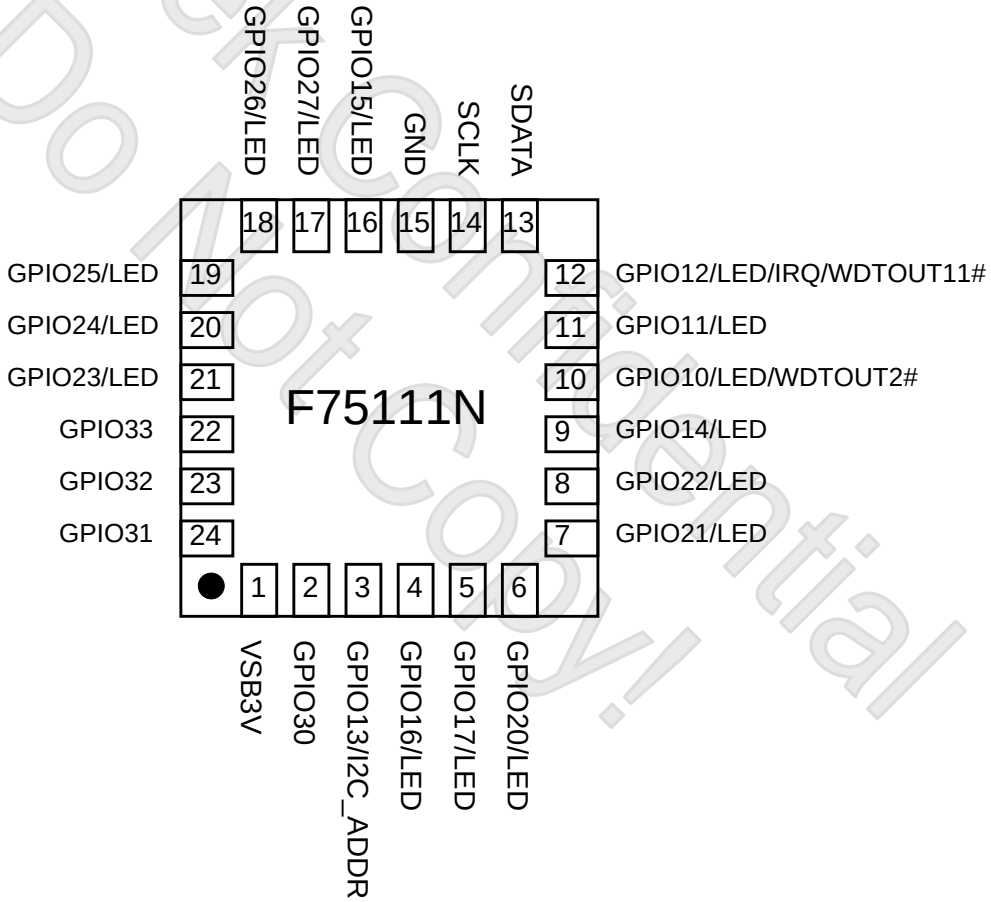
- Support up to 20 GPIO pins
- Two power down mode selection --- Manual or Smart Power Management mode
- 15 pins can be programmed to be LED
- Each GPIO pin can be programmed to be high/low level or pulse
- Each GPIO pin has de-bounce function
- Two sets of watch dog timer
- SMBus address selected pin to expand up to 2 devices
- SMBus interface
- 3VCC operation
- Package in 28-SSOP(150mil) / 24QFN package(4mm x 4mm)

# 3. Key Specifications

| | |
|---|---|
| Supply Voltage | 3.0V to 3.6V |
| Operating Supply Current | 300uA typ. |
| Power Down Current | 3uA typ. |

# 4. Pin Configuration



# 5. Pin Description

$I/O_{12t}$ - TTL level bi-directional pin with 12 mA source-sink capability

$I/O_{12ts}$ - TTL level and schmitt trigger

$I/OOD_{12t}$ - TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability

$I/OD_{12}$ - TTL level bi-directional pin, Open-drain outpu with 12 mA sink capability

$OUT_{12}$ - Output pin with 12 mA source-sink capability

$I/O_{14t}$ - TTL level bi-directional pin with 14 mA source-sink capability

$I/OOD_{16t}$ - TTL level bi-directional pin, can select to OD or OUT by register, with 16 mA source-sink capability

$OD_{12}$ - Open-drain output pin with 12 mA sink capability

$OD_{14}$ - Open-drain output pin with 14 mA sink capability

$OD_{14ts}$ - Open-drain output pin with 14 mA sink capability, TTL level and schmitt trigger

$IN_t$ - TTL level input pin

$IN_{ts}$ - TTL level input pin and schmitt trigger

P - Power

## 5.1 Power Pin

| Pin No. | | Pin Name | Type | Description |
|---|---|---|---|---|
| F75111R/RG | F75111N | | | |
| 1,18 | 1 | VSB3V | P | Standard Power Supply Voltage Input with 3.3V |
| 16,17 | 15 | GND | P | GND |

## 5.2 GPIO Function

| Pin No. | | Pin Name | Type | Description |
|---|---|---|---|---|
| F75111R/RG | F75111N | | | |
| 4 ~ 9 | 4 ~ 9 | GPIO16/17/20/21/22/14 | $I/OOD_{16ts}$ (5V Tolerance) | General purpose I/O pins. |
| | | LED | $OD_{16}$ | LED control output. The multi-function pin is selected by register, so does the freq. programming |
| 19~24 | 16~21 | GPIO15/27/26/25/24/23 | $I/OOD_{16ts}$ (5V Tolerance) | General purpose I/O pins. |
| | | LED | $OD_{16}$ | LED control output. The multi-function pin is selected by register, so does the freq. programming |

| | | | | |
|---|---|---|---|---|
| 2, 27~25 | 2, 22~24 | GPIO30/33/32/31 | $I/OD_{12ts}$ (5V Tolerance) | General purpose I/O pins. |
| 3 | 3 | GPIO13 | $I/O_{16ts}$ (5V Tolerance) | General purpose I/O pin. |
| | | I2C_ADDR | $IN_{tsd100k}$ | The SMBus hardware power on setting pin. Default address is 0x9C (when I2C_ADDR=0). Another one is 0x6E (when I2C_ADDR=1). This pin internal pull-down 100k to Ground. If this pin is pull-up 10k to VSB3V, this pin will be trapped to 1. |
| 10 | 10 | GPIO10 | $I/OOD_{16ts}$ (5V Tolerance) | General purpose I/O pin. |
| | | LED | $OD_{16}$ | LED control output. The multi-function pin is selected by register, so does the freq. programming |
| | | WDTOUT2# | $OD_{16}$ | The 2nd Watch Dog Timer time out output |
| 11 | 11 | GPIO11 | $I/OOD_{16ts}$ (5V Tolerance) | General purpose I/O pin. |
| | | LED | $OD_{16}$ | LED control output. The multi-function pin is selected by register, so does the freq. programming |
| 12 | 12 | GPIO12 | $I/OOD_{16ts}$ (5V Tolerance) | General purpose I/O pin. |
| | | LED | $OD_{16}$ | LED control output. The multi-function pin is selected by register, so does the freq. programming |
| | | IRQ | $OD_{16}$ | IRQ and SMI# function |
| | | WDTOUT11# | $OD_{16}$ | The 1st Watch Dog Timer time out output. System reset signal when the Reset-Out timer is time out. This pin will generate 100mS pulse (default) when the Reset-Out timer is timeout. |
| 15 | - | WDTOUT10# | $OD_{12}$ | The 1st Watch Dog Timer time out output. System reset signal when the Reset-Out timer is time out. This pin will generate 100mS pulse (default) when the Reset-Out timer is timeout. |
| 28 | - | SEL | $IN_{tsd100k}$ | Default pull down. |
| 13 | 13 | SDATA | $I/OD_{12ts}$ | SMBus data. |
| 14 | 14 | SCLK | $IN_{ts}$ | SMBus clock |

# 6. Functional Description

## 6.1 General Description

Dedicate GPIO functions. That includes two sets of watchdog timer. One Set of Watchdog timer timeout unit is set to second and range is 0 to 127 seconds. The other Watchdog timer is set to second or minute and the range is 0 to 256 seconds or minutes. When the timeout has occurred, that will generate a status bit to indicate it and write one will be clear. All GPIO can be programmed to logic one or zero or high pulse or low pulse.

## 6.2 Access Interface

The F75111 provides one serial access interface, I2C Bus, to read/write internal registers. The address of Serial Bus is configurable by using power-on trapping of standby power VBS3V. The pin 3 (GPIO13/I2C _ADDR) is multi-function pin. During the VSB3V power-on, this pin serves as input detection of logic high or logic low. This pin is default pull-down resistor with 100K ohms mapping the Serial Bus address 0x9C (1001_1100). Another Serial Bus address 0x6E (0110_1110) is set when external pull-up resistor with 10K ohms is connected in this pin.

## 6.3 The SMBus access timing are shown as follow:

***(a) SMBus write to internal address register followed by the data byte***

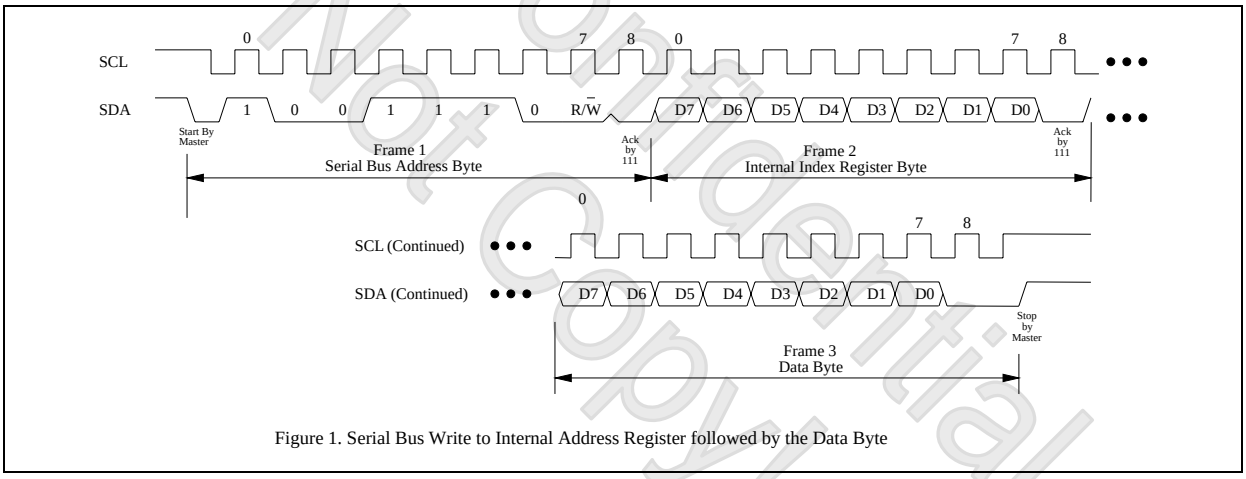



Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

***(b) Serial bus write to internal address register only***

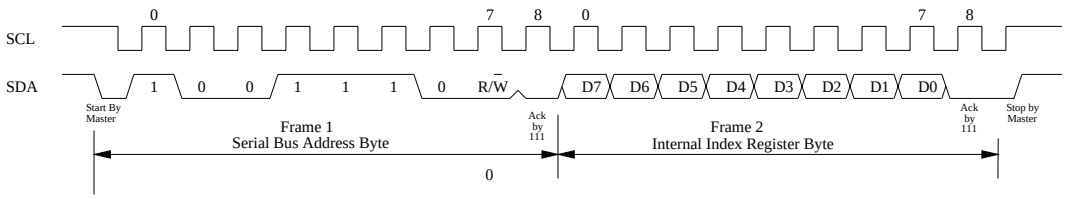



Figure 2. Serial Bus Write to Internal Address Register Only

***(c) Serial bus read from a register with the internal address register prefer to desired location***

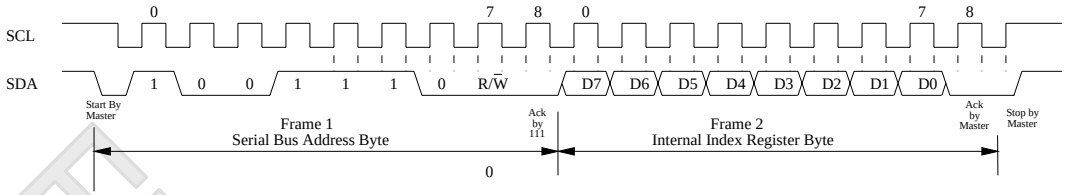



Figure 3. Serial Bus Read from Internal Address Register

# 7. Registers Description

## 7.1 Configuration and Control Register – Index 01h

Power-on default [7:0] =0000_1000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | INIT | R/W | VSB3V | Software reset for all registers including Test Mode registers. Users use only. |
| 6 | Reserved | R/W | VSB3V | |
| 5 | EN_WDT10 | R/W | VSB3V | Enable Reset Out. If set to 1, enable WDTOUT10# output. Default is disable. |
| 4 | Reserved | R/W | VSB3V | |
| 3 | Reserved | R/W | VSB3V | |
| 2 | Reserved | R/W | VSB3V | |
| 1 | SMART_POWR_MANAGEMENT | R/W | VSB3V | Set this bit to 1 will enable auto power down mode, when all function are idle then 20ms the chip will auto power down, it will wakeup when GPIO state change or read write register |
| 0 | SOFT_POWR_DOWN | R/W | VSB3V | Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0. |

## 7.2 Status Register – Index 02h

Power-on default [7:0] =0000_000xb

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | |
| 3 | POWR_DOWN | RO | VSB3V | If this bit is set to 1, it mean the chip is in power down mode |
| 2 | Reserved | RO | VSB3V | Read back will be “0” |
| 1 | I2C_ADDR | RO | VSB3V | GPIO serial bus address Select. Internal pull-down 100K ohms are address 0x9C. If external is pull-up 4.7K ohms, the address is 0x6E. This pin is trapped during the VSB3VOK. |
| 0 | Reserved | RO | VSB3V | |

## 7.3 Configuration and function select Register – Index 03h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | Reserved | RO | VSB3V | |
| 6 | IRQ_LEVEL | R/W | VSB3V | Select IRQ Polarity (Level). Set to 1, IRQ is low active and SMI# is high active. Default, the IRQ is high active and SMI# is low active. |
| 5 | IRQ_MODE | R/W | VSB3V | IRQ/SMI# mode select. 0 – Level mode (IRQ mode), 1 – Pulse Mode (SMI# mode). If pulse mode is selected, the active pulse is over 100us. |
| 4-3 | PIN12_MODE | R/W | VSB3V | 00: GPIO12<br>01: LED12 IN this mode can use REG 0x06(bit5,4) to select LED frequency.<br>10: IRQ<br>11: WDTOUT11#: |
| 2 | PIN11_MODE | R/W | VSB3V | 0: GPIO11<br>1: LED11 IN this mode can use REG 0x06(bit3,2) to select LED frequency. |
| 1-0 | PIN10_MODE | R/W | VSB3V | 00: GPIO10<br>01: LED10 IN this mode can use REG 0x06(bit1,0) to select LED frequency.<br>10,11: WD_OUT |

## 7.4 Pin mode function select Register – Index 04h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | PIN20_MODE | R/W | VSB3V | 0: GPIO27<br>1: LED27 IN this mode can use REG 0x09(bit7, 6) to select LED frequency. |
| 6 | PIN19_MODE | R/W | VSB3V | 0: GPIO15<br>1: LED15 IN this mode can use REG 0x07(bit3, 2) to select LED frequency. |
| 5 | PIN9_MODE | R/W | VSB3V | 0: GPIO14<br>1: LED14 IN this mode can use REG 0x07(bit1, 0) to select LED frequency. |
| 4 | PIN8_MODE | R/W | VSB3V | 0: GPIO22<br>1: LED22 IN this mode can use REG 0x08(bit5, 4) to select LED frequency. |
| 3 | PIN7_MODE | R/W | VSB3V | 0: GPIO21<br>1: LED21 IN this mode can use REG 0x08(bit3, 2) to select LED frequency. |
| 2 | PIN6_MODE | R/W | VSB3V | 0: GPIO20<br>1: LED20 IN this mode can use REG 0x08(bit1, 0) to select LED frequency. |
| 1 | PIN5_MODE | R/W | VSB3V | 0: GPIO17<br>1: LED17 IN this mode can use REG 0x07(bit7, 6) to select LED frequency. |
| 0 | PIN4_MODE | R/W | VSB3V | 0: GPIO16<br>1: LED16 IN this mode can use REG 0x07(bit5, 4) to select LED frequency. |

## 7.5 Pin mode function select Register – Index 05h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | | |
| 3 | PIN24_MODE | R/W | VSB3V | 0: GPIO23 |

| | | | | |
|---|---|---|---|---|
| | | | | 1: LED23 IN this mode can use REG 0x08(bit7, 6) to select LED frequency. |
| 2 | PIN23_MODE | R/W | VSB3V | 0: GPIO24<br>1: LED24 IN this mode can use REG 0x09(bit1, 0) to select LED frequency. |
| 1 | PIN22_MODE | R/W | VSB3V | 0: GPIO25<br>1: LED25 IN this mode can use REG 0x09(bit3, 2) to select LED frequency. |
| 0 | PIN21_MODE | R/W | VSB3V | 0: GPIO26<br>1: LED26 IN this mode can use REG 0x09(bit5, 4) to select LED frequency. |

## 7.6 LED Freq Control Register – Index 06h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-6 | Reserved | R/W | VSB3V | |
| 5-4 | LED12_FREQ | R/W | VSB3V | LED output frequency.<br>Bit: Description<br>00: Tri-state (default).<br>01: 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10: 1 Hz (period is 1 second)<br>11: Low. |
| 3-2 | LED11_FREQ | R/W | VSB3V | LED output frequency.<br>Bit: Description<br>00: Tri-state (default).<br>01: 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10: 1 Hz (period is 1 second)<br>11: Low. |
| 1-0 | LED10_FREQ | R/W | VSB3V | LED output frequency.<br>Bit: Description<br>00: Tri-state (default).<br>01: 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10: 1 Hz (period is 1 second)<br>11: Low. |

## 7.7 LED Freq Control Register – Index 07h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-6 | LED17_FREQ | R/W | VSB3V | LED output frequency.<br>Bit: Description<br>00: Tri-state (default).<br>01: 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10: 1 Hz (period is 1 second)<br>11: Low. |
| 5-4 | LED16_FREQ | R/W | VSB3V | LED output frequency.<br>Bit: Description<br>00: Tri-state (default).<br>01: 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10: 1 Hz (period is 1 second)<br>11: Low. |
| 3-2 | LED15_FREQ | R/W | VSB3V | LED output frequency.<br>Bit: Description<br>00: Tri-state (default).<br>01: 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10: 1 Hz (period is 1 second)<br>11: Low. |
| 1-0 | LED14_FREQ | R/W | VSB3V | LED output frequency.<br>Bit: Description<br>00: Tri-state (default).<br>01: 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10: 1 Hz (period is 1 second)<br>11: Low. |

## 7.8 LED Freq Control Register – Index 08h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|

<table>
<tr><td>7-6</td><td>LED23_FREQ</td><td>R/W</td><td>VSB3V</td><td>LED output frequency.<table><tr><td>Bit</td><td>Description</td></tr><tr><td>00</td><td>Tri-state (default).</td></tr><tr><td>01</td><td>0.5Hz (period is 2 seconds, duty cycle is 50%)</td></tr><tr><td>10</td><td>1 Hz (period is 1 second)</td></tr><tr><td>11</td><td>Low.</td></tr></table></td></tr>
<tr><td>5-4</td><td>LED22_FREQ</td><td>R/W</td><td>VSB3V</td><td>LED output frequency.<table><tr><td>Bit</td><td>Description</td></tr><tr><td>00</td><td>Tri-state (default).</td></tr><tr><td>01</td><td>0.5Hz (period is 2 seconds, duty cycle is 50%)</td></tr><tr><td>10</td><td>1 Hz (period is 1 second)</td></tr><tr><td>11</td><td>Low.</td></tr></table></td></tr>
<tr><td>3-2</td><td>LED21_FREQ</td><td>R/W</td><td>VSB3V</td><td>LED output frequency.<table><tr><td>Bit</td><td>Description</td></tr><tr><td>00</td><td>Tri-state (default).</td></tr><tr><td>01</td><td>0.5Hz (period is 2 seconds, duty cycle is 50%)</td></tr><tr><td>10</td><td>1 Hz (period is 1 second)</td></tr><tr><td>11</td><td>Low.</td></tr></table></td></tr>
<tr><td>1-0</td><td>LED20_FREQ</td><td>R/W</td><td>VSB3V</td><td>LED output frequency.<table><tr><td>Bit</td><td>Description</td></tr><tr><td>00</td><td>Tri-state (default).</td></tr><tr><td>01</td><td>0.5Hz (period is 2 seconds, duty cycle is 50%)</td></tr><tr><td>10</td><td>1 Hz (period is 1 second)</td></tr><tr><td>11</td><td>Low.</td></tr></table></td></tr>
</table>



## 7.9 LED Freq Control Register – Index 09h

Power-on default [7:0] =0000_0000b

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>PWR</th><th>Description</th></tr>
<tr><td>7-6</td><td>LED27_FREQ</td><td>R/W</td><td>VSB3V</td><td>LED output frequency.<table><tr><td>Bit</td><td>Description</td></tr></table></td></tr>
</table>

| | | | | |
|---|---|---|---|---|
| | | | | 00 Tri-state (default).<br>01 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10 1 Hz (period is 1 second)<br>11 Low. |
| 5-4 | LED26_FREQ | R/W | VSB3V | LED output frequency.<br>Bit / Description<br>00 Tri-state (default).<br>01 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10 1 Hz (period is 1 second)<br>11 Low. |
| 3-2 | LED25_FREQ | R/W | VSB3V | LED output frequency.<br>Bit / Description<br>00 Tri-state (default).<br>01 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10 1 Hz (period is 1 second)<br>11 Low. |
| 1-0 | LED24_FREQ | R/W | VSB3V | LED output frequency.<br>Bit / Description<br>00 Tri-state (default).<br>01 0.5Hz (period is 2 seconds, duty cycle is 50%)<br>10 1 Hz (period is 1 second)<br>11 Low. |



## 7.10 GPIO1x Output Control Register – Index 10h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP17_OCTRL | R/W | VSB3V | GPIO 17 output control. Set to 1 for output function. Set to 0 for input function(default). |

| | | | | |
|---|---|---|---|---|
| 6 | GP16_OCTRL | R/W | VSB3V | GPIO 16 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 5 | GP15_OCTRL | R/W | VSB3V | GPIO 15 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 4 | GP14_OCTRL | R/W | VSB3V | GPIO 14 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 3 | GP13_OCTRL | R/W | VSB3V | GPIO 13 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 2 | GP12_OCTRL | R/W | VSB3V | GPIO 12 output control. If this pin serves as IRQ/SMI#, this bit has no effect. Set to 1 for output function. Set to 0 for input function(default). |
| 1 | GP11_OCTRL | R/W | VSB3V | GPIO 11 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 0 | GP10_OCTRL | R/W | VSB3V | GPIO 10 output control. Set to 1 for output function. Set to 0 for input function(default). |

## 7.11 GPIO1x Output Data Register – Index 11h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP17_ODATA | R/W | VSB3V | GPIO 17 output data. |
| 6 | GP16_ODATA | R/W | VSB3V | GPIO 16 output data. |
| 5 | GP15_ODATA | R/W | VSB3V | GPIO 15 output data. |
| 4 | GP14_ODATA | R/W | VSB3V | GPIO 14 output data. |
| 3 | GP13_ODATA | R/W | VSB3V | GPIO 13 output data. |
| 2 | GP12_ODATA | R/W | VSB3V | GPIO 12 output data. If this pin serves as IRQ/SMI#, this bit has no effect. |
| 1 | GP11_ODATA | R/W | VSB3V | GPIO 11 output data. |
| 0 | GP10_ODATA | R/W | VSB3V | GPIO 10 output data. |

## 7.12 GPIO1x Input Status Register – Index 12h

Power-on default [7:0] =xxxx_xxxxb

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP17_PSTS | RO | VSB3V | Read the GPIO17 data on the pin. |

| | | | | |
|---|---|---|---|---|
| 6 | GP16_PSTS | RO | VSB3V | Read the GPIO16 data on the pin. |
| 5 | GP15_PSTS | RO | VSB3V | Read the GPIO15 data on the pin. |
| 4 | GP14_PSTS | RO | VSB3V | Read the GPIO14 data on the pin. |
| 3 | GP13_PSTS | RO | VSB3V | Read the GPIO13 data on the pin. |
| 2 | GP12_PSTS | RO | VSB3V | Read the GPIO12 data on the pin. |
| 1 | GP11_PSTS | RO | VSB3V | Read the GPIO11 data on the pin. |
| 0 | GP10_PSTS | RO | VSB3V | Read the GPIO10 data on the pin. |

## 7.13 GPIO1x Level/Pulse Control Register – Index 13h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP17_OMODE | R/W | VSB3V | GPIO 17 output mode. 0 – level, 1 – pulse. |
| 6 | GP16_OMODE | R/W | VSB3V | GPIO 16 output mode. 0 – level, 1 – pulse. |
| 5 | GP15_OMODE | R/W | VSB3V | GPIO 15 output mode. 0 – level, 1 – pulse. |
| 4 | GP14_OMODE | R/W | VSB3V | GPIO 14 output mode. 0 – level, 1 – pulse. |
| 3 | GP13_OMODE | R/W | VSB3V | GPIO 13 output mode. 0 – level, 1 – pulse. |
| 2 | GP12_OMODE | R/W | VSB3V | GPIO 12 output mode. 0 – level, 1 – pulse. If this serves as IRQ/SMI# mode, it will have same function. |
| 1 | GP11_OMODE | R/W | VSB3V | GPIO 11 output mode. 0 – level, 1 – pulse. |
| 0 | GP10_OMODE | R/W | VSB3V | GPIO 10 output mode. 0 – level, 1 – pulse. |

## 7.14 GPIO1x Pulse Width Control Register – Index 14h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R/W | VSB3V | Reserved. Read return 0. |
| 1:0 | GP1_PSWDTH[1:0] | R/W | VSB3V | GPIO1x pulse width. If set the GPIO1x to pulse mode, the pulse width can be defined as follows.<br>00b – 500us (Default)<br>01b – 1ms<br>10b – 20ms<br>11b – 100ms |

## 7.15 GPIO1x Pull-up Resistor Control Register – Index 15h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP17_RESON | R/W | VSB3V | Set to 1, turn on the GPIO17 internal pull-up resistor. |
| 6 | GP16_RESON | R/W | VSB3V | Set to 1, turn on the GPIO16 internal pull-up resistor. |
| 5 | GP15_RESON | R/W | VSB3V | Set to 1, turn on the GPIO15 internal pull-up resistor. |
| 4 | GP14_RESON | R/W | VSB3V | Set to 1, turn on the GPIO14 internal pull-up resistor. |
| 3 | Reserved | R/W | VSB3V | |
| 2 | GP12_RESON | R/W | VSB3V | Set to 1, turn on the GPIO12 internal pull-up resistor. If this pin serves as IRQ/SMI#, this bit also control IRQ/SMI# pull-up switch. |
| 1 | GP11_RESON | R/W | VSB3V | Set to 1, turn on the GPIO11 internal pull-up resistor. |
| 0 | GP10_RESON | R/W | VSB3V | Set to 1, turn on the GPIO10 internal pull-up resistor. |

## 7.16 GPIO1x Input De-bounce Register – Index 16h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP17_ENDB | R/W | VSB3V | Enable GPIO17 input de-bounce with 7u or 25ms second that selected by 0x1C bit7. |
| 6 | GP16_ENDB | R/W | VSB3V | Enable GPIO16 input de-bounce with 7u or 25ms second that selected by 0x1C bit6. |
| 5 | GP15_ENDB | R/W | VSB3V | Enable GPIO15 input de-bounce with 7u or 25ms second that selected by 0x1C bit5. |
| 4 | GP14_ENDB | R/W | VSB3V | Enable GPIO14 input de-bounce with 7u or 25ms second that selected by 0x1C bit4. |
| 3 | GP13_ENDB | R/W | VSB3V | Enable GPIO13 input de-bounce with 7u or 25ms second that selected by 0x1C bit3. |
| 2 | GP12_ENDB | R/W | VSB3V | Enable GPIO12 input de-bounce with 7u or 25ms second that selected by 0x1C bit2. |
| 1 | GP11_ENDB | R/W | VSB3V | Enable GPIO11 input de-bounce with 7u or 25ms second that selected by 0x1C bit1. |
| 0 | GP10_ENDB | R/W | VSB3V | Enable GPIO10 input de-bounce with 7u or 25ms second that selected by 0x1C bit0. |

## 7.17 GPIO1x Pulse Inverse Register – Index 17h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP17_PULSINV | R/W | VSB3V | GPIO 17 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. |
| 6 | GP16_PULSINV | R/W | VSB3V | GPIO 16 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. |
| 5 | GP15_PULSINV | R/W | VSB3V | GPIO15 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. |
| 4 | GP14_PULSINV | R/W | VSB3V | GPIO14 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. |
| 3 | GP13_PULSINV | R/W | VSB3V | GPIO13 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. |
| 2 | GP12_PULSINV | R/W | VSB3V | GPIO12 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. If this pin services as IRQ/SMI#, this bit has no effect. |
| 1 | GP11_PULSINV | R/W | VSB3V | GPIO 11 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. |
| 0 | GP10_PULSINV | R/W | VSB3V | GPIO10 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR14. |

## 7.18 GP1X Edge Detector Enable Register – Index 0x18

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | EN_GP17EDGE | R/W | VSB3V | Enable GPIO17 Edge Detector. If this bit set to 1 and GPIO17 set to |

| | | | | |
|---|---|---|---|---|
| | | | | input mode [CR10] will enable GPIO17 edge detection. Default is disable |
| 6 | EN_GP16EDGE | R/W | VSB3V | Enable GPIO16 Edge Detector. If this bit set to 1 and GPIO16 set to input mode [CR10] will enable GPIO16 edge detection. Default is disable |
| 5 | EN_GP15EDGE | R/W | VSB3V | Enable GPIO15 Edge Detector. If this bit set to 1 and GPIO15 set to input mode [CR10] will enable GPIO15 edge detection. Default is disable |
| 4 | EN_GP14EDGE | R/W | VSB3V | Enable GPIO14 Edge Detector. If this bit set to 1 and GPIO14 set to input mode [CR10] will enable GPIO14 edge detection. Default is disable |
| 3 | EN_GP13EDGE | R/W | VSB3V | Enable GPIO13 Edge Detector. If this bit set to 1 and GPIO13 set to input mode [CR10] will enable GPIO13 edge detection. Default is disable |
| 2 | EN_GP12EDGE | R/W | VSB3V | Enable GPIO12 Edge Detector. If this bit set to 1 and GPIO12 set to input mode [CR10] will enable GPIO12 edge detection. Default is disable. If this bit serves as IRQ/SMI#, this bit has no effect. |
| 1 | EN_GP11EDGE | R/W | VSB3V | Enable GPIO11 Edge Detector. If this bit set to 1 and GPIO11 set to input mode [CR10] will enable GPIO11 edge detection. Default is disable |
| 0 | EN_GP10EDGE | R/W | VSB3V | Enable GPIO10 Edge Detector. If this bit set to 1 and GPIO10 set to input mode [CR10] will enable GPIO10 edge detection. Default is disable |

## 7.19 GP1X Edge Detector Status Register – Index 0x19

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | STS_GP17EDGE | RW | VSB3V | Indicate GPIO17 Edge Status. If set to 1, the edge of GPIO17 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. |
| 6 | STS_GP16EDGE | RW | VSB3V | Indicate GPIO16 Edge Status. If set to 1, the edge of GPIO16 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. |
| 5 | STS_GP15EDGE | RW | VSB3V | Indicate GPIO15 Edge Status. If set to 1, the edge of GPIO15 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. |
| 4 | STS_GP14EDGE | RW | VSB3V | Indicate GPIO14 Edge Status. If set to 1, the edge of GPIO14 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. |

| | | | | |
|---|---|---|---|---|
| 3 | STS_GP13EDGE | RW | VSB3V | Indicate GPIO13 Edge Status. If set to 1, the edge of GPIO13 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. |
| 2 | STS_GP12EDGE | RW | VSB3V | Indicate GPIO12 Edge Status. If set to 1, the edge of GPIO12 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. If this bit serves as IRQ/SMI#, this bit has no effect. |
| 1 | STS_GP11EDGE | RW | VSB3V | Indicate GPIO11 Edge Status. If set to 1, the edge of GPIO11 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. |
| 0 | STS_GP10EDGE | RW | VSB3V | Indicate GPIO10 Edge Status. If set to 1, the edge of GPIO10 has occurred. Writing 1 will clear this bit to 0. Writing 0 is invalid. |

## 7.20 GP1X IRQ or SMI# Enable Register – Index 0x1A

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | EN_GP17IRQ | R/W | VSB3V | Enable GPIO17 IRQ or SMI# Generation. If this bit set to 1, enable GPIO17 to generate IRQ or SMI#. |
| 6 | EN_GP16IRQ | R/W | VSB3V | Enable GPIO16 IRQ or SMI# Generation. If this bit set to 1, enable GPIO16 to generate IRQ or SMI#. |
| 5 | EN_GP15IRQ | R/W | VSB3V | Enable GPIO15 IRQ or SMI# Generation. If this bit set to 1, enable GPIO15 to generate IRQ or SMI#. |
| 4 | EN_GP14IRQ | R/W | VSB3V | Enable GPIO14 IRQ or SMI# Generation. If this bit set to 1, enable GPIO14 to generate IRQ or SMI#. |
| 3 | EN_GP13IRQ | R/W | VSB3V | Enable GPIO13 IRQ or SMI# Generation. If this bit set to 1, enable GPIO13 to generate IRQ or SMI#. |
| 2 | EN_GP12IRQ | R/W | VSB3V | Enable GPIO12 IRQ or SMI# Generation. If this bit set to 1, enable GPIO12 to generate IRQ or SMI#. |
| 1 | EN_GP11IRQ | R/W | VSB3V | Enable GPIO11 IRQ or SMI# Generation. If this bit set to 1, enable GPIO11 to generate IRQ or SMI#. |
| 0 | EN_GP10IRQ | R/W | VSB3V | Enable GPIO10 IRQ or SMI# Generation. If this bit set to 1, enable GPIO10 to generate IRQ or SMI#. |

## 7.21 GP1X Output Driving Enable – Index 0x1B

Power-on default [7:0] =0000_1000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | EN_GP17_OBUF | R/W | VSB3V | Enable GPIO17 drive high buffer. If this bit is set to 0, the pin GPIO17 will be I/OD pin, if set to 1 the pin GPIO17 is I/O pin. |
| 6 | EN_GP16_OBUF | R/W | VSB3V | Enable GPIO16 drive high buffer. If this bit is set to 0, the pin GPIO16 will be I/OD pin, if set to 1 the pin GPIO16 is I/O pin. |

| | | | | |
|---|---|---|---|---|
| 5 | EN_GP15_OBUF | R/W | VSB3V | Enable GPIO15 drive high buffer. If this bit is set to 0, the pin GPIO15 will be I/OD pin, if set to 1 the pin GPIO15 is I/O pin. |
| 4 | EN_GP14_OBUF | R/W | VSB3V | Enable GPIO14 drive high buffer. If this bit is set to 0, the pin GPIO14 will be I/OD pin, if set to 1 the pin GPIO14 is I/O pin. |
| 3 | EN_GP13_OBUF | R/W | VSB3V | Enable GPIO13 drive high buffer. If this bit is set to 0, the pin GPIO13 will be I/OD pin, if set to 1 the pin GPIO13 is I/O pin(default). |
| 2 | EN_GP12_OBUF | R/W | VSB3V | Enable GPIO12 drive high buffer. If this bit is set to 0, the pin GPIO12 will be I/OD pin, if set to 1 the pin GPIO12 is I/O pin. |
| 1 | EN_GP11_OBUF | R/W | VSB3V | Enable GPIO11 drive high buffer. If this bit is set to 0, the pin GPIO11 will be I/OD pin, if set to 1 the pin GPIO11 is I/O pin. |
| 0 | EN_GP10_OBUF | R/W | VSB3V | Enable GPIO10 drive high buffer. If this bit is set to 0, the pin GPIO10 will be I/OD pin, if set to 1 the pin GPIO10 is I/O pin. |

## 7.22 GP1X Output Driving Enable – Index 0x1C

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | DB_TIME17_SEL | R/W | VSB3V | Select GPIO17 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 6 | DB_TIME16_SEL | R/W | VSB3V | Select GPIO16 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 5 | DB_TIME15_SEL | R/W | VSB3V | Select GPIO15 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 4 | DB_TIME14_SEL | R/W | VSB3V | Select GPIO14 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 3 | DB_TIME13_SEL | R/W | VSB3V | Select GPIO13 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 2 | DB_TIME12_SEL | R/W | VSB3V | Select GPIO12 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 1 | DB_TIME11_SEL | R/W | VSB3V | Select GPIO11 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 0 | DB_TIME10_SEL | R/W | VSB3V | Select GPIO10 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |

## 7.23 GPIO2x Output Control Register – Index 20h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP27_OCTRL | R/W | VSB3V | GPIO 27 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 6 | GP26_OCTRL | R/W | VSB3V | GPIO 26 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 5 | GP25_OCTRL | R/W | VSB3V | GPIO 25 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 4 | GP24_OCTRL | R/W | VSB3V | GPIO 24 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 3 | GP23_OCTRL | R/W | VSB3V | GPIO 23 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 2 | GP22_OCTRL | R/W | VSB3V | GPIO 22 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 1 | GP21_OCTRL | R/W | VSB3V | GPIO 21 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 0 | GP20_OCTRL | R/W | VSB3V | GPIO 20 output control. Set to 1 for output function. Set to 0 for input function(default). |

## 7.24 GPIO2x Output Data Register – Index 21h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP27_ODATA | R/W | VSB3V | GPIO 27 output data. |
| 6 | GP26_ODATA | R/W | VSB3V | GPIO 26 output data. |
| 5 | GP25_ODATA | R/W | VSB3V | GPIO 25 output data. |
| 4 | GP24_ODATA | R/W | VSB3V | GPIO 24 output data. |

| | | | | |
|---|---|---|---|---|
| 3 | GP23_ODATA | R/W | VSB3V | GPIO 23 output data. |
| 2 | GP22_ODATA | R/W | VSB3V | GPIO 22 output data. |
| 1 | GP21_ODATA | R/W | VSB3V | GPIO 21 output data. |
| 0 | GP20_ODATA | R/W | VSB3V | GPIO 20 output data. |

## 7.25 GPIO2x Input Status Register – Index 22h

Power-on default [7:0] =xxxx_xxxxb

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP27_PSTS | RO | VSB3V | Read the GPIO27 data on the pin. |
| 6 | GP26_PSTS | RO | VSB3V | Read the GPIO26 data on the pin. |
| 5 | GP25_PSTS | RO | VSB3V | Read the GPIO25 data on the pin. |
| 4 | GP24_PSTS | RO | VSB3V | Read the GPIO24 data on the pin. |
| 3 | GP23_PSTS | RO | VSB3V | Read the GPIO23 data on the pin. |
| 2 | GP22_PSTS | RO | VSB3V | Read the GPIO22 data on the pin. |
| 1 | GP21_PSTS | RO | VSB3V | Read the GPIO21 data on the pin. |
| 0 | GP20_PSTS | RO | VSB3V | Read the GPIO20 data on the pin. |

## 7.26 GPIO2x Level/Pulse Control Register – Index 23h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP27_OMODE | R/W | VSB3V | GPIO 27 output mode. 0 – level, 1 – pulse. |
| 6 | GP26_OMODE | R/W | VSB3V | GPIO 26 output mode. 0 – level, 1 – pulse. |
| 5 | GP25_OMODE | R/W | VSB3V | GPIO 25 output mode. 0 – level, 1 – pulse. |
| 4 | GP24_OMODE | R/W | VSB3V | GPIO 24 output mode. 0 – level, 1 – pulse. |
| 3 | GP23_OMODE | R/W | VSB3V | GPIO 23 output mode. 0 – level, 1 – pulse. |
| 2 | GP22_OMODE | R/W | VSB3V | GPIO 22 output mode. 0 – level, 1 – pulse. |
| 1 | GP21_OMODE | R/W | VSB3V | GPIO 21 output mode. 0 – level, 1 – pulse. |
| 0 | GP20_OMODE | R/W | VSB3V | GPIO 20 output mode. 0 – level, 1 – pulse. |

## 7.27 GPIO2x Pulse Width Control Register – Index 24h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R/W | VSB3V | Reserved. Read return 0. |
| 1:0 | GP2_PLSWD[1:0] | R/W | VSB3V | GPIO2x pulse width. If set the GPIO2x to pulse mode, the pulse width can be defined as follows.<br>00b – 500us (Default)<br>01b – 1ms<br>10b – 20ms<br>11b – 100ms |

## 7.28 GPIO2x Pull-up Resistor Control Register – Index 25h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP27_RESON | R/W | VSB3V | Turn on the GPIO27 internal pull-up resistor. |
| 6 | GP26_RESON | R/W | VSB3V | Turn on the GPIO26 internal pull-up resistor. |
| 5 | GP25_RESON | R/W | VSB3V | Turn on the GPIO25 internal pull-up resistor. |
| 4 | GP24_RESON | R/W | VSB3V | Turn on the GPIO24 internal pull-up resistor. |
| 3 | GP23_RESON | R/W | VSB3V | Turn on the GPIO23 internal pull-up resistor. |
| 2 | GP22_RESON | R/W | VSB3V | Turn on the GPIO22 internal pull-up resistor. |
| 1 | GP21_RESON | R/W | VSB3V | Turn on the GPIO21 internal pull-up resistor. |
| 0 | GP20_RESON | R/W | VSB3V | Turn on the GPIO20 internal pull-up resistor. |

## 7.29 GPIO2x Input De-bounce Register – Index 26h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP27_ENDB | R/W | VSB3V | Enable GPIO27 input de-bounce with 7u or 25ms second that selected by 0x2C bit7. |
| 6 | GP26_ENDB | R/W | VSB3V | Enable GPIO26 input de-bounce with 7u or 25ms second that selected |

| | | | | |
|---|---|---|---|---|
| | | | | by 0x2C bit6. |
| 5 | GP25_ENDB | R/W | VSB3V | Enable GPIO25 input de-bounce with 7u or 25ms second that selected by 0x2C bit5. |
| 4 | GP24_ENDB | R/W | VSB3V | Enable GPIO24 input de-bounce with 7u or 25ms second that selected by 0x2C bit4. |
| 3 | GP23_ENDB | R/W | VSB3V | Enable GPIO23 input de-bounce with 7u or 25ms second that selected by 0x2C bit3. |
| 2 | GP22_ENDB | R/W | VSB3V | Enable GPIO22 input de-bounce with 7u or 25ms second that selected by 0x2C bit2. |
| 1 | GP21_ENDB | R/W | VSB3V | Enable GPIO21 input de-bounce with 7u or 25ms second that selected by 0x2C bit1. |
| 0 | GP20_ENDB | R/W | VSB3V | Enable GPIO20 input de-bounce with 7u or 25ms second that selected by 0x2C bit0. |

## 7.30 GPIO2x Pulse Inverse Register – Index 27h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | GP27_PULSINV | R/W | VSB3V | GPIO 27 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR24. |
| 6 | GP26_PULSINV | R/W | VSB3V | GPIO 26 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR24. |
| 5 | GP25_PULSINV | R/W | VSB3V | GPIO25 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR24. |
| 4 | GP24_PULSINV | R/W | VSB3V | GPIO24 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR24. |
| 3 | GP23_PULSINV | R/W | VSB3V | GPIO23 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR24. |
| 2 | GP22_PULSINV | R/W | VSB3V | GPIO22 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in |

| | | | | |
|---|---|---|---|---|
| | | | | CR24. |
| 1 | GP21_PULSINV | R/W | VSB3V | GPIO 21 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR24. |
| 0 | GP20_PULSINV | R/W | VSB3V | GPIO20 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR24. |

## 7.31 GP2x Edge Detector Enable Register – Index 0x28

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | EN_GP27EDGE | R/W | VSB3V | Enable GPIO27 Edge Detector. If this bit set to 1 and GPIO17 set to input mode [CR10] will enable GPIO27 edge detection. Default is disabled. |
| 6 | EN_GP26EDGE | R/W | VSB3V | Enable GPIO26 Edge Detector. If this bit set to 1 and GPIO16 set to input mode [CR10] will enable GPIO26 edge detection. Default is disabled. |
| 5 | EN_GP25EDGE | R/W | VSB3V | Enable GPIO25 Edge Detector. If this bit set to 1 and GPIO15 set to input mode [CR10] will enable GPIO25 edge detection. Default is disabled. |
| 4 | EN_GP24EDGE | R/W | VSB3V | Enable GPIO24 Edge Detector. If this bit set to 1 and GPIO14 set to input mode [CR10] will enable GPIO24 edge detection. Default is disabled. |
| 3 | EN_GP23EDGE | R/W | VSB3V | Enable GPIO23 Edge Detector. If this bit set to 1 and GPIO13 set to input mode [CR10] will enable GPIO23 edge detection. Default is disabled. |
| 2 | EN_GP22EDGE | R/W | VSB3V | Enable GPIO22 Edge Detector. If this bit set to 1 and GPIO12 set to input mode [CR10] will enable GPIO22 edge detection. Default is disabled. |
| 1 | EN_GP21EDGE | R/W | VSB3V | Enable GPIO21 Edge Detector. If this bit set to 1 and GPIO11 set to input mode [CR10] will enable GPIO21 edge detection. Default is disabled. |
| 0 | EN_GP20EDGE | R/W | VSB3V | Enable GPIO20 Edge Detector. If this bit set to 1 and GPIO10 set to input mode [CR10] will enable GPIO20 edge detection. Default is |

| | | | | |
|---|---|---|---|---|
| | | | | disabled. |

## 7.32 GP2X Edge Detector Status Register – Index 0x29

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | STS_GP27EDGE | R/W | VSB3V | Indicate GPIO27 Edge Status. If set to 1, the edge of GPIO27 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 6 | STS_GP26EDGE | R/W | VSB3V | Indicate GPIO26 Edge Status. If set to 1, the edge of GPIO26 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 5 | STS_GP25EDGE | R/W | VSB3V | Indicate GPIO25 Edge Status. If set to 1, the edge of GPIO25 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 4 | STS_GP24EDGE | R/W | VSB3V | Indicate GPIO24 Edge Status. If set to 1, the edge of GPIO24 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 3 | STS_GP23EDGE | R/W | VSB3V | Indicate GPIO23 Edge Status. If set to 1, the edge of GPIO23 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 2 | STS_GP22EDGE | R/W | VSB3V | Indicate GPIO22 Edge Status. If set to 1, the edge of GPIO22 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 1 | STS_GP21EDGE | R/W | VSB3V | Indicate GPIO11 Edge Status. If set to 1, the edge of GPIO21 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 0 | STS_GP20EDGE | R/W | VSB3V | Indicate GPIO10 Edge Status. If set to 1, the edge of GPIO20 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

## 7.33 GP2X IRQ or SMI# Enable Register – Index 0x2A

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | EN_GP27IRQ | R/W | VSB3V | Enable GPIO27 IRQ or SMI# Generation. If this bit set to 1, enable GPIO27 to generate IRQ or SMI#. |
| 6 | EN_GP26IRQ | R/W | VSB3V | Enable GPIO26 IRQ or SMI# Generation. If this bit set to 1, enable GPIO26 to generate IRQ or SMI#. |
| 5 | EN_GP25IRQ | R/W | VSB3V | Enable GPIO25 IRQ or SMI# Generation. If this bit set to 1, enable GPIO25 to generate IRQ or SMI#. |
| 4 | EN_GP24IRQ | R/W | VSB3V | Enable GPIO24 IRQ or SMI# Generation. If this bit set to 1, enable |

| | | | | |
|---|---|---|---|---|
| | | | | GPIO24 to generate IRQ or SMI#. |
| 3 | EN_GP23IRQ | R/W | VSB3V | Enable GPIO23 IRQ or SMI# Generation. If this bit set to 1, enable GPIO23 to generate IRQ or SMI#. |
| 2 | EN_GP22IRQ | R/W | VSB3V | Enable GPIO22 IRQ or SMI# Generation. If this bit set to 1, enable GPIO22 to generate IRQ or SMI#. |
| 1 | EN_GP21IRQ | R/W | VSB3V | Enable GPIO21 IRQ or SMI# Generation. If this bit set to 1, enable GPIO21 to generate IRQ or SMI#. |
| 0 | EN_GP20IRQ | R/W | VSB3V | Enable GPIO20 IRQ or SMI# Generation. If this bit set to 1, enable GPIO20 to generate IRQ or SMI#. |

## 7.34 GP2X Output Driving Enable – Index 0x2B

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | EN_GP27_OBUF | R/W | VSB3V | Enable GPIO27 drive high buffer. If this bit is set to 0, the pin GPIO27 will be I/OD pin, if set to 1 the pin GPIO17 is I/O pin. |
| 6 | EN_GP26_OBUF | R/W | VSB3V | Enable GPIO26 drive high buffer. If this bit is set to 0, the pin GPIO26 will be I/OD pin, if set to 1 the pin GPIO26 is I/O pin. |
| 5 | EN_GP25_OBUF | R/W | VSB3V | Enable GPIO25 drive high buffer. If this bit is set to 0, the pin GPIO25 will be I/OD pin, if set to 1 the pin GPIO25 is I/O pin. |
| 4 | EN_GP24_OBUF | R/W | VSB3V | Enable GPIO24 drive high buffer. If this bit is set to 0, the pin GPIO24 will be I/OD pin, if set to 1 the pin GPIO24 is I/O pin. |
| 3 | EN_GP23_OBUF | R/W | VSB3V | Enable GPIO23 drive high buffer. If this bit is set to 0, the pin GPIO23 will be I/OD pin, if set to 1 the pin GPIO23 is I/O pin. |
| 2 | EN_GP22_OBUF | R/W | VSB3V | Enable GPIO22 drive high buffer. If this bit is set to 0, the pin GPIO22 will be I/OD pin, if set to 1 the pin GPIO22 is I/O pin. |
| 1 | EN_GP21_OBUF | R/W | VSB3V | Enable GPIO21 drive high buffer. If this bit is set to 0, the pin GPIO21 will be I/OD pin, if set to 1 the pin GPIO21 is I/O pin. |
| 0 | EN_GP20_OBUF | R/W | VSB3V | Enable GPIO20 drive high buffer. If this bit is set to 0, the pin GPIO20 will be I/OD pin, if set to 1 the pin GPIO20 is I/O pin. |

## 7.35 GP2X Output Driving Enable – Index 0x2C

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | DB_TIME27_SEL | R/W | VSB3V | Select GPIO27 input de-bounce time. If set to 1 de-bounce time is |

| | | | | |
|---|---|---|---|---|
| | | | | 25ms else if set to 0 de-bounce time is 7u(default). |
| 6 | DB_TIME26_SEL | R/W | VSB3V | Select GPIO26 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 5 | DB_TIME25_SEL | R/W | VSB3V | Select GPIO25 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 4 | DB_TIME24_SEL | R/W | VSB3V | Select GPIO24 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 3 | DB_TIME23_SEL | R/W | VSB3V | Select GPIO23 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 2 | DB_TIME22_SEL | R/W | VSB3V | Select GPIO22 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 1 | DB_TIME21_SEL | R/W | VSB3V | Select GPIO21 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 0 | DB_TIME20_SEL | R/W | VSB3V | Select GPIO20 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |

## 7.36 WDTOUT Control Register – Index 34h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-3 | Reserved | RO | | |
| 2 | SEL_RST_2S | R/W | VSB3V | When set this bit to 1, the WDTOUT10 low pulse width is 2 Sec, if set to 0 the low pulse width is 100ms. |
| 1 | WDTOUT10_OINV | R/W | VSB3V | WDTOUT10# output level inverting. When write 1, the output pin will be inverted. Default is low active when time is out. |
| 0 | STS_WDTOUT10 | R/W | VSB3V | Indicate WDTOUT10 is occurred. Write 1 to clear this bit. Writing 0 is invalid. |

## 7.37 WDTOUT10 Control Register – Index 35h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | WDT10_ENABLE | R/W | VSB3V | Enable WDTOUT10 Output Timer. If set to 1, the WDTOUT10 timer will be started. When WDTOUT10# is asserted, low pulse is occurred. |

| | | | | |
|---|---|---|---|---|
| 6-0 | WD1_PTIME | R/W | VSB3V | WDTOUT10 Pre-counter time in second.<br>000_0000b – 0 second (Default)<br>000_0001b – 1 second<br>000_0010b – 2 seconds<br>:<br>111_1111b – 127 seconds |

## 7.38 Watchdog Timer Control Register – Index 36h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7 | Reserved | RO | VSB3V | Reserved. Read will return 0. |
| 6 | STS_WD_TMOUT | R/W | VSB3V | Watchdog is timeout. When the watchdog is timeout, this bit will be set to one. If set to 1, write 1 will clear this bit. Write 0, no effect. |
| 5 | WD_ENABLE | R/W | VSB3V | Enable watchdog timer. |
| 4 | WD_PULSE | R/W | VSB3V | Watchdog output level or pulse. If set 0 (default), the pin of watchdog is level output. If write 1, the pin will output with a pulse. |
| 3 | WD_UNIT | R/W | VSB3V | Watchdog unit select. Default 0 is select second. Write 1 to select minute. |
| 2 | WD_HACTIVE | R/W | VSB3V | Program WD2 output level. If set to 1 and watchdog asserted, the pin will be high. If set to 0 and watchdog asserted, this pin will drive low(default). |
| 1-0 | WD_PSWIDTH | R/W | VSB3V | Watchdog pulse width selection. If the pin output is selected to pulse mode. The pulse width can be choice.<br>00b – 1m second.<br>01b – 20m second.<br>10b – 100m second<br>11b – 4 second |

The is flexible reset out with watchdog

## 7.39 Watchdog Timer Range Register – Index 37h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-0 | WD_TIME | R/W | VSB3V | Watchdog timing range from 0 ~ 255. The unit is either second or minute programmed by the watchdog timer control register bit3. |

## 7.40 GPIO3x Output Control Register – Index 40h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | GP33_OCTRL | R/W | VSB3V | GPIO 33 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 2 | GP32_OCTRL | R/W | VSB3V | GPIO 32 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 1 | GP31_OCTRL | R/W | VSB3V | GPIO 31 output control. Set to 1 for output function. Set to 0 for input function(default). |
| 0 | GP30_OCTRL | R/W | VSB3V | GPIO 30 output control. Set to 1 for output function. Set to 0 for input function(default). |

## 7.41 GPIO3x Output Data Register – Index 41h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | GP33_ODATA | R/W | VSB3V | GPIO 33 output data. |
| 2 | GP32_ODATA | R/W | VSB3V | GPIO 32 output data. |
| 1 | GP31_ODATA | R/W | VSB3V | GPIO 31 output data. |
| 0 | GP30_ODATA | R/W | VSB3V | GPIO 30 output data. |

## 7.42 GPIO3x Input Status Register – Index 42h

Power-on default [7:0] =xxxx_xxxxb

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | GP33_PSTS | RO | VSB3V | Read the GPIO33 data on the pin. |
| 2 | GP32_PSTS | RO | VSB3V | Read the GPIO32 data on the pin. |
| 1 | GP31_PSTS | RO | VSB3V | Read the GPIO31 data on the pin. |
| 0 | GP30_PSTS | RO | VSB3V | Read the GPIO30 data on the pin. |

## 7.43 GPIO3x Level/Pulse Control Register – Index 43h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | GP33_OMODE | R/W | VSB3V | GPIO 33 output mode. 0 – level, 1 – pulse. |
| 2 | GP32_OMODE | R/W | VSB3V | GPIO 32 output mode. 0 – level, 1 – pulse. |
| 1 | GP31_OMODE | R/W | VSB3V | GPIO 31 output mode. 0 – level, 1 – pulse. |
| 0 | GP30_OMODE | R/W | VSB3V | GPIO 30 output mode. 0 – level, 1 – pulse. |

## 7.44 GPIO3x Pulse Width Control Register – Index 44h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7:2 | Reserved | R/W | VSB3V | Reserved. Read return 0. |
| 1:0 | GP3_PLSWD[1:0] | R/W | VSB3V | GPIO3x pulse width. If set the GPIO3x to pulse mode, the pulse width can be defined as follows.<br>00b – 500us (Default)<br>01b – 1ms<br>10b – 20ms<br>11b – 100ms |

## 7.45 GPIO3x Input De-bounce Register – Index 46h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | GP33_ENDB | R/W | VSB3V | Enable GPIO33 input de-bounce with 7u or 25ms second that selected by 0x4C bit3. |
| 2 | GP32_ENDB | R/W | VSB3V | Enable GPIO32 input de-bounce with 7u or 25ms second that selected by 0x4C bit2. |
| 1 | GP31_ENDB | R/W | VSB3V | Enable GPIO31 input de-bounce with 7u or 25ms second that selected by 0x4C bit1. |
| 0 | GP30_ENDB | R/W | VSB3V | Enable GPIO30 input de-bounce with 7u or 25ms second that selected by 0x4C bit0. |

## 7.46 GPIO3x Pulse Inverse Register – Index 47h

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | GP33_PULSINV | R/W | VSB3V | GPIO33 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44. |
| 2 | GP32_PULSINV | R/W | VSB3V | GPIO32 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44. |
| 1 | GP31_PULSINV | R/W | VSB3V | GPIO 31 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44. |
| 0 | GP30_PULSINV | R/W | VSB3V | GPIO30 Pulse inversed. If the pulse inverse is selected, the output pulse is high pulse. Default low pulse. The pulse width is defined in CR44. |

## 7.47 GP3x Edge Detector Enable Register – Index 0x48

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | EN_GP33EDGE | R/W | VSB3V | Enable GPIO33 Edge Detector. If set to 1, enable GPIO33 edge detection. Default is disable. |
| 2 | EN_GP32EDGE | R/W | VSB3V | Enable GPIO32 Edge Detector. If set to 1, enable GPIO32 edge detection. Default is disable. |
| 1 | EN_GP31EDGE | R/W | VSB3V | Enable GPIO31 Edge Detector. If set to 1, enable GPIO31 edge detection. Default is disable. |
| 0 | EN_GP30EDGE | R/W | VSB3V | Enable GPIO30 Edge Detector. If set to 1, enable GPIO30 edge detection. Default is disable. |

## 7.48 GP3X Edge Detector Status Register – Index 0x49

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | STS_GP33EDGE | R/W | VSB3V | Indicate GPIO33 Edge Status. If set to 1, the edge of GPIO33 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 2 | STS_GP32EDGE | R/W | VSB3V | Indicate GPIO32 Edge Status. If set to 1, the edge of GPIO32 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 1 | STS_GP31EDGE | R/W | VSB3V | Indicate GPIO31 Edge Status. If set to 1, the edge of GPIO31 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |
| 0 | STS_GP30EDGE | R/W | VSB3V | Indicate GPIO10 Edge Status. If set to 1, the edge of GPIO30 has occurred. Write 1 to clear this bit. Writing 0 is invalid. |

## 7.49 GP3X IRQ or SMI# Enable Register – Index 0x4A

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | EN_GP33IRQ | R/W | VSB3V | Enable GPIO33 IRQ or SMI# Generation. If this bit set to 1, enable GPIO33 to generate IRQ or SMI#. |
| 2 | EN_GP32IRQ | R/W | VSB3V | Enable GPIO32 IRQ or SMI# Generation. If this bit set to 1, enable GPIO32 to generate IRQ or SMI#. |
| 1 | EN_GP31IRQ | R/W | VSB3V | Enable GPIO31 IRQ or SMI# Generation. If this bit set to 1, enable GPIO31 to generate IRQ or SMI#. |
| 0 | EN_GP30IRQ | R/W | VSB3V | Enable GPIO30 IRQ or SMI# Generation. If this bit set to 1, enable GPIO30 to generate IRQ or SMI#. |

## 7.50 GP3X Output Driving Enable – Index 0x4C

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-4 | Reserved | RO | VSB3V | Read back will be zero |
| 3 | DB_TIME33_SEL | R/W | VSB3V | Select GPIO33 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 2 | DB_TIME32_SEL | R/W | VSB3V | Select GPIO32 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |

| | | | | |
|---|---|---|---|---|
| 1 | DB_TIME31_SEL | R/W | VSB3V | Select GPIO31 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |
| 0 | DB_TIME30_SEL | R/W | VSB3V | Select GPIO30 input de-bounce time. If set to 1 de-bounce time is 25ms else if set to 0 de-bounce time is 7u(default). |

## 7.51 CHIPID(1) Register – Index 5Ah

Power-on default [7:0] =0000_0011b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-0 | CHIPID | RO | VSB3V | Chip ID, High byte (8'h03). |

## 7.52 CHIPID(2) Register – Index 5Bh

Power-on default [7:0] =0000_0000b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-0 | CHIPID | RO | VSB3V | Chip ID, Low byte (8'h00). |

## 7.53 VENDOR ID(1) Register – Index 5Dh

Power-on default [7:0] =0001_1001b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-0 | VENDOR1 | RO | VSB3V | Vendor ID, 8'h19 |

## 7.54 VENDOR ID(2) Register – Index 5Eh

Power-on default [7:0] =0011_0100b

| Bit | Name | R/W | PWR | Description |
|---|---|---|---|---|
| 7-0 | VENDOR2 | RO | VSB3V | Vendor ID, 8h34 |

# 8. Electron Characteristic

## 8.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage | -0.5 to 4.0 | V |
| Input Voltage | -0.5 to 5.5 | V |
| Operating Temperature | -20 to +85 | ° C |
| Storage Temperature | -55 to +150 | ° C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 8.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V) (Note)

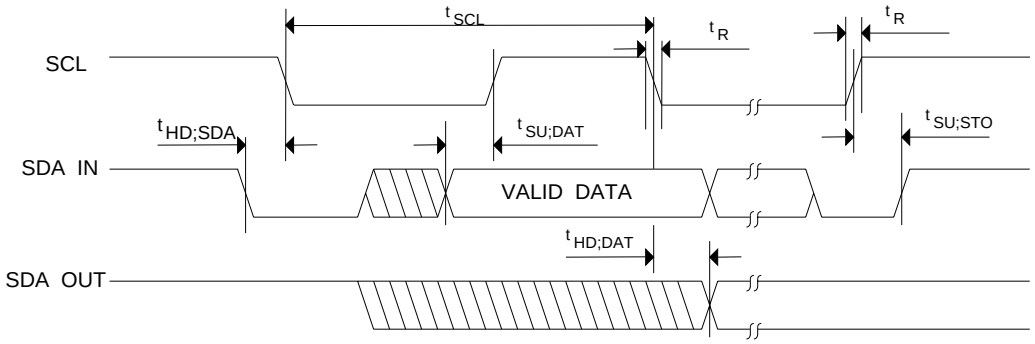
| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **$I/O_{12t}$ - TTL level bi-directional pin with source-sink capability of 12 mA** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Output Low Current | IOL | 10 | 12 | | mA | VOL = 0.4V |
| Output High Current | IOH | | -12 | -10 | mA | VOH = 2.4V |
| Input High Leakage | ILIH | | | +2 | μA | VIN = VDD |
| Input Low Leakage | ILIL | | | -2 | μA | VIN = 0V |
| **$I/O_{12ts}$ - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input** | | | | | | |
| Input Low Threshold Voltage | Vt- | 0.5 | 0.8 | 1.1 | V | VDD = 3.3 V |
| Input High Threshold Voltage | Vt+ | 1.6 | 2.0 | 2.4 | V | VDD = 3.3 V |
| Output Low Current | IOL | 10 | 12 | | mA | VOL = 0.4 V |
| Output High Current | IOH | | -12 | -10 | mA | VOH = 2.4V |
| Input High Leakage | ILIH | | | +2 | μA | VIN = VDD |
| Input Low Leakage | ILIL | | | -2 | μA | VIN = 0V |

8.2 DC Characteristics, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **$OUT_{12t}$ - TTL level output pin with source-sink capability of 12 mA** | | | | | | |
| Output Low Current | IOL | 12 | 16 | | mA | VOL = 0.4V |
| Output High Current | IOH | | -14 | -12 | mA | VOH = 2.4V |
| **$OD_8$ - Open-drain output pin with sink capability of 8 mA** | | | | | | |
| Output Low Current | IOL | 6 | 8 | | mA | VOL = 0.4V |
| **$OD_{16}$ - Open-drain output pin with sink capability of 16 mA** | | | | | | |
| Output Low Current | IOL | 12 | 16 | | mA | VOL = 0.4V |
| **$I/OOD_{16ts}$ - TTL level bi-directional pin, can select to OD or OUT by register, with 16 mA source-sink capability** | | | | | | |
| Input Low Threshold Voltage | Vt- | 0.5 | 0.8 | 1.1 | V | VDD = 3.3 V |
| Input High Threshold Voltage | Vt+ | 1.6 | 2.0 | 2.4 | V | VDD = 3.3 V |
| Output Low Current | IOL | 6 | 8 | | mA | VOL = 0.4 V |
| Output High Current | IOH | | -16 | -12 | mA | VOH = 2.4V |
| Input High Leakage | ILIH | | | +2 | μA | VIN = VDD |
| Input Low Leakage | ILIL | | | -2 | μA | VIN = 0V |
| **$IN_t$ - TTL level input pin** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Input High Leakage | ILIH | | | +2 | μA | VIN = VDD |
| Input Low Leakage | ILIL | | | -2 | μA | VIN = 0 V |
| **$IN_{ts}$ - TTL level Schmitt-triggered input pin** | | | | | | |
| Input Low Threshold Voltage | Vt- | 0.5 | 0.8 | 1.1 | V | VDD = 3.3V |
| Input High Threshold Voltage | Vt+ | 1.6 | 2.0 | 2.4 | V | VDD = 3.3V |
| Input High Leakage | ILIH | | | +2 | μA | VIN = VDD |
| Input Low Leakage | ILIL | | | -2 | μA | VIN = 0 V |

Note: All parameters tested at specific temperature. Specifications over temperature are guaranteed by design.

## 8.3 AC Characteristics




Serial Bus Timing Diagram

**Serial Bus Timing**

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| SCL clock period | $t_{SCL}$ | 2.5 | | uS |
| Start condition hold time | $t_{HD;SDA}$ | 0.6 | | uS |
| Stop condition setup-up time | $t_{SU;STO}$ | 0.6 | | uS |
| DATA to SCL setup time | $t_{SU;DAT}$ | 120 | | nS |
| DATA to SCL hold time (data input) | $t_{HD;DAT}$ | 5 | | nS |
| SCL and SDA rise time | $t_R$ | | 1.0 | uS |
| SCL and SDA fall time | $t_F$ | | 300 | nS |

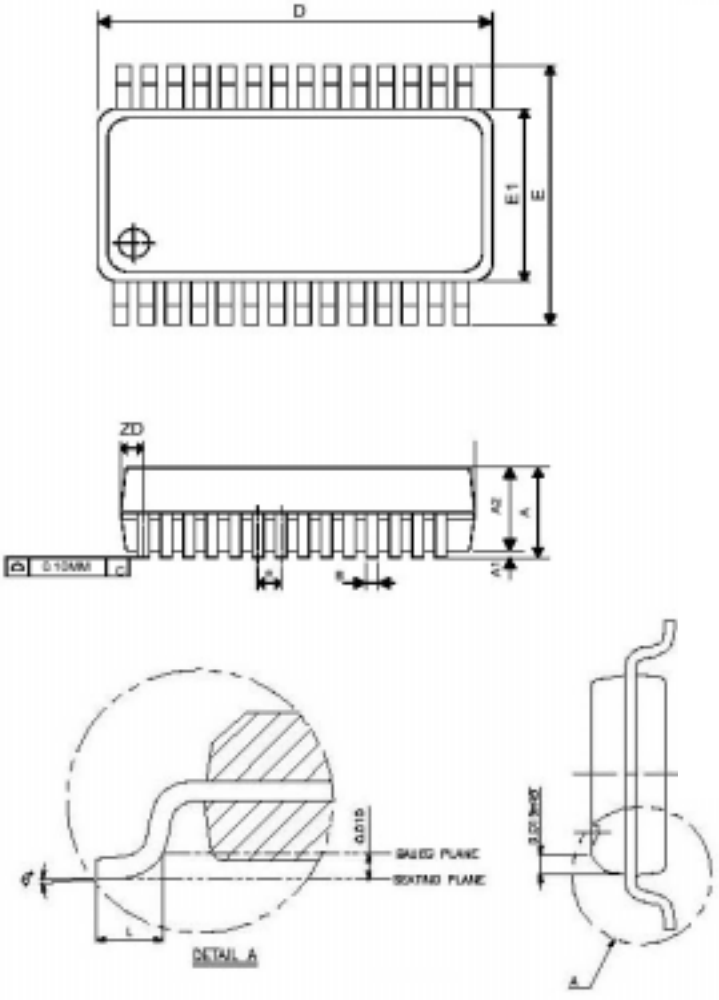
Note : Timing spec. guaranteed by design

# 9. Ordering Information

| Part Number | Package Type | Production Flow |
|---|---|---|
| **F75111R** | 28 PIN SSOP | Commercial, 0°C to +70°C |
| **F75111RG** | 28 PIN SSOP(Green Package) | |
| **F75111N** | 24 PIN QFN (Green Package) | Commercial, 0°C to +70°C |

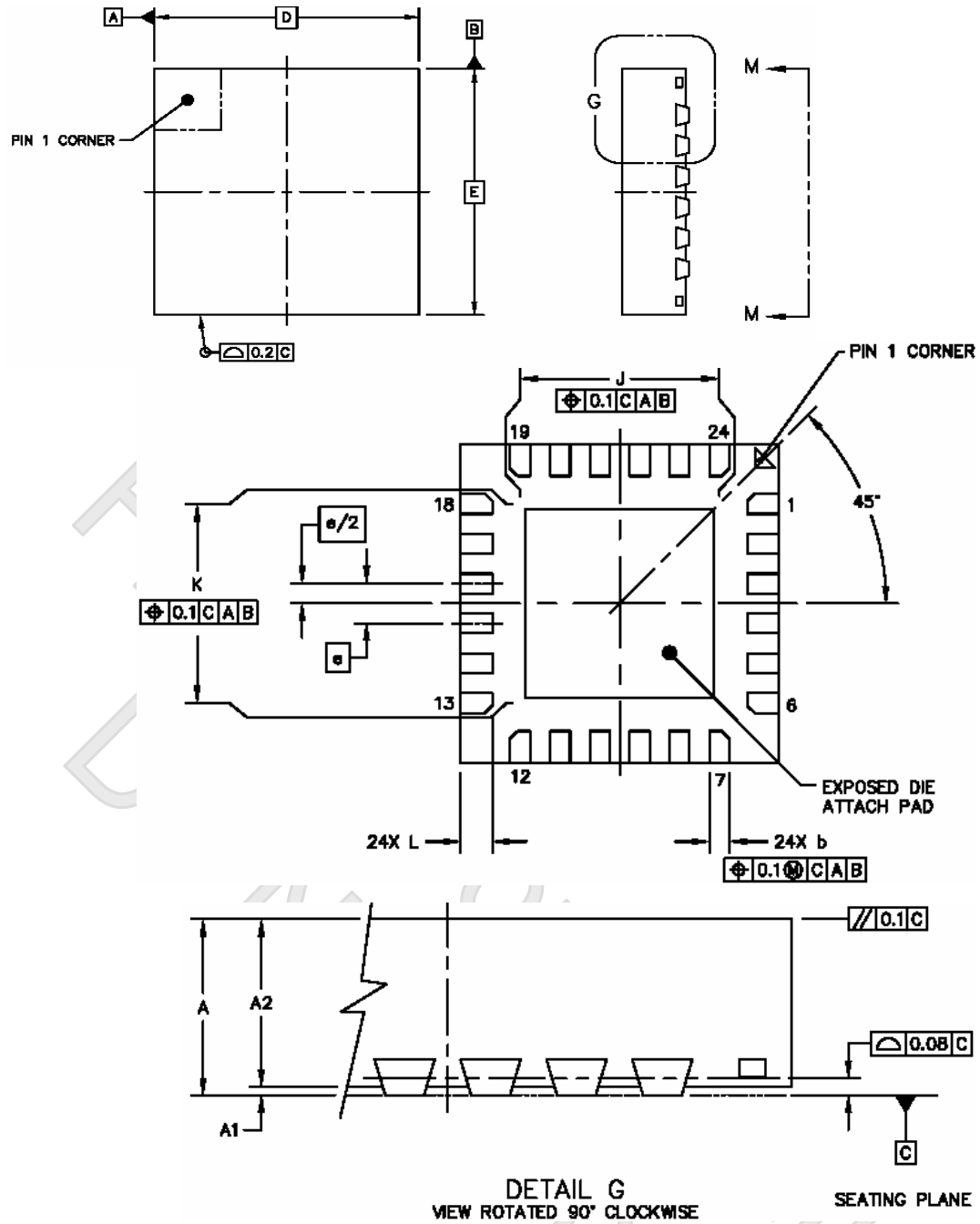
# 10. Package Dimensions

**F75111R/RG 28SSOP(150mil)**




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.35 | 1.63 | 1.75 | 0.053 | 0.064 | 0.069 |
| A1 | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| A2 | | | 0.50 | | | 0.059 |
| B | 0.20 | | 0.30 | 0.008 | | 0.012 |
| c | 0.18 | | 0.25 | 0.007 | | 0.010 |
| e | 0.635 BASIC | | | 0.025BASIC | | |
| D | 9.80 | 9.91 | 10.01 | 0.386 | 0.390 | 0.394 |
| E | 5.79 | 5.99 | 6.20 | 0.228 | 0.236 | 0.244 |
| E1 | 3.81 | 3.91 | 3.99 | 0.150 | 0.154 | 0.157 |
| L | 0.41 | 0.635 | 1.27 | 0.016 | 0.025 | 0.050 |
| H | 0.25 | | 0.50 | 0.010 | | 0.020 |
| ZD | 0.838 REF | | | 0.033 REF | | |
| θ | $0^0$ | | $8^0$ | $0^0$ | | $8^0$ |

## F75111N 24QFN(4mm x 4mm)




| DIM | MIN | NOM | MAX | NOTES |
|---|---|---|---|---|
| A | 0.8 | 0.9 | 1 | 1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD. |
| A1 | 0 | | 0.05 | |
| A2 | 0.8 | | 0.95 | |
| b | 0.18 | 0.25 | 0.3 | |
| D | | 4 BSC | | |
| E | | 4 BSC | | |
| e | | 0.5 BSC | | |
| J | 2.32 | | 2.42 | |
| K | 2.32 | | 2.42 | |
| L | 0.3 | 0.4 | 0.55 | |

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